HIGH-SIGMA PERFORMANCE ANALYSIS USING MULTI-OBJECTIVE EVOLUTIONARY ALGORITHMS

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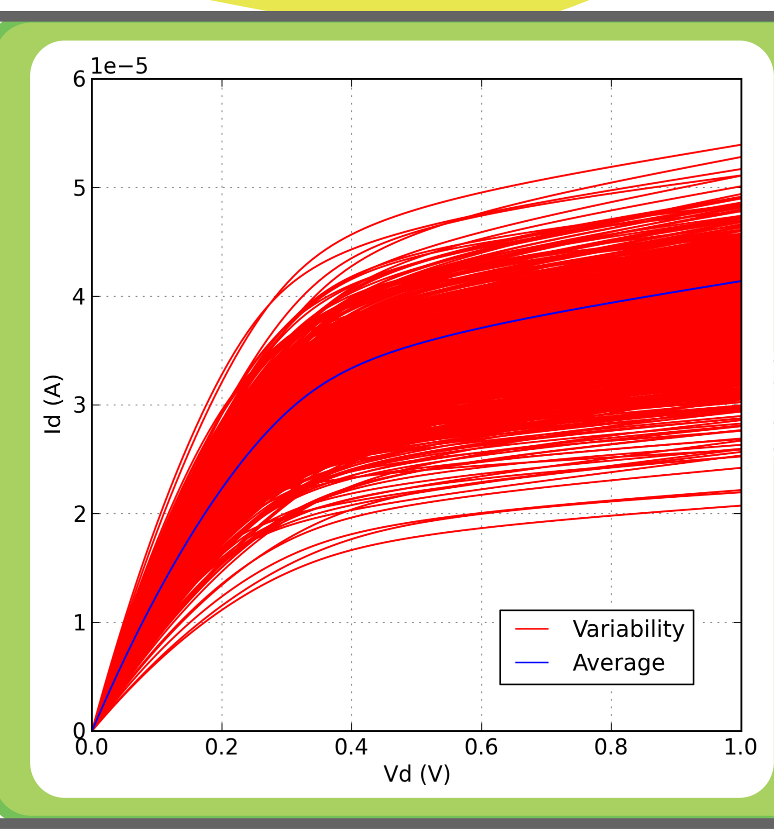
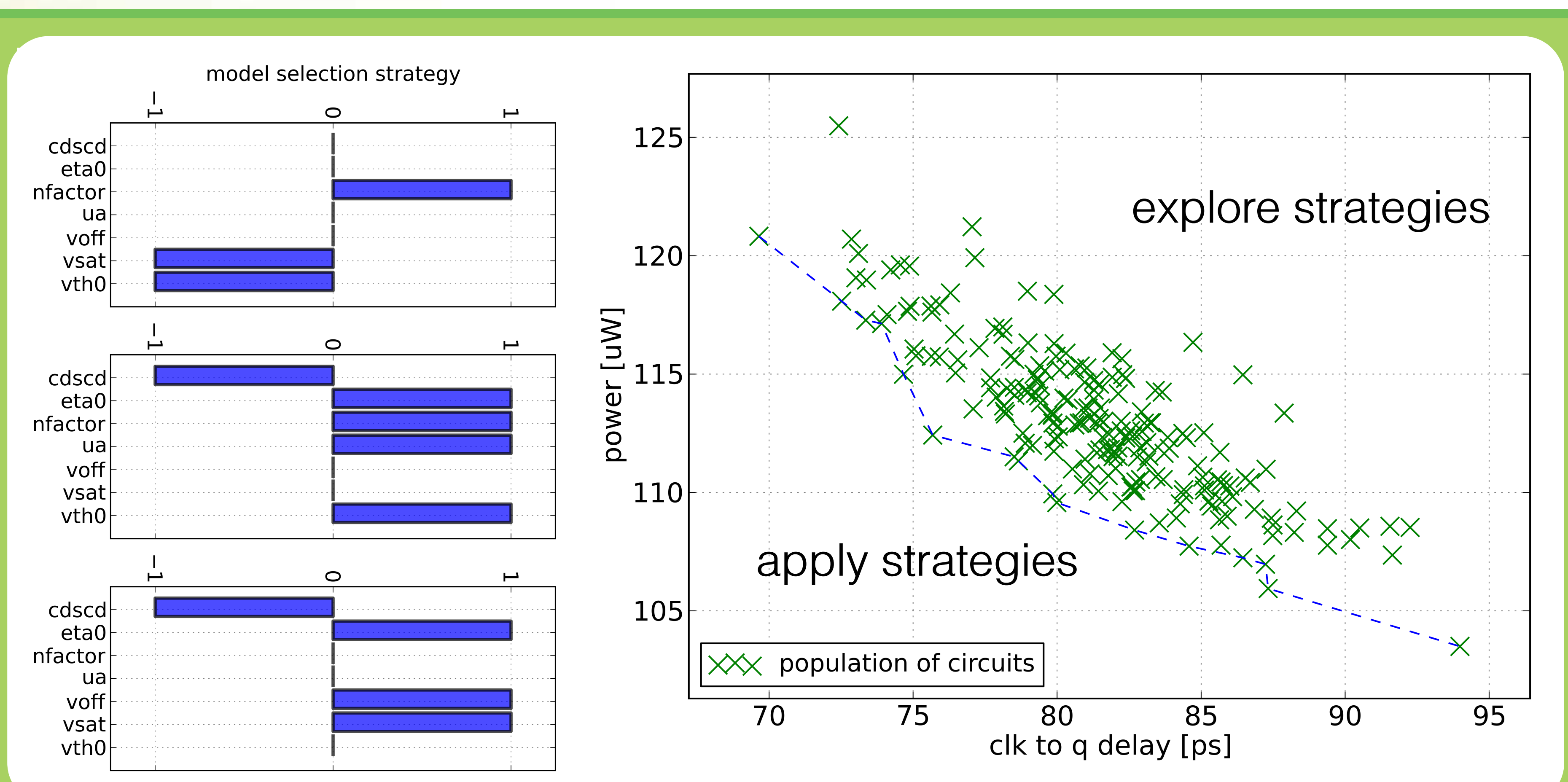
Introduction

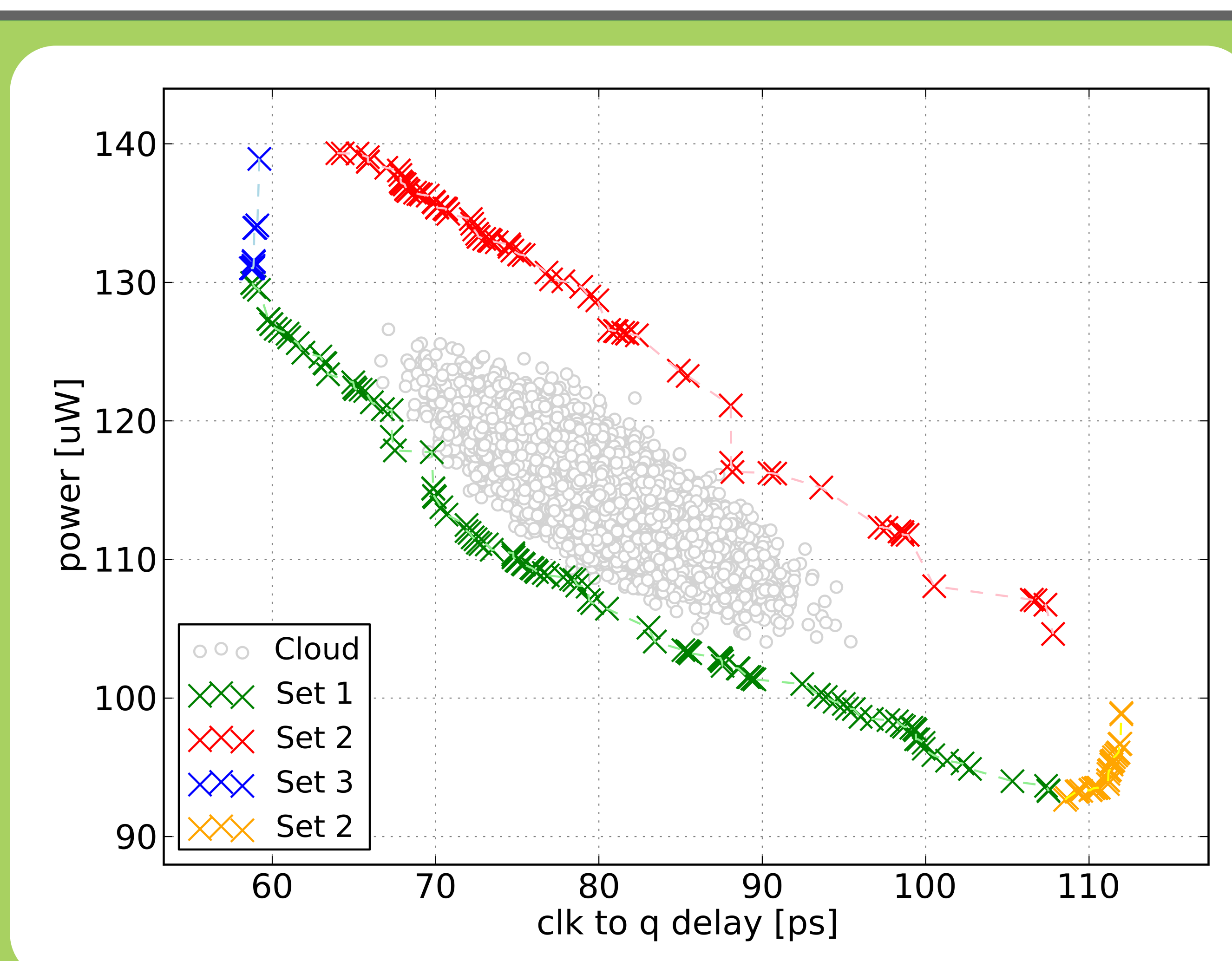
Semiconductor devices have rapidly improved in performance and function density over the past 25 years enabled by the continuous shrinking of technology feature sizes. Fabricating transistors that small, even with advanced processes, results in structural irregularities at the atomic scale, which affect device characteristics in a random manner. To simulate performance of circuits comprising a large number of devices using statistical models and ensuring low failure rates, performance outliers are required to be investigated. Standard Monte Carlo analysis will quickly become intractable because of the large number of circuit simulations required. Cases where the number of samples exceeds 10^6 are known as high-sigma problems. This work proposes a high-sigma sampling methodology based on multi-objective optimisation using evolutionary algorithms. A D-type Flip Flop is presented as a case study and it is shown that higher sigma outliers can be reached using a similar number of SPICE evaluations as Monte Carlo analysis.



Methodology

A multi-objective evolutionary algorithm (MOEA) is used in this work for design optimisation, which is based on NSGA-II. The distinctive feature of the proposed method is that an indirect encoding of the model parameters of each transistor is used, i.e. rather than randomly sampling from a probability distribution of a specific model parameter a *sampling strategy* for each device is optimised. In this case the strategies to chose from are simple: '-1' represents *chose a model card with this parameter value smaller than the current one*, '+1' represents *chose a model card with this parameter value larger than the current one* and '0' means *retain the current parameter value (model card)*. Device model cards are retrieved from a database of 10,000 PMOS and NMOS transistor model cards, respectively, which are generated using GSS's RandomSpice2 tool. The optimisation algorithm's goal is to find model card selection strategies specific to every transistor in a circuit, which guide the search as quickly as possible to the tails of the performance distribution.

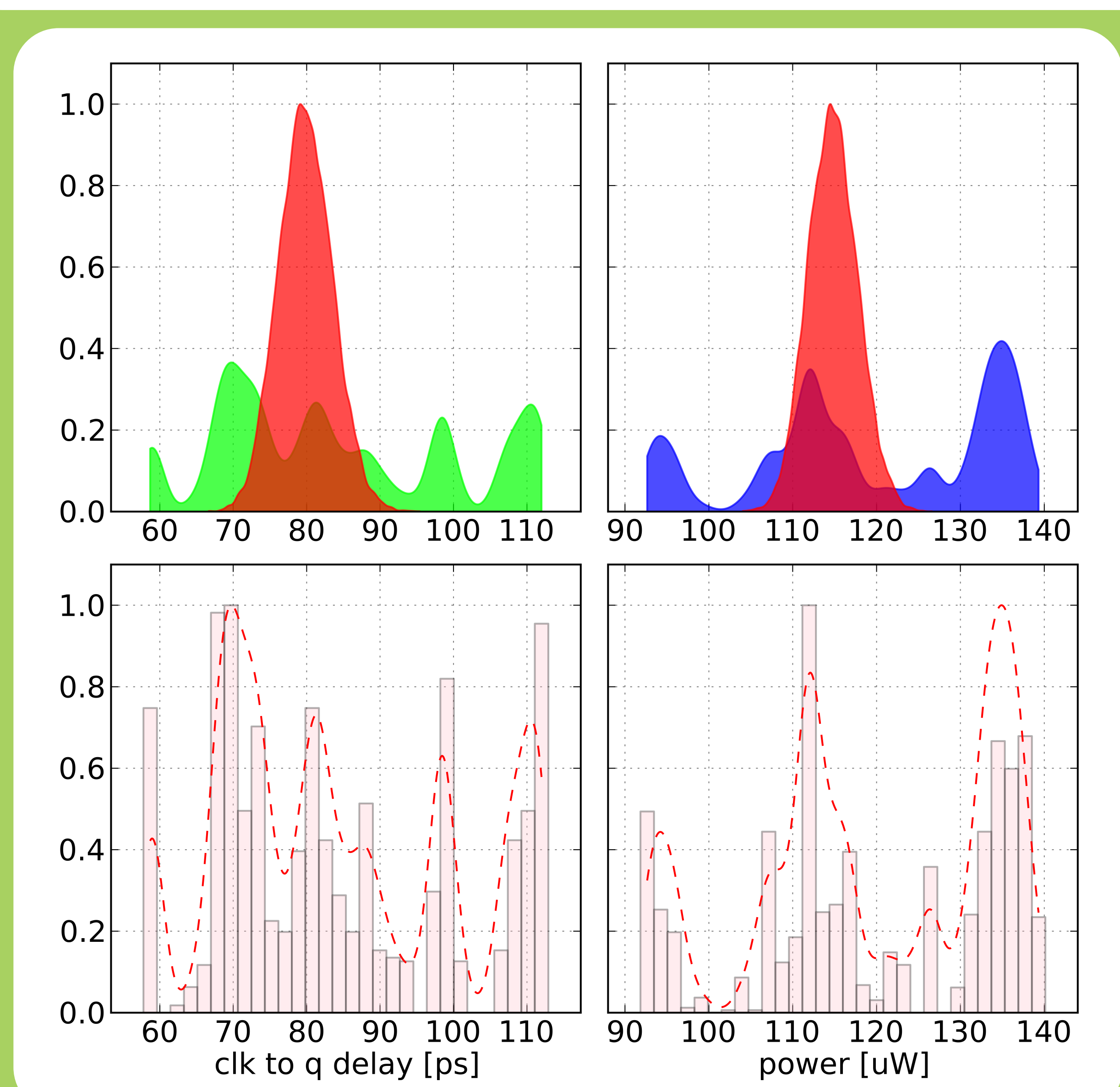




Case Study: D-Type Flip Flop

A DFF is used as a case study. For comparison with the proposed high-sigma sampling method, 20,000 samples of the DFF are randomly generated measuring delay and dynamic power consumption using SPICE. The density, shape and spread of the point cloud illustrates the resulting variability distributions. Also shown are the results of the high-sigma sampling performance of the proposed MOGA-based approach. The four quadrants shown in the figure on the top left have been tackled in four runs amounting to a total of 40,000 SPICE runs. The distance of samples from the mean could be doubled in all directions using only twice as many SPICE runs than MC. For comparison, using standard MC to get to the same sigma range would require up to 2 million SPICE runs.

In this initial work we have only considered V_{th} in the optimisation process, making the problem simpler. However, the full parameter range of GSS model cards with correct model correlations was used and it is promising to see that considering V_{th} alone seems to yield significantly better results than standard MC analysis already.



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