The University Of Sheffield.

SIMULATION STUDY OF SILICON CARBIDE CLUSTERED INSULATED GATE BIPOLAR TRANSISTOR (CIGBT)

by

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TABLE OF CONTENTS

LIST OF SYMBOLS AND TERMS

AC / DC	Alternating Current / Direct Current
HVDC	High Voltage Direct Current
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IGBT	Insulated Gate Bipolar Transistor
MOS	Metal Oxide Semiconductor
SiC	Silicon Carbide
Si	Silicon
CIGBT	Clustered Insulated Gate Bipolar Transistor
TCIGBT	Trench Clustered Insulated Gate Bipolar Transistor
TIGBT	Trench Insulated Gate Bipolar Transistor
GaN	Gallium Nitride
GaAs	Gallium Arsenide
WBG	Wide Band Gap
W	Thickness of cell
$R_{on\text{-}sp}$	Specific On-Resistance
SBD	Schottky Barrier Diode
JFET	Junction Field Effect Transistor
JBS	Junction Breadown Schottky
BV	Breakdown Voltage
ϵ_S	Dielectric permittivity of Silicon
E_c	Critical Electrical Field/ Breakdown electric Field
E_g	Band Gap Energy
N_i	Intrinsic carrier concentration
μ_p	Mobilty of Holes
μ_n	Electron Mobility
V_{sat}	Carrier Saturatin Velocity
V_i	Built-in potential
K	Dielectric Constant
ϵ_r	Relative permitivity
J_p	Hole current Density
J_n	Electron Current Density
J_{tot}	Total Current Density
D_p	Hole diffusion coefficient
D_n	Electron Diffusion coefficient
q	Electron Charge
V_F	Forward Voltage
k	Boltzmann Constant
W_N	Drift depth
R_{ch}	Channel Resistance
n_0	Electron concentration at the anode side
n_w	Electron concentration below the P base
SJ	Super Junction
eV	Electron Volt
ρ	Resistivity
τ_n	Electron Lifetime
τ_n	Hole Lifetime

ABSTRACT

Power semiconductor devices are inevitable parts of a power electronic converter system, with nearly 50% of electricity used in the world controlled by them. Silicon power devices have been used in power systems ever since the vacuum tubes were replaced by them in the 1950s. The performance of devices in a circuit is decided by the switching strategies and the inherent device performance like its on-state voltage, turn-on and turn-off times and hence their losses. Due to their inherent material properties, the growing interest in wide band gap devices is in applications beyond the limits of Si or GaAs. SiC is a wide bandgap material with properties that make it an attractive alternative to Silicon for high power applications.

Silicon Insulated Gate Bipolar Transistor (IGBT) is the most favourable device in the industry today for medium/high power applications. Silicon Clustered Insulated Gate Bipolar Transistor (CIGBT) is experimentally proven to demonstrate better performance as compared to their IGBT counterparts. In this work, the theoretical limit of silicon CIGBT is studied in great detail and compared to previously predicted IGBT limit. Later part of this thesis would explain the design and optimization of CIGBT in 4H- SiC. An in-depth simulation study of the same device is performed for both static and dynamic characteristics. Both planar and trench gate CIGBT devices are discussed here along with possible fabrication process. Along with this, a comparison study between CIGBT with its equivalent IGBT in SiC is also performed through extensive 2D simulations in MEDICI^{TM} in terms of their static and dynamic characteristics. Finally, a comparative study of P channel and N channel SiC CIGBT devices is evaluated through simulations.

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Special thanks to **Dr. Luther-King Ngwendson, Dr. Mark Sweet** and **Dr. Graham Bruce** for their invaluable guidance and time extended to me during this research.

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Chapter 1:

Introduction

Power electronics in simple definition includes electronics involved in the conversion and control of electric power efficiently. Electrical energy has to be transformed from one form to another starting from solar (photovoltaic) cells/wind turbines to electrical consumers. Be it AC to DC voltage conversion or high frequency supplies (such as wind turbine) to constant lower frequency conversion (such as for the grid, 50Hz despite fluctuating wind conditions), all require power electronics. Power electronics ranges from a few milliWatts such as in heart pacemakers or mobile phones to several Gigawatts such as in Automotive, HVDC applications. Similar to microelectronics that deals with processing information, power electronics deals with processing energy.

Power electronics are employed in diverse fields like analog circuits, power electronic devices, power converter systems, control systems, electric machines etc. Power semiconductor devices are inevitable parts of a power electronic system, with nearly 50% of electricity used in the world controlled by them. Hence the efficiency and cost-effectiveness of these devices is of concern to all engineers. Just as in microelectronics, power electronic devices are also fabricated using the same doping, lithography and other methods to make a wafer. However unlike microelectronics, large-scale monolithic integration of power electronics in a single chip is not feasible due to increased cost of manufacture and other issues such as cross-talk and isolation hence hybrid integration with packaging and interconnection methods play a significant role. Silicon power devices have been used in power systems ever since the vacuum tubes were replaced by them in the 1950s. Bipolar

devices were first developed around the same time[1] and ever since research has been focussed on improving the power density of devices. MOSFETs were developed during the 1970s and are used till date as they have high input impedance and can operate at high frequencies. These are however limited to low voltage and high frequency application owing to their high on-resistance. The introduction of Insulated Gate Bipolar Transistor (IGBT) combining both MOS and bipolar characteristics attracted for its use in the medium power electronic applications. These devices are integral part of power electronic converters and are responsible for energy transfers. Hence the performance of these devices has to be optimised in order to reduce the losses in the system to the minimum. The performance of devices in a circuit is decided by the switching strategies and also the inherent device performance like its on-state voltage, turn-on and turn-off times and hence their losses. As the rating of these converters increases, it will be more prone to short-circuits and fluctuations hence the device tolerance under such transient conditions is of concern. In the modern world, high frequency applications of these converters are increasingly on demand. The power supply size is continually being miniaturised and hence an increase in power density is sought after.

1.1 Why SiC devices?

The growing interest in wide band gap devices is in applications beyond the limits of Si or GaAs. Wide Band Gap (WBG) semiconductors were first studied in 1970s when the relation of Breakdown Electric Field and energy bandgap was understood. A large bandgap (2.5eV – 6.2eV) means that it is more difficult to thermally excite electrons from valence to conduction band. This causes a drastic reduction in leakage currents in a device and also an improved high temperature performance.

SiC, GaN and diamond are regarded as promising wide band gap materials studied. Table 1.1 shows a comparison of electrical characteristics of these WBG materials with Si.

Table 1.1 Comparison of material properties between Si, GaN, SiC and Diamond.

	Silicon	GaN	SiC	Diamond
Bandgap Energy (eV)	1.1	3.5	>3	5.5
Electric Field Breakdown (MV/cm)	0.3	3.0	3.0	10
Melting Temp (°C)	1700	2500	3100	3550
Thermal Conductivity (W/cmK)	1.5	1.5	3.7	20

Eq.[1] shows the specific on-resistance of a unipolar device. According to the Eq.[1] one can estimate that on-resistance of a power device is inversely proportional to the cube of critical electric field(E_C^3) of the semiconductor material. E_c is defined as the maximum voltage the material can withstand per unit length above which it leads to breakdown leading to increase in current.

$$R_{on,sp} = \frac{4BV^2}{\mu_n \epsilon_S E_C^3} \qquad \text{Eq.[1]}$$

Hence it is clearly understood that, WBG devices having a higher critical electric field, can reduce the on-resistance considerably at a particular voltage rating compared to Si. Higher thermal conductivity and higher thermal stability of these materials can reduce the cooling requirements of the systems. Using these devices in power systems also means reduction of size and weight in systems as they support higher power density and also support high frequency and high temperature operation.

Table 1.2: Electrical Properties of Silicon and WBG materials (@300K)

Property	Silicon	GaN	3C-SiC	4H-SiC	Diamond
E_g (eV)	1.1	3.4	2.3	3.26	5.6
n_i (cm^{-3})	1.50E+10	1.90E-10	8E-10	8.20E-10	1E-27
μ_n (cm^2/Vs)	1,500	1,250	800	950	2200
μ_p (cm^2/Vs)	600	250	320	120	1600
E_c (MV/cm)	0.3	3.0	1	3.0	5.0
V_{sat} (cm/sec)	1.00E+07	2.20E+07	2.50E+07	2.00E+07	2.7E+07
κ (W/cm-K)	1.5	1.3	3.6	3.7	>20
ε_r	11.8	9	9.6	9.7	5.0

It can be clearly seen from table 1.1 SiC material posses' superior electrical properties (as highlighted in the table) when compared to Si and this is useful in power electronics in many ways, a few of which are described below.

- High breakdown electric field (E_c)
    - Support High voltage rated devices with thinner drift regions
- High Thermal conductivity, larger bandgap and low intrinsic concentration.
    - Supports High temperature operation and produces lower leakage currents.
- Low Intrinsic Concentration (n_i)
    - Lower leakage currents, higher temperature operation.
- Higher carrier saturation Velocity (V_{sat})
    - Higher switching speeds.
- Lower Dielectric Constant (κ)
    - Lower *capacitance leading to lower RC time constant.*

Due to these properties, a lot of research is being focussed presently on SiC devices. They are more rugged under heat and radiation and render a better performance without degrading their electrical properties. The physical properties of Si pose fundamental limitations to performance at higher voltage/power. SiC with the inherent properties mentioned above are believed to achieve performance beyond where Si reaches its limit. However it is worth noting that electron mobility (μ_n) in SiC is lower than in Si (see table 1.1) and it is claimed that SiC unipolar devices will have 400X lower specific on-resistance than an equivalent Si device [2].

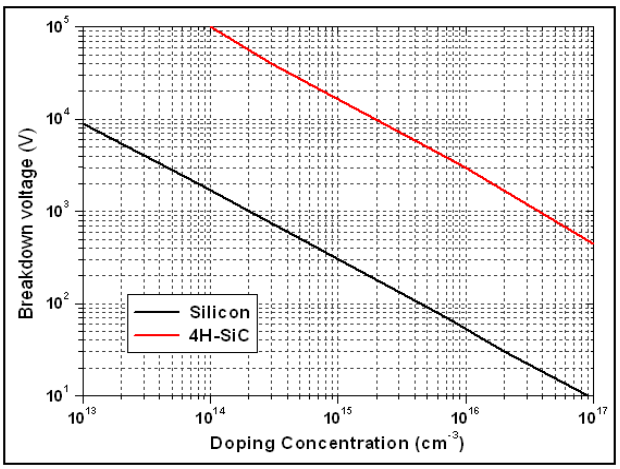


Fig 1.1. Comparison of ideal blocking voltage of p+n diode vs. background doping of Si and SiC devices[2]

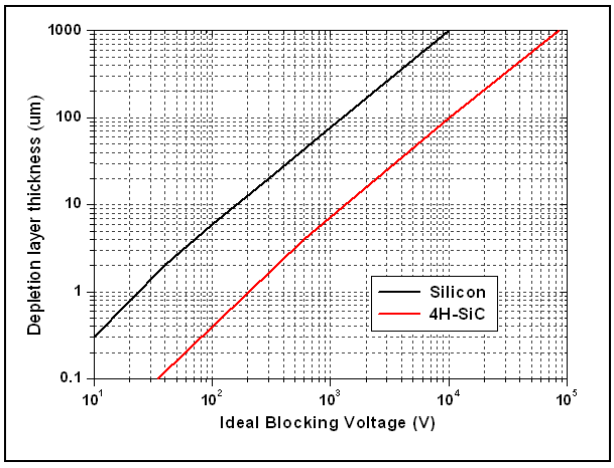


Fig. 1.2. Comparison depletion layer width of p+n diode vs. ideal Blocking voltage of Si and SiC devices

Figure 1.1 shows the ideal blocking voltage versus background doping concentration of a non punch through PN diode for Si and SiC. It can be seen that 4H-SiC can support much larger voltage at given doping concentration when compared to Si. It can also be interpreted that for a given breakdown voltage, it is possible to have much higher doping concentration for SiC devices. From figure 1.2 it can be seen that for the same blocking voltage, the depletion region thickness in SiC is 10 times less than in Si. Hence, we can conclude that SiC can have higher doping concentration and 10 times thinner regions to support the same blocking voltage as compared to Si. This is attributed to the 10 times higher E_c as described earlier.

SiC IGBTs and MOSFETs are being extensively investigated over the past few years due to its superior characteristics, notably lower losses at higher voltage ratings. For many applications such as HVDC and marine the converter development requires more efficient power devices. Extensive literature review shows that SiC offers overall lower losses compared to Si. This will mean that if the material price is low and the inherent material defects can be reduced further, SiC devices can effectively replace Si IGBT for many high voltage applications[3]. Clustered Insulated Gate Bipolar Transistors (CIGBT) with their inherent controlled thyristor action has proven to show better performance in terms of on-state and saturation performance than conventional IGBTs in Si [4] [5]. This work studies the performance and design of CIGBT in 4H-SiC in great detail.

1.2 Organisation of this thesis:

Chapter 2 gives a general overview on SiC material properties, techniques involved in its fabrication, advantages and limitation and also potential applications.

Chapter 3 evaluates the theoretical limit of Si CIGBT for the first time. The limit of SiC CIGBT is also compared to the state-of-the-art technologies and establishes the basis for this work.

Chapter 4 introduces the power device Clustered IGBT with planar gates in SiC for the first time. The designs and performance of possible device structures using extensive 2D simulations in MEDICI™ are reported in this chapter. Comparison with equivalent SiC IGBT device is also provided.

Chapter 5 introduces Clustered IGBT with Trench gates in SiC for the first time. The design and performance analysis of the device structure using extensive 2D simulations in MEDICI™ are reported in this chapter. A general device fabrication process is also discussed within this chapter. Comparison with equivalent SiC Trench IGBT device is also provided for better understanding.

Chapter 6 provides results of a comparison made between N channel and P channel SiC CIGBT devices through simulations.

Chapter 7 summarises the major results of the thesis and discusses future work.

Appendix A : contains the device parameters and models used for simulations.

Appendix B : contains the MEDICI™ codes used.

Appendix C : contains a list of the author's publications

Appendix D : contains a complete list of figures in this thesis.

Appendix E : contains a complete list of tables in this thesis.

Reference:

[1] B. J. Baliga, *Silicon Carbide Power Devices*: World Scientific Publishing Co. Pte Ltd, 2005.

[2] G. G. Walden, "THE FUTURE OF SILICON CARBIDE HIGH POWER ELECTRONIC SWITCHES." PhD: Purdue University, 2009, p. 196.

[3] H. Linewith, "Design and application of SiC Power MOSFET," in *Engineering and Information Technology*. vol. Doctor of Philosophy: Griffith University, 2002.

[4] L. Ngwendson, M. R. Sweet, and E. M. S. Narayanan, "An overview of the recent developments in high-voltage power semiconductor MOS-controlled bipolar devices," in *Proceedings of the IEEE Bipolar/BiCMOS Circuits and Technology Meeting*, Capri, 2009, pp. 198-205.

[5] N. Luther-King, E. M. S. Narayanan, L. Coulbeck, A. Crane, and R. Dudley, "Comparison of trench gate IGBT and CIGBT devices for increasing the power density from high power modules," *IEEE Transactions on Power Electronics,* vol. 25, pp. 583-591, 2010.

Chapter 2:

An Overview of Silicon Carbide

SiC has the following advantage over other potential WBG materials:

- It can be selectively doped using n-type or p-type dopants.
- SiO_2 is the native oxide and can be grown thermally.
- High quality crystals of the material are available and it is freestanding (SiC wafers are readily available) unlike GaN.

2.1 A brief history of Silicon Carbide

SiC was first observed in 1824 by the Swedish Scientist, Jöns Jacob Berzelius [1]. SiC occurs very rarely naturally and the first man made SiC was produced by Acheson in 1891 in an electric furnace for grinding and polishing purposes [2]. In 1955, Lely [3] developed a crystal growth method for producing high quality bulk SiC but faced problems in developing large defect-free areas which had hindered the fabrication of devices. The 'Seeded Sublimation epitaxy' or better known as 'modified Lely method' was introduced in 1978 by Tairov and Tsvetkov [4] creating more interest for further research. Currently, Vapour-phase epitaxy (VPE) method in a Chemical Vapour Deposition (CVD) reactor is used for epitaxial growth of SiC layers. Further details about the fabrication processes of SiC material is discussed later in this chapter.

2.2 Crystal Structure

SiC crystal is formed by equal number of Si and Carbon atoms. Being period IV elements, they form covalent bonds with a bond distance of 1.89Å and also forms

highly ordered crystals. The crystal structure of 4H SiC is shown in fig 2.1. Unlike Si or GaAs, SiC exists in many crystal structures (called polytypes) each of which have different electrical properties. Only a few of these have commendable electrical properties. The most common of these polytypes for power devices are 3C-SiC, 4H-SiC (crystal structure shown in Fig 2.1) and 6H-SiC whose electrical properties are listed in table 2.1 [5]. 3C-SiC is also known as β-SiC as it is the only polytype with a cubic lattice structure and all non-cubic are called α-SiC. The different polytypes can be identified by their colours when doped differently, for example 4H-SiC is brown when N-doped with a high concentration while in the same condition 6H-SiC is green in colour [6]. Currently 4H-SiC is the most mature technology and most of the research is based on this. Both 6H and 4H-SiC wafers are commercially available (Cree) but due to higher electron and hole mobilities, 4H SiC is preferred for power devices. A detailed discussion of SiC crystallography can be found in [7].

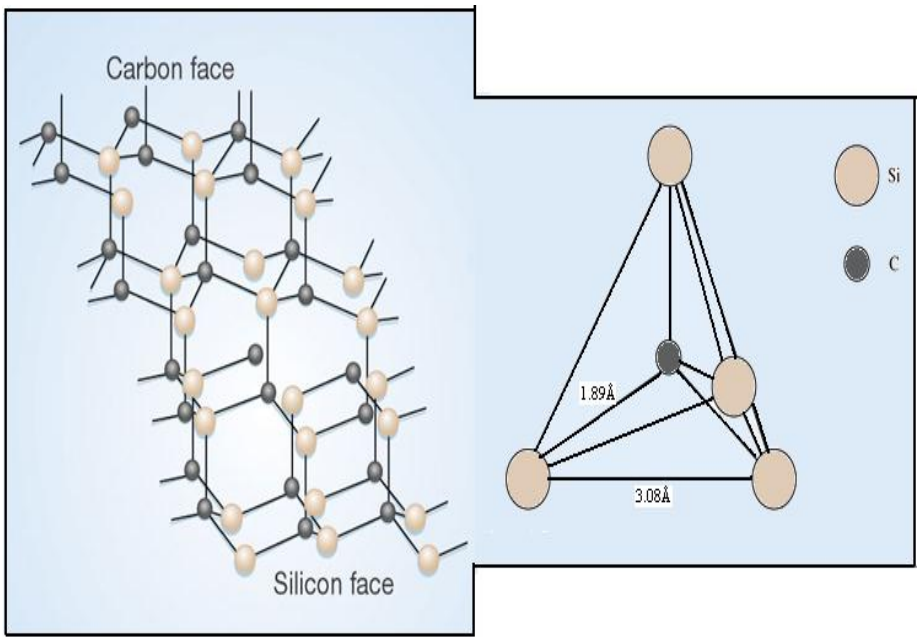


Fig 2.1: Crystal Structure of 4H-SiC

2.3 Electrical Properties Of SiC

As stated in section 2.2 due to different lattice arrangement of Si and C, each of its polytypes have different electrical properties which are listed in table 2.1. Although there are variations of electrical properties among the polytypes, some characteristics are common to all like wider bandgap energy, high breakdown electric field, higher thermal conductivity and high carrier saturation velocity. The thermal conductivity of SiC is >3.2W/cm-K at room temperature which is higher than most metals. This allows for the extraction of heat generated in the device readily and hence allowing for higher power operation of the device. From Eq [1] it can be seen that keeping all other parameters constant other than E_C, the specific on-resistance of a device can be reduced by 1000 times for SiC as compared to Si (it is worth pointing that the electron mobility in SiC is less than that in Si hence this is a theoretical estimation). The higher breakdown field of SiC allows thinning down of the device (by 10 times when compared to Si) and also allows for higher drift doping levels in the drift region thereby decreasing the drift region resistance. Fig 1.1 (a) shows the relation of BV with drift doping concentration and (b) shows depletion layer thickness with BV of the device. It can be clearly seen that SiC is superior to Si for an ideal non-punch-through type device with smaller drift depth and higher drift doping concentration as well as compared to Si for the same voltage rating or breakdown voltage. However, its advantages have not yet been completely realized due to difficulties in material growth, defects and expensive fabrication techniques [8, 9]. High temperature and hostile environment operation of SiC devices is an area under intensive research contributed by its attractive electrical properties.

Table 2.1: Comparison of 4H-,6H- and 3C- SiC polytypes electrical properties @300K

Properties	4H-SiC	6H-SiC	3C-SiC
Bandgap energy , E_g (eV)	3.26	3.03	2.3
Relative Dielectric Constant , ε_r	9.7	9.66	9.6
Thermal Conductivity, κ (W/cmK)	3.7	4.9	3.6
Intrinsic Carrier Concentration (cm^{-3})	8.20E-10	1.6e-6	8E-10
Electron mobility (μ_n) (cm^2/Vs)	950	400	800
Hole Mobility (μ_p) (cm^2/Vs)	120	90	320
Saturation Electron Velocity(cm/sec)	2e7	2e7	2.5e7

2.4 Major Challenges in SiC Electronics

As discussed earlier there are more than 180 polytypes of SiC available and out of which only 4H, 6H, 3C and 15R are in use. A lot more research may be required to fix a suitable polytype for power applications. The growth of the seed crystal is a difficulty faced due to the fact that SiC sublimes at 2200^0C and has no liquid phase. Another problem faced by the industry is the wafer quality and sizes that can be made. Currently the maximum wafer diameter is 6 inch (By Cree) which has to be made larger for reducing the cost per device. The defect density throughout the wafer has been reduced 10/sq.cm which is very low but can be improved further as the technology matures only for selected defects. Device fabrication is done usually epitaxially and/or by ion-implantation as diffusion of dopants in SiC is negligible. Hence improvements in epitaxial growth techniques need to be improved and also ion-implantation causes surface damage and roughness which will need to be improved too. Another problem is the low bulk and channel mobilities of carriers and their uniformity across the wafer/device. Gate oxide quality and reliability is yet another problem for MOS controlled devices. SiC having all those advantages stated earlier cannot yet be used to its full potential as the packaging will limit its

performance. Packaging techniques for high temperature and higher power density operation is to be made available to completely realise its superior electrical properties. Finally, stable contacts and contact resistances are currently poor in SiC devices especially at higher temperature and hence need further improvement.

2.5 Major Fields of development in SiC Electronics

1. SiC Wafer and substrate fabrication
2. SiC device physics and development
3. SiC device modelling and fabrication
4. Device Packaging
5. Identifying potential applications

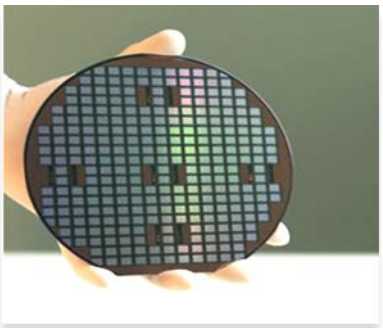


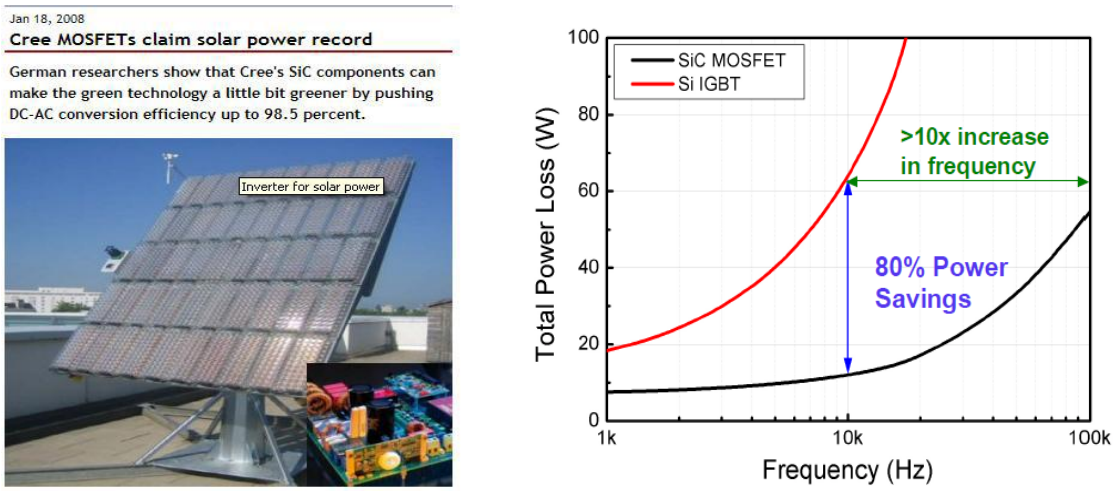
Fig 2.2 : Typical SiC Wafer

2.6 Application areas of SiC electronics.

Before electronic application of SiC was identified, it was used as abrasives and in cutting and polishing tools due to its hardness (only Diamond and Boron Nitride are harder than SiC). As the SiC technology matures, potential areas of application have to be realised so as to predict the advantage of using these devices there. Major areas of application of SiC electronics are:

- Automotive – engine and transmission
- Aerospace – Braking systems, Engine control
- Industrial Applications – Fluid level monitoring
- Space Technology – Power systems and Remote applications

SiC Schottky diodes have been used as anti-parallel diodes in boost or buck converters etc due to their near ideal performance in high voltage switching. These diodes have zero recovery charge and hence can turn-on instantly. Motor drives are another potential application for this technology where SiC devices can improve efficiency of the converters at higher frequencies. Fig 2.3 shows a solar inverter which uses SiC MOSFETs by Cree. It is seen from Fig 2.3 (b) that using SiC MOSFET the switching frequency for operation can be increased by ten times within a reasonable total power loss. This can be useful in many ways since by increasing the switching frequency can reduce the amount of filtering needed thereby saving the weight/volume of the converter.



(a) *(b)*

Fig 2.3 (a) Solar Inverter using SiC MOSFETs by Cree. (b) Total Power loss comparison 1.2kV,10A SiC MOSFET and Si IGBT in the same solar inverter.[10]

2.7 SiC Power Devices – Current Scenario

SiC has been under intensive investigation for more than two decades. SiC devices can be beneficial for high voltage devices (>10 kV) as this represents a reduction in drift thickness of up to 80% in comparison to Si technologies which can in turn reduce the power loss within the device [8]. However, its advantages have not yet been completely realized due to difficulties in material growth, defects and expensive

fabrication techniques [8, 9]. Although fabrication of N-channel SiC devices is a more mature technology at present, P-channel devices are more suitable for high voltage applications due to higher hole impact ionization coefficient and high surge capability and lower resistivity of the n+ substrate in bipolar devices [11]. Devices like IGBTs, SiCGT, JFETs and GTOs have so far been demonstrated at laboratory scale. Schottky diodes up to 1.7 kV and 1.2 kV MOSFETs are commercially available from Cree, Infineon and a few others [12-15]. This section will briefly discuss some of the current state-of-the-art devices demonstrated both commercially and at a laboratory scale.

2.7.1 SCHOTTKY BARRIER DIODES (SBD) :

The first SiC Schottky Barrier Diodes were developed by Infineon in 2001. The advantages of these are that they have Zero Reverse Recovery charge hence turn-on losses can be minimised. They also enable high switching speeds (< 50 nsec) since they eliminate the large reverse currents observed in Si rectifiers. These diodes have been replacing Si PiN diodes due to these characteristics. It is has led to downsizing of system and efficiency improvement but has been limited due to its high cost and difficulty in implementing in power electronic circuits. A PiN diode tends to store a large amount of minority carriers in the conduction state hence for it to be turned off all these charges have to be removed by recombination causing long turn-off times. Whereas SiC Schottky Barrier diode being a majority carrier device has no stored minority carries hence has almost zero reverse recovery charge. Fig 2.4 shows the comparison between Si PiN diode and SiC Schottky diode performance in terms of reverse recovery times. Figure 2.5 shows the structure of a typical SiC Schottky Barrier diode (SBD) along with the termination and Junction Breakdown Schottky (JBS) grid (P+ grid) which is ion-implanted. The termination

shown here is Junction Termination Extension (JTE) which could be replaced by multiple floating guard rings [16]. In this structure the epilayer 1 prevents the high electric field from reaching the substrate and epilayer 2 supports the blocking voltage. Figure 2.6 (a) shows the forward and reverse characteristics of a 1.7 kV SiC SBD and (b) shows the typical reverse recovery waveforms. It can be seen from the figure that, SiC SBD has a much lower reverse recovery time as compared to their Si PiN counterparts for the same forward voltage. It can also be inferred that, the state-of-the-art PiN diodes are quite close to the theoretical limit of these devices as well.

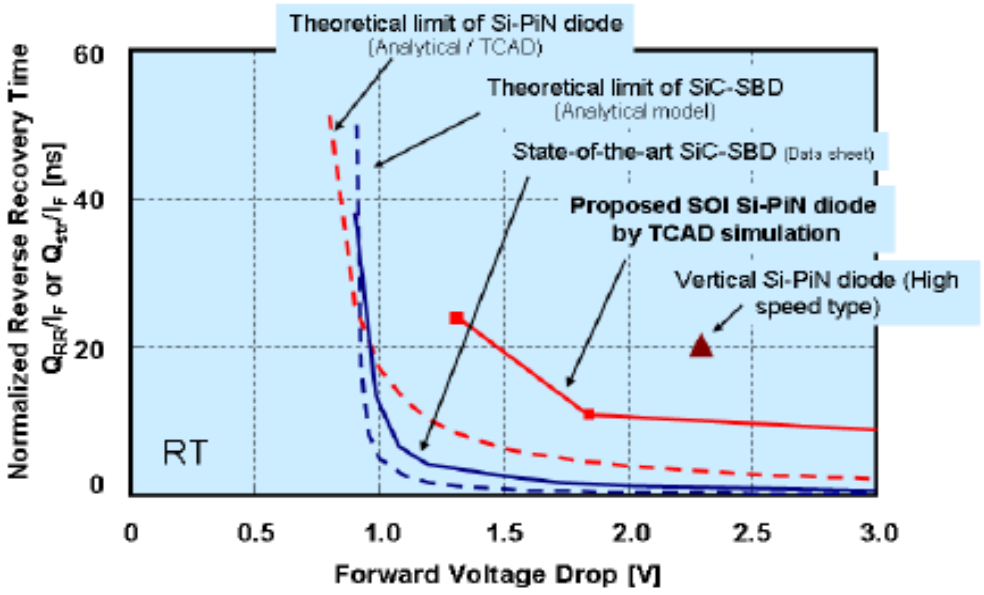


Fig 2.4 : Comparison of Reverse Recovery times of Si PiN diodes and SiC SBDs. [17]

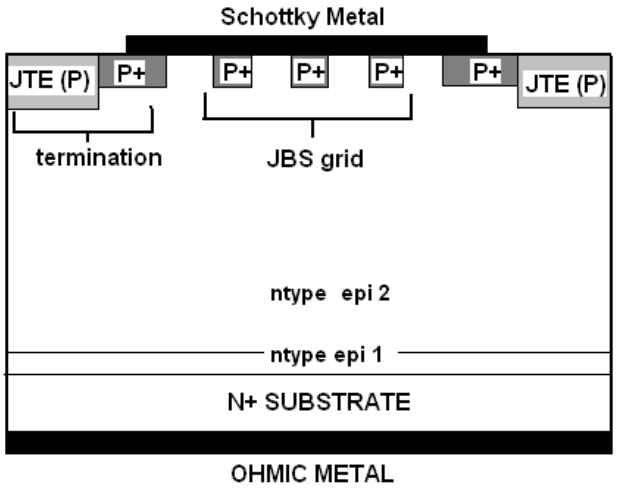
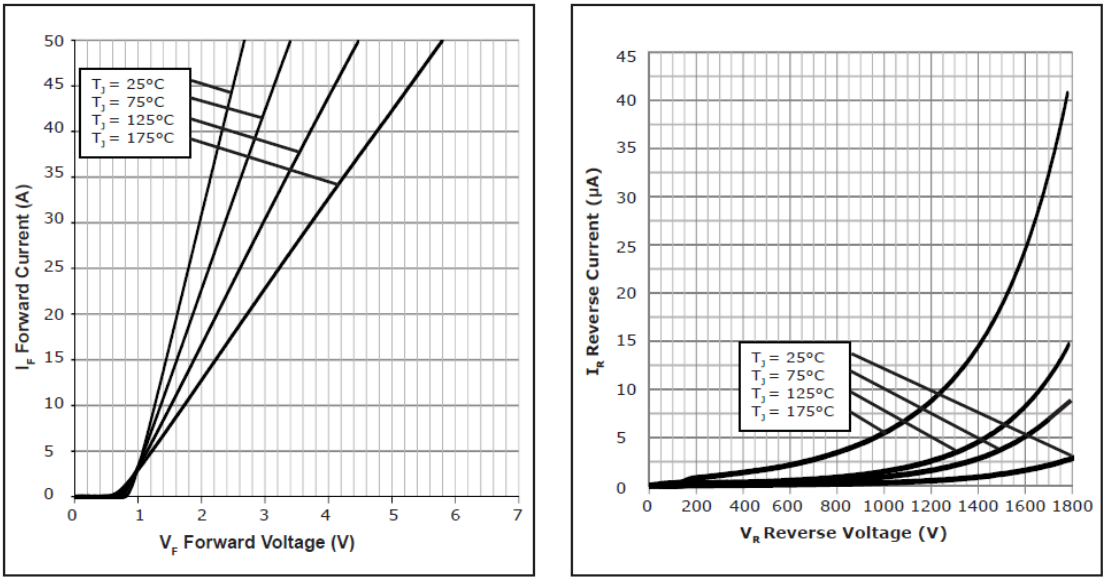
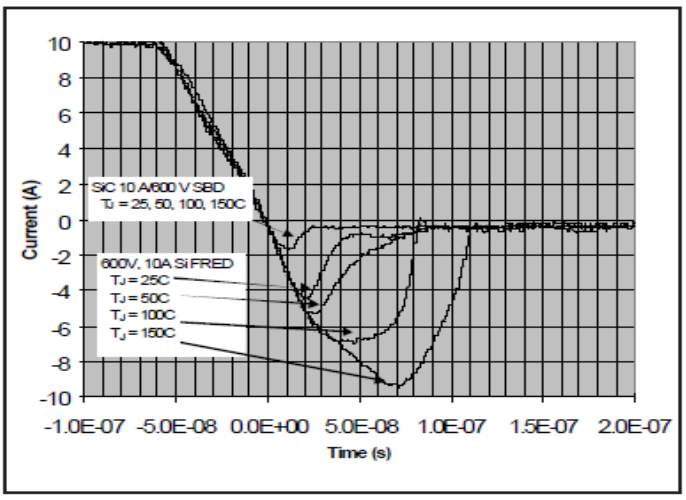


Fig 2.5 : Typical SiC Schottky Barrier Diode showing edge termination and JBS grid.



(a)



(b)

Fig 2.6: (a) Typical device characteristics of a 1.7kV SiC SBD by Cree. [13] (b) Typical Reverse recovery characteristics of a 600V, 10A SiC SBD and Si FRED. [18]

Third generation SBDs by Infineon uses advanced packaging technologies accommodating higher current densities (700A/cm^2). SiC material has very high thermal conductivity however earlier packaging used to add to the overall thermal resistance.

Cree, Infineon, Microsemi, SemiSouth and a few others have commercial SBDs rated upto 1.7kV, 25A max. Details of the some are listed in table 2.2 [13, 19, 20].

Table 2.2 : Commercially available SiC SBDs

Manufacturer	V_{br} (V)	Current (A)	V_f (V)	I_{rev} (µA)
Cree	600	10	1.8 @ 175 ℃	100
	1200	5,20	2.6, 2.5 @150 ℃	100,20
	1200	50	3 @ 175 ℃	50
	1700	25	3.2 @ 175 ℃	100
	1700	50	1.6 @ 175 ℃	<40
Infineon	300	10	1.5 @ 150 ℃	20
	600	4 , 16	2, 1.7 @ 150 ℃	4,10
Microsemi	200	1	1.6@25 ℃	20
	600	4	1.7 @ 25 ℃	20
SemiSouth	1200	5 , 10, 20, 30 and 60	1.6 @ 25 ℃	300 x

2.7.2 PiN DIODES:

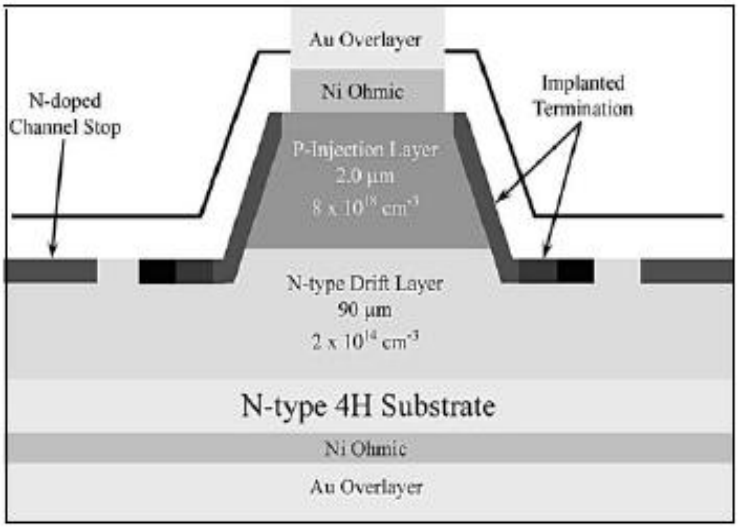
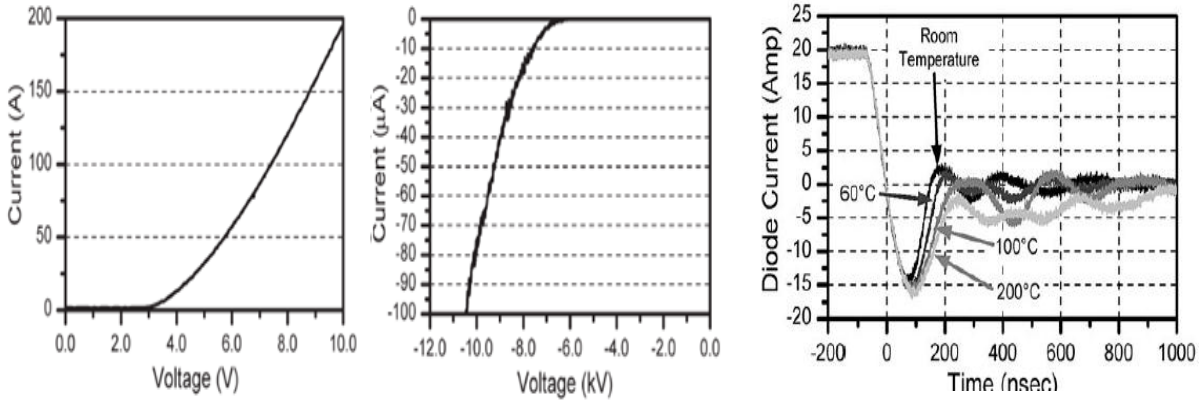


Fig 2.7: Typical Structure of 10kV, 20A SiC PiN diode, Cree. [21]

Continual improvement in SiC epitaxial processes has led to the development of high power devices which requires drift regions. This causes a large forward voltage drop in the drift region and hence has been an obstacle to commercialization of these devices. SiC PiN diodes have been demonstrated in both 4H and 6H SiC. Fig 2.7 shows the structure of a 10kV 4H-SiC PiN diode using a new epitaxial process to

minimise the stacking faults and dislocations. The forward voltage of this device was found to be 4.4V @ 100A/cm^2 conducting 20A through it. The device also showed excellent characteristics at higher temperatures with minimal reverse recovery charge [21]. The forward and reverse characteristics are shown in fig 2.8 (a) and (b). Using this new epitaxial processing the yield of 10kV PiN diodes have been improved by 23% and without affecting long term stability of the device. Table 2.3 lists some of the PiN diodes demonstrated to date.



(a) *(b)*

Fig 2.8 : (a) Typical forward and reverse characteristics (b) Reverse recovery of a 10kV, 20A SiC PiN diode [21]

Table 2.3: State-of-the-art SiC PiN diodes for power applications

Company	BV	Current	Chip Size	V_f (V)
SiCED[22]	*4.5kV*	*6A*	*10.2mm^2*	*-*
SiCED[23]	*6.5kV*	*25A*	*5.7mm^2*	*3.4V @100A/cm^2*
GENESIC [24]	*8kV*	*2A*	*-*	*-*
GENESIC[24]	*15kV*	*1A*	*-*	*-*
CREE[21]	*10kV*	*20A, 50A*	*6.04mm^2,8.7mm^2*	*4.4V, 3.9V @ 100A/cm^2*

2.7.3 Bipolar Junction Transistor (BJT) :

BJTs are known for their properties like low on-resistance, positive temperature coefficient of on-resistance, fast switching speed and negative temperature coefficient of current gain. These characteristics of BJTs help in higher operating

frequencies of the system, and hence reducing the size and cost of passive components. SiC BJTs also possess these same characteristics and are also not prone to secondary breakdown. SiC BJT is an epitaxially grown device which can be used for high power application. One of the main advantages is that there is no gate oxide enabling high temperature operation with improved reliability. Intensive research still exists on BJTs in SiC around the world. Cree demonstrated a 1.2kV

device with a current gain of 70 at 25ºC in 2009 [25]; the structure of which is shown in fig 2.9 and the forward characteristics are shown in fig 2.10. It is seen that the current gain of the BJT drops considerably at higher temperatures. To keep the current gain high enough, the base region is kept thin so as to reduce carrier recombination in this region.

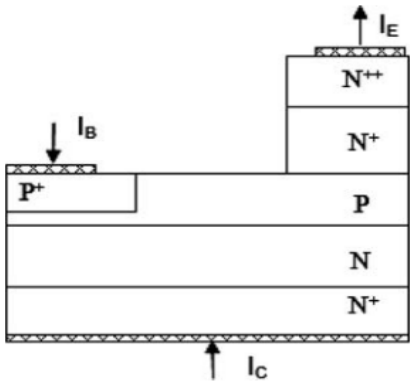


Fig 2.9 : 1200V SiC BJT structure [25]

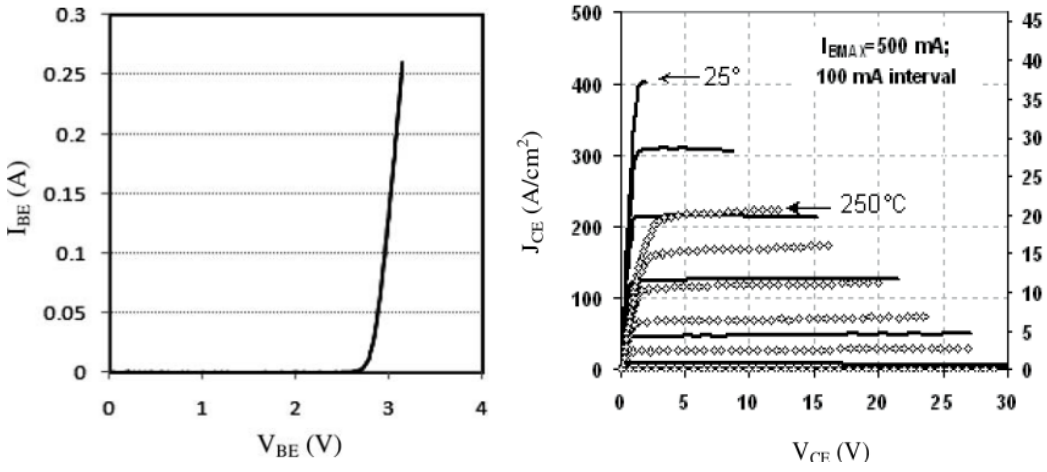


Fig 2.10 : Forward characteristics of 1200V SiC BJT [25]

In SiC BJTs strong conductivity modulation is not possible as the carrier lifetimes are small and also higher drift doping concentration will attribute to the same which leads to faster switching speeds of the device. The current gain of BJT decreases with temperature and this is shown in fig 2.11. In the year 2008 Honda had announced a new SiC BJT named 'Suppressed Surface Recombination Structure (SSR)-BJT' with the highest current gain of 134 at room temperature and a BV of 950V [26]. By 2009 they improved on this technology and increased the current gain to 145 at room temperature with a BV of 1.1kV and an on-resistance of 1.7mΩcm^2 [27]. Very recently Genesic semiconductor has released a large number of transistor products suitable for high temperature and has very good performance [28].

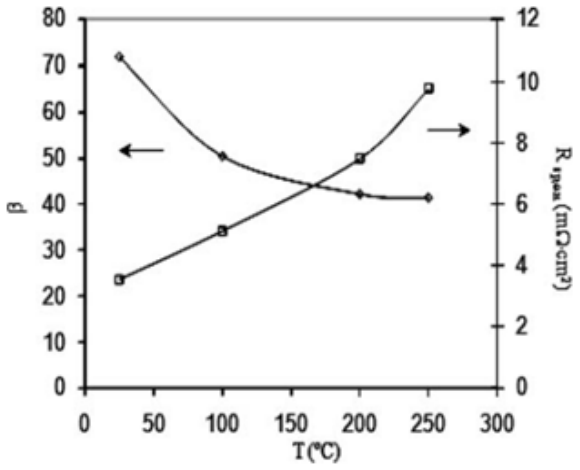
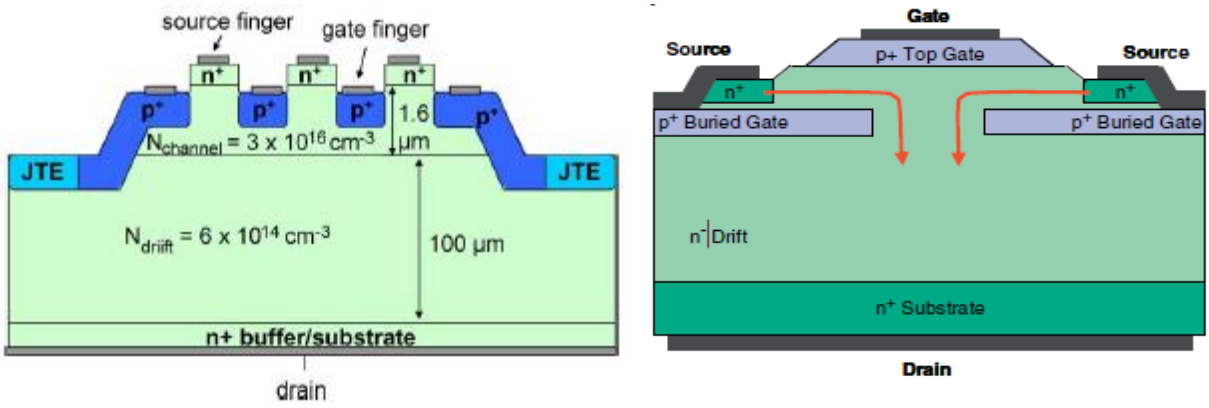


Fig 2.11: Temperature dependence of current gain and specific on-resistance of BJT [25]

2.7.4 Junction Field Effect Transistor (JFET) :

SiC JFET have been studied in detail by many research groups since these devices are free of low carrier mobility and lower gate oxide reliability like their MOSFET counterparts. It is the most mature switch technology in SiC presently. These devices can be normally-ON or normally-OFF and both these have been reported [29, 30]. Detailed discussions on design, fabrication and performance of normally-off

SiC JFETs have been discussed by Rajesh K. Malhan *et al* in their paper [29]. The structures of a typical normally-ON and OFF SiC JFET are shown in fig 2.12 (a) and (b) respectively. SiC JFET can be epitaxially grown and is capable for extremely low on-resistance. Another advantage of JFET is that it does not require anti-parallel diodes thereby eliminating the reverse recovery problem forever and reducing number of semiconductor devices in a system [31]. Normally-ON JFETs are regarded as an undesirable device for power applications (for safety reasons) this feature can be used to get rid of the anti-parallel diode in systems and such a circuit is shown in Fig 2.13.



(a) *(b)*

Fig 2.12 : (a) Normally-ON SiC JFET [30] (b) Normally-off SiC LC JFET [29]

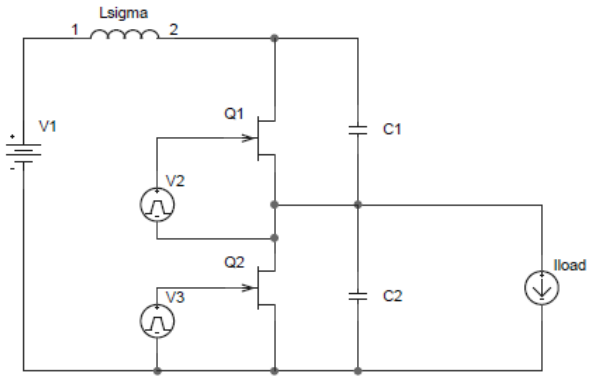


Fig 2.13 : JFET switching circuit without anti-parallel diodes.[31]

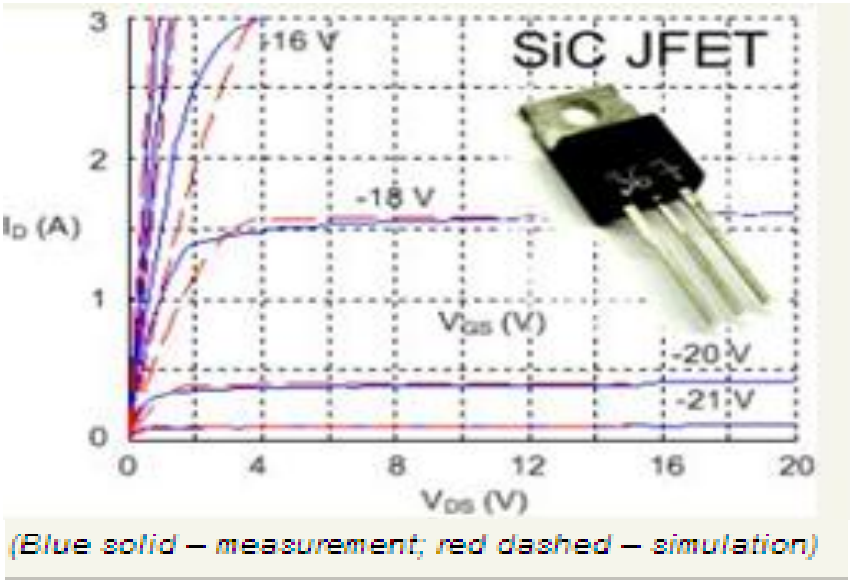


Fig 2.14: 1.2kV SiC JFET output characteristics demonstrated by CPES, Virginia Tech [32].

Although JFETs have benefits of low voltage drop and high switching speeds and the fact that anti-parallel diodes can be avoided, they come with their share of drawbacks. The normally-on property increases the gate drive complexity and also a negative voltage will be required to turn-off the device as well as need higher power input at the gate than a MOSFET. High speed switching in a circuit will lead to high over voltages and since SiC JFET is used as a diode this voltage will appear across the device itself while switching. There are also problems of Electromagnetic Interference (EMI) / Electromagnetic Compatibility (EMC) [33].

In 2010 ISPSD, SiCED had demonstrated a SiC VJFET inverter module for electric vehicles [34]. The module consisted of 1.5kV, 5A SiC VJFET by SiCED and 600V, 12A SBD by Infineon. The inverter built was experimentally tested and its efficiency was found to be 95.7%. The application proposed by them was in electric cars (Senior Car by Suzuki Motor Corporation shown in Fig 2.15).

Fig 2.15 : Senior Car by Suzuki Motor Corporation with SiC JFET Inverter [34]

There have been JFET inverter modules with efficiencies greater than 98% reported by other groups [35]. The efficiencies of two of them at different load powers and temperatures are shown in Fig 2.16 which is controlled by the total power losses in the devices.

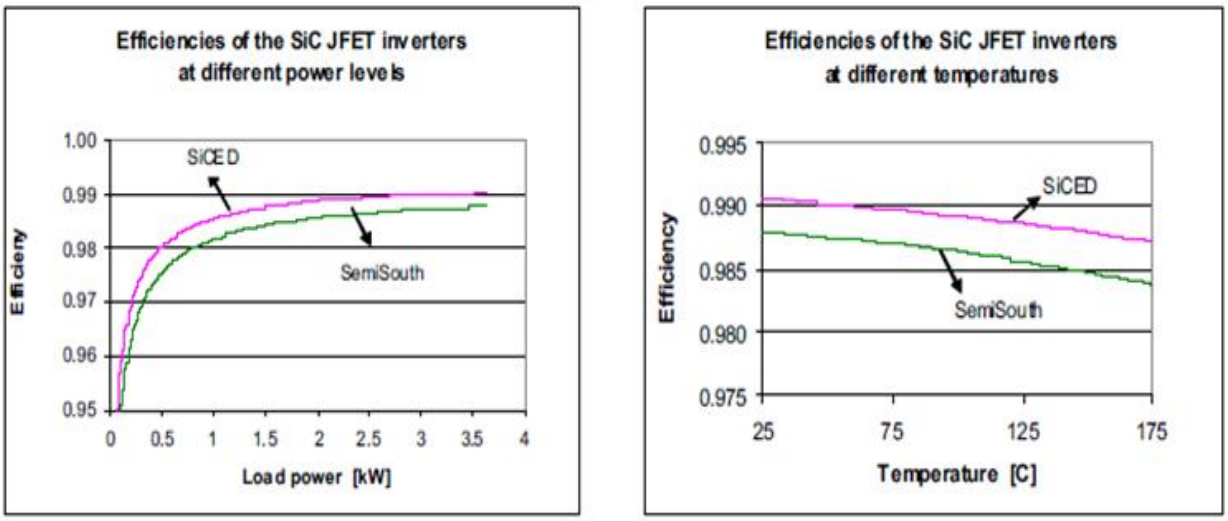


Fig 2.16: Efficiencies of other JFET inverter modules. [35]

2.7.5 Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

The first device to be developed in SiC was MOSFET but was limited by poor oxide quality and hence low channel mobility. Recent improvements in gate oxidation have led to development of better MOSFETs and eventually Cree launched the industry's first SiC MOSFETs[12] in the year 2011. Currently SiC MOSFET device have short-channels and hence higher channel density to overcome the lower channel mobility in SiC so as to get lower specific on-resistances. Today different methods are being implemented to improve channel mobility like nitrous gas passivation[36], phosphorous passivation [37] and yet it still needs a lot of improvement. However, SiC MOSFETs are considered better as compared to JFETs as they are normally-Off and gate driver circuit is easier to build. Fig 2.17 shows a typical SiC MOSFET device with both planar and trench gates.

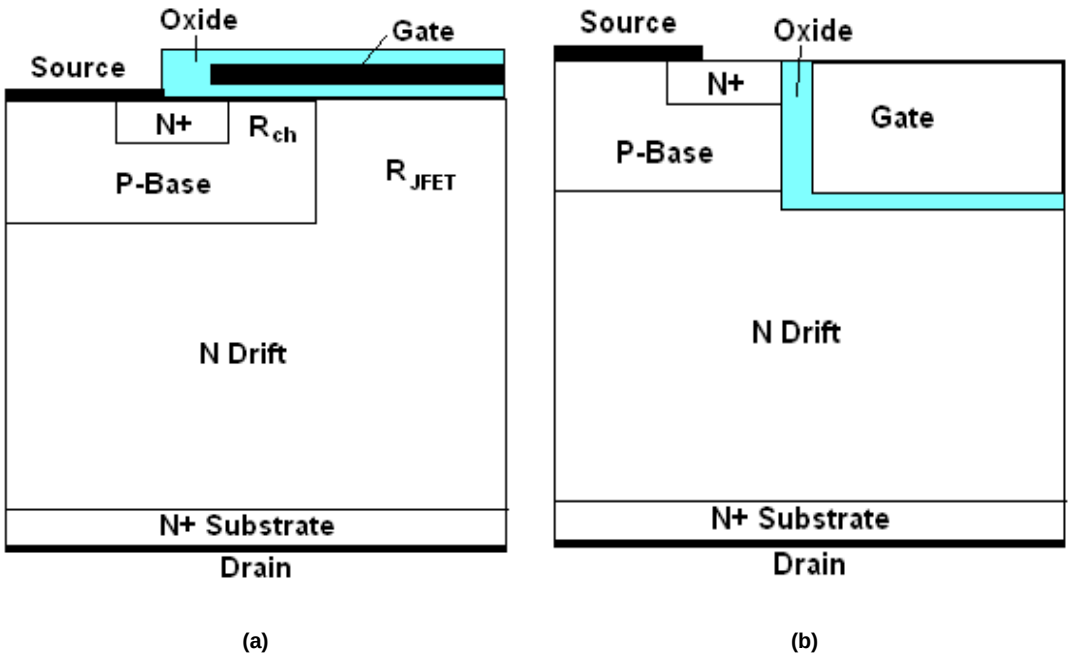
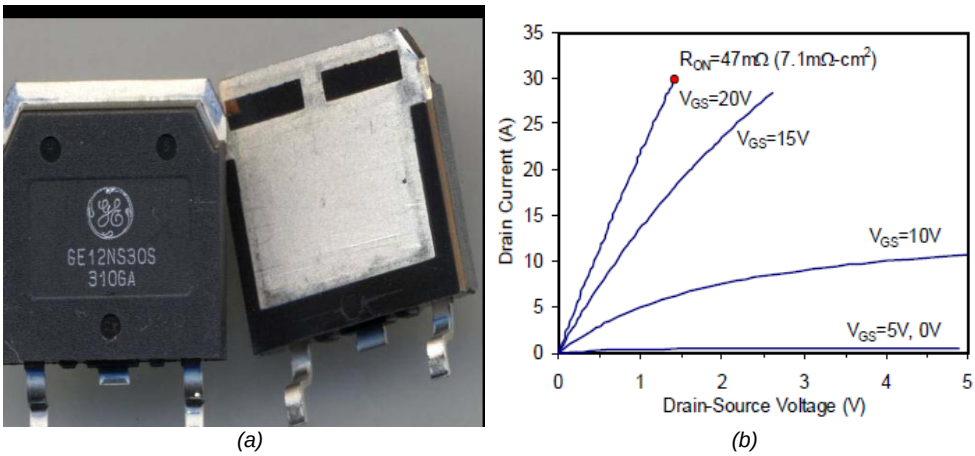


Fig 2.17: Typical MOSFET Structure (a) Planar (b) Trench



(a) *(b)*

Fig 2.18: (a) GE SiC 1.2kV MOSFET Prototype (b) On-state characteristics. [38]

In 2010, General Electric reported a 1.2kV vertical n-channel MOSFET [38] shown in Fig 2.18. A prototype of 10kV SiC MOSFET has been demonstrated by Cree in 2006 [39] which utilizes a 100µm n-type epilayer and later on in 2008 this device was used to demonstrate a DC-DC boost converter [40]. The converter was tested in steady state at 20kHz and had an efficiency of 93%. From Fig 2.19 it is clear that MOSFET turn-on losses are the largest among the device losses as there is no bipolar conduction available. At higher frequencies the junction temperature of the MOSFET increases and so does the conduction losses. This eventually leads to a decrease in the efficiency of the converter.

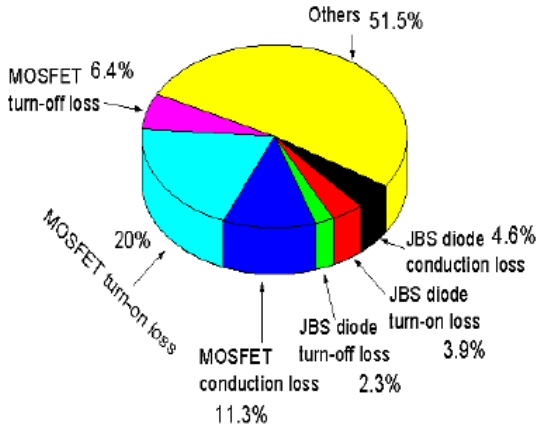
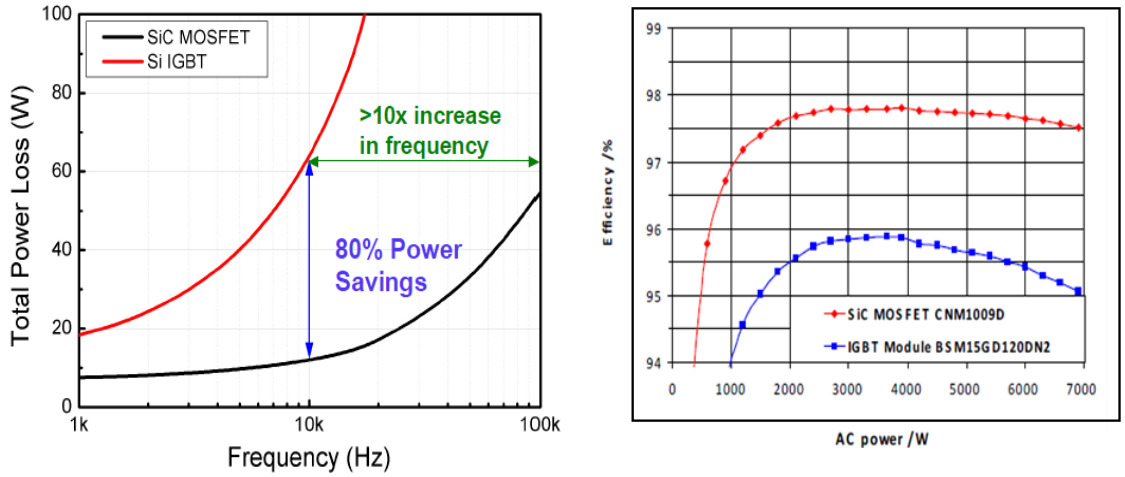


Fig 2.19: Breakdown of the losses in Boost Converter. [40]

Trench gate MOSFETs also have been demonstrated by many research groups. Etching SiC is a difficult task and is possible using special dry etching techniques. Controlling the shape of these trenches is also difficult as surface roughness and sharp angles are formed while etching. Fuji reports that use of high temperature annealing in hydrogen atmosphere improves trench shape and smoothness [41]. Also a trench depth of 4µm and width of 1µm can be achieved[41]. In the year 2010, ROHM announced the industry's first SiC Trench MOSFET and SBD module for vehicle motors rated at 600V/450A [42].

Fig 2.20 shows the power loss (a) and efficiency (b) comparison between 1.2kV, 10A SiC MOSFET solar inverter by Cree with a 1.2kV IGBT solar inverter. Clearly the benefits can be easily seen in these graphs. A 2.5% improvement in efficiency can be obtained by using the SiC MOSFET module which will contribute to significant savings in cost. These SiC modules can be operated at 20kHz switching frequency.



(a) *(b)*

Fig 2.20: Total Power loss and efficiency comparison 1.2kV,10A SiC MOSFET and Si IGBT solar inverters.[10]

Fig 2.21 shows the comparison of a SiC MOSFET based converter with a Si based one in size, both rated at 11kW.Table 2.4 lists some of the commercially available SiC MOSFETs presently.

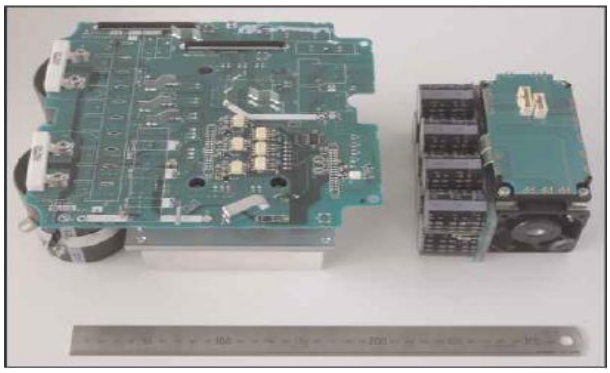


Fig 2.21: Size comparison of Mitsubishi 11kW SiC-based inverter(right) with a Si based inverter.

Table 2.4 : Commercially available SiC MOSFETs

Manufacturer	V_{br}(V)	Current (A)	R_{on} (mΩ)	Max T_j (ºC)
Cree [12]	*1200*	*11-60*	*20-60*	*150*
	1700	*2.6*	*1000*	*150*
RoHM[15]	*400*	*20*	*120*	*150*
	650	*29*	*120*	*175*
	1200	*10-40*	*450-80*	*175*

2.7.6 Insulated Gate Bipolar Transistor (IGBT):

IGBT (Insulated Gate Bipolar Junction Transistor) as a concept was initially demonstrated by Baliga [43] in 1979. As these devices have an extremely low switching loss and on-voltage drop across the drain and cathode ends as compared to MOSFET structure these devices were more favoured for a high performance switching applications. Currently various technologies of IGBTs exists and these are benchmarked in terms of their on-state losses and switching losses commonly known as the Vce-Eoff trade off. In order to optimise the performance of IGBTs for high power application it is essential to understand the internal device dynamics.

IGBTs are a known to be functional integration of MOS and bipolar technologies and it combines the best attributes of both technologies i.e. MOS gate control while

having bipolar mode of conduction. IGBTs have high input impedance and can be designed to support high voltages beyond ~5kV in Si. The introduction of trench technology improves the channel density and conductivity modulation at the cathode side of the drift resulting in superior on-state/switching trade off compared to conventional planar IGBT structures. An IGBT module contains a repetitive array of many cells arranged in a topological layout, providing extremely high current carrying capability and a large aspect ratio (W/L).

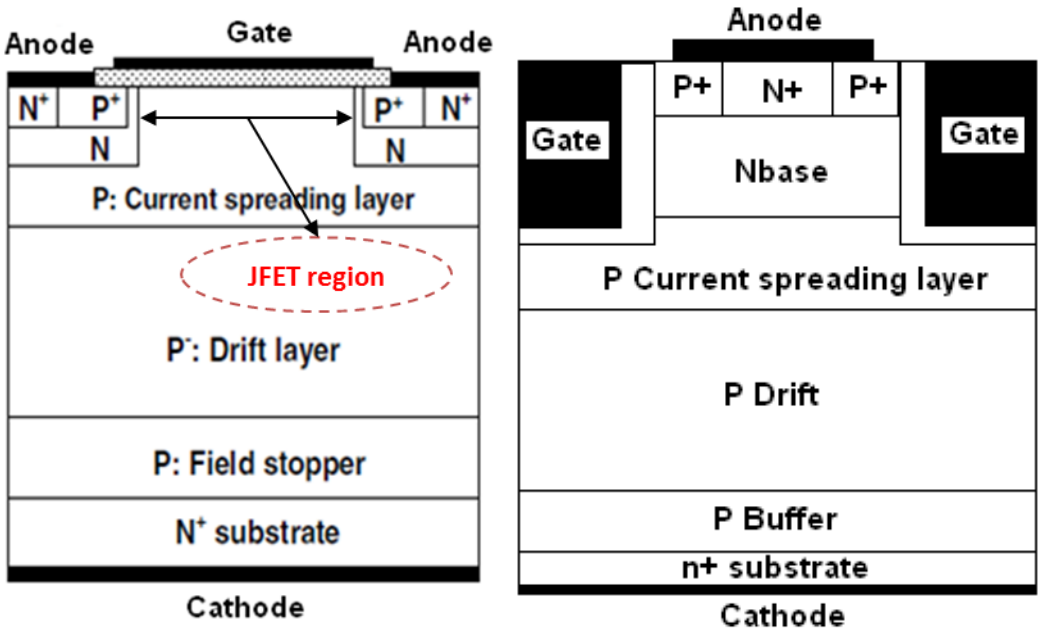
Device Operation

Si IGBT working has been explained in detail in [44]. In order to explain the theory of the IGBT a p-channel IGBT cross section is shown in Figure 2.22. When a negative voltage is applied to the gate with respect to the anode end of the device, the holes from p+ region that form part of the anode are attracted to the surface of the gate. These holes invert the SiC layer between the “n” base and the gate region to form an inversion layer. This allows current flow between “p-drift” bulk SiC region and “p+” anode region. The flow of electrons into the p-drift region lowers the potential of the p-drift region. This allows the n+ Collector / p-drift diode to become forward biased. Once this region is forward biased a high density of minority carriers is injected into the p-drift by the n+ region that form part of the cathode region of the device. The minority carrier injected into the p- drift travels vertically upward where some of these electrons are repelled by the negatively charged accumulation layer that is formed below the gate. These holes then transverse through the n-base and reach anode contact. At high forward voltages a high density of electrons builds up in the p-drift. These electrons attract holes from the anode contact to maintain charge neutrality which drastically enhance the conductivity of the p-drift region. The increased conductivity of the p-drift allows flow of holes through this region with very less

resistance. This process is termed as conductivity modulation. The conductivity modulation of an IGBT can be increased using various methods. However, this comes with a trade off with the switching losses. Hence the Vce-Eoff trade-off is a very useful figure of merit used for comparing IGBT technologies.

In order to regain the blocking state the gate voltage applied to the IGBT must be removed and the charges injected into the bulk region must be extracted. Most of this charge is extracted as the depletion region moves towards the n+ cathode. However, the decay of excess carriers also happens through the process termed as recombination and no external circuit can be used to speed up the process. This determines the turn-off performance of the device.

Although fabrication of N-channel SiC devices is a more mature technology at present, P-channel devices are more suitable for high voltage applications due to higher hole impact ionization coefficient and high surge capability and lower resistivity of the n+ substrate[11].



(a) *(b)*

Fig 2.22: Typical SiC IGBT structures with (a) Planar gate (b) Trench gate

This is further discussed in chapter 6. IGBT combines the high input impedance of MOSFET and high on-state current density due to conductivity modulation of BJT. These devices in Si have practically taken over medium power applications in the current world as MOSFETs have high on-state resistance at these voltage ranges. The drawbacks of IGBT are low switching speed due to requirement to remove the excess charge in the drift region.

SiC IGBT has an extra epilayer called the current spreading layer. The function of this layer is to reduce the JFET resistance (shown in Fig 2.22 (a)) which otherwise due to material properties is very high. Many n-channel and p-channel planar/trench IGBTs have been reported to date [45-49]. Fig 2.23 shows the forward characteristics of IGBT (both p- and n- channels), MOSFET and thyristor all rated at 20kV presented by a research group from Purdue University [50]. Over 10kV applications, bipolar devices are preferred due to their conductivity modulation characteristics and currently IGBT is the most favourable device for the same. Due to material specific difficulties in growth and fabrication SiC IGBT has not yet been commercialized.

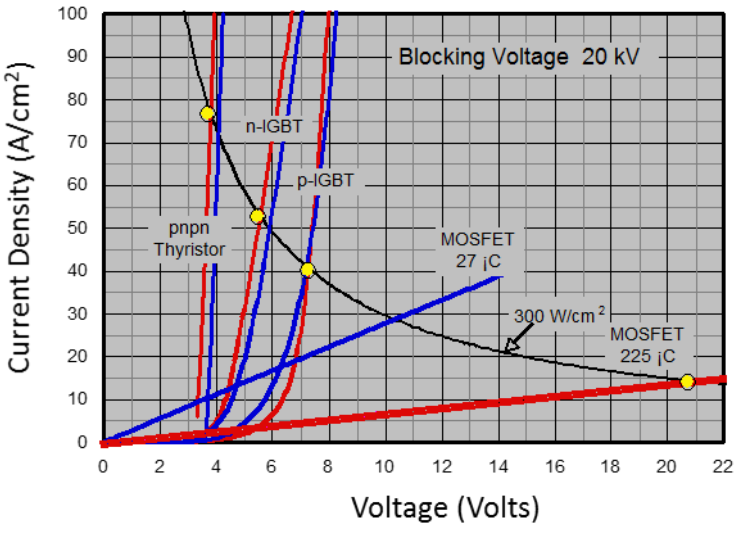


Fig 2.23: 20kV SiC device comparison by Purdue University [51]

Fig 2.24 shows the comparison of SiC and Si IGBT reported by Cree. The 12kV SiC IGBT shows three times lower R_{on} than Si IGBTs (2X 6.5kV) and they also report that SiC IGBT can switch four times faster and yet provide lower losses [10] . More on SiC IGBTs will be discussed in later chapters.

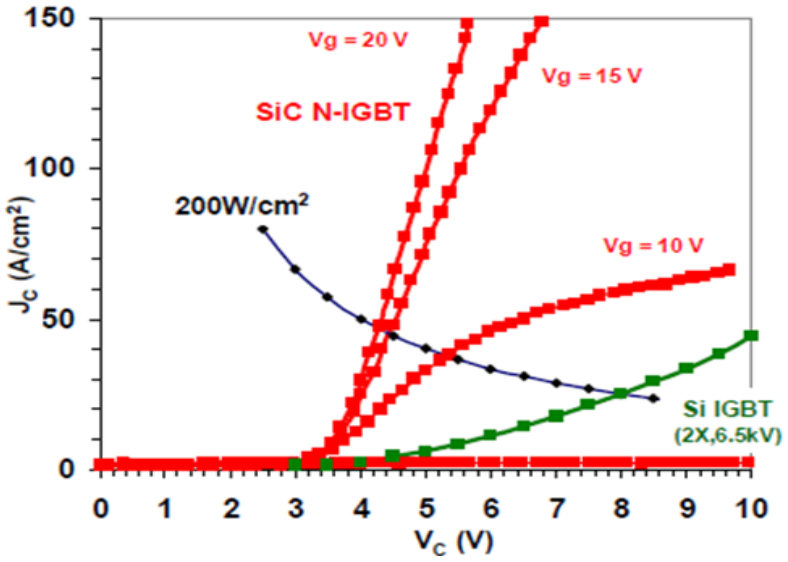


Fig 2.24: Comparison of N IGBT in SiC and Si reported by Cree.

2.7.7 Thyristors

SiC thyristors were first developed in 1990s. A thyristor device consists of four alternate p and n layers as shown in Fig 2.25. They were traditionally made with P substrates but due to the high resistivity of the same in SiC, n type substrates were used instead. 12.7kV SiCGTs (SiC Commuted Gate Turn-off Thyristors) were first demonstrated in 2004 by Kansai Electric in ISPSD [52] . A lot of research has been done on SiC thyristors as they can support very high voltages and also can conduct very high current density thereby reducing on-state voltage[53, 54]. However, their control circuits are pretty complex when compared to a MOS- controlled device. In 2006 a 4.5kV 120A SiCGT was reported in a three phase inverter application by the same group [55] which was further improved and in 2007 they reported a 180kVA

inverter [56]. Later in the year 2010, GeneSiC Semiconductor Inc reported 8kV SiC GTOs [57]. Purdue University has also reported 8-20kV thyristors [58].

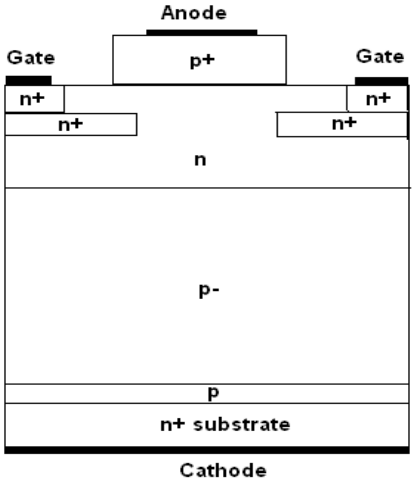


Fig 2.25: A Structure of SiC GTO.

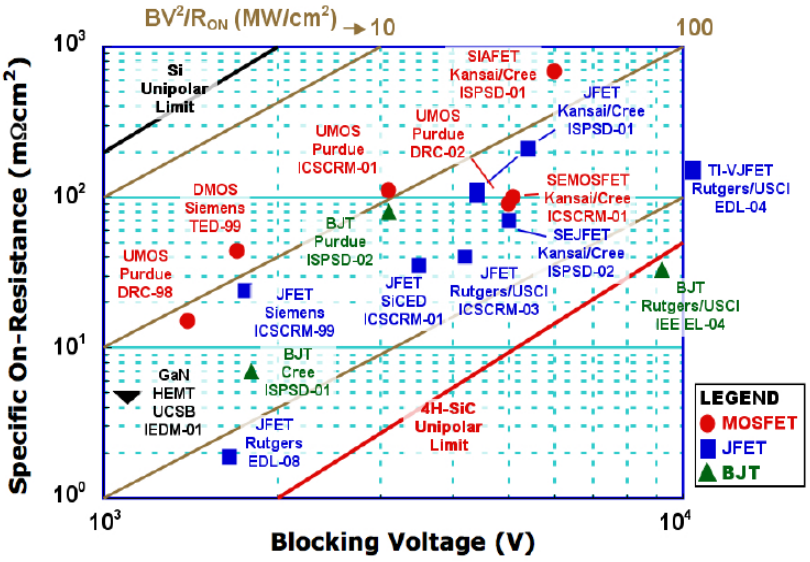


Fig 2.26: Comparison of some of the WBG devices reported. [59]

Having discussed some of the device reported to date a comparison of on-resistance with BV for different reported devices are shown in fig 2.26. Despite the excellent electrical and thermal properties of 4H SiC, the fabrication of high voltage SiC devices is still proving difficult due to the material defects which in turn affect the carrier lifetime, forward voltages and ohmic contacts to P-type material. When the

background work for this thesis was first done, the issues with SiC MOS-based devices were as follows:

1. The poor quality of oxide growth on SiC since it was depended on the crystal orientation of SiC epilayers.
2. The surface roughness in trenches to RIE technique used to form trenches in SiC.
3. The unique problems in activation of implants
4. Low Inversion layer or channel mobilities in the MOS devices

In spite of these problems, MOS based device research in SiC has been undertaken by various groups along with fundamental material and process improvement research. Previously in this chapter various power devices under research and production has been briefly discussed. Based on the background work, it can be concluded that the introduction of new device structures that are designed to overcome the above problems needs to be studied further. Thyristors are devices that can sustain very high voltages and currents and MOS-based Thyristor devices have been discussed in Si earlier [60]. SiC IGBT has been widely discussed in literature and in this thesis SiC CIGBT is discussed for the first time. The device performance is compared to an equivalent SiC IGBT for better understanding of the performance benefits.

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Chapter 3:

Theoretical limit of Clustered Insulated Gate Bipolar Transistor (CIGBT)

Over the years, power devices have evolved rapidly and have replaced GTO's in traction applications with ratings ranging from 100s of kVA to many MVA [1] . Wide bandgap devices have been introduced in the market marking a new era of power devices. It is often claimed that Si based devices face the threat of reaching material limit [2]. The super junction devices [4] have already broken through the Si unipolar device limit. The theoretical limits of Si IGBT has been discussed in detail [5]; the theory of achieving the lowest forward voltage in IGBTs. Considerable research has been focused on improving the on-state voltage of IGBT by increasing the carrier concentration on the cathode side. According to reference [5] very narrow mesa widths are proposed to reduce the on-state voltage to a minimum so that main current flows by electron diffusion and holes contribute to conductivity modulation alone when high anode injection condition. A flat-carrier profile in the n-drift region is assumed so that current flows only by drift within the region. Hence under high injection condition (assuming carrier distribution is linearly decreasing from cathode to anode) and under the assumption that no hole current flows the following equations hold true [5].

$$J_p = q\, D_p \frac{dp}{dx} - q u_p E = 0 \qquad (3.1)$$

$$J_n = J_{total} = 2 \times q D_n \frac{dn}{dx} \qquad (3.2)$$

$$E = \frac{kT}{q} \frac{1}{n} \frac{dn}{dx} \qquad (3.3)$$

The current density to forward voltage relation can be now derived by integrating (3.2) with boundary values as n_0(carrier density at anode end) and n_w (carrier density at cathode end) – further discussion on how this is obtained is explained in [6]

$$V_F = \frac{2kT}{q} \ln\left[\frac{1}{n_i}\left\{\left(\sqrt{\frac{QJ}{qD_E}} + b\right) exp\left(\frac{JW_N}{2qa}\right) - b\right\}\right] + R_{ch}J \qquad (3.4)$$

Where,

$$J = \frac{qD_E n_o^2}{Q} \quad , \quad V_F = V_{diff} + V_i \quad , \quad V_i = {}^{kT}/_{q} \ln({}^{n_w}/_{n_0}) \quad , \quad V_{diff} = {}^{kT}/_{q} \ln({}^{n_o n_w}/_{n_i^2})$$

The above equation is derived from [6] where high current characteristics of PiN diodes having very low forward voltages are discussed in detail.

A comparison of calculated and conventional IGBT VI curves have been published in [5] for various voltage ratings and also proposed as the IGBT limit in comparison to state-of-the-art devices. It was proposed that to realize very high electron injection efficiency in MOS gate structure, the mesa width (trench to trench distance) must be made as small as the inversion layer thickness such that two channels could merge to serve as a barrier to holes and provide a high concentration of electrons N base region within the mesa. This would in turn result in high electron injection efficiency. The lowest V_F was obtained for a mesa width of 40nm as this gave the highest electron injection efficiency. [2, 5]

A Clustered Insulated Gate Bipolar Transistor (CIGBT) is a three terminal MOS-gate controlled thyristor device demonstrated, albeit by simulation, in 2000 with excellent on-state, switching and saturation characteristics in Si [7, 8]. Further this device was experimentally tested up to 3.3kV, which served to verify these characteristics [9, 10]. The structures of planar gate and trench gate Clustered IGBT with PMOS gates are shown in Fig 3.1 and 3.2 respectively. Its unique ‘self-clamping’ feature allows

for current saturation even at high gate voltages, thereby protecting the gates and cathode from high anode voltages during on-state operation. Further discussion of the device operation can be found in section 3.2.

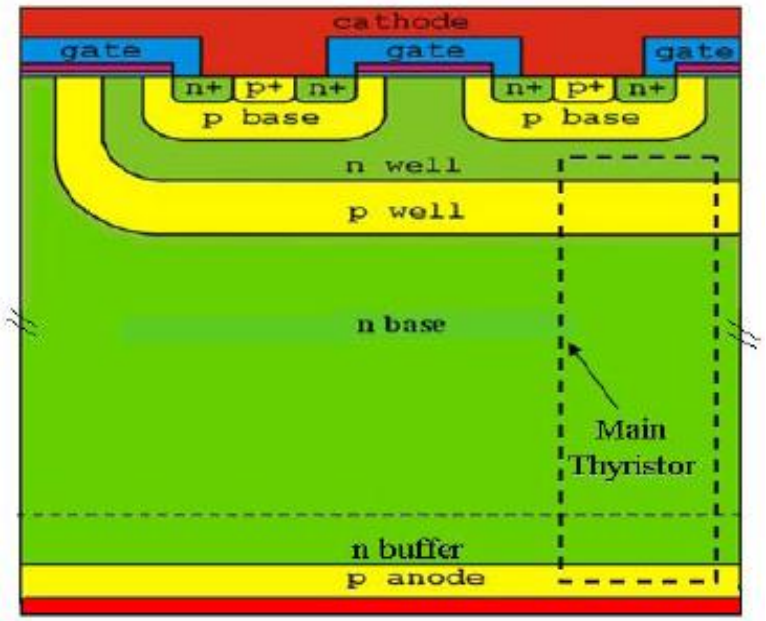


Fig 3.1 Simplified cross-section of a planar gate CIGBT. (Half-cell)

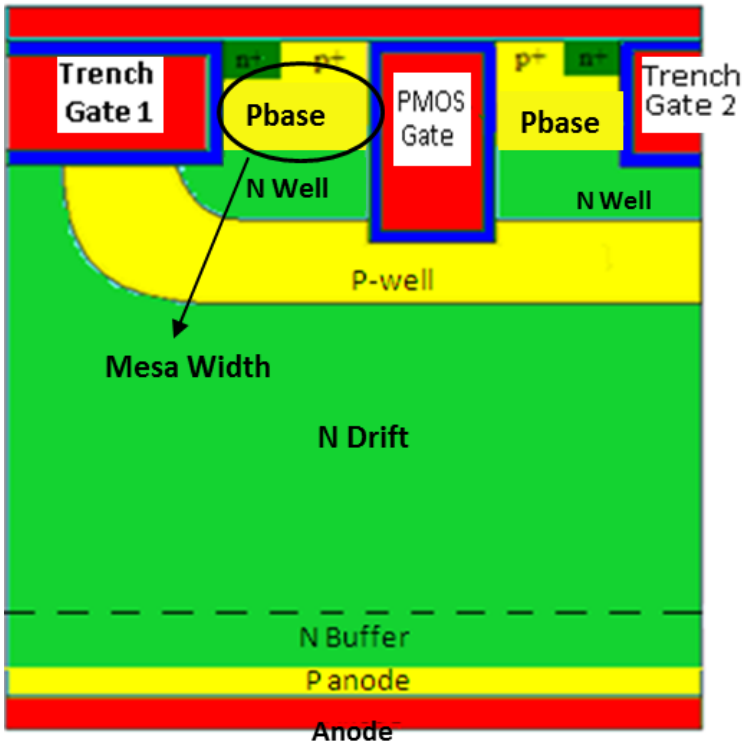
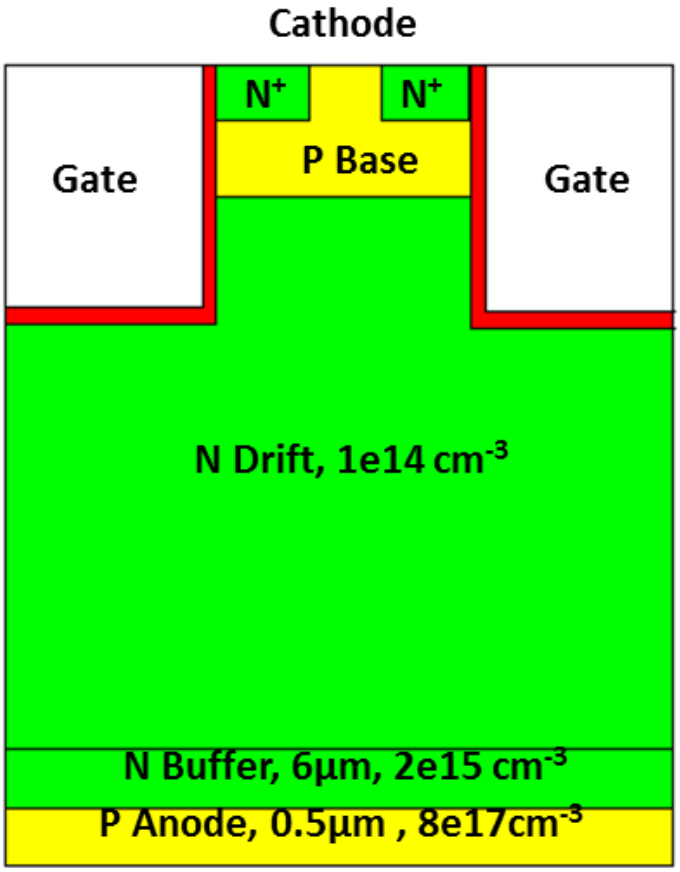


Fig 3.2 Simplified cross-section of a trench gate (Shallow Gate) CIGBT. (Half-Cell)

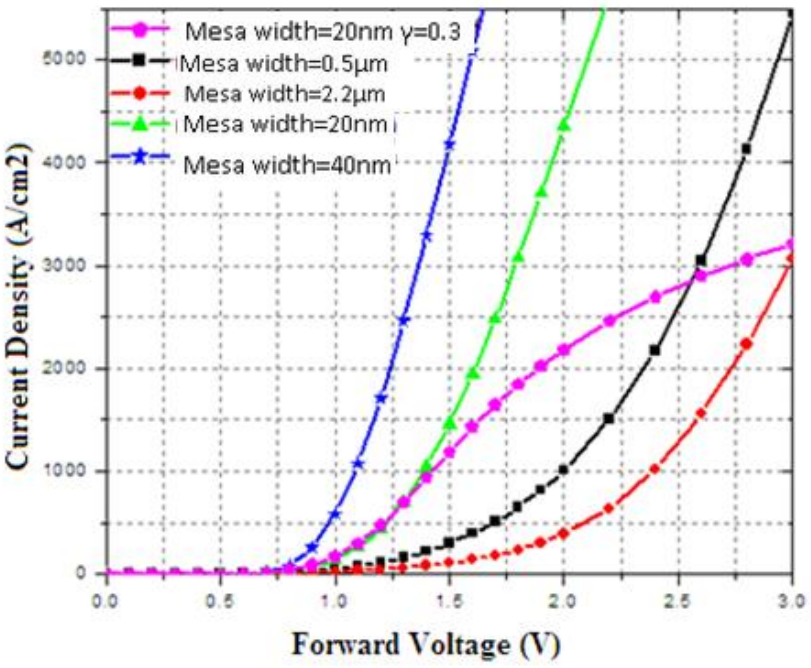
As the power device ratings increase, lower saturation current level becomes pre-requisite in order to withstand onerous short-circuit conditions. Control over saturation current level in IGBT is not possible in IGBT without an increase in $V_{ce(sat)}$[11, 12]. Lowering the self-clamping voltage in CIGBT reduces the saturation current level which can be controlled by varying the N-well depth and concentration. Further, a PMOS trench gate in CIGBT proves to provide lower self-clamping voltage as the charge in the N_{well} region is decreased [11].

3.1 Theoretical Limit of Si IGBT

As discussed earlier, the theoretical limit of Si IGBT has been discussed in detail in [5]. Fig 3.3 shows the structure and simulated I-V characteristics of a 600V IGBT as a function of narrow mesa widths [5]. The device parameters used for simulation in MEDICI™ have been summarised in table 3.1. From Fig 3.3 (b) it can be seen that smaller mesa widths can reduce the on-state voltage of IGBTs. The saturation current of these device can easily be controlled by controlling the anode efficiency, γ (purple line in Fig 3.3) or by using dummy cells (cathode cells that are not connected to cathode or without active channels). It can be clearly seen that the on-state voltage will increase in this case because fewer holes are injected into the drift region thereby reducing conductivity modulation and increasing drift resistance. From an operating view point, there is a need to have 6 to 8 times the rated current for $I_{(sat)}$ to ensure no short circuit failure occurs due to the dynamic increase in current.



(a)



(b)

Fig 3.3: (a) Structure of Si IGBT (b) Typical I-V Characteristics simulated with different mesa width for silicon IGBT. Anode efficiency = 0.8(all) and 0.3 (low)

3.2 Theoretical Limit of Silicon CIGBT

For calculating the theoretical limit of Trench CIGBT, two structures were considered shown in Fig 3.2 and 3.4.

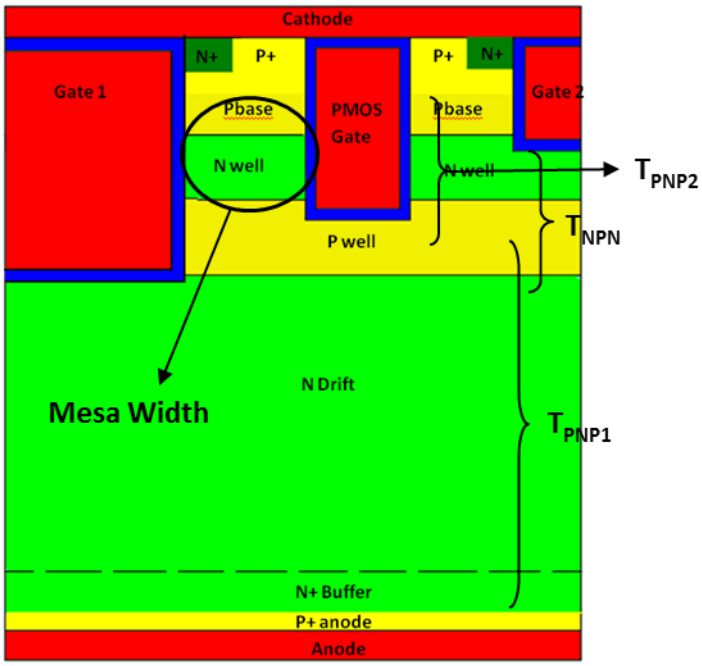


Fig 3.4 Simplified cross-section of a trench gate CIGBT with deep trench gate 1.

The working of planar CIGBT is described in detail in [8] and [13]. The structure of CIGBT can be divided into different regions : the P^+ anode, N drift and P well forming the transistor T_{PNP1} , N drift, P well and N well forming transistor T_{NPN} and P well, N well and P base forming transistor T_{PNP2}. T_{NPN1} and T_{PNP} for the main thyristor and T_{PNP2} is used to achieve the desired current saturation. Gate 1 is the turn-on gate in CIGBT and on application of positive gate voltage the N well is grounded through the inversion and accumulation layers. Since the P well is floating now, its potential will increase with the increasing anode voltage. When the potential drop across the P well/N well junction rises above 0.7V (built-in voltage of Si), T_{NPN} is turned-on and the main thyristor is triggered. Keeping the P well resistance low will ensure the thyristor turn-on without snap-back. Once the thyristor is triggered the N well and P

well potential potentials will continue to increase with the increasing anode voltage. Since the P base/N well junction is reverse biased, the depletion region extends downwards into the N well (this region is lightly doped compared to P base) eventually resulting in punch-through of this region at a certain voltage called 'self-clamping voltage' [13]. This 'self-clamping' feature protects the cathode cells from further increase in anode voltage by ensuring this potential is dropped across P well and N drift regions and also saturated the current in the device. The self clamping voltage can be adjusted by controlling the depth and/or doping concentration of N well region. The device parameters used for simulation in MEDICI™ have been summarised in Table 3.1 and Fig 3.4 shows the structure. PMOS Gate acts as the turn-off gate [11] by providing channels to remove the holes during turn-off of the device. It does not conduct during turn-on of the device and also does not influence the turn-off losses. It simply provide a path for the holes to flow avoiding the area beneath N+ cathode thereby improving safe operating area and dynamic latch-up.

The theoretical limit of CIGBT under the assumptions as mentioned in [5] was evaluated for the structures shown in Fig 3.2 and 3.4 with narrow mesa widths ranging from 20nm-40nm. Figure 3.5 shows the simulated I-V characteristics of a 600V CIGBT as a function of narrow mesa widths. The filled-dotted curves represent the result of deep turn-on gate (Fig 3.4), and the open-doted curves represent the result of shallow turn-on gate (Fig 3.2). Unlike an IGBT, CIGBT used controlled thyristor action hence the current gain of NPN transistor is as important as the PNP transistor to avoid any thyristor latch-up while optimising for better on-state performance.

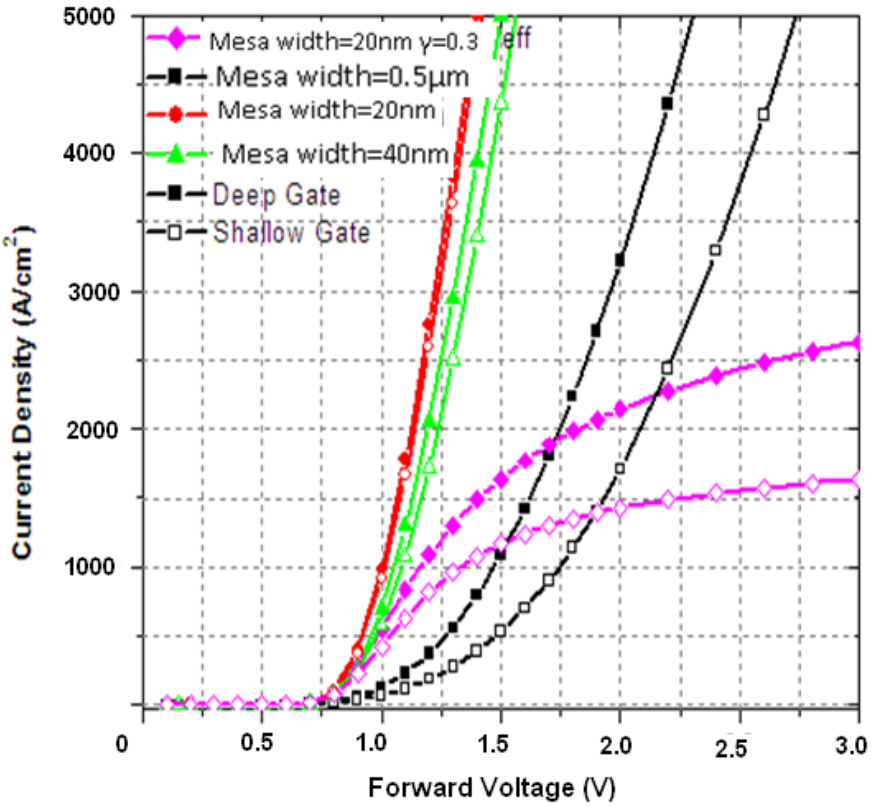


Fig 3.5: Simulated I-V Characteristics simulated with different mesa widths for 600V Si CIGBT.

From Fig 3.5 it can be seen that the theory discussed in [5] holds true for CIGBT as well. It must also be noted that in CIGBT the N well acts as a electron storing region hence the injection enhancement effect described by Nakagawa in [5] is further improved. It can also be noted that deep turn-on trench gate (Gate1) has a better performance than a shallow trench gate. The trench gates are etched deeper into the N_{well} regions and this in turn decreases the self-clamping voltage of the device. The electrons hence have a shorter path via the accumulation region formed by the gate with N well and thereby increase the conductivity modulation by injecting more electrons into the drift region. This in turn reduces the $V_{ce(sat)}$ and improves the on-state performance. Hence, the following sections will be discussed based on CIGBT with deep trench gate 1 as shown in figure 3.4.

3.3 Comparison of Si CIGBT and IGBT results

For a fair comparison between CIGBT and IGBT theoretical limits parameters were chosen to be the same in both devices. Table 3.1 shows the device ratings and design parameters chosen for both devices.

TABLE 3.1 DEVICE PARAMETERS

Parameter	*IGBT*	*CIGBT*
BV	*600V*	*600V*
Threshold Voltage	*4.5V*	*4.5V*
Drift Doping	*$1x10^{14}$ cm^{-3}*	*$1x10^{14}$ cm^{-3}*
Anode doping, thickness	*$8x10^{17}$ cm^{-3}, 0.5µm*	*$8x10^{17}$ cm^{-3}, 0.5µm*
Buffer doping , thickness	*$2x10^{15}$ cm^{-3}, 6µm*	*$2x10^{15}$ cm^{-3}, 6µm*
P base doping, depth	*$4.8x10^{17}$ cm^{-3}, 1.2µm*	*$5.03x10^{17}$ cm^{-3}, 1.2µm*
P_{well} doping, thickness	*N/A*	*1.5µm*
N_{well} doping, thickness	*N/A*	*1.3µm*
$V_{ce(sat)}$ @ 2000A/cm2	*1.25V*	*1.12V*

Figure 3.6 shows the simulated on-state performance of Si CIGBT, IGBT and diode (PN diode) of equivalent ratings (for reference).

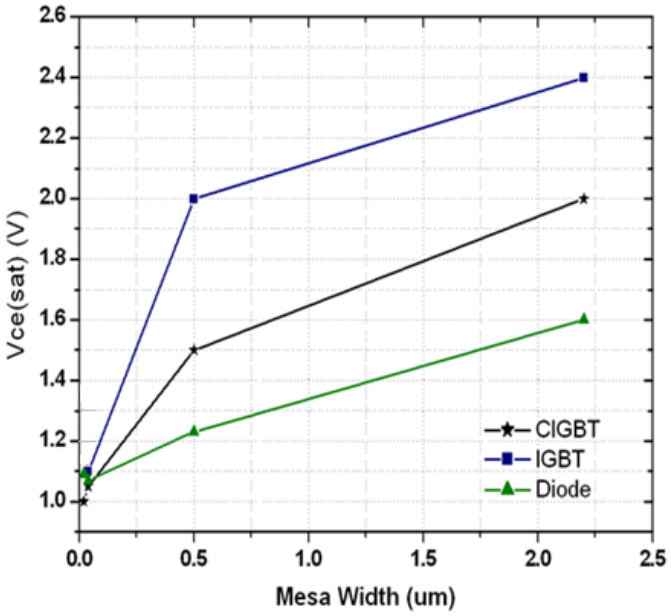


Fig 3.6: Simulated On-state Voltage ($V_{ce(sat)}$) at 1000A/cm^2

It can be clearly seen from the trend in Fig 3.6 that CIGBT performance is closer to that of a diode than an equivalent IGBT due to the controlled thyristor action as explained in section 3.2 due to which it has better on-state performance. The $V_{ce(sat)}$ of IGBT and CIGBT with a mesa width of 40nm is 1.25V and 1.12V at 2000A/cm^2 respectively. The gate voltage used for both IGBT and CIGBT is 15V so as to achieve the same electron enhancement efficiency (τ_e) of all three devices.

$$\tau_e = \frac{I_{electron}}{I_{Total}} \qquad (3.5)$$

Where $I_{electron}$ is the current due to electron flow and I_{total} is the total current due to electrons and holes. Figure 3.7 shows the effect of τ_e on $V_{ce(sat)}$ for both CIGBT and IGBT. As can be seen from figure 3.7, for IGBTs the optimum value of electron enhancement efficiency is around 0.8 below which the on-state voltage increases rapidly. As in the case of CIGBT the electron enhancement efficiency required is less than its IGBT counterpart in order to achieve low on-state voltage. As described in

section 3.2, this is due to the controlled thyristor action which improves the current density in the drift region, therefore, fewer carriers are needed to contribute to the conductivity modulation, in turn leading to lower electron efficiency requirement.

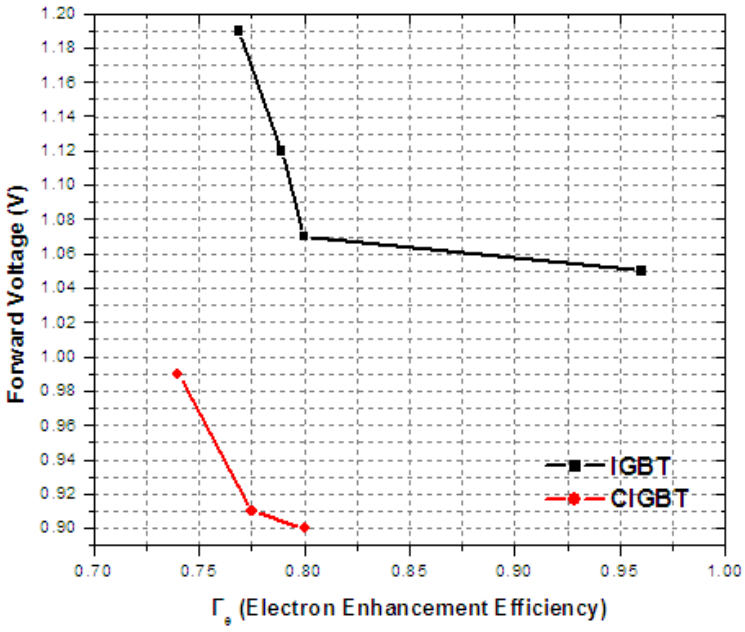


Fig 3.7: Simulated influence of Electron Enhancement Efficiency on On-state voltage of CIGBT and IGBT.

The devices where simulated for switching performance using the chopper circuit shown in figure 3.8.

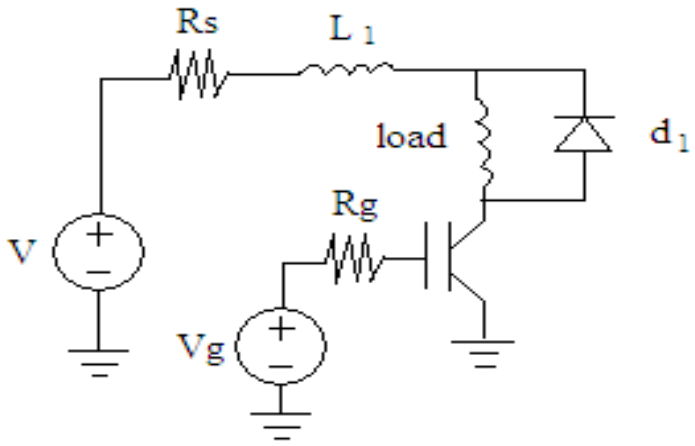


Fig 3.8: Switching circuit used for simulation studies in MEDICI™

Both CIGBT and IGBT were switched at 300V at a current density of 136A/cm^2 at a frequency of 20kHz. The values of R_g is 5Ω, V_g = 15V, R_s = 2.2Ω and L_1 = 55µH. Figure 3.9 shows simulated turn-off losses (E_{off}) – on-state voltage ($V_{ce(sat)}$) trade-off curves. The superior performance of CIGBT in terms of switching losses is clearly evident from these simulation results. This is due to the controlled thyristor action of CIGBT which contributes to the lower $V_{ce(sat)}$. The PMOS gate (turn-off) helps to improve the turn-off losses (E_{off}) by reducing the turn-off times.

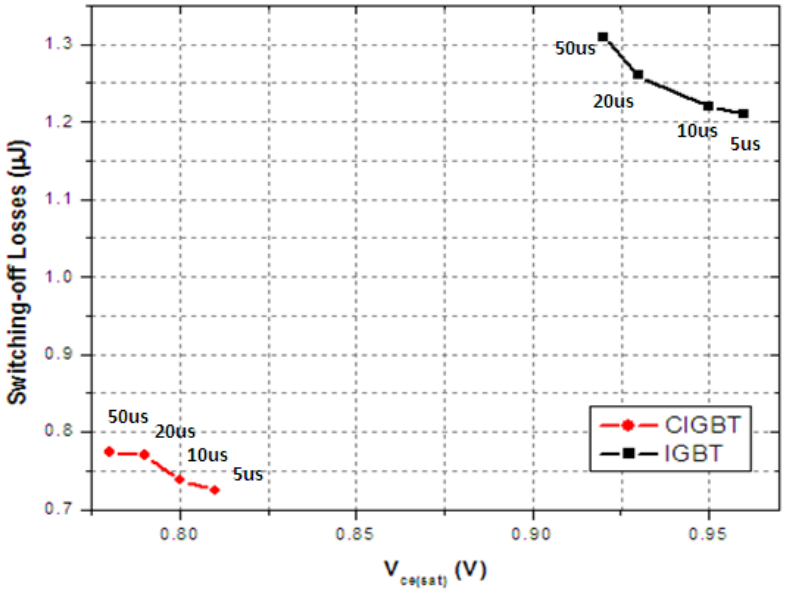


Fig 3.9: E_{off} – $V_{ce(sat)}$ trade-off curves for 600V CIGBT and IGBT.

3.4 Limit of Si Super-Junction CIGBT (SJ CIGBT)

The Super Junction (SJ) concept was originally invented and demonstrated in Si in the 1980s [14, 15]. The concept uses charge balance in drift region through alternate P and N pillars or columns as shown in Fig 3.10. The pillars can be depleted of charges at fairly low voltages thereby making them intrinsic in nature. This will allow flat electric field distribution within the SJ region resulting in higher breakdown voltage supported by thinner drift region. Super Junction was introduced in order to

reduce on-state resistance while keeping the desirable breakdown voltage of the device. The concept was first introduced in MOSFETs and now SJ MOSFETs are now commercially available [16]. More recently, the SJ concept has been extended to IGBTs [17]. Introducing the SJ concept into IGBTs can improve E_{off}-$V_{ce(sat)}$ trade-off thus enabling higher switching speeds. This however comes with increase in saturation current hence affecting the short-circuit performance. A SJ CIGBT was first discussed in [18]. The SJ concept was introduced in a CIGBT to establish the theoretical limit of the device since it was proven to improve the on-state performance of CIGBT considerably in [19]. Fig 3.10 shows the structure of a SJ CIGBT.

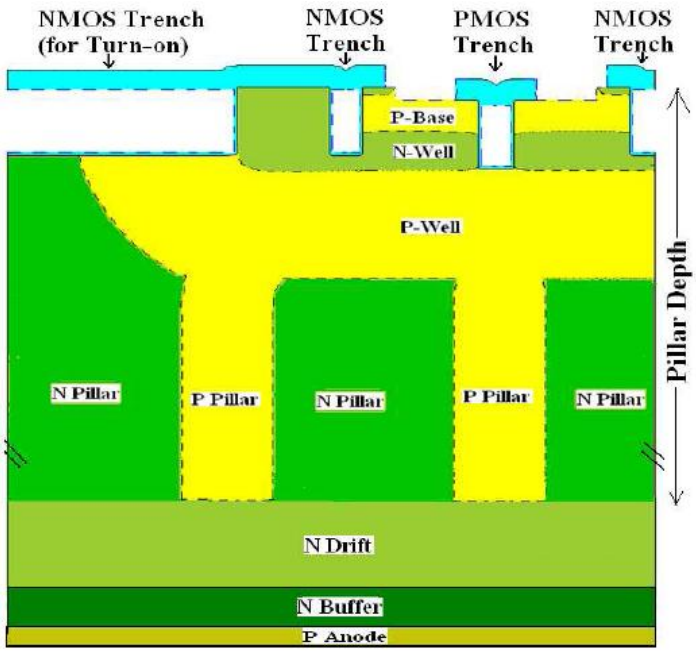


Fig 3.10: SJ CIGBT device structure.[18]

The structure (doping concentrations and depths same as shown in table 3.1) was optimised to attain 600V breakdown. For the pillars to completely deplete, attaining charge balance within the super junction pillars is vital. The following equation was used to size the pillars in order to achieve charge balance (Total electron charge in N Pillar = Total hole charge in P Pillar).

$$dp * Na = dn * Nd \qquad (3.6)$$

where dp and dn are the p- and n- pillar widths respectively and N_a and N_d are the doping concentrations for the p and n- pillars respectively. Figure 3.11 shows the simulated effect of charge balance on breakdown voltage. The optimum point was chosen as the pillar concentration.

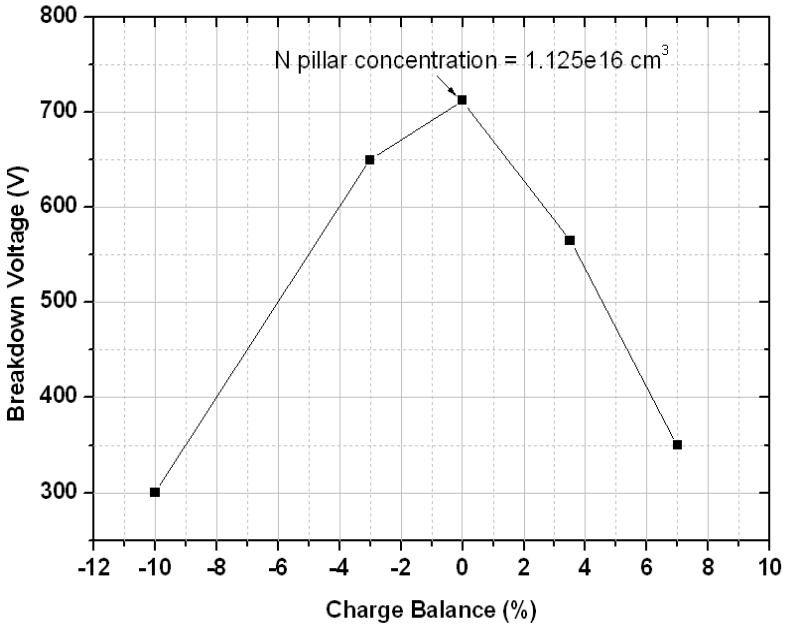


Fig 3.11: Effect of charge balance on BV with P pillar concentration kept constant at 3e16 cm^{-3}

Figure 3.12 shows the influence of pillar depths and doping concentrations on the breakdown voltage of the device. It can be seen that with the increase in pillar depth and Ppillar concentration, the blocking voltage capability of the device increases for a given drift length. A 600V conventional TCIGBT has a drift length of 56µm (shown in Fig 3.4) whereas for a 600V SJ-TCIGBT (Fig 3.10) it is 45µm (at optimum charge balance). This reduction in drift depth is reflected in reduced on-state voltage or resistance. As discussed in section 3.3, to attain the theoretical limit of the device, the mesa width needs to be reduced to a minimum. Figure 3.13 shows the variation of on-state voltage of the device as a function of mesa width.

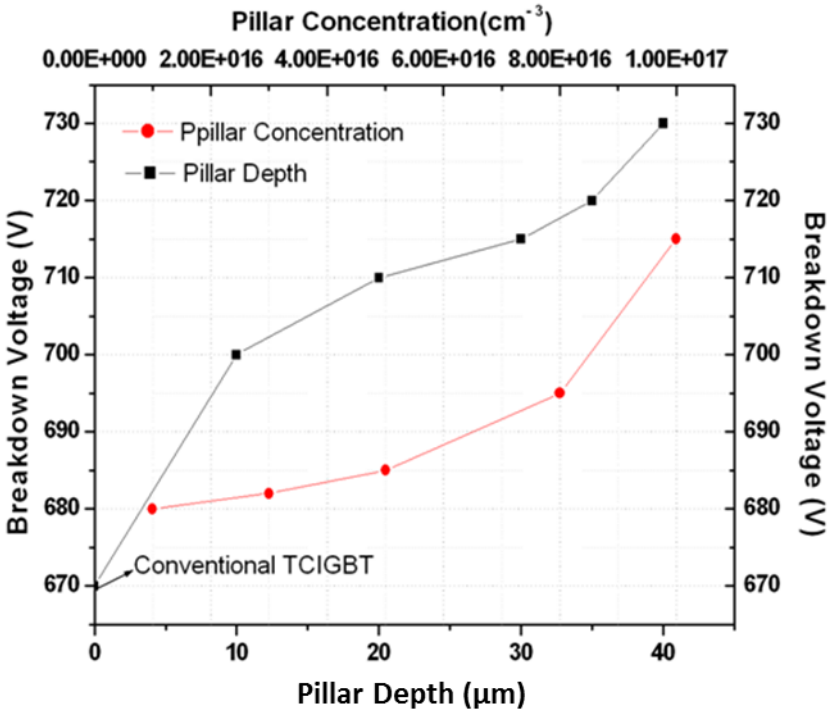


Fig 3.12: Variation of Breakdown voltage of with pillar depths in SJ CIGBT

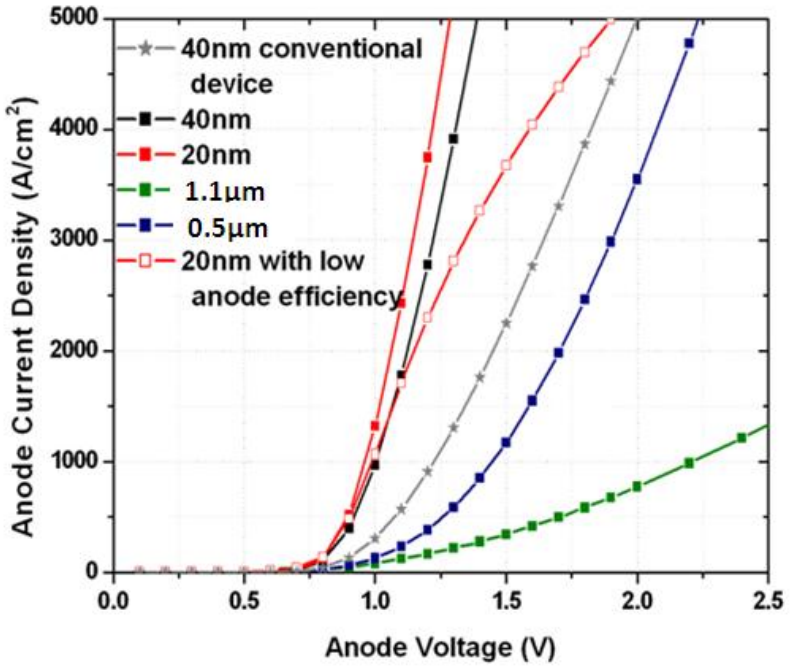


Fig 3.13: Influence of mesa width on the forward voltage drop of 600V SJ-TCIGBT (simulated results)

Reducing the mesa width can decrease the $V_{ce(sat)}$ of the device considerably , in a manner similar to the IGBT structure discussed in section 3.2. Introducing the super junction structure can reduce the Vce(sat) by 18% at 500A/cm^2. Mesa width of 40nm is sufficient to provide very low Vce(sat) (<1.12V) and the anode doping has little influence on this value (see fig 3.14). This indicates the all the current flows by electron diffusion and holes do not contribute to this through conductivity modulation. The SJ-TCIGBT was switched at 136A/cm^2 and Fig 3.14 shows the Energy loss during turn-off (E_{off}) for the device with several combinations of pillar depths and anode doping concentrations. It can be seen that by increasing the pillar depth, it is possible to reduce the turn-off losses of the device without influencing the $V_{ce(sat)}$ of the device to any meaningful degree. Figure 3.15 shows a comparison of on-resistance of all the structures – TIGBT, TCIGBT and SJ CIGBT in Si, with all three being of similar rating.

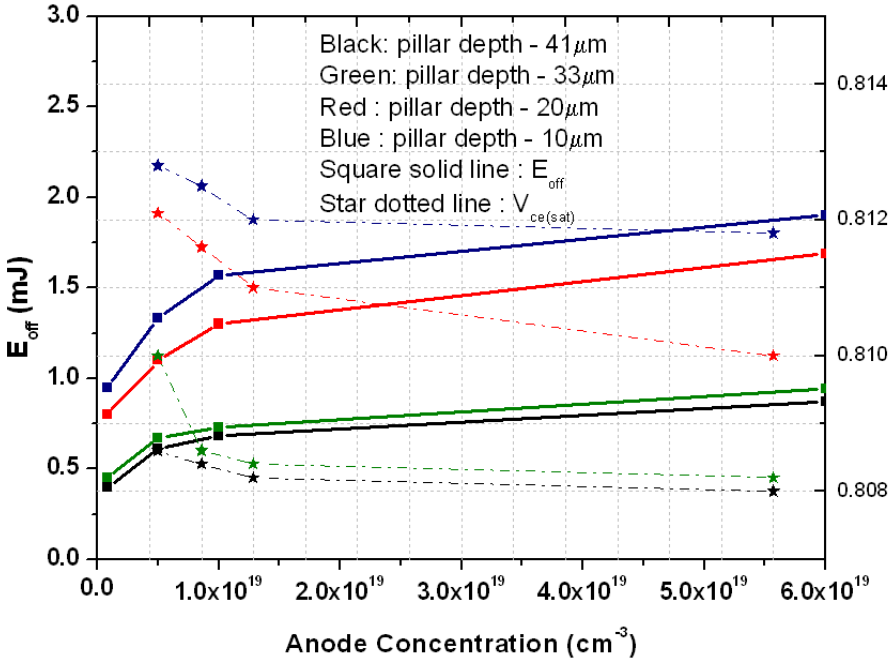


Fig 3.14: Influence of pillar depth on Turn-off losses (E_{off}) and $V_{ce(sat)}$ of SJ TCIGBT.

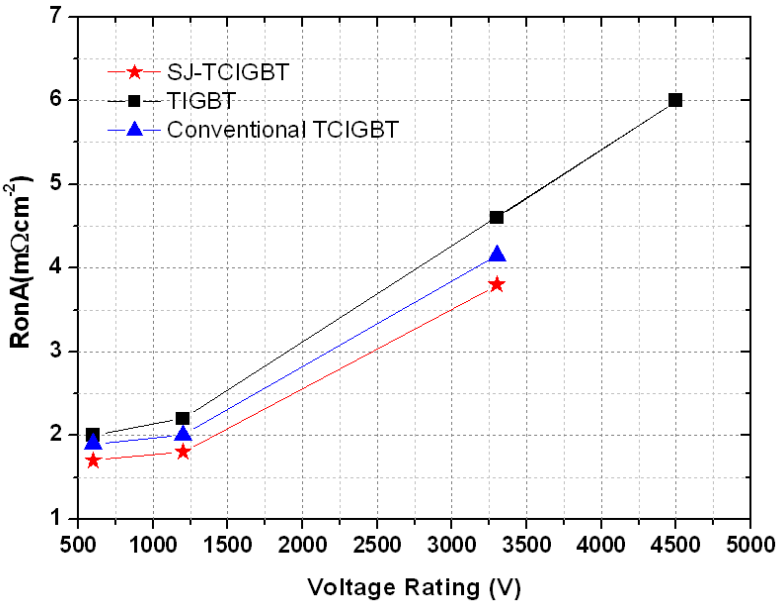
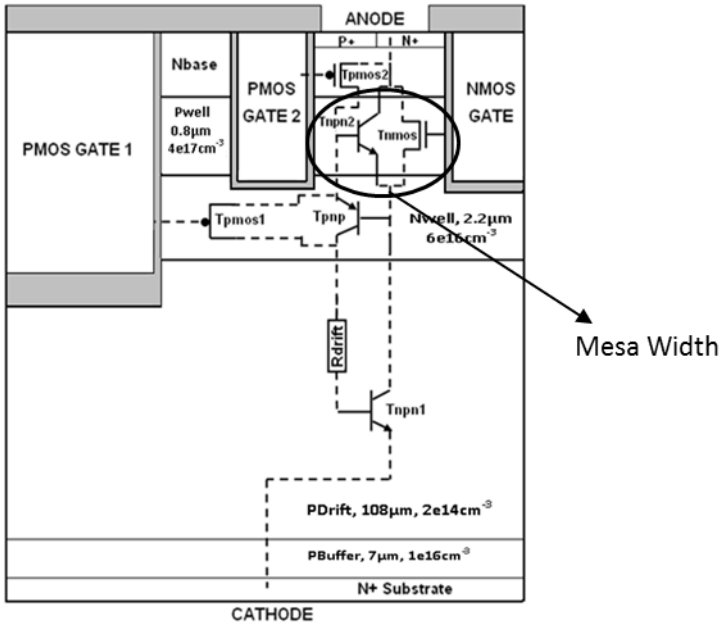


Fig 3.15: Breakdown Voltage versus on-resistance for IGBT, CIGBT and SJ CIGBT with narrow mesa widths

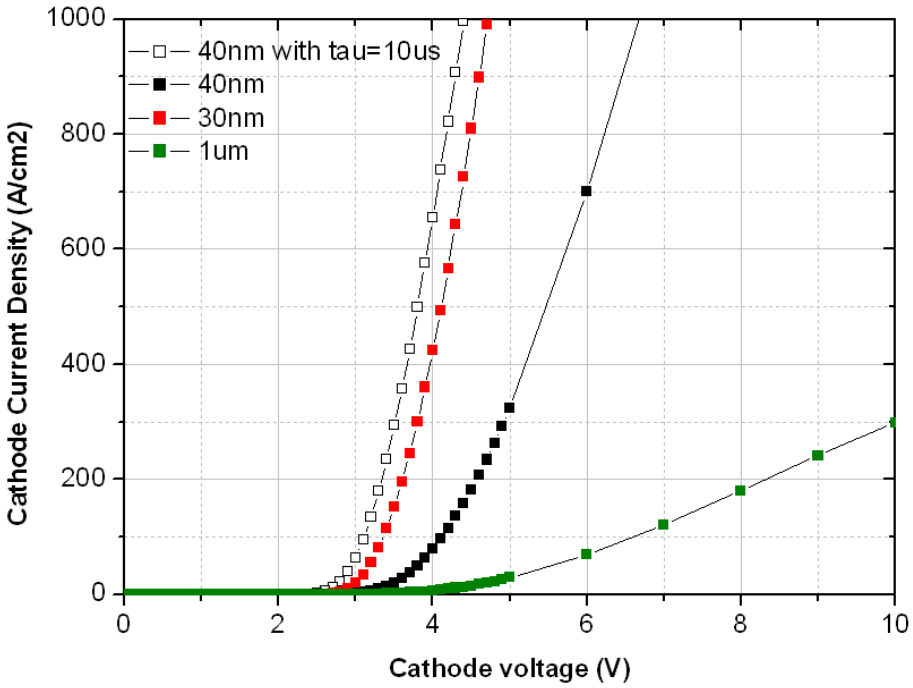
From figure 3.15 it can be seen that the on-resistance can be reduced for higher voltage devices if Super Junction concept is considered (with reduction of up to 20%) due to the reduction in the drift region. However, incorporating the SJ features can result in more complex and costly to manufacture and eventually may translate to more Si thickness and increase the drift resistance.

3.5 4H-SiC TCIGBT theoretical limits

The theoretical limit of 4H SiC in unipolar devices have been established in fig 3.16 [5] and discussed for SJ-MOSFET in SiC in [20]. The specific on-resistance of SiC and Si has been described in chapter 3 of [21]. With all the assumptions mentioned in the beginning of the chapter, SiC TCIGBT was studied using simulations in MEDICI™ with narrow mesa width of 40nm. Figure 3.16 shows the IV characteristics of a 10kV SiC TCIGBT with narrow mesa widths along with conventional device with mesa width 1µm [22] (assumed carrier lifetime is 1µs). Simulation parameters and models are discussed in section 3.6.



(a)



(b)

Fig 3.16: (a) Device Structure (b) Influence of mesa width on the forward voltage drop of 10kV SiC TCIGBT (simulated results) (tau/τ is the lifetime of electrons/holes, same in simulations)

As explained in chapter 1, due to the higher critical electrical field of SiC thinner drift thickness is required to support higher voltages [21]. The E_c of SiC is 3MV/cm in

<0001> [23] which 10 times that of Si (0.3MV/cm) which means that every 1µm of material can support 100V across it in SiC as opposed to 10V in Si [21]. To support 6kV in SiC TCIGBT the drift depth required was 50µm whereas 45µm drift length was required to support 600V SJ-TCIGBT (as discussed in section 3.4).

Figure 3.17 shows the proposed R_{onA} vs BV curves for TCIGBT, Si SJ CIGBT and SiC TCIGBT from this work and Si IGBT proposed in [5] along with GaN HEMT, Si SJ MOS, SiC also from [5]. Considering the carrier lifetime achievable in SiC is low the theoretical limit of the device is simulated at lifetimes of 1µs and 10µs. It can be clearly seen from this figure that SiC TCIGBT can have much lower on-resistance at voltage ratings above 6kV as compared to Si IGBT or CIGBT. This can be attributed to SiC being wide bandgap material and all the device properties mentioned in section 3.2.

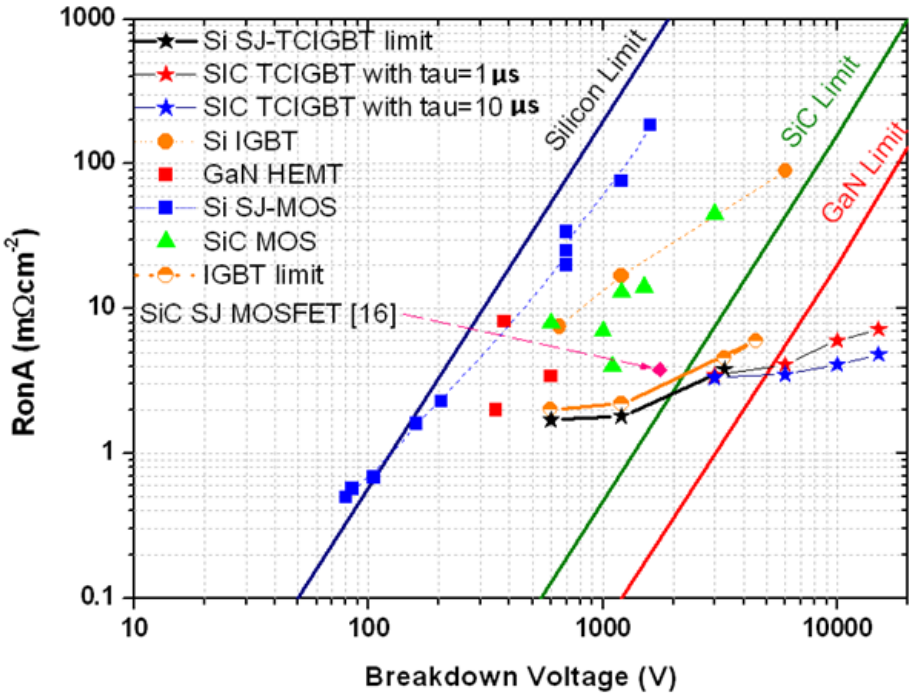


Fig 3.17: Proposed device limits for Si and SiC TCIGBT in this work along with IGBT limits from [5].

From Fig 3.17 CIGBT device in Si and SiC clearly breaks the theoretical unipolar limit of the material and the device performances are much better as compared to other reported devices. It is worth noting at this point that a SJ structure in SiC has not been investigated. A key feature that can be inferred from figure 3.17 is that improvement in carrier lifetime in the SiC material can lead to significant improvement in the device performance in terms of on-state losses at higher breakdown voltages. It can be seen that although Si SJ-TCIGBT has very low on-state at lower breakdown voltages, SiC TCIGBT has better on-resistance at higher voltage ratings (>6kV). Hence for the study of SiC TCIGBT a voltage rating of 10kV was selected for further design and analysis. This will be discussed in detail in chapters 4, 5 and 6.

3.6 Simulation Parameters and models.

Simulation study is of great importance to semiconductor industry. Any device structure can be studied with great ease by just providing its description and operating conditions. Simulations can predict near accurate results for many devices provided appropriate material parameters and models are specified. The simulation tool used throughout the work is MEDICI™. Simulation parameters used for this study has been benchmarked against the work done on SiC IGBT by a group in Purdue University [24] and Figure 3.18 shows the benchmarked data.

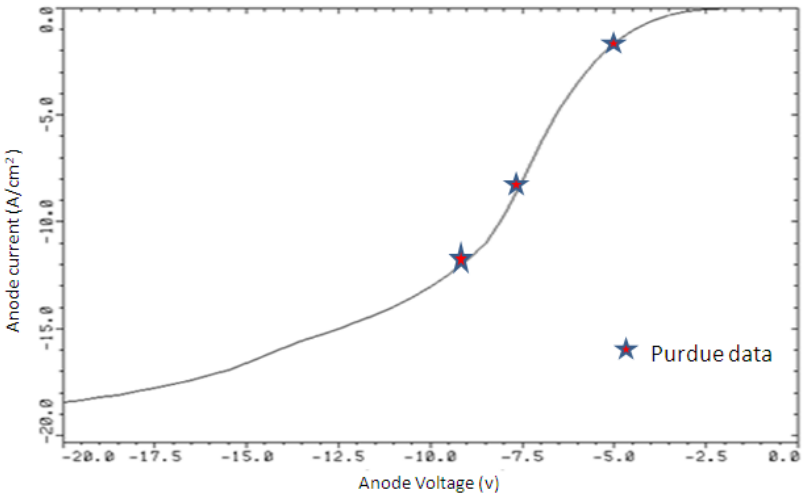


Fig 3.18 Benchmarked Data for a 20kV IGBT [24]

3.2 : Physical Model and Parameters of SiC used for simulations [3]

Bandgap energy [4]	$E_G = 3.23 + 7.036\times10^{-4}\left[49.751 - \frac{T^2}{T+1509}\right]$ (eV)
Electron/Hole mass [5]	$m_e = 0.3713m_0$, $m_h = 1.0001m_0$
Temperature dependence of minority carrier lifetime [6]	$\tau_{n,p} = 39.51\times\exp\left(-\frac{0.105\text{eV}}{kT}\right)$ (μsec)
Incomplete ionization of impurities	$N_D^+ = \frac{N_D}{1+2\exp\left[\left(E_{Fn} - E_C + 0.066 - 1.9\times10^{-8}N_D^{1/3}\right)/kT\right]}$ $N_A^+ = \frac{N_A}{1+4\exp\left[\left(E_V - E_{Fp} + 0.191 - 3.0\times10^{-8}N_A^{1/3}\right)/kT\right]}$
Electron and hole bulk mobility [7]	$\mu_n = \frac{950\times\left(\frac{T}{300}\right)^{-2.8}}{1+\left(\frac{N_{total}(x,y)}{2.00\times10^{17}}\right)^{0.76}}$, $\mu_p = \frac{124\times\left(\frac{T}{300}\right)^{-2.8}}{1+\left(\frac{N_{total}(x,y)}{1.76\times10^{19}}\right)^{0.34}}$ (cm²/Vs)
Field dependent surface mobility [8]	$\mu_{surf,n} = 30\times\left(\frac{10^6}{E_{eff\perp,n}}\right)$, $\mu_{surf,p} = 7.5\times\left(\frac{10^6}{E_{eff\perp,p}}\right)$ (cm²/Vs)
Contact resistivity	$\rho_{c,n} = 5\times10^{-5}$, $\rho_{c,p} = 1\times10^{-4}$ ($\Omega\cdot\text{cm}^2$)

Table 3.2 shows the physical models and parameters used in this work. Appendix A shows further description of parameters and models for this study and Appendix B shows the codes and parameter file used for simulations.

CONCLUSION

This chapter has discussed the theoretical limit of Si CIGBT in detail for the first time and compared it to that of IGBT predicted earlier. Furthermore, SJ CIGBT was simulated for understand the theoretical limit of Si CIGBT for the first time. Establishing these limits of CIGBT showed that at higher voltages (above 3kV) considerable increase in R_{on} of the device will happen and thicker Si will be required to support these voltages. SiC being a wide band gap technology was studied for CIGBT at higher voltages in order to assimilate the advantages of the material to reduce the drift lengths. The simulated results predicted that at higher voltages (>6kV) SiC TCIGBT shows a much better performance than the limits set by Si IGBT and CIGBT. Considering this predicted performance, a 10kV SiC TCIGBT was chosen for further study, in terms of device parameters and physics. Chapters 4, 5 and 6 will describe various structures of SiC TCIGBT and also investigate the performance of this technology in detail. The performance of SiC TCIGBT is also compared to an equivalent SiC IGBT based on the criteria described in chapter 6 of [25]. The simulations have used models and parameters which have been benchmarked to previously reported work (experimentally validated) [3, 26, 27].

Publications

1. K. G. Menon and E. M. Sankara Narayanan "Theoretical Limit of Clustered Insulated Gate Bipolar Transistor (CIGBT)", IEEE Electron Devices, under revision.

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Chapter 4:

Simulation studies on a 10kV P-channel Planar CIGBT in 4H-SiC

Currently IGBT is the device of choice for medium power applications. SiC IGBTs are being extensively investigated over the past few years due to their superior characteristics, notably lower on-state losses at higher voltage ratings than MOSFETs. CIGBTs with their inherent controlled thyristor action have been proven to show better performance in terms of on-state and saturation performance than conventional IGBTs in Si [1] [2]. Both N-Channel planar and trench- CIGBT (CIGBT) has been experimentally demonstrated in Si from 1.2kV to 3.3kV [3, 4]. This device consists of clusters of N-channel MOS cathode cells formed within a floating N-well and P- well. Unlike other thyristor type-devices, CIGBT uses a unique feature called ‘self-clamping’, which together with MOS saturation allows for lower current saturation and protection of cathode cells and gates from high anode voltage surges.

Due to material specific differences, the process, design and working of the device in SiC can be significantly different to that of a Si based structures. Although for fabrication of SiC devices the same equipments as Si can be used, much higher temperatures are needed for annealing of ion implanted regions in order to activate the dopants and remove any lattice damage [5]. It is seen from equation 4.1 that the $R_{on\text{-}sp}$ (Specific on-state resistance) of unipolar devices increases due to the increase in drift region thickness and the reduction of doping concentration in the cathode side of the device which is not desirable. This problem tends to amplify at higher temperatures due to the reduced bulk mobility of carriers [6, 7].

$$R_{on-sp} = \frac{W_D}{qN_D\mu_n} \quad \text{.....(4.1)}$$

Here W_D is the maximum depletion width, N_D is carrier density, μ_n is the electron mobility and q is the charge in the region. Where,

$$W_D = \frac{2BV}{E_C} \quad \text{.....(4.2) } \textit{and}$$

$$N_D = \frac{\varepsilon_S E_C^2}{2.q.BV} \quad \textit{.....(}4.3)$$

Combining the above equations, the specific resistance of the ideal drift region is

$$R_{on-ideal} = \frac{4BV^2}{\varepsilon_S \mu_n E_C^3} \quad \text{.....(4.4)}$$

Various other advantages and disadvantages of unipolar and bipolar devices in SiC have been discussed in [6, 8]. It has been discussed in chapters 1 and 3 why SiC is better material for higher voltage devices. Continual improvement of substrate quality and fabrication techniques have led to the commercialisation of the first SiC based power device - 1.2kV MOSFET by CREE in 2011 [9]. With improvements in the epitaxial growth of SiC, bipolar devices like BJTs, IGBTs, GTOs and thyristors are now being studied intensely [10-13] and although thyristors tend to provide very low on-state losses, they require bulky commutation circuits for control and protection. Hence, voltage controlled devices such as IGBTs are preferred as they offer good on-state characteristics, reasonable switching speeds and a wide safe operating area (SOA). P-channel IGBTs are usually preferred over the N-Channel counterparts for fabrication in SiC as they require an N-type substrate which avoids problems of high resistivity caused by low mobility of holes [14]. P-channel devices are also considered to be more rugged due to higher hole impact ionization and high surge capability[15] as this will lead to better short circuit performance as will be discussed in following chapters.

4.1 Silicon Carbide IGBT – Device Structure and operation.

4.1.1 Planar IGBT in 4H SiC

IGBTs combine the both MOS and BJT characteristics and hence its structure is a combination of these two devices. Fig 4.1 shows the typical IGBT equivalent circuit and Fig 4.2 shows the structure of a p-channel SiC IGBT.

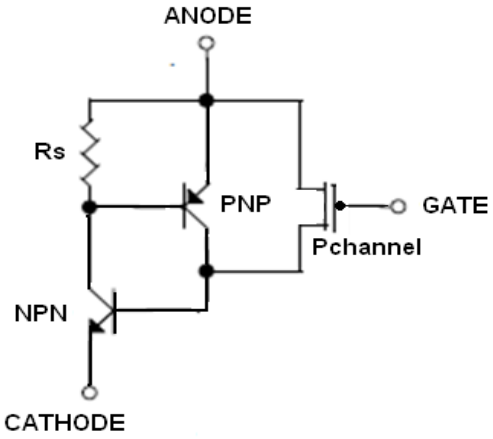


Fig 4.1 P-channel IGBT Equivalent circuit

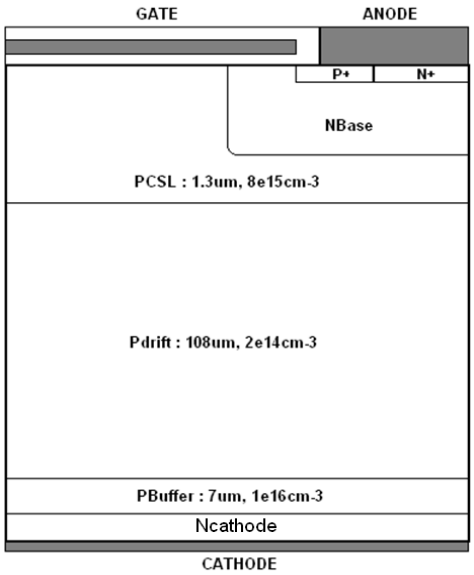


Fig 4.2 Planar SiC IGBT Structure.

The structure of 10kV SiC IGBT is discussed in detail in [16] and [17]. The input to the device is a MOS gate structure and output is a wide base PNP transistor [18]. When the gate voltage is increased above the threshold voltage of the device an

inversion channel is formed within the N base connecting the P+ to the P drift. Holes flow laterally through the channel below the gate in to the drift region reducing its potential. When the N+ Cathode/P-Drift junction turns on, electrons are injected from cathode into the drift region and flow vertically upwards and below the MOS channel into anode. The JFET region shown in Fig 4.2 influences the $V_{ce(sat)}$ of the device as it interacts with the depletion regions of N base and P drift. In SiC, this effect is stronger as diffusion of carriers is very low and hence the on-resistance of the drift region is very high. This is overcome by introducing an additional lightly doped P region called the Current-Spreading Layer (CSL) which lowers the resistance of the drift region by enhancing conductivity modulation as discussed in [15, 19] . The fabrication process of this device is described in [20, 21].

4.2 Silicon Carbide CIGBT – Device Structures and operation.

To improve on the on-state voltage and losses, carrier concentration at the cathode side of the device (in an n-channel device) has to be improved. Hence for this, thyristor technology was considered to be optimal [22]. However, the gate control of such devices is burdensome as they are current controlled devices and as a result MOS-Gated thyristors were developed. Many such devices have been reported to date like MOS-Controlled Thyristors (MCT) [23], Emitter Switched Thyristor (EST) and its variants [24, 25] and Filamentation insensistive BiMOS Switch (FiBs) [26]. All these devices provide very low on-state voltage however suffer either from lower Safe Operating Area as in an MCT, or loses control on device at higher gate voltages as in an EST.

Clustered IGBT (CIGBT), a device developed in 1999 is a three terminal MOS gated thyristor has very low on-state losses, a wide SOA and shows current saturation

even at high gate voltages [27]. This device has a symmetrical cathode structure and is also CMOS/DMOS compatible. N-Channel planar and trench-Clustered IGBT (CIGBT) has been experimentally proven in Silicon from 1.2kV to 3.3kV [3, 4]. The device consists of clusters of N-channel MOS cathode cells formed within a floating N-well and P- well. This device employs a controlled thyristor action to achieve lower power losses in relation to IGBT counterparts. Unlike other thyristor type-devices, CIGBT uses a unique feature called 'self-clamping' as described in chapter 3, which together with MOS saturation allows for lower current saturation and protection of cathode cells and gates from high anode voltage surges. However, due to material specific differences, the process, design and working of the device in SiC is significantly different to that of a Si based structure.

4.2.1 Planar CIGBT in 4H SiC

The half-cell structure of P-channel planar gate CIGBT is shown in Fig 4.3. This device structure is similar to the one in Si [27] and so are the operating principles. Turning ON the Gate above its threshold voltage creates an inversion of holes over the N- base and N well and an accumulation of holes in the P well to ensure that the P drift region is close to the grounded anode potential (hence forming a PMOS gate). Under this condition, the potential of the N well increases in magnitude with the negative N cathode voltage due to 'capacitive coupling'. The P well/N well junction turns on at its bipolar on-set voltage of -3.2V, thereby switching ON the main thyristor formed by N+ cathode, P drift, N well and P well.

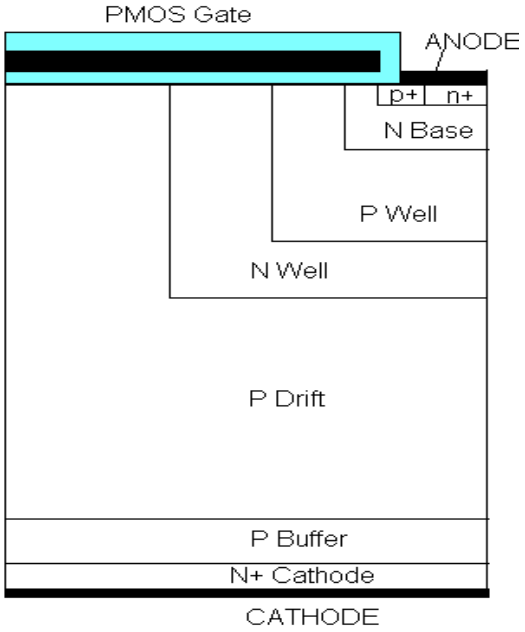


Fig 4.3 SiC planar CIGBT Structure (Half Cell)

After the main thyristor is turned on, the potential across the P well and N well regions increase in magnitude with the cathode voltage. Under high injection conditions, the junctions across the P drift/N well and N well/P well disappear. The depletion region of N-base/P well junction extends into the P well as it is more lightly doped. At a certain cathode voltage, termed as “self-clamping” voltage, the P well is punched through to result in the clamping of its potential and thereby clamping the voltage across anode cells. This unique feature of CIGBT protects the anode and gates from further increase in the cathode voltages.

In conventional Si CIGBT, the self-clamping voltage can be controlled by varying the depth and concentration of P well but since the movement of depletion in SiC is negligible, the self-clamping voltage is very high as shown in Fig 4.4. To realise the structure shown in Fig 4.3, selective epitaxial growth of both N-well and P well can be used. N base could be either grown selectively or by ion-implantation which has

its disadvantages as discussed in chapter 2. Further explanation of the fabrication process of SiC CIGBT is discussed in the next chapter.

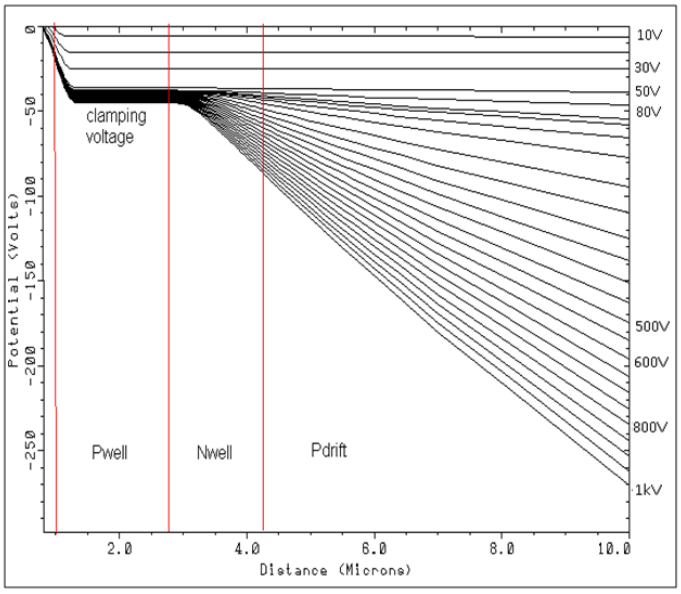


Fig 4.4 SiC Planar CIGBT self-clamping voltage.

4.2.2 Planar CIGBT with NMOS Gate in 4H SiC

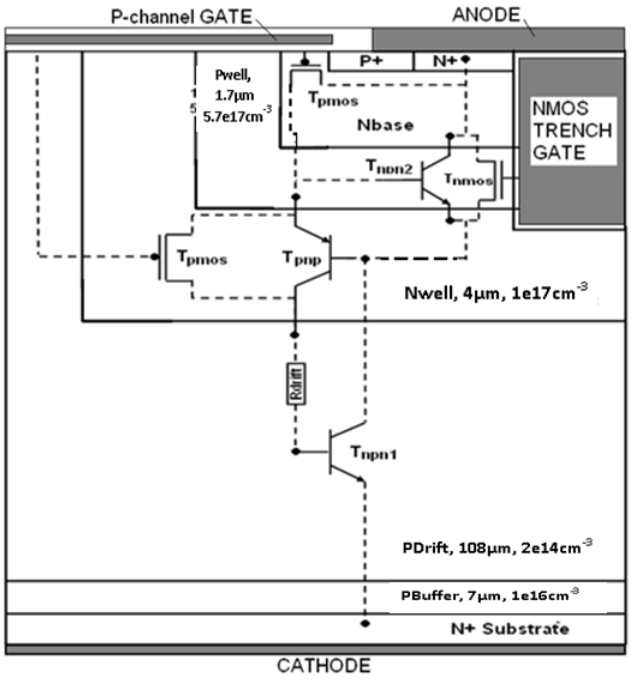


Fig 4.5 SiC Planar CIGBT with NMOS Gate Structure showing its equivalent circuit components.

The half-cell structure of P-channel planar gate CIGBT with NMOS gate is shown in Fig 4.5. For better control of the self-clamping voltage in the device an NMOS Gate reaching the N well is introduced [28]. The NMOS trench gate helps in reducing the clamping voltage as can be seen from figure 4.6 due to the reduction of charge in the P well region below the anode. These NMOS trench gates conducts only during the turn-off cycle, when the gates go positive in voltage, thereby providing a bypass path for the electrons to flow to the anode by avoiding the flow beneath the p+ region. This helps in reducing switching losses and avoiding parasitic dynamic latch-up thereby improving the safe operating area. This has been previously described in N channel Si CIGBT in [28]. This structure can be realised similar to the planar device with the trench technology similar to that in Trench IGBT [17] and [29]. The device parameters are given in the Appendix A.

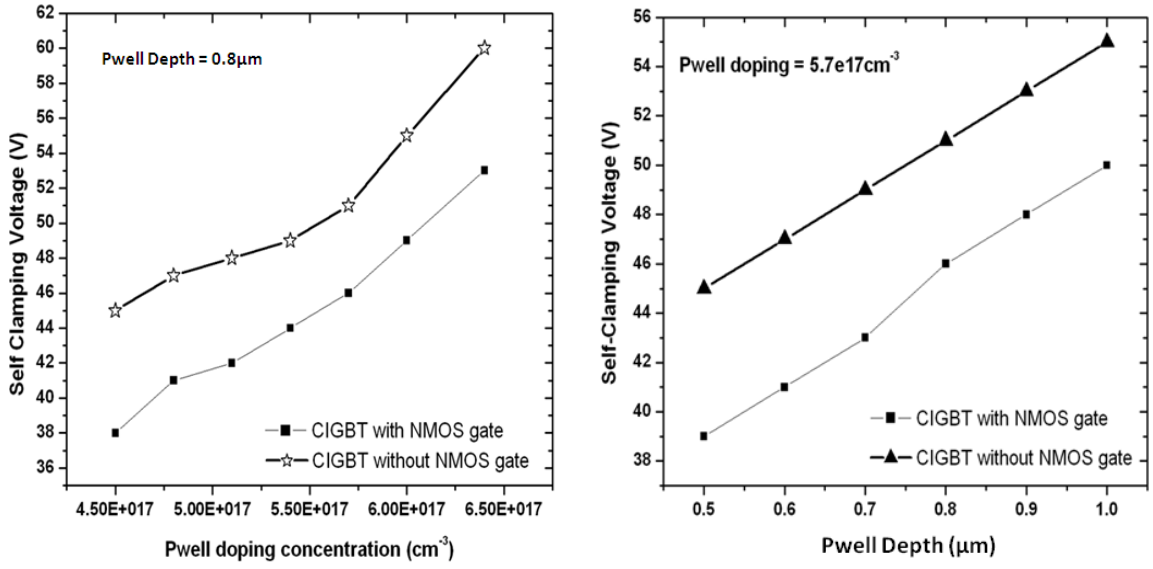


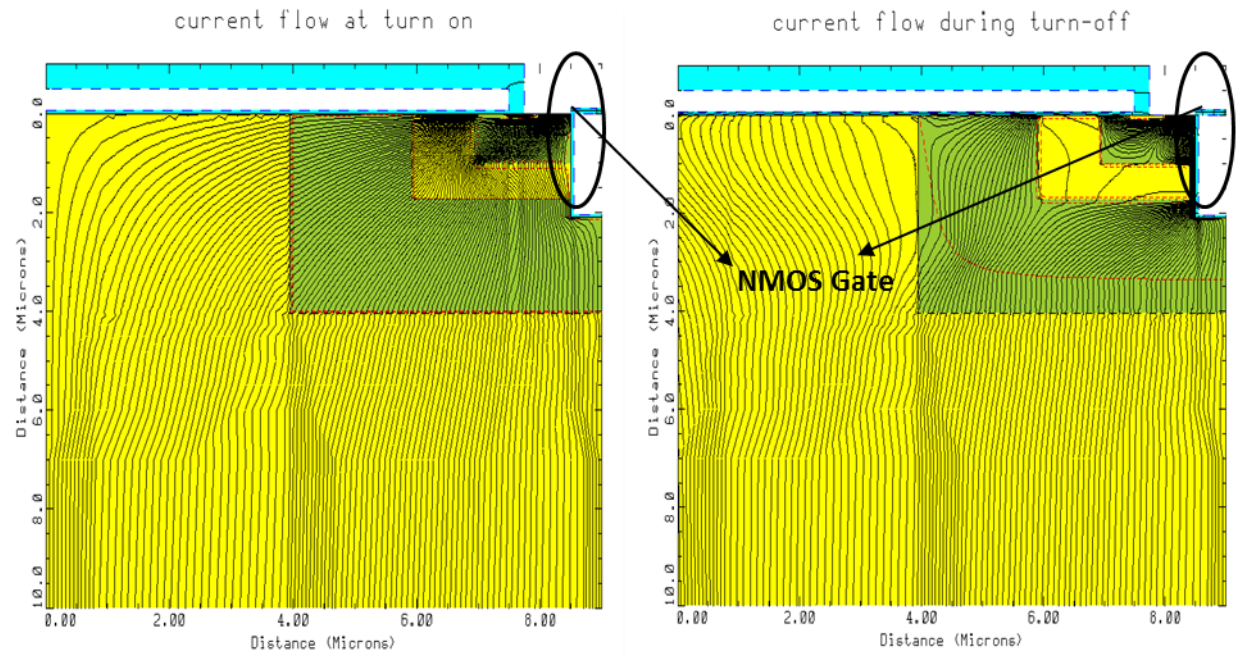
Fig 4.6 Self-clamping voltage variation in SiC CIGBT with P well doping and depth

4.3 PHYSICS OF OPERATION OF Planar CIGBT in 4H-SiC

CIGBT is a three terminal, MOS device with controlled thyristor action, demonstrating excellent on-state, switching and saturation characteristics in Si [28]. Turning on the planar P-Channel gate (Tpmos) above its threshold voltage results in the formation of an inversion layer of holes over the N-base and floating N well regions and an accumulation of holes in the P well region is also formed to ensure that the P drift region is close to the grounded anode potential. Under this condition, the potential of the N well increases in magnitude with the negative N cathode voltage due to 'capacitive coupling'. The P well/N well junction turns on at its bipolar on-set voltage of -3.2V, thereby switching-on the main thyristor (represented by Tnpn1 and Tpnp) formed by N+ cathode, P drift, N well and P well. After the main thyristor is turned on, the potential across the P well and N well regions increase in magnitude with the cathode voltage. The depletion region of N-base/P well junction extends into the P well as it is more lightly doped. At a certain cathode voltage, termed as "self-clamping" voltage, the P well is punched through to result in the clamping of its potential and thereby clamping the voltage across anode cells. This unique feature of CIGBT protects the anode and gates from further increase in the cathode voltages. In conventional Si CIGBT, the self-clamping voltage is optimized by controlling the P well depth and concentration.

However, in SiC, the process margins required to achieve this are much smaller. This can be alleviated by using an NMOS trench gate reaching the N well as shown in Fig 4.5. The NMOS trenches helps in reducing the clamping voltage due to the reduction of charge in the P well region below the anode. These NMOS trench gates conducts only during the turn-off cycle, when the gates go positive in voltage,

thereby providing a bypass path for the electrons to flow to the anode by avoiding the flow beneath the p+ region (see Fig 4.7). This helps in reducing switching losses and avoiding parasitic dynamic latch-up thereby improving the safe operating area [28]. NMOS provides an alternative path for electrons to flow to the anode avoiding the flow beneath the p+ region during turn-off and thus preventing parasitic dynamic latch-up. The half-cell structure of a planar P-channel SiC CIGBT with NMOS trenches is shown in Fig 4.5. CIGBT with NMOS trench gate in 4H-SiC can be realized similar to IGBT using standard photolithographic techniques involving multiple epitaxy and trench formation [5]. The trench depth is chosen in accordance with [6].



(a) Current flow during on-state (b) Current flow during turn-off

Fig 4.7 Current flow during in CIGBT with NMOS gates during (a) on-state and (b) turn-off transient

4.4 PERFORMANCE CHARACTERISTICS OF CIGBT in 4H-SiC

Detailed numerical simulations were performed for both CIGBT (Fig 4.5) and IGBT (Fig 4.2) devices with identical cathode (1e20cm^{-3}, 0.2µm thick). The threshold of planar P-channel MOS in both of the devices is -11V. The NMOS threshold voltage is 9 V. Both devices have a channel length of 0.5µm and oxide thickness of 500Å. All simulations were performed at 700K (=427ºC) to aid convergence and a carrier lifetime of 1µs was used.

4.4.1 Static Characteristics

Having discussed the physics of operation of the device in the previous section, this section will describe the performance of the device in detail. Results of CIGBT device is also compared to an equivalent SiC IGBT. The breakdown of the device under consideration here is 12kV. The forward characteristics of the 12kV CIGBT with NMOS Trench Gate and IGBT are shown in fig 4.8. The CIGBT is snap-back free, unlike other MOS controlled thyristors. Moreover, the CIGBT shows more than 30% reduction in the on-state voltage as compared to an IGBT which is attributed to the increased conductivity modulation in the drift region as shown in fig 4.9. It can be seen from the fig 4.8 that CIGBT shows lower saturation current density than IGBT which is the result of its intrinsic ‘self-clamping’ feature, which is an essential feature to reduce power dissipation under short-circuit condition.

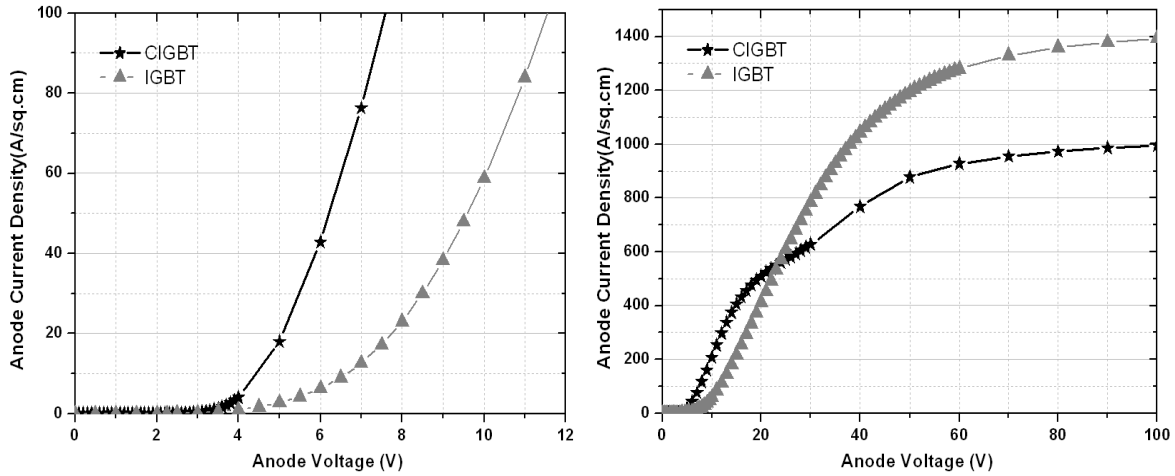


Fig. 4.8 Forward Characteristics of 12kV SiC IGBT and CIGBT at Vg=-20V. (The kink in saturation characteristics of CIGBT is due to Self-clamping voltage and MOS saturation voltages being different)

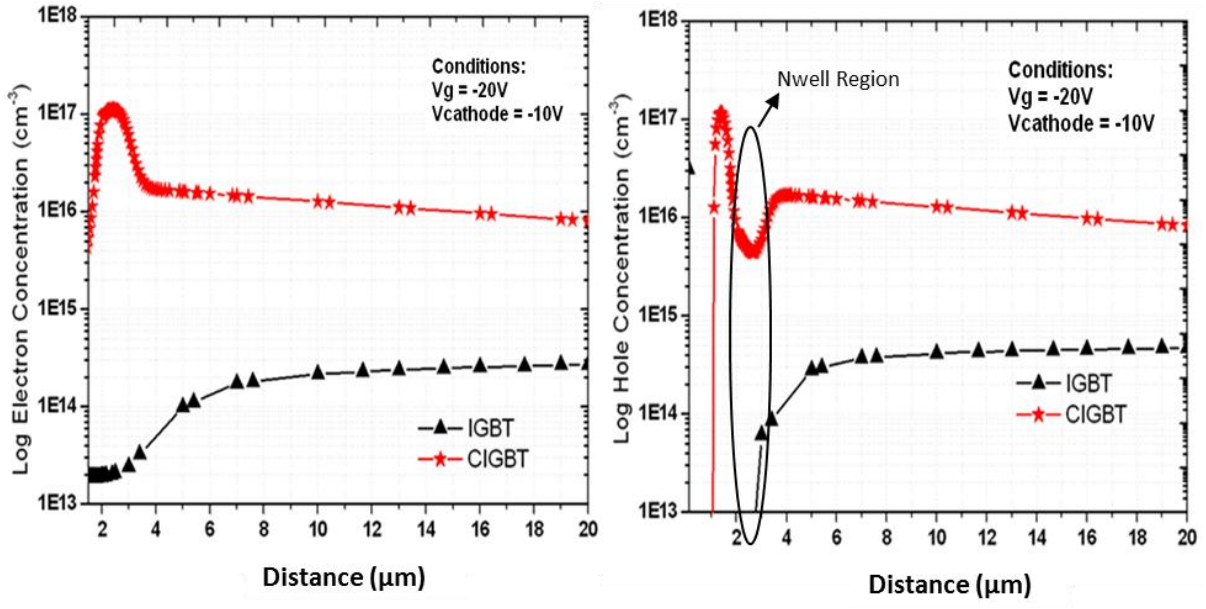


Fig. 4.9 Simulated electron and hole concentrations in the drift region during conduction state of both IGBT and CIGBT.

Furthermore, it can be clearly seen from Fig 4.10 that CIGBT provides lower saturation current level at any given gate voltage. The variation in the on-state voltage for various breakdown voltages is shown in Fig 4.11. In this plot, it is assumed that the on-state losses and switching losses are equal for a given package power limit of 300 W/cm2.

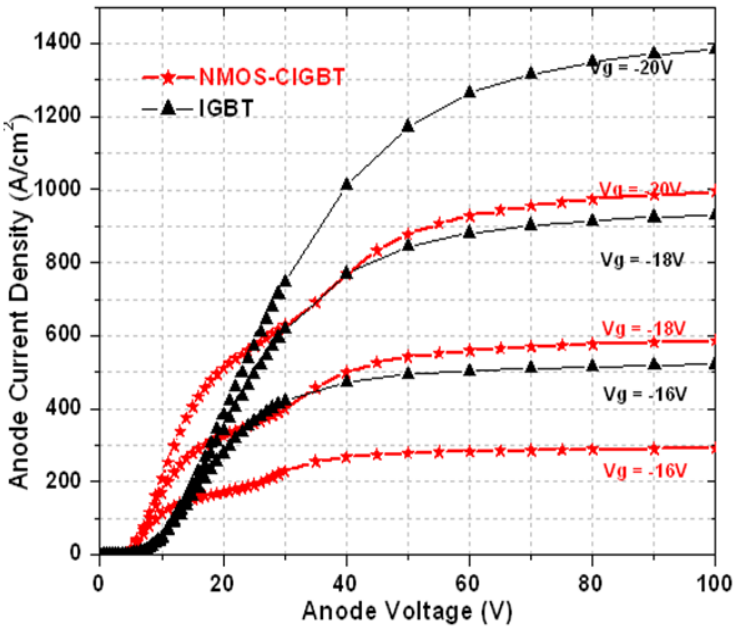


Fig 4.10 : Forward Characteristics of CIGBT and IGBT at different gate voltages.

It can be clearly noted that CIGBT gives a much lower Vce(sat) than IGBT with increasing voltage rating. This implies the CIGBT device technology is beneficial at higher voltages due to thyristor mode of conduction in its on-state. For 12kV rated devices and above, CIGBT can reduce the on-state voltage by more than 40%. This will lead to reduced conduction losses and simplified cooling requirements of the system.

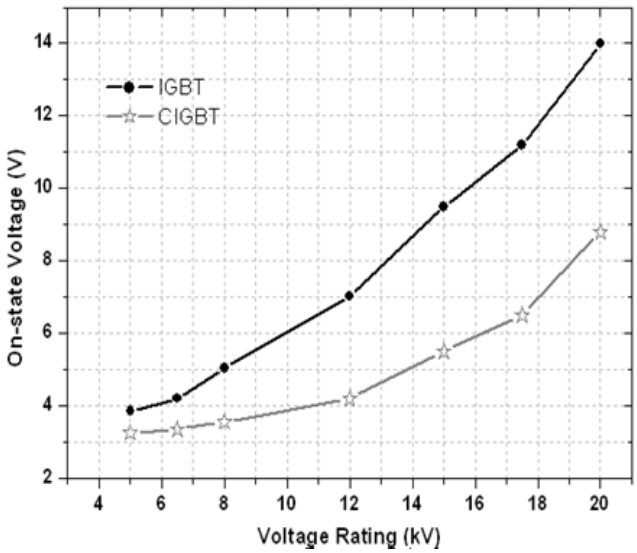


Fig.4.11 Breakdown Voltage (BV) versus On-State voltage (Vce(sat)) curves of 12kV SiC IGBT and CIGBT

4.4.2 Dynamic Characteristics

To simulate the dynamic behaviour of the devices in MEDICI™, an inductive clamped circuit (modelled by a current source) has been used [6] and is shown in fig 4.12.

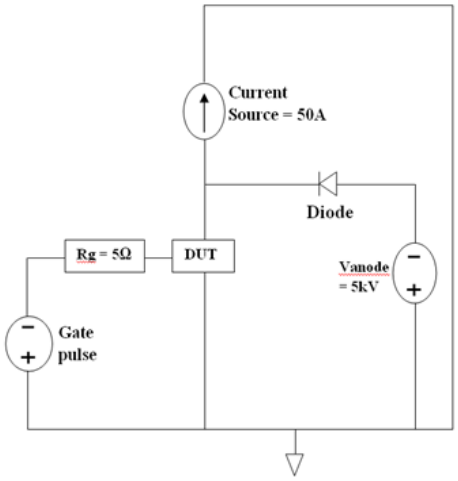


Fig 4.12 Inductive Switching circuit modelled by a current source

The devices were switched at 5kV rail voltage and at a frequency of 20kHz with 50% duty cycle for a 300W/cm^2 package power limit assuming that on-state losses and switching losses are equal. The simulated Eoff-Vce (sat) trade-off curves are shown in Fig 4.13.

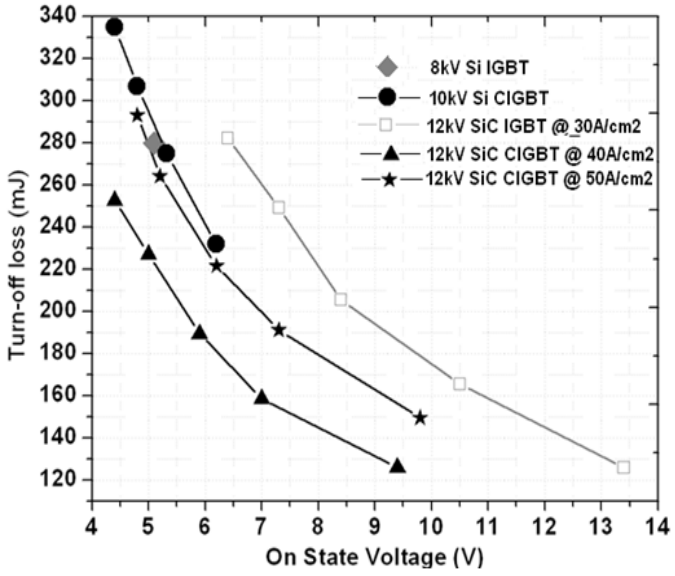


Fig.4.13 Eoff - Vce(sat) Trade-off Curves for CIGBT and IGBT devices

This graph shows that for a given Vce(sat) such as 6.3V, CIGBT technology can provide upto 40% lower turn-off losses by including NMOS Trench Gates. The results also indicate that, the CIGBT within a given package power limit CIGBT could be operated at higher current densities (=50A/cm^2) than an IGBT (=30A/cm^2) and still achieve better trade-off characteristics. This is mainly due to the controlled thyristor action discussion in section 4.3. The losses of 12 kV SiC CIGBT are found to be comparable to 8kV Si IGBT [30] and 10kV Si CIGBT [1] as can be seen from Fig 4.12. The performance improvement obtained by using the CIGBT structure can be beneficial in terms of improving converter efficiencies in a wide range of applications such as HVDC and traction.

4.4.3 Short Circuit Characteristics

An electro thermal simulation of the device under short-circuit condition (cathode voltage= -6kV) was also performed on both CIGBT and IGBT using mixed device and circuit simulator MEDICI™.

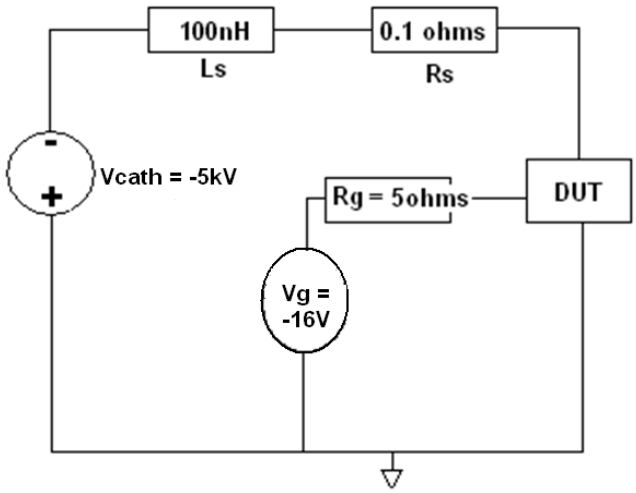


Fig. 4.14 shows the circuit used for modelling short circuit performance of the device.

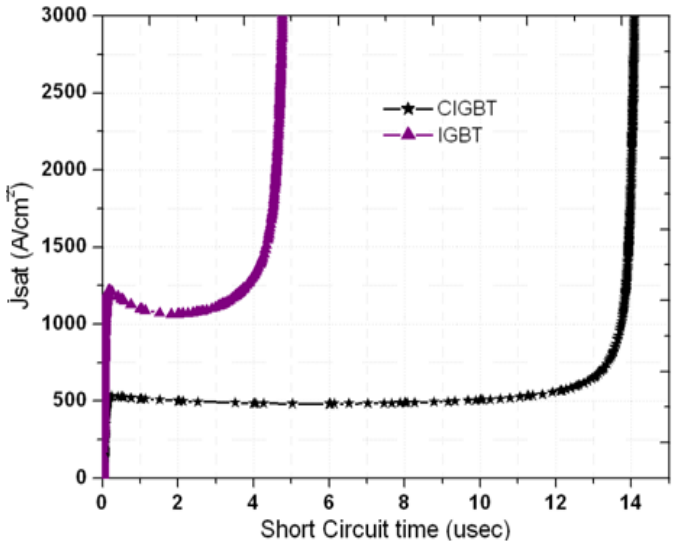


Figure 4.15 Short-Circuit performance of CIGBT and IGBT at 6kV rail voltage

CIGBT as expected supported a much larger short circuit endurance time (12µs) than its IGBT counterpart (4 µs) due to its lower saturation current density which leads to lower heating of the device as shown in Fig 4.15. Higher short circuit endurance times are a prerequisite for high power applications such as HVDC transmission.

CONCLUSION

Comparison of performances of planar IGBT and CIGBT devices in 4H-SiC has been discussed in this chapter. The simulation study shows that due to controlled thyristor conduction the CIGBT technology can provide up to 40% improvement in Eoff-Vce(sat) trade-off as compared to IGBT. Lower saturation current density in CIGBT also leads to an enhanced short-circuit performance. However, due to the complexity in the realisation of clusters within the planar CIGBT (Nbase, Pwell and Nwell regions) in SiC material to fabrication/process limitations, a trench version may be considered a better option as discussed in the following chapters. This is

discussed in detail in the next chapter along with general fabrication process for the device as well. The rest of the thesis will be based on the optimised structure of SiC CIGBT with trench gates as described in chapter 5.

Publications

1. K. G. Menon, L. K. Ngwendson, A. Nakajima, E. M. Sankara Narayanan, G. P. Bruce, "Ultra high performance of 12kV Clustered Insulated Gate Bipolar Transistor (CIGBT) in 4H-SiC", Materials Science Forum, Vols. 717-720, pp. 1139-1142, May. 2012

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Chapter 5:

SIMULATION OF A 10KV P-CHANNEL TRENCH CLUSTERED INSULATED GATE BIPOLAR TRANSISTOR IN 4H-SIC

Vertical trench MOSFET technology was first discussed in 1985 by Ueda et al [1] as a means of improving on-resistance and packing density. Trench gate technology was first introduced to IGBTs in order to realise lower on-state voltages than planar devices [2]. Addition of trench gates not only eliminates the parasitic JFET effect that has been explained in the last chapter but also improve channel density thereby improving on-resistance. Further to this, in 1987 the injection enhancement (IE) effect was demonstrated by Kitagawa et al [3] in IGBT with deeper trenches which can allow for increased injection of electrons as compared to holes. Due to the deeper trench geometry, holes have a thin N^- region to pass through to reach P-base however electron current is not restricted since flow of electrons is through MOS-channel along the trench gate walls. The IE effect allows for enhanced modulation of the drift region and hence combining both trench and injection enhancement (TIEGT) can reduce the on-state voltage comparable to that of a GTO thyristor. Several other trench device technologies have been proposed and discussed, but all of them share one common reliability issue as their gate oxides were exposed to high electric fields during the conduction period. An important consideration for all trench devices is that, care has to be taken during processing to avoid sharp trench corners which can lead to premature breakdown of gate oxide due to electric field crowding.

In this chapter, the Trench Clustered Insulated Gate Bipolar Transistor (TCIGBT) in 4H-SiC is discussed in detail for the first time. Firstly the device structure and physics of operation will be explained followed by the performance characteristics which will be discussed in detail and compared with a corresponding SiC IGBT. A process flow has also been developed for this device, albeit only in theory, and will be illustrated in this chapter as well.

5.1 4H-SiC TCIGBT DEVICE STRUCTURE

Trench CIGBTs have been proposed and demonstrated in Si [4], showing excellent performance in terms of both static and dynamic characteristics. Three feasible structures of trench version of CIGBT with varying trench depths were studied to choose a preferable structure. All the structures are shown in Fig 5.1 – 5.3. The trench widths and depths are in accordance with [5].

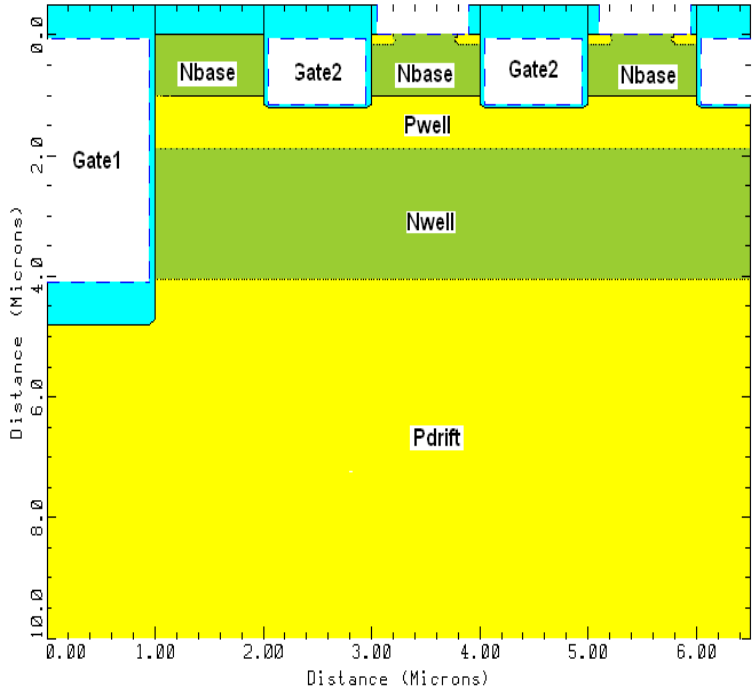


Fig 5.1 : Structure 1 - Trench CIGBT with shallow trenches.

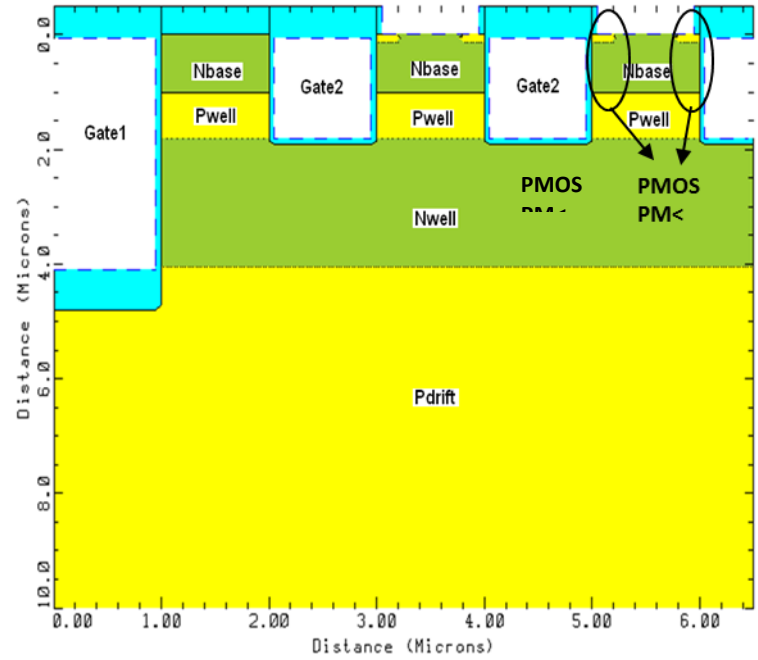


Fig 5.2 : Structure 2 - Trench CIGBT with deep trenches

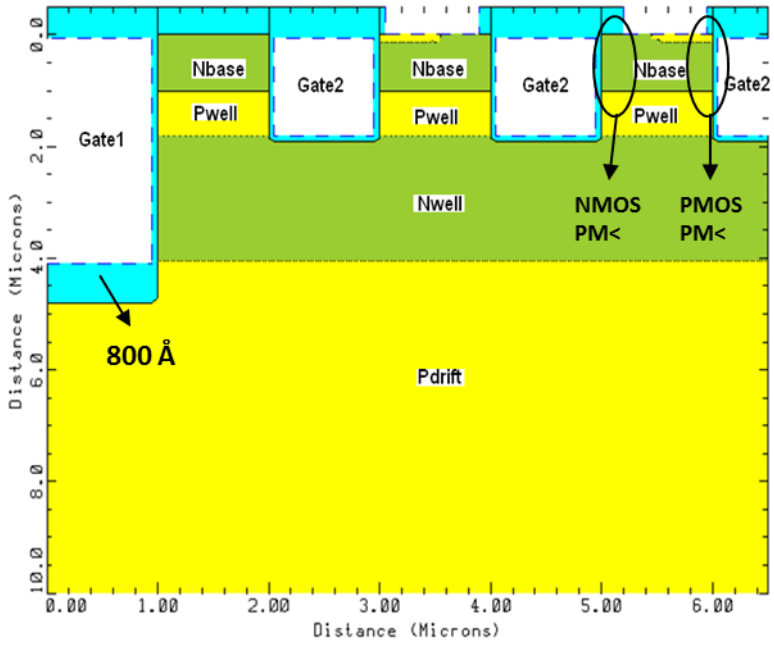


Fig 5.3 : Structure 3 - Dual Trench CIGBT.

In CIGBT, the trench gate 1 reaches below the Nwell and hence the all the layers can be realised by epitaxial growth. However, the oxide thickness at the bottom of Trench gate 1 in T-CIGBT is 800Å in order to support the high voltage without its premature breakdown (it is made to withstand the full blocking voltage). Trench

CIGBT can be realized in a similar manner to a Trench IGBT as in [6] and is explained in detail in section 5.2. All three structures have similar doping parameters and cell-widths as shown in table 5.1.

TABLE 5.1 TCIGBT DEVICE PARAMETERS

Parameter	*Trench CIGBT all structures*
N+ Cathode	*$1x10^{20}$ cm^{-3}, 0.2 µm thick*
P Buffer	*$1x10^{16}$ cm^{-3},7µm thick*
P Drift	*$2x10^{14}$ cm^{-3}, 102µm thick*
N Well	*$6x10^{16}$ cm^{-3}, 4µm thick*
P Well	*$4x10^{17}$ cm^{-3}, 1.8µm thick*
N Base	*$8.9x10^{17}$ cm^{-3}, 1µm deep*
Gate Oxide thickness	*500Å*
Channel Length	*0.5µm*

The Gate 1 has a threshold of 5V acts as the turn-on gate and has no effect on the Vce(sat) of the device. The device remains in the on-state even if the Gate1 is turned off after device is conducting and will be explained in detail in section 5.2. Simulation studies shows that the width between gate 1 and gate 2 does not affect the performance of the device significantly hence this distance is chosen to be 1µm similar to all other trench to trench widths (mesa widths) in the device (Fig 5.4).

Fig 5.5 shows the simulated on-state characteristics of all the three structures of SiC Trench CIGBT in consideration. Str1 refers to Dual Trench CIGBT (Fig 5.3), str2 refers to Trench CIGBT with deep trenches (Fig 5.2) and str3 is Trench CIGBT with shallow trenches (Fig 5.1). Dual Trench structure is so called because it incorporates both PMOS and NMOS trench gates whereas the other two Trench CIGBT structures have only PMOS Trench Gates.

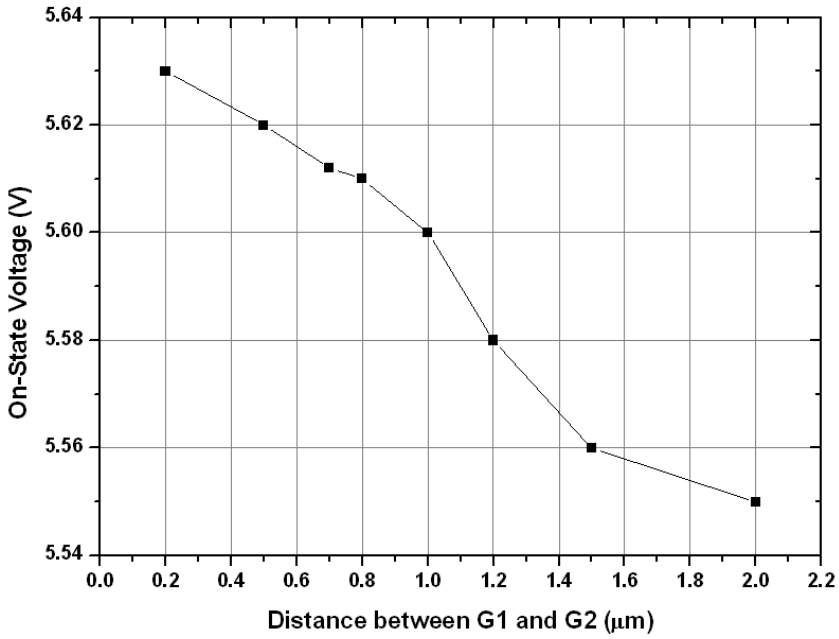


Fig 5.4 Effect on On-State voltage with varying width between Gate 1 and Gate 2

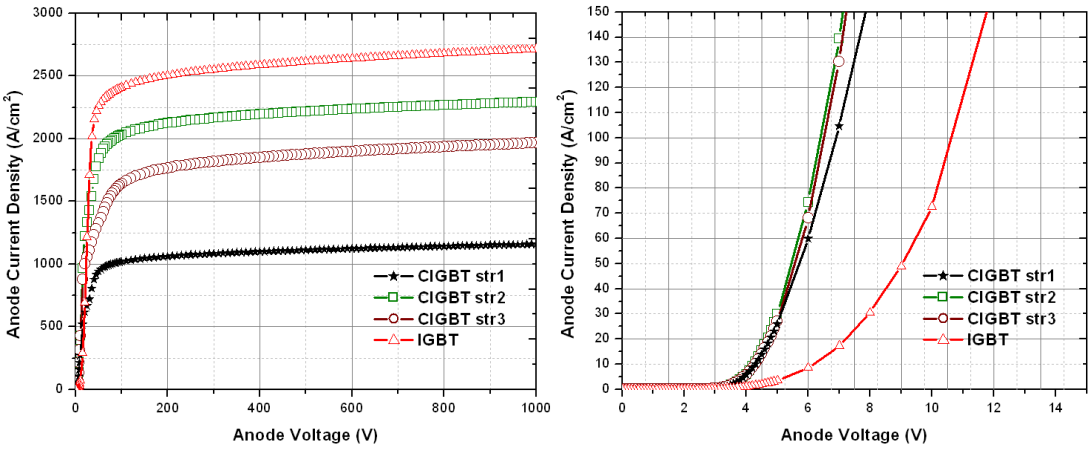


Fig 5.5 On-State and saturation characteristics of Trench CIGBT structures

It is clearly seen from Fig 5.5 that all three CIGBT structures have similar on-state voltage but introduction of an NMOS Trench Gate reduces the saturation current drastically which will be beneficial under short-circuit conditions as there will be lower power loss. Hence the Dual-Trench CIGBT can be considered to have superior performance. Fig 5.6 shows the Eoff- $V_{ce(sat)}$ tradeoff for all the devices and it is

noted that all of them have similar tradeoff. Also shown for reference in Fig 5.5 and 5.6 is an equivalent 4H-SiC IGBT performance.

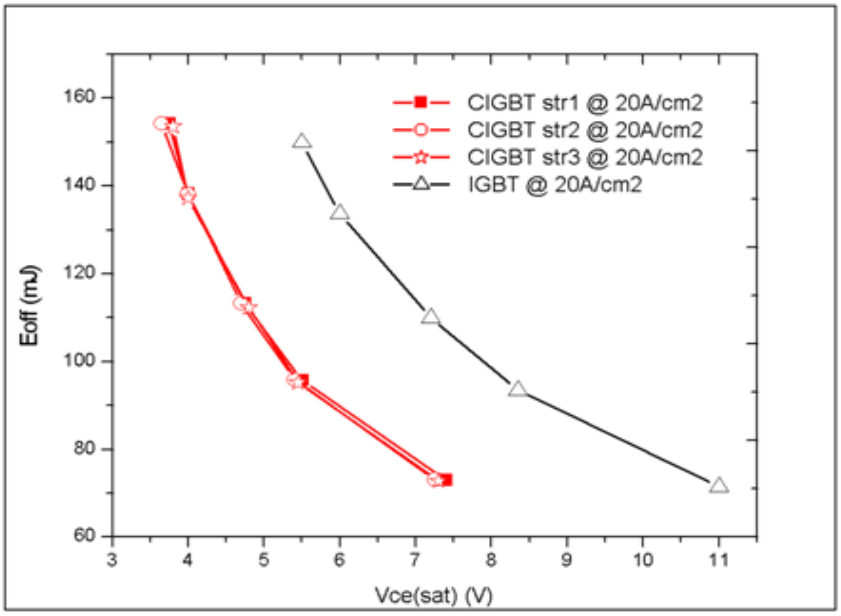


Fig 5.6 Eoff – Vcea(sat) Tradeoff Curves

The half-cell structures simulated in this work along with the equivalent circuit components of two p-channel TCIGBTs (str2 and str3) are given in Fig 5.7 and 5.8. All the gates are connected together to form a three terminal device. Fig 5.9 shows the half-cell of the SiC IGBT structure used for the comparison given in this study. All the regions in this device can be grown by epitaxy as will be discussed in section 5.2. The trench depths were chosen in accordance with [5] .

In the light of the superior performance of the dual trench CIGBT structure (Fig 5.3) in terms the saturation characteristics, this structure was selected for further evaluation in this work and will be henceforth be referred to as Trench CIGBT (TCIGBT).

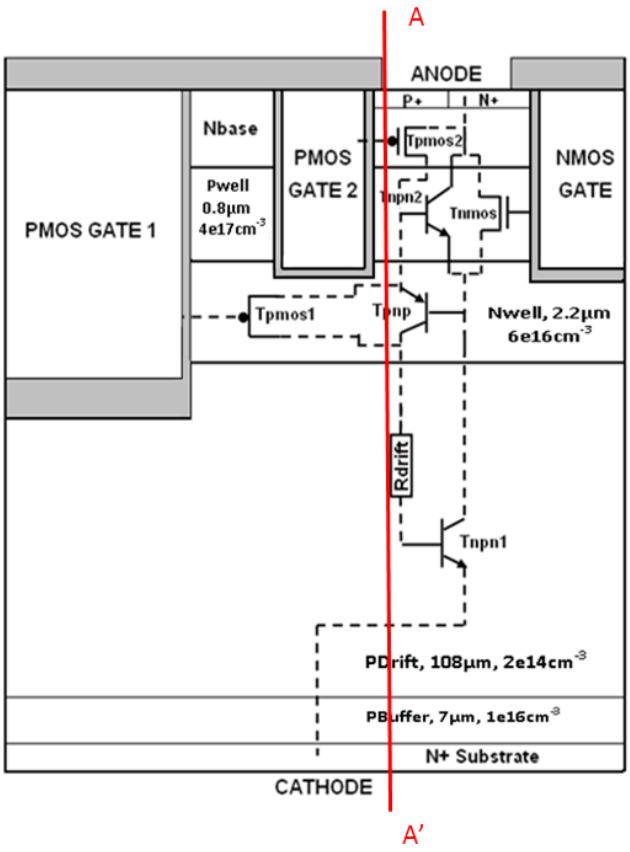


Fig. 5.7 Half Cell structure of a 10 kV p-channel TCIGBT with NMOS gate

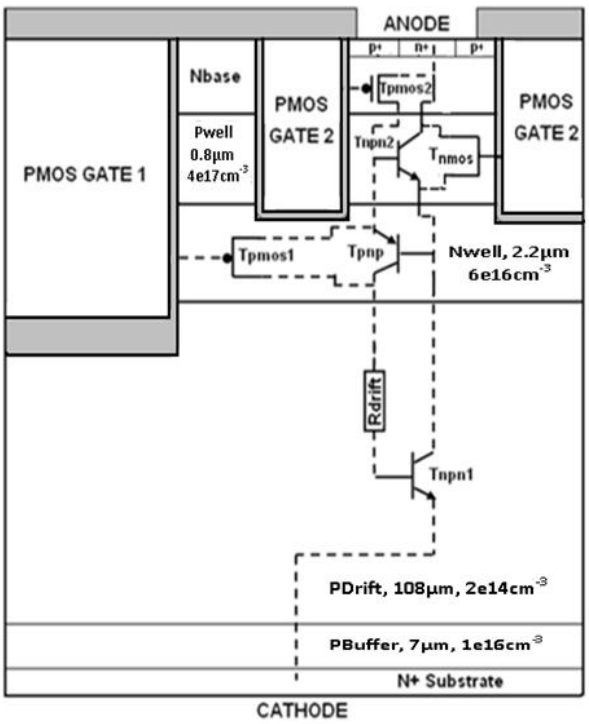


Fig. 5.8 Half Cell structure of a 10 kV p-channel TCIGBT with only PMOS gates

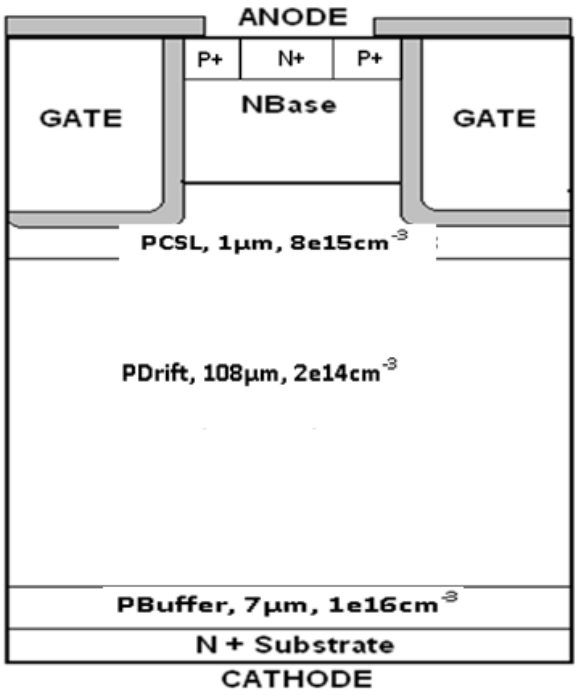


Fig. 5.9 Structure of a 10 kV p-channel TIGBT used in this study.

5.2 PROPOSED GENERAL PROCESS FEATURES FOR 10Kv SiC TCIGBT

The proposed process steps are listed in table 5.2 below. This is illustrated through figures as well for clarity (Fig 5.10 (a) – (e)). As mentioned in previous section, all layers can be grown by epitaxy and is similar to SiC IGBT fabrication in [6].

Table 5.2 : Proposed general process features for 10kV SiC TCIGBT

N+ Substrate, 1e20cm^{-3}
P buffer, P Drift, N well and P well are grown by epitaxy on the N+ substrate.
N base can be formed by epitaxy or by ion-implantation and annealed at high temperatures.
Trench gate regions are etched.
N+ and P+ selectively implanted and annealed at high temperatures.
Gate oxides and polysilicon layers are grown
All contacts metallised.

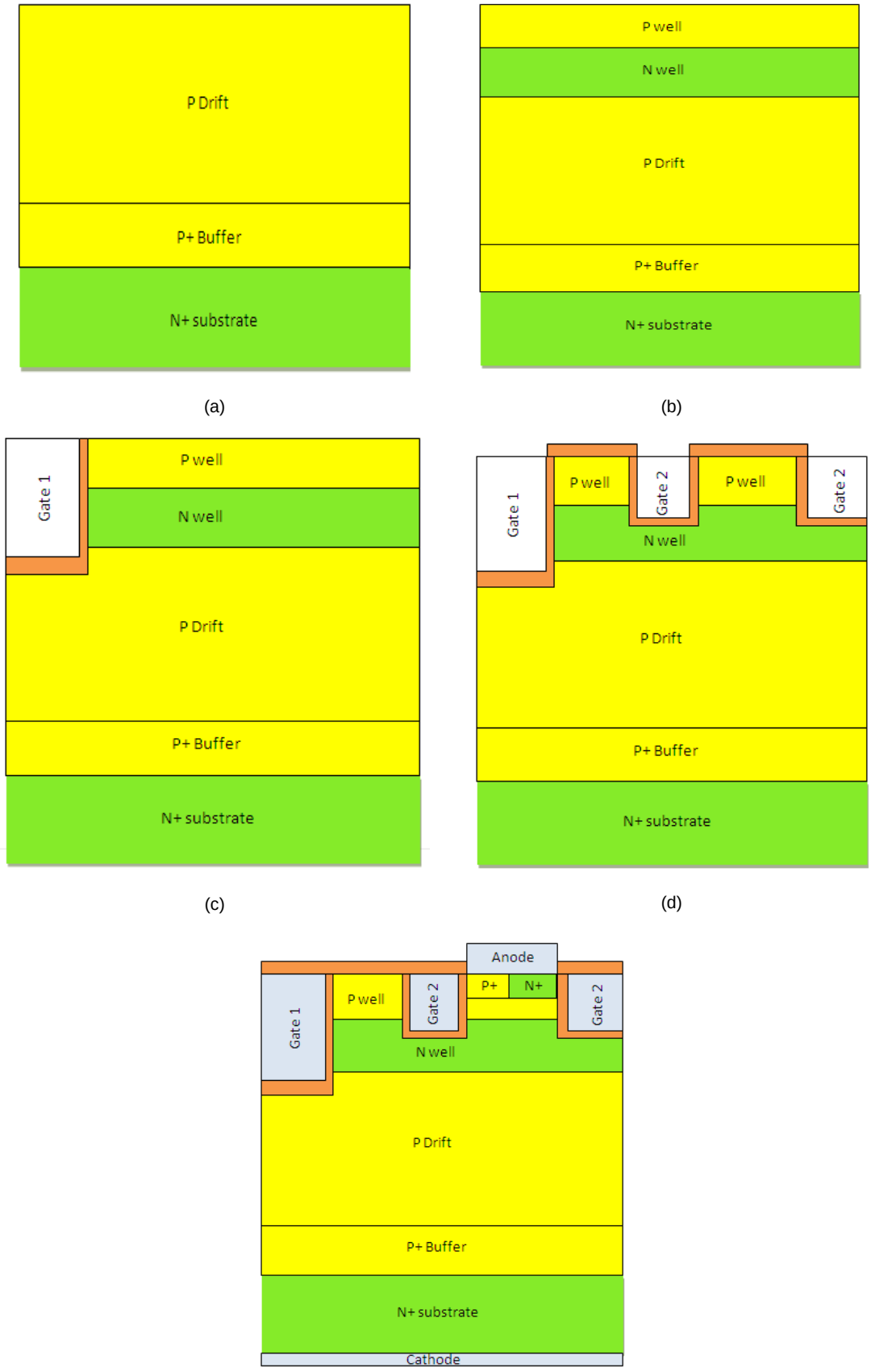


Fig. 5.10(a) Buffer and drift regions grown through epitaxy on N+ Substrate *b)* Nwell and Pwell regions grown through epitaxy. *(c)* Gate 1 etched and Oxide is grown *(d) Gate 2 trenches etched and Oxide is grown (e) P+ and N+ regions implanted and contacts metallised.*

5.3 PHYSICS OF OPERATION OF TCIGBT in 4H-SiC

To study the detailed physics of operation, the device simulation was conducted using the software MEDICI™. Device parameters used for simulation is given in Appendix A. The channel length used was 0.5µm and gate oxide thickness of 500Å. The thickness of oxide below the PMOS Gate 1 is 700Å (thicker than other gates which are 500Å) to prevent premature oxide breakdown. Here, a critical electric field strength of $1X10^7$ V/cm is assumed for the oxide. Parameters from a previously reported p-channel IGBT in 4H-SiC has been used for fitting the simulation parameters [7, 8] and are specified in table I of [9]. Referring to Fig 5.7, on application of negative voltage on the PMOS gates, an inversion layer of holes forms over the Nbase and floating Nwell layers and an accumulation of holes forms over the Pwell layer to ensure that the P drift region is close to the grounded anode potential. Under this condition, the potential of the N well increases in magnitude with the negative N cathode voltage due to 'capacitive coupling' as shown in Fig 5.11.

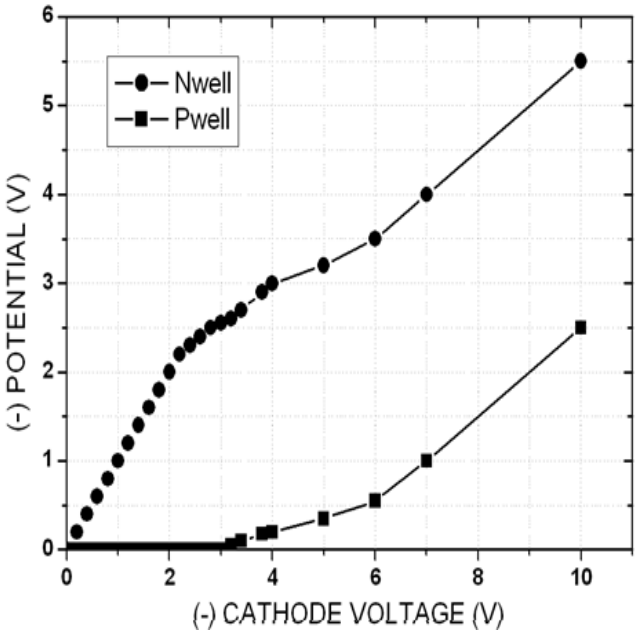


Fig. 5.11 Capacitive Coupling in P channel TCIGBT

The P well/N well junction turns on at its bipolar on-set voltage of -3.2V, thereby switching ON the main thyristor (represented by Tnpn1 and Tpnp in Fig 5.7/5.8) formed by N+ cathode, P drift, N well and P well. After the main thyristor turns on, the potential across the P well and N well regions increase in magnitude with the cathode voltage. At a certain cathode voltage, the potential across the Pwell is clamped thereby preventing any further increase in voltage across the anode cells. This voltage is termed as the 'Self-Clamping Voltage' and happens in Si when the depletion region from the Nbase punches through to the Pwell. However, in SiC as the depletion movement is negligible; the self-clamping phenomenon takes place through the punch-through of the channel of the NMOS region (shown in Fig 5.12(b)) formed by the gates with the Pwell region when the gate voltage is applied i.e. when the potential in the region increases to the self-clamping voltage. This is shown in fig 5.12 (a), (b) and (c)

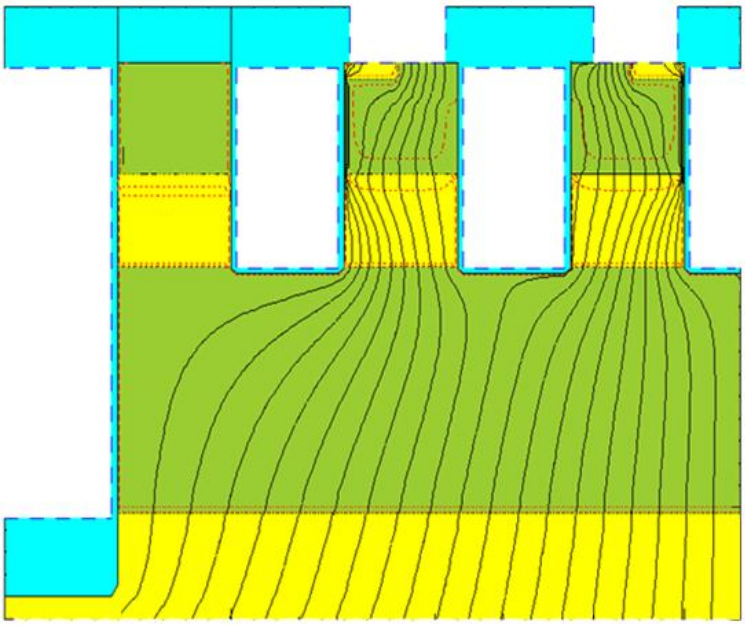


Fig 5.12 (a) Movement of Depletion region within the Pwell region of the TCIGBT at Vcathode = -10V (Before Self-Clamping voltage)

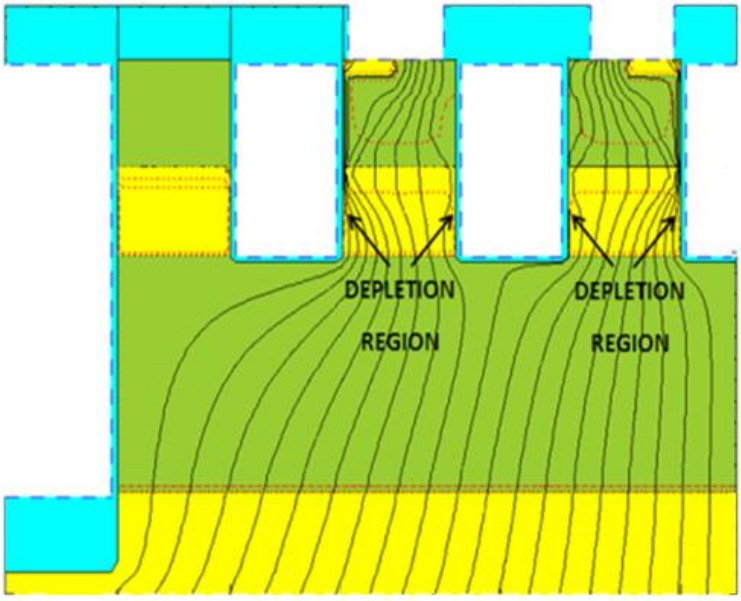


Fig 5.12 (b) Movement of Depletion region within the Pwell region of the TCIGBT at Vcathode =-30V (at self-clamping voltage)

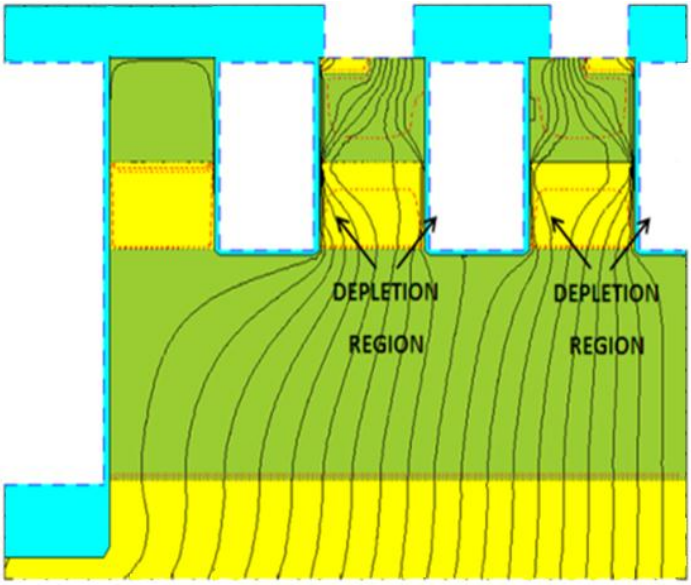
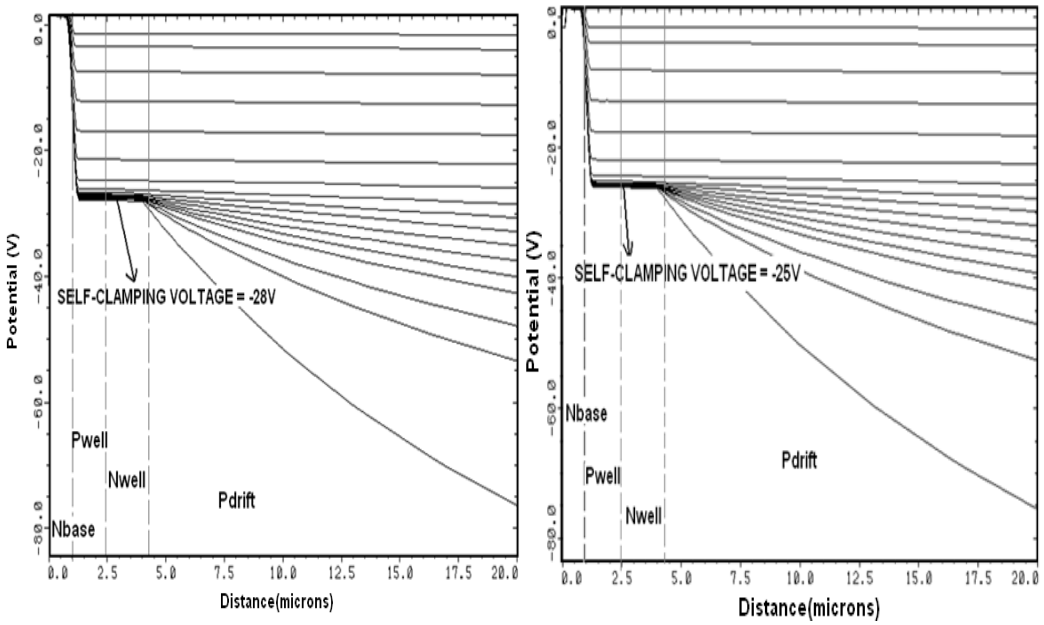


Fig 5.12 (c) Movement of Depletion region within the Pwell region of the TCIGBT at Vcathode = -50V (After self-clamping voltage).

In the above figures both the depletion region movement (shown in red dotted areas) and the current flowlines (black lines) are shown.

Including NMOS trench gates in the structure reduces the self-clamping voltage of the device as shown in fig 5.13(a) and (b) due to reduction of charge within the Pwell region. Additionally, the PMOS trench gates are kept at the same depth. By making

the PMOS trench gates as deep as NMOS gate, the self-clamping voltage of the device is reduced further due to the removal of charge beneath the anode area. These NMOS trench gates only conduct during the turn-off cycle, when the gates go positive in voltage, to provide a bypass path for the electrons to flow to the anode. This reduces the electron current density (J_e) flowing beneath the p+ region which helps to prevent parasitic dynamic latch-up thereby improving the Reverse Biased Safe Operating Area (RBSOA) without degrading its on-state or switching performance [10]. However as PMOS trenches are as deep as NMOS trenches, the Forward Biased Safe Operating Area (FBSOA) is improved only marginally by including NMOS but on-state voltage is improved appreciably as will be discussed in the next section.



(a) *(b)*

Fig 5.13. Potential distribution within TCIGBT structure via simulation (a) without the NMOS trench gates (b) with the NMOS Trench Gates.

5.4 PERFORMANCE CHARACTERISTICS OF TCIGBT in 4H-SiC

5.4.1 Static Characteristics

Having understood the physics of operation of the device in previous section, this section will describe the performance of the device in detail. Results of TCIGBT device is also compared to an equivalent SiC IGBT. The function of Gate 1 as a turn-on gate is explained through the figure 5.14. It is observed that the device does not turn off even if the gate 1 is turned off. It also shows that turning off gate 1 at any point after the device is completely turned on, does not alter its on-state behaviour. It can be reasonably concluded that TCIGBT is a MOS-controlled thyristor device.

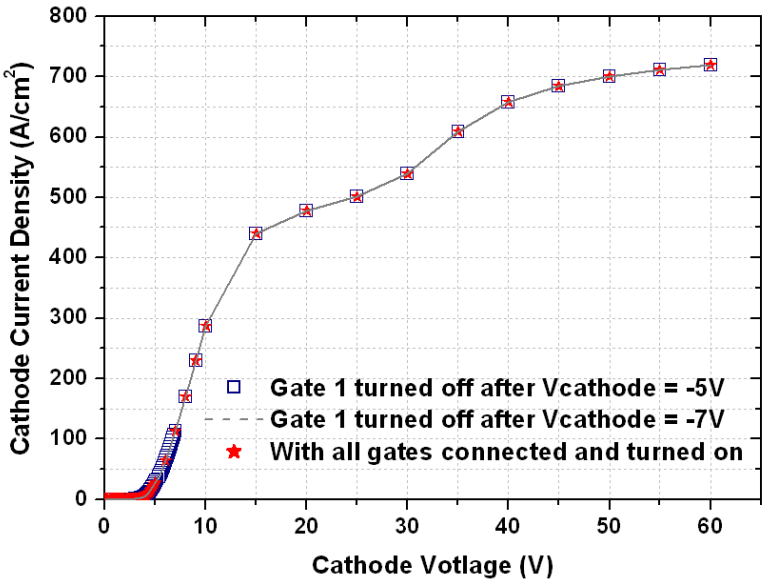


Fig 5.14 Effect of Gate 1 turned off after cathode voltage = -5V and = -7V on the on-state characteristics of TCIGBT device.

5.4.1.1 Breakdown Characteristics

The forward blocking capability in IGBT is determined by the open-base breakdown of the N^+-base/P-drift/N^+-substrate transistor however in CIGBT the voltage is shared between N-well and P-drift. The physics of this is further explained in [11] in Si.

Figure 5.15 shows the predicted peak electric fields in both SiC IGBT and CIGBT and it can be seen that similar to what happens is Si, the peak electric field in CIGBT is lower than that of IGBT due to the presence of N-well region. This can allow for thinner and higher doped drift regions to support similar voltages as compared to IGBT.

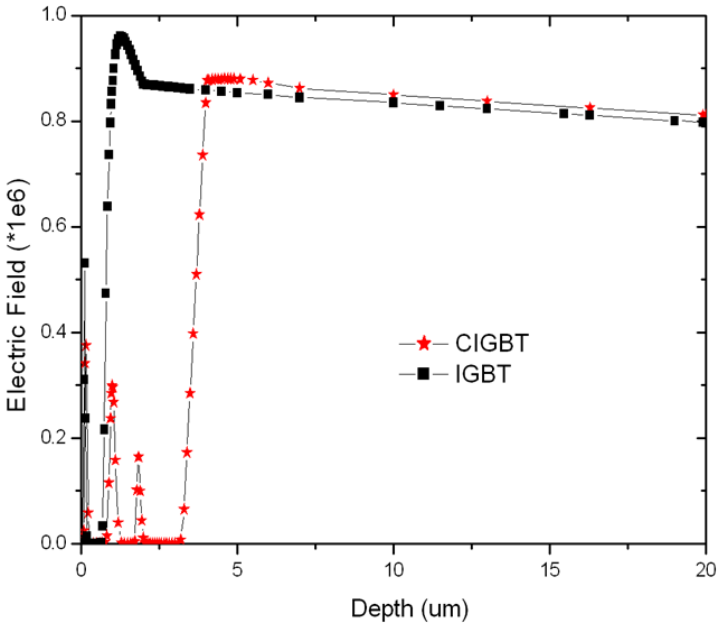


Fig 5.15 Electric field distribution within the device at cathode voltage = -7kV for both SIC CIGBT and IGBT. Cutline AA' shown in Fig 5.7

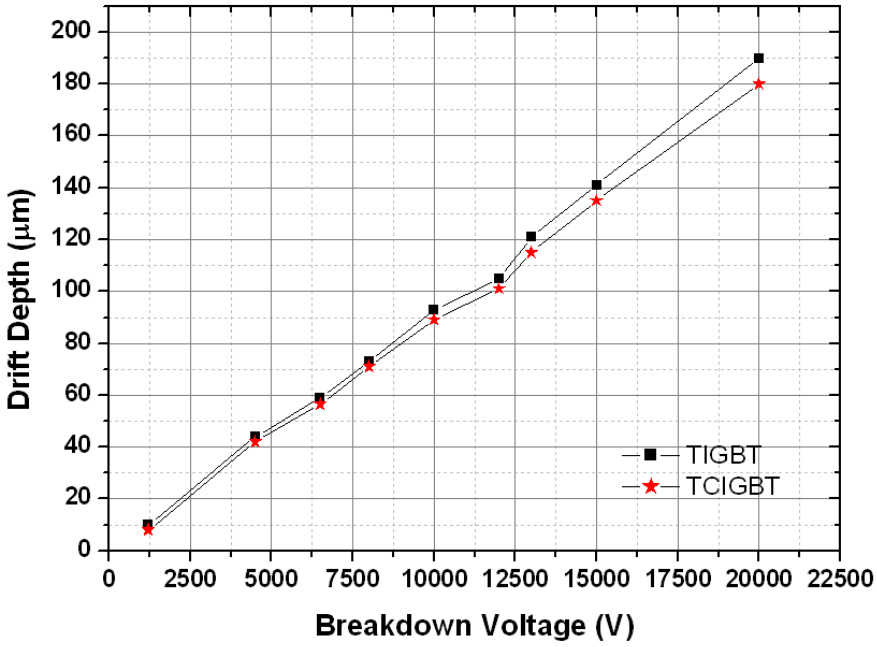


Fig 5.16 Effect of drift depth on the breakdown of device.

Fig 5.16 shows the variation of breakdown voltage of both devices with drift depth. It can be seen that CIGBT needs slightly thinner drift depths to support equivalent breakdown voltages as compared to an IGBT. This becomes more prominent at higher voltage ratings. For the simulations in this work, the drift depth is 100µm and doping is $2x10^{14}cm^{-3}$ for both IGBT and CIGBT in order to support 10kV forward blocking voltage. This is to enable a fair comparison between the two devices as explained in [12].

5.4.1.2 On-State Characteristics

Fig 5.17 shows the on-state characteristics of both TCIGBT and TIGBT. NMOS Trench gates improves the Vce(sat) of TCIGBT by about 5% at a current density of 50 A/cm^2. TCIGBT shows an improvement of more than 30% in the on-state voltage as compared to TIGBT devices. This is due to the enhanced conductivity modulation in the drift region due to the thyristor action in the TCIGBT structure.

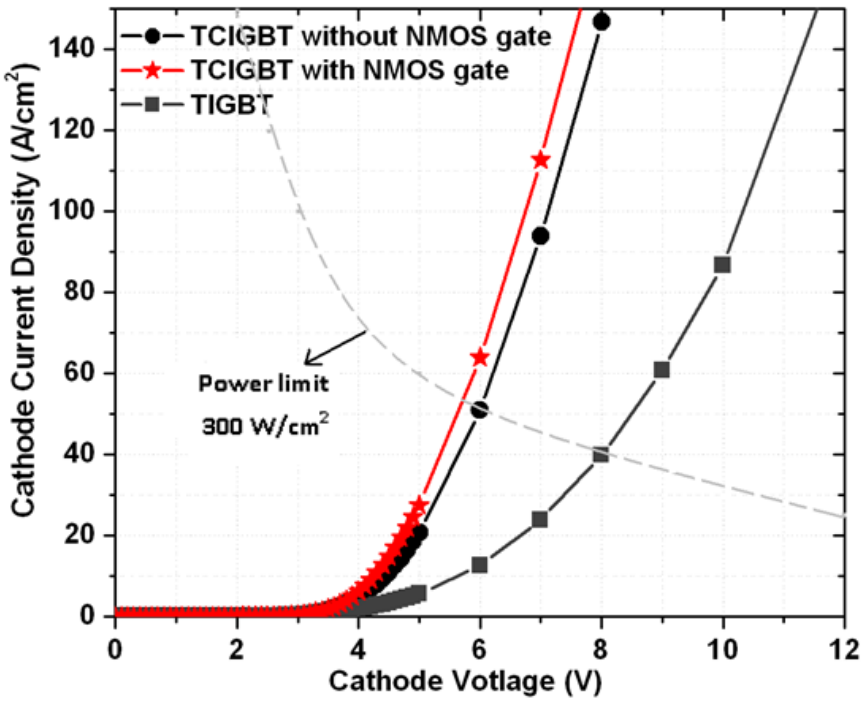


Fig 5.17 Predicted *On-State Characteristics of both TCIGBT and TIGBT devices at Vg = -20V at T in MEDICI™*

Fig 5.18 shows the simulated carrier distribution across the device in the on-state. It can be seen that using the NMOS trench gates, improves the conductivity modulation marginally.

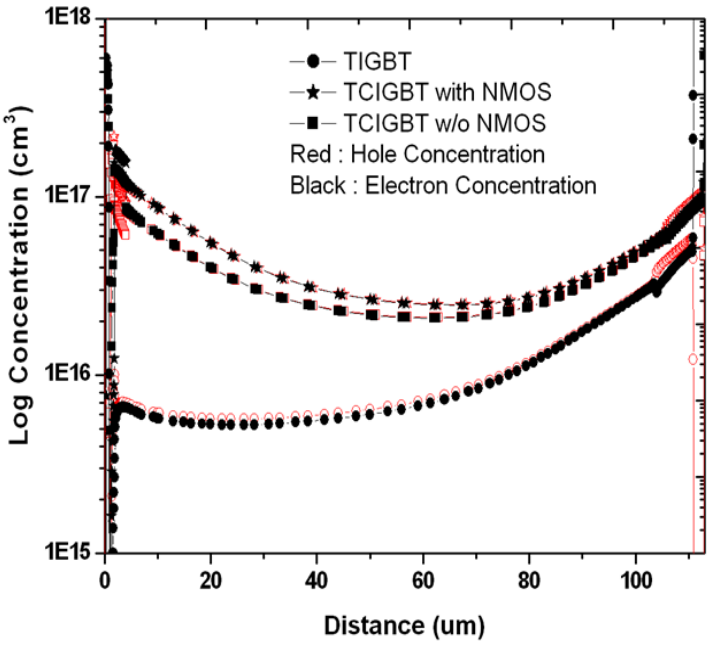


Fig 5.18 Simulated carrier concentrations in the drift regions of TCIGBT and TIGBT devices during conduction state. Cutline AA' shown in Fig 5.7

Fig 5.19 shows the predicted saturation characteristics and FBSOA of all devices. An improvement in the FBSOA is seen by including NMOS Trench gates in a TCIGBT structure, due to the slightly lower self-clamping voltage as in fig 5.13 as compared to the conventional structure (see fig 5.8). Since the PMOS Trench gates are etched deep into the Pwell, there is no significant change in the self-clamping voltage by including an NMOS Trench gate. As explained earlier, self-clamping phenomenon in SiC TCIGBT occur not by punch through of the Pwell region but by the punch through of the Tnmos formed by Pwell and the trench gates. Since Tnmos exists in the device without the NMOS trench gates, the self-clamping in this device also occurs via punch through of this Tnmos. Hence by including NMOS trench gates; the charge within the anode cell is reduced further to decrease the self-

clamping voltage slightly as shown in fig 5.13. This explains the marginal improvement in the SOA in TCIGBT with NMOS trench gates. However it can be seen that TCIGBT a has a larger Safe Operating Area than an TIGBT of the same rating which is desirable for improved short circuit endurance time.

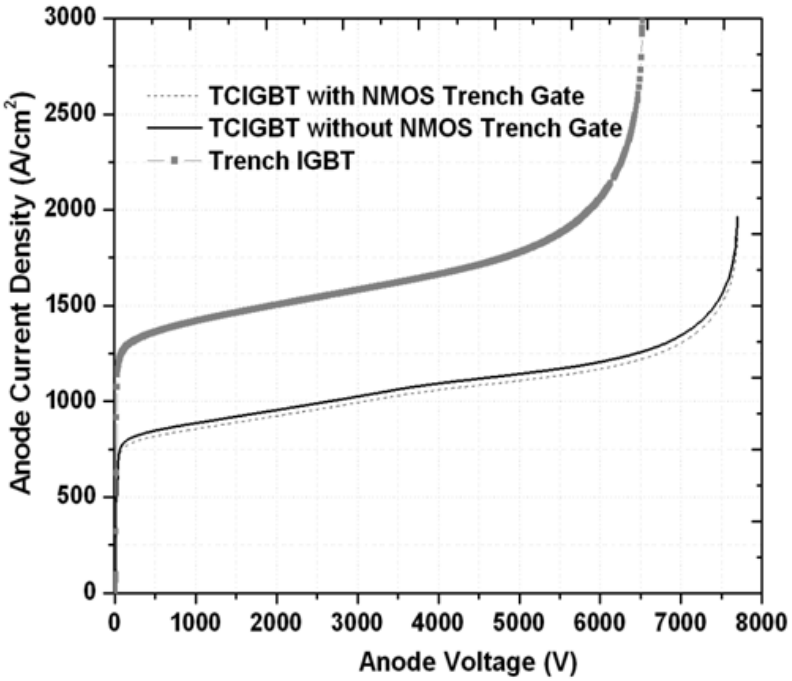


Fig 5.19 Predicted *Saturation characteristics of both TCIGBT and TIGBT devices at Vg = -20V.*

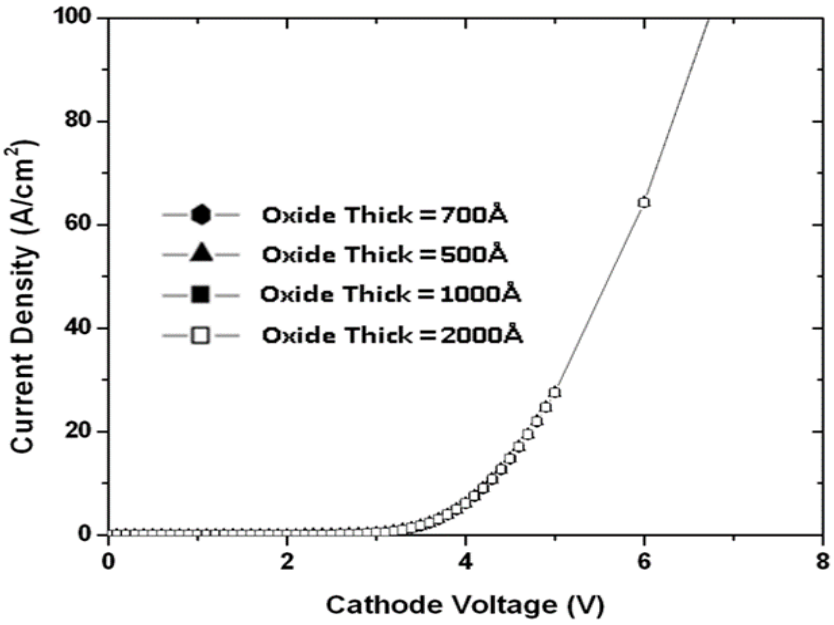


Fig 5.20 The effect of gate oxide thickness (at the bottom of gate 1) on the on-state voltage of TCIGBT.

The oxide thickness below the gate 1 is kept at 700Å to protect it from high electric fields at higher cathode voltages. Furthermore, the corners of the gates can be rounded for additional protection similar to [5]. Moreover, due to the capacitive coupling, increasing the oxide thickness has no effect on on-state as shown in fig 5.20. The Nwell and Pwell doping are important parameters in the CIGBT device design as they are critical in determining the on-state voltage, blocking performance and the current saturation property of the device.

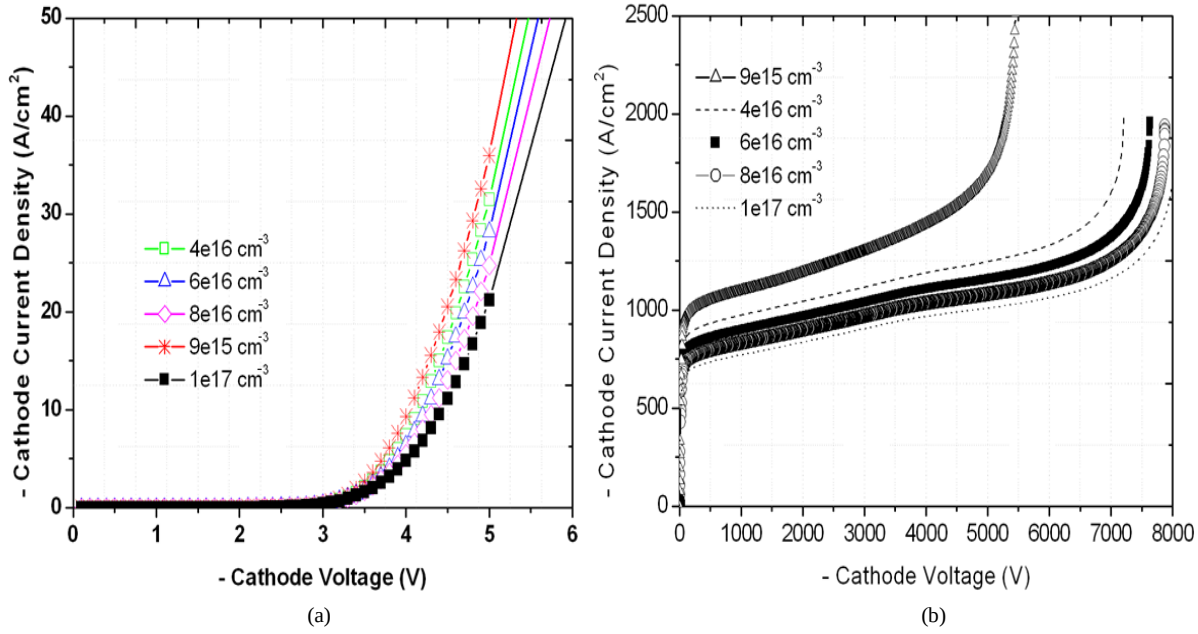


Fig. 5.21 Effect of Nwell Concentration on Vce(sat) of TCIGBT (a) within the power limit of 300W/cm^2 (b) upto cathode voltage = -8kV at T.

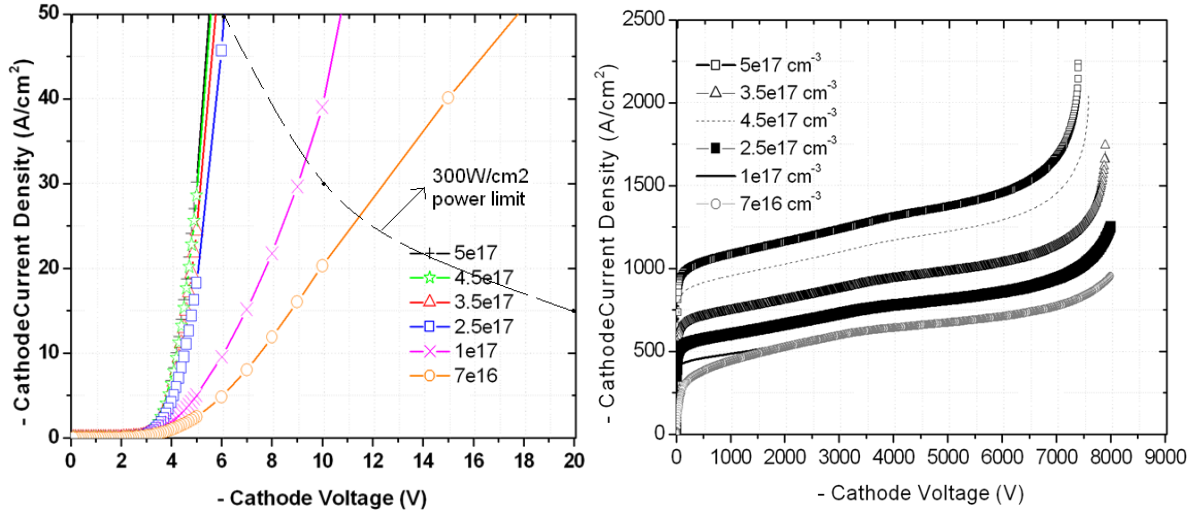


Fig. 5.22 Effect of Pwell Concentration on Vce(sat) of TCIGBT (a) within the power limit of 300W/cm^2 (b) upto cathode voltage = -8kV.

Fig 5.21 (a) and (b) shows the influence of Nwell concentration and fig 5.22 (a) and (b) shows the influence of Pwell concentration on the on-state characteristics of the device. The Pwell dosage controls the self-clamping of the device. It has to be sufficient enough to reduce the self- clamping voltage and saturation current density, and to maintain low on-state voltage. The doping density of this region if too low can lead to very high on-state voltage and if too highly doped then the self-clamping voltage will increase both of which are not desirable.

At full inversion (Vg = -20V) the TCIGBT shows more than 30% improvement in the Vce(sat) at a current density of 50A/cm^2 as shown in Fig 5.17. The differential specific on- resistance of TCIGBT can be calculated from the Fig to be 20 mΩcm^2 which is lower than TIGBT (25 mΩcm^2). The unique feature of self-clamping in TCIGBT leads to lower saturation current density at any given gate voltage as shown in Fig 5.23.

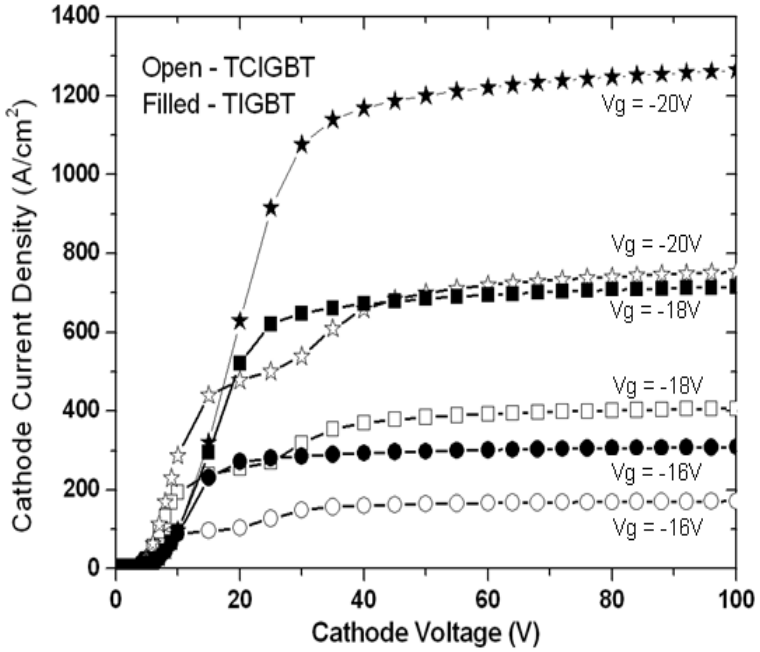


Fig. 5.23 Forward Characteristics of both TCIGBT and TIGBT at different gate voltages.

Fig 5.24 shows that SiC TCIGBT has a positive temperature coefficient on forward voltage similar to TIGBT which is desirable for paralleling operation of devices. This ensures equal current sharing between devices however will increase losses due to higher $V_{ce(sat)}$ at higher temperatures.

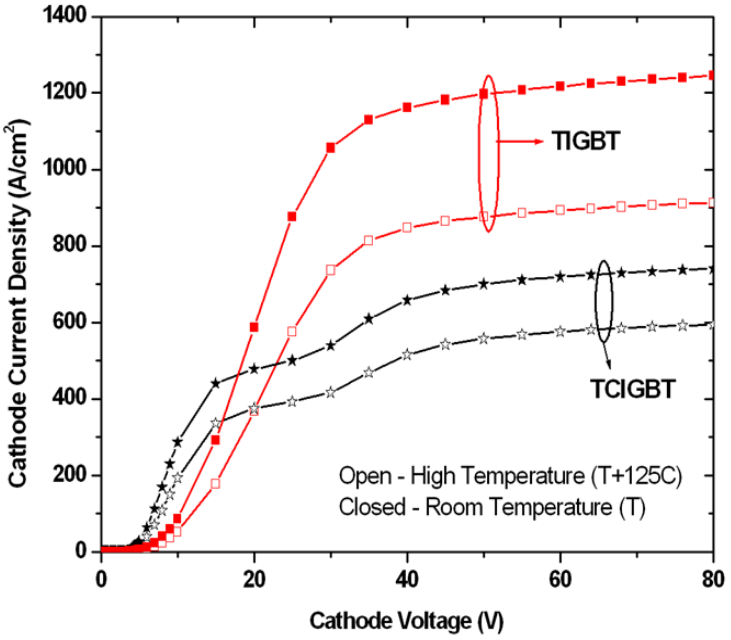


Fig 5.24 Forward characteristics of both TCIGBT and TIGBT devices at different temperatures showing positive temperature coefficients.

5.4.2 Dynamic Characteristics

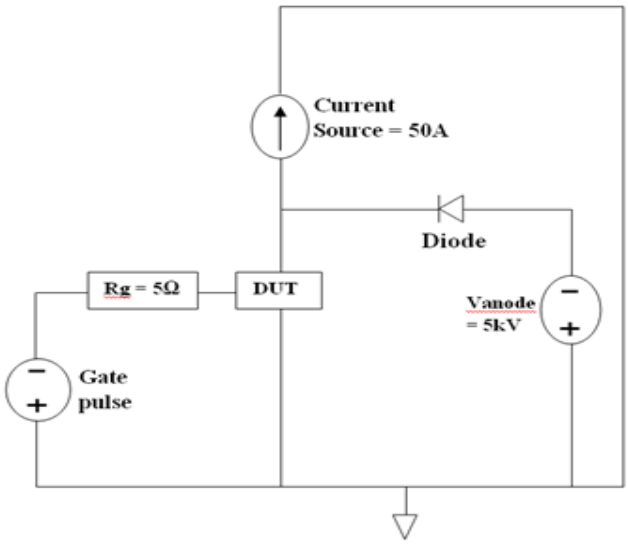


Fig 5.25 Inductive Switching circuit modelled by a current source

The switching performance of all the devices was simulated using a traditional chopper circuit modelled in MEDICI™ by a current source as shown in Fig 5.25[7]. The devices were switched at half their breakdown voltage (= -5kV) at a frequency of 20 kHz with 50% duty cycle assuming a 300W/cm^2 package power limit. For simplicity the device active area is assumed to be 1cm^2. The initial carrier lifetime assumed at 300K is 1µs as mentioned in chapter 3 and [13]. The lifetimes at elevated temperatures are taken into consideration by the experimental fit formula shown in [14]. The simulated Eoff-Vce(sat) trade-off curves are shown in Fig 5.26.

It can be seen that including an NMOS trench gate does not change the trade-off however TCIGBT improves the trade-off when compared to TIGBT as the on-state voltage is significantly reduced. The turn-off mechanism is similar to that in TIGBT and since all gates are connected no special driving sequence is required for the NMOS gate. When a positive voltage is applied at the gates, the NMOS gates will have a conducting channel through inversion of P well providing a path for electrons to flow to the anode thus conducting during the turn-off cycle.

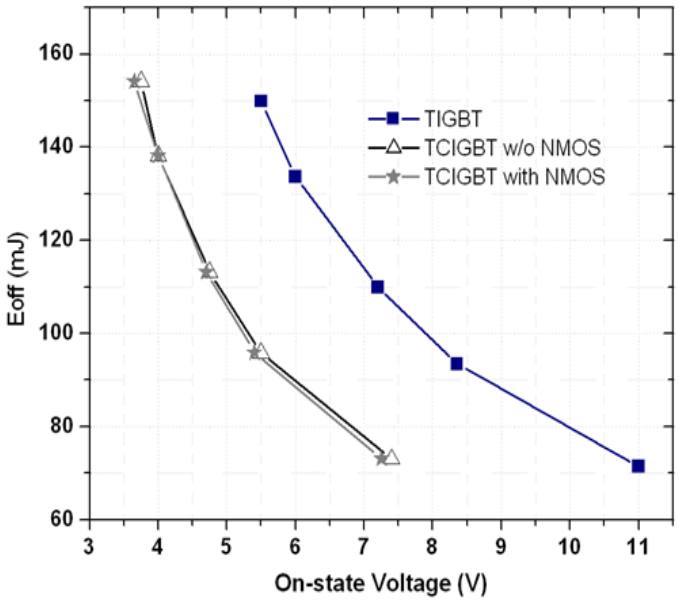


Fig.5.26 Eoff- Vce(sat) Trade-off Curves of the all devices at a current density of 20A/cm^2 (points are calculated at different lifetimes) at T

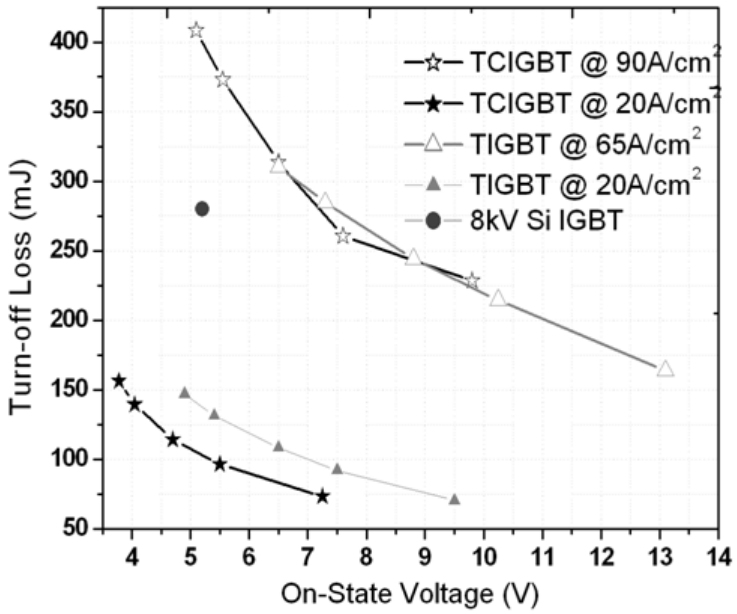


Fig. 5.27 Eoff - Vce(sat) Trade-off Curves for TCIGBT and TIGBT (points are calculated at different lifetimes) at T.

Fig 5.27 shows simulated E_{off}-$V_{ce(sat)}$ tradeoff curves for SiC TCIGBT and TIGBT at different current densities. This graph shows that for a given voltage rating, TCIGBT technology can provide more than 25% lower total losses. The turn-off losses and turn-off times of TIGBT and TCIGBT when switched at a current density of 20A/cm^2 are 109.23mJ/114.2mJ and 0.572µs/0.543µs respectively. The turn-off time in TCIGBT is reduced as self-clamping and the NMOS trench gates aid the removal of excess charges in the drift region [10]. The results also indicate that, at a given package power limit and a carrier lifetime of 1µs, TCIGBT can be operated at higher current densities (90A/cm^2) than an IGBT (65A/cm^2) and still achieve better trade-off performance. The losses of 10 kV SiC TCIGBT are found to be much lower than an 8kV Si IGBT reported in [15].

5.4.3 Short Circuit Characteristics

An electro thermal simulation of the device under short-circuit condition (cathode voltage= -5kV) was also performed on both TCIGBT and TIGBT. Fig 5.28 shows the circuit used for modelling short circuit performance of the device. TCIGBT as

expected supported a much larger short circuit endurance time (20µs) than its IGBT counterpart (10 µs) due to its lower saturation current density which leads to lower heating of the device.

Fig 5.29 shows the simulated short-circuit times of both devices. Longer short circuit endurance times are a prerequisite for medium/high power applications for withstanding transient fault conditions without failure.

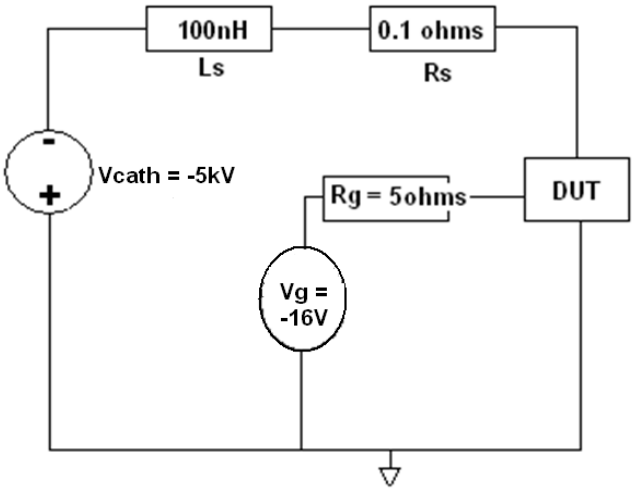


Fig. 5.28 Short Circuit simulation circuit model used for simulation

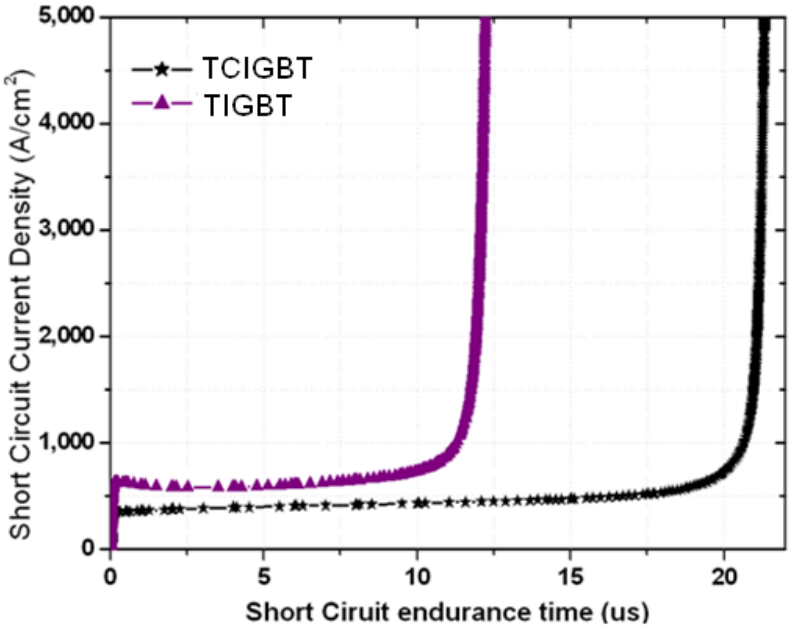


Fig 5.29 Electro thermal Short Circuit simulation of TCIGBT and TIGBT at 5kV rail voltage at T.

CONCLUSION

A detailed study of Trench Clustered Insulated Gate Bipolar Transistor has been discussed in this chapter. Based on the results shown it can be concluded that including NMOS trench gates can improve the on-state performance by about 5% and lower self-clamping voltage without affecting the Eoff- Vce(sat) trade-off. Further, reduction of electron density flowing under the p+ region can potentially improve RBSOA. 10kV SiC TCIGBT can outperform its IGBT counterpart by providing more than 25% lower losses as well as upto two times improvement in short-circuit endurance time. Hence TCIGBT can be considered as a potential candidate for high power applications. The following chapter (Chapter 6) will compare P channel TCIGBT with its N channel equivalent through simulation studies.

Publications

1. K.G.Menon, L.Ngwendson ,E.M.Sankara Narayanan, "Performance Evaluation of 10-kV SiC Trench Clustered IGBT " *Electron Device Letters,* vol. 32, pp. 1272-1274, 15 August 2011.
2. K. G. Menon and E. M. S. Narayanan. Numerical evaluation of 10-kV clustered insulated gate bipolar transistor in 4H-SiC. *IEEE Transactions on Electron Devices, 60*(1), pp.366-373, 2013

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Chapter 6:

Comparison of N Channel and P Channel Trench CIGBT devices in 4H – SiC

The majority of unipolar power devices in Silicon are N-channel due to the higher electron mobility than for holes. However, P channel devices are required for some applications that utilise complementary devices and for battery charger circuits. In spite of the same trend of carrier mobility in SiC, P-channel devices are preferred for fabrication [1]. Although N channel devices benefit from higher electron inversion channel mobility and lower n-type source contact resistance, these require low resistivity P+ type substrates. The reason for this is that due to relatively high ionization energy required in SiC; most impurities are not ionized at high doping levels [1]. The ionization energy of acceptors is larger than donors, and hence N-channel devices using P^+ substrate exhibits larger specific on-resistance than P-channel devices using N^+ substrate.

Due to unavailability of low resistivity P+ substrates, P-channel devices utilising N+ substrates were fabricated initially [2-4]. More recently Cree and few other research groups have been reporting N-channel IGBTs in SiC, however there are still limitations for removal of substrates and formation of the collector regions [5-7]. Despite these drawbacks, the advantage of using N-Channel devices would be faster switching speeds due to the lower current gain of the backside transistor (P+NP), making them preferable to P channel devices for high frequency applications. Table 6.1 shows a comparison of various parameters between N and P-IGBTs in Si and SiC.

Table 6.1: COMPARISON OF IGBTS IN SI AND SIC WITH RESPECT TO VARIOUS PERFORMANCE PARAMETERS [4]

	Vertical Mobility (cm^2/Vs)	***Built-in voltage (V)***	***Substrate type Resistivity (mΩ-cm)***	***Stored charge/Latchup Susceptibility***	***Gate Oxide reliability***	***Inversion layer mobility (cm^2/Vs)***
Si N-IGBT	865	0.7	P type 0.01	Higher/Low	Best	350-400
4H-SiC N-IGBT	550	3.0	P type 1-10	Higher/Medium	Poor	1-5
4H-SiC P-IGBT	550	3.0	N type 0.01 – 0.02	Lower/High	Good	0.5-2
6H-SiC N-IGBT	40	2.6	P type 1-5	Higher/Low	Good	25-100
6H-SiC P-IGBT	40	2.6	N type 0.05-1	Low/High	Better	5-25

In previous chapters, P-channel Clustered Insulated Gate Bipolar Transistor (CIGBT) has been discussed in detail. This chapter will compare an N-channel Trench CIGBT (TCIGBT) with the P-channel equivalent in terms of both the on-state and transient performance.

6.1 N - CHANNEL TCIGBT DEVICE STRUCTURE AND OPERATION

The half-cell structure of an N channel TCIGBT along with its equivalent circuit is shown in Fig 6.1. Table 6.2 shows the proposed general process for N channel SiC TCIGBT; this is same as a P channel device but starting with N+ substrate. The structure of P channel device with the equivalent structure is shown in Fig 6.2 for clarity.

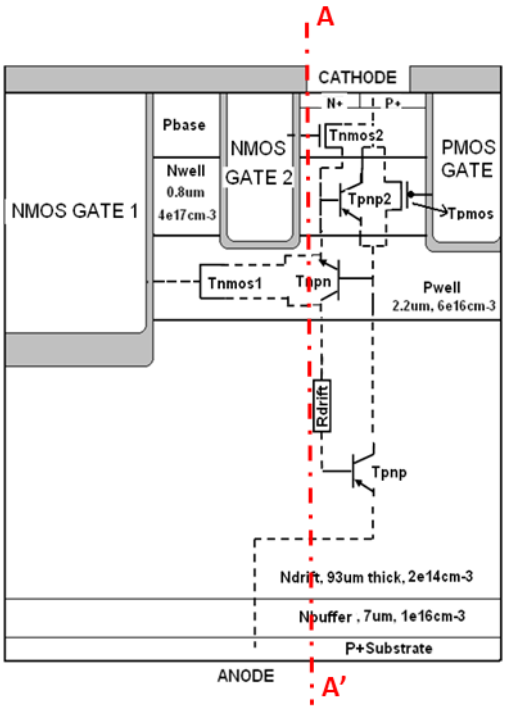


Fig.6.1: Half cell structure of 10kV 4H-SiC N-channel TCIGBT with its equivalent circuit

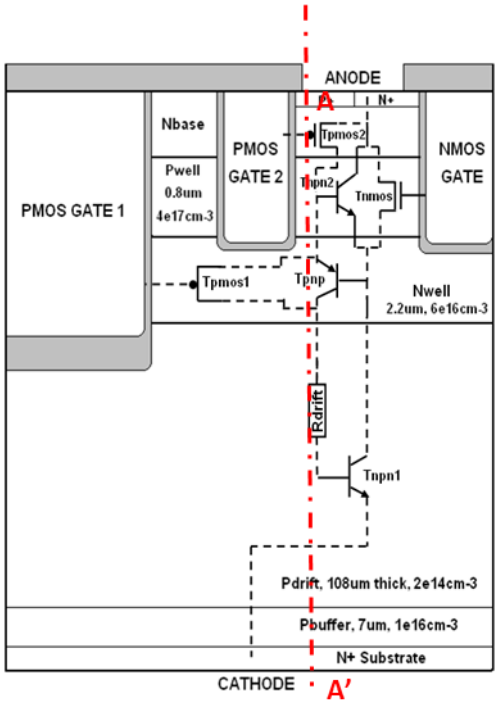


Fig. 6.2: Half cell structure of 10kV 4H-SiC P-channel TCIGBT with its equivalent circuit

For fair comparison of the devices, simulations were performed using the same number of channels, channel length (0.5µm) and gate oxide thicknesses (500Å) [2].

Table 6.2: Proposed general process features for N channel SiC TCIGBT

P+, 1e20cm^{-3}
N buffer, N Drift, P well and N well are grown by epitaxy on the N+ substrate.
P base can be formed by epitaxy or by ion-implantation and annealed at high temperatures.
Trench gate regions are etched.
N+ and P+ selectively implanted and annealed at high temperatures.
Gate oxides and P-type polysilicon layers are grown
All contacts metallised.

The physics of operation of the device is similar to the P channel TCIGBT as described in section 6.3 with inverted regions. Similar to the P channel device, the self-clamping phenomenon takes place through the punch-through of the channel of the PMOS region formed by the gates with the N well region when the gate voltage is applied i.e. when the potential in the region increases to the self-clamping voltage.

6.2 SIMULATED PERFORMANCE CHARACTERISTICS

The following sections will discuss the comparison of performance of N-channel and P-channel TCIGBT in 4H-SiC. The results were obtained through simulation using MEDICI™ and uses models mentioned in chapter 3.

6.2.1 Static Characteristics

For the same carrier lifetimes and forward blocking voltages, P-channel TCIGBT has a thicker drift region than an N-channel device (108µm – P channel and 90µm – N channel). This is because, the forward breakdown in a Field Stop CIGBT is determined by the open-base breakdown voltage of the transistor formed by

N^+cathode/P drift/N well in a P channel device and P^+ anode/N drift/P well in an N channel device. The current gain of an NPN transistor is higher than the PNP transistor hence the P-channel device is prone to breakdown at a lower voltage thereby requiring a thicker drift region to support the same voltage than an N-channel device. The predicted breakdown characteristics of both devices are shown in Fig 6.3.

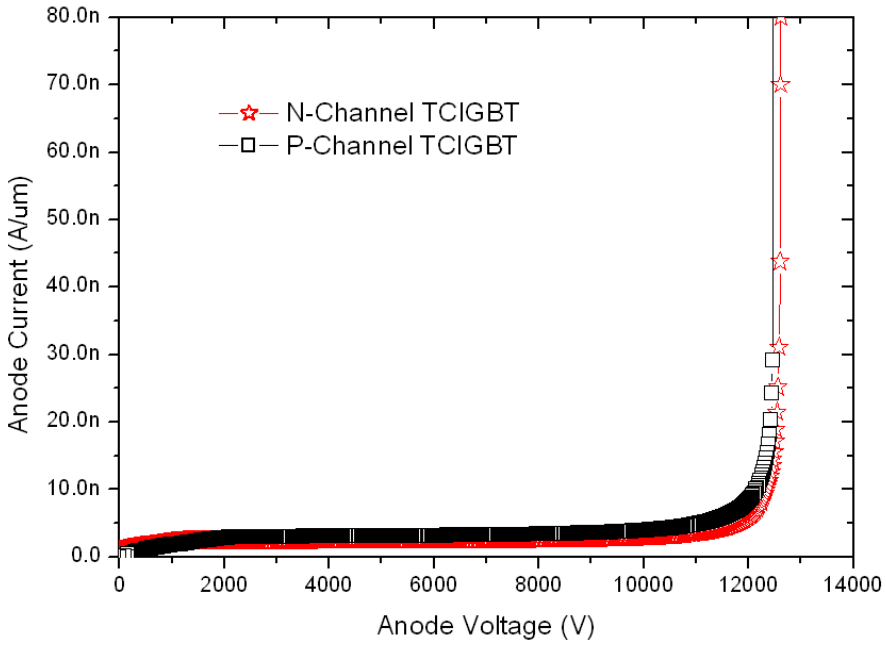


Fig 6.3: Predicted breakdown voltages of N channel and P channel with drift lengths of 93µm and 108µm respectively

The thinner drift region together with higher electron mobility in the material will help reducing the on-state losses of the N channel device as shown in Fig 6.4. The self-clamping voltage of both N-channel and P-channel devices is around 26V. Fig 6.5 shows the saturation characteristics of both the devices. Due to the lower current gain of the backside P+NP transistor in an N-channel device, the saturation current density is much lower (more than 30%) than the P channel device. This can be beneficial in terms of short circuit characteristics of the device since it can accommodate more dissipation within the device. However, due to higher hole

ionization coefficient than that of electrons in SiC, P channel devices perform better under short circuit conditions as discussed in section 6.2.3.

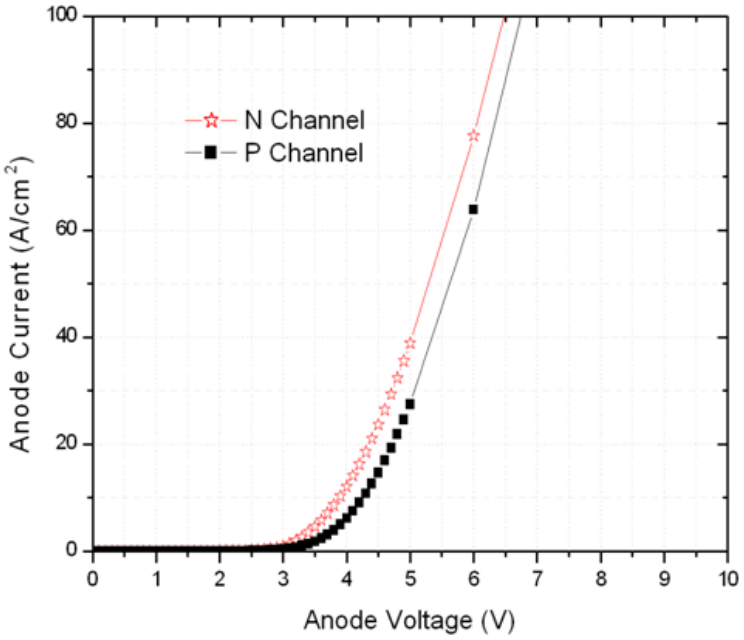


Fig. 6.4: Forward characteristics of both N-channel and P-channel SiC TCIGBT at Vg= +/- 20V

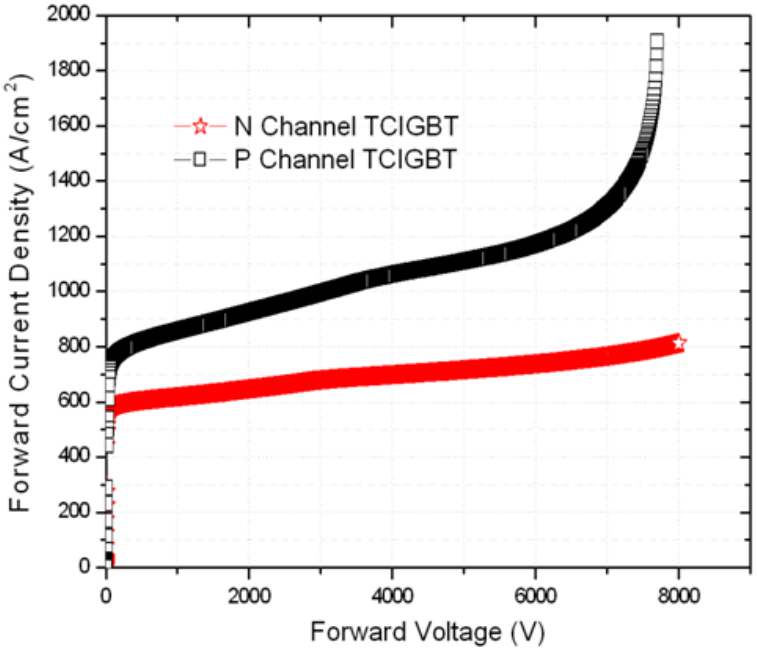


Fig. 6.5: Saturation characteristics of N-channel and P-channel TCIGBT at Vg= +/-20V.

6.2.2 Switching Characteristics

The switching performance of both the devices was simulated using a traditional chopper circuit modelled in MEDICI™ by a current source as shown in Fig 5.25[8].

The devices were switched at half their breakdown voltage (= -5kV) at a frequency of 20kHz with 50% duty cycle assuming a 300W/cm^2 package power limit. For simplicity the device active area is assumed to be 1cm^2. The initial carrier lifetime assumed at 300K is 1µs as mentioned in chapter 3 and [9]. The lifetimes at elevated temperatures are taken into consideration by the experimental fit formula shown in [10]. The simulated Eoff-Vce(sat) trade-off curves are shown in Fig 6.6.

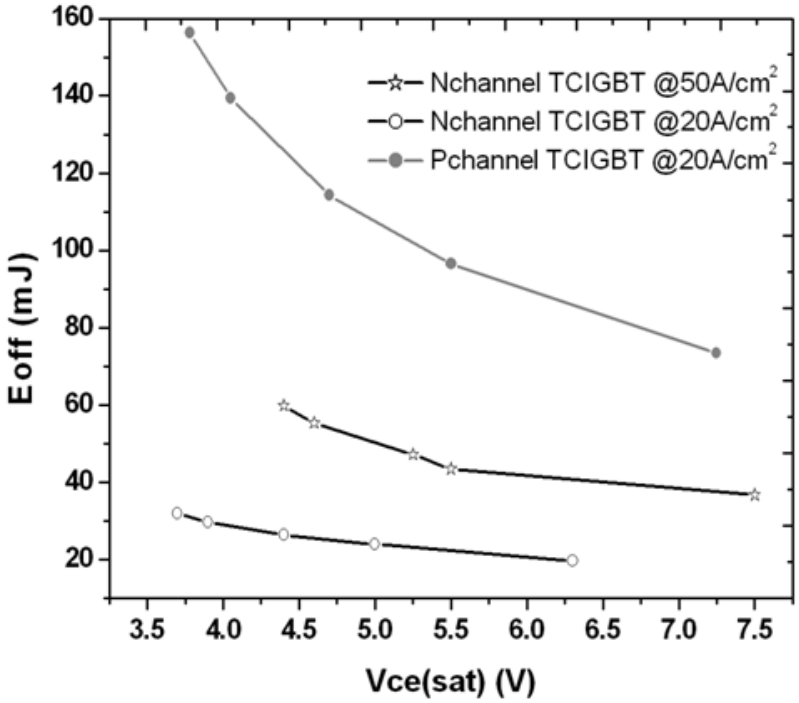


Fig. 6.6: Eoff-Vce(sat) Trade-off Curves of N-channel and P-channel TCIGBT at Vg= +/-20V.

It can be clearly seen than N channel devices can switch much faster than P channel counterparts leading to more than 60% reduction in switching losses. This can be explained as follows:

When the gate voltage drops below the threshold voltage of the devices, the channel current is cut-off leading to the turn-off of the device. The channel current forms a significant part of the on-state current in the N channel CIGBT. Fig 6.7 shows the current flow in the N channel CIGBT during on-state, it can be clearly seen that

channel current (current flowing through the MOS channel) is quite dense. On the contrary, in P channel devices the on-state current is mainly contributed by drift current. In P channel CIGBT, the on-state current comprising of holes is less than the electron current in the N well/ P drift region (as shown in Fig 6.9). This increases the turn-off time and turn-off losses of a P channel device. In addition to this, as mentioned in section 6.2.1, for the same breakdown voltage, the P channel CIGBT drift region is wider than the N channel CIGBT. Thus in general, N channel devices are faster and have lower switch-off losses as compared to P channel devices.

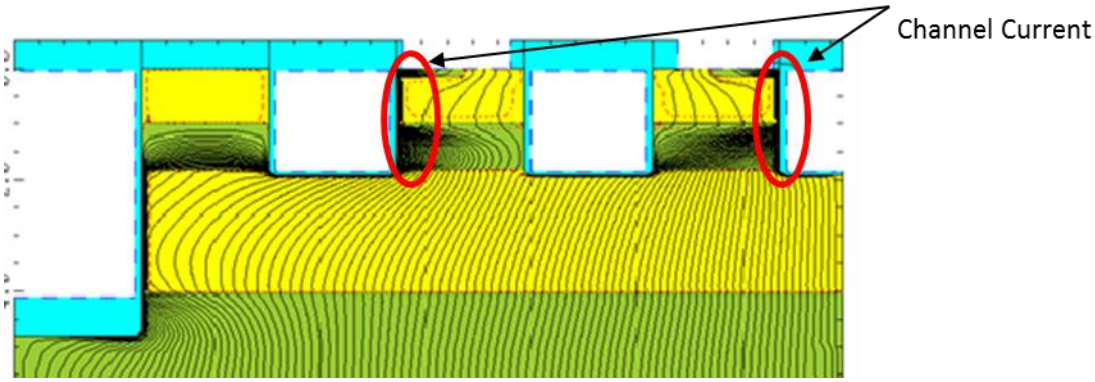


Fig 6.7 N channel device current flow during conduction

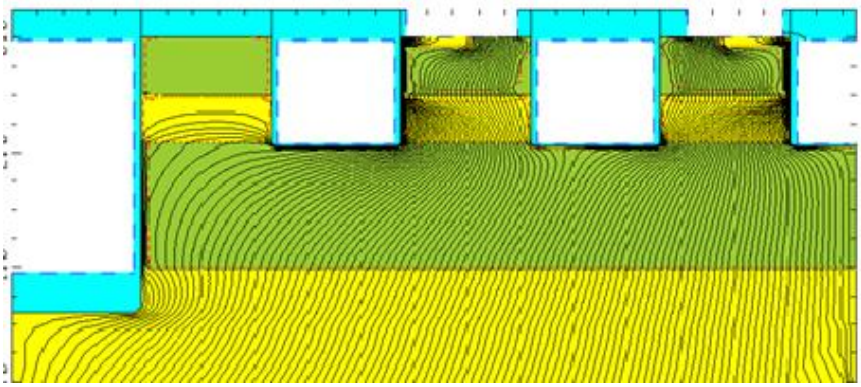
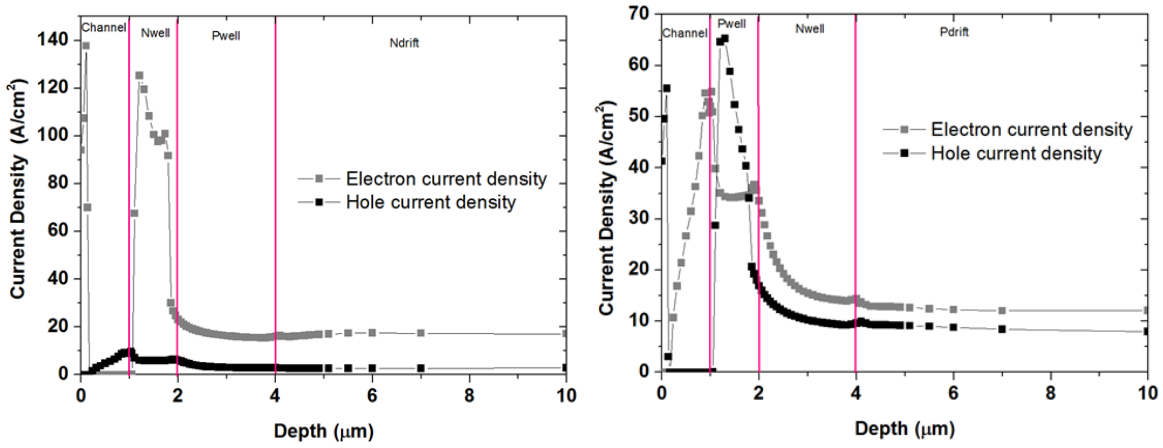


Fig 6.8 P channel device current flow during conduction



(A)

(B)

Fig 6.9 Electron and hole current densities in (A) N channel and (B) P channel CIGBT devices across the channels during conduction. Cutline AA' as shown in Fig.6.1 and Fig.6.2.

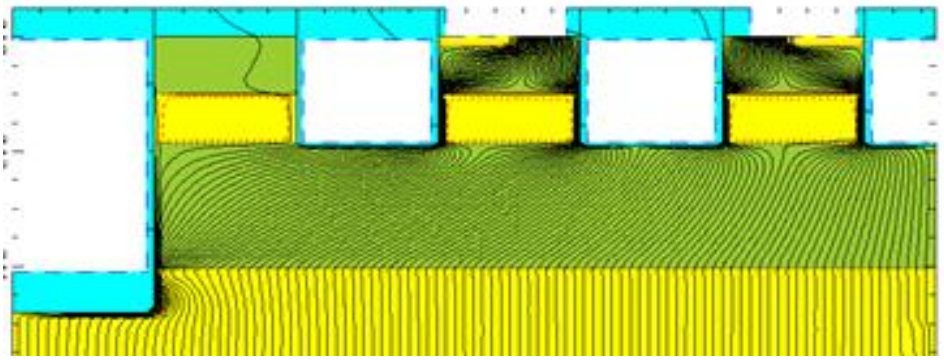


Fig 6.10 P channel device current flow during turn-off

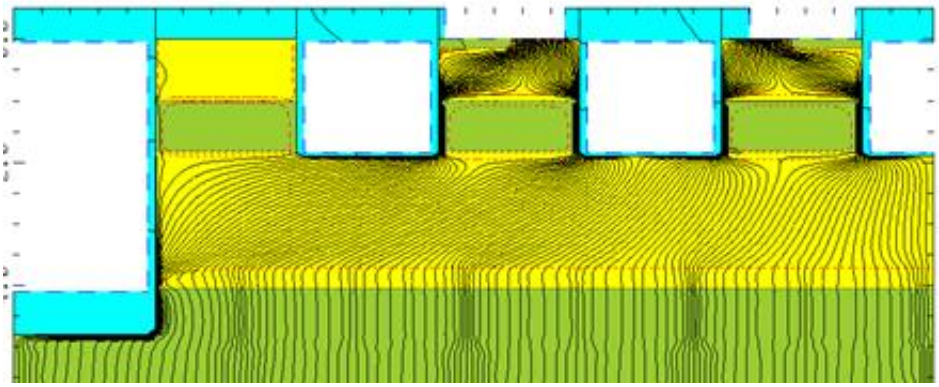


Fig 6.11 N channel device current flow during turn-off

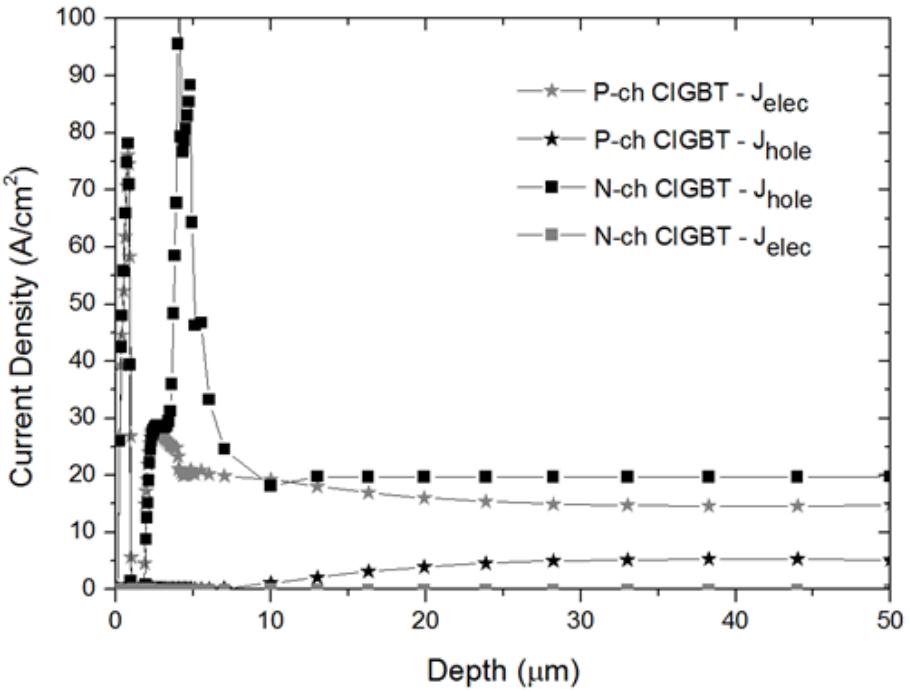


Fig 6.12 Electron and hole current densities in N channel and P channel CIGBT device during turn-off. Cutline AA' as shown in Fig 6.1 and Fig 6.2

Fig 6.10 and 6.11 shows the current flow in TCIGBT and Fig 6.12 shows the hole and electron current distribution in the device during turn-off.

6.2.3 Short-circuit Characteristics

The short-circuit endurance time of p-channel device can be seen to be longer and much smoother than the n-channel device which latches-up prematurely due to avalanche breakdown from Fig 6.13. In Si, the Short Circuit Safe Operating Area (SCSOA) of P-channel IGBT device has been found to be worse than the n-channel devices [11]. This is due to significantly higher avalanche multiplication due to larger ionisation coefficients of electrons moving through the space charge layer [11]. However, in SiC the ionisation coefficient of holes is higher than that for electrons [12] (see Appendix A) and this explains the higher over current in and N channel device. The hole and electron carrier distributions in both devices during short circuit are shown in Fig 6.14.The minority carriers in an N channel SiC CIGBT being holes

and due to their higher impact ionisation in the material as opposed to Si, N channel device has a reduced short circuit tolerance as compared to P channel device.

A noticeable feature in the N channel device short-circuit characteristics is the negative slope of current (figure 6.13). This is primarily due to the drastic reduction in carrier mobility with temperature [13]which is due to the multiplication of carriers in the drift region for the reasons explained above and the fact that N channel CIGBT carrier density is much higher than the P channel CIGBT. Hence we can conclude that the N channel device short circuit performance is poorer compared to a P channel device due to all above stated reasons.

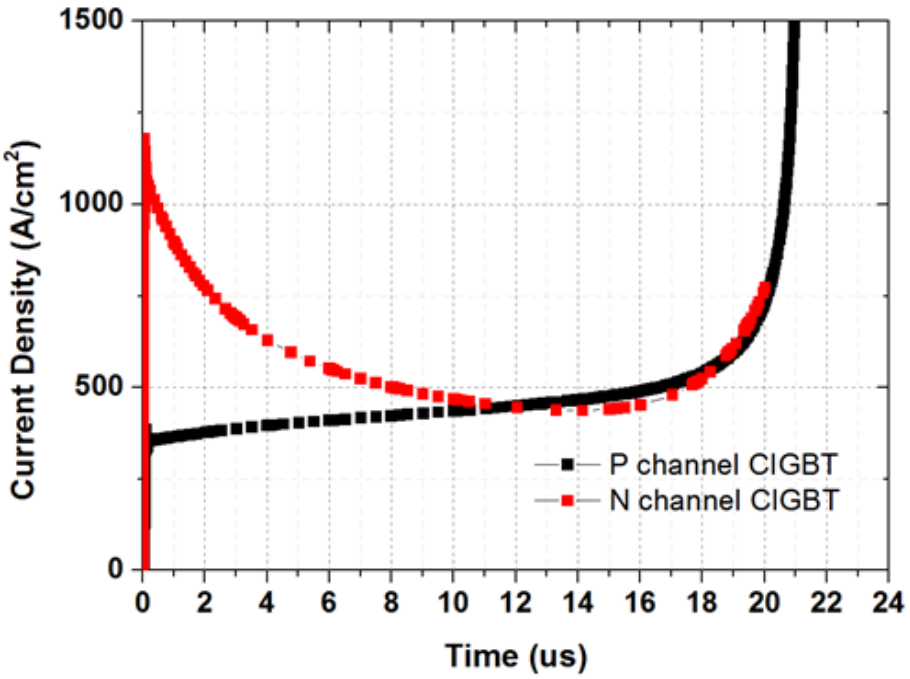
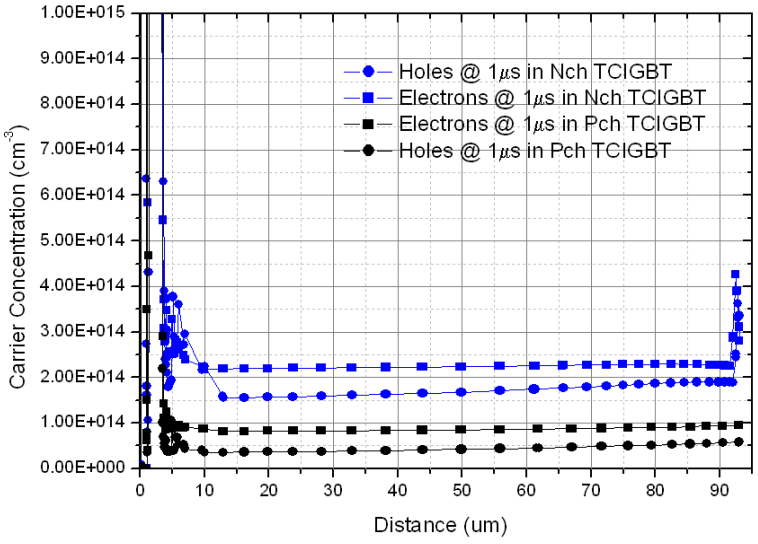
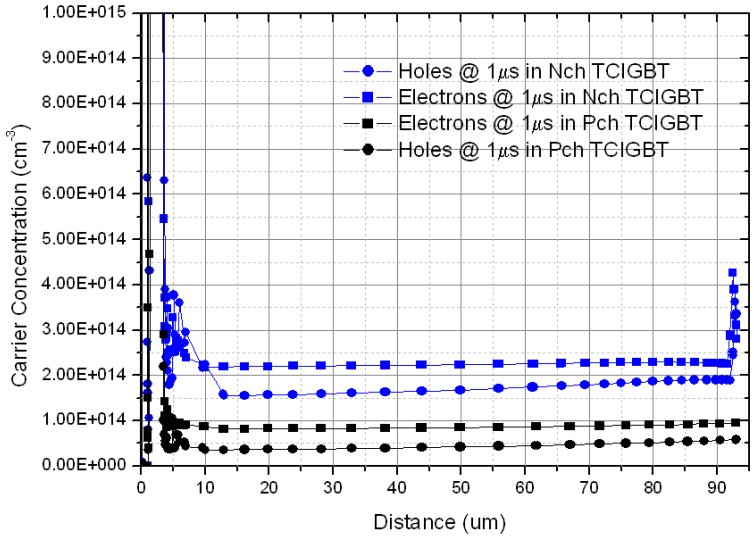


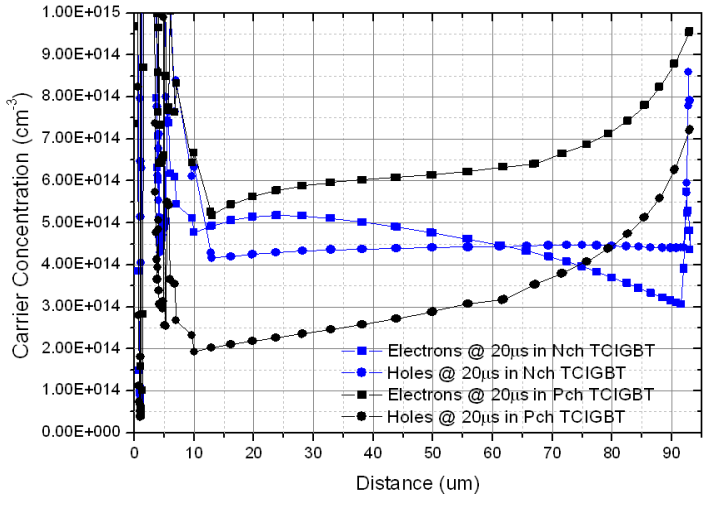
Fig. 6.13: Predicted Short Circuit characteristics of Pchannel and Nchannel CIGBT devices at rail voltage of 5kV using electro-thermal simulations



(a)



(b)



(c)

Fig. 6.14:Electron and Hole carrier distribution in P channel and N channel CIGBT devices at (a) 1μs short circuit time (b) 6μs short circuit time and (c) 10μs short circuit time

CONCLUSION

In this chapter the performances of N channel and P channel TCIGBT was compared for various parameters. Table below summarises the findings in a 10kV 4H SiC TCIGBT through simulations.

Table 6.3: Summary of P channel and N channel TCIGBT devices.

Parameter	*N channel TCIGBT*	*P Channel TCIGBT*
Breakdown Voltage	*Thinner drift length required to support higher BV (90µm for 10kV)*	*Thicker drift length required to support higher BV (108µm for 10kV)*
On-state voltage	*Slightly lower due to thinner drift length (~5%)*	*Slightly higher due to thicker drift length*
Saturation current density	*Higher (~ 40%)*	*Lower*
Turnoff losses	*Lower (~ 60%)*	*Higher*
Short circuit performance	*Poor compared to P channel*	*Good*

Recently a study by Cree reported the comparison between N channel and P channel IGBT devices in SiC [6] for inverter application. The results from the study is follows the same trend in terms of losses in the N channel device.

The results obtained in this chapter suggests that N channel CIGBT have potentially better overall performance due to lower losses than can benefit in terms of efficiency in a power converter application.

Publications

"Comparison of 10kV N-channel and P-channel Trench Clustered Insulated Gate Bipolar Transistor (TCIGBT)" presented at ISPS conference 2012, Prague, Czech Republic.

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Chapter 7:

Conclusions and Further Study

In this work, high voltage SiC based devices have been discussed. SiC Clustered Insulated Gate Bipolar Transistor (CIGBT) device performance was studied through simulations for the first time for high voltage (>10kV) applications. Device design using both planar and trench gate technologies were discussed in great detail. Novel concept of using SiC CIGBT for reducing the losses and improving short circuit performance were evaluated through modelling and simulations in MEDICI™.

The theoretical limit of Si CIGBT was discussed in detail for the first time and compared it to that of IGBT predicted earlier. Further, SJ CIGBT was simulated to understand the ultimate limit of Si CIGBT. Establishing these limits of CIGBT showed that at higher voltages (above 3kV) considerable increase in R_{on} of the device will occur and thicker Si will be required to support these voltages. SiC being a wide band gap technology was studied for CIGBT at higher voltages in order to assimilate the advantages of the material to reduce the drift lengths at these voltages. The simulated results predicted that at higher voltages (>6kV) SiC TCIGBT shows a much better performance than the limits set by Si IGBT and CIGBT technologies. Considering this predicted performance, 10kV SiC TCIGBT was chosen for further study of device parameters and physics. Comparison of performances of planar IGBT and CIGBT devices in 4H-SiC was discussed chapter 4. The simulation study showed that due to controlled thyristor conduction the CIGBT technology can provide up to 40% improvement in Eoff-Vce(sat) trade-off as compared to IGBT. Lower saturation current density in CIGBT also leads to an enhanced short-circuit performance. However, due to the complexity involved to realise the planar structure

of CIGBT in SiC material, a trench version may be considered a better option. This was discussed in detail in chapter 5 along with general fabrication process for the device as well. Based on the results shown it can be concluded that including NMOS trench gates can improve the on-state performance by about 5% and lower self-clamping voltage without affecting the Eoff- Vce(sat) trade-off. Further, reduction of electron density flowing under the p+ region can potentially improve RBSOA. 10kV SiC TCIGBT can outperform its IGBT counterpart by providing more than 25% lower losses as well as upto two times improvement in short-circuit endurance time. Further on, the performances of N channel and P channel TCIGBT devices were compared for various parameters as shown in table 6.3.

FUTURE WORK

In this study a detailed simulation investigation of the physics and design of SiC CIGBT has been conducted. The results showed better performance of CIGBT when compared to IGBT in terms of on-state voltage, Eoff-Vce(sat) trade-off and short circuit performance. However these results need to validated by characterising these devices experimentally hence fabrication of these devices is suggested by the author as the next step. The device performance needs to be evaluated for applications such as HVDC systems.

4H SiC CIGBT have a potential to be operated at higher current densities than MOSFETs/ IGBTs in high voltage switching applications. The CIGBT must be designed carefully since N well, P well and P buffer parameters can affect the performance of the device. It is the hope of the author that the simulation data presented in this thesis (fig 3.17) will suggest further development of lifetime of carriers in SiC. It is also hoped that these devices be fabricated and the switches will

find use in high power switching applications. SiC having higher thermal conductivity inherent to the material can perform well at high temperatures but engineers should be able to develop packages that will not limit the power density of such high performing technologies. The cost of SiC wafers is also several times higher than Si wafers and advances in SiC crystal growth must be made in order to make large area wafers with low defect densities. This will in turn have an impact on cost of devices.

Cost-effective integration of available/novel technologies to improve the efficiency of a converter for any given application is of high concern depending on the operating environment and power capabilities. Having studied 4H SiC based devices much in detail it can be concluded that this technology alone will not improve the performance of power converter systems but other technologies and materials will need to be considered while designing. Si-based solutions are currently in the market and intense research is being carried out to improve the efficiency of these converters as well. Heterogeneous integration will be an important aspect in power systems in order to improve their performance/efficiency depending on the application. The author suggests that to carry forward this work first the SiC CIGBT device discussed in this thesis is fabricated to validate the performance of the device. The design of a power converter based on this technology can then be designed along with gate drivers, thermal management, packaging and filters for a chosen application such as HVDC or marine. Considerable thought has to be given in choosing the right technology in order to benefit most in terms of efficiency of the system as a whole.

APPENDIX A :

DEVICE PARAMETERS AND MODELS

1. SiC IGBT :

Table A.1 IGBT device parameters – Planar and Trench structures

Parameter	*Planar*	*Trench*
N+ Cathode	*1e20cm^{-3}, 0.2 µm thick*	*1e20cm^{-3}, 0.2 µm thick*
P Buffer	*1e16cm^{-3},7µm thick*	*1e16cm^{-3},7µm thick*
P Drift	*2e14cm^{-3}, 108µm thick*	*2e14cm^{-3}, 105µm thick*
P CSL	*8e15cm^{-3}, 1.3µm thick*	*8e15cm^{-3}, 1µm thick*
N Base	*6.5e17cm^{-3}, 1µm deep*	*6.2e17cm-3, 1µm deep*
Gate Oxide thickness	*500Å*	*500Å*
Threshold	*-11V*	*-11V*
BV	*12kV*	*>10kV*
Channel Length	*0.5µm*	*0.5µm*
Carrier Lifetime	*1µsec*	*1µsec*

2. SiC CIGBT :

Table A.2 CIGBT P channel device parameters – Planar structures

Parameter	*Planar*	*Planar with NMOS Trench Gate*
N+ Cathode	*1e20cm^{-3}, 0.2 µm thick*	*1e20cm^{-3}, 0.2 µm thick*
P Buffer	*1e16cm^{-3},7µm thick*	*1e16cm^{-3},7µm thick*
P Drift	*2e14cm^{-3}, 102µm thick*	*2e14cm^{-3}, 102µm thick*
N Well	*1.2e17cm^{-3}, 4µm thick*	*1.1e17cm^{-3}, 4µm thick*
P Well	*5.6e17cm^{-3}, 2.5µm thick*	*5.7e17cm^{-3}, 1.8µm thick*
N Base	*9e17cm^{-3}, 1µm deep*	*8.9e17cm-3, 1µm deep*
Gate Oxide thickness	*500Å*	*500Å*
Threshold	*-11V*	*-11V*
BV	*12kV*	*12kV*
Channel Length	*0.5µm*	*0.5µm*
Carrier Lifetime	*1µsec*	*1µsec*

Table A.3 CIGBT P channel device parameters – Trench structure

Parameter	Trench CIGBT
N+ Cathode	1e20cm^{-3}, 0.2 µm thick
P Buffer	1e16cm^{-3},7µm thick
P Drift	2e14cm^{-3}, 102µm thick
N Well	6e16cm^{-3}, 4µm thick
P Well	4e17cm^{-3}, 1.8µm thick
N Base	8.9e17cm^{-3}, 1µm deep
Gate Oxide thickness	500Å
Threshold	-12V
BV	>10kV
Channel Length	0.5µm
Carrier Lifetime	1µsec

Table A.3 CIGBT N channel device parameters – Trench structure

Parameter	Trench CIGBT
P+ Cathode	1e20cm^{-3}, 0.2 µm thick
N Buffer	1e16cm^{-3},7µm thick
N Drift	2e14cm^{-3}, 89µm thick
P Well	6e16cm^{-3}, 4µm thick
N Well	4e17cm^{-3}, 1.8µm thick
P Base	8.9e17cm^{-3}, 1µm deep
Gate Oxide thickness	500Å
Threshold	12V
BV	>10kV
Channel Length	0.5µm
Carrier Lifetime	1µsec

TABLE A.4 MATERIAL PROPERTIES AND MODELS USED FOR SIMULATIONS[102]

PROPERTIES	***MODELS/VALUES***
Bandgap energy, electron and hole bulk mobility, Incomplete Ionization of impurities models are same as specified in [1].	
Channel mobility model used is PRPMOB and Extracted value of channel mobility is 15-20cm^2/Vs.	
4H SiC Critical field – default value in MEDICI™	
Temperature	*700 K*
Electron mobility (cm^2/Vs)	*950*
Hole Mobility (cm^2/Vs)	*124*
Initial Carrier Lifetime assumed	*1μs @ 300K*
CONSRH (concentration and temperature dependant) and Auger Recombination models are specified in [101].	

References:

[1] K.G.Menon, A.Nakajima, L.Ngwendson, and E. M. S. Narayanan, "Performance Evaluation of 10-kV SiC Trench Clustered IGBT " *Electron Device Letters,* vol. 32, pp. 1272-1274, 15 August 2011 2011.

[2] T. Tamaki, G. G. Walden, Y. Sui, and J. A. Cooper, "Optimization of ON-state and switching performances for 15-20-kV 4H-SiC IGBTs," *IEEE Transactions on Electron Devices,* vol. 55, pp. 1920-1927, 2008.

[3] J. Wang and B. W. Williams, "A simulation study of high voltage 4H-SiC IGBTs," *Semiconductor Science and Technology,* vol. 13, pp. 806-815, 1998.

APPENDIX B :

SIMULATION CODES IN MEDICI™

3. CIGBT structure generation

```
assign name=thick n.val=113
assign name=xmax n.val=6.5
assign name=tr1 n.val=1
assign name=tr2 n.val=1
assign name=plen n.val=0.5
assign name=nlen n.val=0.5
assign name=nbdepth n.val=1
assign name=pwdepth n.val=1.8
assign name=nwdepth n.val=4
assign name=nbase n.val=8.9e17
assign name=pwell n.val=4.2e17
assign name=nwell n.val=6.4e16
assign name=pdrift n.val=2e14
assign name=pbuffer n.val=1e16
assign name=nanode n.val=1e20
assign name=nplus n.val=1e20
assign name=pplus n.val=1e19

$$$Meshing

mesh  adjust smooth.k=2.0 ^diag.fli

x.mesh    x.min=0          x.max=1.0          h1=0.05   h2=0.05
x.mesh    x.min=2.0        x.max=3.0          h1=0.05   h2=0.05
x.mesh    x.min=3.0        x.max=4.0          h1=0.05 h2=0.05
x.mesh    x.min=4.0        x.max=5.0          h1=0.05  h2=0.05
x.mesh    x.min=5.0        x.max=6.0                h1=0.05  h2=0.05
x.mesh    x.min=6.0        x.max=6.5          h1=0.05  h2=0.05

y.mesh   loc=-0.5     spac=0.1
y.mesh   loc=-0.2      spac=0.05
y.mesh   loc=-0.1      spac=0.05
y.mesh   loc=0         spac=0.05
y.mesh   loc=0.5       spac=0.1
y.mesh   loc=1        spac=0.05
y.mesh   loc=1.2      spac=0.1
y.mesh   loc=1.9       spac=0.05
y.mesh   loc=3.2       spac=0.1
y.mesh   loc=4.0       spac=0.1
y.mesh   loc=4.8        spac=0.1
y.mesh   loc=6         spac=0.5
```

```
y.mesh   loc=10         spac=3
y.mesh   loc=50         spac=6
y.mesh   loc=@thick-25   spac=2.5
y.mesh   loc=@thick-15.5  spac=2
y.mesh   loc=@thick-8  spac=0.5
y.mesh   loc=@thick      spac=0.2

eliminate columns y.min=4.9
eliminate columns y.min=5.0
eliminate columns y.min=6.0
eliminate columns y.min=6.5
eliminate columns y.min=10


$$$$$ Defining regions

region num=1 Oxide x.min=0    x.max=@xmax   y.max=0

region num=2 SiC   x.min=0   x.max=@xmax   y.min=0   y.max=@thick

region num=3 Oxide x.min=0    x.max=@tr1   y.max=4.8

region num=5 Oxide x.min=2    x.max=2+@tr2   y.max=1.9

region num=6 Oxide x.min=4    x.max=4+@tr2   y.max=1.9

region num=7 Oxide x.min=6    x.max=@xmax    y.max=1.9


$$$$ Electrodes

elec name=Cathode x.min=3.05   x.max=3.9  y.min=-0.5  y.max=0  void
elec name=Cathode x.min=5.2  x.max=5.95 y.min=-0.5 y.max=0 void

$$$trench 1
elec name=Gate  x.min=0  x.max=@tr1-0.05   y.min=0.05  y.max=4.1  void


$$$turn on gate1
elec name=Gate  x.min=2.05  x.max=2.95    y.min=0.05  y.max=1.85  void

$$$turn off gate
elec name=Gate  x.min=4.05 x.max=4.95  y.min=0.05  y.max=1.85   void

$$$turn on gate2
elec name=Gate  x.min=6.05 x.max=@xmax  y.min=0.05  y.max=1.85   void
```

```
elec name=anode  bottom


$$$DOPING REGIONS

$$$$$ doping drift region
doping unif conc=@pdrift p.type y.max=@thick  reg=2


$$$$doping anode region
doping  conc=@nanode  n.type reg=2  x.min=0 x.max=@xmax   junc=@thick-0.2
peak=@thick

$$$$doping buffer region
doping unif  conc=@pbuffer p.type  reg=2  x.min=0  x.max=@xmax  y.min=@thick-7.2
y.max=@thick-0.2


$$$$doping nw region
doping unif conc=@nwell  n.type reg=2   x.min=0.8  x.max=@xmax  y.min=0   y.max=4


$$$$doping pw region
doping unif conc=@pwell  p.type reg=2   x.min=0.8  x.max=@xmax  y.min=0   y.max=1.8

$$$$ doping nbase region
doping n.peak=@nbase  n.type reg=2   x.min=0.8  x.max=@xmax  peak=0 y.max=0.6
junc=1.0


$$$doping nplus region
doping unif N.PEAK=@pplus  n.type  reg=2   x.min=3.5 x.max=4 y.min=0 y.max=0.3
doping unif N.PEAK=@pplus  n.type  reg=2   x.min=5 x.max=5.5 y.min=0 y.max=0.3


$$$doping pplus region
doping  unif N.PEAK=@nplus  p.type  reg=2   x.min=3  x.max=3.5 y.min=0 y.max=0.1
doping  unif N.PEAK=@nplus  p.type  reg=2   x.min=5.5  x.max=6 y.min=0 y.max=0.1

$$$$regrid
regrid doping abs log ratio=1
```

4. Breakdown characteristics run code

```
assign name=dobv  c.val=yes
assign name=bv    n.val=10000
assign name=icharge  n.val=1e11
assign name=name  c.val="TCIGBT"
```

```
if cond=(@dobv="yes")
mesh in.file=TCIGBT.med
option save.sol
contact name=gate n.poly
interface qf=@icharge
call file=parameter.inp
models  @models
symb carriers=0
solve init
symb newton carriers=2
method cont.stk
solve
solve v(gate)=0  v(anode)=0
log out.file="bv_"@name".log"
solve elec=anode vstep=0.01 nstep=100
solve elec=anode vstep=0.5 nstep=20
solve elec=anode vstep=1 nstep=20
solve elec=anode vstep=5 nstep=200
save out.f="bv_1k" solution
solve elec=anode vstep=5 nstep=200
save out.f="bv_2k" solution
solve elec=anode vstep=10 nstep=400
save out.f="bv_6k" solution
solve elec=anode vstep=10 nstep=100
save out.f="bv_7k" solution
solve elec=anode vstep=10 nstep=100
save out.f="bv_8k" solution
solve elec=anode vstep=10 nstep=100
save out.f="bv_9k" solution
solve elec=anode vstep=10 nstep=100
save out.f="bv_10k" solution
solve elec=anode vstep=10 nstep=200
save out.f="bv_12k" solution
solve elec=anode vstep=10 nstep=200
save out.f="bv_14k" solution
```

5. On-state characteristics run code

```
assign name=doiv  c.val=yes
assign name=va    n.val=5
assign name=icharge n.val=-1e11

mesh in.file=TCIGBT.med
option save.sol
contact name=gate n.poly
interface qf=@icharge
```

```
call file=parameter.inp
symb carriers=0
solve init
symb newton carriers=2
method cont.stk
solve
solve v(gate)=0 v(anode)=0
log out.file="iv_vg20.log"
solve elect=(gate) vstep=-0.5 nstep=40
solve elect=(anode)  vstep=-0.1 nstep=50
solve elect=(anode)  vstep=-1 nstep=5
save out.f="iv@10va" solution
solve elect=(anode)  vstep=-5 nstep=10
save out.f="iv@60va" solution
solve elect=(anode)  vstep=-4 nstep=10
save out.f="iv@100va" solution
solve elect=(anode)  vstep=-10 nstep=10
save out.f="iv@200va" solution
solve elect=(anode)  vstep=-10 nstep=50
save out.f="iv@700va" solution
solve elect=(anode)  vstep=-10 nstep=50
save out.f="iv@1200va" solution
solve elect=(anode)  vstep=-10 nstep=100
save out.f="iv@2200va" solution
solve elect=(anode)  vstep=-8 nstep=100
save out.f="iv@3000va" solution
solve elect=(anode)  vstep=-10 nstep=100
save out.f="iv@4000va" solution
solve elect=(anode)  vstep=-10 nstep=100
save out.f="iv@5000va" solution
solve elect=(anode)  vstep=-10 nstep=100
save out.f="iv@6000va" solution
solve elect=(anode)  vstep=-10 nstep=100
save out.f="iv@7000va" solution
solve elect=(anode)  vstep=-10 nstep=100
save out.f="iv@8000va" solution
```

6. Switching characteristics run code

```
assign name=vrail n.val=5000
assign name=ia n.val=50
assign name=J n.val=50
assign name=L n.val=6.5
assign name=W n.val=@ia/(@L*1e-8*@J)
assign name=icharge  n.val=1e11
assign name=name  c.val="SiC_CIGBT_SW"
assign name=msh  c.val="CIGBT"
```

```
mesh inf=TCIGBT.med
options save.sol
contact name=gate n.poly
interface qf=@icharge
call file=parameter.inp
symb newton carriers=0
solve
symb newton carriers=2
solve
save out.f=DUT mesh w.models
end
start circuit
Va   1  0  0
I1   0  2  50
d1   2  1  modela
Rg   3  4  5
Vg   4  0  pulse 20 -20 10n 10n 10n 25u 50e-6
PDUT 2=anode 3=Gate file=DUT width=@W
.model modela d
.ic v(3)=20 v(4)=20
finish circuit
save structure=pdut out.f=SIC_CIGBT.str15us mesh
symb carriers=0
solve init
symb newton carriers=2
method cont.stk
solve
$Voltage Source
solve element=Va v.elem=1    vstep=1       nstep=100
solve element=Va v.elem=100    vstep=2     nstep=150
solve element=Va v.elem=400    vstep=2     nstep=100
solve element=Va v.elem=600   vstep=1     nstep=200
solve element=Va v.elem=800   vstep=2     nstep=150
solve element=Va v.elem=1100  vstep=10   nstep=90
solve element=Va v.elem=2000  vstep=10     nstep=100
solve element=Va v.elem=3000  vstep=10     nstep=100
solve element=Va v.elem=4000  vstep=10     nstep=100

log out.f="sw_"@msh"_50u_20A.log"
save structure=pdut sol out.f="sw_"@msh"_T"
solve dt=1e-12  tstop=50e-6
```

7. Parameter File

```
$$$$MODELS used
assign name=models c.val="CONSRH AUGER IMPACT.I INCOMPLE BGN FLDMOB
PRPMOB ARORA TEMPERATURE=700 "
```

```
$$$PARAMETER VALUES
$$$BANDGAP ENERGY from PURDUE SIMULATIONS
assign name=egmodel n.val=1
assign name=permi n.val=9.66
assign name=eg300 n.val=3.23
assign name=egalpha n.val=4.73e-4
assign name=egbeta n.val=636
assign name=nc300 n.val=7.68e18
assign name=nv300 n.val=4.76e18

$$lattice temperature parameters
assign name=density  n.val=3.21e-3
assign name=a n.val=0.01
assign name=b n.val=6e-4
assign name=c c.val=6e-7

$$$SRH recombination
assign name=taun0 n.val=1e-6
assign name=taup0 n.val=1e-6
$$$$default values
assign name=nsrhn n.val=5e16
assign name=psrhn n.val=5e16
assign name=nsrhn n.val=1e16
assign name=psrhn n.val=1e16

$$$$AUGER recombination from JUE WANG's thesis[86]
assign name=augn n.val=8.3e-32
assign name=augp n.val=1.8e-31

$$$$INCOMPLETE IONIZATION from PURDUE UNIVERSITY SIMULATION
PARAMETERS[3]
assign name=edb n.val=0.066
assign name=eab n.val=0.191
$$$default MEDICI
assign name=gdb n.val=4
assign name=gcb n.val=2


$$$$IMPACT IONIZATION from JUE WANG'S THESIS[86]
assign name=nioniza n.val=1.66e6
assign name=ecnii       n.val=1.273e7
$$$default values from MEDICI
assign name=pioniza n.val=5.18e6
assign name=ecpii       n.val=1.4e7

$$$$BANDGAP NARROWING default values
assign name=conbgn n.val=9e-3
assign name=n0bgn n.val=1e17
```

```
$$$$ANALYTIC MOBILITY MODEL from jue wang's thesis and PURDUE SIMULATIONS[3]
assign name=nmin n.val=0
assign name=nmax n.val=950
assign name=pmin n.val=15.9
assign name=pmax n.val=124
assign name=Nrefn n.val=2e17
assign name=Nrefp n.val=1.76e19
assign name=nun n.val=-2.8
assign name=nup n.val=-2.8
assign name=alphan n.val=0.76
assign name=alphap n.val=0.34
$$$default MEDICI values for Nrefn2 and Nrefp2

$$$$FIELD MOBILITY MODEL FROM JUE WANG'S THESIS
assign name=vsatn n.val=2.7e7
assign name=vsatp n.val=2.7e7
assign name=betan n.val=2
assign name=betap n.val=1
assign name=fldmob n.val=1

$$$$SHIRAHATA MOBILITY MODEL FOR HIGH FIELD DEPENDENCE
assign name=e1n n.val=8.9e3
assign name=p1n n.val=0.28
assign name=e2n n.val=1.22e6
assign name=p2n n.val=2.9
assign name=e1p n.val=8e3
assign name=p1p n.val=0.3
assign name=e2p n.val=3.9e5
assign name=p2p n.val=1

$$$$Specifications
models  @models

$$ bandgap using EG.MODEL=1 as default change to 0 if necessary
material SIC EG.MODEL=@egmodel EG300=@eg300 PERMITTI=@permi
NC300=@nc300 +
  NV300=@nv300 EGALPH=@egalpha EGBETA=@egbeta CON.BGN=@conbgn
N0.BGN=@n0bgn
$$recombination
material SIC TAUN0=@taun0 TAUP0=@taup0 AUGN=@augn AUGP=@augp
EXP.TAU=1.72  EXN.TAU=1.72
$$EXP.TAU=2.8 EXN.TAU=2.2
$$$lattice temperature (used for Short circuit modelling)
material SIC DENSITY=@density A.TH.CON=@a B.TH.CON=@b C.TH.CON=@c
$$ionization impact and incomplete
material SIC EDB=@edb EAB=@eab N.IONIZA=@nioniza ECN.II=@ecnii
$$$mobility models
```

```
$$bulk mobility

$$arora model
MOBILITY SIC MUN1.ARO=0 MUN2.ARO=950 MUP1.ARO=15.9 MUP2.ARO=124 +
 AN.ARORA=0.76 AP.ARORA=0.34 CN.ARORA=1.94e17 CP.ARORA=1.76E19
 EXN1.ARO=0 EXP1.ARO=0 EXN2.ARO=-2.8 EXP2.ARO=-2.8 +
 EXN3.ARO=0 EXN4.ARO=0 EXP3.ARO=0 EXP4.ARO=0

$$PARELLEL SURFACE MOBILITY
MOBILITY SIC VSATN=@vsatn VSATP=@vsatp +
 BETAN=@betan BETAP=@betap FLDMOB=@fldmob

$$high field mobility
MOBILITY SIC E1N.SHI=@e1n EX1N.SHI=@p1n E2N.SHI=@e2n EX2N.SHI=@p2n
MOBILITY SIC E1P.SHI=@e1p EX1P.SHI=@p1p E2P.SHI=@e2p EX2P.SHI=@p2p
```

REFERENCES:

[1] J. Wang, " Silicon carbide power devices ". vol. Thesis (Ph.D.) Heriot-Watt University, 2000.

[2] G. G. Walden, "THE FUTURE OF SILICON CARBIDE HIGH POWER ELECTRONIC SWITCHES." vol. PhD: Purdue University, 2009, p. 196.

APPENDIX C :

List of Author's Publications

Main Author : Journal publications

1. "Performance Evaluation of 10-kV SiC Trench Clustered IGBT" , K. G. Menon, A. Nakajima, L. Ngwendson, and E. M. Sankara Narayanan, Electron Device Letters, September 2011.

2. "Numerical Evaluation of 10kV Clustered Insulated Gate Bipolar Transistor in 4H-SiC", K G Menon and E M Sankara Narayanan, IEEE Transaction on Electron Devices, Jan 2013.

Main author: Conference publications

3. "Ultra high performance of 12kV Clustered Insulated Gate Bipolar Transistor (CIGBT) in 4H-SiC", K G Menon, L Ngwendson, Akira Nakajima, E M Sankara Narayanan and G Bruce, International Conference on Silicon Carbide and Related Materials 2011, Cleveland Ohio.

4. "Comparison of 10kV N-channel and P-channel Trench Clustered Insulated Gate Bipolar Transistor (TCIGBT)", K G Menon and E M Sankara Narayanan, ISPS 2012, Prague.

Conference Talk:

5. "12kV Clustered Insulated Gate Bipolar Transistor (CIGBT) in 4H-SiC",Prof S Madathil and K Menon, Presentation at ISICPEAW, Kista, May 2011.

Co-authored publications:

6. "GaN-based Bidirectional Super HFETs Using Polarization Junction Concept on Insulator Substrate", A Nakajima, Sumida, Y. ; Kawai, H. ; Unni, V. ; Menon, K.G. ; Dhyani, M.H. ; Narayanan, E.M.S., ISPSD 2012, Belgium.

APPENDIX D :

List of figures

APPENDIX E :

List of tables