Design of Completion Detectors in Asynchronous Communication System

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Abstract. In digital design, there are two types of design, synchronous design and asynchronous design. In synchronous design, global clock is one of the main system that consume a lot of power. The power in synchronous design is consumed by clock even if there is no data processing take place. The asynchronous design that depends on data is clockless and as far as the power is concerned, asynchronous design does not consume much power compared with synchronous design and this really make asynchronus design the preffered choice for low power consumption. Besides having low power consumption, there are many advantages of aynchronous design compared with synchronous design. This paper proposed new dual rail completion detector (CD), 3-6 CD, 2-7 CD and 1-4 CD for on-chip communication that are used widely in an asynchronous communication system. The design of CD is based on the principle of sum adder. The circuit is designed by using Altera Quartus II CAD tools, synthesis and implementation process is executed to check the syntax error of the design. The design proved to be successful by using asynchronous on-chip communication in the simulation.

Keywords:Asynchronous, converter, completion detector, Quartus II

I. INTRODUCTION

In digital design, there are two types of design, synchronous design and asynchronous design. In synchronous design, global clock is one of the main system that consume a lot of power and therefore need to be removed for better power efficiency [1] [2] [3]. The power in synchronous design is consumed by clock even if there is no data processing take place. The asynchronous design that depends on data is clockless and as far as the power is concerned, asynchronous design does not consume much power compared with synchronous design and this really make asynchronous design the preferred choice for low power consumption. Besides having low power consumption, there are many advantages of asynchronous design compared with synchronous design. [4], [5].

(i) Absence of clock skew as the arrival time of the clock signal is depended on the data.

(ii) Better than worst case performance because for asynchronous design, the average case performance is the most likely case due to the data-dependent data flow and functional unit that exhibit data-dependent delay.

(iii) Automatic adaption to physical properties since in asynchronous design, it is depended on the data as a clock, the above factors are automatically adjusted and hence the designer need not to worry the functionality of the circuit even under the worst case scenario.

(iv) Reduced electromagnetic interference as the activities of the circuit is very much independent from one to another. Despite all the advantages of asynchronous design over synchro-nous design, some of the disadvantages include

(v) Deadlock which is common situation in asynchronous design that the system faces due to the incorrect circuit design, token mismatch and also by arbitration.

(vi) The arrival of the data is detected by a completion detection (CD). Since the asynchronous design is data dependent and detected by CD, the design of CD is a trivial task and in some cases, it is a complex task.

One of the components in the above system is particularly important to substitute the clock system is the completion detector (CD). The dual rail CD is the simplest circuit which is basically an XOR gate to detect 1-bit of dual rail code. However, for other codes such as 3-6 code and 2-7 code, the CD circuits are quite complex. The design of CD to detect the arrival of data is an important and non-trivial problem [6, 7]. Other than dual rail CD, author in [8] proposed a method called as Delay-Insensitive Minterm Synthesis (DIMS) to tackle the problem. By using this method, for m to n code, the code is broken into smaller codes and concatenated. Part of the code is divided into control group and body of the code.

II. METHODOLOGY

The purpose of the communication system is converting single rail to dual rail and back to single rail data as shown by Figure 1. Dual rail encoding is necessary for long on-chip interconnect since it is delay insensitive which refers to the data is transmitted correctly regardless of the delay in the interconnecting wires. It uses two wires to represent 1 bit of information. The intermediate code in the communication is 3-6 code. Even though the dual rail encoding is suitable for long on-chip interconnect communication, it suffers the lowest capacity (bits/wire) compared with other code. Hence, this makes it more costly. Table 1 compares some of the codes with information regarding the number of wires, transitions, capacities and the complexities. From Table 1, it is obvious that the 3-6 code has the highest capacity compared with other codes. Besides, the 3-6 code has double wire capacity compared with dual rail.

Revised Manuscript Received on January 05, 2020
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