Improved Delayering Method for SOI Wafer Processing

Handie Ahmataku[1*], Shahrol Mohamaddan [2], Mahshuri Yusuf [2], Aidil Azli Alias [2], Kuryati Kipli [2], and Norhayati Soin [3, 4]

[1] X-FAB Semiconductor Foundries AG, 1 Silicon Drive, Sama Jaya FIZ, 93350 Kuching Sarawak, Malaysia
[2]Faculty of Engineering, Universiti Malaysia Sarawak, 94300 Kota Samarahan, Sarawak, Malaysia
[3]VLSI Research Group, Department of Electrical Engineering, Faculty of Engineering, University of Malaya, Malaysia
[4]Center of Printable Electronics, University of Malaya, Malaysia
[*]Phone: +682354888 ext. 1310 Email: handie.ahmataku@xfab.com

***Abstract*- The benefits of Silicon on Insulator (SOI) technology are to reduce parasitic device capacitance, improving performance as well as smaller build area. Current delayering method to reveal polysilicon using 49% Hydrofluoric (HF) concentration is not suitable for SOI wafer. Furthermore, the method cannot remove small, thin and dense gate poly such as in Static Random Access Memory (SRAM) cells. The implication of the current method will cause Top Silicon to be damaged. A parallel lapping is used to improve surface flatness while exposing the polysilicon layer. Subsequently, Poly-etchant is employed to etch the exposed polysilicon and remaining the oxides. An optimum HF's concentration and etching time are crucial in order to etch the remaining oxides while protect Top Silicon from damage during SOI delayering process. The idea is to halt the oxide etching somewhere in Deep Trench Isolation (DTI) without delaminating Top Silicon on Buried Oxide (BOX). In addition to this process, Interlayer Dielectric (ILD) oxide, Gate Oxide (GOX) and polysilicon layer can be removed completely. Hence, 20% HF and 10 minutes etching time (HFt) followed by supersonic cleaning is a recommended combination for a complete removal of remaining layers on silicon surface, such as metals, polysilicon, nitride, and oxides. A clean exposed silicon substrate is vital to allow wet etchant solution to be carried out successfully to reveal silicon defects. Improved delayering method of Parallel Lapping → Poly-Etchant → Diluted and Time Controlled Hydrofluoric Acid Etching is capable to remove thin and dense polysilicon precisely without damaging the Top Silicon made it suitable for SOI technology..**

Keywords –SOI, Parallel lapping, Top Silicon, Buried Oxide, Delayering Method, Wet etchant.

I. INTRODUCTION

The SOI wafers increase chip functionality without the cost of major process equipment changes such as higher resolution lithography process tools. The advantages are faster circuit operation, reducing parasitic device capacitance, smaller devices build area and lower operating voltages [1]–[2]. The lower voltages, low power consumption and high performance for today requirements disclosed the limitations of Bulk Commentary Metal-Oxide Semiconductor (BulkCMOS) [3].

The existing of Buried Oxide (BOX) layer in between "handle wafer" and Top Silicon which linked with DTI oxide make polysilicon removal more challenging. The chemical wet etches such HF which supposed to etch GOX, loosen the gate poly attachment on active surface is now also etching the DTI trench oxide. In the worst scenario, etching can even go deeper into BOX layer which untie the Top Silicon attachment on BOX surface. Hence, the Top Silicon plate will peel off during the supersonic clean resulting in a loss of key information which is useful to discover physical cause of the failure.

Hence, using wet etch delayering alone, for instance 49%HF to remove all layers including polysilicon and revealing active layers only works for BulkCMOS wafer. This method cannot be used for SOI wafer since HF will etch ILD oxide all the way down to BOX and leave Top Silicon unattached [4]. Thus results Top Silicon structures to be damaged, crack and unclean as shown in Fig 1. This problem will not happen in BulkCMOS wafer since structure builds on bulk silicon wafer [5].

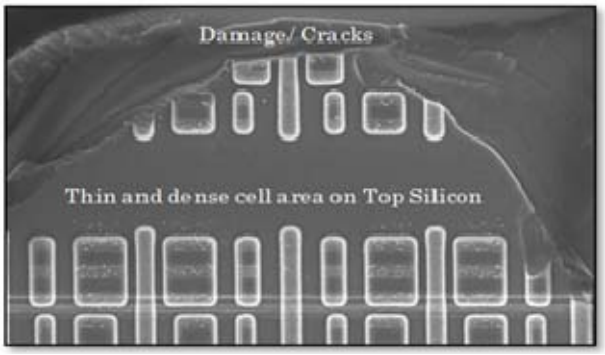

Fig. 1 SEM Images OF Top Silicon Crack due to Over-etch DTI Trench [5]

This work focuses on combination of parallel lapping + diluted and time controlled hydrofluoric chemical etching to remove small, thin and dense gate poly without damaging the Top Silicon [6]. Removing small, thin and dense gate poly by exposing epitaxial active layer is robust, stable, clean and controllable. This is important to ensure further analysis on active layer can be carried out successfully. For example, an investigation of active defect like originated particle (COP), dislocation and HF defects analysis (Lim, An, Guo, & Fan, 1998).