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The Analysis of Soft Error in C-elements

Norhuzaimin Julai, Ahmed M. A. Haidar, Abdul Rahman Kram
Departement of Electrical and Electronics Engineering, Faculty of Engineering, Universiti Malaysia Sarawak, Malaysia

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ABSTRACT

Soft errors are a serious concern in state holders as it can cause temporarily malfunction of the circuit. C-element is one of the state holders that is used widely in the asynchronous circuit. In this paper, the investigation will focus on the vulnerability of two types of C-element towards soft errors. A framework has been proposed for the rate of error due to neutron spectrum energy that can cause failure in the state holder. Effective analysis has been conducted on two different C-elements at different nodes by using UMC90 nm technology and 180nm technology. Based on the vulnerability data, a method for assessing vulnerability on a different implementation of C-elements has been developed. From the obtained data, it can be concluded that SIL is more resistant towards soft errors.

Corresponding Author:

Norhuzaimin Julai,
Department of Electrical and Electronics Engineering, Faculty of Engineering,
Universiti Malaysia Sarawak,
94300 Kota Samarahan, Sarawak, Malaysia.
E-mail: jnorhuza@unimas.my

1. INTRODUCTION

Asynchronous circuits operate without a clock and there are numerous advantages of using asynchronous circuits such as no clock skew problem and no global timing issues. Asynchronous circuits are also less affected by the technology and process [1]. There is also power issue in synchronous design since it utilizes clocks to make any transition at the logic. On the other hand, the power in asynchronous design will be less compared with synchronous design. However, one of the disadvantages of asynchronous circuit is the circuit failure due to deadlock: A state where the system will be disabled indefinitely until the system has been reset or the error is filtered or corrected from the system. That means the circuit will be in the waiting state unless there is a feedback or some kind of acknowledgement signal since it is depended on the data itself rather than clock to function. Single event upset (SEU) has been identified as a possible reason that caused data corruption. The term soft error refers to the temporarily error that is due to the particle strike provided the sufficient current and with certain width of current pulse is needed to cause the state change.

The PMOS or NMOS will be the most sensitive towards SEU when it is in the OFF mode, in particular at the drain region. Figure 1 shows the single event transient (SET) produced after an energetic ionizing particle has been brought to the silicon near sensitive device [2]. The density of electron-hole pairs is produced by particle as shown in Figure 1(a). The carriers are collected by electric field and will cause the charge collection to expand due to drift current (Figure 1(b)) and result in the sudden current pulse. Then, the diffusion current will dominate until all the excess carrier have been collected, recombined or diffused away from junction area (Figure 1(c)). The size of funnel as shown in Figure 1(b) and collection time is very much inversely proportion with the substrate doping. The collection time is usually complete within picoseconds and the diffusions current begin to dominate until all the excess carriers have been collected [3].