# High Efficiency CMOS Class E Power Amplifier Using 0.13 μm Technology

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***Abstract*—This paper presents the design of a 2.4-GHz CMOS Class E power amplifier (PA) for wireless applications in Silterra 0.13-μm CMOS technology. The Class E PA proposed in this paper is a single-stage PA in a cascode topology in order to minimize the device stress problem. All transistors are arranged in parallel to decrease on-resistance for high efficiency with on-chip input and output impedance matching. The simulation results indicate that the PA delivers 11.9 dBm output power and 53% power added efficiency (PAE) with 1.3-V power supply into a 50- Ω load. The chip layout is 0.27 mm².**

***Keywords-component; Class E; power amplifier; Silterra; output power; power added efficiency***

## I. INTRODUCTION

Recently, wireless systems demand a low cost, compact, power efficient, high integration and reliable consumers' devices. In addition, more and more signal processing is done in CMOS and high levels of integration are desired for reducing a cost and achieving compact systems. Hence, the wireless transceivers need to merge as many components as possible in a single chip using low cost technology. Therefore, there is a demand in utilizing CMOS PAs in a single chip transceiver called system on chip (SoC). However, as the down-scaling of MOS devices continues, the CMOS PA is not the optimum technology of choice due to the problem such as low oxide breakdown voltage, low current drive capability, substrate coupling, low quality and high tolerances of on-chip passives [1][2]. Although a lot of researches have been conducted recently to realize fully integration of PAs into SoC, unfortunately it is still a major challenge [3], particularly when designing in GHz frequencies range.

In CMOS, Class E PA is the most favored candidates among all classes of switching mode power amplifiers (Class D & Class F) due to their circuit simplicity and excellent PAE [4]. High PAE is important because PAs typically dominate the power consumption in a wireless transmitters system. However, the linearity is very poor due to the switching nature, thus the systems with the constant envelope modulation scheme such as FSK (or FM) are most suitable for switched-mode amplifiers. Furthermore, signal swing in a Class E PA can be two or three times the supply voltage that seriously stresses MOS devices. Safe device operating conditions can be guaranteed by decreasing supply voltage is usually less than the maximum available, at the price of efficiency degradation [1,5]. Cascode configurations have been used to overcome the device stress problem in MOS devices [1].

Most CMOS PAs that are published choose differential topology to obtain high linearity watt range [6]. Since the components driven by the PA and the antenna input are still single-ended, such a topology still requires off-chip baluns for converting signals from single-ended to differential and vice versa [7]. Therefore, fully integrated CMOS chip is difficult to realize. However, on-chip baluns can be integrated in differential topology for converting signals, but the design becomes complicated and increased the chip size [1],[8].

This paper describes a 2.4 GHz Class E single-stage PA designed using Silterra 0.13-μm CMOS process. The proposed design employed cascode topology to increase breakdown voltage and the power stage transistors are arranged in parallel to decrease the switch on-resistance. This method helps to reduce the losses thus increase efficiency.

## II. CIRCUIT DESIGN

The complete schematic of the proposed Class E PA single-stage cascode topology is shown in Fig. 1. Cin and Lin are part of the on-chip input matching. Rb is a bias resistance for M1.

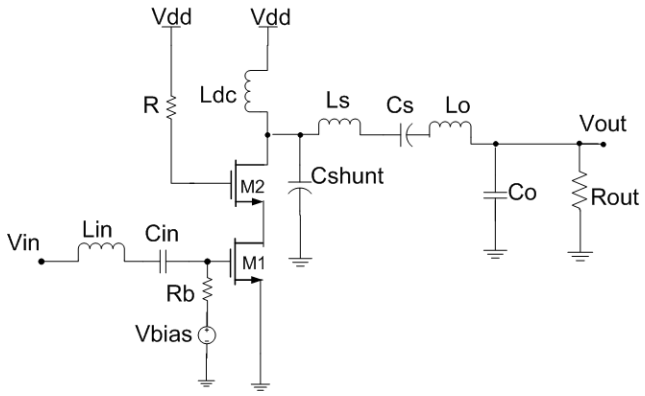


Figure 1. Complete schematic of the proposed single-stage Class E PA.