Improved Multiple Faults-Aware Placement Strategy: Reducing the Overheads and Error Rates in Digital Circuits

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Abstract:
State-of-the-art commercial placement tools have as goals to optimize area, timing, and power. Over the years, several reliability oriented placement strategies have been proposed with distinct goals, such as to improve the error rate. However, we found that there are still improvements that can be made for this type of approach, to improve not only the error rates but also the performance of the placer itself. Thus, this paper proposes several improvements toward an efficient multiple faults-aware placement strategy. First, an analytical method to profile pair of gates is proposed. Second, we add another level of optimization to reduce the amount of wirelength observed after the placement is completed without jeopardizing the main objective (reliability). Third, we propose a way to manipulate white spaces between gates smartly, to separate the gates that are profiled as the most likely to reduce the error rate when paired adjacently in the circuit. Results show that a wirelength reduction of up to 61% is achieved. Also, additional reduction of the error rate of up to 23% can be achieved with only an overhead on placement execution time.

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