COMPARISON OF PARALLEL PREFIX ADDER (PPA)

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Dedicated to my beloved parents, family members and friends

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ABSTRAK

Penambah awalan selari merupakan salah satu jenis penambah terpantas yang pernah direka dan dibangunkan. Dua jenis penambah awalan selari yang biasa digunakan adalah penambah Brent Kung dan penambah Kogge Stone. Projek ini akan membandingkan dan membuat kajian terhadap prestasi kedua-dua jenis penambah ini dari segi tundaan rambatan dan keluasan rekabentuk. Perbandingan dan kajian untuk kedua-dua penambah akan dijalankan untuk saiz bit 8, 16 dan 32. Dengan menggunakan perisian rekabentuk Quartus II, rekabentuk untuk untuk kedua-dua penambah Brent Kung dan penambah Kogge Stone akan dicipta. Daripada rekabentuk kedua-dua penambah, bentuk gelombang vektor akan dihasilkan daripada simulasi rekabentuk-rekabentuk tersebut. Hasil simulasi juga akan menunjukkan tundaan rambatan untuk penambah-penambah tersebut. Oleh itu, projek ini adalah penting bagi menunjukkan daripada kedua-dua penambah yang diuji, yang manakah menjalankan fungsi lebih baik dari segi tundaan rambatan dan rekabentuk kawasan berdasarkan saiz bit yang berbeza.

ABSTRACT

The parallel prefix adder is one of the fastest types of adder that had been created and developed. Two common types of parallel prefix adder are the Brent Kung and Kogge Stone adders. This project will compare and study the performances of these two adders in terms of propagation delay and design area. The comparison and study for both adders will be conducted for 8, 16 and 32 bits size. By using the Quartus II design software, the designs for both Brent Kung and Kogge Stone adders will be developed. From the designs of both adders, a vector waveform will be produced as a result of the designs' simulations. The simulation result will also show the propagation delay for the adders. Hence, this project is significant in showing which of the two adders being tested perform better in terms of propagation delay and design area based on different sizes of bits.

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LIST OF ABBREVIATIONS

PPA	-	Parallel Prefix Adder
BKA	-	Brent Kung Adder
KSA	-	Kogge Stone Adder
VHSIC	-	Very High Speed Integrated Circuit
VHDL	-	VHSIC Hardware Description Language
t_{pd}	-	Time Propagation Delay
x	-	Input bits
y	-	Input bits
s	-	Sum
c_{in}	-	Carry in
c_{out}	-	Carry out
RCA	-	Ripple Carry Adder
CLA	-	Carry Look-Ahead Adder
PFA	-	Partial Full Adder
VLSI	-	Very Large Scale Integration
g	-	Generates function
p	-	Propagate function
o	-	Carry Operator
n	-	number of bits
MSB	-	Most Significant Bit
LSB	-	Less Significant Bit
PG	-	Propagate-Generate function

FCO	-	Fundamental Carry Operator
PPC	-	Parallel Prefix Carry
PPS	-	Parallel Prefix Sum
SPICE	-	Simulation Program with Integrated Circuit Emphasis
RTL	-	Register Transfer Level
FPGA	-	Field-Programmable Gate Array
CPLD	-	Complex Programmable Logic Devices

CHAPTER 1

INTRODUCTION

1.1 Project Overview

This project is a research of two common adders of Parallel Prefix Adder (PPA) type, the Brent Kung Adder (BKA) and Kogge Stone Adder (KSA). BKA and KSA are chosen because these two adders are the most common adders being used in the electronic industry at the moment. The research is done by comparing the two PPAs based on their performances. The performances mentioned here are the speed and the area (cost) of the adders. The comparison is conducted for 8 bits, 16 bits and 32 bits for both PPAs.

Before comparing these two PPAs, the PPAs need to be designed first. PPAs can be designed by using PSpice or Quartus II software. The software Quartus II is chosen because it has designing files, Very High Speed Integrated Circuit (VHSIC) Hardware Description Language (VHDL) source file and other necessary files that can be used for the execution of the designed PPAs. The Quartus II software also comes with interactive tutorials to help its users to understand better. This project uses the Quartus II Version 9.0sp2 Web Edition.

This project will provide solid proof of the capabilities of BKA and KSA in terms of time delay, area and number of bits. The increase in area design will increase the cost price. Meanwhile, time delay plays a role in instancing the output. The shorter the time delays, the faster the output will be produced. From the proofs proven in this thesis, we will know which PPA is better in terms of performance, speed and cost.

1.2 Problem Statement

One problem that exists in this project is to find the differences between BKA and KSA in terms of area size for different number of bits. Although both are PPA that performs the same functions, these adders have differences between them. After conducting this project, the differences between BKA and KSA can be known. Another problem in this project is requirement to find which PPA is better in terms of time propagation delay (t_{pd}) with different numbers of bits. By conducting this project, it is interesting to see which PPA can perform better in terms of bits addition.

1.3 Project Objectives

The main objectives of this project are;

i) To design BKA and KSA using design software

ii) To simulate BKA and KSA with 8 bits, 16 bits and 32 bits by using Quartus II 9.0 SP2 Web Edition

iii) To compare the performance of both PPAs based on their speed

iv) To compare the performance of both PPAs based on their area (cost)

1.4 Project Scope

By considering the problem statement and objectives of this project, the scope of this project are to understand, design and compare the performance of both BKA and KSA. The specification of this project can be divided into three parts as follows:

i) Study and understand the basic principle of BKA and KSA

ii) Design the PPAs by using Quartus II software and simulate using the same software

iii) Describe the design and measurements obtained

iv) Compare the performances between BKA and KSA in terms of area and computational speed

1.5 Project Report Outline

This project has 5 main chapters. Chapter 1, which corresponds to this introduction, provides project overview, project scope and objectives of the project. The project overview gives a brief idea of what the project is really about. Project scope is mainly about the scope of work to be done in this project. The objectives are the main purposes why this project is conducted.

Chapter 2 of this thesis is the Literature Review. This chapter discusses about the basic idea of PPA. This chapter also explains how does PPA function based on its algorithm. The design for BKA and KSA will be shown here. This is followed by the discussion on the thoughts of previous researchers of PPA.

Chapter 3 is the Methodology this project. This chapter discusses the methods used to conduct this project which comprises of designing the PPAs and obtaining the simulation results. This chapter also describes the methods used to analyze and compare between the BKA and KSA. Basically it gives a more detailed outlook on how the project was done.

Chapter 4 is the Results, Analysis and Discussions. This chapter shows the results obtained from the project. Results are shown in tables, graphs and calculations. The results obtained here are derived from the predefined in Chapter 3, which is the methodology. The results will be analyze and discuss in this chapter. Discussion is done by translating the results into more understandable conclusions. Explanations on the result outcome will also be given in this chapter.

Chapter 5 is the Conclusion and Recommendations. This chapter summarizes all of the work that has been done. This chapter summarizes the conclusions and give some suggestions or recommendations for further works. All appendices are included at the end of the report, following the list of references.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

This project entitled a comparison of Parallel Prefix Adder (PPA). Comparison is defined as examining people or things for similarities and differences between them [1]. In the case for this project, the Brent Kung Adder (BKA) and Kogge Stone Adder (KSA) are the ones to be examined. Any similarities and differences between them will be discussed in this thesis. The PPA is a type of adder which performs data addition arithmetic at high speed. Parallel in this project's context means relating at a certain distance apart. Prefix on the other hand means arranging something in advance. Hence, the title parallel prefix adder mainly means an adder that arranges the output data in advance but relates them at a certain distance. Details on this type of adder will be further discussed in the following sections.

Arithmetic operations are used in all computers, calculators, mobile telephone and other various types of technology devices. That is why there is an increasing need of faster and higher performance adder in the technology world. The basic function of an adder is to sum up two or more different input bits in digital electronics. The most basic arithmetic that can be done by an adder is the addition of two binary bits [2]. Equations (2.1), (2.2), (2.3) and (2.4) are four most basic binary arithmetic operations that can be perform by an adder.

$$0 + 0 = 0 \tag{2.1}$$

$$1 + 0 = 1 \tag{2.2}$$

$$0 + 1 = 0 \tag{2.3}$$

$$1 + 1 = 1\ 0 \tag{2.4}$$

2.2 Half Adder

The four outputs from the basic binary arithmetic operations shown in Equations (2.1) – (2.4) are basically the outcome of a half adder. Half adder produces sum-bit and carry-bit by adding two bits of input binary data as shown in the Figure 2.1 [3]. The output expression of the half adder is expressed in Equations (2.5) and (2.6) where s is sum-bit, c_{out} is carry-bit and both x and y are data input bits.

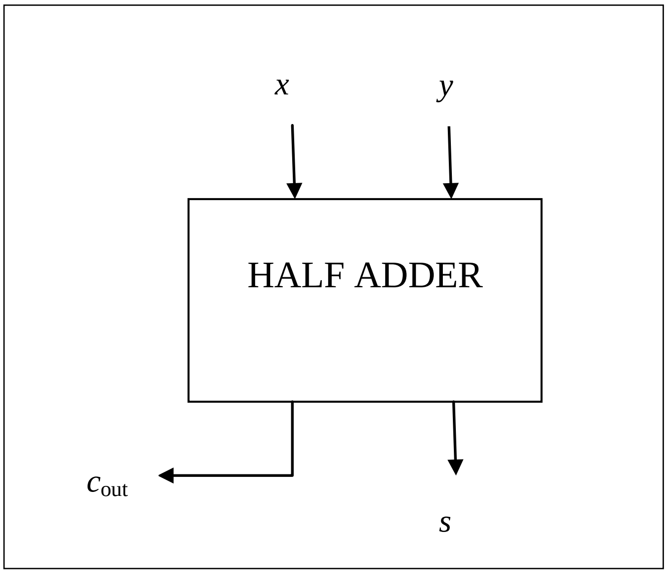

Figure 2.1: Half Adder Logic Symbol

$$s = x \oplus y \tag{2.5}$$

$$c_{\text{out}} = x \cdot y \tag{2.6}$$

From Equations (2.5) and (2.6), we can see that the sum-bit of a half adder is the same as the product of an XOR gate for two input binary bits. On the other hand, the carry-bit is the same as the product of an AND gate for two input binary bits. Hence, the half adder logic diagram is shown in Figure 2.2 in gate logic form.

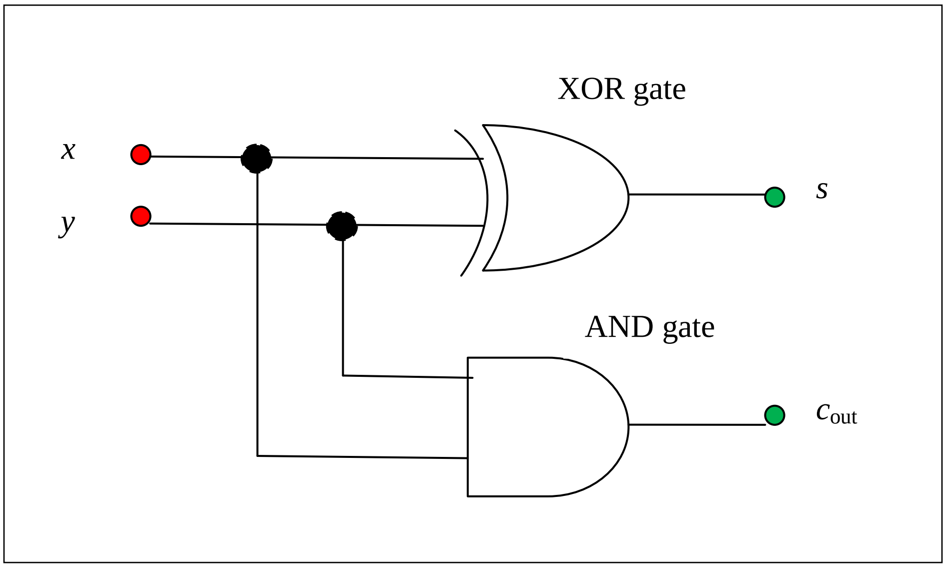

Figure 2.2: Half Adder Logic Diagram

When both data input bits, *x* and *y* are 0, the output bits, *s* and c_{out} are also 0. The sum output, *s* is 1 if the input variables, *x* and *y* are not equal. Output carry bit, c_{out} however is 0. When both input data bits are 1, the sum bit will be 0, meanwhile the output carry bit, c_{out} is 1. Table 2.1 shows the truth table for half adder.