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Magnetising inductance of multiple-output flyback dc–dc convertor for discontinuous-conduction mode

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Abstract: This study presents the following: (i) detailed derivation of the expressions for the maximum value of the magnetising inductance of the ideal and lossy two-output flyback dc–dc convertor operating in discontinuous-conduction mode, (ii) a method to appropriately select the duty cycle for the metal–oxide–semiconductor field-effect transistor based on the rated output dc voltages of the two stages, and (iii) a design approach for a three-winding transformer with a gapped core used in the two-output flyback convertor. The expressions derived and the proposed design technique can be extended to flyback convertors with more than two output stages with equal or unequal load voltages. A universal power supply (ac line adapter) employing a flyback dc–dc convertor with output voltages 15 and 32 V, supplying a rated output current of 0.563 and 0.533 A, and operating at a switching frequency of 85 kHz is designed using the proposed methodology. Simulation and experimental results are presented to validate the theoretical predictions.

1 Introduction

The multiple-output flyback dc–dc convertor is a widely used topology for applications such as LED drivers, power supplies for point-of-load applications, universal power supplies for laptop chargers, and so on [1–30]. In addition to the several benefits of flyback convertors, the multiple-output flyback convertors is capable of providing equal or unequal output powers in each stage, isolate each output stage, provide regulated dc output voltages simultaneously, and offer a reduced parts count [1–4].

In a flyback convertor, the ability to transfer energy from the power source to the output stages depends mainly on the magnetising inductance of the transformer. Hence, its appropriate value must be chosen to satisfy: (i) the power requirement and (ii) the mode of operation. The analysis of the single-output or the conventional flyback dc–dc convertors in both continuous-conduction mode (CCM) and discontinuous-conduction mode (DCM) is well documented in the literature [4–33]. A short design procedure and component selection for the multiple-output flyback dc–dc convertors have been discussed in [5–8]. In [5, 6], the magnetising inductance was calculated in terms of the total input power or output power and does not take into account the resistance and voltage of the individual output stages. A closed-form solution for calculating the magnetising inductance in terms of the load parameters (resistance and voltage) was introduced in [8] for the multiple-output flyback convertor in CCM. A detailed steady-state analysis and design methodology for the multiple-output flyback convertor in DCM has not been reported in the literature.

This paper provides closed-form solutions to determine the various parameters for the operation of the multiple-output flyback converter in DCM. Analysis of the steady-state waveforms, derivations of the expressions for the current and voltage transfer functions and the magnetising inductance, and the method to design a transformer with multiple windings are presented. The study is focused on two-output flyback convertors, and the results can be extended to topologies with more than two outputs as well. The main objectives of this paper are as follows:

i. To determine the expressions for the maximum value of the magnetising inductance to ensure DCM operation of ideal and lossy multiple-output flyback convertors.
ii. To determine the criteria to choose the duty ratio, when the flyback convertor is loaded by multiple-output stages with equal or unequal output voltages.
iii. To propose a method for the design of the multiple-winding transformer.
iv. To validate the theoretical results through simulations and experiments.

The paper is organised as follows. Section 2 provides a general overview of the two-output flyback convertor and discusses its steady-state operation in DCM. Section 3 presents the derivations for the maximum magnetising inductance and the duty cycle for operation in DCM. The expressions for both ideal and lossy multiple-output flyback convertors are presented. In Section 4, the design of a universal power supply (ac power adapter) with two independent output stages is shown and the coil-core arrangement for a three-winding transformer is proposed. Section 5 provides validation of theoretical results through simulations and experiments, while Section 6 concludes the paper and provides suggestions for future work.

2 Circuit description

Fig. 1*a* shows the circuit diagram and the equivalent circuit of the flyback convertor with two output stages. The input dc voltage source V_I is connected in series with the three-winding transformer. The primary winding L_p of the transformer has N_p number of turns, the secondary winding L_{s1} of the first output stage consists of N_{s1} number of turns, and the secondary winding L_{s2} of the second output stage consists of N_{s2} number of turns. The inductance L_m, as shown in Fig. 1*b* represents the magnetising inductance of the transformer responsible for storing the energy required for the flyback operation. The winding dc resistances of the primary and the two secondaries are r_{Tp}, r_{Ts1}, and r_{Ts2}, respectively.

The metal–oxide–semiconductor field-effect transistor (MOSFET) S is in series with the primary winding. The first and second output stages consist of the rectifying diodes D_{s1} and D_{s2}, respectively, while the filter network of the two stages are formed by $C_1 - R_{L1}$ and $C_2 - R_{L2}$, respectively.

The turns ratios for the three-winding transformer are defined as

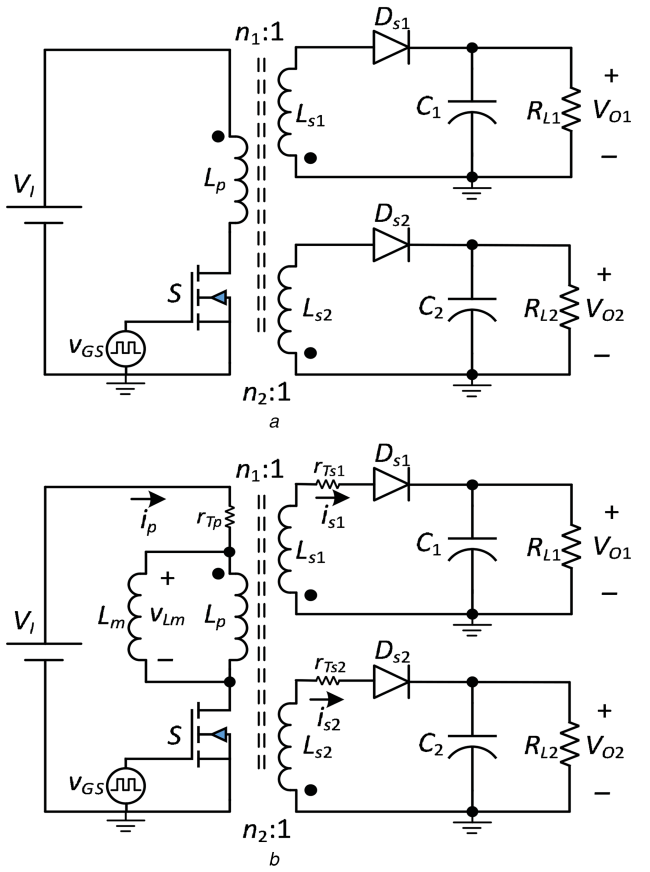


Fig. 1 *Two-output flyback dc–dc convertor*
(a) Circuit diagram of the convertor, ***(b)*** Equivalent circuit of the convertor showing the magnetising inductance across the primary winding

$$n_1 = \frac{N_\mathrm{p}}{N_{\mathrm{s}1}}, \quad n_2 = \frac{N_\mathrm{p}}{N_{\mathrm{s}2}} \tag{1}$$

The MOSFET S is controlled by the gate-to-source voltage v_{GS} at a switching frequency f_s and a duty cycle D. Fig. 2 shows the idealised waveforms of gate-to-source voltage v_{GS}, current i_{Lm} through L_m, voltage v_L across L_m, and drain-to-source voltage v_{DS} for the flyback convertor operating in DCM. For the interval $0 < t \leq DT$, S is ON and the input current i_I energises the magnetising inductance L_m. The currents through the secondary windings $i_{\mathrm{s}1}$ and $i_{\mathrm{s}2}$ are zero. Thus, the current through the primary winding L_p is also zero, hence $i_\mathrm{I} = i_{Lm}$. Consequently, when the MOSFET is OFF in the interval $DT < t \leq T$, the magnetising inductance L_m discharges the stored energy during the time DT to D_1T through the primary winding L_p and delivers power to the load resistance due to the turn-on of the diodes $D_{\mathrm{s}1}$ and $D_{\mathrm{s}2}$. For the time interval D_1T to T, the magnetising inductance current is zero, S is OFF, $D_{\mathrm{s}1}$, $D_{\mathrm{s}2}$ are also OFF and the filter capacitors sustain the required load voltages.

Applying volt-second balance to v_{Lm}, we get

$$V_\mathrm{I}DT = n_1V_{\mathrm{O}1}D_1T = n_2V_{\mathrm{O}2}D_1T, \tag{2}$$

where V_I is the supply voltage, D is the duty cycle of the MOSFET, D_1 is the duty cycle of the diodes $D_{\mathrm{s}1}$, $D_{\mathrm{s}2}$, n_1, n_2 are the turns ratios of the transformers given in (1). The dc voltage transfer function for DCM operation of the first output stage is

$$M_{\mathrm{VDC}1} = \frac{V_{\mathrm{O}1}}{V_\mathrm{I}} = \frac{D}{n_1D_1}, \tag{3}$$

and that for the second output stage is

$$M_{\mathrm{VDC}2} = \frac{V_{\mathrm{O}2}}{V_I} = \frac{D}{n_2D_1}. \tag{4}$$

Using (3) and (4), the two output voltages and the turns ratios can be related as

$$\frac{V_{\mathrm{O}1}}{V_{\mathrm{O}2}} = \frac{n_2}{n_1} = n. \tag{5}$$

The waveform of the current i_{Lm} through L_m is shown in Fig. 3 for the minimum and the maximum input voltages, V_{Imin} and V_{Imax}, respectively. The waveforms represent the operation of the convertor at the boundary between the CCM and DCM. The average input current at boundary is I_{IB} and the duty cycle at boundary is D_B. For CCM, the maximum inductor current ripple is considered, which occurs at $V_I = V_{\mathrm{Imax}}$ and $D = D_{\mathrm{min}}$. For DCM, the minimum inductor current ripple $\Delta i_{Lm(\mathrm{min})}$ must be considered and is the focus of study in the following section.

3 Maximum magnetising inductance and duty cycle in DCM

General expressions for the maximum magnetising inductance for the ideal and lossy multiple-output flyback convertor in DCM are derived in this section. Further, the criterion to decide the appropriate duty cycle for the multiple-output convertor with equal or unequal output voltages is discussed.

i. *For an ideal flyback convertor* ($\eta = 1$): One may observe that the inductor current ripple Δi_L (or the peak-to-peak value) is minimum, when the input voltage $V_\mathrm{I} = V_{\mathrm{Imin}}$ at $D = D_\mathrm{B}$, where D_B is the duty cycle at the boundary between CCM and DCM. This operating point is the worst case condition for the DCM, at which, the maximum value of the magnetising inductance must be estimated. The minimum value of the inductor current ripple is given by

$$\Delta i_{Lm(\mathrm{min})} = \frac{V_{\mathrm{Imin}}D_\mathrm{B}}{f_\mathrm{s}L_{\mathrm{m(max)}}}. \tag{6}$$

The input energy transferred to L_m from the supply voltage source during transistor ON-time at the boundary between the CCM and DCM is

$$W_{\mathrm{IB}} = \frac{1}{2}L_{\mathrm{m(max)}}\Delta i^2_{Lm(\mathrm{min})}, \tag{7}$$

and the resulting input power is

$$P_{\mathrm{IB}} = \frac{W_{\mathrm{IB}}}{T} = \frac{1}{2}L_{\mathrm{m(max)}}\Delta i^2_{Lm(\mathrm{min})}f_\mathrm{s}. \tag{8}$$

Substituting (6) into (8), we obtain

$$P_{\mathrm{IB}} = \frac{1}{2}\frac{V^2_{Imin}D^2_\mathrm{B}}{f_\mathrm{s}L_{\mathrm{m(max)}}}. \tag{9}$$

The total maximum output power of the convertor at the boundary between CCM and DCM is the sum of output powers of each stage

$$P_{\mathrm{OB}} = P_{\mathrm{O1B}} + P_{\mathrm{O2B}} = \frac{V^2_{\mathrm{O}1}}{R_{\mathrm{L1(min)}}} + \frac{V^2_{\mathrm{O}2}}{R_{\mathrm{L2(min)}}}, \tag{10}$$

where $P_{\mathrm{O1B}}, P_{\mathrm{O2B}}$ are the maximum output powers and $R_{\mathrm{L1(min)}}, R_{\mathrm{L2(min)}}$ are the minimum values of the load resistance of each stage. Assuming that the convertor is ideal, then $P_{\mathrm{IB}} = P_{\mathrm{OB}}$. Equating (9) and (10), the expression for the maximum magnetising inductance is obtained as

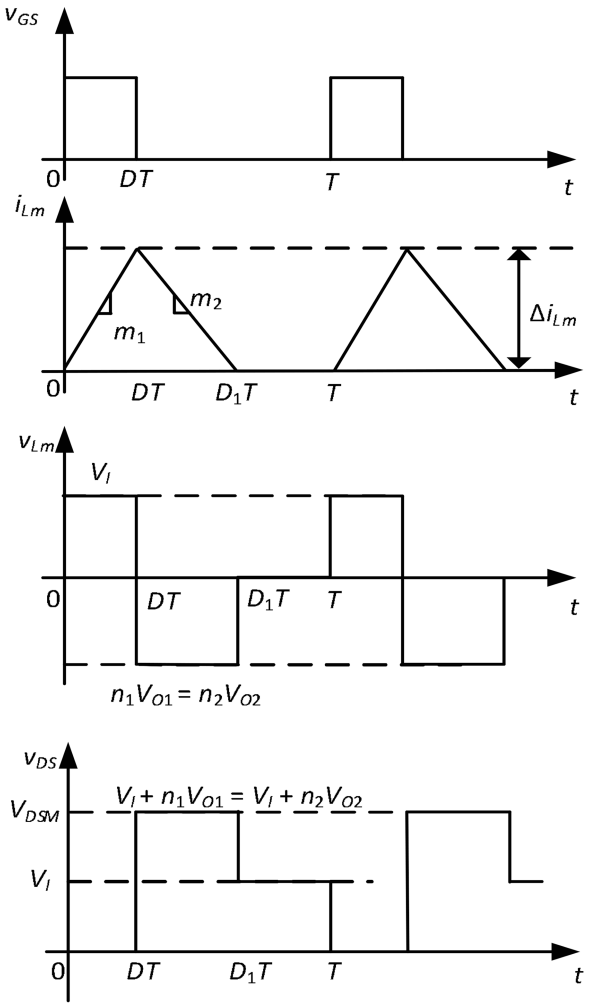


Fig. 2 *Ideal current and voltage waveforms of the two-output flyback convertor in DCM*

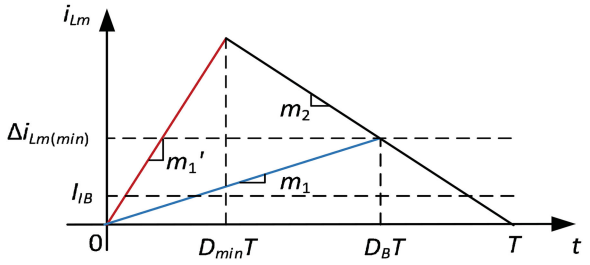


Fig. 3 *Waveforms of the magnetising inductor current at* $V_I = V_{Imin}$ *and* $V_I = V_{Imax}$, *where* $m_1 = V_{Imin}/L_m$, $m_{1'} = V_{Imax}/L_m$, *and* $m_2 = -n_1V_{O1}/L_m = -n_2V_{O2}/L_m$

$$L_{m(max)} = \frac{V_{Imin}^2 D_B^2}{2f_s} \frac{1}{(V_{O1}^2/R_{L1(min)}) + (V_{O2}^2/R_{L2(min)})}. \quad (11)$$

The dc voltage transfer functions at the boundary between the two modes for the two stages are

$$M_{VDC1B} = \frac{V_{O1}}{V_{Imin}} = \frac{D_B}{n_1(1-D_B)} \quad (12)$$

or

$$M_{VDC2B} = \frac{V_{O2}}{V_{Imin}} = \frac{D_B}{n_2(1-D_B)}. \quad (13)$$

The expressions in (12) or (13) can be rearranged to get V_{Imin}. Substituting for V_{Imin} and $V_{O2} = V_{O1}/n$ into (11) results in the maximum value of the magnetising inductance required for the two-output ideal flyback dc–dc convertor required to ensure DCM. The maximum inductance is

$$L_{m(max)} = \frac{n_1^2(1-D_B)^2}{2f_s} \frac{1}{(1/R_{L1(min)}) + (1/n)^2(1/R_{L2(min)})} \quad (14)$$

or in terms of the second output stage, the inductance is

$$L_{m(max)} = \frac{n_2^2(1-D_B)^2}{2f_s} \frac{1}{(n^2/R_{L1(min)}) + (1/R_{L2(min)})}. \quad (15)$$

Thus, the selected value of the magnetising inductance must satisfy $L_m < L_{m(max)}$ for the convertor to operate in DCM. In general, for the flyback convertor with multiple-output stages, the maximum magnetising inductance must not exceed

$$L_{m(max)} = \frac{n_1^2(1-D_B)^2}{2f_s} \frac{1}{(1/R_{L1(min)}) + \sum_{k=2}^{m}(N_{sk}/N_{s1})^2(1/R_{Lk(min)})}, \quad (16)$$

where m is the number of output stages, N_{sk}/N_{s1} is the ratio of the number of secondary turns of the kth output stage to the number of secondary turns of the first output stage.

The expression for magnetising inductance in (14) can be expressed in terms of the two load currents and load voltages as

$$L_{m(max)} = \frac{n_1^2(1-D_B)^2}{2f_s} \frac{V_{O1}}{I_{O1(max)} + (I_{O2(max)}/n)}. \quad (17)$$

Similar expression in terms of the second output stage can be written by suitably manipulating (15).

1. *For a lossy flyback convertor* ($\eta < 1$): The derivation for the maximum magnetising inductance in DCM for the two-output lossy flyback convertor is similar to that presented above. The input power and the total output power of the lossy convertor at the boundary between CCM and DCM are related as $P_{OB} = \eta P_{IB}$, where η is the overall efficiency of the convertor. Using (9) and (10), we get

$$\frac{V_{O1}^2}{R_{L1(min)}} + \frac{V_{O2}^2}{R_{L2(min)}} = \frac{\eta}{2}\frac{V_{Imin}^2 D_B^2}{f_s L_{m(max)}}, \quad (18)$$

resulting in the maximum magnetising inductance as

$$L_{m(max)} = \frac{\eta V_{Imin}^2 D_B^2}{2f_s} \frac{1}{(V_{O1}^2/R_{L1(min)}) + (V_{O2}^2/R_{L2(min)})}, \quad (19)$$

or equivalently

$$L_{m(max)} = \frac{\eta n_1^2(1-D_B)^2}{2f_s} \frac{1}{(1/R_{L1(min)}) + (1/n)^2(1/R_{L2(min)})}. \quad (20)$$

Using the power losses and efficiency analysis presented in [10], the total power loss in the two-output flyback convertor obtained by neglecting the MOSFET switching loss, transformer core loss, and the loss in the filter capacitors is

$$P_{LS} = D\Delta i_{Lm(max)}^2 \frac{R_p}{3} + \Delta i_{Lm(max)} D_1 \left[\frac{\Delta i_{Lm(max)} R_s}{3} + \frac{V_F}{2}\right]. \quad (21)$$

Fig. 1 shows the circuit of the flyback convertor with the winding resistances included. In (21), the total resistance of the primary-side R_p is the sum of the primary-winding dc resistance r_{Tp} and MOSFET on-resistance r_{DS} given as $R_p = r_{Tp} + r_{DS}$, total resistance of the two secondary-sides R_s is the sum of the secondary-winding resistances r_{Ts1}, r_{Ts2} and the diode forward resistances R_{F1}, R_{F2} given by $R_s = r_{Ts1} + r_{Ts2} + R_{F1} + R_{F2}$, and the total diode forward voltage is $V_F = V_{F1} + V_{F2}$, where V_{F1}, V_{F2} are the individual forward voltages of the diodes D_{s1} and D_{s2}, respectively. Using (21), the overall efficiency is

$$\eta = \frac{P_O}{P_O + P_{LS}} = \frac{1}{1 + (P_{LS}/P_O)}. \tag{22}$$

For the multiple-output topology, the total power loss is

$$P_{LS} = D\Delta i^2_{Lm(max)}\frac{R_p}{3} + \sum_{k=2}^{m}\Delta i_{Lm(max)}D_1\frac{\Delta i_{Lm(max)}R_{sk}}{3} + \frac{V_{Fk}}{2}, \tag{23}$$

where R_{sk} is the total parasitic resistances at the output side of the multiple-winding transformer with k stages and V_{Fk} is the sum of the forward voltage of all the diodes in the k output stages of the transformer. Therefore, for the multiple-output flyback convertor, the efficiency reduces with the addition of an output stage. Consequently, the value of the maximum allowable magnetising inductance $L_{m(max)}$ also reduces as more stages are added.

3.1 Duty cycle to ensure DCM operation

The analysis in this section considers an ideal transformer. For the chosen value of $L_m < L_{m(max)}$ described in the previous section, the maximum duty cycle $D_{MAX} < D_B$ can be obtained from (20) as

$$D_{MAX} = 1 - \frac{1}{n_1}\sqrt{\frac{2L_m f_s}{\eta R_{L(eq)}}}, \tag{24}$$

where $R_{L(eq)}$ is the equivalent load resistance for the convertor with two output stages given by

$$R_{L(eq)} = \frac{1}{(1/R_{L1(min)}) + (1/n)^2(1/R_{L2(min)})} = \frac{R_{L1(min)}n^2R_{L2(min)}}{R_{L1(min)} + n^2R_{L2(min)}}. \tag{25}$$

Thus, for k number of output stages, the equivalent resistance is

$$R_{L(eq)} = \frac{1}{(1/R_{L1(min)}) + \sum_{k=2}^{m}(N_{sk}/N_{s1})^2(1/R_{Lk(min)})}, \tag{26}$$

where m is the number of output stages, N_{sk}/N_{s1} is the ratio of the number of secondary turns of the kth output stage to the number of secondary turns of the first output stage. The dc load current of either of the two stages for the operation of the flyback convertor in DCM is

$$I_{O1} = \frac{1}{T}\int_0^T i_{D1}\,dt = \frac{1}{T}\int_{DT}^{(D+D_1)T} i_{D1}\,dt. \tag{27}$$

In the interval $DT > t \geq (D + D_1)T$, the diode current is a fraction of the magnetising inductor current, i.e. $i_{D1} = n_1\Delta i_{Lm}/2$ yielding

$$I_{O1} = \frac{D_1 n_1 \Delta i_{Lm}}{2}. \tag{28}$$

However, from (6), the inductor current ripple at any duty cycle $D < D_{MAX}$ is $\Delta i_{Lm} = V_I D/f_s L_m$, yielding

$$I_{O1} = \frac{n_1 D D_1 V_I}{2f_s L_m} = \frac{V_{O1}}{R_{L1}}. \tag{29}$$

Similarly, the dc load current in the second stage is

$$I_{O2} = \frac{n_2 D D_1 V_I}{2f_s L_m} = \frac{V_{O2}}{R_{L2}}. \tag{30}$$

From (29) and (30), the dc voltage transfer functions in terms of the circuit components and parameters are

$$M_{VDC1} = \frac{V_{O1}}{V_I} = \frac{n_1 D D_1 R_{L1}}{2f_s L_m}, \tag{31}$$

and that for the second output stage is

$$M_{VDC2} = \frac{V_{O2}}{V_I} = \frac{n_2 D D_1 R_{L2}}{2f_s L_m}. \tag{32}$$

Equating the right-hand sides of (3) with (31) and (4) with (32) yields

$$D_1 = \frac{1}{n_1}\sqrt{\frac{2f_s L_m}{R_{L1}}} = \frac{1}{n_2}\sqrt{\frac{2f_s L_m}{R_{L2}}}. \tag{33}$$

Substituting (33) into (3) and (4) gives

$$M_{VDC1} = \frac{D}{n_1 D_1} = D\sqrt{\frac{R_{L1}}{2f_s L_m}}. \tag{34}$$

and that for the second output stage is

$$M_{VDC2} = \frac{D}{n_2 D_1} = D\sqrt{\frac{R_{L2}}{2f_s L_m}}, \tag{35}$$

yielding the duty cycle as

$$D = M_{VDC1}\sqrt{\frac{2f_s L_m}{R_{L1}}} = M_{VDC2}\sqrt{\frac{2f_s L_m}{R_{L2}}}. \tag{36}$$

The duty ratio must be less than D_{MAX} as given in (24). If the output stages have unequal load voltages, then the duty cycle can be determined as

$$D = \max\left\{M_{VDC1}\sqrt{\frac{2f_s L_m}{R_{L1}}},\quad M_{VDC2}\sqrt{\frac{2f_s L_m}{R_{L2}}}\right\}. \tag{37}$$

In general, the duty cycle for the multiple-output flyback convertor in DCM is

$$D = \max\left\{M_{VDC1}\sqrt{\frac{2f_s L_m}{R_{L1}}}, \ldots, \ldots, M_{VDCk}\sqrt{\frac{2f_s L_m}{R_{Lk}}}\right\}, \tag{38}$$

where M_{VDCk} is the dc voltage transfer function between the supply and the kth output stage and R_{Lk} is the load resistance of the kth output stage.

4 Multiple-output flyback convertor design for DCM

A universal power supply (ac power adapter) that accepts a single-phase line voltage from 100 to 240 V_{rms} capable of operating at line frequencies of 50 and 60 Hz is designed in this section. The power adapter must supply two output stages with the following load voltages and currents:

- Stage 1 – $V_{O1} = 32$ V at $0 \leq I_{O1} \leq 0.563$ A.

- Stage 2 – $V_{O2} = 15$ V at $0 \le I_{O2} \le 0.533$ A.

The switching frequency of the MOSFET is $f_s = 85$ kHz and the output voltage ripple must satisfy the condition $V_{r1}/V_{O1} = V_{r2}/V_{O2} < 1\%$.

4.1 Calculation of magnetising inductance

The minimum and maximum values of the dc input voltage are

$$V_{Imin} = \sqrt{2}V_{rms(min)} = \sqrt{2} \times 100 = 141.42\,\text{V} \tag{39}$$

and

$$V_{Imax} = \sqrt{2}V_{rms(max)} = \sqrt{2} \times 240 = 339.41\,\text{V}\,. \tag{40}$$

A tolerance factor ($\simeq 10\%$) of the supply voltage is neglected. The minimum dc voltage transfer ratios for the two output stages are

$$M_{VDC1(min)} = \frac{V_{O1}}{V_{Imax}} = \frac{32}{339.41} = 0.094 \tag{41}$$

and

$$M_{VDC2(min)} = \frac{V_{O2}}{V_{Imax}} = \frac{15}{339.41} = 0.0441. \tag{42}$$

Similarly, the maximum dc voltage transfer ratios are

$$M_{VDC1(max)} = \frac{V_{O1}}{V_{Imin}} = \frac{32}{141.42} = 0.2262 \tag{43}$$

and

$$M_{VDC2(max)} = \frac{V_{O2}}{V_{Imin}} = \frac{15}{141.42} = 0.106. \tag{44}$$

The minimum values of the load resistance of the two stages are

$$R_{L1(min)} = \frac{V_{O1}}{I_{O1(max)}} = \frac{32}{0.563} = 56.83\,\Omega \tag{45}$$

and

$$R_{L2(min)} = \frac{V_{O2}}{I_{O2(max)}} = \frac{15}{0.533} = 28.14\,\Omega\,. \tag{46}$$

The next step in the design process is to determine the turns ratios of the two-output transformer. For DCM operation, the following inequality must be satisfied $D + D_1 < 1$ for the entire range of the input voltage and the output current. Let us assume the duty cycle at the CCM/DCM boundary as $D_B = 0.4$. Using (12) and (13)

$$n_1 = \frac{D_B}{(1 - D_B)M_{VDC1(max)}} = \frac{0.4}{(1 - 0.4) \times 0.2262} = 2.94 \tag{47}$$

and

$$n_2 = \frac{D_B}{(1 - D_B)M_{VDC2(max)}} = \frac{0.4}{(1 - 0.4) \times 0.106} = 6.28. \tag{48}$$

Let $n_1 = 3$ and $n_2 = 6$, resulting in $n = n_2/n_1 = 2$. Assuming an overall efficiency of $\eta = 0.95$, the maximum value of the magnetising inductance can be estimated using (20) as

$$\begin{aligned} L_{m(max)} &= \eta \frac{n_1^2(1 - D_B)^2}{2f_s} \frac{1}{(1/R_{L1(min)}) + (1/n)^2(1/R_{L2(min)})} \\ &= \frac{0.95 \times 3^2 \times (1 - 0.4)^2}{2 \times 85 \times 10^3} \frac{1}{(1/56.83) + (1/2)^2 \times (1/28.14)} \\ &= 683.74\,\mu\text{H}\,. \end{aligned} \tag{49}$$

A Magnetics® ferrite ETD gapped core OP-42929 was chosen. The core was selected using the A_p method and a detailed procedure is given in the following section. The core cross-sectional area is $A_c = 76$ mm^2, the mean magnetic path length is $l_c = 72$ mm, the air gap length is $l_g = 0.2$ mm $\pm$ 5%, and core relative permeability is $\mu_{rc} = 2250 \pm 20\%$. The worst case condition is at minimum l_g, i.e. $l_{g'} = l_g - 0.05l_g = 0.19$ mm, which exists due to mechanical aberrations and at minimum core relative permeability $\mu'_{rc} = \mu_{rc} - 0.2\mu_{rc} = 1800$. The number of turns of the primary winding can be calculated as

$$\begin{aligned} N_p &= \sqrt{\frac{L_m}{\mu_0 A_c}\left(l_{g'} + \frac{l_c}{\mu_{rc'}}\right)} \\ &= \sqrt{\frac{683.74 \times 10^{-6}}{4\pi \times 10^{-7} \times 76 \times 10^{-6}}\left(0.19 + \frac{72}{1800}\right) \times 10^{-3}} = 40.57. \end{aligned} \tag{50}$$

To ensure convertor operation in DCM, let the selected number of turns of the primary winding be $N_p = 36$. Thus, the new magnetising inductance at $N_p = 36$ can be obtained by manipulating (50) to get $L_m = 534.7\,\mu\text{H} < L_{m(max)}$. Consequently, the self-inductance of the secondary winding of the first output stage is $L_{s1} = L_m/n_1^2 = 59.411\,\mu$H and that of the second output stage is $L_{s2} = L_m/n_2^2 = 14.85\,\mu$H.

By inspection, the duty cycle required to provide V_{O1} is greater than that for V_{O2}. Using (37), the minimum duty cycle at full load required to deliver $V_{O1} = 32$ V is

$$\begin{aligned} D_{min} &= M_{VDC1(min)}\sqrt{\frac{2f_sL_m}{R_{L1(min)}}} \\ &= 0.094\sqrt{\frac{2 \times 85 \times 10^3 \times 534.7 \times 10^{-6}}{56.83}} = 0.1188 \end{aligned} \tag{51}$$

and the maximum duty cycle at full load to obtain $V_{O1} = 32$ V

$$\begin{aligned} D_{max} &= M_{VDC1(max)}\sqrt{\frac{2f_sL_m}{R_{L1(min)}}} \\ &= 0.2262\sqrt{\frac{2 \times 85 \times 10^3 \times 534.7 \times 10^{-6}}{56.83}} = 0.286. \end{aligned} \tag{52}$$

The maximum duty cycle for which the diode D_{s1} is ON at full load is

$$\begin{aligned} D_{1max} &= \frac{1}{n_1}\sqrt{\frac{2f_sL_m}{R_{L1(min)}}} \\ &= \frac{1}{3}\sqrt{\frac{2 \times 85 \times 10^3 \times 534.7 \times 10^{-6}}{56.83}} = 0.4211 \end{aligned} \tag{53}$$

satisfying the condition $D_{max} + D_{1max} = 0.7071 < 1$.

4.2 Efficiency

The overall efficiency can be determined by considering the parasitic resistances of the components in the experimental set-up. The on-state resistance and the forward resistance of the MOSFET and diodes were $r_{DS} = 0.65\,\Omega$ and $R_F = 0.125\,\Omega$. The diode

forward voltages of the selected diodes were $V_{F1} = V_{F2} = 0.75$. The primary and secondary winding resistances measured at dc were $r_{Tp} = 150.8\,\text{m}\Omega$, $r_{Ts1} = 61.75\,\text{m}\Omega$, $r_{Ts2} = 36.42\,\text{m}\Omega$. In (21), $R_p = r_{Tp} + r_{DS} = 0.8008\,\Omega$, $R_{sk} = R_{s2} = r_{Ts1} + r_{Ts2} + R_{F1} + R_{F2} = 0.348\,\Omega$, $V_{Fk} = V_{F2} = 1.5\,\text{V}$. For the given specifications

$$\Delta i_{Lm(\max)} = \frac{V_{\text{Imax}} D_{\min}}{f_s L_m} = \frac{339.41 \times 0.131}{85 \times 10^3 \times 650 \times 10^{-6}} = 0.8041\ \text{A}. \quad (54)$$

Thus, the total power loss using (21) is (see (55)) The total maximum output power is $P_O = V_{O1} I_{O1(\max)} + V_{O2} I_{O2(\max)} = 25.51\ \text{W}$. Thus, the overall efficiency is

$$\eta = \frac{P_O}{P_O + P_{LS}} = 96.93\%. \quad (56)$$

4.3 Two-output transformer design

To verify the analysis given above, the following assumptions are considered:

(1) The effects due to fringing flux are negligible.
(2) The cross-regulation phenomenon present in the multiple-winding transformers is ignored.
(3) The leakage inductances of the transformer windings are treated as a part of the magnetising inductance.
(4) The MOSFET output capacitance and the diode junction capacitance are small enough and do not affect the switching waveforms.

Using the expression for skin depth of a conductor [9]

$$\delta_w = \sqrt{\frac{2\rho}{2\pi f \mu_r \mu_0}}, \quad (57)$$

where ρ is the resistivity of the conductor ($\rho = 1.724 \times 10^{-8}\,\Omega \cdot \text{m}$ for copper), f is the frequency of operation, μ_r is the relative permeability of the conductor ($\mu_r = 1$ for metals), and μ_0 is the absolute permeability of free space ($\mu_0 = 4\pi \times 10^{-7}\,\text{H/m}$) to yield $\delta_w = 66.2/\sqrt{f}$. Thus, the skin depth of copper at $f = f_s = 85\,\text{kHz}$ is

$$\delta_w = \frac{66.2}{\sqrt{f_s}} = \frac{66.2}{\sqrt{85 \times 10^3}} = 0.2270\ \text{mm} \quad (58)$$

resulting in the diameter for the primary winding wire as

$$d_{ip} = 2\delta_w = 2 \times 0.2270 = 0.4541\ \text{mm}. \quad (59)$$

The chosen copper wire is AWG25 with an inner diameter $d_{is} = 0.45466\,\text{mm}$. The maximum current through the primary winding is equal to the maximum inductor current ripple. Thus

$$I_{\text{pmax}} = \Delta i_{Lm(\max)} = \frac{V_{\text{Imax}} D_{\min}}{f_s L_m} = \frac{339.41 \times 0.118}{85 \times 10^3 \times 534.7 \times 10^{-6}} = 0.8812\ \text{A}. \quad (60)$$

To account for a safety margin, let $I_{\text{pmax}} = 1\,\text{A}$. The maximum energy stored in the magnetising inductance is

$$W_{Lm(\max)} = \frac{1}{2} L_m I_{\text{pmax}}^2 = \frac{534.7 \times 10^{-6} \times 1}{2} = 0.267\ \text{mJ}. \quad (61)$$

Assume the following core parameters: window utilisation factor $K_u = 0.25$, peak value of the magnetic field density $B_{pk} = 0.25\,\text{T}$, and current density $J_m = 4\,\text{A/mm}^2$. The core area product is [9]

$$A_p = \frac{4W_m}{K_u J_m B_{pk}} = \frac{4 \times 0.267 \times 10^{-3}}{0.25 \times 4 \times 10^6 \times 0.2} = 0.534\ \text{cm}^4. \quad (62)$$

A Magnetics® ferrite ETD gapped core OP-42929 is selected, which has [29–31]:

- Core area product $A_p = 0.73\ \text{cm}^4$.
- Core cross-sectional area $A_c = 76\ \text{mm}^2$.
- Mean magnetic path length $l_c = 72\,\text{mm}$.
- Relative permeability of the core material $\mu_{rc} = 2250 \pm 20\%$.

The minimum gap length required to avoid core saturation is (see (63)) Thus, the chosen length of the air gap, i.e. $l_g = 0.2\,\text{mm}$ suffices the requirements to avoid core saturation. The peak value of the magnetic flux density is

$$B_{pk} = \frac{\mu_0 \mu_{rc} N_p I_{\text{pmax}}}{l_c + \mu_{rc} l_g} = \frac{4\pi \times 10^{-7} \times 2250 \times 36 \times 1}{(72 \times 10^{-3}) + (2250 \times 0.2 \times 10^{-3})} = 194.99\ \text{mT}. \quad (64)$$

For the selected core material, the saturation flux density is $B_{sat} = 0.47\,\text{T}$ and $B_{pk} < B_{sat}$. Thus, the chosen air gap avoids core saturation. Fig. 4*a* shows an illustration of the three-winding transformer used in the flyback convertor with all the three windings wound on a bobbin placed over the gapped centre-post. It must be noted that multiple ways to arrange the different windings exist in literature and a simplest case, which lies within the capability of the simulation tool has been shown here.

The three-winding transformer was constructed on SABER® circuit simulator using the built-in Model Architect, which hosts the magnetic component tool. The properties of the selected core and windings were used in the simulations. Fig. 4*b* shows the proposed winding arrangement for the two-output flyback convertor used solely for simulation purposes. The primary winding has $N_p = 36$ turns, the secondary winding of the first output stage has $N_{s1} = 12$ turns, and the secondary winding of the

$$P_{LS} = 0.131 \times 0.8041^2 \times \frac{0.8008}{3} + \left(0.8041 \times 0.4647 \times \frac{0.8041 \times 0.348}{3} + \frac{1.5}{2}\right) = 806.2\ \text{mW}. \quad (55)$$

$$l_g > l_{g\min} = \frac{2\mu_0 W_m}{A_c B_s^2} - \frac{l_c}{\mu_{rc}} = \frac{2 \times 4 \times 10^{-7} \times 0.267 \times 10^{-3}}{76 \times 10^{-6} \times 0.25^2} - \frac{72 \times 10^{-3}}{2250} = 0.1412\ \text{mm}. \quad (63)$$

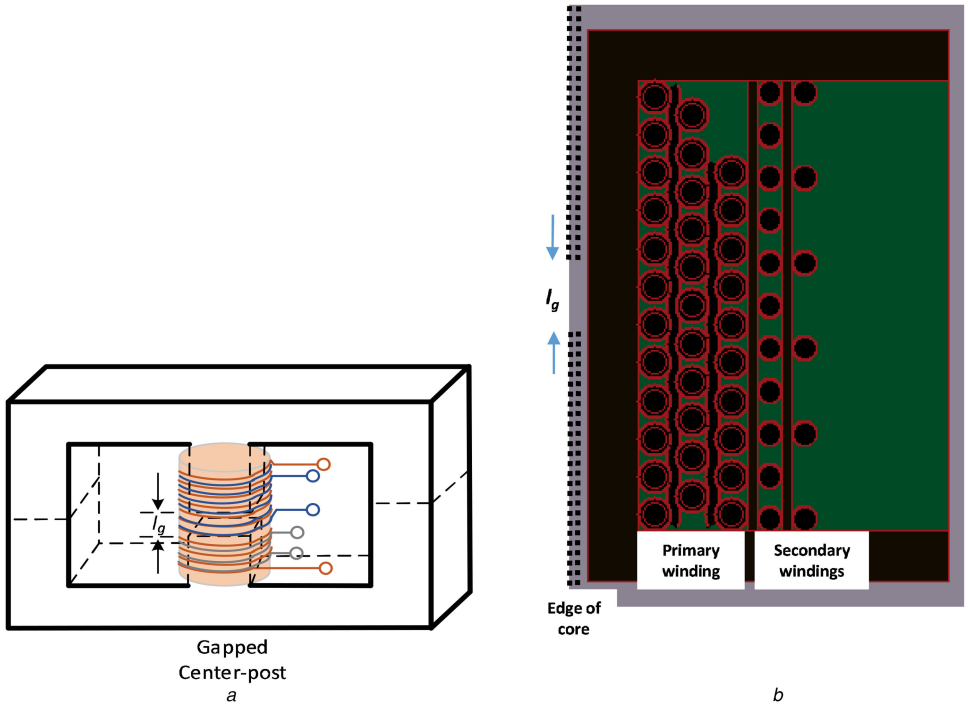


Fig. 4 *Representative core and winding arrangement and simulated winding arrangement*
(a) Representation of the core-winding structure with air gap l_g, ***(b)*** Simulated winding arrangement developed using the SABER Model Architect, where l_g is the air gap length

second output stage has $N_{s2} = 6$ turns to yield following values given in Table 1.

5 Results

The flyback convertor was designed using the proposed approach, simulated, built, and tested, whose results are presented in this section. Simulations were performed on SABER circuit simulator and the transformer built using the Model Architect tool as discussed in the previous section was implemented. The switching devices used were MTB6N6E n-channel power MOSFET as the main switch and MBR10100 silicon diodes as the secondary freewheeling diodes.

5.1 Simulation results

Fig. 5 shows the waveforms of the gate-to-source voltage v_{GS}, drain-to-source voltage v_{DS}, diode voltages v_{D1}, v_{D2}, current through magnetising inductance i_{Lm}, switch current i_S, diode currents i_{D1}, i_{D2}, output voltages v_{O1}, v_{O2}, and output powers p_{O1}, p_{O2} of the two-output flyback convertor operating in the DCM. The results obtained satisfy the desired specifications. The value of the magnetising inductance chosen ensures that the flyback convertor operated in the DCM, thereby validating the theoretical predictions.

The maximum value of the drain-to-source voltage V_{DSM} is governed by the input voltage and the reflected value of the maximum of the two output voltages. In this design, $V_{O1} > V_{O2}$ yielding

$$V_{DSM} = V_{Imax} + n_1 V_{O1} = 339.41 + (3 \times 31.25) = 433.2\,\text{V}. \quad (65)$$

The diodes D_{s1} and D_{s2} were observed as the lossy components in the circuits. In Fig. 5*b*, the sum of the currents through the MOSFET and the diodes is equal to the current through the magnetising inductance. When the power MOSFET turns-off, the energy stored in the transformer magnetising inductance is transferred to the secondary winding and diode conducts. The equivalent circuit at the transformer primary side of a real flyback converter is constituted by a series connection of a dc source, a voltage source of value equal to the output voltage as seen by the transformer primary side, the transformer leakage inductance, and the MOSFET output capacitance C_{oss}, which is not shorted any longer. The two last components, i.e. leakage inductance and C_{oss}. The current overshoot shown in Fig. 5*b* depends on this described phenomena. In this case, the resonance is not so evident and only a current overshoot is visible because the energy stored in the leakage inductance is low and resonance cannot be maintained. The dc output voltage of the first stage is nearly 31.2 V. The drop in voltage can be attributed to the losses in the real transformer. The total output power obtained from the simulation results was $P_O = P_{O1} + P_{O2} = 4.36 + 37.528 = 41.88\,\text{W}$. The average input power consumed was $P_I = 45.33\,\text{W}$. The overall efficiency of the convertor simulated at the maximum input voltage and full load was calculated as $\eta = 92.31\%$. The error between the simulated and theoretical data is 3.94%. The error could be attributed to the neglected core, switching, and capacitor losses in the theoretical estimation as well as the power consumed by the gate-driver circuit of the power MOSFET.

Table 1 Simulated and measured values of the components in the three-winding transformer

Component	Notation	Simulations	Measured
primary self-inductance	$L_p = L_m$	540 μH	645 μH
secondary 1 self-inductance	L_{s1}	60.57 μH	71.52 μH
secondary 2 self-inductance	L_{s2}	15.89 μH	21.90 μH
primary dc winding resistance	r_{Tp}	150.8 mΩ	176.2 mΩ
secondary 1 dc winding resistance	r_{Ts1}	61.75 mΩ	68.2 mΩ
secondary 2 dc winding resistance	r_{Ts2}	36.42 mΩ	32.5 mΩ

5.2 Experimental results

A practical circuit of the two-output flyback convertor was set up. Fig. 6*a* shows the photograph of the experimental circuit of the two-output flyback dc–dc convertor. Fig. 6*b* clearly shows the transformer core with a gapped centre-post. While the measured values of the three-winding transformer are given in Table 1, the other electronic circuitry used in the set-up are:

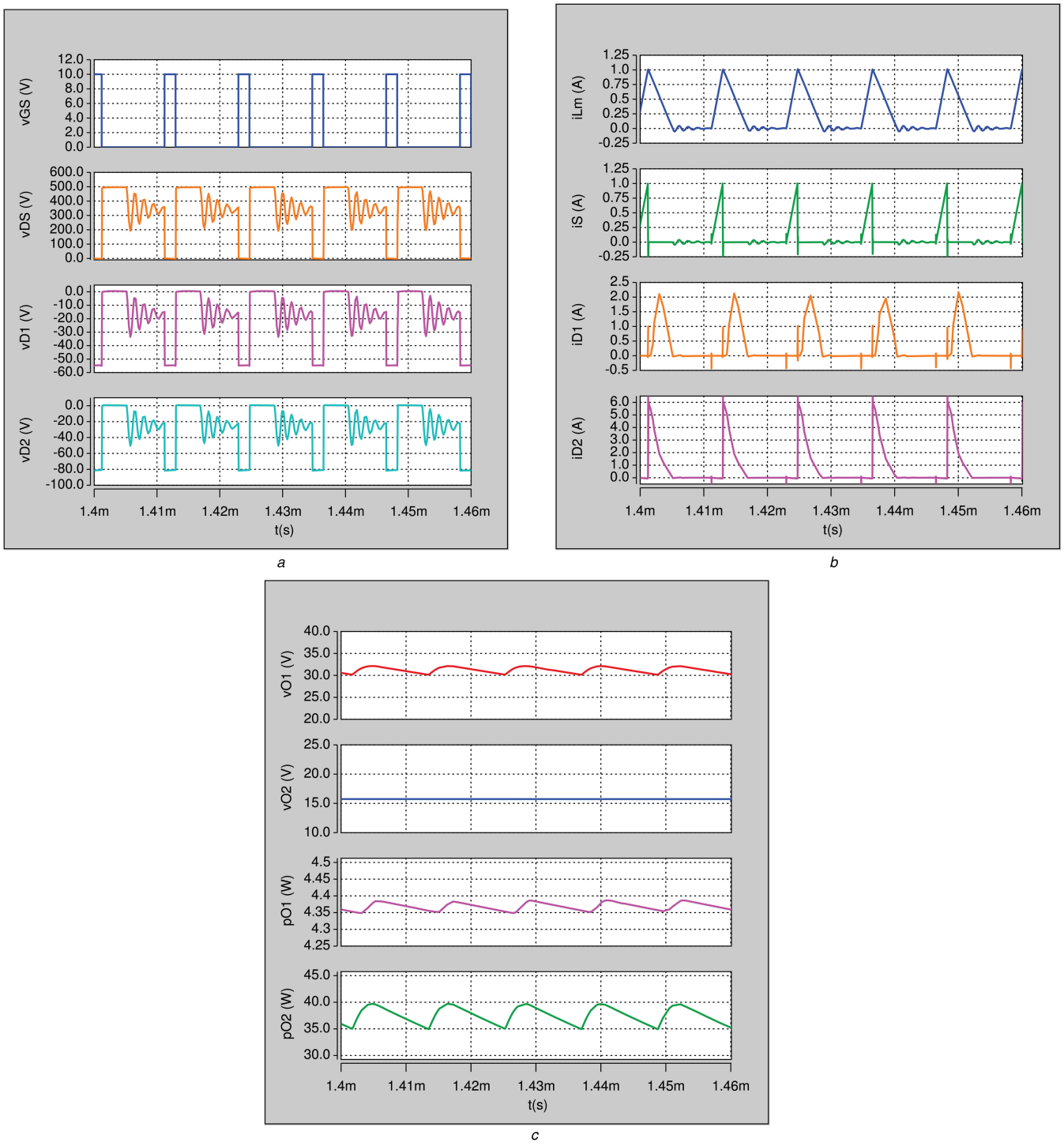
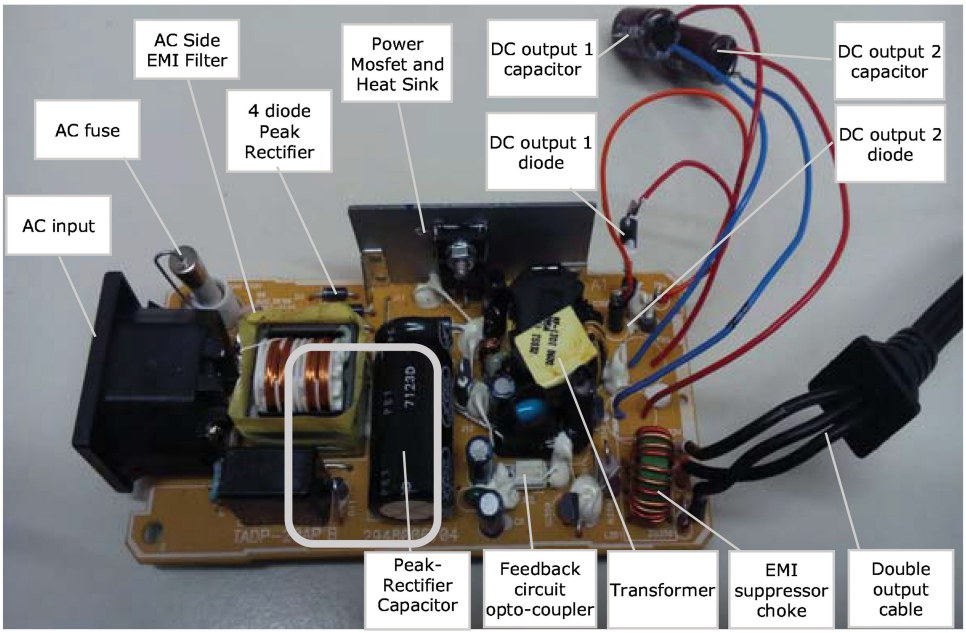


Fig. 5 *Simulated waveforms of selected voltages and currents of the two-output flyback convertor operating at DCM*

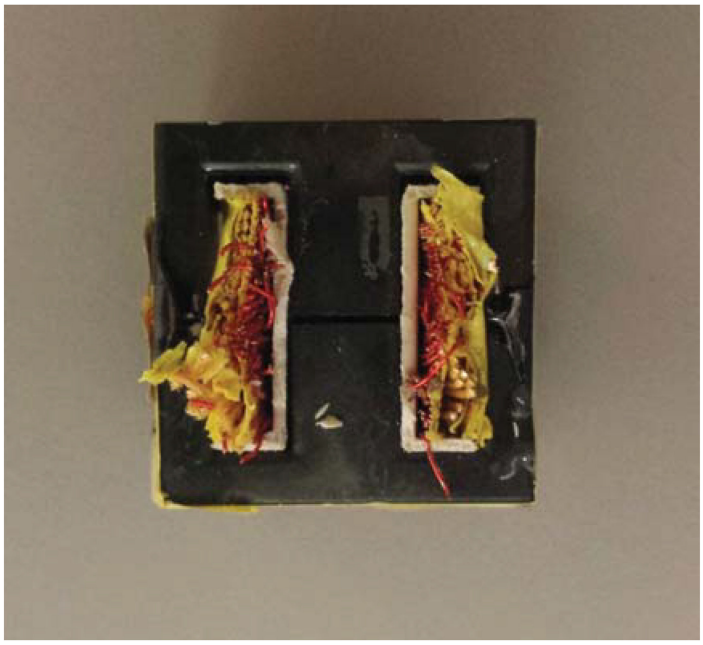
(a) Simulated waveforms of gate-to-source voltage v_{GS}, drain-to-source voltage v_{DS}, and diode voltages v_{D1}, v_{D2}, ***(b)*** Simulated waveforms of the magnetising inductance current i_L, switch current i_S, and diode currents i_{D1}, i_{D2}, ***(c)*** Simulated waveforms of the output voltages v_{O1}, v_{O2} and the output powers p_{O1}, p_{O2}

- STP10NK60ZFP n-channel power MOSFET with $V_{DSM} = 600\,V$, $r_{DS} = 0.65\,\Omega$, $I_{DM} = 10\,A$.
- STTH152 high-efficiency ultra-fast recovery diodes with $I_{F(av)} = 1.5\,A$, $V_{RRM} = 200\,V$, and $R_F = 0.125\,\Omega$.
- A $220\,\mu F$ electrolytic capacitor with $V_{max} = 50\,V$ and $r_C = 0.042\,\Omega$ for stage 1 with $V_O = 32\,V$.
- A $470\,\mu F$ electrolytic capacitor with $V_{max} = 25\,V$ and $r_C = 0.023\,\Omega$ for stage 2 with $V_O = 15\,V$.

The capacitors were estimated based on the design procedure given in [10]. The snubber circuits can be designed using the methodologies presented in [32–35]. An HP AC 0957-2119 power adapter based on a two-output flyback convertor was utilised during the experimental test. A Tektronix Digital Oscilloscope TDS224, 100 MHz 1 GS/s was used to acquire current and voltage waveforms. Current waveforms were acquired using a Tektronix P6021 ac current probe. The P6021 provides a 120 Hz to 60 MHz bandwidth and the passive termination is switchable from 2 to 10 mA/mV. Two rheostats were used to load the two convertors and their resistances were regulated according to the prescribed test conditions. The dc voltages and currents and resistance values were measured using a Keithley 2110 digital desk multimeter. In Fig. 6*a*, the wiring introduced in the experimental circuit during the tests to accommodate the Tektronix P6021 ac current probe is shown. This facility allows to acquire the data of the current flowing through



a



b

Fig. 6 *Photographs of the circuit and transformer*
(a) Picture of the experimental evaluation hardware, ***(b)*** Picture of the three-winding transformer used in the experiments

the two output diodes and the two electrolytic filter capacitors connected in parallel to the load.

The experiment was performed at a switching frequency $f_s = 85\,\text{kHz}$, the duty cycle $D_{\min} \simeq 0.12$, and the input voltage was set at $V_{\text{Imax}} = 340\,\text{V}$. The required load resistance for the first output stage was achieved using a rheostat, whose value was adjusted to get $56\,\Omega$. Similarly, the load resistance of the second output stage was set at $29\,\Omega$. Fig. 7 shows the experimentally obtained waveforms of selected voltages and currents of the two-output flyback convertor operating in the DCM. The duty cycle for which the diode current i_{Ds1} is ON was measured as $D_1 = 0.45$ and the theoretically predicted value calculated using (33) is 0.4211.

Fig. 7*a* shows the waveforms of the drain-to-source voltage and current through the primary winding. The maximum voltage stress V_{DSM} of the MOSFET was measured as 430 V. The peak value of the primary current I_{pmax} was recorded as 0.82 A. Fig. 7*b* shows the waveforms of the diode current and the diode voltage of the first output stage. The voltage stress V_{D1M} across the diode D_1 was measured to be 138 V and its average value was equal to the output voltage of the first stage. The peak diode current is $I_{D1M} = n_1 I_{\text{pmax}} = 2.46\,\text{A}$, which is validated experimentally. Fig. 7*c* shows the waveform of the capacitor voltage ripple of the first output stage. The maximum amplitude of the ripple was recorded as 146 mV and satisfies the design constraint $V_r/V_O \leq 1\%$. Fig. 7*d* shows the waveforms of the voltages across the two load resistances. The voltages across the two load resistance were measured as $V_{O1} = 31.8\,\text{V}$ and $V_{O2} = 15.4\,\text{V}$, respectively, and agree with the design specifications.

6 Conclusions

This paper has presented a derivation for magnetising inductance of the multiple-output flyback convertor in DCM. The expressions for both ideal and non-ideal flyback dc–dc convertors have been determined. The steady-state analysis of the multiple-output flyback converter in DCM has been performed. The work presented in this paper has made the following contributions:

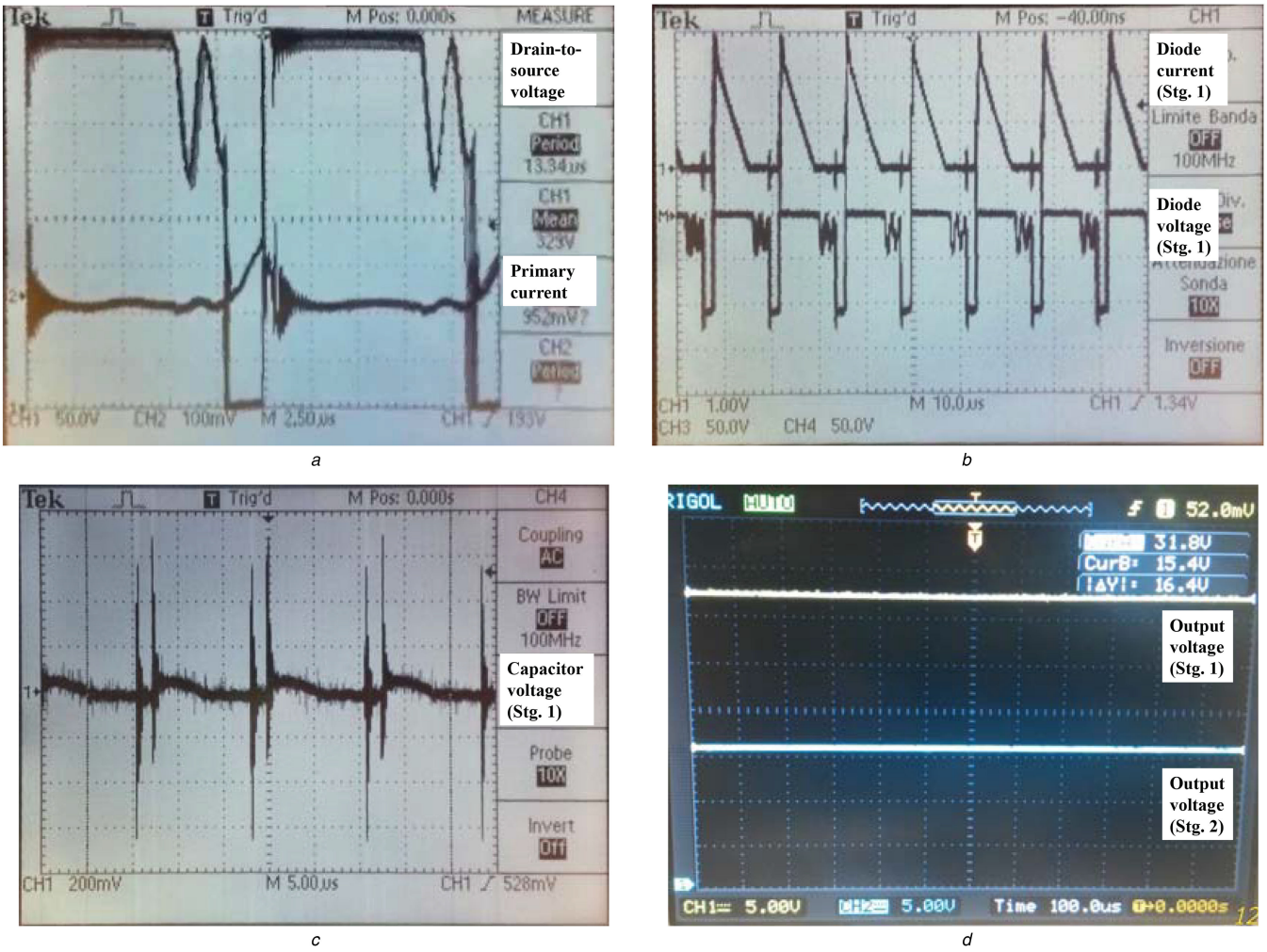


Fig. 7 *Experimentally obtained waveforms of selected voltages and currents of the two-output flyback convertor operating at the boundary at DCM*
(a) Measured drain-to-source voltage (scale 50 V/div) and primary current (scale 0.1 A/div) waveforms, ***(b)*** Measured diode voltage (scale 50 V/div) and diode current (scale 1 A/div) waveforms of the first output stage, ***(c)*** Measured capacitor voltage waveform for the first output stage (scale 2 V/div), ***(d)*** Measured output voltages across each load resistor (scale 5 V/div)

- A detailed theoretical framework to determine the maximum magnetising inductance of ideal and non-ideal multiple-output flyback convertor in DCM.
- A comprehensive steady-state analysis to determine the expressions for the (i) voltage transfer function, (ii) maximum inductor current ripple, (iii) maximum magnetising inductance, and (iv) overall power losses and efficiency in terms of the multiple-output stages.
- A step-by-step procedure to design, build, and test a multiple-output flyback convertor used as a universal power supply with two isolated output stages.

The flyback convertor used in the ac power adapter was designed to provide two unequal output voltages (15 and 32 V) and at a maximum output power of 20 W at both outputs. A design methodology for the three-winding transformer, which includes winding conductor selection, core selection, and coil-core arrangement has been presented. Finally, simulations and experimental results have been provided and the two results were found to be in good agreement. The simulated overall efficiency for the proposed design at maximum input voltage and at full load was found to be 91.3% and the theoretically predicted efficiency was 96.93%.

The following conclusions are made as a result of this analysis:

i. The maximum magnetising inductance for DCM operation depends on the load resistances of all the outputs and reduces with increase in the number of outputs and is provided in (16).
ii. The value of the maximum allowable magnetising inductance for DCM operation decreases with efficiency and is given in (20).
iii. The overall efficiency reduces as the number of output stages is increased and are described by (21)–(55).
iv. The duty cycle for the main switch is decided by the stage producing the maximum output voltage as given in (37).
v. The maximum voltage stress across the main switch (neglecting ringing) is

$$V_{\mathrm{DSM}} = V_{\mathrm{I}} + \max\left(n_1 V_{\mathrm{O1}}, n_2 V_{\mathrm{O2}}, \ldots n_n V_{\mathrm{On}}\right).$$

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