NEURAL RECEIVER FOR CPM SIGNALS

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ABSTRACT

Neural networks have been succesfully applied in many fields thanks to their learning and generalization capabilities and to the parallel processing and fault tolerance properties. Typical applications concern images processing, pattern recognition and digital signal processing, such as adaptive filtering and channel equalization. In this paper we propose the use of neural networks as digital receiver for continuous phase modulations (CPM). Simulation results refer to the European GSM digital cellular radio system. The neural receiver performance has been evaluated for a coherent detection, considering an additive white Gaussian noise (AWGN) channel and compared with a maximum likelihood sequences estimator (MLSE) receiver based on the Viterbi algorithm. The paper also presents a hardware implementation of the proposed network based on a digital signal processor (DSP) and on a programmable gate array (PGA).

1. INTRODUCTION

Continuous phase modulation schemes are tipically used in peak-power limited transmission systems, such as in digital satellite and radio-mobile communications. Their spectral efficiency makes CPM signals well suited to narrow bandwidth communication systems. On the other hand, because of the signal memory, CPM signals need complex receiver structure.

In this paper we propose the use of neural networks as digital receiver for CPM signals. Specifically the neural receiver, employing a multilayer perceptron structure (MLP), is aimed to the European GSM digital cellular radio system. In radio-mobile communications the transmitted signal arrives at the receiver passing through different transmission paths having different features. Each path can be delayed, time-dispersed, attenuated and distorted. A Doppler phase shift due to the mobility of the mobile station has also to be considered. The combined effect of these phenomena gives rise to a time-varying transmission channel, thus adaptive receivers are necessary. To compensate for the intersymbol interference (ISI) due to the channel memory, maximum likelihood demodulators based on the Viterbi algorithm and using matched filters are often employed [1], resulting in a complex receiver structure. Exploiting the neural networks generalization capability our purpose is to realize a self-adaptive receiver including channel and phase estimation tasks. Moreover thanks to the simple arithmetic operations carried out in parallel from several identical units constituting the network, it is possible to significantly reduce the receiver hardware complexity thus making easier the digital and analogue VLSI implementations. Furthermore the parallel distributed processing allows the use of large dimension structures keeping low the processing time and giving high representation capability and fault tolerance to the system. A hardware simulator of the proposed neural receiver has been developed so to get the receiver working in real time together with a GSM simulator and thus overcoming the delay introduced by computer simulations. This receiver prototype is based on a DSP and PGA devices. The PGA realizes a fast computation of the neurons constituting the network while the DSP can periodically updates the net weights.

In this paper we present the preliminary results of a larger research effort aimed to the realization of a neural receiver for the GSM system. The paper is organized as follow. In section 2 we briefly review the MLP theory. In section 3 we describe the neural receiver structure and present some simulation results concerning a received signal passed through an AWGN channel and perfectly recovered in time and phase. A performance comparison of the neural receiver with a MLSE receiver based on the Viterbi algorithm is also presented. The proposed hardware simulator is then presented in section 4. Finally section 5 is reserved for conclusions and aims for future research studies.

2. MULTILAYER PERCEPTRON

The use of neural networks as digital receiver can be justified viewing the demodulation problem as a more general statistical classification problem [2]. The neural network architecture considered is a feedforward neural net constituted by one or more layers of identical units, called neurons, each computing a non linear function (e.g. sigmoid) of the weighted sum of the unit inputs x_j.

$$y_i = f(\sum_j w_{ij} x_j) \tag{1}$$

$$f(h) = \frac{1 - e^{-h}}{1 + e^{-h}} \tag{2}$$

In the equation (1) w_{ij} denotes the weight connecting the jth node to the ith node of the next layer.

The neurons are connected together so that the output of each neuron in one layer feeds the inputs of the neurons in the next layer, but no connections exist between neurons in the same layer. This structure, known as multilayer perceptron (MLP) is one of the most popular neural networks thanks to the efficient supervised training algorithm, the backpropagation algorithm, used for weights updating [3]. The backpropagation rule consists

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in minimizing the error function E on the whole set of training patterns $\{x_p, d_p\}$ using a gradient-descent method, being d_p the desidered output for the pth presentation.

$$E = \sum_p E_p = \frac{1}{2} \sum_p \sum_i (d_{pi} - y_{pi})^2 \quad (3)$$

This method can be approximated updating the weight vector on-line rather than after the entire training set presentation. In this way we can significantly reduce the training time. The network weights are iteratively updated according to the following equation, being α the learning coefficient and μ the momentum term,

$$\Delta w_{ij}(n+1) = \alpha \delta_i y_j + \mu \Delta w_{ij}(n) \quad (4)$$

where

$$\Delta w_{ij}(n) = w_{ij}(n) - w_{ij}(n-1) \quad (5)$$

and

$$\delta_i = (d_i - y_i) f'(h_i) \quad (6)$$

for the neurons in the output layer,

$$\delta_i = f'(h_i) \sum_k \delta_k w_{ki} \quad (7)$$

for the neurons belonging to the hidden layers.

The network performance depends on the network size, the training set and from the reached solution in minimizing the error function. In fact, one of the major drawback of the backpropagation training rule is the possibility of running into local minima. Anyway it has been demonstrated that MPL can successfully applied to solve statistical classification problems since it approximates the Bayes optimal decision rule [4]. Furthermore simulation results confirm that the neural network based receiver gets very close performance to the MLSE receiver representing the optimal solution for an AWGN channel including ISI.

3. COMMUNICATION SYSTEM AND RECEIVER STRUCTURE

The transmission system features have been choosen according to the standard of the new pan-European digital mobile radio system, the ETSI/GSM. This system employes a time-division multiple access (TDMA) transmission with 8 slots per carrier. All the carriers are located in the f_0=900 MHz frequency band and are spaced by a 200 kHz bandwidth. The adopted modulation scheme is the GMSK signaling, with normalized bandwidth BT=0.3 and modulation index h=1/2. Before entering in the GMSK phase modulator the binary sequence is differentially encoded, in such a way that a linear model can be used for the transmitted signal [5]. The derotation technique, introducing a $\pi/2$ phase shift per symbol interval, allows to get a simplified representation of the received signal, which can be demodulated taking a finite lenght signal window into consideration [6]. Such a signal mantains a π phase uncertainty. The blocks scheme of the communication system enploying the neural receiver is depicted in Fig. 1.

3.1. Receiver structure

Because of the signal memory, the input vector to the MLP consists of the sampled baseband signal belonging to a window centered on the symbol interval to be demodulated. To choose the observation window length m (number of symbol intervals), it has to be considered the intersymbol interference due to the adopted partial response modulation and to the limited bandwidth of the receiver filter. According to the GSM recommendations a receiver filter with a 200 kHz bilateral bandwidth has been used to reduce the intersymbol interference between adjacent channels. Hence a sampling frequency equal to the bit rate (R=270.833 kbit/s) correctly represents the signal. The complex input signal is splitted in the in-phase (I) and quadrature (Q) components, so to get real inputs to the network. Instead of a real network, a complex-values MLP and a modified training algorithm could be used, as described in literature [7]. Using one sample per interval per quadrature components, 2m network inputs are required. The network dimension has been established after several trials, resulting in a 2-layer perceptron with one output neuron and 10 hidden neurons. We shall refer to a such network as a 2m-10-1 network. One output neuron is sufficent for binary sequences. A threshold criterion which associates 1 to positive outputs and 0 to negative outputs has been adopted as decision rule in demodulating the received signal. Because of the π phase ambiguity, the transmitted sequence or its complementary can be reconstructed by the receiver. This ambiguity can be eliminated if a piece of the transmitted sequence is known at the receiver (e.g. midamble). The simulation results reported below refer to a coherent demodulation being known the starting phase of the transmitted signal exactly recovered in time.

3.2. Simulation results

The proposed receiver requires a training phase, during which the network weights are evaluated so to minimize the output error as described in section 2. For the weights updating a binary random sequence has been used, being 0.5 the probability of each symbol and the corresponding noisy training patterns have been sequentially presented to the network inputs. The network weights have been randomly initialized between ± 0.1. After several trials the learning coefficient α and the momentum term μ have been respectivly set to 0.2 and 0.9. We let them decrease in time to closer approach the best solution. The network has been trained over 100 bursts (14800 bits) referring to the GSM system [8] althought it already converges after about 300 steps, as shown in Fig. 2.

The neural receiver performance has been evaluated for an AWGN channel in term of bit error-rate (BER) versus energy per bit over noise spectral power density E_b/N_0. The network has been tested over 1000 bursts. A 5 poles Chebychev receiver filter has been used. Since the GMSK modulation with BT=0.3 spreads the information above about 3 symbol intervals, m gets the minimum value of 3. Due to the additional ISI introduced from the receiver filter, larger m values have to be considered. The performance of a 2m-10-1 MLP with m=3,5,7,9 is depicted in Fig. 3. A comparison with a MLSE receiver using the Viterbi algorithm has also been made [8].

The following section proposes a hardware implementation of the neural receiver. As it can be seen from Fig. 3, it is not worth using m>5 because it would increase the structure complexity getting a negligible performance improvement. Thus a 10-10-1 network has been considered.

4. RECEIVER IMPLEMENTATION

The hardware implementation of the 10-10-1 structure, proposed as neural receiver, is based on the Texas Instruments TMS320C30 digital signal processor (DSP) and on the Xilinx programmable gate array (PGA) devices (XC3000 and XC4000 families). In this structure the PGA realizes a fast computation of the neurons while the DSP updates the net weights. The floating point arithmetic of the TMS320C30 and its parallel architecture are useful features to implement the backpropagation algorithm used to update the net weights. The sigmoid function of each neuron is implemented using a look-up table. The DSP needs around 1100 processor cycles to execute the backpropagation algorithm taking about 66 μs per iteration and thus allowing a maximum sample-rate of about 15 ksample/s. Using a gate array device it is easy to create parallel structures so to get a higher system throughput satisfying the requirements for satellite and radio mobile communications. Moreover the Xilinx's configurable logic blocks (CLBs) are well suited to the implementation of the simple arithmetic operations required from a neuron. The PGA use 5-bit coded weights and input data. The $<5,2>$ notation will be considered as a fixed point format using a two's complement five bits representation with two bits reserved to the integer part of the value (excluding the sign bit). Considering the 10-10-1 network, whose weights values at the end of the training phase range between about ± 3, the performance degradation is negligible when $<5,2>$-coded weights and inputs are used.

4.1. Neuron hardware architecture

The hardware architecture has to compute $h=\sum_i X_i W_i$, where X_i are the neuron inputs and W_i are the neuron weights. This is the basic neuron operation, thus only additions and multiplications between two $<5,2>$-coded numbers are required. The Xilinx's configurable logic blocks can easily implement logic functions, as adders or logic gates, thanks to the combinatorial logic (CL) within them. In addition each CLB contains two latches useful for the implementation of sequential functions. To get a high system throughput serial pipeline multipliers have been used so to get a result every (n+1) clock time intervals, where n is the number of bits used to code the absolute value of the input signal. The result is truncated to the (n+1) most significative (MS) bits [9]. We consider n=4. Figure 4.a shows the multiplication between two sign-magnitude (SM) five bit coded numbers, where $x_3x_2x_1x_0$, $w_3w_2w_1w_0$ represent the amplitude bits of the numbers. This structure is correctly working with positive numbers only, so the sign bit must be considered in a separate way. This problem is easy to solve XOR-ing the sign bits Sx, Sw of the two numbers to be multiplied to get the sign of the result. From a hardware point of view the two's complement (C2) representation is much more convenient of the SM representation if an adder has to be developed, since subtractions are considered in the same way of additions and therefore full-adders can be used. That is why the SM output of the pipeline multiplier is converted in a C2 format. The resulting structure, which we will refer as basic neural element (BNE), is shown in Fig. 4.b. The figure also shows the serial inclusion of the sign bit in the C2 multiplication result. For this sign-extension an additional bit equal to 0 has to be considered at the end of the input signal X. Hence, we get a complete C2 result after (n+2) clock intervals. If this structure is repeated N times, where N is the number of inputs to the neuron, and the N obtained outputs are added together, we get the desidered output h. Figure 5.a shows how the BNEs are arranged to get the neuron implementation. The look-up table implementation of the activation function f(h) is performed through the five C2 bits of the result used to address a 32-word table formed with two CLs of two different CLBs. The sign bit is used to address one of the two CLs. In so doing we get a five bits SM coded output, including the sign bit, that is used as input to the other neurons (see Fig. 5.b). The table has to be addressed once every 6 clock intervals.

4.2. CLB and memory requirements

About six CLBs per BNE are needed thus requiring 726 CLBs for the eleven neurons forming the 10-10-1 neural net. When the CLBs needed for the activation functions and for the two tapped delay lines (TDLs) are also taken into account, at least 863 CLBs are required for the entire network.

Using a XC4000 device, which provide an on-chip RAM, is possible to get an adaptive receiver thus allowing its use in a time-varying channel contest. A training phase on the DSP can be periodically started. At the end of the training phase the DSP stores the final weights values onto the on-chip RAM of the XC4000, so to code up the pre-trained MLP running on the PGA device. Hence, a 121 cells PGA RAM is required to store the weights values. The XC4020 device satisfies the foregoing requirements.

4.3. Computational time

Using the structure depicted in Fig. 5.b we get a net output result every 6 clock times. The maximum clock frequency which can be used working with the Xilinx's PGA devices is around Ftr/3, where Ftr is the specified PGA toggle-rate. Thus, considering a PGA having a 100 MHz toggle-rate, the maximum input sample-rate is about 5.5 Msample/s. The incoming data have therefore to be stored to allow the weights updating procedure on the DSP without interfering with the on-line PGA calculation. Thanks to the high sample rate achievable, the implemented network can process the input GSM data up to 20 samples per bit.

5. CONCLUSIONS AND FURTHER CONSIDERATIONS

In the first part of the paper a brief theoretical study and some simulation results demonstrating the possibility of using a multilayer perceptron as digital receiver for CPM signals, have been presented. Simulation results refer to the GSM environment. The performance of the neural receiver has shown to closely approximate that of the optimum MLSE receiver for a coherent detection in a contest of an AWGN channel. A hardware implementation of the 10-10-1 neural receiver, based on DSP and gate array devices, has been proposed in the second part of the paper. The high system throughput is perfectly suitable for GSM specifications. Moreover it can be used in a time-varying channel contest so as to implement adaptive training schemes. A more general evaluation board, based on Xilinx devices working in parallel, is currently being developed.

Future efforts are aimed to investigate the behaviour of larger dimension networks in demodulating multipath and Doppler affected signals, so to design a self-adaptive receiver able to operate in a time-varying contest without retraining. Different

architectures either including feedback connections or considering different activation functions are also worth of further studying.

REFERENCES

[1] J.G. Proakis, Digital Communication, McGraw-Hill.

[2] G. de Veciana and A. Akhor, "Neural net-based continuous phase modulation receivers", IEEE Trans. on Comm., Aug. 1992.

[3] D.E. Rumelhart, G.E. Hinton and R.J. Williams, "Learning internal representations by error propagation", Parallel Distributed Processing vol. 1, D.E. Rumelhart e J.L. McClelland, Eds. Cambridge, MA: M.I.T. Press 1986.

[4] D.W. Ruck, S.K. Rogers, M. Kabrisky, M.E. Oxley and B.W. Suter, "The Multilayer Perceptron as an approximation to a Bayes optimal discriminant function", IEEE Trans. on Neural Networks, Dec. 1990.

[5] P.A. Laurent, "Exact and approximate construction of digital phase modulation by superposition of amplitude modulated pulses (AMP)", IEEE Trans. on comm., Feb. 1986.

[6] A. Baier, "Derotation tecniques in receivers for MSK-type CPM signals", Proc. EUSIPCO-90, Vol. III, Barcelona, Spain, Sept. 18-21, 1990, pp. 1799-1802.

[7] M. Benvenuto and F. Piazza, "On the complex backpropagation algorithm", IEEE Trans. on Signal Processing, Apr. 1992.

[8] E. Del Re, G. Benelli, G. Castellini, R. Fantacci, L. Pierucci, L. Pogliani, "Design of a Digital MLSE receiver for mobile radio communications", IEEE Global Telecomm. Conf., Dec. 1991.

[9] L. B. Jackson, S. F. Kaiser, H. S. McDonald, "An approach to the implementation of digital filters", IEEE Trans. Audio and Electroacust., Vol. AU-16, pp. 413-421, September 1968.

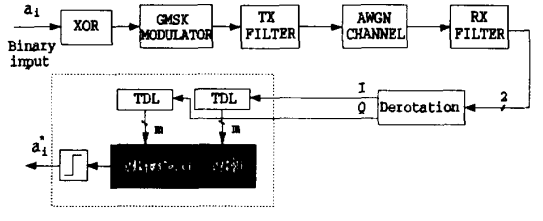

Fig. 1. Blocks scheme of the communication system employing the neural receiver.

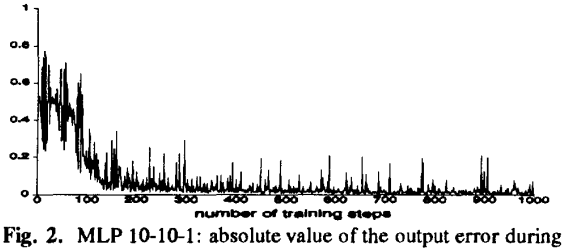

Fig. 2. MLP 10-10-1: absolute value of the output error during the training phase (E_b/N_0=8 dB).

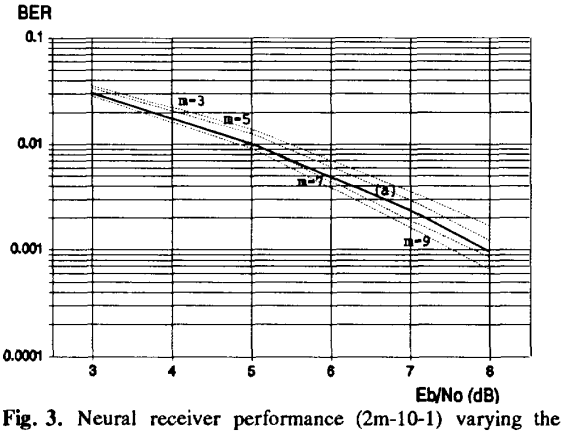

Fig. 3. Neural receiver performance (2m-10-1) varying the demodulation window lenght m; (a) MLSE receiver based on the Viterbi algorithm (m=5).

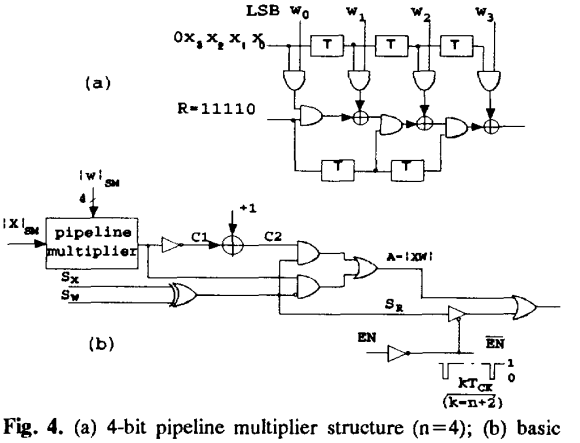

Fig. 4. (a) 4-bit pipeline multiplier structure (n=4); (b) basic neural element (BNE).

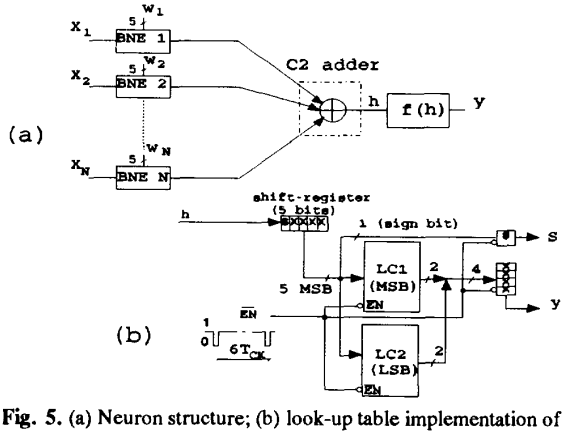

Fig. 5. (a) Neuron structure; (b) look-up table implementation of the neuron activation function.