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Power Loss Comparison of DC Side and AC Side Cascaded Modular Multilevel Inverters

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***Abstract*—High-voltage DC (HVDC) transmission systems based on voltage source converter technology are increasingly being used for interconnecting power networks and for transporting energy from remote renewable energy sources. Modular multilevel converters (MMCs) are emerging as the technology of choice for future HVDC transmission systems. Several MMC topologies have been introduced for high power applications and among them the AC side and the DC side cascaded topologies have received most interest because of their high efficiency, low switching losses and good modularity. In high power applications, the efficiency of the converter is an important consideration. Hence it is essential converter power loss analysis is addressed at design stage. Due to the high number of switches the various MMC topologies, the power loss calculations is particularly complex. This paper presents the analysis of the power losses in both DC side and AC side cascaded converters and compares their overall efficiency for a 500 MW power rating. The nominal values of efficiency quoted for an existing HVDC interconnector between Ireland and Wales are used to verify the methodology used for power loss calculations presented in this paper.**

Keywords—HVDC, Hybrid-MMC, Efficiency, Converter Power Loss

I. INTRODUCTION

Modular Multi-level inverters (MMC) are going to become more common because of the development of smart grids and multi-terminal HVDC networks [1]. The MMC has advantages over traditional two level voltage source converter which are: high efficiency, low harmonic distortion without the necessity of using filters, low switching frequency and good modularity to meet any voltage level requirements [2]. Among the different topologies that have been proposed for MMC, three main topologies have received much more interest: a hybrid multilevel converter with AC-side cascaded H-bridge cells, an alternative arm modular multilevel converter and a DC side cascaded multilevel with half bridge or full bridge cells connected across the DC link.

Additional details about the control and structure of AC side cascaded topology has been presented in [3]. This kind of topology has fault tolerant capability because H-bridge cells are used in the AC side of the two-level inverter. In addition, it has higher DC voltage utilization because of floating capacitors acting as a virtual DC link for each H-bridge cell to increase modulation index. The main drawback of this structure is the presence of some spikes in the output voltage which necessitates using of filters to attenuate the 5^{th} and 7^{th} harmonics.

From practical point of view, the DC side cascaded topology has been installed in a wide range of industry applications usually with half bridge or full bridge cell sub modules [4-6]. The main drawback of this topology is that there is no specific set point for voltage stress on switches. The other issue is that the hybrid multilevel converter with half bridge cells are unable to block DC side faults. Hence, using full bridge cells instead of half bridge cells could be considered as a solution. However, this practice will increase the initial investment cost as well as the switching losses. As a result, with a trade-off between cost and efficiency, the hybrid MMC consisting of half bridge and full bridge cells could be a promising solution [7]. In addition to DC side short circuit current blocking capability, this construction can also supply AC side during the fault [8].

In high power applications, efficiency of the converter is important issue so power loss analysis should be addressed at converter design. Due to a large number of switches, the power losses calculations are particularly complex in the MMC. The power loss issue is investigated in [9] and [10] but no details of the calculation process were reported and the junction temperature is not considered. There are several methods for the loss calculation in the MMC: calculation using adjustment of switching waveforms [11], calculation using the linear interpolation and semiconductor energy [12] and using real-time waveforms and temperature feedback [13]. A junction temperature feedback method is used in this paper in order to estimate the power losses more accurately. Based on the data provided by the manufacture, the characteristic of semiconductor device is acquired. The junction temperatures and power losses with different heat sink temperatures are also estimated by using the thermal circuit models.

This paper provides a comparative study on power losses and efficiency between two different topologies of MMC which are the AC side cascaded and DC side cascaded structures. The nominal values of efficiency quoted for an existing HVDC interconnector between Ireland and Wales are used to verify the methodology used for power loss calculations. The rest of this paper is organized as follows. Section II introduces circuit topologies of dc side cascaded and ac side cascaded MMC and their operational principle. In section III, the loss analysis and comparison between two topologies is presented and the conclusion remarks are introduced in section IV.

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II. TOPOLOGIES AND OPERATIONAL PRINCIPLE OF DC SIDE CASCADED AND AC SIDE CASCADED MMC

Circuit topologies and operational principle of dc side cascaded and ac side cascaded MMC are presented in this section. In DC side cascaded topology two arms form a converter phase, where the DC system is connected to the upper(p) and lower(n) sides of the phase and the three-phase AC system is connected to the middle point of each phase(a,b,c). Both arms comprise N series-connected identical sub-modules (SM).The AC and DC systems are usually modelled as voltage sources and the lines as inductors. The arm inductance (L), must be connected in series with each group of cells in order to limit the current due to instantaneous voltage differences of the arms. Fig .1 shows the structure of DC side cascaded MMC.

The simple and most common type of the DC side cascaded topology uses half-bridge sub module (HBSM). The HBSM inserts only one switch in series with the current path, for each ac voltage step and, therefore, the resultant MMC features low power losses. The main disadvantage of this sub module topology is that in the case of DC faults, the switches are disabled and the sub modules become short circuits, allowing the ac grid to feed the dc fault. So, in this case, HSBM sub module topology relies on the AC side breakers which can result in damage to converter station because of the long period of operation.

To address the aforementioned shortcoming, the full-bridge sub module (FBSM)-based configuration has been proposed. The FBSM has fault tolerant capability to eliminate the DC fault current by blocking the switching signals to the converter switches. Therefore, it isolates the AC and DC sides of the converter faster than an AC breaker. However, as compared to an HBSM-based MMC, an FBSM-based MMC has twice the number of series-connected switches in its current path and, consequently, features higher power losses.

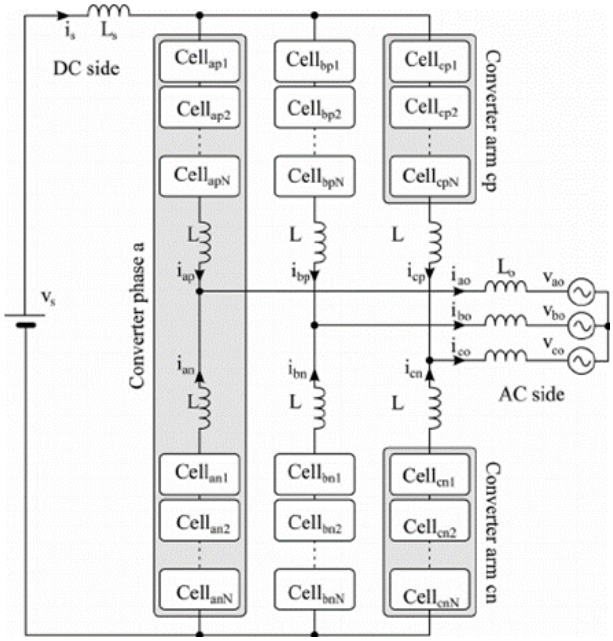

Fig .1 DC side cascaded topology [4]

Fig. 2 depicts the structure of the AC side cascaded topology with N cells per phase. It can generate 4N+1 voltage levels at each converter output phase relative to an imaginary supply mid-point, with predetermined voltage steps equal to one H-bridge capacitor voltage. The final modulation signal for the H-bridge cells will be the difference between the target fundamental voltage and the two-level converter output voltage (chopped square waveform) as shown in Fig. 2. Using selective harmonic elimination at the two-level converter stage will minimize the switching losses and the DC link voltage utilization will be increased [14]. The DC fault reverse-blocking capability of the proposed topology is achieved by blocking the gate signals to the converter switches, therefore no direct path exists between the AC and DC side through freewheel diodes, and cell capacitor voltages will oppose any current flow from one side to another. Consequently, with no current flows, there is no active and reactive power exchange between AC and DC side during DC-side faults. The H-bridge cells voltage balancing scheme is realized by rotating the H-bridge cell capacitors, taking into account the voltage magnitude of each cell capacitor and phase current polarity. So, operation of the hybrid multilevel VSC requires a voltage-balancing scheme that ensures that the voltages across the H-bridge cells are maintained at V_{DC}/N under all operating conditions, where V_{DC} is the total DC link voltage and N is the number of H-bridge cells.

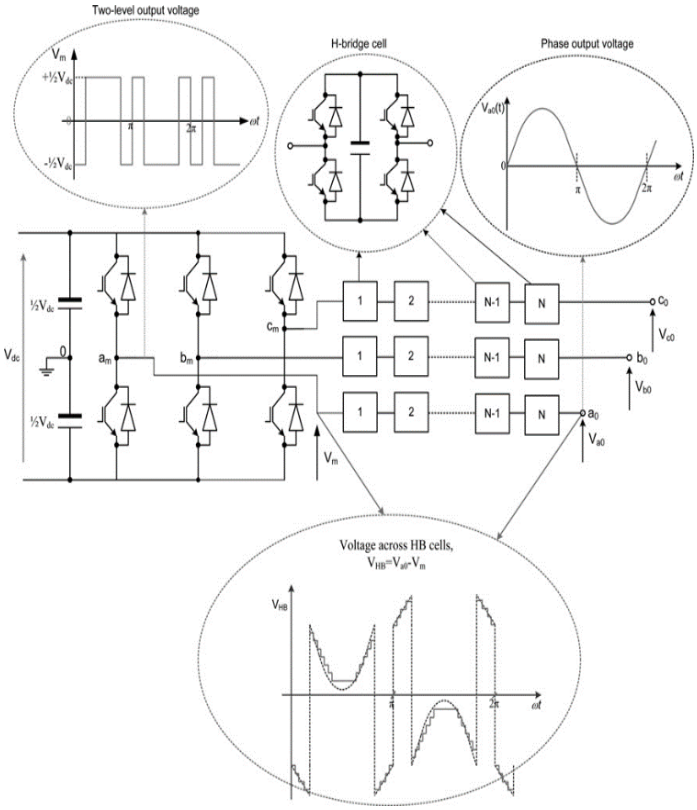

Fig .2 AC side cascaded topology [3]

III. COMPARISON OF THE LOSSES BETWEEN AC SIDE CASCADED AND DC SIDE CASCADED TOPOLOGIES

This section introduces loss and efficiency calculations for the half bridge DC side cascaded and AC side cascaded topologies at the same input DC voltage and the same AC load conditions. Several studies have investigated the efficiency of the DC side cascaded topology [15]. There are four different types of loss for any kind of power electronics device which are: 1) Conduction losses, 2) Switching losses, 3) OFF-state losses and 4) Gate losses [16]. The Off-state and Gate losses are very small and normally neglected. Hence, in this paper, only the conduction and switching losses have been considered for the analysis. Paper [17] presents the exact method for the inverter losses calculation. However, loss calculation for high power rates is challenging because of the number of series switches required to withstand nominal voltage and parallel switches to withstand the rated current. Computer simulation is one of the powerful methods to calculate and evaluate the losses in a MMC converter. In this case the accuracy of loss the calculations depends on how well the model constructed replicates the real system.

A. Conduction losses

The on state voltages drop in the device produces the conduction losses. These losses are computed by averaging the conduction losses in each switching cycle as shown in equation (1):

$$P_{cond} = \frac{1}{T}\int_0^T V_f(wt)i(wt)dwt \tag{1}$$

Where, P_{cond} shows the conduction losses of the device, $V_f(wt)$ shows the forward voltage drop of the device and $i(wt)$ represents the current flowing through the device during the conduction period. T is the switching period. The forward voltage drop is calculated by using the following equation:

$$V_f = V_{f_o} + r_f i(wt) \tag{2}$$

Where V_{f_o} and r_f show the forward voltage drop of the device at no load and the device forward resistance respectively. The device's data sheet provided by the manufacturer is used to calculate V_{f_o} and r_f.

Substituting equation (2) into equation (1), results in equation (3):

$$P_{cond} = V_f I_{av} + I_{rms}^2 r_f \tag{3}$$

I_{av} is the average current flowing through the device while I_{rms} is the root mean square value of the current flowing through the device. These values of the current are calculated by using equation (4) and (5) respectively.

$$I_{av} = \frac{1}{T}\int_0^t i(wt)d(wt) \tag{4}$$

$$I_{rms}^2 = \frac{1}{T}\int_0^t i^2(wt)d(wt) \tag{5}$$

B. Switching Losses

The combination of turning on losses and turning off losses results in the switching losses of the device. These losses depend on the device characteristics, switching frequency and the current, which is flowing through the device. The following relationship is used for the calculation of the switching losses of the device:

$$P_{sw} = \frac{f_s}{2\pi}\int_0^t ki(wt)dwt \tag{6}$$

Where P_{sw} are the device switching losses, k is constant and is obtained from the switching energy graph of the device which is given in the data sheet. f_s is the switching frequency of the device. The switching frequency has a direct impact on the switching losses. For the losses calculation, the current and voltage waveforms of the switching devices must be known.

This paper presents the analysis of the power losses in both DC side and AC side cascaded converters and compares their overall efficiency for a 500 MW power rating using a computer simulation based method. The nominal values of efficiency quoted for an existing HVDC interconnector between Ireland and Wales are used to verify the methodology used for power loss calculations presented in this paper. For East-West HVDC interconnector, the DC link voltage is 400 kV and output power is 500 MW. So considering a 9-level output voltage for the DC side cascaded topology, each arm will have 8 sub modules with 100kV DC voltage on each sub module. The design for AC side cascaded topology is different. However with considering 2 full-bridges that are cascaded on AC side of 2-level inverter, the DC link voltage for each full-bridge will be 100 kV [3].The datasheet of 3.3 kV, 450A Infineon switch is used to determine the converter devices characteristics. The coefficient of 1.15 has been considered to determine the withstand voltage for the converter switches. As example for 100 kV, 35 Infineon 3.3 kV switches should be series ($35\times3.3\cong115$). The number of parallel branches depends on the rated current of the system and the rated current of each switch.

The parameters for AC side and DC side cascaded topologies compared in this paper are given in Table I and Table II. The comparison has been done for the same input DC voltage and the same AC load conditions. In the AC side cascaded topology, the proper output voltage with acceptable THD necessitates 2 kHz switching frequency for level shifted carriers. Paper [3] introduces more details about the control and operation of the AC side cascaded topology

TABLE I. Simulation parameters for AC side cascaded topology

Parameter	Value	Parameter	Value
Number of SMs	2	***DC bus voltage***	400 kV
SM capacitance	9 mF	***SM capacitor voltage***	100 kV
Carrier frequency	2 kHz	***Output power per phsases***	$\frac{500}{3} MW$

For the DC side cascaded topology, phase shifted carrier pulse width modulation (PS-PWM) is considered as a superior method for control of sub modules because of its special features including even distribution of stress and power between SMs and low total harmonic distortion (THD) of output voltage[18]. More details and operation principles are presented in [7].

TABLE II. Simulation parameters for DC side cascaded topology

Parameter	Value	Parameter	Value
Number of SMs in each arm	8	***Carrier frequency of HBSMs***	550 Hz
Number of Half-Bridge SMs in each arm	8	***DC bus voltage***	400 kV
SM capacitance	6 mF	***SM capacitor voltage***	100 kV
Buffer inductor	0.5 mH	***Output power per phsases***	$\frac{500}{3} MW$

According to simulation parameters and choosing the 3.3 kV, 450 A Infineon switch, Fig. 3 depicts the conduction losses and switching losses for both topologies at the same output power (500/3MW). It can clearly be seen that the DC side cascaded topology has slightly higher overall losses than the AC side cascaded converter However, the difference is minimal. It should be recalled from Table I and Table II that the input DC voltage is the same for both topologies as well as output power. Table III shows the losses and efficiency calculations for both topologies. Hence, both converters are promising for HVDC applications.

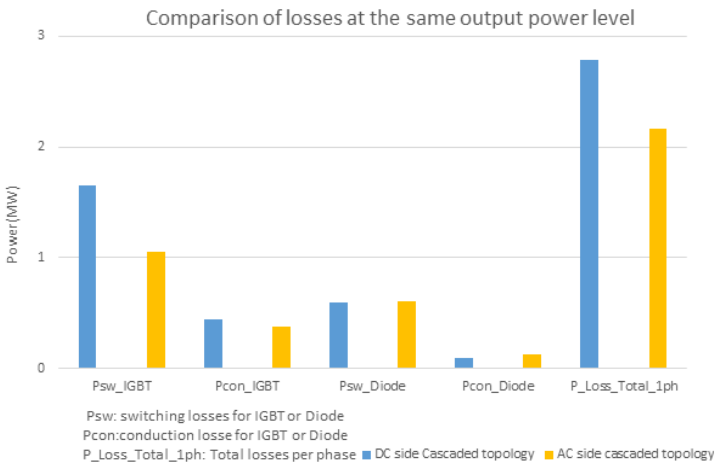

Fig. 3 Conduction losses and switching losses for both topologies

TABLE III. Power and efficiency calculations for ac side cascaded and dc side cascaded topologies

	Output_Power Per Phase	Total_Loss Per Phase	Efficiency
AC side Cascaded Topology	166.67 MW	2.13 MW	98.73%
DC side Cascaded Topology	166.67 MW	2.8 MW	98.34%

IV. CONCLUSION

Power losses are considered as a critical issue in converter design especially in high voltage applications. This paper presents a comparative study of the conduction losses and switching losses between two types of modular multi-level inverters which are AC side and DC side cascaded topologies. The loss analysis has been done for the same AC load condition and the same DC input voltage for both topologies. Results confirm that both topologies have the similar losses and efficiency. However, the AC side cascaded topology can be a proper choice for HVDC applications because of its lower capacitor size when more space is needed.

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