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Harmonic Power Compensation Capacity of Shunt APF and its Relationship to Design Parameters

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Abstract

In this paper, the equation for the reactive and harmonic power compensation of a shunt Active Power Filter (APF) system has been derived by studying the power exchange mechanism and power tetrahedron phasor diagram. The switching dynamics of a VSI based 3-phase, 3-wire (3-leg /Half-Bridge) Shunt APF system with hysteresis band current control has been studied and verified by simulation. The relation between the design parameters and their effects on the active losses have also been identified. Detailed calculation and extensive simulation have been performed for a 3-phase, 3-wire shunt APF implemented in a $400V_{L-L}$ distribution system, as an example, to study the effects of design parameter selection and their role in active power loss calculation. Simulated and calculated results are presented for the important design parameters for different switching frequencies together with their associated losses and kVA ratings. The procedure can be followed to design the parameters for other topologies, such as 3-phase, 4-wire or single-phase systems.

1. Introduction

Technological advancement in power generation from conventional and non-conventional sources, exploitation of renewable energy sources and their integration into supply networks and final utilization by highly sophisticated devices in the end users' equipment has increased the awareness of the quality and reliability/security of the power supply. Minimization of harmonic currents, generated due to harmonic voltages in the supply side and the non-linear loads in the end user side, is also one of the most important and dominating components for power quality improvement. Though the concept

of harmonic current elimination by the magnetic flux compensation in a transformer core was introduced by H Sasaki in 1971 [1], the Shunt APF (APF_{sh}) was first demonstrated by Gyugyi and Strycula in 1976 [2]. After that, rapid progress in the development of modern power electronic devices and state-of-art electronics circuit technology has led to a greater concentration on the improvement of the active power filter. This includes series or shunt compensation or both at the utility point of common coupling (PCC) to overcome voltage or current distortions or deviations. The main purpose of these configurations is to improve the power quality in the network so that the other consumers will not be affected by the voltage or current disturbances. Otherwise, poor power factor, together with reactive and harmonic power losses will lead to higher costs for consumers [3,4].

To date, more than hundred research papers on shunt APF have been published in international journals and presented at conferences. Most of the papers surveyed are based on a specific control mechanism. Very few of them deal with the basic design configuration to select the appropriate design components for single/three phase, three or four wire power distribution system. The design configuration of these filters depends on the type of converter, topology, number of phases, interfacing inductor, DC link capacitor and switching frequency. Further details of these classifications can be found in [5-7]. Detailed discussion on classification is beyond the scope of this study. Whatever the converter types, topologies or number of phases, there are some basic and most important components/parameters that are needed to be properly designed to compensate unbalanced and non-linear loads. These are;

i. DC link voltage
ii. DC storage capacitor
iii. Interfacing inductor
iv. Hysteresis band
v. Switching frequency of the inverter

A comprehensive study detailing the design procedure of an APF is not in place, where the critical design trade-offs can be analysed. The aim of this paper is to organize the overall design procedure for a VSI based APF system with hysteresis band current controller and to discuss the critical issues that should be taken into consideration while choosing the design components. As the switching mechanism plays a very important role in design/selection of the system parameters [8], the switching dynamics of the system have been analysed and studied here in detail. The switching frequency and the allowable maximum kVA rating also depend on the switching devices [7]. Hence the most popular IGBT has been chosen here as the switching device for application in the low voltage distribution level. Active power loss associated with the design parameters has also been analyzed as a rating requirement of the shunt APF unit. Therefore, based on the switching dynamics and power exchange mechanism, the relation among the different parameters such as switching frequency (f_{sw}), VSI output voltage (v_{sh}), voltage at PCC (v_{pcc}), DC capacitor voltage (V_{dc}), compensating current (i_{sh}), hysteresis band (h), interfacing inductor (L_{sh}) and their effect on total power loss of the filter (P_{loss}) have been identified. A wide number of simulation studies have been performed to choose the best value of hysteresis band and the DC link reference voltage (V_{dcref}). Again, as the hysteresis band is fixed, an APF_{sh} ($400V_{L\text{-}L}$) should have a maximum compensating capacity limit (with an appreciable high efficiency greater than 90%) within which it can operate to keep the THD_{Is} at a minimum.

This paper presents a step by step procedure of parameter selection for the design of an APF to compensate the harmonic current, generated by the load, with the following contributions;

- Equations of the compensating reactive and harmonic power calculation for the shunt APF have been derived through the working principle, power exchange mechanism and power tetrahedron phasor diagram of the APF
- Switching dynamics has been studied to determine the relations between the design parameters and switching frequency. Active power loss (due to the conduction and switching) has been associated with the design procedure for the selection of design parameters.

- Procedure for the derived equation, calculation of switching frequency and design parameters are generalized for single/three phase half/full-bridge system
- The best choice of hysteresis band and the minimum value of V_{dc} are determined based on the extensive simulation results which are important for the selection of other design parameters

The remainder of the paper has been organized as follows. The working principle, compensating power exchange mechanism and the power tetrahedron phasor diagram to derive the equations of reactive and harmonic power compensation for a 3-phase, 3-wire APF system is described in Section 2. The switching mechanism has been studied in Section 3 which has been further extended in Section 4 to derive the relation between the switching frequencies and design parameters. A design example of a shunt APF ($400V_{L\text{-}L}$) to achieve a maximum limit of compensating harmonic power and a wide range of selection parameters has been presented in Section 6. The step-by-step calculation procedure and the associated active loss limit of the compensator have also been described. As the switching frequency plays an important role in selecting the design parameters, a simulation study to verify the switching dynamics is presented in Section 7.

2. Working principle

Fig 1(a) shows a simple 3-phase 3-wire power system with APF_{sh}. The purpose of a APF_{sh} is to compensate the reactive and harmonic power of non-linear loads so that harmonics from the load current are not injected into the grid. Thus the THD_{Is} is minimized and the grid current is kept in phase with the grid voltage. To achieve this, the power transfer from the APF_{sh} to the PCC, as shown in Fig 1(b), is performed in a controlled manner so that $\theta_{pcci} = \theta_{pccv} = 0$.

Therefore, the injected current of the APF_{sh} can be written as;

$$\overline{I_{sh}} = \frac{V_{sh}\angle\theta_{shv} - V_{pcc}}{Z_{sh}\angle\theta_{shz}} \quad (1)$$

The voltage will be;

$$\overline{V_{sh}} = V_{pcc} + Z_{sh} I_{sh} \angle(\theta_{shz} + \theta_{shi}) \tag{2}$$

Injected power at the PCC can be obtained as;

$$S_{sh} = V_{pcc}\overline{I_{sh}^{*}} = \frac{V_{pcc}(V_{sh}\angle -\theta_{shv} - V_{pcc})}{Z_{sh}\angle -\theta_{shz}} = \frac{V_{pcc}V_{sh}}{Z_{sh}}\angle(\theta_{shz} - \theta_{shv}) - \frac{V_{pcc}^2}{Z_{sh}}(\angle\theta_{shz})$$

$$= \left\{\left(\frac{V_{pcc}V_{sh}}{Z_{sh}} cos(\theta_{shz} - \theta_{shv})\right) - \frac{V_{pcc}^2}{Z_{sh}} cos(\theta_{shz})\right\} + j\left\{\left(\frac{V_{pcc}V_{sh}}{Z_{sh}} sin(\theta_{shz} - \theta_{shv})\right) - \frac{V_{pcc}^2}{Z_{sh}} sin(\theta_{shz})\right\}$$

$$= \left\{\left(\frac{V_{pcc}V_{sh}}{Z_{sh}} cos\theta_{shv} - \frac{V_{pcc}^2}{Z_{sh}}\right) cos\theta_{shz} + \frac{V_{pcc}V_{sh}}{Z_{sh}} sin\theta_{shv} sin\theta_{shz}\right\}$$

$$+ j\left\{\left(\frac{V_{pcc}V_{sh}}{Z_{sh}} cos\theta_{shv} - \frac{V_{pcc}^2}{Z_{sh}}\right) sin\theta_{shz} - \frac{V_{pcc}V_{sh}}{Z_{sh}} sin\theta_{shv} cos\theta_{shz}\right\}$$

$$S_{sh} = \{A cos\theta_{shz} + B sin\theta_{shz}\} + j\{A sin\theta_{shz} - B cos\theta_{shz}\} \tag{3}$$

where, $\frac{V_{pcc}V_{sh}}{Z_{sh}} cos\theta_{shv} - \frac{V_{pcc}^2}{Z_{sh}} = A \; and \; \frac{V_{pcc}V_{sh}}{Z_{sh}} sin\theta_{shv} = B$

Subsequently, this transferred power can be divided into its fundamental and harmonic components. The components can be given as;

$$S_{sh} = P_{sh} + jQ_{sh} = \left(P_{shf} + P_{shH}\right) + j\left(Q_{shf} + Q_{shH}\right) = \sqrt{P_{shf}^2 + Q_{shf}^2 + H_{sh}^2} \tag{4}$$

where, $H_{sh} = \sqrt{P_{shH}^2 + Q_{shH}^2}$

This can be reflected in the power tetrahedron diagram [9], as shown in Fig 1(c). Therefore, from (3 and 4), putting the values of A and B, it can be written as;

$$\begin{cases} P_{shf} = \left(\frac{V_{pcc}V_{sh}}{Z_{sh}} cos\theta_{shv} - \frac{V_{pcc}^2}{Z_{sh}}\right) cos\theta_{shz} \\ Q_{shf} = \left(\frac{V_{pcc}V_{sh}}{Z_{sh}} cos\theta_{shv} - \frac{V_{pcc}^2}{Z_{sh}}\right) sin\theta_{shz} \\ H_{sh} = \frac{V_{pcc}V_{sh}}{Z_{sh}} sin\theta_{shv} \end{cases} \tag{5}$$

Now, as $\angle\theta_{shv}$ is very small ($sin\theta_{shv} = \theta_{shv};\ cos\theta_{shv} = 1$), then $\angle\theta_{shi}$ is approximately depends on $\angle\theta_{shz}$, i.e. the injecting/compensating current depends on the type of impedance. If Z_{sh} is inductive, then $\angle\theta_{shz} = 90^0$, therefore,

$$\begin{cases} P_{shf} = 0 \\ Q_{shf} = \frac{V_{pcc}V_{sh}}{Z_{sh}} - \frac{V_{pcc}^2}{Z_{sh}} = V_{pcc}I_{sh} \\ H_{sh} = \frac{V_{pcc}V_{sh}}{Z_{sh}}\theta_{shv} = V_{pcc}I_{sh} \end{cases} \quad (6)$$

This is the general equation (6) for the reactive and harmonic power compensation of a shunt APF system. It indicates that the active fundamental power (P_{shf}) transfer from the APF_{sh} to the PCC is zero. The compensating reactive and harmonic power can be controlled by varying the amplitude of V_{sh} and θ_{shv} (the phase difference between the voltage at VSI and PCC). From (6) it is also found that the APF_{sh} can compensate the reactive power only when $V_{sh} > V_{pcc}$. The maximum compensating capacity of the filter can also be found by solving $\frac{dQ_{shf}}{dV_{pcc}} = 0$. Therefore, the maximum reactive power compensation capacity of the 3-phase APF_{sh} will be;

$$Q_{shf-max} = 3\frac{V_{pcc-max}^2}{Z_{sh}} \quad (7)$$

and it occurs when $V_{sh} = 2V_{pcc}$ (8)

Similarly, the maximum harmonic compensation capacity of a 3-phase APF_{sh} can be obtained as;

$$H_{sh-max} = 3\frac{V_{pcc-max}V_{sh-max}}{Z_{sh}} \quad ; \text{while } sin\theta_{shv} = 1 \quad (9)$$

Therefore, (7) or (9) can be used to calculate the maximum reactive or harmonic compensation capacity of a 3-phase APF_{sh}.

The main VSI rating for the reactive and harmonic power compensation of the APF_{sh} can be written as;

$$\begin{cases} VSI_{rating-q} = S_{vsi-q} = \sqrt{{Q_{shf}}^2 + {P_{loss}}^2} \\ VSI_{rating-h} = S_{vsi-h} = \sqrt{{H_{sh}}^2 + {P_{loss}}^2} \end{cases} \quad (10)$$

where P_{loss} is the total active power loss of the APF_{sh} during its compensation task which includes conduction loss of interfacing inductor, transformer (if any), VSI and switching loss of VSI. The value of conduction and switching losses of VSI mainly depends on the DC voltage source of the switches, current flow and energy transfer during the on-off condition and the switching frequency [10]. If the overall impedance of the APF system is considered as $(j\omega L_{sh} + R_{sh})$, then the P_{loss} will be;

$$P_{loss} = 3I_{sh}^2 R_{sh} \quad (11)$$

where I_{sh} is the rms value of the compensating current, R_{sh} represents the conduction and switching losses per phase of the VSI and the isolation transformer (if any) [8].

For circuit simplicity and to describe the compensating power exchange mechanism between the APF_{sh} and grid PCC, a working diagram for phase A is shown in Fig 2(a), where S_w represents the switch of the switching devices. When $v_{sh} > v_{pcc}$, switch S_{w1} conducts and a leading current flows from the APF_{sh} to the PCC. In this case, the APF_{sh} operates in capacitive mode and a leading current is generated by the APF. Similarly, $v_{sh} < v_{pcc}$ results in a lagging current in the conducting switch S_{w4}. In that case, the APF operates in inductive mode. Both of the conditions can be represented as an Inverter and Rectifier mode of operation respectively if the VSI of the APF deals with active power exchange [11]. When $v_{sh} = v_{pcc}$, no current flow occurs between the APF and PCC and hence the power exchange becomes zero. According to Kirchhoff's voltage law, the basic equations for the capacitive and inductive mode can be derived as;

$$\begin{cases} v_{sh} - v_{pcc} - L_{sh}\frac{di_{sh}}{dt} - R_{sh}i_{sh} = 0 \; for \; capacitive \\ -v_{sh} - v_{pcc} - L_{sh}\frac{di_{sh}}{dt} - R_{sh}i_{sh} = 0 \; for \; inductive \end{cases} \quad (12)$$

3. Switching dynamics

Because of its simplicity of implementation, fast response, enhanced system stability and increased reliability [12, 13], a hysteresis band current controller is generally used to control the actual compensating current (i_{sh}) at the PCC by tracking the desired reference current. Fig 2(b) represents the switching dynamics for one phase of the APF_{sh}. It also shows how the compensating current (i_{sh}) tracks the reference current (i_{shref}) within the hysteresis band limit (h). For H-bridge single phase system, the detailed switching dynamics has been studied in [8]. Similar approach can be implemented here for single / three phase system and can be generalized with respect to V_{sh}.

The switching on and off time for S_{w1} or S_{w4} can be found from (12) and [8] as;

$$\begin{cases} Sw1_{on} = \frac{(2h+h_{on})L_{sh}}{v_{sh}-v_{pcc}-i_{sh}.R_{sh}} \\ Sw1_{off} = \frac{(2h-h_{off})L_{sh}}{v_{sh}+v_{pcc}+i_{sh}.R_{sh}} \end{cases} \quad (13)$$

where, $h_{on} = i_{shref2} - i_{shref1}$ and $h_{off} = i_{shref3} - i_{shref2}$

These (h_{on}, h_{off}) values are negligible for a smooth variation of reference current and it occurs when switching frequency is high or close to its maximum. During low/minimum switching frequencies the variation of reference current could be high and then it may be required to consider in case of minimum switching frequency calculation. The general equation for the switching frequency can be written as;

$$f_{sw} = \frac{1}{S1_{on}+S1_{off}} = \frac{1}{\left[\frac{(2h+h_{on})L_{sh}}{v_{sh}-v_{pcc}-i_{sh}.R_{sh}}\right] + \left[\frac{(2h-h_{off})L_{sh}}{v_{sh}+v_{pcc}+i_{sh}.R_{sh}}\right]} \quad (14)$$

4. Calculation of design parameters

The following section will discuss the procedure for harmonic current compensation. A similar procedure can be followed for reactive current compensation. As the $VSI_{rating-h}$ value is calculated from H_{sh} and P_{loss} of the APF_{sh}, (which depends on the V_{sh}, I_{sh}, L_{sh} and f_{sw}) to compensate specific

harmonics, the maximum limit of these values should be considered to determine the maximum acceptable P_{loss} as well as $VSI_{rating-h}$. Again, from the study of switching dynamics it is found that the switching frequency is very much dependent on the V_{pcc}, V_{sh}, i_{sh}, L_{sh} and h. Therefore, the proper value and selection procedure of these parameters are very important to determine the capacity of the APF_{sh} to perform its required tasks. Based on the working principle, power flow and switching dynamics study, the following steps describe the procedure and criteria for the selection of design parameters.

Switching frequencies (f_{sw})

Considering that h_{on} and h_{off} are negligible for smooth varying reference current and high frequency conditions, the switching frequency (14) can be simplified as;

$$f_{sw} = \frac{v_{sh}^2 - \left(v_{pcc} + i_{sh}.R_{sh}\right)^2}{4hL_{sh}.v_{sh}}$$

$$= \frac{v_{sh}}{4hL_{sh}}\left[1 - \left\{\frac{V_{pcc-max}}{v_{sh}}\left(\sin wt + \frac{i_{sh}R_{sh}}{V_{pcc-max}}\right)\right\}^2\right] \quad (15)$$

where, $v_{pcc} = V_{pcc-max}\sin wt$. The solution of this equation to derive the maximum (f_{swmax}), minimum (f_{swmin}) and zero-crossing (f_{swzero}) switching frequencies has been explained in [8] and can be found as;

$$f_{swmax} = \frac{v_{sh}}{4hL_{sh}} \quad (16)$$

$$f_{swzero} = f_{sw,max}\left[1 - \left(\frac{i_{sh}R_{sh}}{v_{sh}}\right)^2\right] \quad (17)$$

$$f_{swmin1} = f_{sw,max}\left[1 - \left\{\frac{V_{pcc-max}}{v_{sh}}\left(1 + \frac{i_{sh}R_{sh}}{V_{pcc-max}}\right)\right\}^2\right] \quad (18)$$

$$f_{swmin2} = f_{sw,max}\left[1 - \left\{\frac{V_{pcc-max}}{v_{sh}}\left(1 - \frac{i_{sh}R_{sh}}{V_{pcc-max}}\right)\right\}^2\right] \quad (19)$$

Over a complete cycle, the switching frequency (f_{sw}) and compensating current (i_{sh}) also vary. The maximum compensating current can be found where ($v_{sh} - v_{pcc}$) is maximum and this can be explained from (1) and Fig 2(a). That is, when v_{pcc} is near to 0 (zero), i_{sh} should be maximum. Therefore, it is clear that the maximum switching frequency, f_{swmax} should occur at or near the zero crossing condition (depending on the reactive and harmonic components of the load current). Also, at this point, h_{on} and h_{off} both are negligible compared to *2h*. Equation (16) should then be modified as;

$$f_{swmax} = \frac{v_{sh}(0)}{4hL_{sh}} \tag{20}$$

where $v_{sh}(0)$ represents the value of v_{sh} at or near the zero crossing condition. Similarly i_{sh} should be minimum where ($v_{sh} - v_{pcc}$) is minimum. Here, the switching frequency will also be minimum. At that condition, the values h_{on} and h_{off} should be comparable to *2h* and will have an effect on calculating the minimum switching frequency, f_{swmin}. Therefore, equations (18) and (19) may not give the accurate result and hence the general equation (15) should be used to calculate the other switching frequencies.

The relation between the V_{dc} and v_{sh} for single and three phase VSI can simply be obtained from [12], as shown in Fig 3. Therefore, (20) can be used to calculate the f_{swmax} for single or three phase system. Thus it can be written as;

$$f_{swmax} = \begin{cases} \frac{V_{dc}}{8hL_{sh}} \; for\; 1-phase, Half-Bridge\; (HB)\; system \\ \frac{V_{dc}}{4hL_{sh}} \; for\; 1\; or\; 3-phase, Full-Bridge\; (FB)\; system \\ \frac{V_{dc}}{12hL_{sh}} \; for\; 3-phase, Half-Bridge\; (HB)\; system \end{cases} \tag{21}$$

Interfacing inductor (L_{sh})

The derived methods in [14-17] for calculating the value of L_{sh} are mainly based on a fixed frequency PWM converter with an assumption that the ripple current attenuation or peak compensation current and the maximum harmonic voltage also are known. The value of L_{sh} can also be calculated from (6) where the value of H_{sh}, V_{sh} and I_{sh} should be pre-determined.

$$L_{sh} = \frac{V_{pcc}}{\omega H_{sh}} V_{sh} \quad (22)$$

In the case of a hysteresis band current controller, this value of L_{sh} can easily be calculated from (20), once the values of f_{swmax} and hysteresis band (h) are set. As the switching devices, typically, have a limit for the maximum switching frequency and therefore the value of L_{sh} also should have a minimum value which is acceptable for the compensating devices. It is found that the f_{swmax} of IGBT is around 20kHz. The minimum value of L_{sh} then should be;

$$L_{shmin} = \frac{v_{sh}(0)}{4hf_{swmax(IGBT)}} \quad (23)$$

Once the value of V_{sh} and f_{swmax} are fixed, the limit of L_{shmin} for a specified APF_{sh} can be determined by lowering the value of h within the acceptable range.

Hysteresis band (h)

From (16), it is clear that the selection of hysteresis band is very important for selecting the switching frequency and there should be a typical range of h to keep the THD_{Ipcc} within 5% as specified by IEEE. This can be found as;

$$h = k.I_{shmax} \quad (24)$$

where, $k = 0.05 \sim 0.15$. Although there are several advantages associated with hysteresis band controllers as mentioned earlier, the only disadvantage is the varying switching frequency with the system voltage. This can be overcome by fixing the switching frequency with a modified or variable hysteresis controller [18, 19] but then the complexity in the system control may increase.

DC link voltage (V_{dc})

The purposes of the DC link capacitor (C_{dc}) are - i) to maintain the V_{dc} with minimal ripple in steady-state, ii) to serve as an energy storage element to supply the reactive/harmonic power of the load and iii) to supply the real power difference between the load and source during the transient period. Therefore, the size of the C_{dc} should be selected, and the controller should be designed in such a way, that the APF_{sh} can compensate the real power difference for a short transient period (typically a

number of msec.) after which the controller should be able to adjust the reference current. Thus the V_{dc} can be maintained at a reference value.

Depending on the topology, different methods or approaches have been presented in [14–18] to develop the relation between V_{pcc}, V_{sh} and V_{dc}. For a 3-ph, 3-leg system, considering the amplitude modulation factor, m_a=1, the minimum value of V_{dc} should be at least equal to $2V_{pcc-max}$ [14], or $2\sqrt{2}.V_{sh}$ [15-17], or greater then $\sqrt{3}.V_{shmax}$ [18]. Based on this information, the minimum value of V_{dc} can be derived as;

$$V_{dc} > \sqrt{3}.V_{pcc-max} \tag{25}$$

Although the higher V_{dc} does not have much impact of THD_{Ipcc}, it can increase the THD_{Vpcc} and thus degrade the quality of the source voltage [20]. Therefore, lowering the difference between V_{pcc} and V_{sh} will improve the system performance and stability of the voltage at PCC.

DC link capacitor (C_{dc})

As an energy storage element, the DC link capacitor should be capable of performing all the functions described in the DC link voltage section. And in general, the energy handling capacity determines the size of the capacitor. The basic equation can be written as;

$$C_{dc} = \frac{2.S.n.T}{V_{dcmax}^2 - V_{dcmin}^2} = \frac{2.S.n.T}{\{(1+z)V_{dc}\}^2 - \{(1-z)V_{dc}\}^2} = \frac{S.n.T}{2.z.V_{dc}^2} \tag{26}$$

where S is the power required to be compensated during the steady state condition or the transient condition to fulfil the functions described in the DC link voltage section. *T* is the required time period for one complete cycle, *n* is the number of cycles for energy transfer and z is the percentage of V_{dc} to replace the V_{dcmax} and V_{dcmin}, the maximum and minimum allowable V_{dc} respectively to perform the specific task. For a specific system, it is better to consider the higher value of C_{dc} so that it can handle all of the above conditions. It also helps to get a better transient response and lower the steady-state ripple.

5. Selection of design parameters for a 3-ph, 3-wire APF_{sh}

This section deals with some simulation study and calculation for the proper selection of design parameters. As an example, the initial target of maximum harmonic compensating current, I_{shmax}, has been set at 100A which requires an APF_{sh} of 48.8 kVA rated capacity (H_{sh}) in a $400V_{(L-L)}$ distribution system. Again the rating of the VSI, S_{vsi-h} of the compensator depends on the H_{sh} and P_{loss} which are associated with the V_{sh}, I_{sh} and R_{sh} in (6) and (11). These are also related to the rating of the switching device and other design parameters including f_{sw}, h and V_{dc}, in (17 - 25). Therefore a wide range of values of these parameters has been chosen to calculate the P_{loss} and S_{vsi-h} and to perform the simulation study to observe the performance of the selected appropriate design components. The connection topology and switching configuration of a 3-ph, 3-wire APF_{sh} together with the chosen parameters range is shown in Fig 4(a).

Fig 4(b) shows how the actual VSI rating (S_{vsi-h}) increases with the value of R_{sh} for a specific I_{shmax}. The actual compensating power of the APF_{sh}, H_{sh} can be calculated from (6) and in the Fig 7(a) it is represented when R_{sh} is zero. Though R_{sh} is related with the design parameters, in some research articles the value of R_{sh} was considered to be between 0 and 2Ω [16, 21 - 27]. For example, to compensate 48.8 kVA of H_{load}, the required S_{vsi-h} will be 49.0 kVA, if a value of 0.3 Ω for R_{sh} is used as shown in Fig 4(b) (point A). The VSI rating will be increased upto 57.7 kVA, if R_{sh} is assumed to be 2Ω. This is shown as point B in Fig 4(b).

The corresponding active power loss P_{loss} as a ratio (%) of (P_{loss} / S_{vsi-h}) for the unit is shown in Fig 4(c). For R_{sh} = 0.3Ω, the actual P_{loss} is 4.5 kW, calculated from (11). In terms of ratio it is around 9.2% of the VSI rating which is reflected as point A in Fig 4(c). Point B in Fig 4(c) shows the corresponding ratio for the point B in Fig 4(c), which is around 52%. Therefore it would be better to lower the R_{sh} value. Considering the ratio of 10% as a loss, it can be calculated that a value of R_{sh} up to 0.4 Ω would be an acceptable selection for a 49kVA (I_{shmax} = 100A) compensator. The shaded part of the Fig 4(c) also reflects the possible limits of I_{shmax} for possible R_{sh} values that can be considered between 10% ratio and 1Ω.

Again from the switching dynamics study (14-16), it is found that the f_{sw} depends on the system parameters such as V_{sh} or V_{dc}, h, L_{sh}, V_{pcc}, I_{sh} and R_{sh}. Practically, the maximum switching frequency, f_{swmax} depends on the type of power switching devices. Generally, IGBT switches are preferred in most of the power electronics devices at distribution level due to their fast switching speed, low switching power losses and high power handling capability. With these above stated constraints, the initial limit for some of the parameters was fixed to design a shunt APF which has been given in Table 1. The remainder of the component selection has been carried out based on these parameters.

Table 1- Initial maximum limit for some of the design parameters

Parameters	Value (Initial Maximum Limit)
H_{load}	49kVA
$V_{pcc\ (L-L)}$	400V
I_{shmax}	100A
f_{swmax}	20kHz
R_{sh}	1Ω
P_{loss}	10%

A series of simulation studies and other calculations have been performed based on the design procedure, as shown in Fig 8, to select the best values of h and V_{dc} which are further required to set the value of L_{sh} and to determine the limit of I_{sh} and H_{sh} and S_{vsi-h} to operate the APF_{sh} within its loss limit or with maximum efficiency. Critical design decisions are then verified against the derived procedure in the previous section and described in the following section.

Selection of hysteresis band, h

Within the f_{swmax} and P_{loss} limit, some simulation studies have been performed for different values of compensating current (I_{sh}), interfacing inductor (L_{sh}), ratio of V_{dc}/V_{pccmax} (m) and hysteresis band (h) to select the appropriate band limit and to obtain the best THD_{Is} or THD_{Ipcc} within the IEEE standard limit. Fig 5(a) shows the result of these simulation studies in terms of THD_{Is} (%) vs h (% of I_{shmax}) which reflects the limits of h that has been considered in (24). It is found that for a precise calculation and to obtain the best performance of a APF_{sh}, h should be selected as between 5% to 10 % of I_{shmax}.

Limit on the I_{shmax}

The relation between f_{swmax} and I_{shmax} can be derived, from (21) and (24), as follow;

$$f_{swmax} = \frac{V_{dc}}{12kI_{shmax}L_{sh}} \quad (27)$$

It shows that for a constant value of I_{shmax}, the maximum switching frequency, f_{swmax}, increases with the decrease of L_{sh}. Again the size limit of L_{sh} can be increased with the increase of *m* (V_{dc}/V_{pccmax}) and I_{shmax}.

For a fixed value of L_{sh} and f_{swmax}, the limit of I_{shmax} can also be increased by reducing *h*. Fig 5(b) shows how the switching frequency increases with the decrease of L_{sh} and increase of *m*. For I_{shmax} = 10A, a minimum 2mH of L_{sh} should be used with *h* = 10% of I_{shmax} and *m* = 1.4 to keep the f_{swmax} within the IGBT switching limit (20kHz), shown in point A. Within this 20kHz, the limit of I_{shmax} can also be increased up to 40A (as shown in the shaded part of Fig 5(b) by reducing the L_{sh} to 1mH, at point B) or up to 200A (at point C, as shown in the shaded part of Fig 5(c) by reducing the L_{sh} to 0.5mH, *h* = 5% and increasing m to 3.6). But in these cases (B and C), there will be a high level of power loss in the VSI unit and the voltage *THD* at PCC will also increase due to the higher V_{dc} (high *m*) [20]. Therefore, after fixing f_{swmax} (20kHz) and *h* (10%), the I_{shmax} has been calculated for different L_{sh} and *m* values which are given in Table 2.

Table 2 - Values of I_{shmax} and L_{sh} for different V_{dc} condition at f_{swmax} = 20kHz

f_{sw} = 20K	*m*							
h =10%	1.6	1.8	2	2.4	2.8	3.2	3.6	4
L_{sh} (mH)	I_{shmax}							
0.1	216.8	244.0	271.1	325.3	379.5	433.7	487.9	542.1
0.5	43.4	48.8	54.2	65.1	75.9	86.7	97.6	108.4
1	21.7	24.4	27.1	32.5	37.9	43.4	48.8	54.2
2	10.8	12.2	13.6	16.3	19.0	21.7	24.4	27.1
4	5.4	6.1	6.8	8.1	9.5	10.8	12.2	13.6
6	3.6	4.1	4.5	5.4	6.3	7.2	8.1	9.0
8	2.7	3.0	3.4	4.1	4.7	5.4	6.1	6.8
10	2.2	2.4	2.7	3.3	3.8	4.3	4.9	5.4
12	1.8	2.0	2.3	2.7	3.2	3.6	4.1	4.5

Selection of V_{dc}

A number of simulation studies were performed for various values of I_{shmax}, f_{swmax}, h and L_{sh} to observe the THD_{Is} with respect to V_{dc}. It is found from Fig 6(a and b) that the *m* value should be at least 1.7 (V_{dcmin} = 1.7V_{pccmax}) to obtain a THD_{Is} within the IEEE limit, as shown in the shaded area. This also validates the relation between V_{dc} and V_{pccmax} as given in (25). For higher V_{dc}, THD_{Is} is also found to be within the limit, shown in Fig 6(c) but it then can degrade the quality of voltage at the PCC. Therefore it is preferable to consider the value of *m* close to its lower limit. It will also help to reduce the value of R_{sh} by reducing the L_{sh}.

Fig 7(a) shows how the P_{loss} increases (point A, B and C) with the decrease of f_{swmax} while other parameters are fixed. This also shows the loss increases with the increase of *m*. Therefore it is better to chose a lower value of *m*. Corresponding design parameter values for the points A, B and C are also given in Table 3.

Once the values of *m*, f_{swmax} and h are fixed, I_{shmax} can be calculated for different L_{sh}. Lower the value of L_{sh} will help to reduce the R_{sh}. The value of R_{sh} is set from Fig 4(b,c) for a fixed value of S_{vsi-h} and P_{loss} within the limit. It is difficult to calculate the switching loss. Therefore, the resistance value (act as a loss emulator) should be low, as it is responsible for conduction loss (transformer + inductor). Table 4 shows the possible limit of compensating current (I_{shmax}) and harmonic power (H_{shmax}) for the corresponding L_{sh} while f_{swmax} = 20kHz, $m = 2.0$; $h = 10\%$. The ratio of active power loss (P_{loss}) to the rating of the VSI (S_{vsi-h}) for different values of $R_{sh}$are also shown in the table which helps to select the appropriate parameters for the design of the shunt APF compensator. As an example, (while f_{swmax} = 20kHz, $m = 2.0$; $h = 10\%$), a 0.5mH of interfacing inductor (L_{sh}) can be used to compensate upto 90A of I_{shmax} for which the required capacity of the APF (H_{sh}) is 44 kVA. But then the rating of the VSI and the active power loss depend on the R_{sh}. To keep the loss within 10%, the value of R_{sh} should not be more than 0.4Ω.

Selection of C_{dc}

From the general equation (26) it is found that the value of C_{dc} depends on the purposes of the DC link capacitor, the required level of power (S) to be compensated/transferred, the number of cycles (n) and the allowable change of V_{dc} (z). Once the value of V_{dc} (or m) and the number n are fixed, C_{dc} only depends on S and z. Fig 7(b) shows the relation between z and S with respect to C_{dc}. For example, if a compensator is allowed to transfer 20kVA of load power during the transient condition and the task is completed within a half cycle (n = 0.5) with an allowable change in V_{dc} of 10%, then the required capacity of C_{dc} will be around 3000µF for m = 1.8, point A, which is further reduced to 2500µF for m = 2.

Table 3 - Parameter values corresponding to the points shown in Fig 12

$R_{sh} = 1\Omega; m = 2.0;\ L_{sh} = 2mH; h = 10\%$			$\frac{P_{loss}}{S_{vsi-h}}$ (%)
Point	$f_{sw}\ (kHz)$	$I_{shmax}\ (A)$	
A	20	14	4
B	16	17	5
C	12	23	7

Table 4 - Possible limit of I_{shmax} , H_{shmax} and L_{sh} with the $\frac{P_{loss}}{S_{vsi-h}}$ (%) for different values of R_{sh}

$f_{sw} = 20\ kHz;\ m = 2.0;\ h = 10\%$			$R_{sh}\ (\Omega)$					
			1.0	0.8	0.6	0.4	0.2	0.1
L_{sh} (mH)	I_{shmax} (A)	H_{sh} (kVA)	$\frac{P_{loss}}{S_{vsi-h}}$ (%)					
0.1	451	220	58.1	46.5	34.9	23.2	11.6	5.8
0.5	90	44	21.7	17.4	13.0	8.7	4.3	2.2
1	45	22	12.2	9.7	7.3	4.9	2.4	1.2
2	23	11	6.5	5.2	3.9	2.6	1.3	0.6
4	11	6	3.4	2.7	2.0	1.3	0.7	0.3
6	8	4	2.3	1.8	1.4	0.9	0.5	0.2
8	6	3	1.7	1.4	1.0	0.7	0.3	0.2
10	5	2	1.4	1.1	0.8	0.5	0.3	0.1

6. Verification of switching dynamics and frequencies

As discussed, the design parameters of the APF_{sh} are related to the switching frequency, f_{sw} as well as the hysteresis band, h and V_{dc}. The switching mechanism has been studied and verified with the derived equations in the previous Section. Table 5 shows the design parameters for a specific compensator that has been chosen to investigate the switching dynamics and to determine the

switching frequency. Fig 8(a) shows the V_{pcc}, V_{sh}, I_s, I_{sh}, I_{load} and S_{w1} for phase A when the shunt APF_{sh} is operating. It is clear that the f_{swmax} occurs near the zero crossing condition where V_{pcc} is close to zero and V_{sh} is 1/3 of V_{dc}. The variation of I_{shref} during one on-and-off time period (h_{on} and h_{off}) of gate S_{w1} is also negligible compared to *2h* (in Fig 2). Otherwise, the effect of these values on the calculation of f_{swmax} is negligible. Fig 8(b) shows that the system has been designed for f_{swmax} = 15kHz which can simply be calculated using (16) and by neglecting h_{on} and h_{off}. If the values are compared with that in (20), f_{swmax} is found to be the same.

Similarly f_{swmin1} occurs where I_{sh} is close to zero, shown in Fig 8(c). At this point, V_{pcc} goes to its positive peak and V_{sh} = 2/3 of V_{dc}. h_{oh} can be calculated as 0.77A and h_{off} is 0.64 (from 13). Putting these values in (16), the f_{swmin1} is calculated as 10.7kHz whereas neglecting the values of h_{on} and h_{off} in the calculation gives a value of 12.1kHz. This makes a significant difference in the actual simulated f_{swmin} condition, though it does not have any impact on selection the design parameters.

Table 5 - Design parameters of a Shunt APF for the verification study of switching frequencies

Component Parameters	Values
Supply Voltage	230 Vrms, 50 Hz
DC link Voltage	600 V
DC storage Capacitor	2200 µF
Interface Inductor	1.666 mH, 1Ω
Hysteresis band (h)	2 Amp
Maximum Compensating Shunt Current	30 Amp

7. Conclusion

Equations for reactive and harmonic power compensation have been derived for a shunt APF system by analyzing the power exchange mechanism and power tetrahedron phasor diagram. Switching dynamics has been studied to develop the relation between the design parameters and the switching frequencies. This is also verified by simulation. Active power loss is also co-related with the selection of design parameters and maximum switching frequency. A design parameter selection procedure with an example has been described here by initially setting a maximum switching frequency and loss limit. The best choice of hysteresis band and the minimum value of DC link voltage are set by carrying out extensive simulation to maintain the source current THD within the IEEE limit. Variation

of these parameters to design the other components and associated losses are also calculated. A Shunt APF system with a wide range of design parameters has been simulated and the results are shown to compare the design parameters with their associated power losses and the required kVA rating. This procedure can be generalized to design the parameters for other topologies of APF_{sh} system and would be useful for practical design and development of the shunt APF system.

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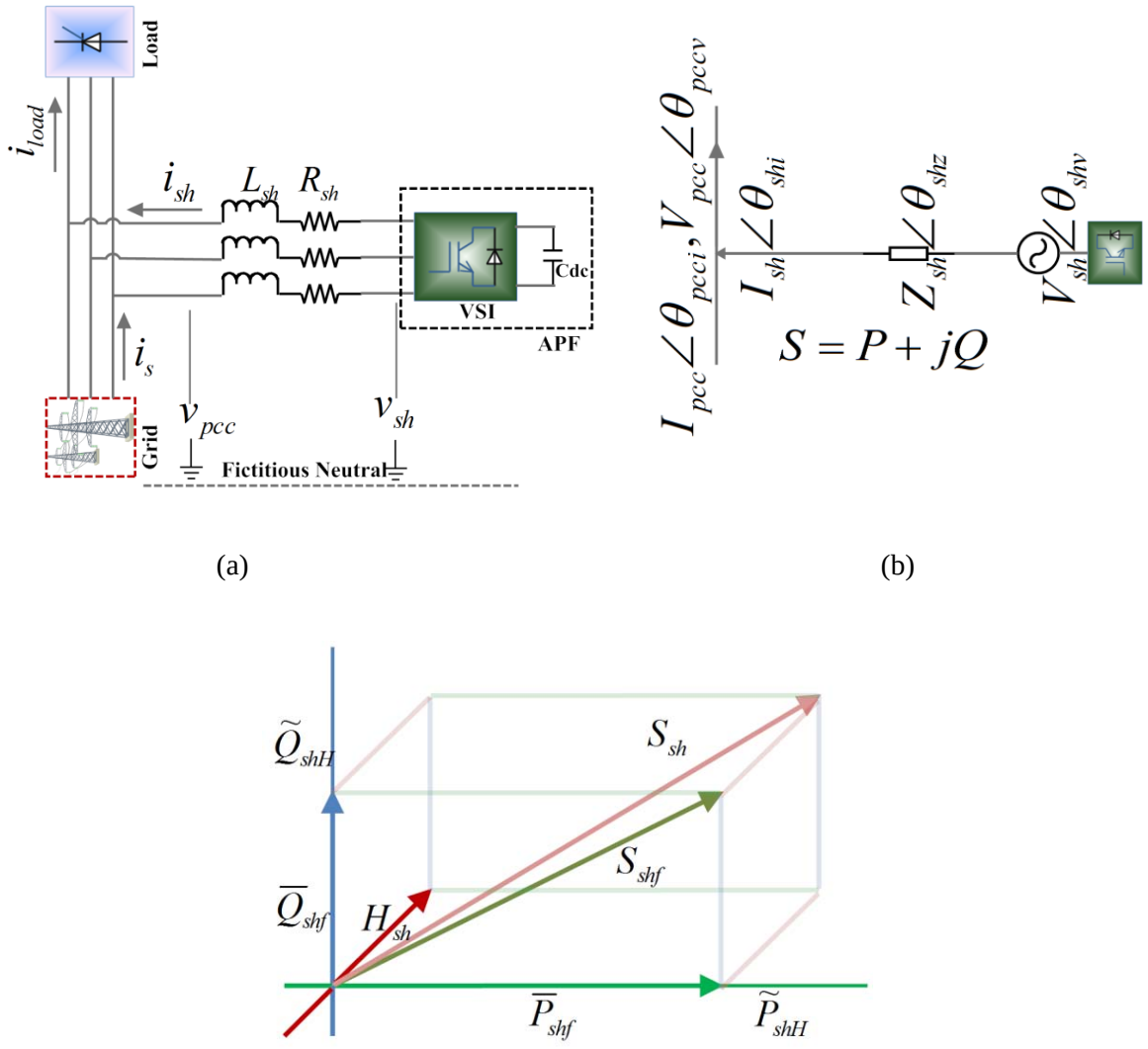
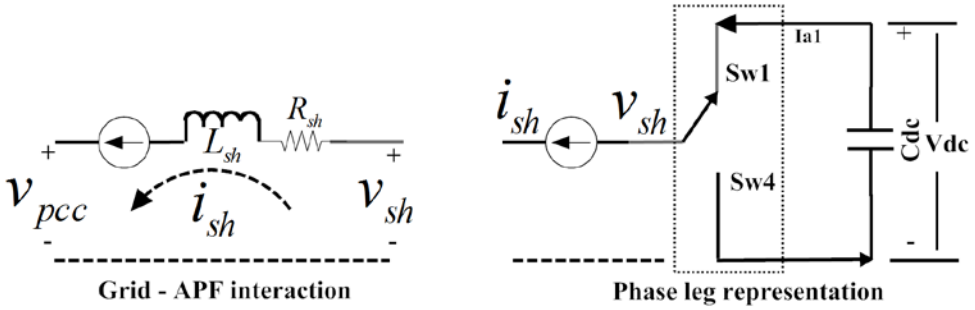
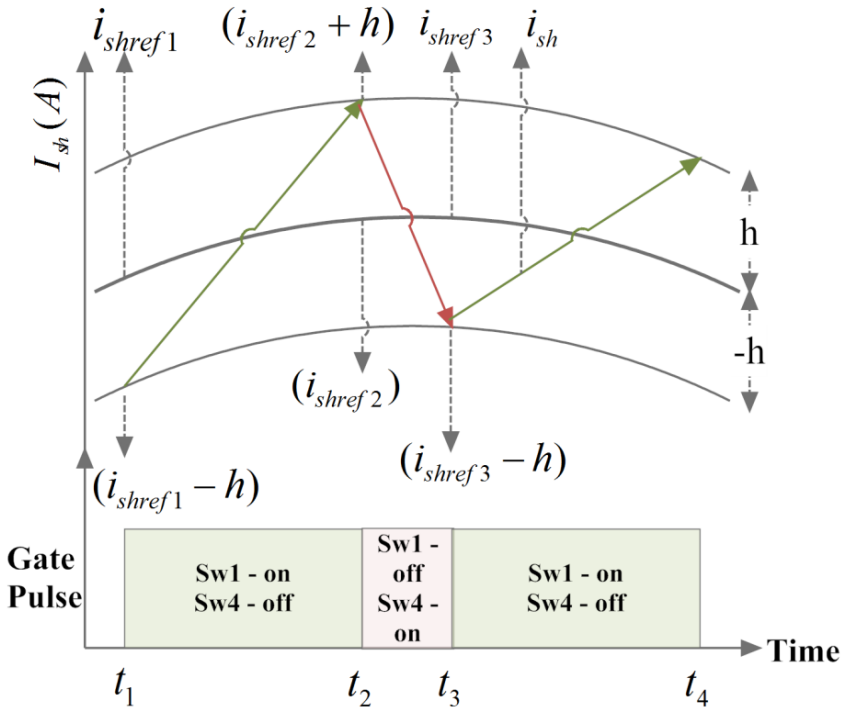


Fig 1- (a) A 3-phase 3-wire power system with APF_{sh}; (b) Power transfer from APF_{sh} to the PCC; (c) Power tetrahedron diagram for APF_{sh}



(a)



(b)

Fig 2 - (a) Compensating power exchange between the Grid and shunt APF and the phase leg representation for Phase A; (b) Switching dynamics of a hysteresis based current controller

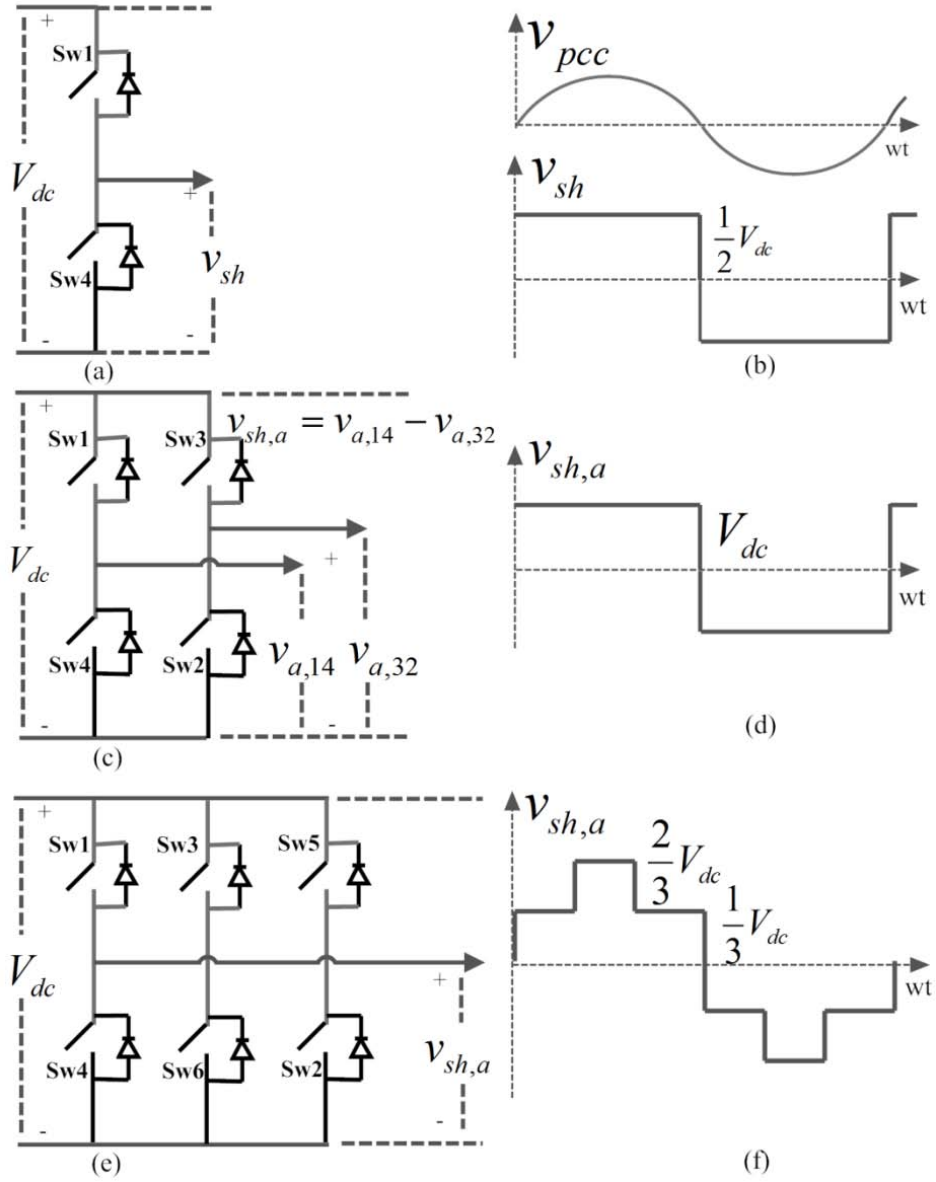


Fig 3 - a) Switching configuration of VSI and output waveform for (a,b) 1-phase, HB; (c,d) 1 or 3-phase, FB and (e,f) 3-phase HB

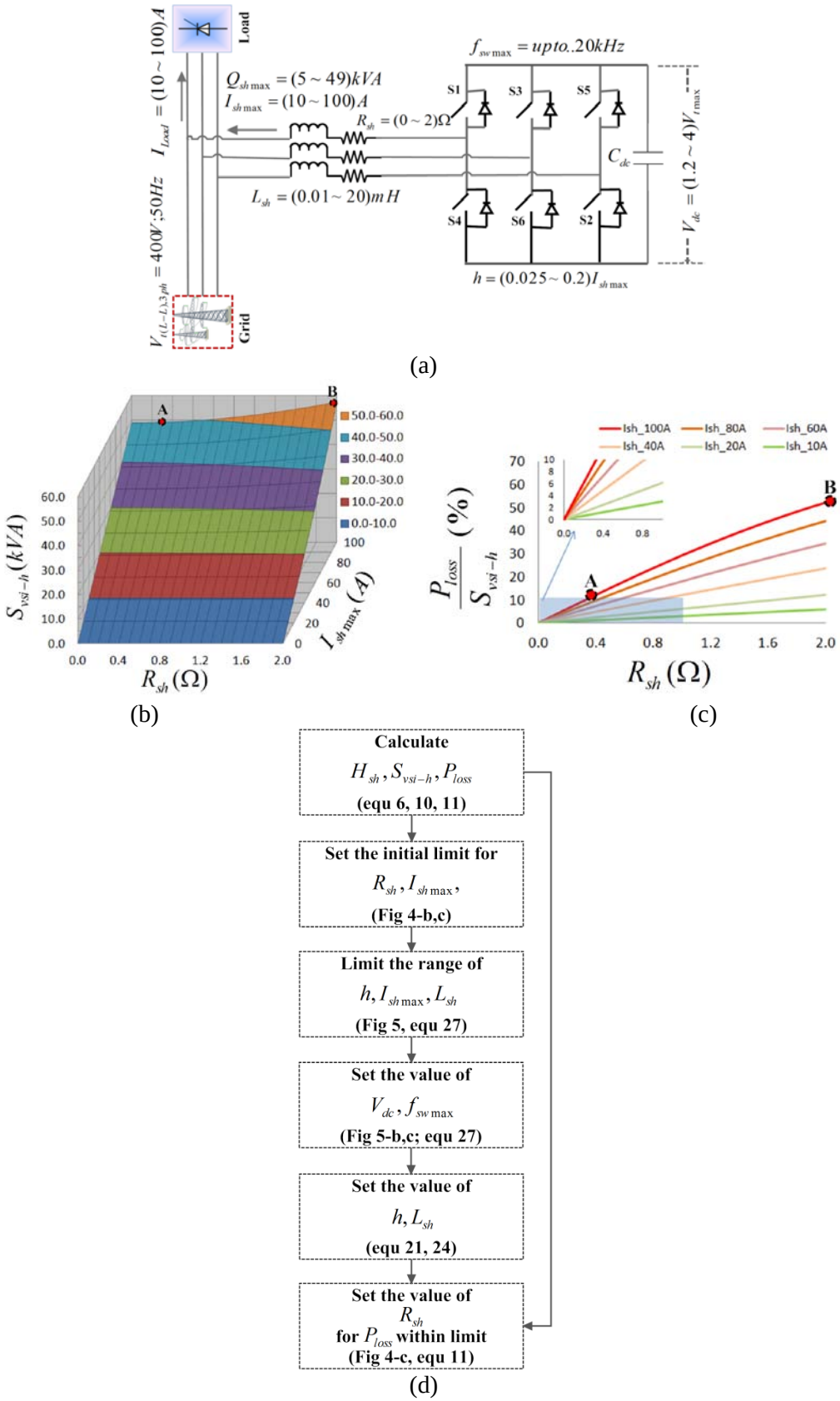
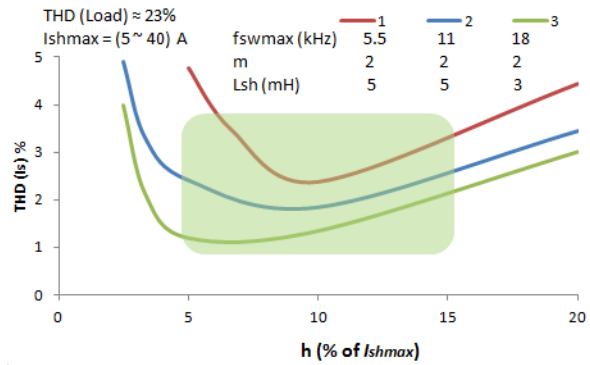


Fig 4 - (a) A 3-ph, 3-wire APF_{sh} connected to the grid and load at PCC; (b) Relation between Actual VSI rating (S_{vsi-h}), R_{sh} and I_{sh}; (c) Corresponding loss of inverter; (d) Design parameters selection procedure/algorithm for APF_{sh}



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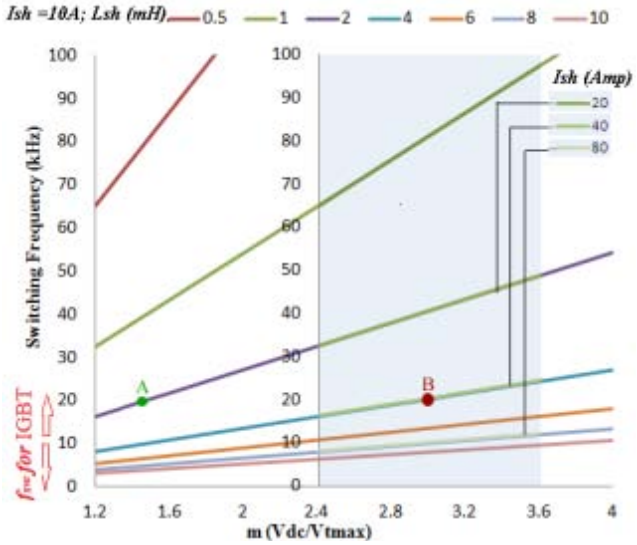

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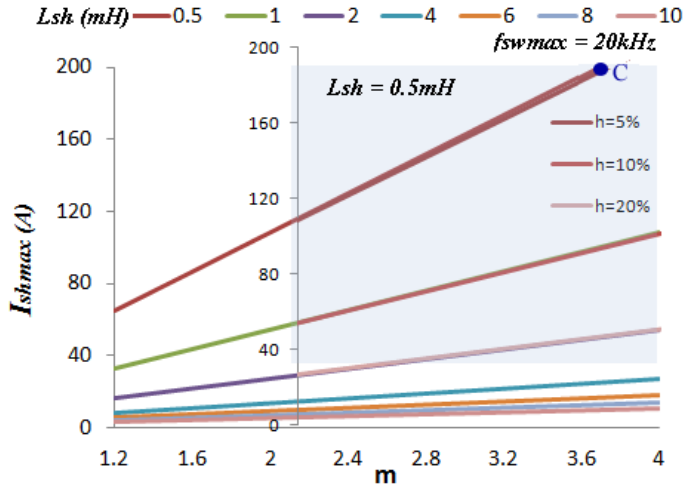
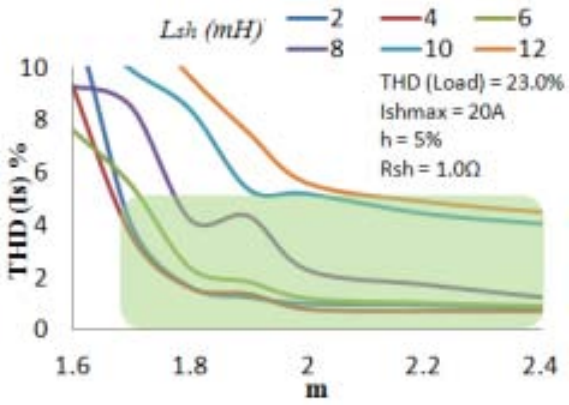


(c)

Fig 5 - (a) Selection of *h* to maintain THD_{Is} within IEEE standard ; (b) Relation between f_{swmax} and L_{sh} for the variation of *m* and I_{shmax}; (c) Relation between I_{shmax} and L_{sh} for the variation of *m* and *h*.



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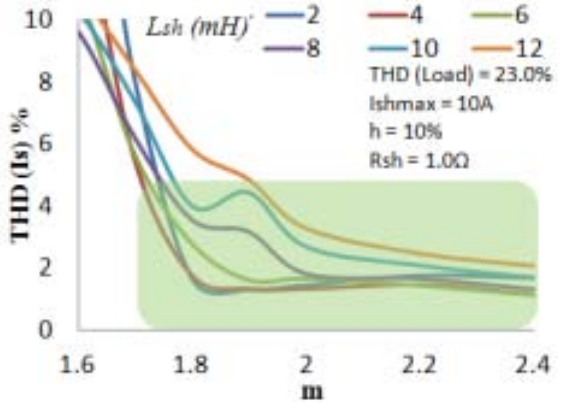

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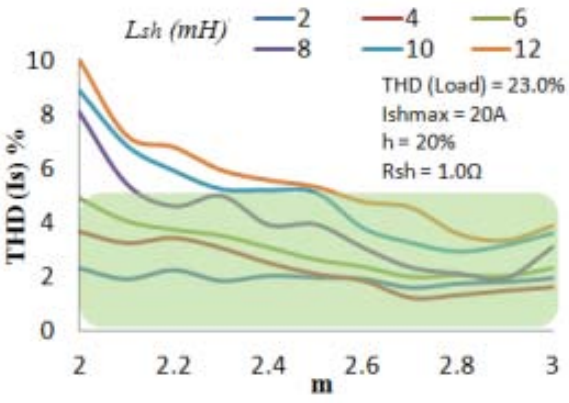
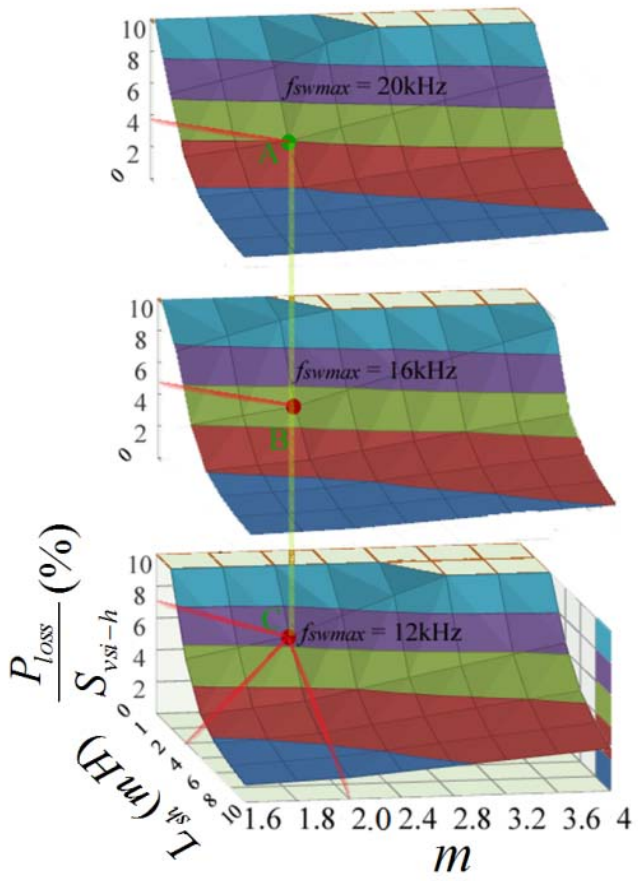


(c)

Fig 6 - THD_{Is} (%) for different values of m, obtained from simulation result for a system to compensate I_{shmax} = 10 to 20A using hysteresis band, *h* as a) 5%, b) 10% and c) 20%



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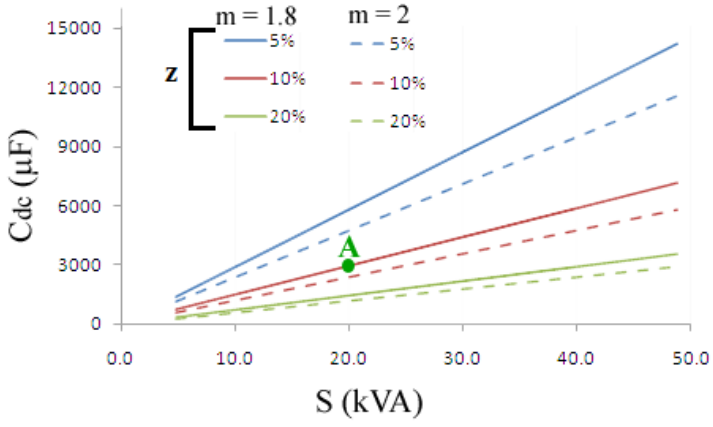

(b)

Fig 7 - (a) Reduction of P_{loss} with the increase of f_{swmax} while the other parameters are constant; (b) Relation between z and S to calculate the C_{dc} for m = 1.8 and 2.0

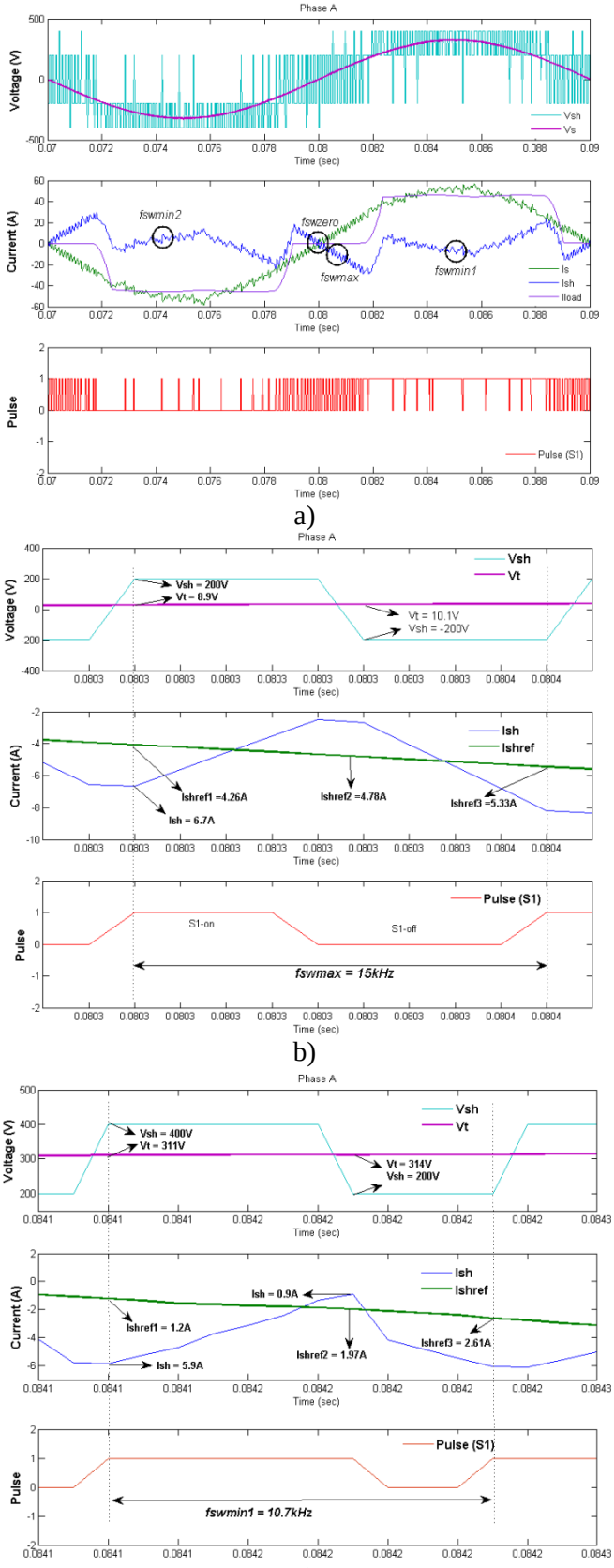

Fig 8 - (a) One complete cycle of an APF in compensating mode, (b) the maximum switching frequencies, f_{swmax} and c) one of the minimum frequency, f_{swmin} at close to 90 deg of v_{pcc}