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PAPER REFERENCE: E/P34 **REVISED VERSION**

MICRO-RAMAN STUDY OF STRESS DISTRIBUTION GENERATED IN SILICON DURING PROXIMITY RAPID THERMAL DIFFUSION

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Abstract

Micro-Raman spectroscopy has been used for analysing the thermally induced stress distributions in silicon wafers after proximity rapid thermal diffusion (RTD). A compressive stress was found on the whole silicon wafer after 15 s RTD. After 165 s RTD the distribution of the stress across the wafer was found to be different: compressive at the edge and tensile at the middle. Thermal stress was relieved in the RTD wafers via slip dislocations. These slip dislocations were observed in the product wafers using optical microscopy. Slip lines propagated from the wafer edge to the wafer centre in 8 preferred positions of maximum induced stress. The thermally induced stress and the slip dislocation density increased with time spent at the RTD peak temperature.

Keywords

Micro-Raman spectroscopy, rapid thermal diffusion, silicon

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Introduction

It has only recently become evident that micro-Raman spectroscopy is a valuable technique for the study of the local mechanical stress in the devices and structures used in microelectronics [1-3]. In particular, it has been shown that this technique can be used for the analysis of defects introduced during metallisation in LOCOS structures and trenches and also in SOI (Si-On-Insulator) materials. To date, the technique has been principally applied to measurements of the stress and strain generated in silicon wafers during thermal processes in furnaces [1]. However, to our knowledge, this technique has not been applied, as yet, to the stress analysis of silicon wafers after rapid thermal diffusion.

Proximity Rapid Thermal Diffusion (RTD) is a technique which can be used to dope silicon wafers with boron during the fabrication of silicon MOSFETs [4]. At present, VLSI and ULSI silicon technologies depend on ion implantation for doping. However, there are limitations on this technique in the formation of shallow boron p-type junctions [5-7]. Ion implantation generates defects in silicon, and these defects must be annealed out at high temperatures after the implant. The high diffusivity of boron in silicon [8] and transient-enhanced diffusion of channelling tails during the thermal anneal makes control of shallow junction depth difficult. Proximity RTD is a suitable alternative to ion implantation because the wafers are heated to high temperatures for very short times, minimising dopant diffusion.

One of the main challenges in rapid thermal processing lies in minimising the development of thermal stress in the wafer [9]. Usually, the wafer is heated on both sides within the RTP using tungsten halogen lamps. There is greater heat loss from the wafer edges than from the wafer centre. The resulting temperature gradient induces thermal stress in the wafer, which can be relieved by the formation of slip lines [10].

There have been several efforts to model thermal stress during RTP. Lord [9] modelled the wafer temperature and stress distribution for unpatterned silicon wafers during RTP, using a simple two-dimensional (2-D) reactor scale model and assuming the temperature profiles to be axisymmetric. Erofeev *et al* [11] modelled the three-dimensional (3-D) temperature and stress distributions of wafers. In [12] the effect of metallisation patterns on thermal stress during RTP processing in silicon wafers have been predicted. Bentini *et al* [13] evaluated the topographic distribution of the slip lines in thermally stressed <100> silicon. The largest deformation in the silicon crystal is experienced in the <110> direction. When the thermally induced resolved stress is larger than the yield strength of the silicon, then slip on the {111} planes in the <110> direction occurs. There are 12 positions on the wafer where stress concentration occurs and where the elastic limit is expected to be exceeded first. Figure 1 illustrates schematically the distribution of these positions. The thermally induced stress component S_1, produces glide which results in steps on the wafer edge, with no visible effect on the wafer surface. The stress components S_2, S_3, S_4 and S_5 give rise to slip lines, which should be visible on the polished surface of the wafer.

In this paper we discuss the application of micro-Raman spectroscopy to the investigation of stress introduced into silicon wafers during rapid thermal processing. Also, micro-Raman spectroscopy measurements and optical microscopy observations of wafers subjected to RTP are compared with theoretical predictions of stress distribution across the wafer.

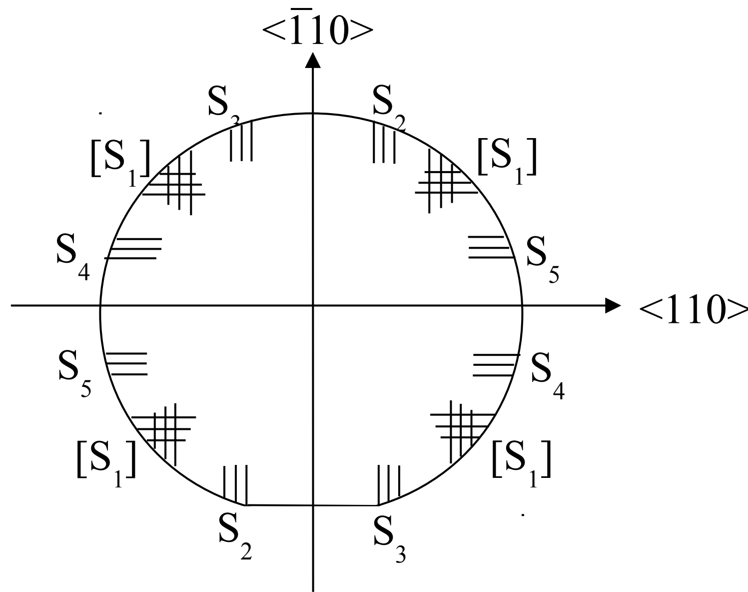

Fig. 1. Locations of the maxima of the thermally induced resolved stresses and the corresponding slip line directions on a <100> silicon wafer

Experimental Procedure

Micro-Raman spectroscopy

The micro-Raman measurements were performed in backscattering mode on a Renishaw Raman microscope system 2000. The 514.5 nm line of Ar^+ laser at a power of 25 mW was used as the excitation source. The incident light is polarised parallel to the width of the line, the scattered light was not analysed. Two objective lenses (40x, 4x), located outside the microscope, were used in conjunction with a pinhole having a diameter of 10 μm to expand the laser spot size. The light is then focused onto the sample using a 50x objective lens mounted on the Olympus BH-2 optical microscope. The size of the laser spot was ~ 2 μm. A Peltier cooled CCD detector with 1 cm^{-1} resolution was used to analyse the spectrum.

The sample is placed underneath the objective lens on an XY translation stage. The sample is moved with this XY stage and at each position a Raman spectrum is recorded. The phonon vibration peak at ~ 520 cm^{-1} is registered together with the exciting line peak at each point, in order to avoid inaccuracy in the peak position due to drift of the calibration frequency. The spectral line was fitted to a Lorentzian, allowing the frequency shift to be measured with an accuracy of 0.02 cm^{-1} [2].

Proximity rapid thermal diffusion

Czochralski grown 4 inch n-type, <100> oriented, 9-15 Ω cm resistivity silicon wafers were used throughout this study.

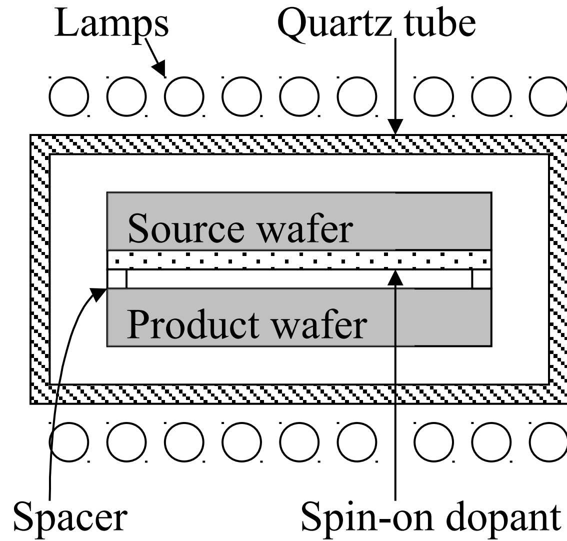

Fig. 2. Wafer configuration during Proximity RTD

As-received wafers were cleaned using H_2SO_4:H_2O_2 followed by a HF dip. Boron doped spin-on dopant (SOD) (Filmtronics, USA) was spun onto the wafers at 6000 rpm for 15 s. The wafers were then baked at 200 °C to evaporate moisture and light organics from the SOD. This dopant source was stacked in proximity to a silicon product wafer on 0.5 mm silicon spacers, Fig. 2. All rapid thermal diffusions were performed in 25% O_2:75% N_2. During proximity RTD, the rapid thermal processor (RTP) ramp rate was 50 °C/s for all wafers. The wafers were held at a peak temperature of 1000 °C for 15 s (product wafer A) and 165 s (product wafer B), respectively.

In this paper, only the silicon product wafers were analysed for stress. Slip lines were observed using optical microscopy. The stress distribution across the wafer was measured using micro-Raman spectroscopy.

Results and Discussion

During RTD, boron trioxide (B_2O_3) evaporates from the spin-on dopant (SOD) at a temperature of 1000 ºC, across the separation gap to the product wafer, where it is adsorbed onto the surface. Boron diffusion is then accomplished by means of a surface oxidation-reduction reaction between the B_2O_3 and the silicon wafer [14], given by:

$$2B_2O_3 + 3Si \leftrightarrow 4B + 3SiO_2 \quad (1)$$

In this reaction doped SiO_2 is formed on the surface of the product wafer and becomes a dopant source for elemental boron, which diffuses into the silicon substrate. The thermal stress which develops within the wafer during RTP may be relieved by slip.

Slip lines were observed in both wafers using an optical microscope. The slip lines observed extended from the edge of the wafers in 8 positions ($S_2 \ldots S_5$), as predicted by Bentini *et al*. The

length of the slip lines in wafers A and B were 0.5 cm and 2.5 cm, respectively. The number of slip lines in wafer A was small compared to the number of slip lines observed in wafer B.

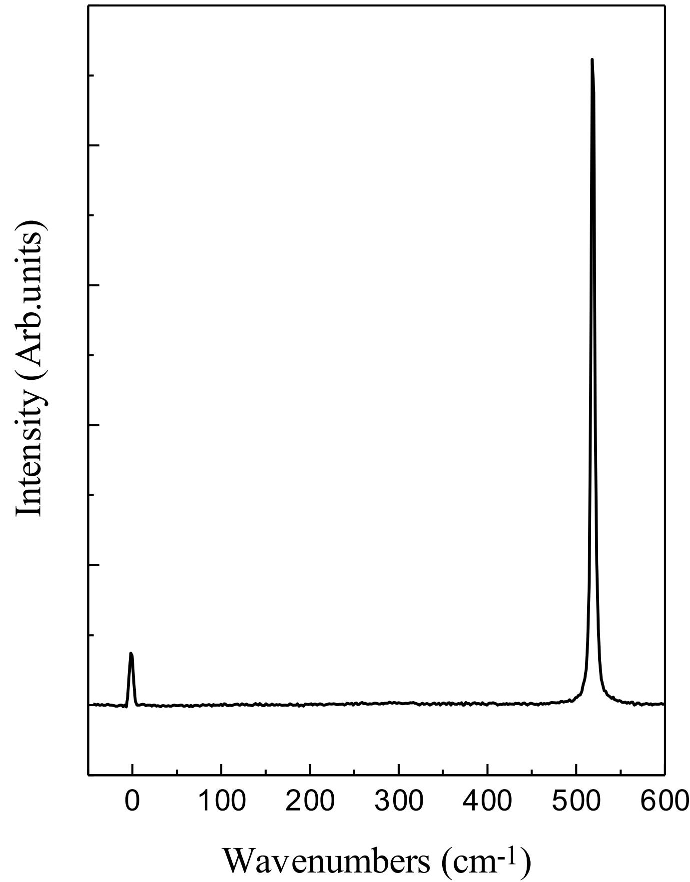

Fig. 3. Raman spectra (in Stokes side) of silicon wafer after RTD process

The crystalline silicon Raman spectrum in a phonon region mainly consists of a narrow peak around 520 cm^{-1} with a half width of about 3.5 cm^{-1}. The spectrum arises from scattering by long-wavelength transverse optical phonons [15]. With a state–of-the-art spectrometer it is possible to identify a shift in the Raman band of the order of ~0.01 cm^{-1} [1]. Background baseline removal followed by a line fit using a Lorentzian function allows three components of the Raman spectrum to be determined viz. intensity, half width and position. These variations are related to the composition, defect density, and magnitude of stress respectively. A relationship exists between the stress, σ (in Pa), and the Raman shift, $\Delta\omega$ (in cm^{-1}) [16]:

$$\Delta\omega = -2\times10^{-9}\sigma, \quad (2)$$

where $\Delta\omega=(\omega_{stress} - \omega_{ref})$ (in cm^{-1}), ω_{stress} is the peak frequency of the phonon band of silicon under the stress and ω_{ref} is the peak frequency of the phonon band of the stress free silicon wafer. A positive or negative shift in the Raman peak position corresponds to compressive or tensile stress, respectively [1] , assuming uniaxial stress only i.e within the plane of the wafer.

Raman measurements for the reference silicon wafer and for the product wafer after 15 s at 1000 °C RTD are shown in Figure 3. The stress free reference value (0 cm^{-1}) is taken on the bare 4 inch silicon wafer directly after the initial cleaning procedure.

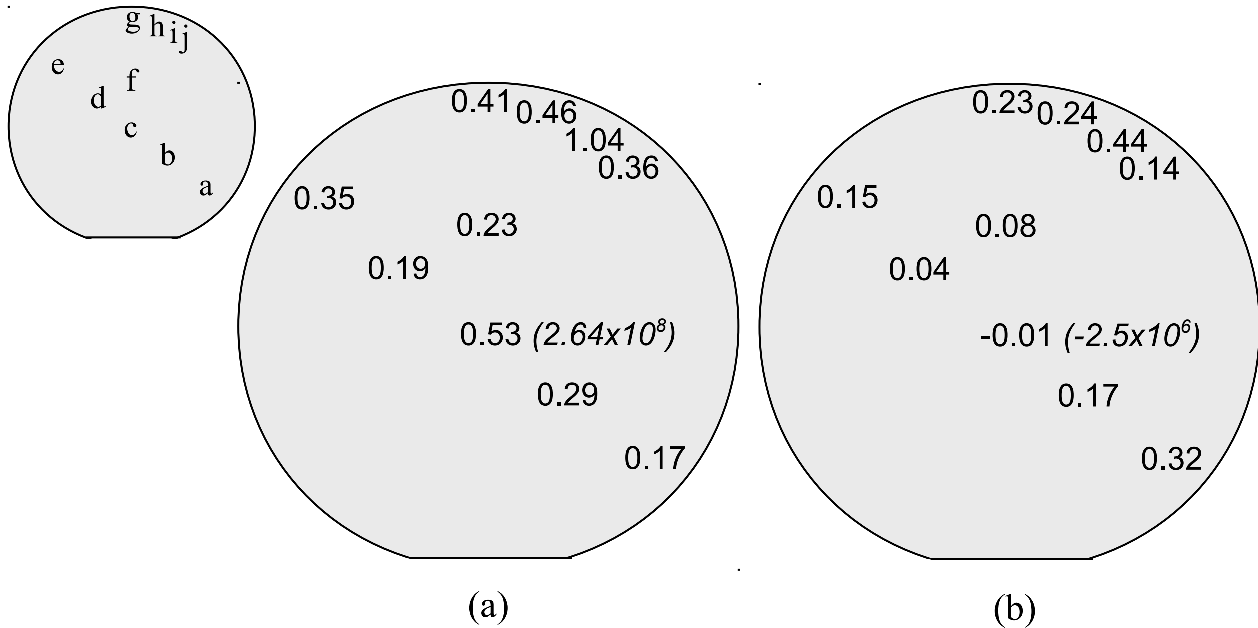

Fig. 4. Raman peak shift measurements ($\Delta\omega$) for (a) Wafer A: RTD at 1000 °C for 15 s, (b) Wafer B: RTD at 1000 °C for 165 s. A positive shift in the Raman peak position corresponds to a compressive stress, and a negative shift corresponds to a tensile stress. The value in brackets denotes the stress, σ, (in Pa), calculated using equation 2.

Figure 4 shows the measured Raman peak shift for wafers A and B. The magnitude of the stress in wafer A is larger than the stress in wafer B. The induced stress in both wafers exceeded the yield strength of the silicon causing the crystal to slip. The formation of slip dislocation lines increased with increased time at the peak temperature, resulting in a greater stress relaxation in wafer B compared to wafer A. Lord predicts that the rapid ramp rates are not the cause of the most damaging stresses in the wafers; it is the temperature non-uniformity at the peak temperature that tends to stress the wafers beyond the yield stress. Due to the strong temperature dependence of the silicon critical yield stress [17], the extent of slip line formation depends on both the peak wafer temperature and the time spent at the peak temperature. Our observations of slip lines and Raman measurements agree with this previous work, and show that for a given peak temperature, slip line formation increases with increasing time at peak temperature. These observations were verified for wafers A and B using a second Raman spectrometer (Dilor SA Labram 1B Raman spectroscopic microscope). Several other wafers were exposed to 1050 ºC for a wide range of RTD durations. Stress distributions similar to wafers A and B were observed for all samples.

These results are also confirmed from the analysis of the band contour. As seen in Table 1, the values of half width (**Γ**) obtained for wafer A change very little for the 10 different points measured. However, for the case of wafer B there is a noticeable increase of half width at the

points where the largest slip lines were observed using optical microscopy. This means that a quite noticeable structural disorder exists in the regions of the large slip lines.

A compressive stress is induced at the edge of wafers A and B, Fig. 4. This observation disagrees with the work of Deaton *et al* [18]. Deaton observed tensile stress at the wafer edges after rapid thermal oxidation of the wafers. We repeated our rapid thermal process using a bare silicon wafer instead of a SOD source wafer. By doing this, the product wafer experienced the same temperature profile as before, however oxidation occurred instead of boron diffusion. The number and length of slip dislocations observed in the oxidised wafer was very small compared to the boron doped wafer. The boron seems to cause additional stress in the silicon lattice. Raman measurements indicated that a compressive stress also exists at the edges of the oxidised wafers. Further investigations are necessary in order to explain why a compressive stress was induced instead of a tensile stress. We believe that this anomalous result may be a result of a variation in the temperature gradient, or some other effect specific to our RTP tool. In Figure 4, point i corresponds to stress component S_2 in figure 1. The Raman peak shift, and therefore the induced stress, at point i in wafers A and B is greater than the peak shift at points g, h and j. This observation also agrees with the predictions of Bentini *et al*.

Table 1
Measured parameters of the Raman bands for wafers A and B: shift of the peak position ($\Delta\omega$) and half width (**Γ**). Note: the half width for the reference wafer shown at the bottom.

Position on the wafer	$\Delta\omega$, cm^{-1}		Γ, cm^{-1}	
	Wafer A	Wafer B	Wafer A	Wafer B
a	0.17	0.32	4.18	4.65
b	0.29	0.17	4.23	4.72
c	0.53	-0.01	4.21	5.21
d	0.19	0.04	4.14	5.26
e	0.35	0.15	4.21	5.14
f	0.23	0.08	4.17	5.32
g	0.41	0.23	4.3	4.86
h	0.46	0.24	4.23	4.95
i	1.04	0.44	4.28	5.06
J	0.36	0.14	4.19	5.17
Bare Si			4.18	

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