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Investigation on the Performance of UPQC-Q for Voltage Sag Mitigation and PQ Improvement at a Critical Load Point

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Abstract

The Unified Power Quality Conditioner (UPQC) is one of the major custom power solutions, which is capable of mitigating the effect of supply voltage sag at the load end or at the Point of Common Coupling (PCC) in a distributed network. It also prevents the propagation of the load current harmonics to the utility and improves the input power factor of the load. The control of series compensator of the UPQC is such that it injects voltage in quadrature advance to the supply current. Thus, the series compensator consumes no active power at steady state. The other advantage of the proposed control scheme is that the series compensator can share the lagging VAR demand of the load with the shunt compensator and can ease its loading. The UPQC employing this type of *quadrature* voltage injection in series is termed as UPQC-Q.

The present paper discusses the VA requirement issues of series and shunt compensators of a UPQC-Q. A PC-based new hybrid control has been proposed and the performance of the UPQC-Q is verified in a laboratory prototype. The phasor diagram, control block diagram, simulations and experimental results are presented to confirm the validity of the theory.

1. Introduction

The Unified Power Quality Conditioner (UPQC) has evolved to be one of the most comprehensive custom power solutions for power quality issues relating to non-linear harmonic producing loads and the effect of utility voltage disturbance on sensitive industrial loads [1- 13]. A UPQC is a combination of shunt and series compensation and is designed to cater for multiple power quality problems. Two cascaded inverters joined back to back by a common DC link constitute the power circuit of a UPQC. The shunt compensator (SHUC), provides VAR compensation to the load, and is positioned parallel to the load. It also

provides harmonic isolation between the load and the utility supply, and compensates for load current unbalance. The series compensator (SERC), regulates the incoming voltage quality from the supply side, and keeps the load end voltage insensitive to the supply voltage problems such as sag/swell or unbalance depending upon the control strategy of the SERC. This is achieved by injection of a compensating voltage between the supply and load, which restores the load voltage to its pre-disturbance value. At the same time, the reactive compensation of the load can be provided by both the SERC and the SHUC. The cost of power quality to manufacturing (in the semiconductor, pharmaceutical, automobile sectors, etc) and emergency services (aviation, medical, etc), together with the driver of efficient energy performance, justifies the cost and complex control required for a UPQC [14-17].

The present paper proposes a new voltage sag compensation strategy enhancing the capability of UPQC as voltage sag is a source of major PQ problem [14, 16, 17]. The control strategy has been designed for the SERC to inject a voltage that leads the supply current by 90^o in phase such that the same desired effect is achieved as in case of a voltage injection in phase with the supply current. The operating principle, rating, and the detail of the control strategy have been discussed in the paper. To investigate the performance of the proposed control scheme for the UPQC, simulations are carried out and validated with experimental results.

2. Proposed UPQC-Q System and Its Operating Principle

The UPQC proposed and developed in this paper has the following features:

- Eliminates the harmonics in the supply current, thus improving utility current quality for nonlinear loads.

- Provides the VAR requirement of the load, so that the supply voltage and current are always in phase and therefore no additional power factor correction equipment is necessary.
- Maintains load end voltage at the rated value even in the presence of balanced supply voltage sag.
- Ensures that voltage injected by UPQC to maintain the load end voltage at the desired value is taken from the common dc link of the UPQC, which is self-sustaining and therefore no additional dc link voltage support is required for the series compensator.
- Maintains a quadrature advance relationship between the injected voltage and the supply current, so no real power is consumed by the SERC in the steady state, which is a significant advantage when the UPQC mitigates under-voltage conditions.
- Because of the self-sustaining dc bus voltage, duration of the sag or under-voltage is not a constraint on the operation of UPQC. The SERC of the UPQC also shares the VAR of the load with the SHUC. This reduces the VA loading of the SHUC.

To highlight this new aspect of quadrature voltage injection, the equipment has been termed as a **UPQC-Q** in the paper.

Fig. 1 shows a typical power circuit schematic of a UPQC. Each compensator consists of an IGBT-based full bridge inverter (single- or three-phase, according to the application), which may be operated in a voltage or a current controlled mode depending on the control scheme. The SERC is connected in series with the supply voltage through a low-pass RLC filter and transformer. The SHUC is connected in parallel to the load (which may be linear or non-linear) through an inductor, L_{SHUC}.

The UPQC could be modelled as a combination of an ideal controlled voltage source and an ideal controlled current source, as shown in Fig. 2, where the operation of the UPQC is explained by means of phasor analysis.

In the following analysis, the source voltage (V_S) is taken as the reference and is given by:

$$V_L \angle \theta = V_S \angle 0 + V_{inj} \angle \gamma \tag{1}$$

where V_L is the load voltage and V_{inj} is the injected voltage from the SERC of the UPQC. It may be noted that for a given load power factor and voltage sag the requirement is to determine the magnitude and phase angle of V_{inj} to maintain the load voltage constant at its rated value. There are an infinite number of solutions for V_{inj} to satisfy this requirement. The specific control strategy proposed in this paper maintains the angle of injection γ equals to 90^o in advance of the supply current of the UPQC to minimise the power consumption of the SERC. The load current is given by:

$$I_L \angle \theta - \phi = I_S \angle 0 + I_C \angle \beta \tag{2}$$

The angle ϕ represents the lagging angle of the load current I_L with respect to V_L and θ is the voltage advance angle of V_L due to V_{inj} with $\beta = (\theta \pm 90^0)$.

Fig. 3(a,b,c) show the current and voltage required from UPQC under different load power factor conditions for the same voltage sag. When the supply voltage has no deficiency; $V_S = V_{L1} = V_{S1} = V_0$ (a constant), and the series injected voltage V_{inj} requirement is zero.This state is represented by adding suffix "1" to all the voltage and current quantities of interest. The load current is I_{L1} ($I_{L1}=I_1$) and the SHUC compensates the reactive component I_{c1} of the load, resulting in unity power factor. Thus, the current drawn by the SHUC is $-I_{c1}$, which is opposite to the load reactive current I_{c1}. As a result, the load always draws the in-phase component I_{s1} from the supply. For non-linear loads, the SHUC not only supplies the reactive current, but also the harmonic currents required for the load. Thus, after the compensation

action of the SHUC, only the fundamental active component of the current is required to be supplied from the utility. Since the SHUC is able to compensate load VAR and harmonics, the SERC can compensate the voltage sag. However, under certain situations the SERC can provide capacitive VARs and thus relieve the SHUC from supplying the total amount of VAR of the load, as discussed later in this section.

As soon as the load voltage V_L sags, due to utility voltage problems, the UPQC is required to take action to compensate for the sag, so that V_L is restored to its desired magnitude. As seen from Fig. 3a, the restoration of V_L has been achieved by specifically selecting $\gamma = 90^0$. This condition is represented by adding suffix "2" to the parameters. Consequently the load current changes to I_{L2}. The SHUC injects I_{c2} in such a way that the active power requirement of the load is only drawn from the utility. It can be observed from the phasor diagram that the utility current is $I_{s2,}$ and is in phase with V_{s2}.

From the phasor diagram in Fig. 3a, the following relationships can be obtained.

$$I_{s2}\cos\theta = I_{L2}\cos\phi \tag{3}$$

$$I_{c2} = I_{L2}\sin(\phi-\theta)/\cos\theta \tag{4}$$

If $\theta<\phi$, then the two compensators share the load inductive VAR (Fig. 3a).

It is interesting to observe that if the supply voltage sag is such that for a certain load power factor, the angle θ becomes equal to ϕ, then from (3) it can be inferred that

$$I_{s2} = I_{L2} \tag{5}$$

Thus, I_{c2}, as shown in Fig. 3b is zero. This is the minimum loading condition or zero VA loading of the SHUC. This is a special case where the SERC supplies the VAR demand of the load.

If the supply voltage sag is such that θ>ϕ (Fig. 3c), then the SHUC current has to be increased to restore the leading power factor to unity. This condition may occur even with small voltage sag (say 15%) when load power factor is already high.

The pre-sag voltage and post-sag voltage, will not necessarily be in the same phase. However, the control scheme is valid irrespective of this as the compensation is with respect to the post sag voltage only.

3. VA Requirement of UPQC-Q

Following the operational requirement, it would be straight-forward to decide the rating of the UPQC.

From Fig. 3, it can be seen that at the fundamental power frequency

$V_{L1} = V_{L2} = V_{s1}$ = 1 p.u . (Constant) (6)

If the load current is assumed to be $I_L = I_{L1} = I_{L2} = 1$ p.u, (7)

with fundamental p.f. (D. P. F) = $\cos\phi$,then the active power demand in the load remains constant, i.e.

$V_s I_s = V_L I_L \cos\phi$ = Constant (8)

In the case of a sag where $V_{s2} < V_{s1}$, and x denotes the p.u. sag,

$V_{s2} = (1-x)V_{s1} = (1-x)p.u.$ (9)

Now, to maintain constant active power

$V_{s1} I_{s1} = V_{s2} I_{s2}$ (10)

which leads to, $I_{s2} = (1.I_L \cos\phi)/(1-x) = \cos\phi/(1-x)\, p.u.$ (11)

From the right angle triangle formed by V_{s1}, V_{s2} and V_{inj} in Fig.3, the following equations can be derived.

$V_{inj} = \sqrt{V_{s1}^2 - V_{s2}^2}$ (12)

$$\frac{V_{inj}}{V_{s2}} = \tan\theta, V_{inj} = V_{s2}\tan\theta \ , \ \ V_{inj} = (1-x)\tan\theta \qquad (13)$$

Thus, the rating of the SERC is expressed as = $V_{inj} I_{s2} = \cos\phi \tan\theta$ p.u. (14)

The SHUC current can be calculated from the trigonometry of the vector diagram (fig.3)

$$I_{c2} = \sqrt{I_{L2}^2 + I_{s2}^2 - 2I_{L2}I_{s2}\cos(\phi-\theta)}$$

$$= \frac{\sqrt{(1-x)^2 + \cos^2\phi - 2\cos\phi\cos(\phi-\theta)(1-x)}}{(1-x)} \text{p.u.} \qquad (15)$$

It follows that the rating of the SHUC is

$$= \frac{\sqrt{(1-x)^2 + \cos^2\phi - 2\cos\phi\cos(\phi-\theta)(1-x)}}{(1-x)} + \frac{(1-x)^2 + \cos^2\phi - 2\cos\phi\cos(\phi-\theta)(1-x)}{(1-x)^2} Z_{SHUC}\, p.u. \qquad (16)$$

where Z_{SHUC} is the shunt inductance impedance.Adding (14) and (16), the total VA rating of the UPQC-Q can be evaluated.

Under any condition, the net active power flow through the UPQC would be zero, as the generation is always balanced by consumption of power between the SHUC and the SERC. As seen from (8) and (10), the utility active power is balanced by load power demand, UPQC ideally does not demand any net active power from the utility (apart from the device losses). The generation and consumption of power by the SERC and the SHUC is balanced within the UPQC.

As found earlier if $\theta = \phi$, $I_{s2} = I_{L2}$. Under these circumstances, the current I_{C2} as given in (15) becomes zero. The VAR loading is completely provided by the SERC under these conditions. For several power factors and voltage sag values, the condition of zero VA loading of the SHUC can be observed in Fig. 4a. Fig. 4b shows the SERC VA loading of UPQC-Q under different voltage sag and load power factor conditions. The Z_{SHUC} in all these cases has been

chosen to be 0.1 p.u. The combined loading curve is shown in Fig. 4c, with varying p.f. and voltage sag conditions.

A typical example when the load p.f. = 0.7 with a supply voltage sag is discussed. For 20% voltage sag, the loading on the SERC and the SHUC are 0.525 p.u and 0.1927 p.u. respectively, which means the total VA consumption of UPQC-Q is 0.7177 p.u. With the conventional UPQC control the SERC and the SHUC loading under the same condition would be 0.175 p.u. and 0.7893 p.u. respectively, which would add up to 0.9643 p.u [7]. Thus the VA demand of the UPQC-Q is lower than the conventional UPQC for low power factor loads, which is of an advantage in terms of minimising all operational losses including the device losses and dc link losses. This would lead to better efficiency. By phase shifting the V_L with respect to the V_s, the effective power factor as computed with reference to V_s is increased, which lowers the overall VA demand from the supply. In addition, the VAR shared between the SERC and the SHUC helps in lowering the total VA demand of the UPQC-Q.

4. Control Strategy of the UPQC-Q

Based on the above analysis, a suitable control technique has been designed for the UPQC-Q. Fig. 5 shows the closed loop control circuit for both the SERC and the SHUC. The control scheme can be divided into 4 modules:

- SHUC controller
- DC link voltage Controller
- SERC controller
- PWM voltage controller

To enhance the speed of response, and also to retain the flexibility to modify parameters of the controller, a hybrid controller has been designed. Thus controller was partly implemented

with analog circuits and partly with digital circuits using a PC and with PCL-726 (DAC)and PCL-208 data acquisition cards. This implementation helps in achieving shorter sampling time. Analog and digital circuits were built on modular cards.

The control scheme is explained on per phase basis.

With i_s and V_{dc} sensed, the SHUC controller generates the appropriate switching signals for the SHUC as follows. The DC link voltage reference V_{dc}^* is selected depending upon the maximum VAR to be compensated at the load end and the % sag to be mitigated at the supply end. The difference between the two voltages (V_{dc}^* - V_{dc}) is processed through a PI controller (PI -1) (in Fig.5) and gives a direct measurement, $I_{ref(mag)}$, of the active power requirement of the load and the UPQC from the supply. The Kp and Ki gains used in the experiment are 1 and 0.1 respectively, which have been found by trial simulations. The trial was based on the performance of the dc link voltage reaching its reference value after a disturbance and minimal transient oscillations respectively. The DC link voltage controller is completely PC based digital controller. $I_{ref(mag)}$ multiplied by a synchronised sinusoidal template with the supply voltage, generates the reference current (i_s*) for the hysteresis controller, which is analog controller to overcome the speed of limitation of the available data acquisition cards. The harmonic current suppression in the utility current is performed through a hysteresis controller, where the hysteresis band determines the quality of the supply current spectra. A narrow band will yield less THD, but the switching frequency of the converter may be very high. Then, based on minimum THD guidelines, a suitable trade-off can be designed. In the experiment the average switching frequency was found to be about 12 KHz for satisfactory performance.

Because of the fast acting current controller of the SHUC, the SERC would always find the load as linear in nature and with unity power factor. Therefore, for all load conditions the phasor diagram analysis in Fig. 3 would hold good for voltage injection analysis for SERC.

When a sag is detected such that $|V_{s2}| < |V_{s1}|$ (rated), then V_{inj} is calculated from(12). Now from PWM method [18], $\sqrt{2}V_{inj} = MI\ (V_{dc}/2)$, where MI is the desired modulation index (MI).

Therefore, $MI = (2\sqrt{2}\ .V_{inj})/V_{dc}$ (17)

If *x* is the p. u. sag to be mitigated, minimum dc link voltage would be

$V_{dc} = 2\sqrt{2}\ .\sqrt{x(2-x)}\ .V_{s1}$, (18)

for maximum value of MI =1 (taking the injection transformer turns ratio to be 1:1).

However, the theoretically derived MI cannot be directly implemented to the PWM voltage controller due to low pass filter phase shift incorporated in the measurement circuit (to sense the vsec) and the load current variation. Hence, with appropriate pre-calculated phase shift and a combination of feed-forward (m1) and feedback controller (m2) the final modulating signal (m3) could be derived for the SPWM generator for the SERC, which is explained in detail in the following section.

The supply voltage peak calculator (Vs_peak) primarily detects voltage sag, and decides the appropriate voltage to be injected through the feed forward controller that determines the MI in Fig. 5.

The output of the low pass filter, that feeds vsec to ADC, incorporates a phase shift of about 15° lag to the actual injected voltage. To account for this phase shift appropriately, in the quadrature injection control, the sine-multiplier has been chosen to be 75°(instead of 90°). It multiplies with the calculated MI and makes a sinusoidal modulating signal m1, such that the net effect could have the desired phase angle at the output. It is to be mentioned that in general all low pass filters will introduce phase shift. In the present case, the calculations are

performed according to the phase shift of the laboratory prototype. While designing for other values, the phase shift of the filters can be calculated from the components and switching frequency and the phase can be adjusted accordingly. On top of that, the m2 signal explained later in the section can dynamically adjust any additional phase shift due to load change.

To generate the ideal injected voltage (vinj*), a sinusoidal template with the respective phase-voltage is phase shifted by 90° (v90). It is sensed through another ADC. It is then multiplied with a gain, and becomes the reference injected voltage for a particular phase ($vinj^*$). The error ($vinj^*$ - vsec) is processed through a software PI controller (PI-2 in Fig 5), whose output is fed through the DAC card, to generate a signal m2. The Kp and Ki gains are 0.002 and 0.005 respectively, which are chosen by extensive trial simulations for fast response, dynamic phase shifting performance and fast response of sag controller.

The dynamic load current change in the quadrature voltage control principle will be reflected as change in inductance, and would alter the pre-calculated filter shift that cannot be predetermined. But a feedback controller (m2) that compares the actual voltage (vsec) with the ideal voltage (vinj*) can eliminate this error caused due to dynamic load change.

In addition, there are transformer leakage reactance drops, resistance drops and the voltage drop due to low pass filter connected at the output of the SERC to filter the switching ripples of the SERC. The load active power demand increase will also increase the source current. That current will be reflected to the primary side of the injection transformer as well. Thus, the drop in the above mentioned elements will change the injected voltage magnitude and phase which need to be corrected by a closed loop control with good dynamics. It should be noted that only open loop controller for the SERC will be inadequate.

The signals m1 and m2 are externally added with an analog adder to generate the final modulating signal for each phase of the SERC (m3). This control scheme ensures fast and effective control of the series injected voltage.

This goes to the PWM generator to generate appropriate switching signal for the SERC. Thus the hybrid control method maintains the accuracy, speed and flexibility, combining the advantages of analog and digital controllers.

5. Case Studies Through Simulation and Experiment

5a. Simulation Results

The three-phase UPQC-Q with its control scheme has been simulated in SABER, which is a Power Electronics software capable of simulating power circuit with control signals. Fig. 6a shows the steady state voltage and current for phase-A. It is found that the SHUC of the UPQC is capable of maintaining unity input power factor. Fig. 6b shows the supply current, the load current and the SHUC current of phase-A. A three phase 10 KVA diode bridge rectifier has been selected as nonlinear, harmonic current producing load for 400 V three phase distribution system. The THD of the load current is around 24% in each phase, which after compensation, is reduced to 4.8%. Fig. 7a shows the performance of UPQC-Q under 20% supply voltage sag. It is seen that when the sag occurs, the load voltage also dips. But due to fast compensation, the load voltage is recovered completely in the next cycle. In the result presented, the maximum sag is 14.7% in phase A at the time of the occurrence of the disturbance. When the voltage is restored, maximum overshoot is 15% in phase-A of the load voltage. At the time of injection of series voltage, THD in the load voltage is found to be around 4% (within the IEEE specified limit of 5%).

Fig. 7b shows the dynamic change in the SHUC current in phase A under supply voltage sag. To control the leading load power factor, the SHUC current has to be lagging during sag compensation. Fig. 8 shows an interesting result with leading and lagging linear load current (combination of R, L and C). The value of the load current prior to 0.2 sec is 7.6 A (per phase), with a lagging p.f. of 0.8. The supply current is 6.3A and the SHUC current is 4.5 A.

At t = 0.2 sec, the load power factor has been changed to leading p.f. of 0.81. It is observed from Fig. 8 that the SHUC current also changes its phase so as to keep the supply current in phase with the supply voltage. From the measurement it is found that the SHUC current is 4.5 A (which is close to the theoretical value of 4.45A). The harmonic spectrum of the supply current shows that the THD is 4.2%, which is within the IEEE specified limit.

5b. Experimental Results

After extensive simulation of the proposed system in SABER, a small scale laboratory prototype of the UPQC-Q for experimentation has been designed and fabricated. The algorithm for real time coordinated control of the UPQC-Q is implemented in Turbo-C; the computation of each cycle takes about 168 μsec. The sampling speed is found to be sufficient for successful operation. Detail system parameters of the experimental setup are given in Table 1.

Table 1: System parameters for experimental set up

System voltage	60 V (L-L), 3 Phase, 50 Hz
Three phase non-linear load: Diode bridge rectifier load, drawing dc load current of	2A
DC Capacitor for the UPQC	2200 μF, 400V
Dc link voltage reference	110 V
IGBT make of the UPQC inverters 50A, 1200 V, Fuji Electric (Japan)	
Model no. 2MB150N-120	
Interface Inductor (Z_{SHUC})	4.3 mH, 0.6 Ω
LPF parameters	R = 0.6 Ω, L = 4.2 mH, C = 60 μF
Transformer parameters	(pri)Lp = 5.66 H, Rp = 0.7 Ω, (sec) Ls = 1.38H, Rs = 0.5 Ω

A three-phase diode bridge rectifier has been used as a non-linear load and the effect of change in load current is recorded for each phase. Fig. 9(a) (for phase A) shows a change in load current from 1.64 A to 2.14 A (24% change) per phase. The corresponding change in supply current is observed to be from 2.65 A to 3.5 A. Fig. 9(b) show results of the supply voltage and supply current of phase-A when the load change, as mentioned above, occurs.

The measurement of harmonic spectra is carried out through a power analyzer (PM100R). It is observed that the dominant harmonics in the load currents are the 5^{th}, 7^{th}, 11^{th} and 13^{th}, and the THD of the load current is 23.28% (for phase A). With the application of the UPQC, the utility current THD has been reduced to 2.957%. The displacement factor has improved from 0.768 to 0.992.

Three-phase UPQC-Q dynamic performance is observed in Fig. 10a on a 100 V pk-pk supply system. It shows that for supply voltage sag of 8%, the (Ch-1) load voltage remains at its specified level. Ch-2 shows the peak of the supply voltage (1V in the sensor output is equivalent to 10.53V in the actual circuit). Fig. 10b shows the actual injected voltage of the SERC during voltage sag. The experimental results show that the control objectives are satisfied.

6. Conclusion

A control scheme for UPQC with injection of voltage in quadrature to the supply current has been proposed in this paper. The operational and rating issues of this UPQC-Q are investigated. It is seen that the UPQC-Q is capable of maintaining harmonic isolation between utility and load. The utility voltage sag does not affect the load voltage as the SERC injects adequate compensation to maintain the load voltage to its desired value. On the other hand, the load VAR and harmonics do not pollute the utility as their demand is supported locally by the SHUC and partly by the SERC. The major advantage of this control scheme is that for a long duration under-voltage the VA consumption of the UPQC-Q remains minimal. Also, the SHUC provides constant support to the common dc link, so that it does not require an external supply to maintain its specified voltage for longer duration sags.

The control scheme effectively creates a voltage shift between the supply voltage and the load voltage in the presence of voltage sag, and reduces the effective power factor of the load

seen from the supply voltage. This strategy effectively helps to achieve minimum VA loading during the operation of UPQC. Simulation results have been carried out to examine the performance of the UPQC-Q. Simulation has been validated by experimental results.

Although the proposed control scheme cannot compensate for unbalanced voltage conditions, an optimal control can be designed to eliminate this problem, which has been discussed as a separate work [19, 20].

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Investigation on the Performance of UPQC-Q for Voltage Sag Mitigation and PQ Improvement at a Critical Load Point

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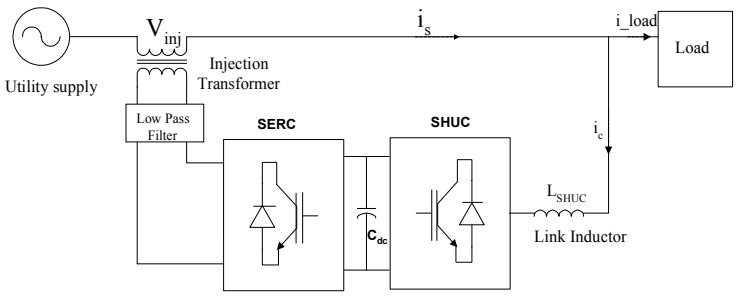

Fig. 1 Schematic Diagram of UPQC

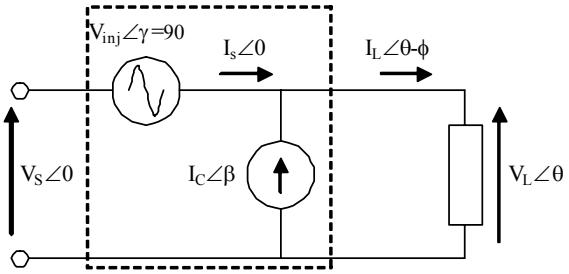

Fig. 2 Fundamental Frequency Representation of UPQC

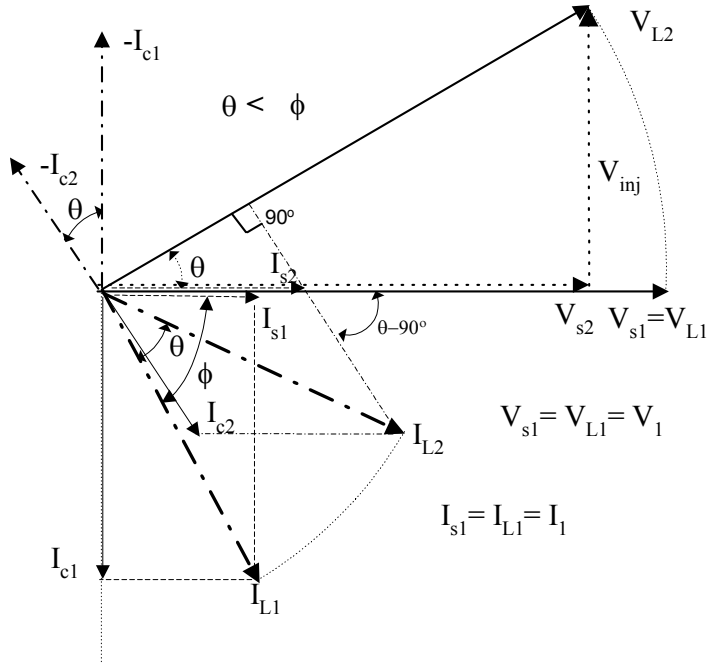

Fig. 3 a Phasor diagram of UPQC-Q for fundamental power frequency when θ <Φ

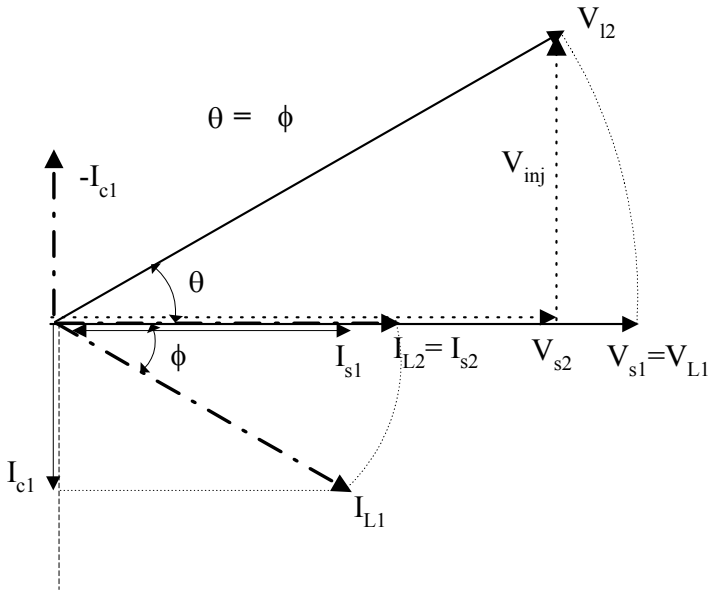

Fig. 3 b Phasor diagram of UPQC-Q for fundamental power frequency when θ = Φ

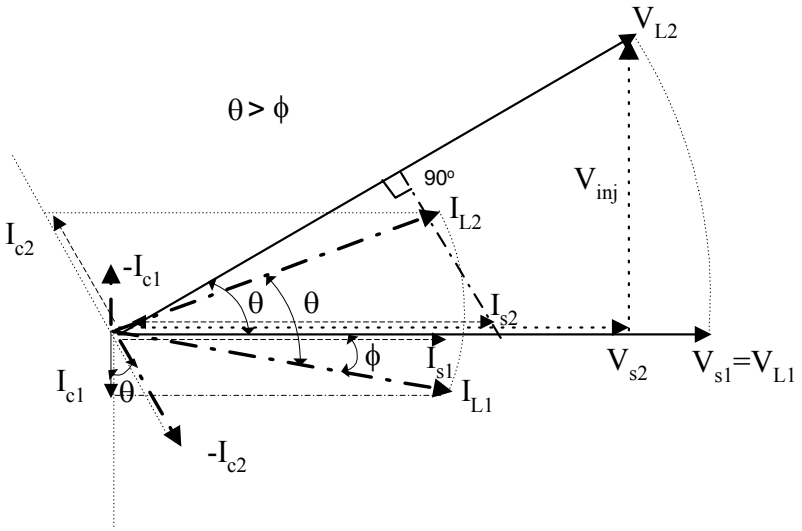

Fig. 3 c Phasor diagram of UPQC-Q for fundamental power frequency when θ >Φ

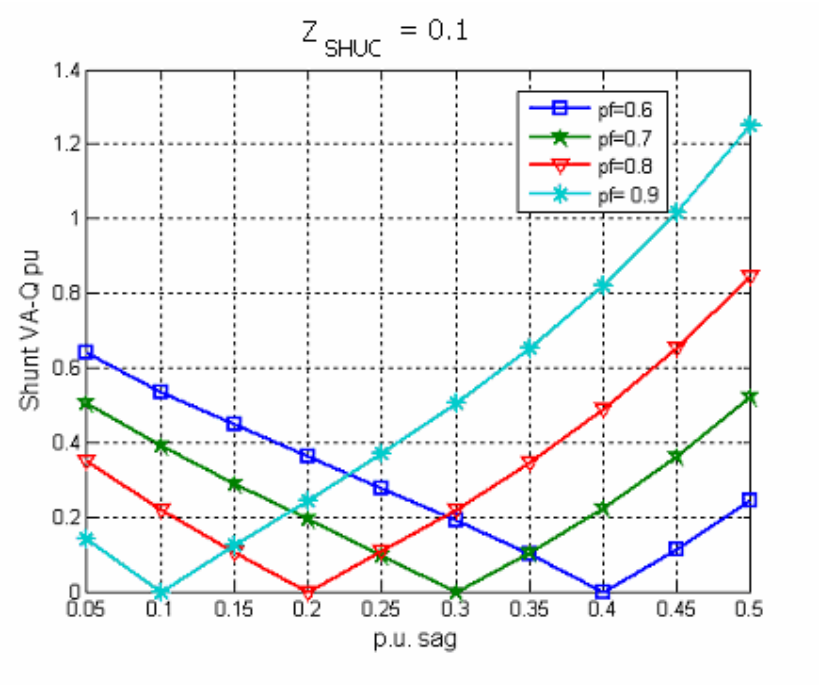

Fig.4 a Shunt VA loading of UPQC-Q

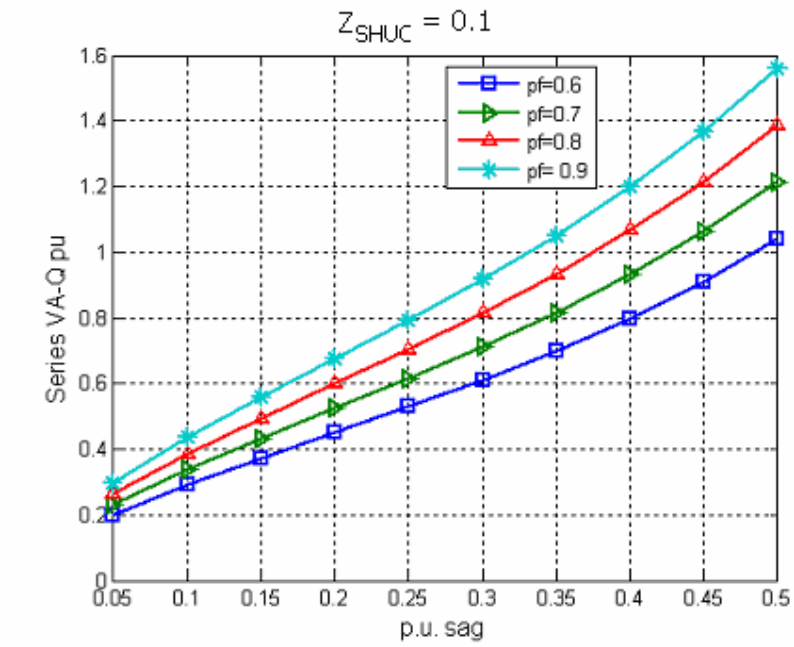

Fig.4 b Series VA loading of UPQC-Q

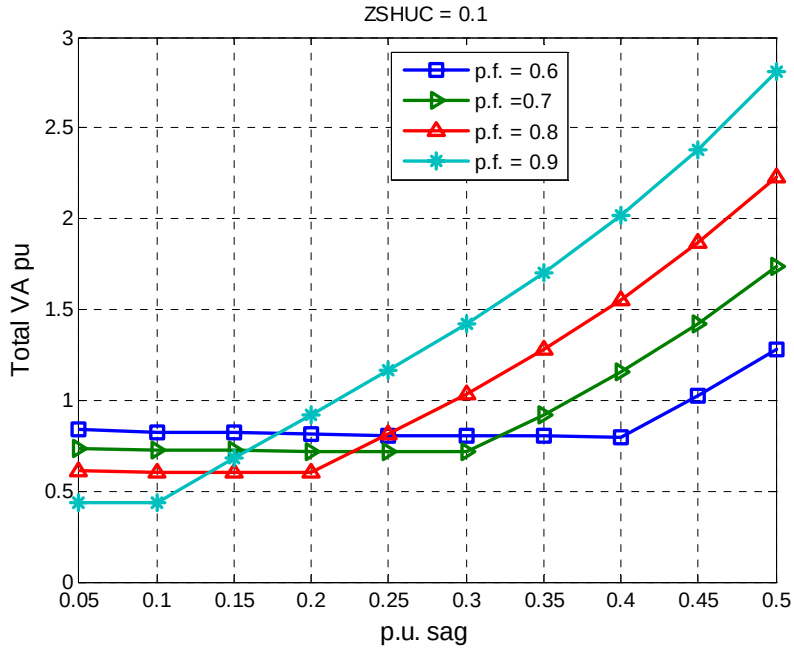

Fig.4 c Total VA loading of UPQC-Q

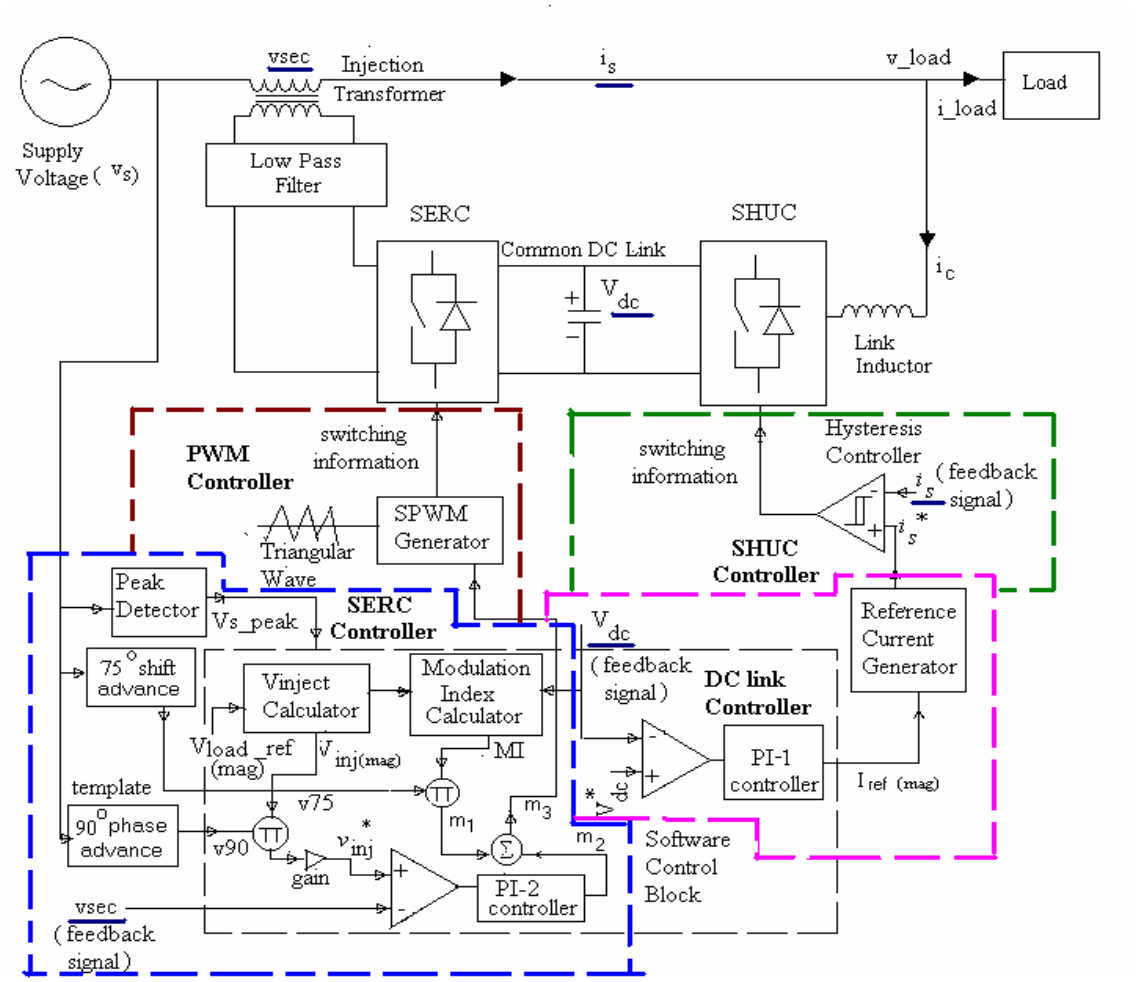

Fig. 5 Per phase control block diagram of UPQC-Q

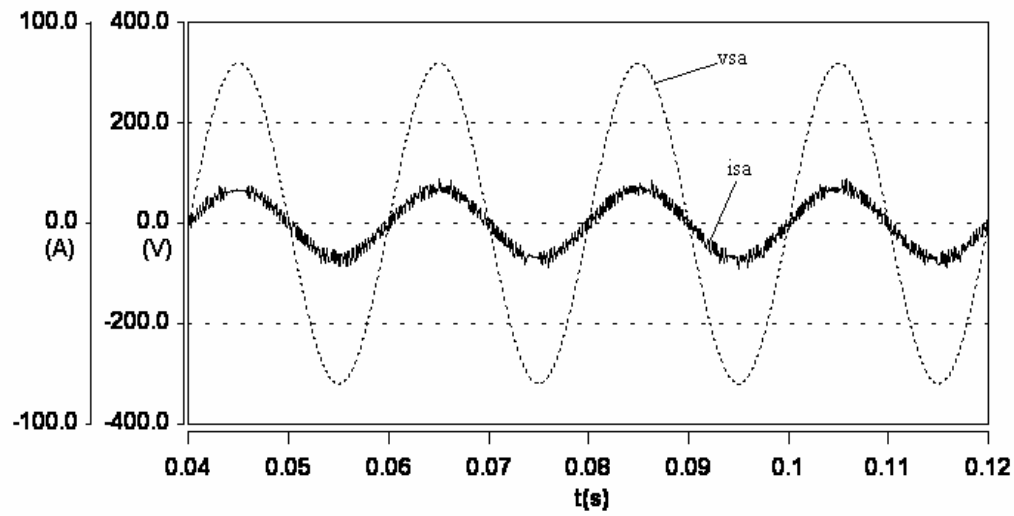

Fig.6a Steady state voltage (vsa) and current (isa) of supply phase A

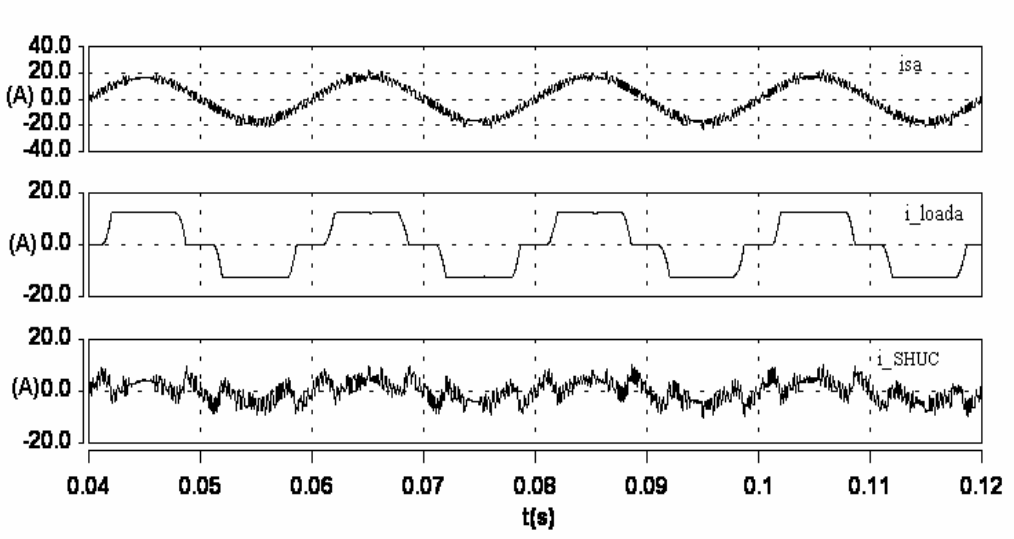

Fig. 6b Supply current (isa), load current (i_loada) and SHUCcurrent (i_SHUC) of phase A

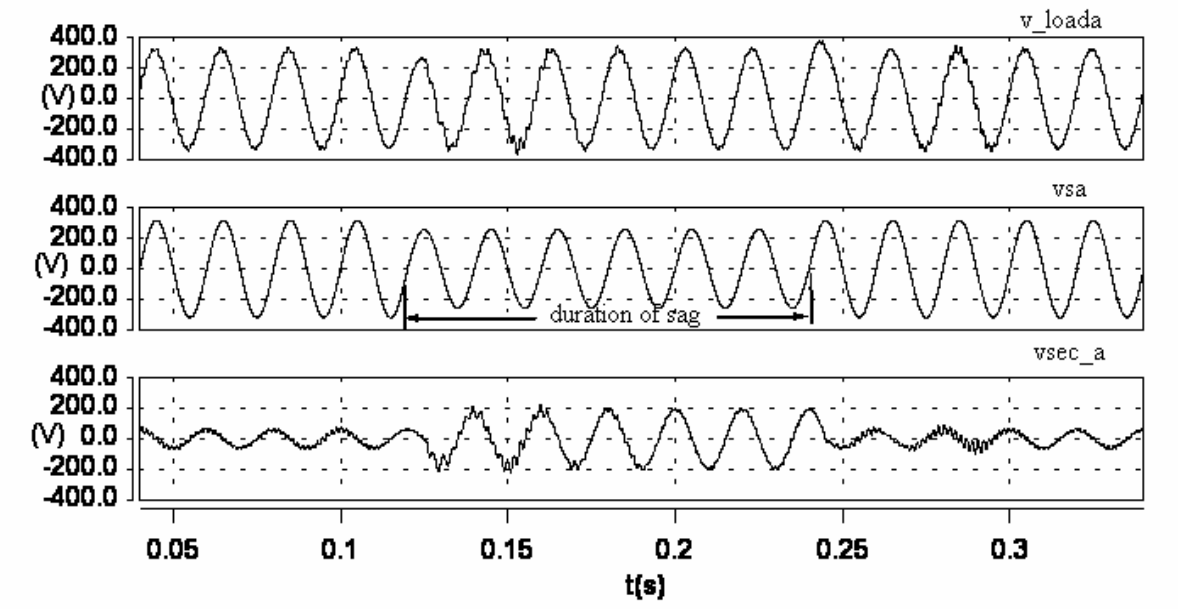

Fig. 7a Load voltage(v_loada), supply voltage (vsa) and injected voltage(v_seca) of phase A, under normal and 20% supply voltage sag condition

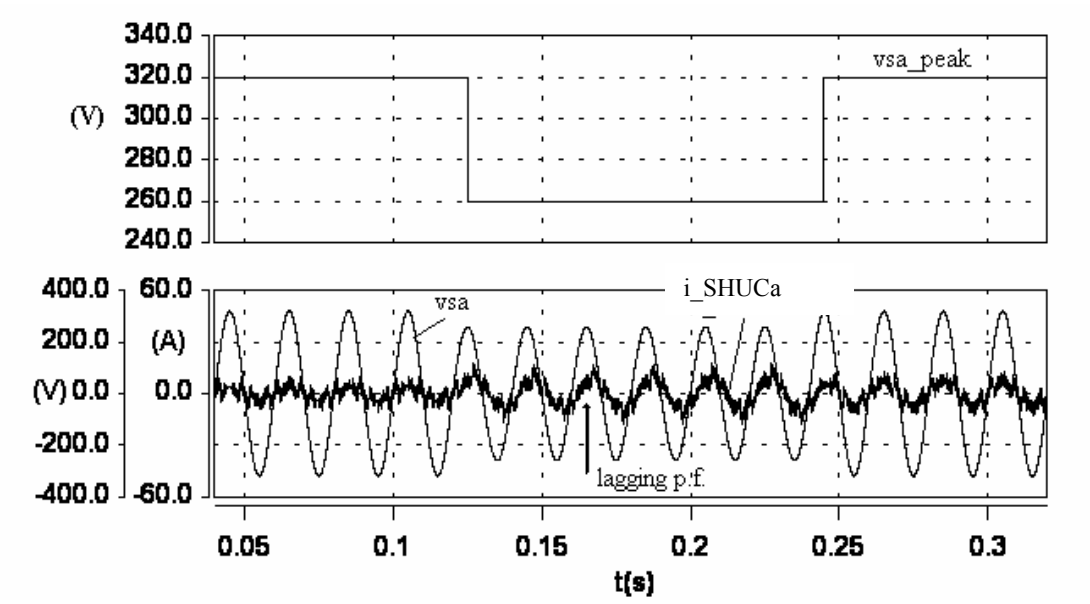

Fig.7b Peak of supply voltage (vsa_peak), SHUC current (i_SHUCa) and supply voltage (vsa) of phase A under normal and 20% sag condition

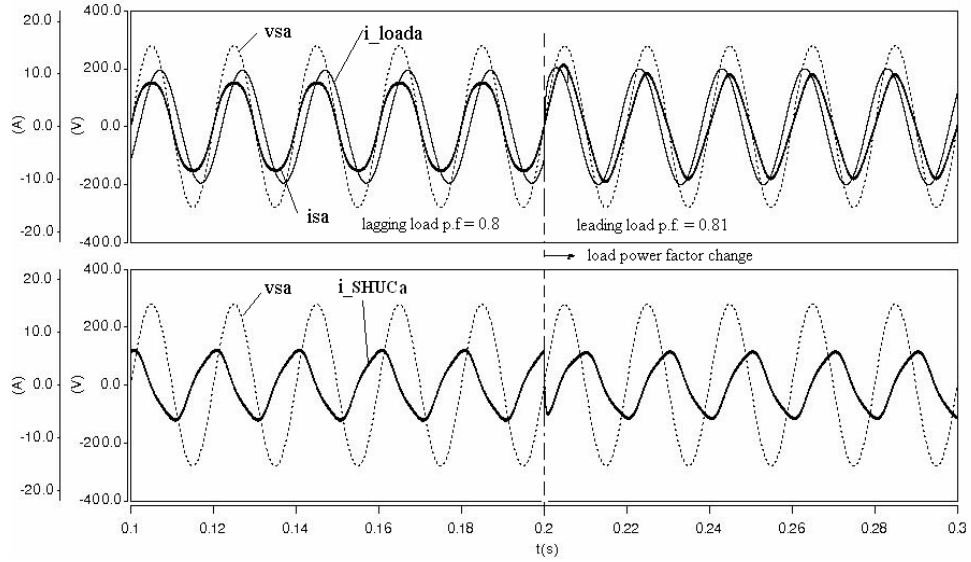

Fig. 8 Effect of load change from lagging p.f. = 0.8 to leading p.f. = 0.81

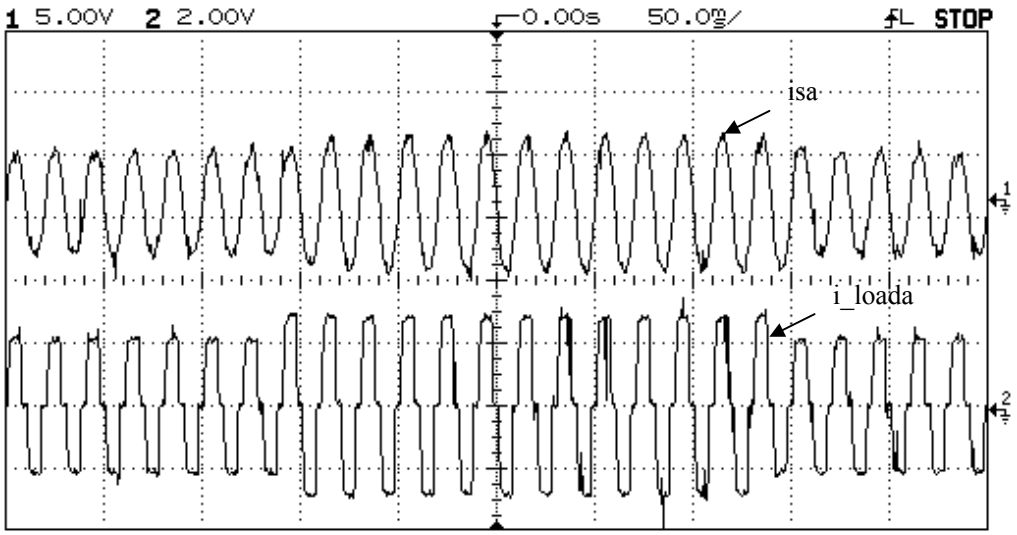

Fig. 9a Experimental results of supply current (isa)(5A/div), and load current (i_loada) (2A/div) of phase-A

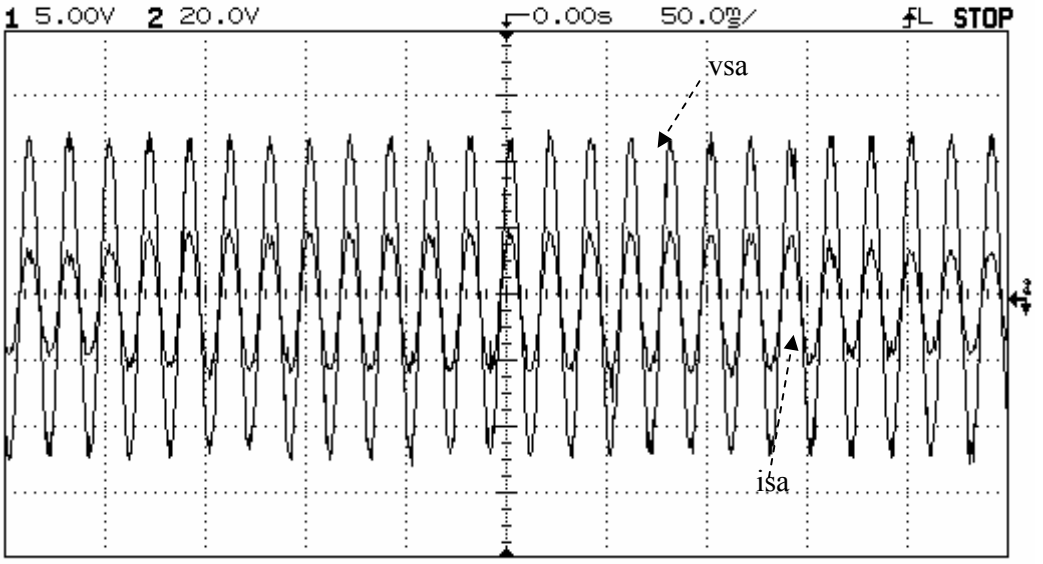

Fig. 9b Experimental results of supply current (isa)(5A/div) and supply voltage(vsa)(50V/div) of phase-A

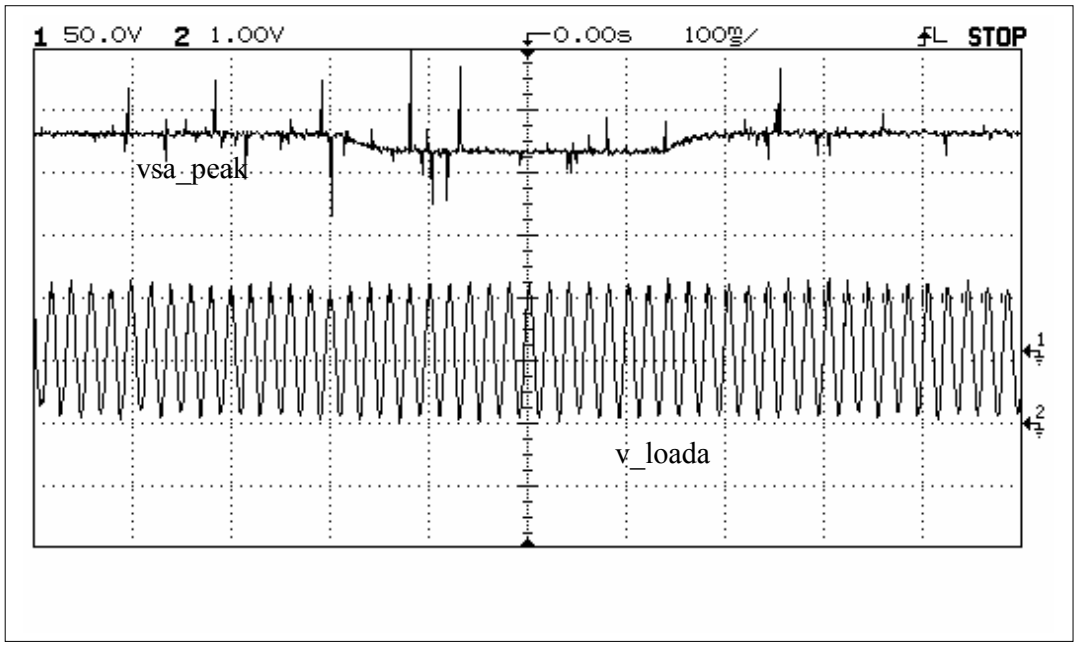

Fig. 10a Experimental result of peak of supply voltage (vsa_peak) and load voltage (v_loada) of phase-A, X axis: 100 ms/div, Y axis: 50 V/div for v_loada, 10.48 V/div for Vsa_peak

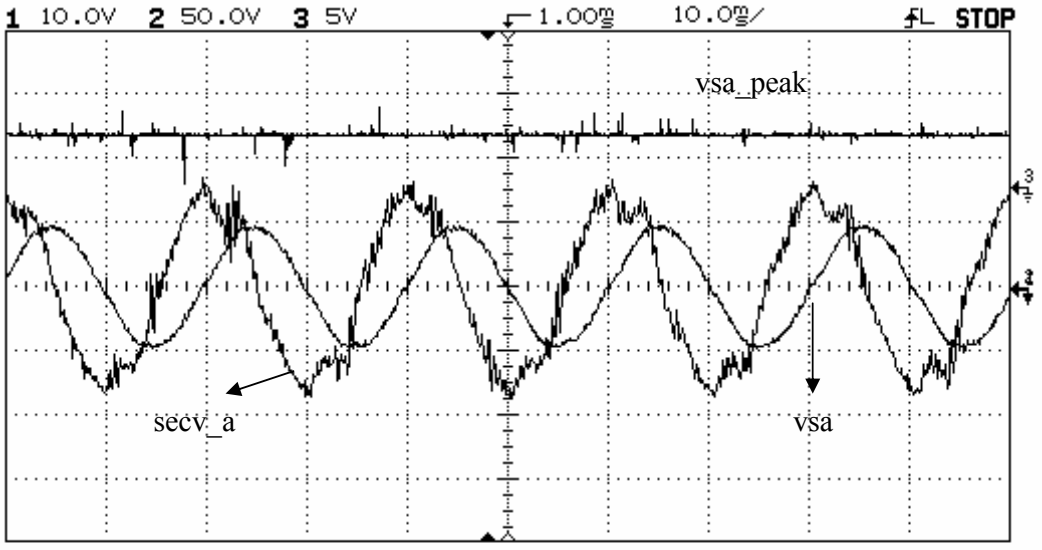

Fig. 10b Experimental result of peak of supply voltage and injected voltage and supply voltage of phase A, X axis: 10 ms/div, Y axis: 10 V/div for secv_a, 50 V/div for vsa, 52.4 V/div for Vsa_peak