2006-01-01

Protection of DVR against short circuit faults at the load side

Iurie Axente
Technological University Dublin

Malabika Basu
Technological University Dublin, mbasu@tudublin.ie

Michael Conlon
Technological University Dublin, michael.conlon@tudublin.ie

Kevin Gaughan
Technological University Dublin, Kevin.Gaughan@tudublin.ie

Recommended Citation

Axente, Lurie et al. :Protection of DVR against short circuit faults at the load side. 3rd. IET International Conference on Power Electronics, Machines and Drives, Dublin Ireland, 2006, pp.627-631. doi:10.21427/qay0-qc14

Protection of DVR against Short Circuit Faults at the Load Side

Iurie Axente, Malabika Basu, Michael F. Conlon and Kevin Gaughan

School of Control Systems and Electrical Engineering
Dublin Institute of Technology, Kevin Street, Dublin 8, Ireland

Keywords: Power quality, UPQC, DVR, Protection.

Abstract

An additional control scheme has been proposed in this paper for a dynamic voltage restorer (DVR), to protect it against load short circuit conditions. When overcurrents occur in the distribution system, under the proposed scheme the DVR reverses its injected voltage polarity so as to minimise the current flow. The detection method is based on impedance measurement feedback. The advantage of the scheme is that no additional over current device or protection is required for the DVR and it is easy to implement. The proposed control scheme has been validated through simulation.

1 Introduction

The Dynamic Voltage Restorer (DVR) is used to protect sensitive loads from sag/swell or disturbances in the supply voltage [1]. Another device, which is expected to be one of the most powerful solutions for power quality improvement is the Unified Power Quality Conditioner (UPQC). UPQC combines the operations of a shunt active filter and a DVR together. The series component of the UPQC (DVR) inserts a voltage so as to maintain the voltage at the load terminals balanced and free of distortion. This voltage is derived from a voltage source inverter (VSI) operated under pulse width modulation (PWM). Simultaneously, the shunt component of the UPQC injects current in the AC system such that the currents entering the bus to which the UPQC is connected are balanced sinusoids. In the case of a DVR, the active power injected in the series compensator is derived from a separate energy source.

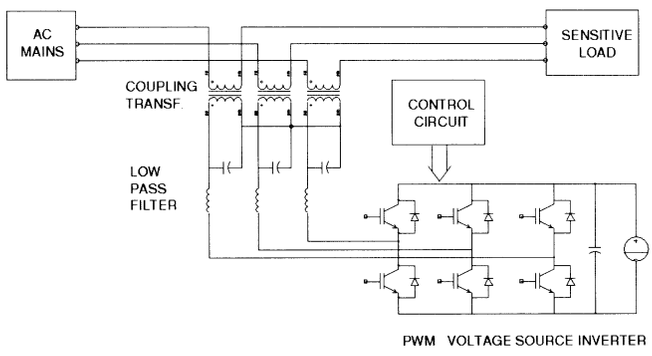

Figure 1: Dynamic Voltage Restorer Structure

This paper focuses on the protection of a series compensator associated with either a UPQC or a DVR. For the purposes of this paper, the DVR is investigated. The three-phase DVR structure is shown in Figure 1.

The DVR is connected in series with the electricity supply via transformer coupling to provide voltage support in the event of voltage sag/swell or disturbances from the supply side. This presents an imminent danger to the DVR when there is excess current flowing from the supply. Such a situation may arise due to several reasons but primarily as a result of short circuits at the load side. As the excessive current is also reflected in the secondary side of the transformer, the power semiconductor devices need to be protected.

One disadvantage of DVR and UPQC is that they require a special protection scheme [2]. The compensating voltage is injected in series with the source by means of the primary of the injection transformer. As noted in [3], the transformer operates as a current transformer and hence the secondary cannot be opened during a fault in the distribution system. Otherwise, excessive voltages would appear on the secondary side. Therefore the series compensator cannot be protected with circuit breakers or fuses. A failure to balance the mmf from the primary winding will cause the transformer to be driven into excessive magnetic saturation. Rather, a path must be provided for the flow of the referred (secondary) current. If the current flows through the VSI, the DC bus voltage will rapidly increase, even when the VSI is disabled [4].

As a path for the secondary current must be provided, the performance of varistors and other protection devices in parallel with the secondary of the series transformer have been investigated [3][4]. In the event of a fault in a distribution network, the fault is cleared after a duration, which is determined by the time delay imposed by the protection system. This delay in turn is determined by the response time of the switching devices and the requirements of the protection co-ordination. As noted in [3], total clearing time of a low-voltage circuit breaker depends on the amplitude of the current fault, but usually has a minimum value higher than 45 ms., whilst the minimum clearing time can exceed 100 ms. for medium-voltage applications. Thus, the duration of the fault is a significant parameter in relation to the ability of the inverter to withstand the fault but also with regard to the ability of the varistors to accommodate the excessive current. In general, the power electronic devices of

the series compensator will be the most vulnerable elements to system faults.

Additional protection hardware could be used, as proposed in [3], but this involves additional cost and energy dissipation. The scheme proposed in this paper involves an additional control function combined with the normal DVR operating scheme. The proposed protection scheme ensures that the devices are protected from excessive high current without additional circuit complexity. The basis of the scheme is that when an overcurrent occurs in the distribution system, the DVR reverses its injected voltage polarity so as to minimise the current flow. The detection method associated with the protection scheme is based on impedance measurement feedback. The proposed control scheme has been validated through simulation.

2 Simulation Model

The one-line diagram of the system under consideration and its parameters are shown in Figure 2. The 400 V (line-line) system has a fault level of approximately 1.2MVA. A three-phase load of 18 kW and 16 kVAr is supplied. The voltage at the load is regulated by a DVR which has a rated primary voltage of 230V and a secondary voltage of 130V. The parameters of the transformer are given in Table 1.

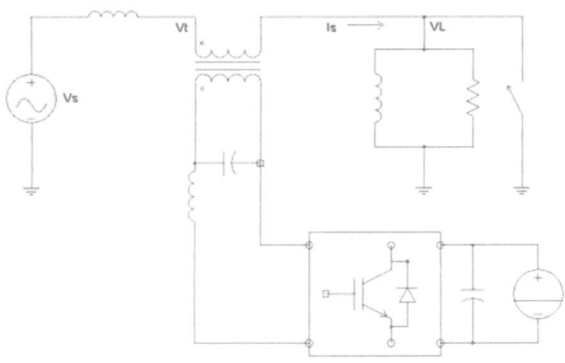

Figure 2: One-line diagram of system under consideration

Table 1: Transformer Parameters

Rating	8kVA	
Core Resistance	1470Ω	
Core inductance	1.86H	
	Primary	**Secondary**
Voltage	230V	130V
Winding resistance	0.474Ω	0.152Ω
Winding leakage inductance	0.904mH	0.288mH

The low pass filter has the following parameters: capacitor branch: R=0.01Ω and C=33 μF; inductance branch: R=0.02Ω and L=0.3 mH.

The simulation model was created in Simulink. The fault occurs at 0.1 s. and is cleared at 0.2 s. During the normal operation the DVR injects an appropriate voltage in series to maintain the load voltage V_L at the desired level. The fault is detected by measuring the impedance at the load side. During the normal operation the measured impedance is equal to the load impedance, which is quite a high value. When a short circuit occurs the impedance of faulted phase is approximately zero and this holds until the fault is cleared.

2.1 Fault Detection Technique

The fault detection control block measures instantaneously the load voltage and source current in each phase and determines their RMS values. Then the impedance is calculated for each cycle as follows:

$$Z_F = \frac{V_{L,RMS}}{I_{S,RMS}} \qquad (1)$$

and is compared with the preset impedance Z*, which is a system dependent constant. If Z_F is found to be less than Z* a short circuit fault condition is indicated. The DVR control then reverses its voltage polarity and applies an appropriate opposite voltage to that of the supply to reduce the supply current. In this way, during the fault, the voltage injected by the DVR opposes the supply voltage (providing that the DVR voltage rating is the same as the source voltage rating), and the voltage applied to the short circuit is approximately zero. The described above control strategy is shown in Figure 3.

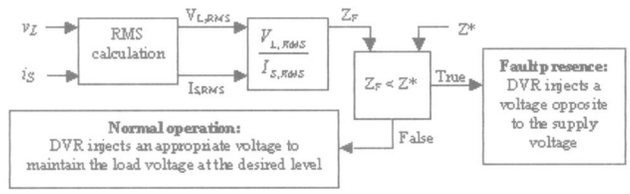

Figure 3: Control strategy

If the source current is chosen for the fault detection instead of impedance, then, as the control takes action (after fault detection) the source current decreases considerably (compared to the fault current) and the fault detection block would not "see" the fault in spite of its persistence. Because of this, during the fault the control action would be intermittent. The fault detection by impedance measuring does not suffer from this drawback.

2.2 Implementation of Simulation Model

The simulation model for the system under consideration was created using two different specialized software: Simulink and Saber. As simulations showed, Saber proved to have a smaller simulation time, especially when the simulation model includes inverters as each switching operation of the inverters is represented in the simulation. The Simulink simulation was carried out using controlled voltage sources rather than switching inverters and consequently the computational overhead was considerably reduced. Simulink also has an extensive component library, which makes the process of building the simulation model to be faster.

3 Analysis of Results

The simulations have been performed for two cases: a three-phase short-circuit and single-phase to ground short-circuit. The simulation results for three-phase short-circuit are shown in Figures 4-7, and for the single-phase to ground short-circuit they are presented in Figures 8-10. The fault occurs at 0.1 s. and it is cleared at 0.2 s.

During the normal operation the DVR injects an appropriate voltage in series to maintain the load voltage V_L at the desired level. When the fault occurs on the load side, the DVR reverses its voltage polarity and applies an appropriate opposite voltage to that of the supply to reduce the fault current.

Figure 4 shows the simulation result for the case where the secondary of the series transformer is short-circuited during the fault. As it can be seen from this result the supply current during the fault is as high as 260 A peak. The fault current in this case is 5 times higher than the load current, which is around 50 A peak. If the secondary of the series transformer is short-circuited using the anti-parallel thyristors, as it is proposed in [3], the thyristors have to withstand currents of quite a high value.

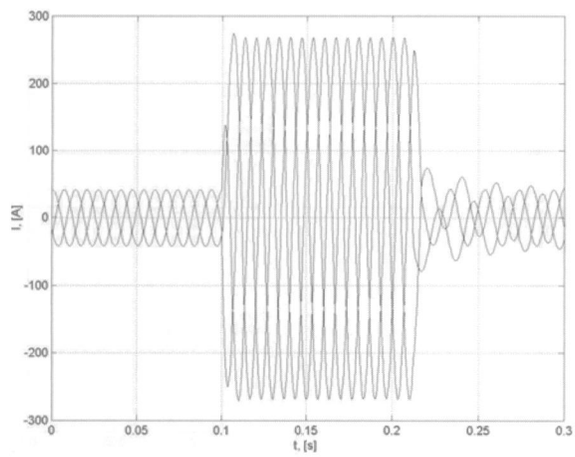

Figure 4: Source current when the secondary of the transformer is short-circuited during the fault (three-phase short-circuit)

Figure 5 shows the simulation result for the case where the control action described above is taken during the fault and the DVR injects a voltage opposite to that of the supply. The magnitude of the injected voltage is 50% of the supply voltage. Now, during the fault, the current is reduced from 260 to 115 A peak. Injecting 50% of the opposite supply voltage during the fault causes the source current to be reduced by a factor of 2.3. The fault current in this case is only two times higher than the load current. If we increase the magnitude of the injected voltage it is possible to get a fault current even smaller than the load current. Theoretically, injecting the voltage equal in magnitude to the supply voltage but of reversed polarity, it is possible to reduce the fault current to zero. As can be seen from Figure 5, during the first half cycle of the fault (0.1-0.11 s.) the current is somewhat higher than during the remaining duration of the fault (0.11-0.2 s). This is because the control action is not taken immediately after the short-circuit occurrence. The calculation of impedance takes some time (maximum one cycle) so that the fault occurrence is detected with some delay. For the same reason the fault clearing is also detected with some delay.

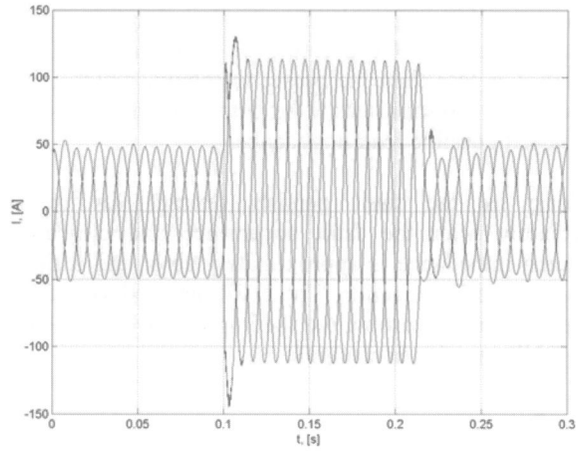

Figure 5: Source current when the DVR inserts 50% of source voltage (three-phase short-circuit)

In Figure 6 the voltage injected in series is shown. As we can see, during the normal operation only a small amount is injected, around 30 V peak. This small voltage is necessary to be injected during the normal operation in order to maintain the load voltage V_L at the desired level (230 V). During the fault, the DVR injects a voltage of around 110 V peak, which is opposite to the supply voltage.

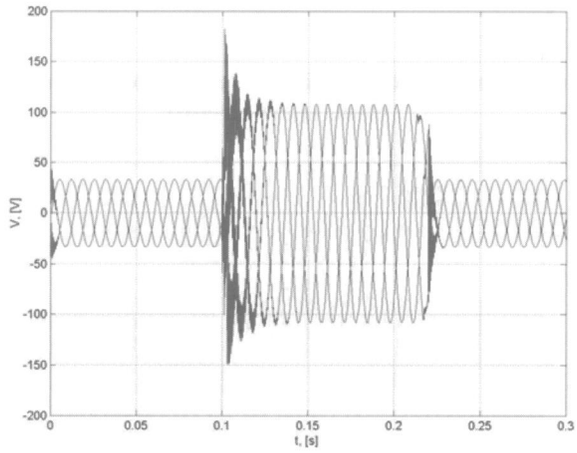

Figure 6: Voltage across the secondary (130 V) of the series transformer (three-phase short-circuit)

The impedance profile on the load side of the DVR is shown in Figure 7. At the beginning of the simulation there is some transient associated with the impedance calculation, which decays in one cycle. From the figure we can see that after one cycle the impedance is stable and it is equal to the load

impedance (6.6Ω). In order to avoid the incorrect control action during the first cycle when the calculated impedance is not stable, the control mechanism should start working only after one cycle. When the fault occurs (0.1 s) the impedance starts to decrease, and after one cycle it is approximately zero. The one cycle delay is due to the same reason discussed above (time associated with the impedance calculation). It is worth mentioning that even the transient associated with the impedance calculation lasts for one cycle the control takes action earlier than one cycle after the fault occurrence. This is because the control takes action as soon as the calculated impedance is less than the preset threshold, which is 6Ω in our case. The threshold has to be with some reserve less than the smallest possible load impedance.

As long as the fault persists (except for transients immediately after the fault occurrence and clearing) the calculated impedance is approximately zero, and it does not depend on the DVR action. The DVR action during the fault reduces the source current, but the impedance on the load side of the DVR remains unchanged.

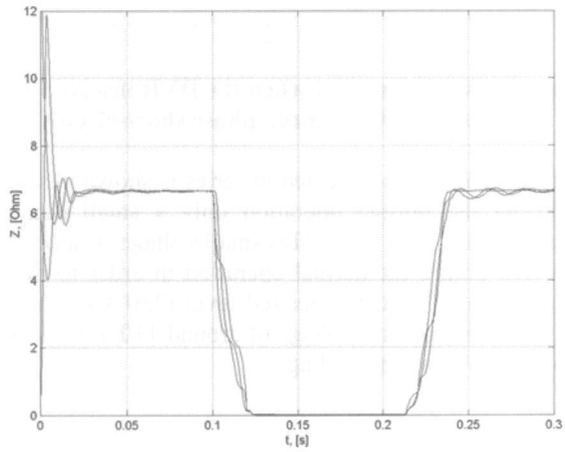

Figure 7: Impedance profile on load side of DVR (three-phase short-circuit)

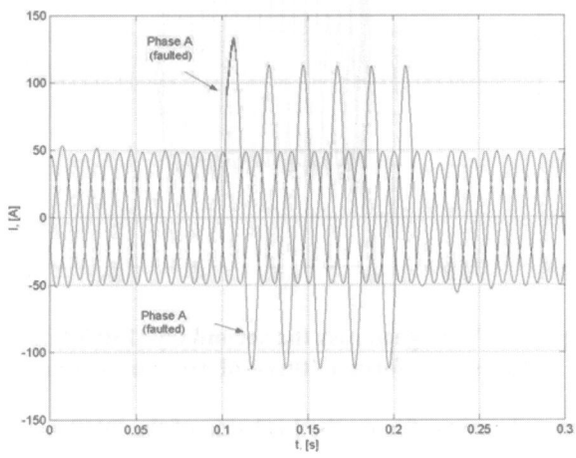

Figure 8: Source current when the DVR inserts 50% of opposite source voltage during the fault (single-phase to ground short-circuit)

In the case of a single-phase short-circuit, the DVR injects a voltage opposite to the source voltage during the fault but only in the faulted phase. This can bee seen from Figure 9. In phase A, which is faulted, the injected voltage during the fault is around 110 V peak. In the other two phases B and C, which are not faulted, the DVR injects just a small voltage for maintaining the load voltage at the desired level.

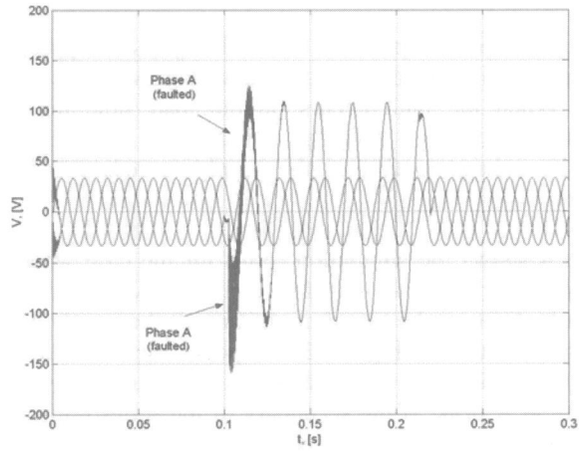

Figure 9: Voltage across the secondary (130 V) of the series transformer (single-phase to ground short-circuit)

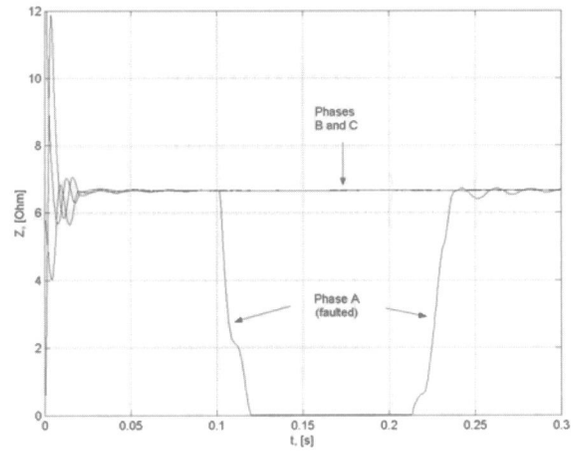

Figure 10: Impedance profile on load side of DVR (single-phase to ground short-circuit)

4 Conclusions

The DVR is connected in series with the distribution supply via transformer coupling to provide voltage support in the event of voltage sag/swell or disturbances from the supply side. This presents an imminent danger to the DVR when there is excess current flowing from the supply. Such a situation may arise due to several reasons but primarily as a result of short circuits at the load side. As the excessive current is also reflected in the secondary side of the transformer, the power semiconductor devices need to be protected.

The proposed protection scheme ensures that the devices are protected from excessive high current without additional circuit complexity. The basis of the scheme is that when an overcurrent occurs in the distribution system, the DVR reverses its injected voltage polarity so as to minimise the current flow. The detection method associated with the protection scheme is based on impedance measurement feedback. The proposed control scheme has been investigated through simulation.

The DVR protection must not interfere with the protection scheme of the power distribution system. Since the proposed DVR protection reduces the source current during the fault, in order to avoid the interference with the distribution system protection, it should be incorporated with the conventional fault protection.

Further work will involve a more detailed simulation of the protection scheme, incorporating a full representation of VSI series voltage supply. It is also proposed to investigate the performance of the scheme on an experimental prototype.

Acknowledgements

The authors gratefully acknowledge Enterprise Ireland for their sponsorship of the Unified Power Quality Conditioner project.

References

[1] Arindam Ghosh and Gerard Ledwich: *Power quality enhancement using custom power devices*, Boston: Kluwer Academic Publishers, 2002

[2] W-C Lee, T-K Lee, C-S Ma, D-S Hyun, "A Fault Protection Scheme for Series Active Compensators", Power Electronics Specialists Conference, 2002, Vol. 3, pp. 1217-1222

[3] L.A. Morán, I. Pastorini, J. Dixon and R. Wallace, "A Fault Protection Scheme for Series Active Power Filters", IEEE Trans. On Power Electronics, Vol. 14, No. 5, Sept. 1999, pp. 928-938

[4] M.J. Newman and D.G. Holmes, "An integrated approach for the protection of series injection inverters", Industry Applications Conference, 2001, Vol.2, pp. 871-878