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Investigation to Improve the Control and Operation of a Three-phase Photovoltaic Grid-tie Inverter

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MY WIFE

Abstract

Solar Energy or more precisely photovoltaic energy is one of the most promising sources of electricity for the future and it can be used as a distributed generator (DG) to play its role in 'smart grids of the future'. Distributed PV (photovoltaic) generators can provide numerous potential benefits such as augmenting the capacity of distribution systems, deferring capital investments on distribution and transmission (T&D) systems and improving power quality and system reliability. The PV energy which possesses very special I-V and P-V characteristics has to be conditioned by a PV inverter before it can be consumed by an ac load and/or the grid. Technical improvements in maximum power point tracking (MPPT) and islanding detection are proposed for a three-phase photovoltaic grid tied inverter (GTI) keeping in mind the requirements of the international standards for connecting a DG to the utility grid. This PhD thesis will contain four major sections which are briefed below.

A three phase GTI has been simulated using Matlab/Simulink to test the various control blocks and algorithms involved in the building of the power conditioning unit. A DS1104 dSpace DSP controlled, 5.625 kW three-phase GTI laboratory prototype has then been built. Various hardware components, including inverter switches, gate drivers, LCL filter, rectified dc source, boost circuit, transformer, 16A current protection circuit, additional sensing interface circuits and PWM level shifter have been designed and built within the laboratory. The software algorithm created in Simulink communicates directly with the built hardware via the graphical user interface that has been designed with dSPace Control Desk. Algorithms have been developed for the inverter in order to protect it from operating out of nominal frequency and voltage ranges. An algorithm has been developed

to ensure the boost dc link voltage is controlled to 300V when dc voltage source varies between 150V and 265V.

The Z-Source inverter (ZSI), with nine operating states that employs an extra shoot through (ST) state compared to the eight states (6 active and 2 zero states) in traditional VSI is one of the most recent boost topologies that has been proposed in the literature. A step by step design procedure of a ZSI has been developed. A topology comparison between Z-Source inverter and dc-dc boost with VSI is done using literature and simulations. Merits and demerits of the two topologies are summarised and the choice of the topology is justified.

MPPT is a process by which maximum power from a PV panel or array is tracked and absorbed during a particular weather condition (insolation level and temperature). There are various MPPT techniques in the literature which are reviewed and a new MPPT approach based on the P&O (Perturb and Observe) method is proposed. The proposed technique is tested on the three phase GTI simulation, it is analysed and compared to the conventionally reviewed P&O MPPT approach.

The issue of islanding of GTI's has raised concerns of equipment and personal safety, for which reason the inverter has to detect and stop the inverter during loss of grid. Passive techniques can detect the grid failure quite well when there is a large power mismatch between the DG and the load but not when the mismatch is small. Active techniques can work well with lower levels of power mismatch but they degrade power quality by introducing disturbances into the power system. A novel wavelet based anti-islanding technique is proposed and incorporated into the running hardware protection. This uses physical measurements to reduce the non-detection zone close to zero and keep the power quality of the inverter output unchanged. The developed algorithms have been validated in the laboratory prototype and yield very satisfactory performance.

Declaration

I certify that this thesis which I now submit for examination for the award of the Degree of Doctor of Philosophy, is entirely my own work and has not been taken from the work of others save and to the extent that such work has been cited and acknowledged within the text of my work.

This thesis was prepared according to the regulations for postgraduate study by research of the Dublin Institute of Technology and has not been submitted in whole or in part for an award in any other Institute or University.

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Signature _____ Date _____

Candidate

Acknowledgement

I take this opportunity to express my sincere gratitude to all those people who directly or indirectly helped me to carry out this research work successfully.

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List of Abbreviations

PV	Photovoltaic
T&D	Transmission and distribution
GTI	Grid-tie inverter
ZSI	Z-source inverter
VSI	Voltage source inverter
CSI	Current source inverter
MPP	Maximum power point
MPPT	Maximum power point tracking
ICT	Incremental conductance technique
P&O	Perturb and observe
CRV	Constant reference voltage
DSP	Digital signal processor
NDZ	Non-detection zone
DG/DER	Distributed generation/Distributed energy resource
PWM	Pulse width modulation/modulated
PCC	Point of common coupling
PLL	Phase lock loop
THD	Total harmonic distortion
GUI	Graphical user interface
ADC	Analogue to digital converter
ST	Shoot-through
CMR	Common mode rejection

OVP/UVP	Over/Under voltage protection
OFP/UFP	Over/Under frequency protection
SMS	Sliding mode frequency shift
AFD	Active frequency drift
SFS	Sandia frequency shift
DWT	Discrete wavelet transform
WBA	Wavelet based analysis
RMAC	Root mean absolute of wavelet coefficients
DRMAC	Difference in root mean absolute of wavelet coefficients
PCS/PCU	Power conditioning system/unit

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List of Symbols

V_{mpp}	Voltage at MPP
V_{PV}	PV operating voltage
I_{mpp}	Current at MPP
I_{PV}	PV operating current
V_{oc}	Open circuit voltage
I_{sc}	Short circuit current
V_{inv}	Inverter output voltage
I_{inv}	Inverter output current
P_{inv}	Inverter output power
V_g	Grid voltage
I_g	Grid current
P / P_{PV}	Active power
Q / Q_{PV}	Reactive power
V_a, V_b, V_c	Three phase voltages
I_a, I_b, I_c	Three phase currents
V_{dc}	DC link voltage
V_0 / V_{out}	Output voltage
V_i / V_{in}	Input voltage
P_{out}	Power output

I_{out}	Current output
V_r	Voltage ripple
D	Duty cycle
L, C, R, Z	Inductor, Capacitor, Resistor, Impedance
f / T	Frequency / Time
M	Modulation index
I_L	Inductor current
V_L	Inductor voltage
$T_0, \frac{T_0}{T}$	Shoot-through interval, Shoot through duty cycle
I_C	Capacitor current
V_C / V_{cap}	Capacitor voltage
V_d	Diode voltage
$\overline{\mathrm{V_L}}$	Average inductor voltage
$\hat{V}_{ac}$	Peak ac voltage
$\hat{I}_L, \check{I}_L$	Maximum inductor current, minimum inductor current
$\overline{I_L}$	Average inductor current
B	Boost factor
I_{ref}	AC current reference
P_k	Power at k^{th} sample
dP, dV	Differential power, differential voltage

$SW1, SW2$	Switch/circuit breaker 1, switch/circuit breaker 2
P_{Load}	Active power of load
Q_{Load}	Reactive power of load
ω_i	Islanding frequency
V_n	Nominal system voltage
ΔP	Active power difference
ΔP	Reactive power difference
X_n	Signal X with n samples
c_m	Scaling coefficient at level m (approximation)
d_m	Wavelet coefficient at level m(detail)
d_3	3rd level wavelet coefficient
E_p	Root mean absolute of coefficients (RMAC), $p \in$ {a, b, c}

Chapter 1

1. INTRODUCTION

1.0 General introduction

Recent developments in Photovoltaic technology have contributed towards lower cost, increased efficiency and better performance of PV panels over a wide range of temperatures. These positive gains coupled with deregulation as a driving thrust have resulted in a rapidly increasing number of non utility owned distributed PV powered generation plant/equipment operating in parallel with the utility.

The use of PV inverter integrated to the utility can provide numerous benefits to both utilities as well as customers [1]. From the utility perspective, some of the apparent advantages include distribution and transmission capacity relief, load peak shaving, deferral of high cost transmission and distribution (T&D) system upgrades. Utility customers also gain benefits from efficient use of energy from photovoltaics, enhanced power quality and reliability, tax incentives [1], [2].

Despite the benefits gained as described, PV grid connection has many technical challenges that remain to be tackled. Requirements for grid integration of DG are discussed in IEEE Std 929-2000 [3], IEEE Std. 1547 [4] and EN50438 [5].

Photovoltaic (PV) cells which are usually made of semiconductor material generate low output dc voltage (current) and have a nonlinear I-V / P-V characteristic. These cells are connected in series and parallel to form a module, and several of these modules are combined to form a panel which finally forms an array of panels [6].

In order to power the utility, the PV panels require power electronic converters to condition this varying dc voltage to the grid. Each of these power electronic converters in an inverter system can comprise of a dc-ac converter, boosting circuit, maximum power point tracker (MPPT) and filtering circuit linking the dc source to the local load and grid as shown on Figure 1.1. Figure 1.1 shows the proposed configuration of a three-phase photovoltaic inverter connected to the utility grid.

The boost stage of the inverter is usually incorporated to connect panels that cannot independently produce the minimum required dc link voltage (i.e. for the inverter to produce the required ac grid voltage). Control of this dc link voltage is crucial in order to obtain a smooth ac output. Various techniques and control methods are used to force the PV panel(s) to operate at its maximum power point (mpp) at all times by utilizing an algorithm called maximum power point tracker (MPPT) . The MPPT employs maximum power transfer theory by keeping the impedance presented by the inverter bridge system close to the internal impedance of the PV Panel(s).

One of the most serious issues in grid connected systems is the islanding phenomenon. Islanding is a situation in which a portion of the distribution system is intentionally or accidentally isolated from the utility grid. It is energized by the local power generation without control and/or supervision of the utility. This phenomenon can result in a number of potential hazards to the customer's equipment and in particular to any maintenance personnel who attempt to service the energised feeder.

1.1 Focus of research

The focus of this research work is to investigate the major parts of a three phase grid connected photovoltaic inverter system and to test the performance of the proposed improvements (see Section 1.2 for research contributions) which can be demonstrated in simulation and experimentally.

In order to carry out the study the following objectives were laid out.

- Literature survey dealing with: photovoltaic characteristic, PWM techniques, boost and inverter topology, control of grid connected inverter, maximum power point tracking, inverter output filter, islanding protection, interfacing circuits and DSP control.
- Development of simulation models for the two boost topologies and detail research study on operation, control and design of a ZSI.
- Simulation of full three-phase grid connected inverter system using PV characteristic and MPPT.
- Testing of the proposed MPPT algorithm using simulation (discussed in Chapter 4).
- Construction of 5.625 kW grid connected inverter prototype (main blocks of the system, interface circuits and cabinet with instrument panel)
- Design of software control algorithms using the DSP and development of a user interactive interface.
- Interaction of both software and hardware to produce successful test results.
- Testing of the proposed anti-islanding algorithm in simulation and hardware experiments (discussed in Chapter 6).

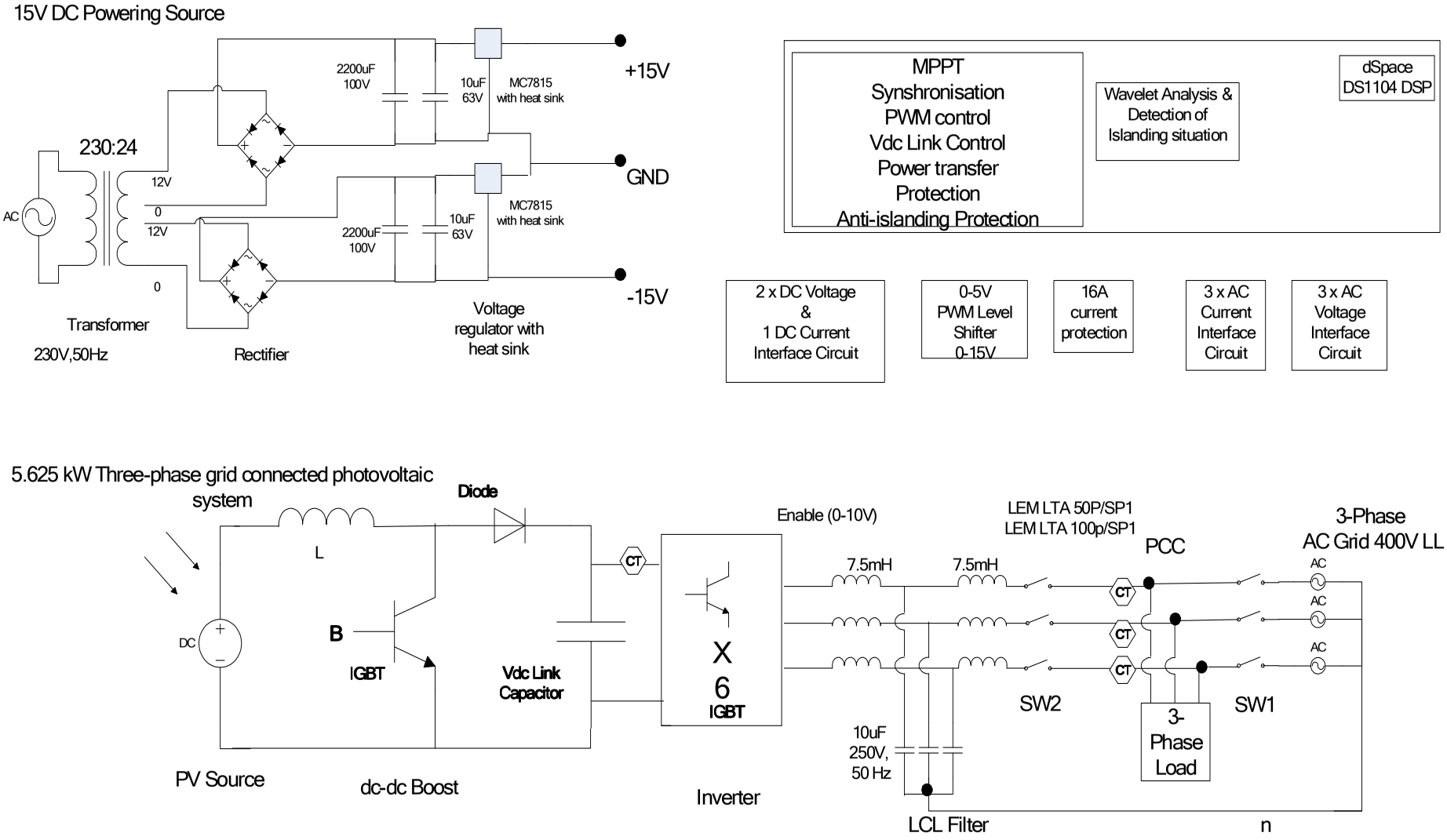


Figure 1. 1: Block diagram of the proposed grid-tie inverter

1.2 Research contribution

1. An extensive topology comparison is done between conventional voltage source inverters (VSI) that employ a dc-dc boost circuit and recently proposed Z-Source inverters (ZSI). This comparison looks at the relative complexity of circuits, the relative complexity of control and the relative efficiency of both methods in order to compare their suitability for photovoltaic grid connected applications. As part of this work a step by step design procedure for a ZSI has been developed.

2. A new MPPT approach that uses the perturb and observe (P&O) method is proposed, simulated, analysed and compared to the conventionally reviewed P&O MPPT approach. The proposed P&O method does not require any voltage and current measurements on the PV side of the inverter.

3. A 5.625 kW three-phase grid connected inverter with a rectified dc source (instead of PV, due to laboratory limitations) has been built. Necessary interface circuits have been designed and built for the hardware prototype to communicate with the software that is run on the dSpace DS1104 DSP control board. Algorithms have been developed for the inverter, in order to protect it from operating beyond nominal frequency and voltage ranges. An algorithm has been developed to regulate the boost dc link voltage at 300V.

4. A novel islanding detection technique has been proposed which employs wavelet based analysis to evaluate the high frequency components introduced by the pulse

width modulator in the dc-ac inverter. This new passive technique will keep the output power quality unchanged unlike other active methods used for detection and will reduce the non-detection zone(NDZ) to near zero unlike other passive methods.

1.3 Organization of the thesis

This research thesis is divided into seven Chapters. The literature review and background for each of the sections is discussed within their respective Chapters. The Chapters are organised as below:

Chapter 2: Three-phase photovoltaic grid connected inverter

This Chapter details the design and simulation studies carried out on the grid connected system in general. It covers PV characteristics, power transfer theory, and control of ac current and ac voltage using PWM techniques. The synchronization process and the control of the dc link voltage are explained. Standards for distributed generation (DG) interaction are investigated and analysed. A full PV system simulated in Simulink with simulation results is presented and discussed. The choice of DSP controller for the final hardware implementation is justified.

Chapter 3: Topology comparison between Z-Source inverter and dc-dc boost with voltage source inverter

The Chapter reports the investigation carried out on the boost topologies for a grid connected inverter system. DC-DC boost being the most common boost topology discussed in the literature is compared with the newer Z Source inverter. DC-DC boost

structure and control, ZSI structure, ZSI equations and shoot through control are discussed. A step by step design procedure of a ZSI has been developed. The choice of the topology used for this development is justified.

Chapter 4: New maximum power point tracking approach based on perturb and observe method

This Chapter discusses the existing MPPT methods utilized to track the maximum power of a PV panel. There are various MPPT techniques in literature of which most reliable and commonly used are ICT (incremental conductance technique) and P&O (perturb and observe). A new MPPT approach based on the P&O method is proposed. Simulated results are compared to the conventional P&O MPPT approach.

Chapter 5: Implementation of the three-phase grid connected inverter: hardware, software and control

This Chapter looks at the main hardware blocks required to develop the grid connected inverter prototype and the necessary design calculations are presented. It also details the design of the interface circuits that are required by the dSpace DSP to communicate with the hardware. Details of development of the interface circuits are presented with simulation results from Spice. Results of the hardware implementation of the circuits are presented and compared with the simulations. Simulink is used to simulate the grid connected system and this Simulink program is adjusted with the relevant blocks from the 'dSpace block set' to run on real hardware. A flow chart of the program identifying the various algorithms to control the inverter voltage, boosted dc link, PWM switching

and inverter protection is given. A user interface designed with the Control Desk software that is linked to the Simulink program is shown. Experimental results of the laboratory prototype under the control of DS1104 are produced to validate both the hardware construction and the software implementation, and their interaction.

Chapter 6: Novel anti-islanding technique proposed using wavelet analysis

This Chapter discusses islanding of grid connected inverters and the current passive and active methods used to detect island formation. It analyses the importance of power mismatch in detecting grid failure soon after an island is formed. A new anti-islanding technique is proposed and incorporated into the protection scheme of the operating hardware prototype. It uses physical measurements to reduce the non-detection zone almost to zero while keeping the power quality of the inverter output unchanged. A flow chart of the proposed algorithm is given along with simulation and experimental results that compare the simulation and experimental results.

Chapter 7: Conclusion and future work

Chapter 7 summarises the main findings of this research and discusses possible further research extensions based on the research carried out in this thesis.

Chapter 2

2. THREE PHASE PHOTOVOLTAIC GRID CONNECTED INVERTER

2.0 Introduction

The Chapter details the background and literature for PV characteristic, power transfer theory, control of ac current and ac voltage using PWM techniques. The synchronization process and control of dc link voltage is explained along with a control flow chart of the simulation model. Various standards for distributed generation (DG) interaction with the grid are considered. A full PV grid connected system model is simulated in Simulink and simulation results are provided. The choice of DSP control board to use with the final prototype is justified.

2.1 Photovoltaic source

The photovoltaic source characteristic is studied so that a dc source that represents PV characteristic can be simulated. This section will detail the main sections and terms related to PV. The I-V characteristic of a solar cell is similar to that of an inverted diode characteristic and follows the general shape and equation shown below:

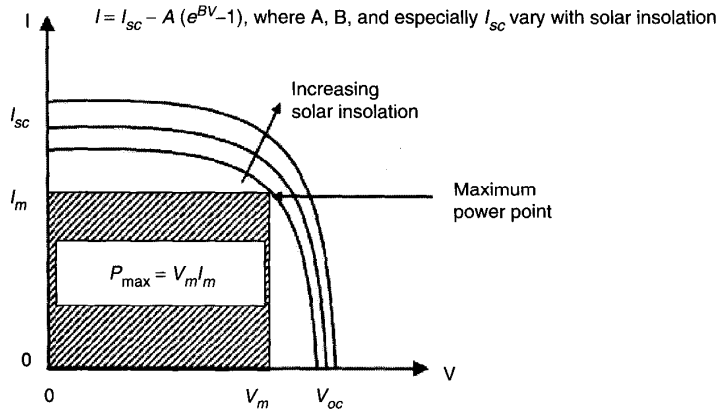


Figure 2. 1: I-V curve of a solar cell [7]-[14]

The FF (Fill Factor) describes how "square" the I-V curve is,

$$FF = (V_{mpp} \cdot I_{mpp} / V_{oc} \cdot I_{sc}) \tag{2. 1}$$

The simplified equivalent circuit for a solar cell is a current source in parallel with a diode as shown below:

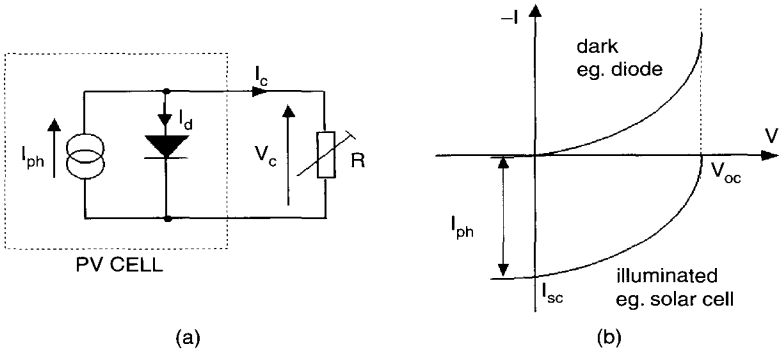


Figure 2. 2: (a) Solar cell equivalent circuit, (b) Inverted diode characteristic

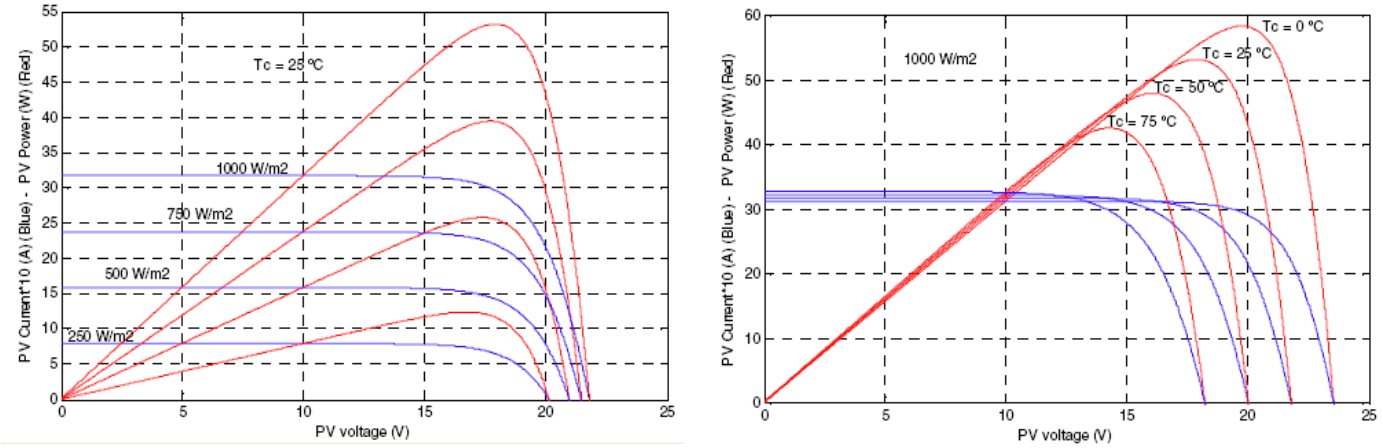
The variable resistor acts as a load. The voltage/current relationship is given by the diode equation [7], [8]:

$$I = I_{ph} - I_0(e^{qV/kT} - 1) = I_{ph} - I_d \tag{2. 2}$$

Where: q = electron charge, k = Boltzmann constant, I_{ph} = photocurrent, I_0 = reverse saturation current, I_d = diode current, T = the solar cell operating temperature (^{o}K).

Figure 2.3 shows P-V and I-V characteristics of the PV module BP350U [15]. The P-V curves below show that the power increases with voltage until it reaches its peak value and falls down as the resistance increases, causing the current to drop-off. This peak power point is called the Maximum Power Point (MPP).

Insolation is a measure of solar radiation energy received on a given surface area in a given time, for photovoltaic panels: kWh / (kWp.y) (kilowatt hours per year per peak rating) [9], [10].



(a) (b)

Figure 2. 3: (a) PV panel insolation characteristic (b) PV panel temperature characteristic [15]

The two Figures 2.3(a) and 2.3(b) show how the MPP point varies with insolation level and temperature respectively. When the insolation level increases, short circuit current increases linearly and the open circuit voltage increases logarithmically [2].

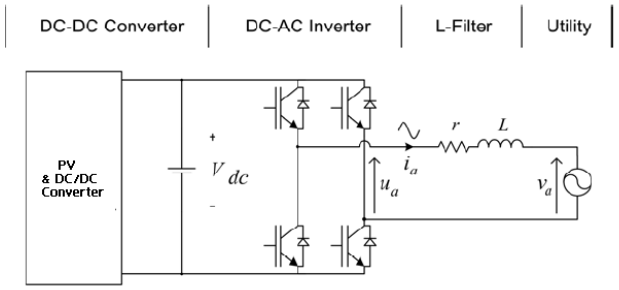
With increase in temperature, the open circuit voltage decreases and the short circuit current increases slightly, thus making the cell less efficient.

2.2 Maximum power point tracker

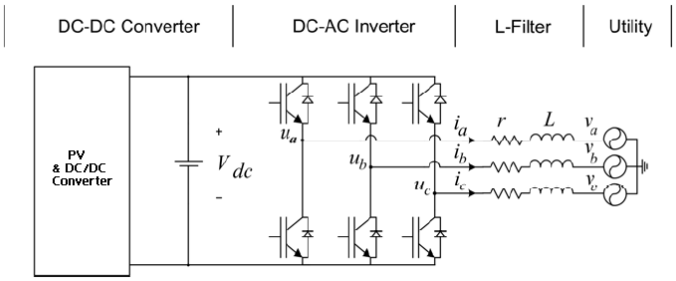
For maximum power transfer, the load should be matched to the resistance of the PV panel at MPP. Therefore, to operate the PV panels at its MPP, the system should be able to match the load automatically and also change the orientation of the PV panel to track the Sun if possible (Sun tracking is usually left out of most systems due to the high cost of producing the mechanical tracker). A control system that controls the voltage or current to achieve maximum power is needed. This is achieved using a MPPT algorithm to track the maximum power together with a dc-dc converter circuit that is used to transfer this tracked power [10]-[14]. A detail review of the MPPT techniques is given in Chapter 4 of this thesis.

Figure 2.4 shows system integration of PV inverter system which comprises of a PV panel, associated with a dc-dc converter and a widely used dc-ac pulse width modulation (PWM) inverter connected to the utility grid.

A single phase PV power conditioning system is often selected for low power applications (< 3 kW) i.e., residential applications. For higher power applications i.e., commercial or industrial applications, a three-phase PV power conditioning system is preferable.



(a)System integration of single phase PV power conditioning system



(b) System integration of three phase PV power conditioning system

Figure 2. 4: System integration of PV power conditioning system

2.3 Inverter control types

Voltage control and current control are two types of waveform generation control schemes used for grid-connected inverters. PV inverters inject energy directly into the grid and are controlled as power sources ie. they inject “constant” power into the grid at close to unity power factor. The control system constantly monitors power extracted from the PV array and adjusts the magnitude and phase of the ac voltage (in voltage control mode) or current (in current control mode) to export the power extracted from the PV array.

2.3.1 Voltage control

A voltage controlled inverter produces a sinusoidal voltage at the output. It can be used in standalone operation supplying a local load. If non-linear loads are connected within the rating of the inverter, the inverter's output voltage remains sinusoidal and supplies non sinusoidal current as demanded by the load. Since it is a voltage controlled source it cannot be directly connected to the grid and therefore it is connected via an inductance. The inverter voltage may be controlled in magnitude and phase with respect to the grid voltage. The inverter voltage is usually controlled by controlling the modulation index and this controls the reactive power. The phase angle of the inverter may be controlled with respect to the grid which controls the active power.

2.3.2 Current control

A current controlled inverter produces a sinusoidal current at output. It is only used for injection into the grid and not for stand alone applications. The output is generated using a sinusoidal reference which is phase locked to the grid voltage. The output stage is switched so that the output current follows the generated sinusoidal reference. The reference waveform may be varied in amplitude and phase with respect to the grid and the output current automatically follows the reference. The output current waveform is ideally not influenced by the grid voltage waveform quality and always produces a sinusoidal current. The current controlled inverter is inherently current-limited because the current is tightly controlled even if the output is short circuited.

2.4 Power transfer theory

To understand the power flow from the PV source (PV panel and the inverter) to the grid in a grid connected system, basic power flow theory was studied. The power flow between two ac sources as shown in Figure 2.5 is analyzed.

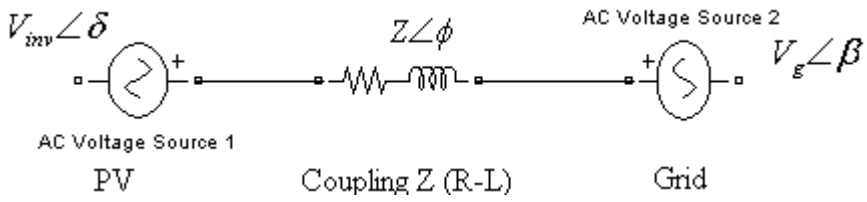


Figure 2. 5: Power flow between two AC sources

The diagram above shows two power sources coupled with an impedance of $Z = R + jX$ whose

$$|Z| = \sqrt{R^2 + X^2}$$

$$\phi = \tan^{-1}\left(\frac{X}{R}\right)$$

Source 1 and source 2 represent the PV source and the grid respectively.

Source 1 is identified with $V_{inv}\angle\delta$ and source 2 with $V_g\angle\beta$, where V represents the rms voltage and the angle represents the phase reference.

If power flows from source 1 to source 2 through the coupling Z, the current flow I, can be defined as: $I = \frac{V_{inv}\angle\delta - V_g\angle\beta}{R + jX} = \frac{V_{inv}\angle\delta - V_g\angle\beta}{Z\angle\phi}$, (2. 3)

Using $S = VI^*$ we get:

$$S = V_{inv}\angle\delta\left(\frac{V_{inv}\angle\delta - V_g\angle\beta}{Z\angle\phi}\right)^* \quad (2.\ 4)$$

$$S = \frac{V_{inv} V_{inv} \angle(\delta - \delta) - V_{inv} V_g \angle(\delta - \beta)}{Z \angle - \phi} \tag{2. 5}$$

$$S = \frac{V_{inv}{}^2}{Z} \angle \phi - \frac{V_{inv} V_g}{Z} \angle(\delta - \beta + \phi) \tag{2. 6}$$

$$S = \frac{V_{inv}{}^2}{Z} \cos\phi + j \frac{V_{inv}{}^2}{Z} \sin\phi - \frac{V_{inv} V_g}{Z} \cos(\delta - \beta + \phi) - j \frac{V_{inv} V_g}{Z} \sin(\delta - \beta + \phi) \tag{2. 7}$$

$$S = \frac{V_{inv}{}^2}{Z} \cos\phi - \frac{V_{inv} V_g}{Z} \cos(\delta - \beta + \phi) + j \left(\frac{V_{inv}{}^2}{Z} \sin\phi - \frac{V_{inv} V_g}{Z} \sin(\delta - \beta + \phi) \right) \tag{2. 8}$$

$$\mathrm{Re}[S] = P = \frac{V_{inv}{}^2}{Z} \cos\phi - \frac{V_{inv} V_g}{Z} \cos(\delta - \beta + \phi) \tag{2. 9}$$

$$\mathrm{Im}[S] = Q = \frac{V_{inv}{}^2}{Z} \sin\phi - \frac{V_{inv} V_g}{Z} \sin(\delta - \beta + \phi) \tag{2. 10}$$

2.4.1 Real power flow

Now considering (2.9), if the phase reference β, for Source 2 (grid) is taken as the reference ($\beta = 0$), we get:

$$P = \frac{V_{inv}{}^2}{Z} \cos\phi - \frac{V_{inv} V_g}{Z} \cos(\delta + \phi) \tag{2. 11}$$

And if we assume R is very small, only inductive coupling is used in Z,

$R \approx 0$, $\phi \approx 90^o$ $Z \approx jX$

$$P = \frac{V_{inv}{}^2}{X}\cos 90 - \frac{V_{inv}V_g}{X}\cos(\delta + 90) \tag{2. 12}$$

$$P = \frac{V_{inv}V_g}{X}\sin\delta \tag{2. 13}$$

2.4.2 Reactive power flow

Considering (2.10) and assuming phase reference $\beta = 0$, $R \approx 0$, $\phi \approx 90^o$ and $Z \approx jX$

We have:

$$Q = \frac{V_{inv}{}^2}{X} - \frac{V_{inv}V_g}{X}\sin(\delta + 90) \tag{2. 14}$$

$$Q = \frac{V_{inv}{}^2}{X} - \frac{V_{inv}V_g}{X}\cos\delta \tag{2. 15}$$

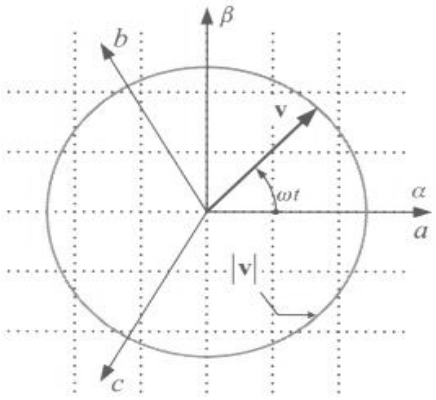
$$Q = \frac{V_{inv}}{X}\left(V_{inv} - V_g\cos\delta\right) \tag{2. 16}$$

Since $V_g\angle 0$ represents the grid of $230\angle 0$ (230V rms and 0 phase reference) and X is of fixed value, using the above analysis and the simulation results it was found that when R is close to 0, the loss across R is very small, and the power transfer depends as follows:

- Real power mainly depends on δ
- Reactive power mainly depends on V_{inv} (rms voltage of Source 1) [16]

2.5 Synchronization and control of three phase grid connected inverter system

One of the most important and necessary features of a power converter connected to electric utility grid is proper synchronization with the three-phase voltages in a three phase system. The synchronization methods used for three-phase systems are more complex than in single phase systems due to the relationship of phase shift and phase sequence of the coordinated three phase voltages. Figure 2.6 shows the voltage vector describing a circular locus on a Cartesian plane, generally referred to as the α-β plane. The modulus and the rotational speed of the three phase voltage vector are maintained constant when balanced sinusoidal waveforms are present in the three-phase system.



$$V_{abc} = \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = V \begin{bmatrix} \cos(\omega t + \phi) \\ \cos(\omega t - \frac{2\pi}{3} + \phi) \\ \cos(\omega t + \frac{2\pi}{3} + \phi) \end{bmatrix}$$

Figure 2. 6: Ideal three-phase voltage vector

Non-idealities in power system can originate disturbances giving rise to undesirable effects on electrical equipment such as resonances, increasing power losses, pre-mature aging. Voltage disturbances may cause sensitive grid-connected power converters to lose controllability and adequate protection should be incorporated to prevent the destruction of the power converter. In case of voltage vectors at point of common coupling (PCC) being distorted by high order harmonics, the detection system should cancel out the effect of these harmonics by reducing the bandwidth of the system [10]. Having

protected from harmonic voltages, unbalanced voltages are going to trouble the synchronization process, which needs attention. In case of unbalanced voltages, sequence components of the unbalanced voltages are identified by using special techniques, and this balanced sequence component information is passed to the inputs of the controller. Moreover, three-phase power converters used with PV are expected to inject positive-sequence current at fundamental frequency into the grid and only deliberately inject negative-sequence and harmonic currents in abnormal cases, depending on the purpose of the converter [10]. Therefore, grid synchronization of a three phase system requires an advanced detection system designed to reject both higher order harmonics and detect the sequence components in a quick and accurate manner.

Phase locked loops (PLL) are employed in order to track the angular frequency and phase shift of the three phase voltages [1] or more precisely positive-sequence components of the three-phase voltages, for synchronization. Various advanced PLL techniques have been proposed in literature but a simple and easy to implement software based, three-phase discrete PLL is used on the extracted positive sequence of the three-phase voltages. The PLL is capable of synchronizing the inverter well to the grid, in order to test the proposed ideas (goals).

2.6 Symmetrical components

In 1918, C.L Fortescue proposed a method for analyzing unbalanced polyphase networks, which can be applied to three-phase systems and is known as symmetrical components. The symmetrical components method decomposes the steady state phasors of an unbalanced three-phase system into a set of balanced sequence components,

namely the positive, the negative and the zero sequence components [10]. The transformation that can be applied to both the currents and voltages is given in (2.17).

$$\begin{bmatrix} i_0, v_0 \\ i_1, v_1 \\ i_2, v_2 \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} i_a, v_a \\ i_b, v_b \\ i_c, v_c \end{bmatrix} \tag{2. 17}$$

where a is e^{j120^o} and terms 0,1,2 subscripts are zero, positive and negative sequence components, respectively.

The discrete three-phase PLL used in the simulation and the final software (run on the prototype) extracts the positive sequence components before processing to retrieve the ωt information.

2.7 Voltage source inverter

The type of inverter to be used in the power conditioning unit for this study was selected to be a VSI. This type of inverter was selected not only because of the readily available power electronics building block (PEBB) based inverter system, but also because of the type of control systems to be implemented. The VSI is controlled in voltage mode using well known pulse width modulated (PWM) switching technique described in detail in [2], [17]. The three-phase inverter comprises of three legs of two IGBT switches each. The three top switches are enabled using three generated PWM pulses and the bottom switches are enabled using the complementary of three generated PWM pulses. To avoid the shorting of a single leg, a dead band needs to be incorporated between the top and bottom PWM pulses of the same leg.

2.7.1 Generation of PWM pulses

PWM is generated using Sine Triangle PWM. For simulation purposes, due to the high frequency of the carrier (20 kHz), a much higher sampling frequency (125 kHz or 8μs) is chosen to run the simulation which reduces the speed of execution badly. This is not the case for actual implementation as the dSPace PWM Block is used to run the real hardware which is discussed in Chapter 5. In Sine Triangle PWM, in order to produce the output voltage of desired magnitude waveform, phase shift and frequency, the desired signal is compared with a carrier (triangular waveform signal) of higher frequency to generate appropriate switching signals (shown in Figure 2.7). The dc link capacitor is alternately connected to the inverter outputs with positive and negative polarity. When the switches are closed at t_{on}, the voltage time averaging over one carrier wave begins. Control of t_{on} and t_{off} is achieved by comparing the modulating voltage with the carrier voltage. When the magnitude of the carrier voltage exceeds the magnitude of the modulating voltage, one of the active switches is opened to end any contribution to the time average voltage. Similar triangles on the control plot of voltage vs. time show that $\frac{T}{T_s} = \frac{V_{carrier} - V_{modulation}}{V_{carrier}}$. The average voltage at any time is:

$$V_{average} = \frac{T_s - T}{T_s} \times \frac{V_{dc}}{2} = \frac{V_{modulation}}{V_{carrier}} \times \frac{V_{dc}}{2} = M \frac{V_{dc}}{2} \qquad (2.18)$$

where the modulation index, M, varies with time to synthesize the average voltage. If the average voltage were plotted, it would look like the modulating voltage waveform (inverter sine output).

The output voltage of the VSI does not have the shape of the desired signal, but switching harmonics, can be filtered out by the series LCL low pass filter, to retrieve the 50Hz fundamental sine wave (desired average voltage as explained).

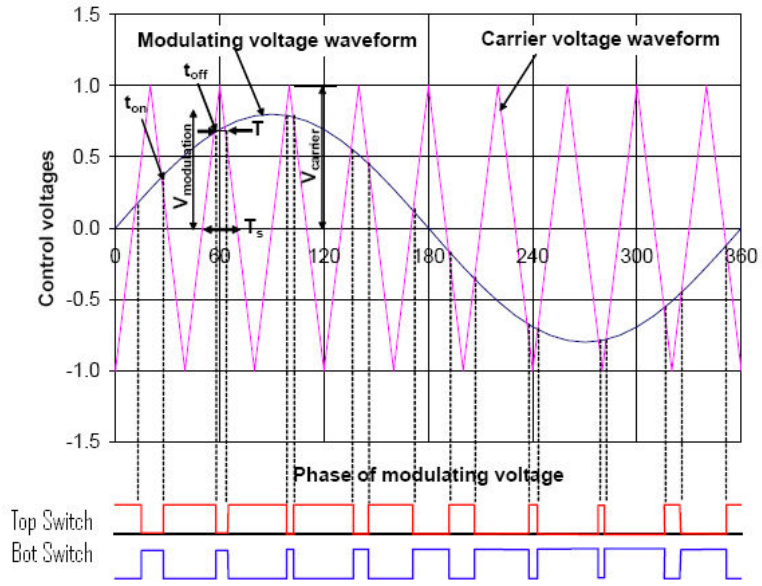


Figure 2. 7: Showing (1 of the 3 Phases) one phase of control voltage waveforms to modulate pulse widths

2.8 Management of dc link voltage

The dc voltage input is subjected to variation depending on the power extracted from the photovoltaic source (or dc source), i.e. the point where the load line meets the I-V characteristic of the PV. The dc link voltage is also subjected to variation depending on the power available and the amount of power extracted. The increase of power results in voltage overshoot and decrease in power results in voltage undershoot at the dc link. Either way control of dc link voltage is compensated by a charging and discharging process.

The control of dc link voltage is either achieved by:

1) Controlling the exchanged power between the inverter and grid
2) Using a voltage controlled dc-dc converter

In the simulation model, PV is simulated within the grid connected system. When PV is used, the boost stage (dc-dc converter) is used for boosting and MPPT. Therefore the dc link voltage level is increased or decreased by injecting less or more power respectively, into the grid. The injection of power into the grid is controlled by changing of the ac reference current that changes the ac voltage amplitude and phase displacement across the LCL filter. When a dc voltage source instead of PV is used, the dc link voltage is increased or decreased by increasing or decreasing the boost duty cycle and a user defined ac current reference (in real-time) is taken into the controller to transfer the required power.

In both cases the ac current reference, impedance of LCL filter, dc link voltage and the grid voltage are used in calculating the ac voltage output references of the inverter. Sine triangle PWM (as explained above) is then used to generate the switching pulses. Usually a PI (proportional and integral) controller needs to be properly tuned to generate the 'ac current reference' for case 1 (see control flow chart in Figure 2.15) and to generate the 'boost duty cycle' for case 2 (see control flow chart in Figure 5.23 of Chapter 5). The error between the actual dc link voltage and the reference dc link voltage is used as the input to the PI controller. To achieve the goals of this research work, the dc link voltage control is done using an embedded Matlab function discussed in Chapter 4 and 5, which maintains the dc link voltage well, as required.

As part of the literature study, the importance of grid impedance was also understood. Knowing the grid impedance helps in designing the size of coupling inductor (in order to reduce the size of added inductance). Also in the literature, continuous detection in change of grid impedance is used to identify the situation when islanding occurs (impedance jump within a particular time interval). Further according to [18], it is said that the stability of the current controller is affected by large varying impedance. Many methods in the literature used for grid detection are based on injecting a certain perturbation at a particular frequency (that is assumed to be absent in the grid voltage). Then calculating the impedance (sensing the V and I at that frequency by applying Fourier analysis on output parameters), and then predicting the impedance at 50Hz line frequency [18], [19], [20].

2.9 Standards for micro generation in the Republic of Ireland

EN 50438 is the main standard followed by ESB (the dominant local energy supplier) and Eirgrid (the Irish Transmission System Operator) in Ireland. EN50438 [5] and the following standards are considered as guidelines during the design process of the power conditioning unit (PCU) and control thereof:

- ANSI/IEEE C84.1 – 1995, [21]
- IEEE 519 – 1992, [22]
- IEEE 929 – 2000, [3]
- IEEE 1547 – 2003, [4]
- UL 1741, [23]

These standards provide guidelines and specifications for the interconnection and control of DERs (distributed energy resources) to the utility grid. The following are brief summaries of each standard:

ANSI/IEEE C84.1 – 1995 standard deals with common line voltages at different distributions levels (i.e. residential power is single phase and an RMS voltage of 240 V, whereas some commercial sites have three phase, with an RMS voltage of 240 V).

IEEE 519 – 1992 are recommended practices and requirements for the harmonic control of electrical power systems. It sets maximum Total Harmonic Distortion (THD) limits on voltages and currents that a power system is allowed; therefore the power conditioning unit (PCS) cannot inject harmonics into the grid that cause the system to go above these

limits set forth by the standard, and if at all possible, the PCS should filter these harmonics [22].

IEEE 929 – 2000 are recommended practices for the utility interface of photovoltaic (PV) systems. Though written for PV inverters, the guidelines and specifications can be adapted to be used for an inverter connecting a DER to the utility.

IEEE 1547 – 2003 is the standard for the interconnection of distributed resources to the utility grid. This standard outlines requirements and specifications that the conversion systems of the DER have to meet to be allowed to connect to the utility. This standard does not deal with the concepts and issues of intentional islanding, and currently dictates that the DER shall disconnect from the distribution system when islanding events occur. As noted above, the standard does leave a section open for consideration of intentional islanding in future revisions of the standard. An analysis of 1547 raising questions to issues proposed by it can be found in [4].

UL 1741 is the Underwriters Laboratories' testing standards for equipment as they relate to IEEE 1547.

A document from ESB (Irish electricity supplier) in support of utility connected micro generation states that [24]:

"Micro-generation is defined as a source of electrical energy and all associated equipment, rated up to and including

- 25A at low voltage [230V], when the DSO network connection is single-phase
- 16A at low voltage [230/400V], when the DSO network connection is three-phase"

All installed Micro-Generators must comply with EN 50438 with the specific Irish protection settings [24].

EN50438 provides requirements relevant to the performance, operation, safety consideration, testing, and maintenance of interconnection. Summary of essential interconnection technical specifications and requirements are given in Table 2.1.

Table 2. 1: Micro-generation interface settings for the Republic of Ireland as published in EN50438

Parameter	**Trip Setting**	**Clearance time**
Over voltage	230 V + 10%	0.5 s
Under voltage	230 V -10%	0.5 s
Over frequency	50 Hz + 1%	0.5 s
Under frequency	50 Hz - 4%	0.5 s

The document states the standard for Loss of Mains (LoM) protection, automatic reconnection after network outage and synchronization as follows:

Loss of Mains (LoM)

LoM protection shall use rate of change of frequency or vector shift methods. The trip setting shall ensure the micro generator stops energizing within the prescribed clearance time irrespective of where, on ESB's network the interruption takes place. This requirement is deemed to be satisfied by passing the test in Section 6.4 of the document [24]. Operation of LoM interface protection at any given site shall not in and of itself, disturb or cause spurious operation of LoM interface protection at any other site [24].

Automatic reconnection after a network outage

The interface protection shall ensure that feeding power to the ESB's network will only commence, after the voltage and frequency on the ESB's network, have been within the limits of the interface protection settings for a minimum of

– 3 min for mechanical ac generation;

– 20 s for inverter based systems.

In order to facilitate such automatic reconnection power input to the interface protection equipment and sensing connections to the interface protection shall be made on the ESB Networks side of the disconnector (but on the micro-generator side of the isolator) that is initiated by the interface micro-generator protection. Manufacturers should give consideration to limiting the number of attempted reconnections within any one period of time [24].

Synchronization

The operation of synchronizing a micro-generator with the DSO's network shall be fully automatic i.e. it shall not be possible to manually close the switch between the two systems to carry out synchronization [24].

2.10 Modelling of three phase grid connected photovoltaic inverter

The whole three phase grid connected photovoltaic inverter system shown in Figure 1.1 of Chapter one, is modelled in Simulink with embedded Matlab codes where necessary. The simulation model is used to get a better understanding of all the subsystems and their interaction with each other. It eases the process of design and implementation of the prototype in a safe environment before building the final product.

2.10.1 Simulink

Simulink is a software package for modeling, simulating, and analyzing dynamic systems. It supports linear and nonlinear systems, modeled in continuous time, sampled time, or a hybrid of the two. Systems can also be multi rate, i.e., have different parts that are sampled or updated at different rates (this feature is used to run different controls at different speeds).

For modeling, Simulink provides a graphical user interface (GUI) for building models as block diagrams, using click-and-drag mouse operations. With this interface, one can draw the models just as one would with pencil and paper (or as most textbooks depict them).

Simulink includes a comprehensive block library of sinks, sources, linear and nonlinear components, and connectors.

One can also customize and create one's own block. Models can be hierarchical, and this approach provides insight into how a model is organized and how its parts interact. The graphical Simulink interface runs on an underlying MATLAB engine. After one defines a model, one can simulate it, using a choice of integration methods, either from the Simulink menus or by entering commands in MATLAB's command window.

The menus are particularly convenient for interactive work, while the command-line approach is very useful for running a batch of simulations (for example, if one is doing Monte Carlo simulations or want to sweep a parameter across a range of values). Using scopes and other display blocks, one can see the simulation results while the simulation is running. In addition, one can change parameters and immediately see what happens, for "what if" exploration. The simulation results can be put in the MATLAB workspace for post processing and visualization. Because MATLAB and Simulink are integrated, one can simulate, analyze, and revise one's models in either environment at any point.

Figure 2.8 below shows a screen shot of MATLAB and Simulink environment with the Sim Power Systems tool box open.

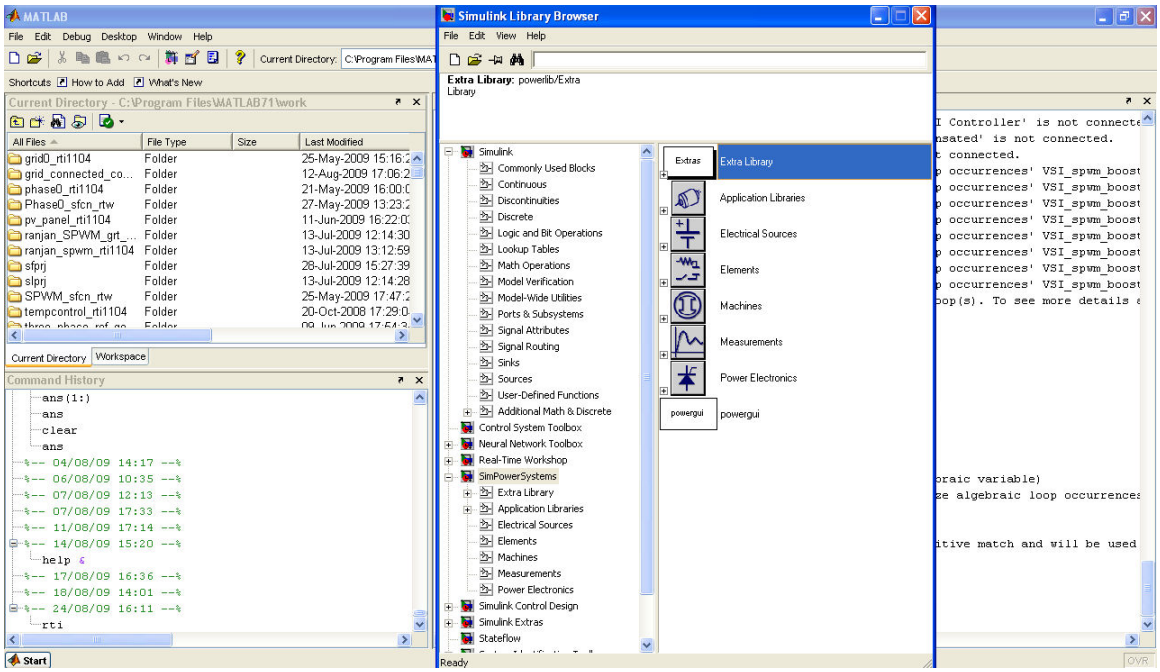


Figure 2. 8: Screen shot of MATLAB & Simulink environment

Each component is modelled and evaluated on its own, to check if it gives the expected output, before it fits into the main simulation system. Most of the blocks are built with components available in the 'Sim Power Systems' toolbox and using some of the standard Simulink components along with the dSpace library. A few embedded Matlab control blocks are created by writing Matlab codes according to the user requirements. Some subsystems that require slower sampling rate are enabled using a different slower enable switching pulse. The sections below discuss most of the major simulation blocks and their design parameters used in our simulation model. A full control program for the Simulink model is presented in Figure 2.15. The Simulink model developed is shown in Appendix 1.

2.10.2 The PV model

A PV characteristic behaves almost like a current source at the left side of the maximum power point (MPP). To the left of the maximum power point (MPP) power is most strongly determined by voltage variation. On the right hand side of the MPP the PV behaves like a voltage source and power is determined by the variation of current. This is shown in Figure 2.9[16].

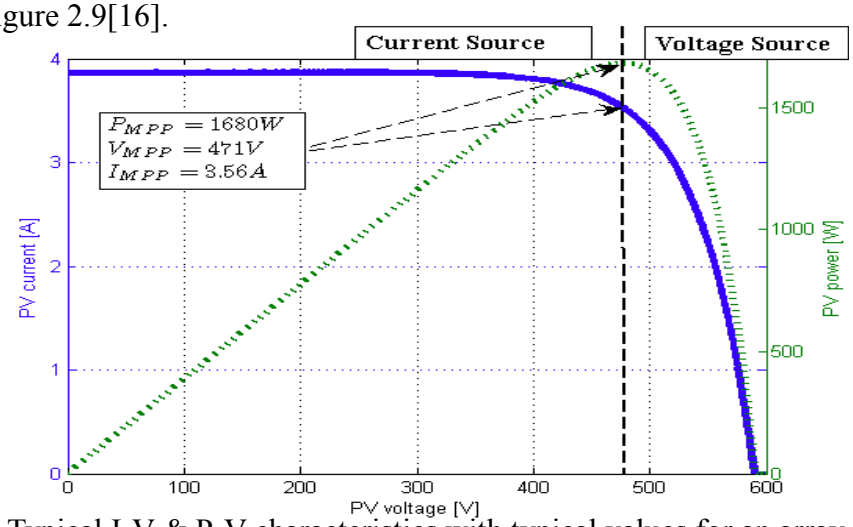


Figure 2. 9: Typical I-V & P-V characteristics with typical values for an array [16]

This special characteristic curve which can reach a maximum power point of 1680W (1.7 kW) shown in Figure 2.9 is used in simulations to create a working model of a PV panel.

A current controlled source is used in the model as PV is a current source. The output voltage of this source is measured and passed through a transfer function to average out the voltage fluctuations. This voltage is passed through a look up table which represents the PV curve of 1680W which is shown in the Figure 2.10. A current corresponding to the measured voltage is sent to the current source in order to output the exact power corresponding to the operating point on the PV curve. A large resistor is added in parallel

to run the simulation without which algebraic problems occur. A few different PV curves including 1680W, 3400W and 6800W have been developed for simulation purposes.

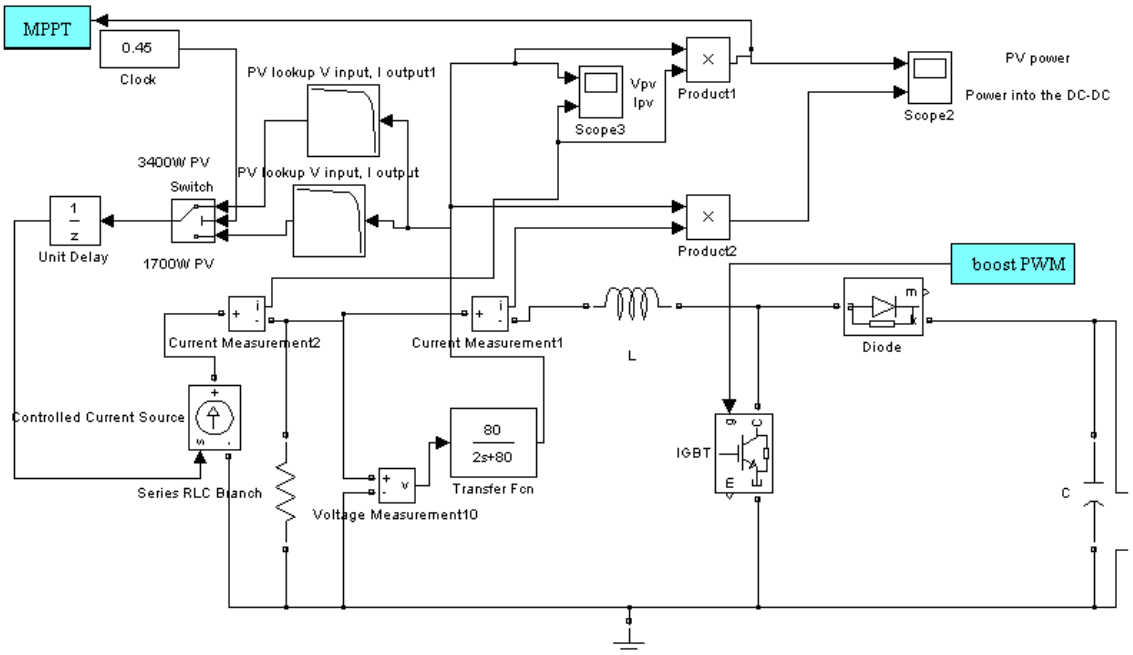


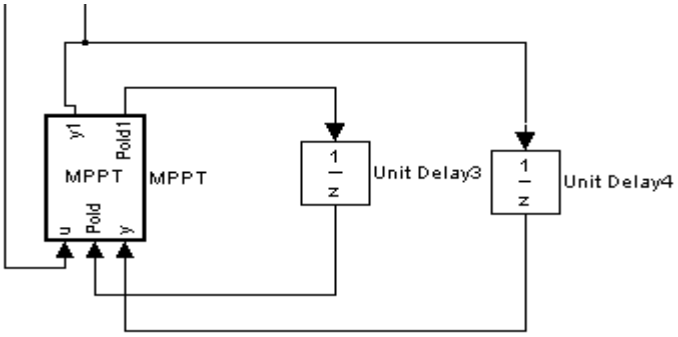
Figure 2. 10: PV model designed in Simulink.

2.10.3 MPPT control block

The MPPT block shown in Figure 2.11 is an Embedded Matlab Function designed to track the operating point by measuring the output power from the PV model. The simple Perturb and Observe (P&O is discussed in detail in Sections 4.1 and 4.2 of Chapter 4) algorithm shows how the block observes the change in power and moves the operating point on the curve by moving in the direction of increased power. The algorithm shown in Figure 2.11 senses the instantaneous power (u) and compares it with the previous value (Pold) in order to decide the change in duty cycle reference (y1) with steps of 0.1. The output of the MPPT block is a reference to generate the required duty cycle (PWM pulse) which is used to operate the dc-dc boost circuit.

y1=dc-dc boost duty cycle reference

u=PV power input




```
function [y1,Pold1]   = MPPT(u,Pold,y)
% This block supports an embeddable
  subset of the MATLAB language.
% See the help menu for details.
 if (u>Pold)
    inc=1;
else
    inc=-1;
end
ref = y +0.1*inc;

if (ref>6)
    ref=6;
else if (ref<-6)
        ref=-6;
    end
end
    Pold1=u;
y1=ref;
```

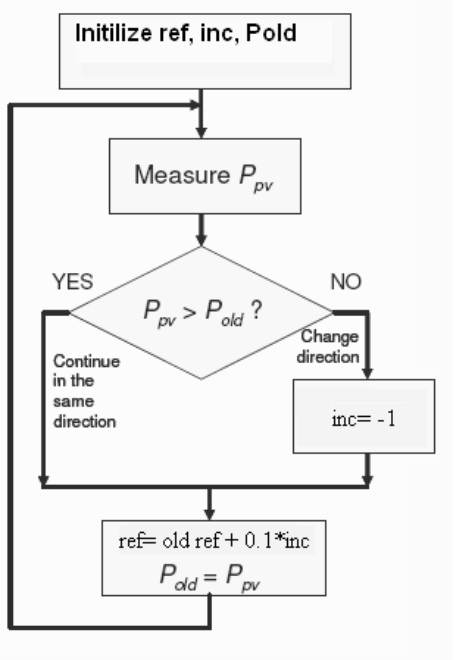


Figure 2. 11: The design of MPPT block

2.10.4 Design of dc-dc boost circuit

The dc-dc converter in the photovoltaic system (shown in Figure 2.12) is used to convert the dc electrical energy from the solar panel into a stable and reliable dc power source for use by the load or transfer energy to the grid. The dc-dc converter will also provide impedance matching for maximum power transfer.

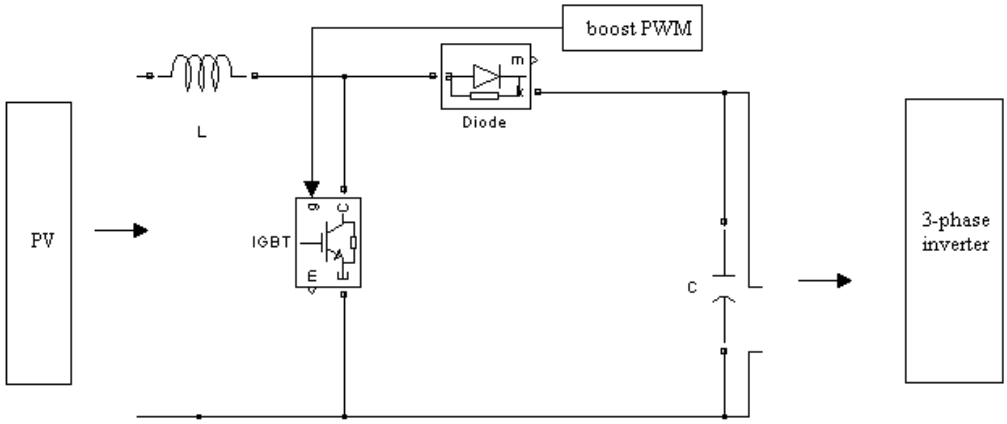


Figure 2. 12: DC-DC boost circuit model for simulation

The 1.7 kW and 3.4 kW PV curves created in Section 2.10.2 are used in the simulation of the PV grid connected system. A dc link of 780V is maintained to generate 325V ac pk, 50 Hz sinusoidal voltage at the inverter output terminals with a modulation index of 0.8.

Inductor and capacitor calculation for the power curves of 1.7 kW and 3.4 kW are as follows.

DC current flowing out of the dc-dc boost circuit for the two PV curves are:

$$\frac{1.7\,\text{kW}}{780\text{V}} = 2.15\,\text{A} \text{ and } \frac{3.4\,\text{kW}}{780\text{V}} = 4.36\,\text{A}$$

Resistance seen by the boost circuit = $\frac{780\text{V}}{2.15\text{A}} = 362\Omega$ and $\frac{780\text{V}}{4.36\text{A}} = 179\Omega$

If 400V input is considered and 780V is required output, d (duty cycle) required is 49%

using (2.19): $\frac{V_o}{V_i} = \frac{1}{1-D}$ (2. 19)

To calculate the required inductor, L and capacitor, C values, the following two equations from [25], [43] are required:

$$L = \frac{(1-D)^2 DR}{2f} \quad (2.\ 20)$$

$$C = \frac{DV_{out}}{V_r Rf} \quad (2.\ 21)$$

Where: D is the duty cycle, f is frequency of the switching PWM, V_0 is the dc link voltage, V_r is the dc link voltage ripple and R is the resistance of the load seen by the boost converter.

The equations (2.20) and (2.21) give the minimum value of the L and C respectively, which is required for safe operation in continuous conduction mode.

According to the equations (2.20) and (2.21), once D is fixed, the value of L and C will depend on R and f. Once f is decided, the L value is proportional to R and the C value is

inversely proportional to R. The L and C values are chosen such that the converter can operate at both the power levels efficiently. Therefore, according to the required D value of 49%, R = 362Ω is used for choosing L and R=179 Ω is used for choosing C. Two frequency scenarios were simulated.

(a) Low frequency PWM for running the simulation faster:

Inverter PWM frequency = 2 kHz

Simulink sampling frequency / step size = 125 kHz / 8μs

dc-dc boost PWM frequency = 2 kHz

Therefore required L≈33mH using (2.20) and C≈68μF using (2.21) with 2% voltage ripple.

(b) High frequency PWM for running the simulation with real small sized L and C

Inverter PWM Frequency = 20 kHz

Simulink sampling frequency/ step size = 1250 kHz / 800ns

dc-dc boost PWM frequency = 20 kHz

Therefore required $L \approx 3.4\text{mH}$ and $C \approx 7\mu\text{F}$ using (2.20) and (2.21) respectively.

2.10.5 Model of PWM inverter

Figure 2.13 shows the inverter block in Simulink used for simulation purposes along with its property window.

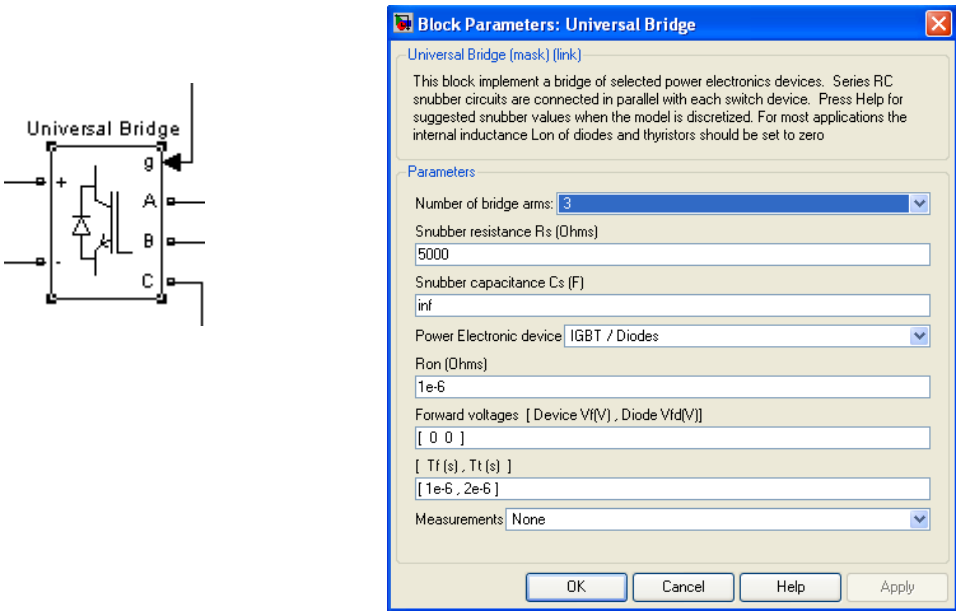


Figure 2. 13: 3-leg inverter block and its properties

2.10.6 Model of LCL filter

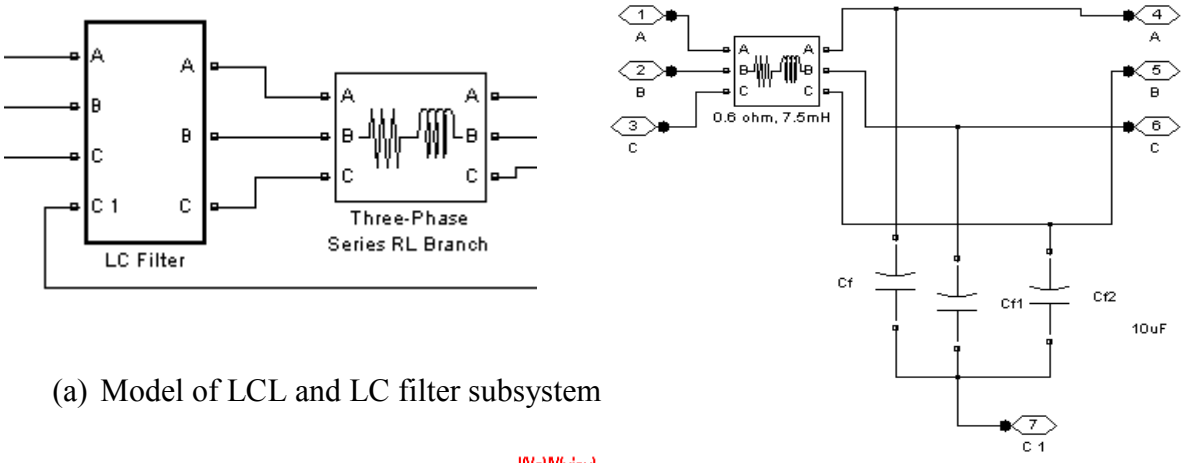
A low pass filter is used to retrieve the fundamental sine wave from the PWM output of the inverter block. A compromise is made between the values of L and C, to reduce the absorption of current by the filter and have a lower cut-off, which in turn would also reduce the physical size of the components (mainly inductor size).

The cut of frequency of the filter can be defined as $f = \frac{1}{2\pi}\sqrt{\frac{L+L}{L \cdot L \cdot C}}$ (2. 22)

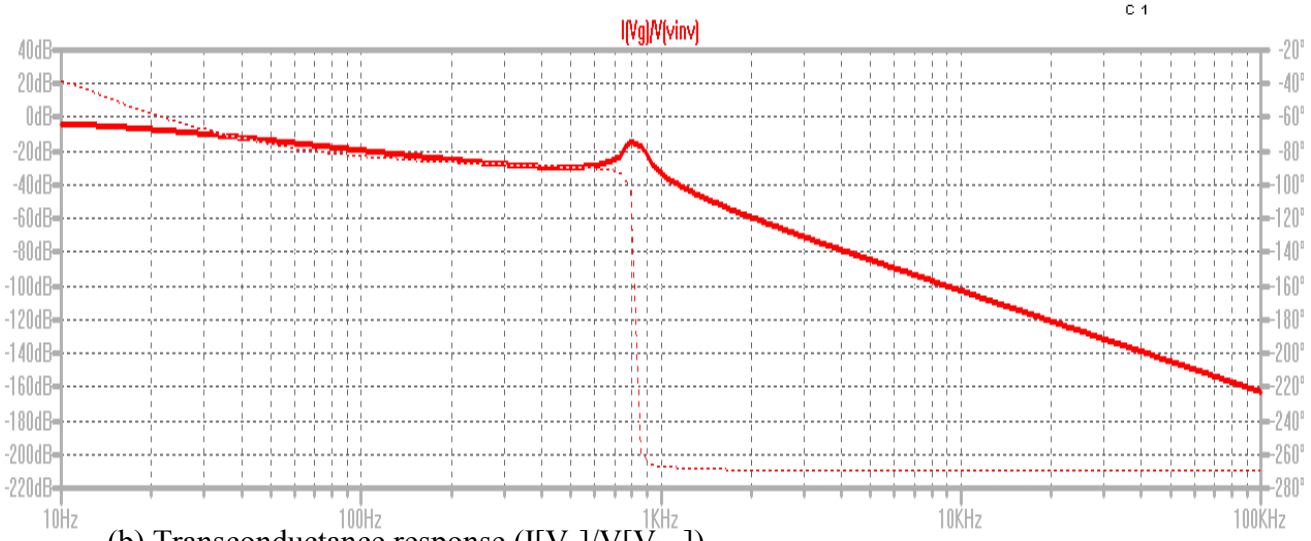
Section 5.1.7 and 5.1.8 discuss the inductor and capacitor values chosen for the final hardware prototype, which are also used in simulation. For the setup, L=7.5mH (0.6Ω)

and C=10μF has been used for which the cut off frequency, f=851 Hz allows the fundamental and up to seventeen harmonics of the inverter voltage to enter the grid. Figure 2.14(a) shows the LC part of the filter which is connected to the series RL branch (0.6Ω,7.5mH) in order to model the LCL filter (see Appendix 1).

Figure 2.14(b) shows the transconductance response against the frequency for the LCL filter that was simulated in LT Spice. It clearly shows that the 50Hz components pass through the filter and it behaves mainly as an inductor within the region of interest. 20 kHz PWM components are well attenuated and the cut off frequency is close to 850Hz.



(a) Model of LCL and LC filter subsystem



(b) Transconductance response (I[V_g]/V[V_{inv}])

Figure 2. 14: Selection of LCL filter values

2.10.7 Coupling impedance

The coupling impedance between the inverter and the grid is the impedance of the LCL filter as shown in Figure 1.1, across which the inverter voltage is displaced to transfer the required ac current. If the impedance of the capacitor (10μF) is ignored, the impedance of the two inductors (0.6Ω, 7.5mH) in series comes into effect as the coupling impedance (i.e. $Z = 4.86\angle 75.71$ for 50 Hz).

2.10.8 DC link controller

The dc link controller algorithm shown below maintains the dc link voltage at 780V during the simulation and outputs the ac current reference that is used to inject power into the grid (see Figures 2.17 to 2.19).

```
function Iref    = DC_Link_controller(Vcap,Iref_old)
% This block supports an embeddable subset of the MATLAB language.
% See the help menu for details.
  if (Vcap>780)
    inc=1;
else if(Vcap<779)
    inc=-1;
    else
        inc=0;
    end
end
ref = Iref_old +(0.01*inc);
 if (ref>15)
    ref=15;
else if (ref<0)
        ref=0;
```

```
    end
end
Iref=ref;
```

2.10.9 List of simulations carried out

The following simulations (a) to (f) were performed in modules to study and develop the final grid connected photovoltaic inverter system simulation models (g) to (i).

a) SPWM and SVPWM generation

b) Voltage source inverter control using SPWM

c) Z-Source inverter control using SPWM, with simple shoot-through control

d) PV model is run with a variable resistor to see how the operating point on the power curve moves

e) Boost circuit and three-phase inverter interaction using a fixed dc source

f) Boost and MPPT algorithm with three-phase inverter supplying a standalone load

g) Full three-phase grid connected inverter system with: PV (1.7kW and 3.4kW), boost, MPPT, three-phase inverter and grid where full control program in Figure 2.15 is applied. (see Appendix 1 for the full Simulink model)

h) Islanding situation is simulated during the worst case, where the supply of generator and load matches (three-phase load of 3.2 kW is used). Simulation is carried out with 1.7kW and 3.4 kW PV curves, where the load is almost matched with the 3.4kW PV curve.

i) Islanding situation with large mismatch of power (5 kW load and the above two PV curves are simulated)

2.11 Control program

The flowchart shown in Figure 2.15 describes the full control program algorithm for the last three simulation models (g, h, i) mentioned in Section 2.10.9. The following steps are carried out at fixed Simulink sampling frequencies described in Section 2.10.4:

- Three-phase grid voltages (V_a ,V_b,V_c) at PCC, PV operating voltage (V_{PV}), dc link voltage (V_{dc}), and PV operating current (I_{PV}) are continuously acquired.
- The RMS and peak value $(RMS * \sqrt{2})$ of these sampled grid voltages are calculated.
- The sensed grid signals are divided by the fixed peak value to get a sinusoidal normalised to 1V Pk-Pk, which is the normalised grid voltage signal. Any voltage distortion, sag or swell would directly be reflected on the normalised grid signal with this process.
- Positive sequence component is retrieved for the above three-phase voltage signals which go through a three-phase discrete PLL.
- The PLL is then used to retrieve the frequency and phase information (ωt) of this normalised grid voltage signals.
- The RMS of the three grid voltages, along with the I_{ref} (inverter ac current reference which is generated by the dc link controller), V_{dc} and Z (value of coupling impedance of the LCL filter) are used to calculate the V_{inv} Pk (required inverter peak voltage) and δ (lead angle) continuously, using the power flow theory discussed earlier in Chapter 2.
- The V_{dc} is sensed simultaneously. The M (modulation index) is calculated using V_{dc} to produce the required V_{inv} .

- V_{inv}, δ and M along with the ωt information is used to generate three sinusoidal reference signals for generation of three PWM pulses at 20k Hz using SPWM.
- The three PWM pulses switch the three top switches of the inverter block. Inverted sinusoidal references are used to generate three inverted 20 kHz switching pulses that switch the three bottom switches.

DC link controller

The dc link controller runs in parallel to the above steps, which is based on a programmed embedded Matlab script. It keeps the dc link voltage maintained at 780V by controlling the I_{ref} accordingly. If the dc link voltage below 779V is sensed, I_{ref} is decreased and if voltage above 780V is sensed then the I_{ref} is increased. This step size for increment and decrement is carefully chosen in order to keep up with the 250 Hz sampling frequency of the dc link controller. Algorithm shown in Section 2.10.8.

MPPT Controller

The MPPT controller is also based on an embedded Matlab script which runs in parallel by calculating the instantaneous P_{PV} and perturbing the duty cycle of the dc-dc boost converter as explained in Section 2.10.3. The controller is run at only 50Hz as MPPT is run at much lower speeds compared to the dc link controller and the main program.

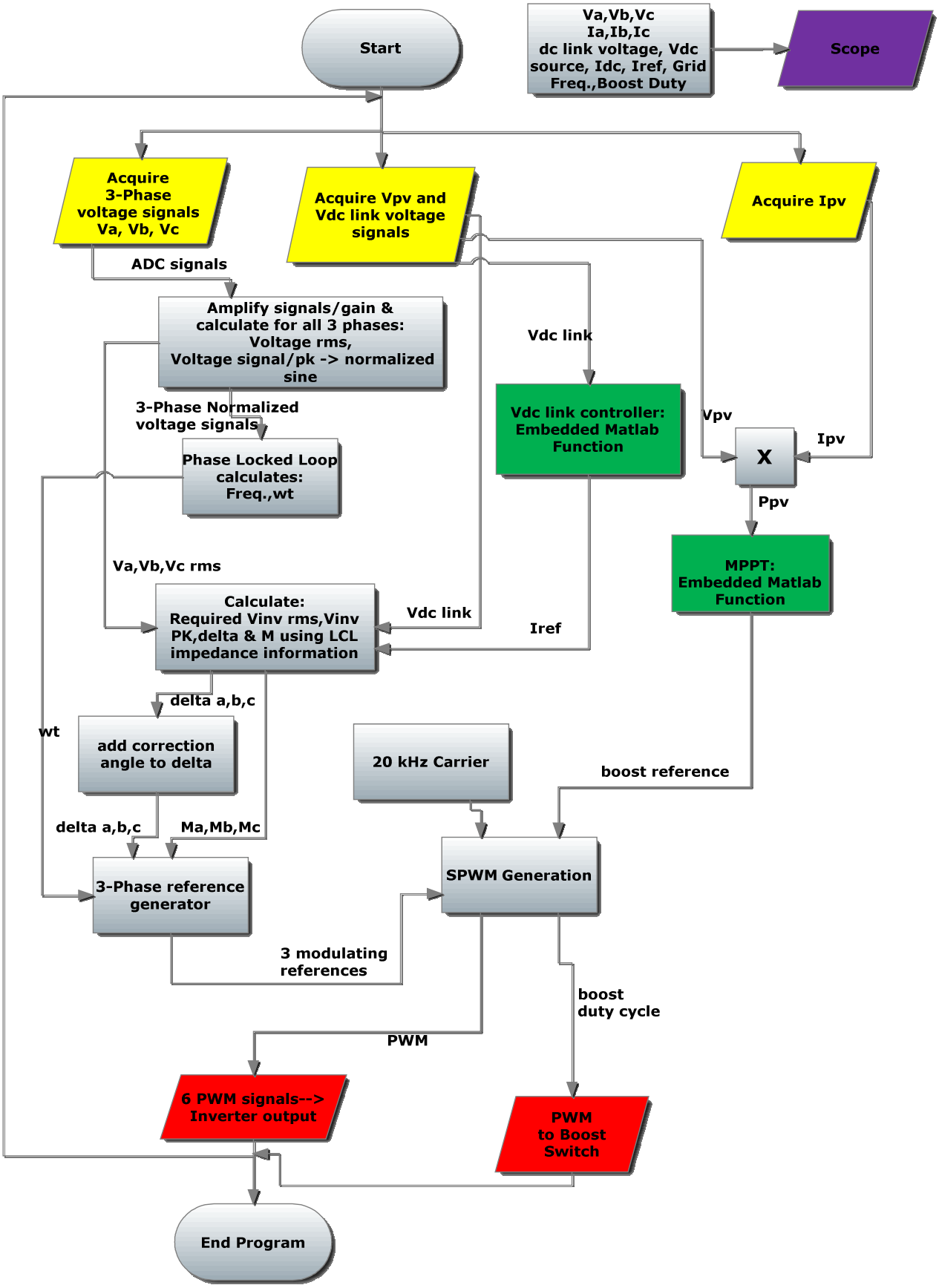


Figure 2. 15: Control program used for simulation of grid connected PV inverter

2.12 Simulation and results

This section shows only the simulation results obtained from the basic grid connected inverter control. Two PV curves 1.7kW and 3.4kW are used to supply power to the 400V L-L three-phase grid and 400V L-L three-phase load. The P&O MPPT algorithm extracts maximum power from the PV source at all times by controlling the boost duty cycle. The power fed into the dc link capacitor is transferred to the grid, using the current reference that is generated by the dc link controller. The dc link controller maintains the dc link voltage close to 780V with a 2% ripple (this dc link voltage is required to produce 325V ac pk, M=0.8 during synchronization, M is increased accordingly to transfer the available power). The flow chart of the full control program with description is given in Section 2.11.The three-phase load of 3.2 kW absorbs active power at the PCC at all times. The simulation is run with the 1.7kW PV curve until 0.1s and automatically shifted to the 3.4kW PV curve till the end of simulation. This is done to verify that the MPPT algorithm works at different power levels i.e. with different panel output power levels and extreme variation in insolation.

At this stage no islanding protection (passive or active) is incorporated in the inverter and two main cases were simulated**:**

Case 1: the PV generation closely matches the load

Case 2: large mismatch of power

Islanding protection is incorporated and will be seen in Chapter 6 of this thesis.

Case 1

During the first 0.1s period, the PV source can only supply 1.7kW of power and the remaining power required by the load is delivered by the grid. After 0.1s the PV can supply all the power required by the load and the grid is expected to play no part in delivering power (matched power situation or we can call it very little mismatch of power). The grid is disconnected at 0.4s by opening the breaker (SW1) at the grid side and the system experiences islanding with matched power between the source and the load. The expected inverter voltage, grid voltage, inverter current, load current, grid current and dc link voltage are retrieved using Simulink scopes and sent to Matlab workspace, which are used for plots below. Photovoltaic power transferred into the grid and the maximum power point tracking capability of the conventionally adopted P&O method are presented. Figure 2.16(a) shows the tracked ωt information with respect to the normalized grid voltage. Figure 2.16(b) shows the frequency tracked by the three-phase software PLL. Figure 2.17 shows the dc link voltage maintained throughout the simulation time. Inverter dc link controller controls the I_{ref} to keep the V_{cap} to 780V as close as possible. This controlled current reference depends on the V_{cap} and is shown in Figure 2.18. Figure 2.19 shows the extracted PV power. Figure 2.20 shows the PV operating voltage and Figure 2.21 shows PV operating current against time. Figure 2.22 shows the inverter line voltage, phase voltage and inverter output current. Figure 2.23 presents the grid voltage and the injected grid current. Figure 2.24 shows the inverter output current, grid current, load current and load voltage before and after islanding. Results of simulation in Figure 2.24 clearly show the grid is supplying the balance of power (2.3 A rms) until 0.1s and then the grid current goes towards zero as the 3.4 kW

PV is capable of fully powering the load (3.2 kW) after 0.27s (when I_{ref} reaches the maximum). At 0.4s the grid fails and the grid current goes to zero while the inverter current (4.6 A rms) stays the same providing the load (islanded). The load current (4.6 A rms) remains almost unchanged throughout the period. No appreciable change in load voltage profile is observed with this matching power case.

Case 2

The simulation is again carried out with a large three-phase load (5 kW, 7.3A rms required per phase) connected to the existing system model. Figures 2.25 and 2.26 show the simulation results of an islanding scenario with large mismatch of power between the PV source (3.4 kW) and the load after islanding.

Figure 2.25 gives the frequency at PCC. It shows that the frequency goes down after islanding at 0.4s due to large mismatch of power.

Figure 2.26 presents the inverter output current, grid current, load current and load voltage before and after islanding. It shows that before 0.1s the inverter provides little current (only 2.3A rms is expected of 1.7kW PV) and the grid supplies the rest (5 A rms). After 0.1s the power from the PV has increased (4.6A rms expected of 3.4 kW PV, I_{ref} reaches the maximum at around 0.23s) thus reducing the current from grid. After 0.4s, the grid has failed and inverter tries to provide all the power to the load (5 kW) even though it is not capable (PV can provide only 4.6A of the 7.3A rms required), hence the PCC voltage and frequency start to drop.

All plots clearly indicate the three different periods occurring:

- 1.7kW PV in grid connected mode till 0.1s
- 3.4kW PV in grid connected mode from 0.1s till the end of simulation
- Islanded at 0.4s

The results above show that the MPPT algorithm works well tracking the MPP at all times. The dc link controller works well maintaining the dc link voltage and generating an ac current reference as expected. The system runs as expected producing satisfactory results leading to the construction of hardware prototype which is looked at, in Chapter 5.

Chapter 3 (detailing the boost), Chapter 4 (detailing the MPPT) and Chapter 6 (detailing the anti-islanding) include their own detailed simulation results.

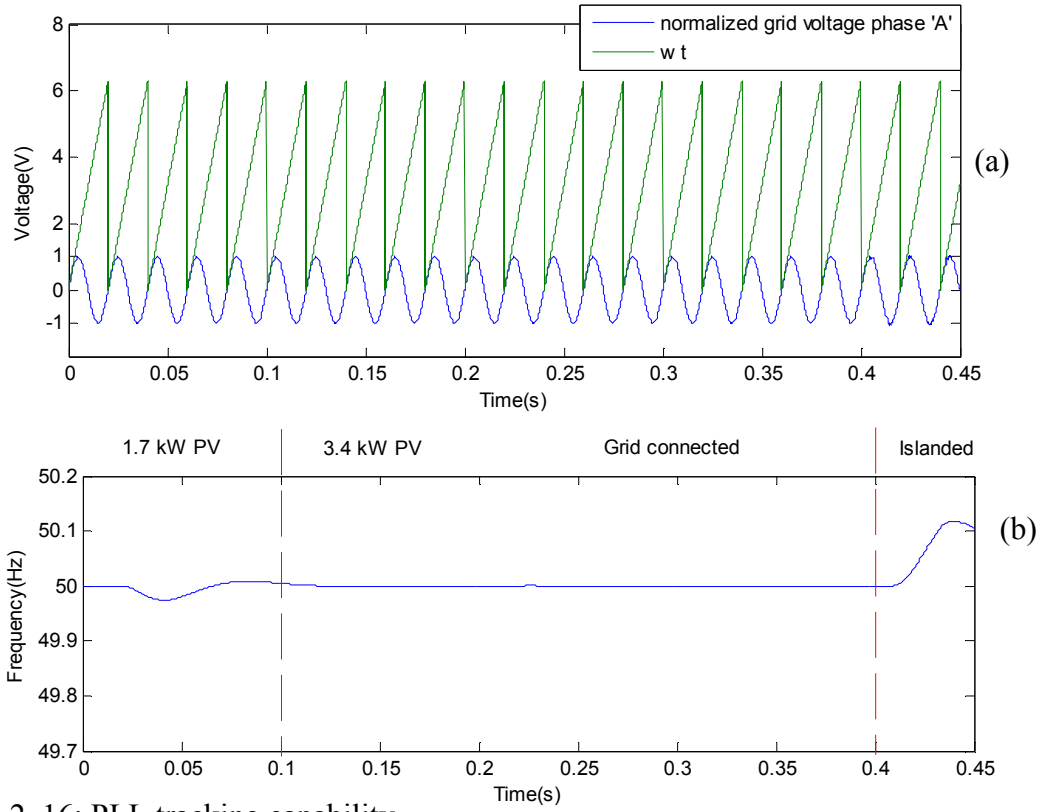


Figure 2. 16: PLL tracking capability

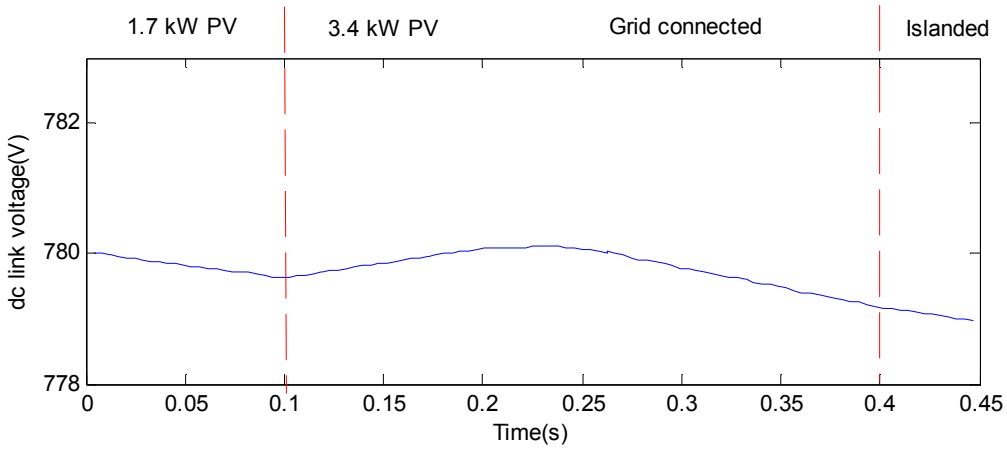


Figure 2. 17: V_{cap} maintained at 780V

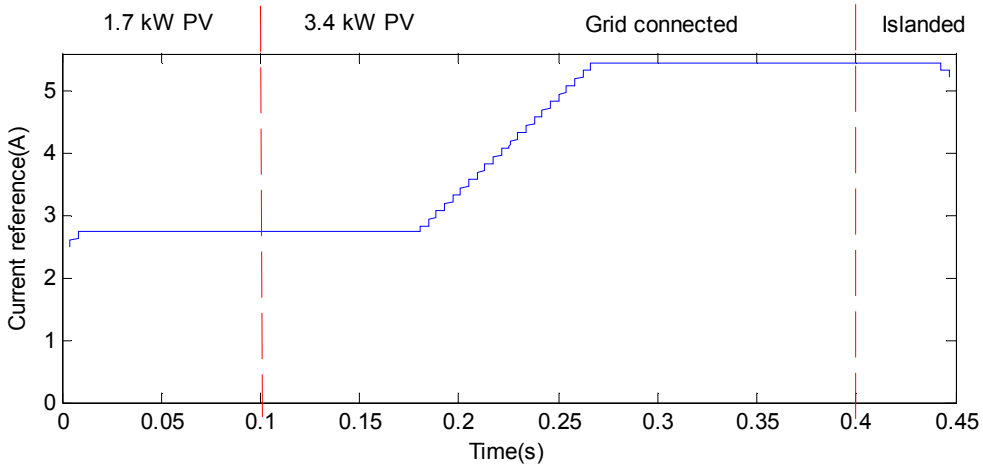


Figure 2. 18: I_{ref} changed according to the available power

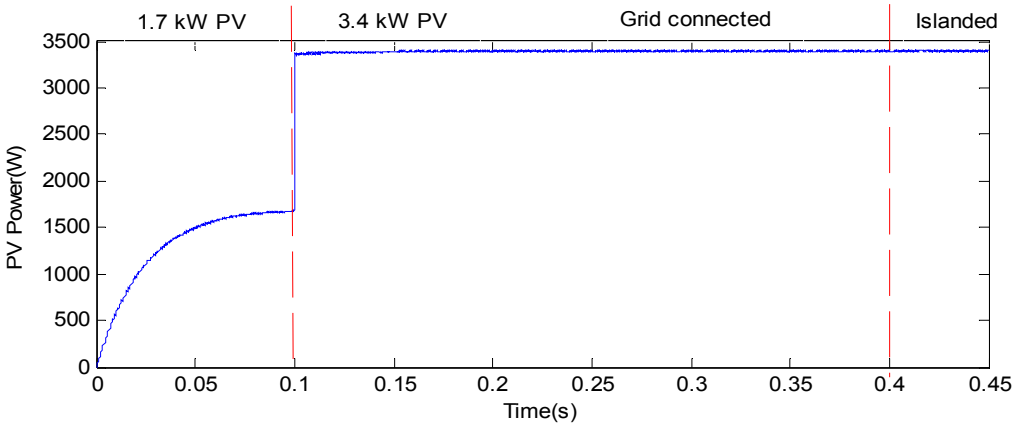


Figure 2. 19: Power from PV extracted at MPP, tracked using the MPPT algorithm

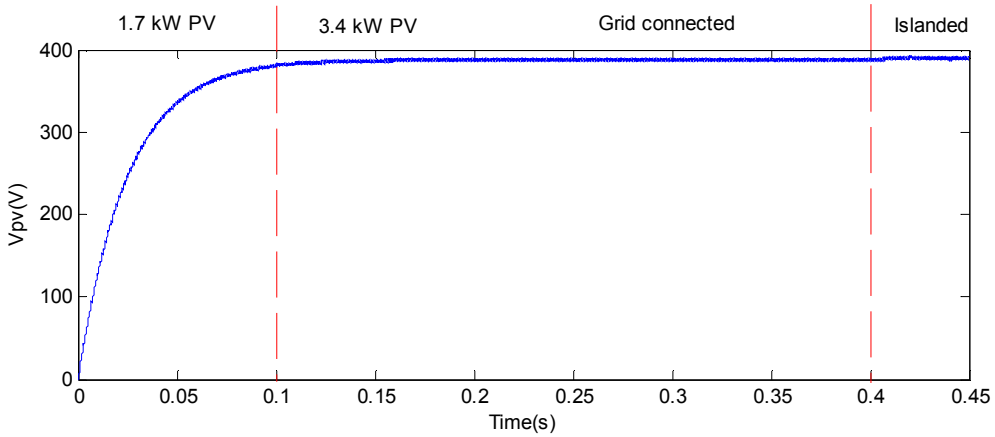


Figure 2. 20: Operating Vpv against time

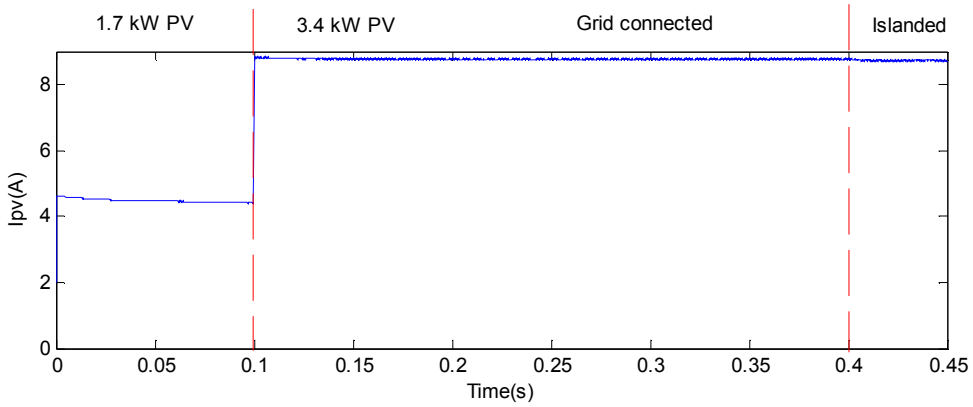


Figure 2. 21: Operating Ipv against time

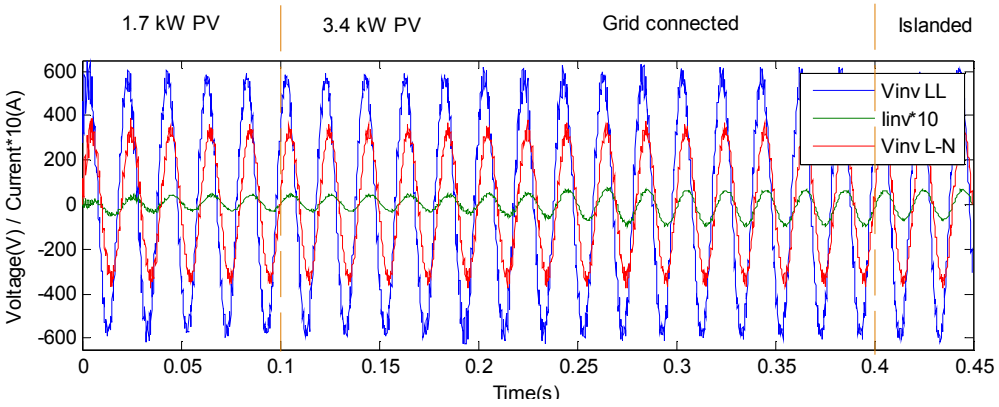


Figure 2. 22: Inverter voltage and current

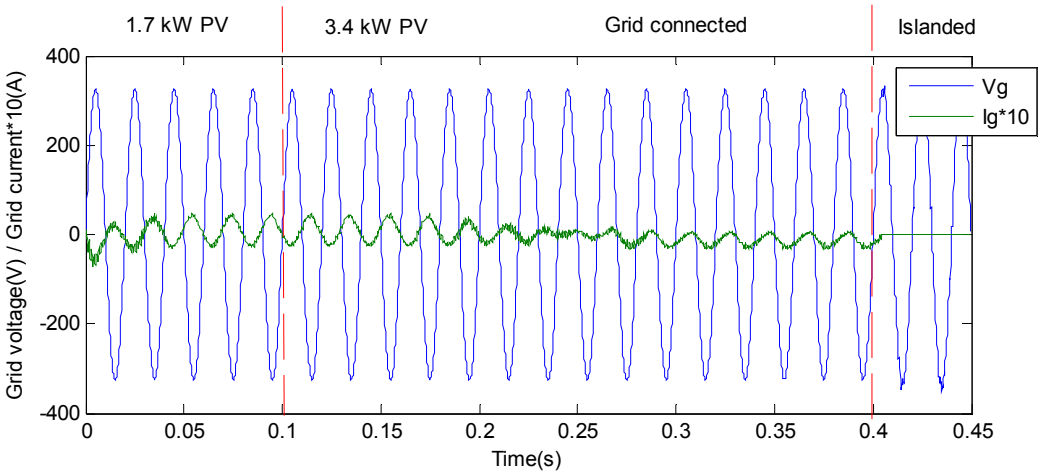


Figure 2. 23: Grid voltage and injected grid current

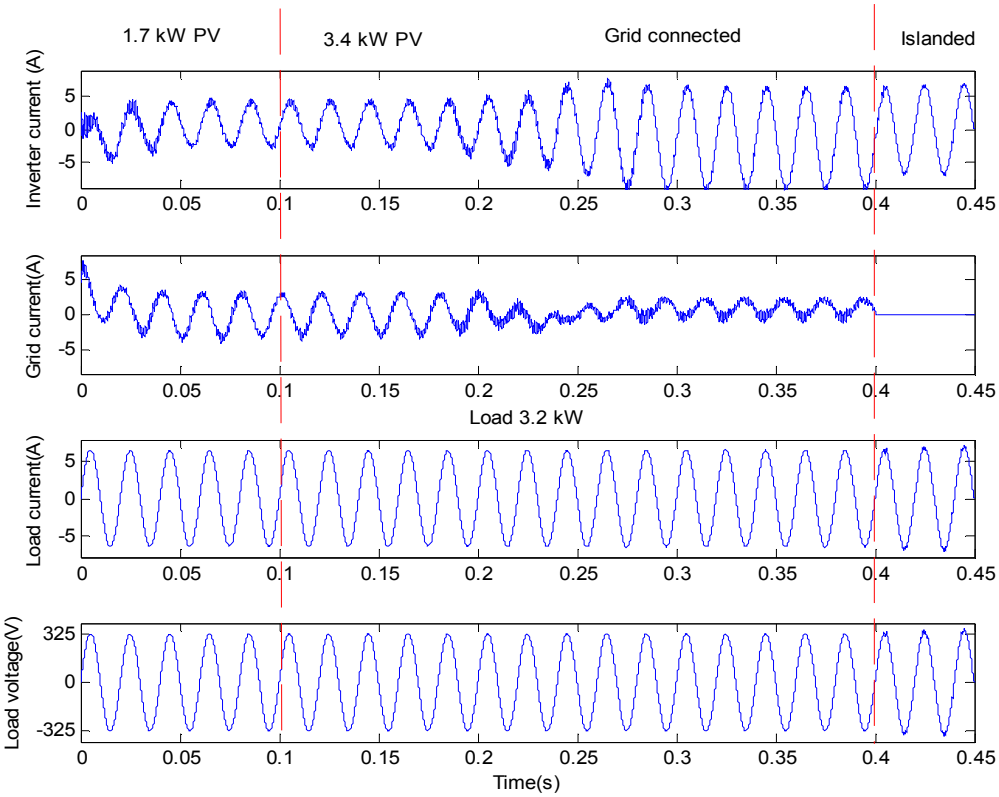


Figure 2. 24: PV inverter and grid together supply power to the load until islanded at 0.4s.

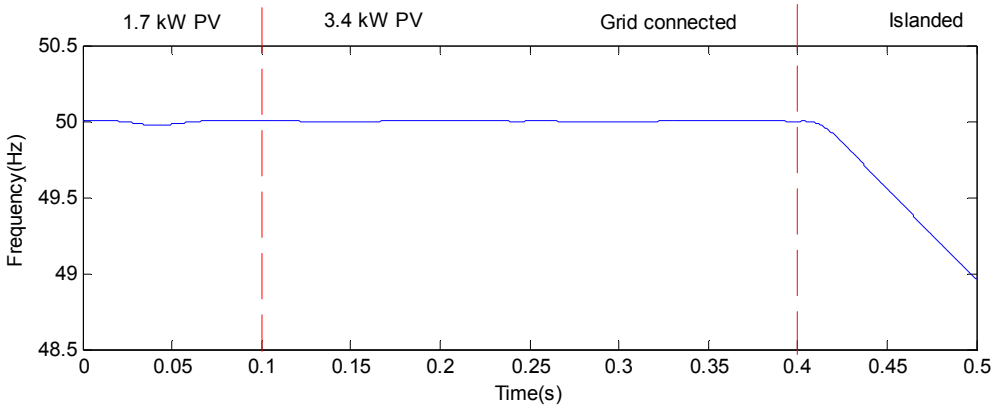


Figure 2. 25: Frequency at PCC, large mismatch at 0.4s

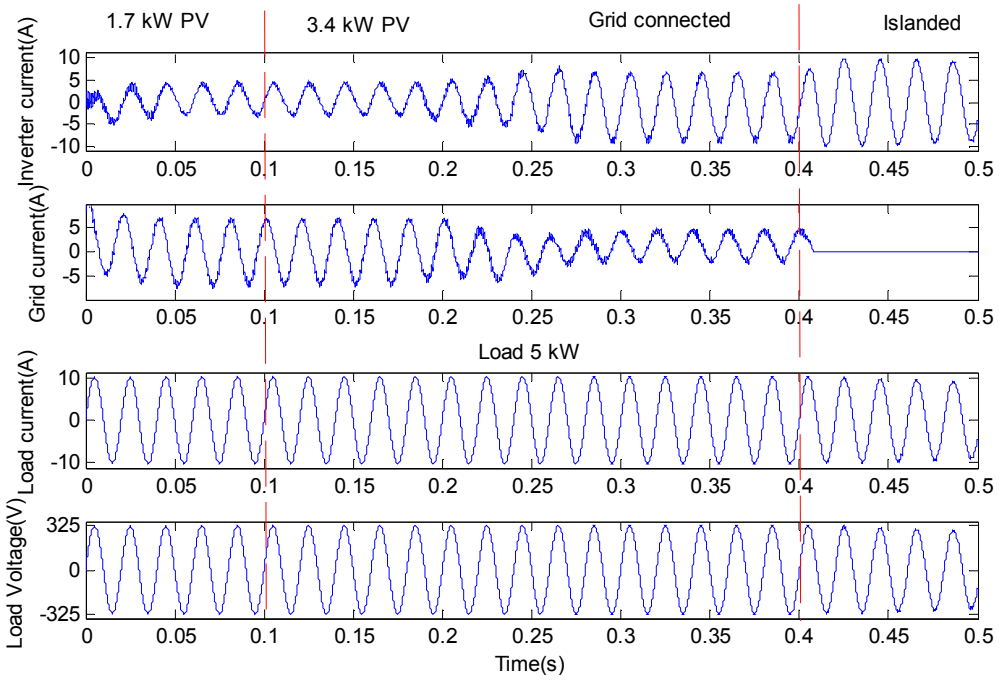


Figure 2. 26: PV inverter and grid together supply power to the load until islanded at 0.4s (large mismatch)

2.13 DSP

Implementation of power electronic converters traditionally employs analogue control. Lower cost compared to DSP based control was seen as a major advantage in the past. Despite the cost competitiveness, analog control has many drawbacks such as, the number of component counts and connections, long-term component instability (aging) and thermal drift. These adverse effects directly degrade the performance of converters and cause expensive routine maintenance. In addition, analogue control is typically designed specifically for a single converter model. As a result, converter upgrade and scalability are impossible without replacing it with new hardware. Currently, the price of a single DSP chip has fallen substantially to a few Euros but its performance and capability of executing millions of instructions (MIPS) is significantly increased.

Two DSP boards are available in the laboratory. Figure 2.27 shows the block diagram of one of the available DSP controller's, TMS320F2812 from Texas Instruments. It has a 16 bit fixed-point DSP core which is integrated with several specific peripherals on-chip including – 2 general purpose timers and 8 PWM generators, 3 capture units, 16 channels 10 bit ADC, CAN interface, SPI, SCI etc. Integration of a high speed DSP core with specific peripherals not only simplifies the design process but also offers flexibility via programmability. Thus, advanced control algorithms can be implemented and upgraded by a short period of development time.

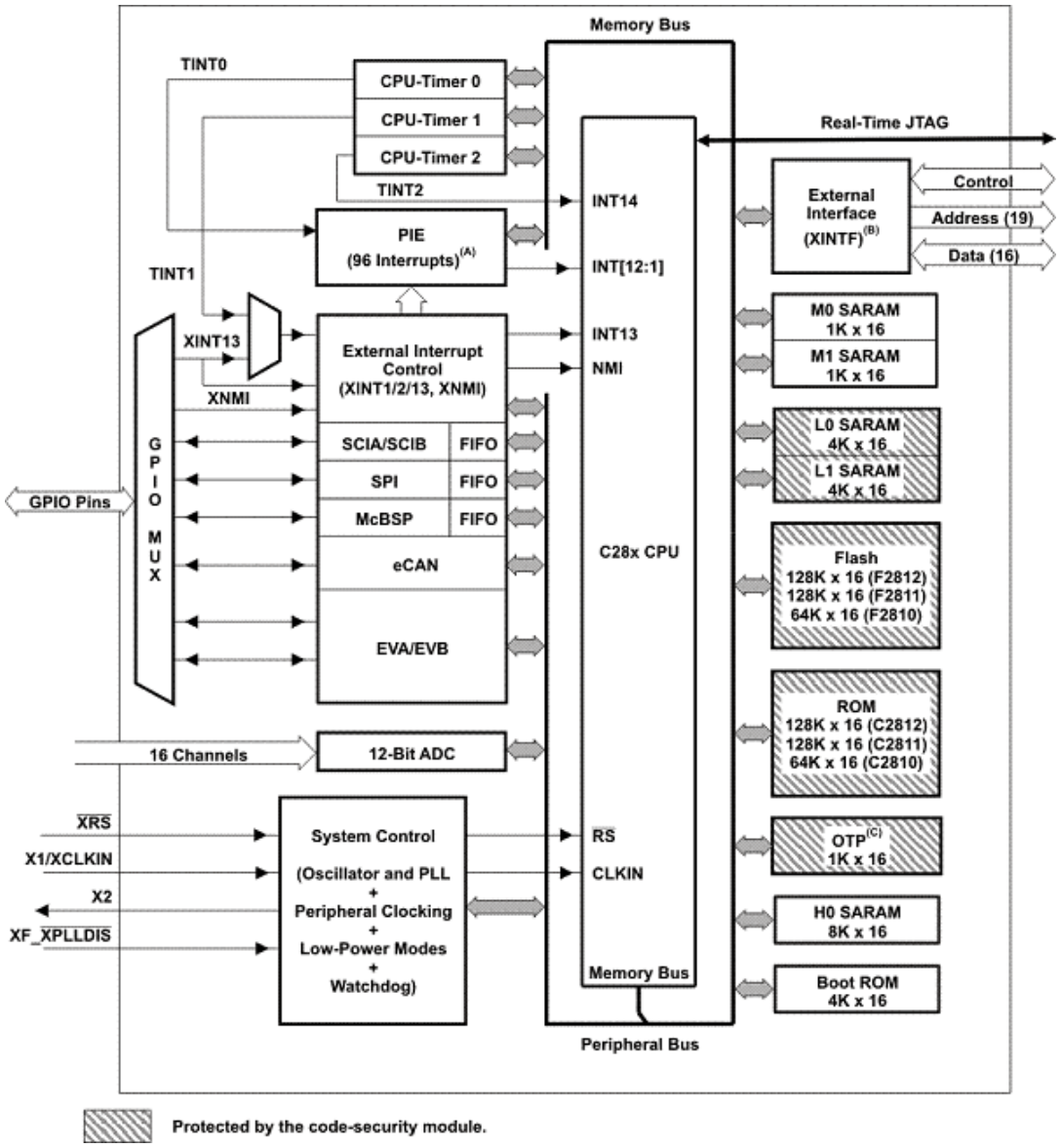


Figure 2. 27: Block diagram of Texas Instrument DSP controller TMS320F2812

Figure 2.28 shows the block diagram of the second DSP controller, DS1104 from dSpace. The DS1104 R&D controller board is a standard board that can be plugged into the PCI slot of a PC. The DS1104 is specifically designed for the development of high-speed multivariable digital controllers and real-time simulations which suited our grid connected inverter application. It is a complete real-time control system based on a 603

PowerPC floating point processor (better precision compared to the previous one) running at a 250 MHz (much faster compared to the previous one). For advanced I/O purposes the board includes a slave-DSP subsystem based on the TMS320F240 DSP microcontroller.

The controller board comes with a connector panel CP1104 which provides easy access to all the input and output signals of the DS1104 controller board. Devices can be individually connected, disconnected or interchanged without soldering via BNC connectors and Sub-D connectors. This simplifies some parts of the additional hardware circuitry that needs to be designed in order for safe usage of the DSP controller.

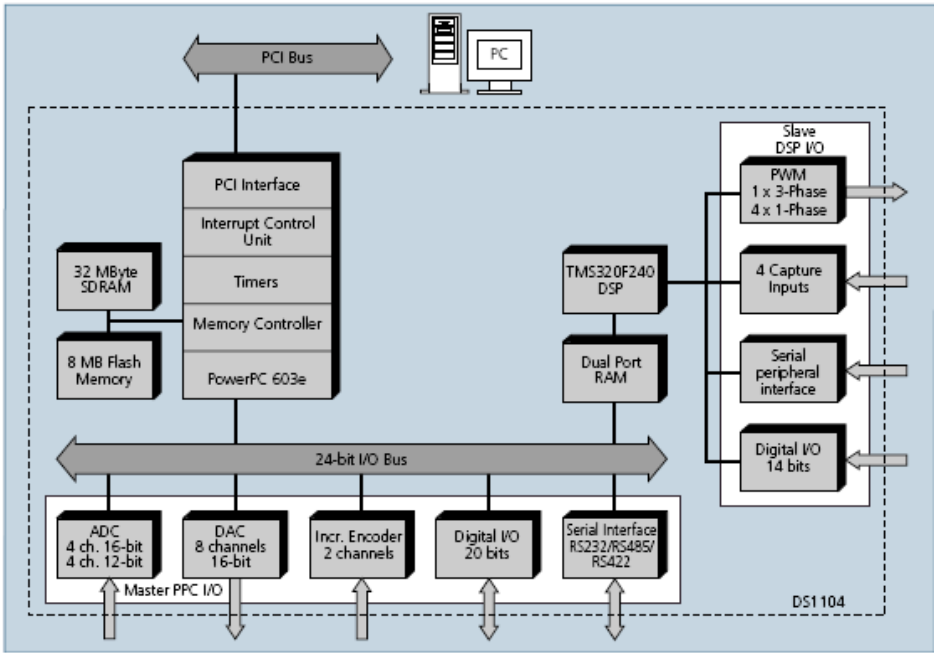


Figure 2. 28: Block diagram of the dSPace DSP controller DS1104

2.13.1 Choice of DSP

While the DIT engineering research team had prior experience with the TM320F2812 the dSpace DSP had not yet been explored prior to this project. This gave an opportunity to explore its peripherals and capabilities and to choose which one would suit best for the project.

A detailed study was carried out on both the controller boards with special emphasis being given to their peripherals like Analog to Digital Converters (ADC), Timers, General Purpose Input/Output (GPIO), Event Managers (EVA and EVB), Interrupts system and Pulse Width Modulation (PWM) output channels.

Programming with both the controller boards was practiced, Code Composer Studio for the TMS320F2812 board and Simulink and Control Desk for DS1104 dSPace board. Programming with dSPace would take very little time compared to TMS (reduces design time) as many readily available blocks from Simulink and dSpace (shown in Appendix 7) could be used to build the software.

The DSP controller DS1104 from dSpace was chosen for this project as this controller could reduce the programming design time. Simulink programs could be run on this DSP controller via the Real-Time Workshop feature, which means it reduces the development time greatly. The chosen processor is a floating point processor for higher precision and a faster processor compared to TMS320F2812.

Simple programs were tested initially to read data into the controller via the ADC and simple PWM output (with and without dead time) were analyzed on the oscilloscope to confirm the correct operation of hardware and software. Signals used for control and monitoring will be received by the DSP after it is conditioned by the measurement

interface cards in order for the outside world to interact with the DSP controller safely. A few measurement interface circuits including the PWM level shifter that drives the inverter and the boost gate have been designed and built. They are discussed in detail within the hardware section under Chapter 5 of this thesis.

2.14 Conclusion

This Chapter contained most of the sections that cover the background and literature study required to achieve the goals stated in Chapter one. It went into details of PV, grid connected inverter control, power transfer theory, MPPT and generation of PWM. It also looked into detailed design of the parts that make up the full simulation model such as PV, dc-dc boost converter, inverter switches, LCL filter etc. The full control program flow chart is presented with comprehensive description of the steps involved. Results seen are as expected and agree with the theory in the literature study. The design complied mainly with the EN50438 standard and also was in agreement with some of others listed. The two DSP boards available were discussed and the chosen board was justified. Literature review related to boost topology, MPPT and anti islanding is detailed in Chapter 3, 4 and 6, respectively.

Chapter 3

3. TOPOLOGY COMPARISON BETWEEN Z-SOURCE INVERTER AND DC-DC BOOST WITH VOLTAGE SOURCE INVERTER

3.0 Introduction

A comparative review of VSI (voltage source inverter) with dc-dc boost and a ZSI (Z-source inverter) was done to choose the topology to be used in implementation of the final design of the laboratory prototype. Some papers suggest that that ZSI could increase the efficiency of the inverter by a few percent, while some argue the difference is not much [26]-[29]. A detailed comparison of VSI with dc-dc boost to ZSI is given in this Chapter and the choice of boost topology employed for final design is discussed.

3.1 Boost converter

As dc-dc boost converter is a well known dc voltage step up converter (shown in Figure 3.1 (a)), only a brief description is given in this section. The dc-dc boost circuit design in Chapter 2 and 5, operates in continuous conduction mode. When the boost converter operates in continuous conduction mode, the inductor current (I_L) never falls to zero. Figure 3.2 shows the typical voltage and current waveforms of a boost converter operating in the continuous conduction mode. Assuming components with ideal behavior operating in steady state conditions, the two operating modes, 'On state' and 'Off state' are as follows.

During the On-state, the switch S is closed as shown in Figure 3.1 (b) and the input dc voltage (V_i) appears across the inductor, which causes a change in current (I_L) flowing through the inductor during a time period (t) by the equation:

$$\frac{\Delta I_L}{\Delta t} = \frac{V_i}{L} \tag{3. 1}$$

At the end of the On-state, the increase of I_L is therefore:

$$\Delta I_{L.on} = \frac{1}{L}\int_0^{DT} V_i dt = \frac{DT}{L} V_i \tag{3. 2}$$

Where, D is the duty cycle. It represents the fraction of the commutation period T during which the switch is on. Therefore, D ranges between 0 (S is never on) and 1 (S is always on).

During the Off-state, the switch S is open as shown in Figure 3.1 (b), so the inductor current flows through the load. If we consider zero voltage drop across the diode, and the capacitor is large enough for its voltage to remain constant, the evolution of I_L is:

$$V_i - V_o = L\frac{dI_L}{dt} \tag{3. 3}$$

Therefore, the variation of I_L during the Off-period is:

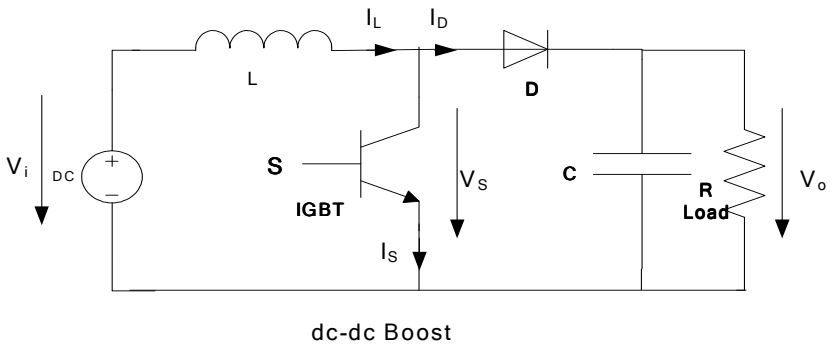
$$\Delta I_{L.off} = \int_0^{(1-D)T} \frac{(V_i - V_o)dt}{L} = \frac{(V_i - V_o)(1-D)T}{L} \tag{3. 4}$$

Substituting (3.2) and (3.4) into $\Delta I_{L.on} + \Delta I_{L.off} = 0$ we get:

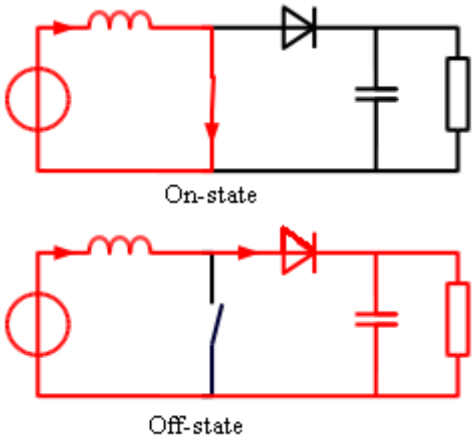
$$\frac{V_o}{V_i} = \frac{1}{1-D} \tag{3.5}$$

From the above expression (3.5) it can be seen that the output voltage is always higher than the input voltage (as the duty cycle goes from 0 to 1), and that it increases with D,

theoretically to infinity as D approaches 1. This is why this converter is sometimes referred to as a step-up converter.



(a) Boost converter



(b)The two configurations of a boost converter (On-state and Off-state)

Figure 3. 1: Boost converter

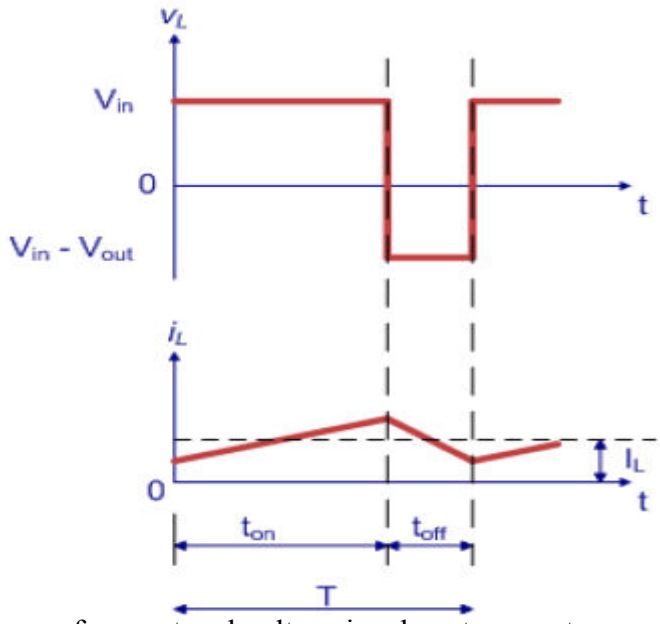


Figure 3. 2: Waveforms of current and voltage in a boost converter operating in continuous mode.

3.1.1 Choice of capacitor and inductor

The choice of inductor and capacitor values for the dc-dc boost converter can be made using (3.6) and (3.7), respectively [25], [43]. The equations below give the minimum value of the L and C required for safe operation in continuous conduction mode.

$$L = \frac{(1-D)^2 DR}{2f} \tag{3.6}$$

$$C = \frac{DV_o}{V_r Rf} \tag{3.7}$$

Where: D is the duty cycle, f is frequency of the switching PWM, V_0 is the dc link voltage, V_r is the dc link voltage ripple and R is the resistance of the load seen by the boost converter.

3.2 Z-Source inverter

The ZSI has a unique impedance network with two split inductors and two capacitors in X- shape, as shown in Figure 3.3. The three-phase ZSI bridge has nine permissible switching states unlike the traditional VSI that has eight switching states. The ZSI has six active states when the dc voltage is impressed across the three-phase load, and two zero states when the load terminals are shorted through either the lower or upper three switching devices, respectively. The ninth state, the ST state (shoot-through state) occurs when the load terminals are shorted by both the upper and lower switching devices of any phase leg (this state is forbidden in the traditional inverters to avoid ST fault). This ST state sometimes also called the 'third zero state', can be achieved by seven different ways: ST via any phase, combinations of any two phase legs and all three phase legs [30]-[32]. Since the ZSI uses the traditional eight states as in traditional inverters with an extra state, the traditional PWM techniques (Sine PWM and Space Vector PWM) can be used with slight modification to the zero states. The ST states are inserted only into the zero states while the active states remain unchanged and hence the ac output voltage of the inverter remains similar to a traditional inverter. The ST states are limited by the zero states and may replace some or all of them depending on the modulation index, M . This shoot-through zero state gives a unique buck-boost feature to the inverter, which makes it distinct from a traditional VSI or CSI [26]-[39].

The Z-network is responsible for boosting and also tracking the MPP. The shoot-through duty cycle T_0/T [31], can be increased or decreased depending on the change in power absorbed by the inverter from the dc source (P&O Method). This process is identical to

MPP tracking in the traditional VSI with dc-dc boost topology. The duty cycle at MPP, absorbs all the power from the PV panel hence matching the PV panel with the ZSI.

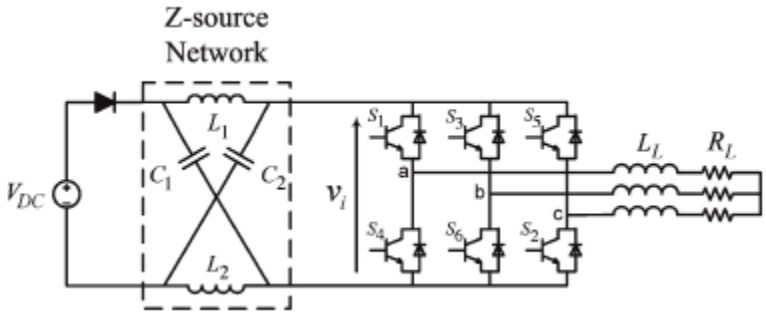


Figure 3. 3: General configuration of a ZSI [30]

3.2.1 Z-Source inverter operation

Depending on the switching states of the inverter bridge, the ZSI can be classified into three operation modes as given below:

Mode 1: Inverter bridge is operating in one of the six active states and the bridge can be seen as an equivalent current source as shown in Figure 3.4(i). During this mode the dc source voltage appears across the 'inductor and the capacitor'. Capacitor is charged (stays charged at steady state) and energy flows to the load via the inductor.

Mode 2: Inverter bridge is operating in one of the two zero states as the bridge 'short-circuits' the load through either the upper or lower three switching devices. During this mode the bridge can be viewed as an 'open-circuit' (current source with zero current flowing, shown on Figure 3.4 (i)). Voltage of the dc source appears across the 'inductor and the capacitor', except that no current flows to the load, from the dc source.

Mode 3: Inverter Bridge is operating in one of the seven different ways of ST. The bridge is viewed as a 'short-circuit' from the dc link of the inverter as shown in Figure 3.4 (ii). During this mode, no voltage appears across the load like in the zero state

operation, the dc voltage of the capacitor is boosted to the required value according to the ST duty ratio. This ST interval (T_0) is inserted into the zero states to boost the voltage whenever the PV panel is unable to provide the required voltage or during any voltage dips due to the changing insolation (irradiance) and temperature. While in this mode the dc source (PV) is separated from the inverter bridge by the diode ($V_d > V_{PV}, V_d = 2V_c$) and the voltages across C_1 and C_2 appear across L_1 and L_2 respectively causing the inductor currents to ramp up. It is noted that the diode conducts in both modes 1 and 2 (non Shoot-through (non-ST)) while it is reversed biased during mode 3 (ST).

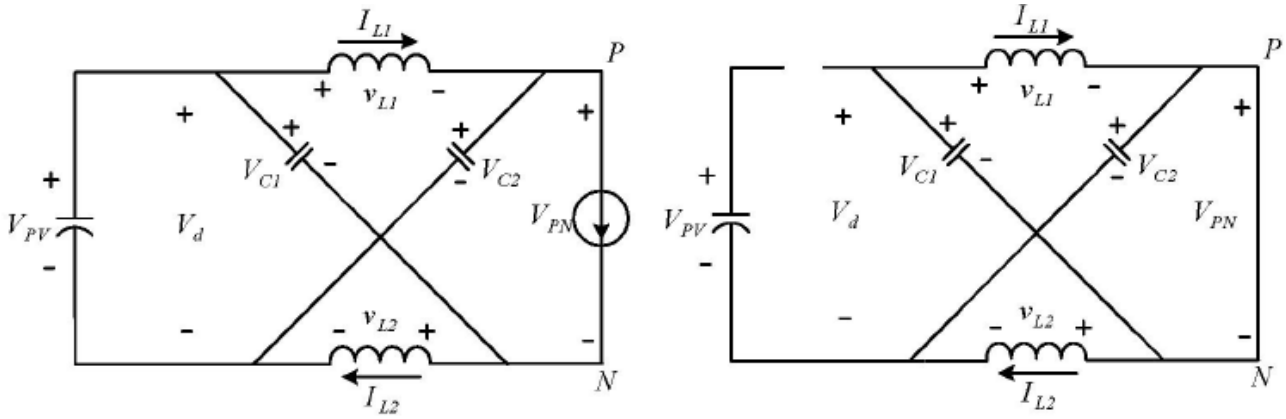


Figure 3. 4: Equivalent circuits of ZSI: (I) Non–Shoot-through mode (II) Shoot-through mode [31]

3.2.2 ZSI circuit equations

Assuming inductors L_1 and L_2 and capacitors C_1 and C_2 have the same value ($L_1 = L_2 = L$ and $C_1 = C_2 = C$), respectively, we can write the voltage equations of ZSI as:

$$\left.\begin{aligned} V_{L1} &= V_{L2} = V_L \\ V_{C1} &= V_{C2} = V_C \end{aligned}\right\} \tag{3.8}$$

During mode 3 (ST, T_0 time interval):

$$\left.\begin{aligned} V_L &= V_C \\ V_d &= 2V_C \end{aligned}\right\} \tag{3.9}$$

$$V_{PN} = 0 \text{ (ST)}$$

V_{PN} is PV output voltage or input to the ZSI, V_{PN} is the inverter bridge dc link Voltage (as shown in Figure 3.4).

During mode 1 and 2 (non-ST, T_1 time interval):

$$\left.\begin{aligned} &V_L \neq V_C \text{ , } V_d = V_{PV} = V_L + V_C \\ &V_L = V_{PV} - V_C = V_C - V_{PN} \\ &V_{PN} = V_C - V_L = 2V_C - V_{PV} \end{aligned}\right\} \tag{3.10}$$

During steady state, average voltage across $V_{L1} = 0$ over a switching period T

(Where T_1 is the non-ST period and T_0 is the ST period)

$$\overline{V_L} = V_C \cdot T_0 + (V_{PV} - V_C)T_1 = 0$$

$$\frac{V_C}{V_{PV}} = \frac{T_1}{T_1 - T_0} \tag{3.11}$$

Average dc link voltage of the inverter bridge:

$$\overline{V_{PN}} = \frac{T_0 * 0 + T_1 (2V_C - V_{PV})}{T} = \frac{T_1 (2V_C - V_{PV})}{T} = \frac{T_1}{T_1 - T_0} V_{PV}$$

From (3.11) $\overline{V_{PN}} = \frac{T_1}{T_1 - T_0} V_{PV} = V_C$ (3. 12)

Peak dc link voltage during non ST, $\hat{V}_{PN} = V_C - V_L = 2V_C - V_{PV}$ (3. 13)

Substituting V_C from (3.11) into (3.13) gives $\hat{V}_{PN} = \frac{T}{T_1 - T_0} V_{PV} = BV_{PV}$ (3.14)

Where B is the boosting factor, $B = \frac{T}{T_1 - T_0} = \frac{1}{1 - \frac{2T_0}{T}} \geq 1$ (3.15) $(T_0 + T_1 = T)$

The output peak phase voltage from the inverter can be expressed as:

$$\hat{V}_{ac} = \frac{M.\hat{V}_{PN}}{2} = \frac{M.B.V_{PV}}{2} \quad (3.16)$$

where M is the modulation index ($M \leq 1$)

By choosing the appropriate buck-boost factor $B_B = M \cdot B$ (0 to infinity) the output voltage can be stepped up or down.

Capacitor voltage can be expressed as:

From (3.14) we have $V_C = \frac{T_1}{T_1 - T_0} V_{PV} = \frac{T_1}{T} \frac{T}{T_1 - T_0} V_{PV} = \frac{1 - \frac{T_0}{T}}{1 - \frac{2T_0}{T}} V_{PV}$ (3.17)

3.2.3 Alternate equations for Z-Source inverter

From equation (3.15) we can derive $\frac{T_0}{T} = \frac{B-1}{2B}$ (3.18)

therefore $1-\frac{T_0}{T} = \frac{B+1}{2B}$ (3.19)

Substituting (3.18), (3.19) into (3.17) we can have capacitor voltage as:

$$V_C = \frac{1-\frac{T_0}{T}}{1-\frac{2T_0}{T}} V_{PV} = \frac{B+1}{2B} * B * V_{PV} = \frac{B+1}{2} V_{PV} \quad (3.20)$$

Substituting (3.20) into (3.14) we can also have peak dc link at the inverter bridge during non-ST as:

$$\hat{V_{PN}} = \mathrm{BV_{PV}} = \mathrm{B} * \frac{2\mathrm{V_c}}{\mathrm{B}+1} = \frac{2\mathrm{B}}{\mathrm{B}+1}\mathrm{V_C} \quad (3.21)$$

3.2.4 Z-network component design

3.2.4.1 Inductor calculation

During traditional operation mode (when no boost is involved) the input voltage appears across the capacitor and no voltage appears across the inductor (only a pure dc current flows through the inductors). During Z-Source mode (boost is involved) the inductor should be sized to limit the current ripple. During ST, the inductor current increases linearly and the voltage across the inductor is same as the voltage across the capacitor. During non-ST mode (traditional 8 states) the inductor current decreases linearly and the voltage across the inductor is the difference between the PV input voltage and the capacitor voltage [33]-[39].

The average current through the inductor is: $\overline{I_L} = \frac{P}{V_{PV}}$ (3.22)

where P is the total power.

Maximum current ripple through the inductors is when maximum ST happens. Therefore, the peak to peak current ripple of the inductors needs to be decided. A ripple amplitude of 30% (60 % peak to peak) of the average inductor current is commonly recommended in the literature [26], [33]. Inductor max current, $\hat{I}_L = \overline{I_L} + 30\%$

Inductor min Current, $\check{I}_L = \overline{I_L} - 30\%$

During ST, $V_L = V_C = V$

$V = \frac{V_{unboosted} + V_{boosted}}{2}$ or V can be calculated using (3.20)

Inductor value can be calculated using: $L = \frac{V * T_0}{\Delta I}$ (3.23)

Where $\Delta I = \hat{I}_L - \check{I}_L$,

T_0 is the ST period per switching cycle and can be calculated using

$B = \frac{T}{T_1 - T_0} = \frac{1}{1 - \frac{2T_0}{T}}$ and $T = \frac{1}{SwitchingFrequency, F}$

3.2.4.2 Capacitor calculation

The capacitors absorb the input current ripple and provide a stable boosted dc voltage to the inverter bridge when it is not in ST mode [33]-[35]. Since the dc source

and the inverter are both decoupled from the L C section during ST the capacitor must supply the full inductor current for the duration of the shoot through (T_0) (see Figure 3.11). Limiting the capacitor voltage ripple (ΔV_C) to about 3% at peak power (as recommended by [26], [33] the capacitor value can be roughly calculated using:

$$C = \frac{\overline{I_L} T_0}{\Delta V_C} \tag{3.24}$$

Where T_0 is the ST period per switching cycle, $\overline{I_L}$ is the average current through the inductor calculated using (3.22), and $\Delta V_C = V * 3\%$

3.2.5 Shoot-through (ST) control

Several control methods have been proposed: simple, maximum boost and maximum constant boost control [36]. Unlike the traditional inverters, the ZSI's have an extra ST state during which the output voltage to the load terminal is zero. In order to maintain the sinusoidal output the active state duty ratio remains unchanged and all or some of the zero states are turned into ST states.

3.2.5.1 Simple control

In this simple control, two straight lines are used as upper and lower ST reference lines V_p and V_n respectively, as shown in Figure 3.5. Whenever the triangular waveform is greater than V_p all the upper switching devices of the inverter are switched "On" while the lower devices are already "On" causing ST. Similarly ST occurs by turning the lower switches "On" whenever the line V_n is greater than the triangular waveform. In this control method the ST duty ratio decreases with increase in M (modulation index) and

since all the zero states are not fully utilized, voltage stress on the device is relatively high as mentioned in [27], [32], and [36].

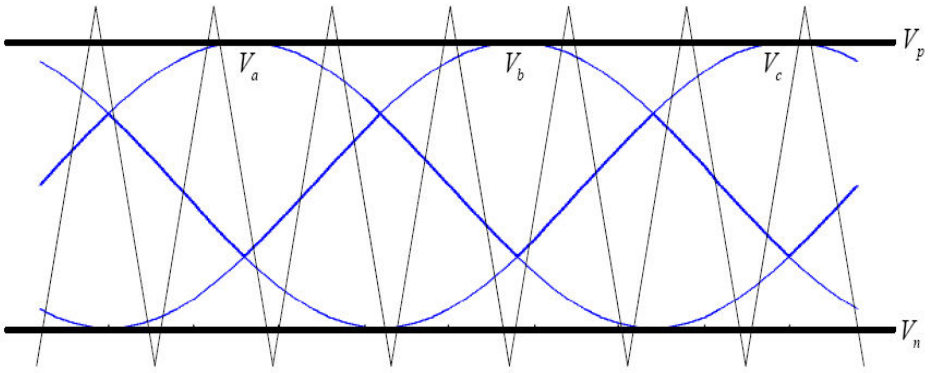


Figure 3. 5: Sketch map of simple control [36]

3.2.5.2 Maximum boost control

Maximum boost control method is used to obtain the maximum voltage boost. This control shoots through the entire zero state in a switching cycle, as a result reduces the voltage stress on the devices. The top contour of all three sinusoids together and bottom three contours of all three sinusoids together act as the upper and lower ST references respectively. These references are compared with the triangular waveform to perform the ST; a control map is shown on Figure 3.6(a). Figure 3.6(b) shows control with third harmonic injection which gives the advantage of extending the modulation index range. This method experiences varying ST duty ratio in a line cycle which causes higher inductor ripple hence requiring high inductance for low frequency or variable-frequency applications according to [36], [37].

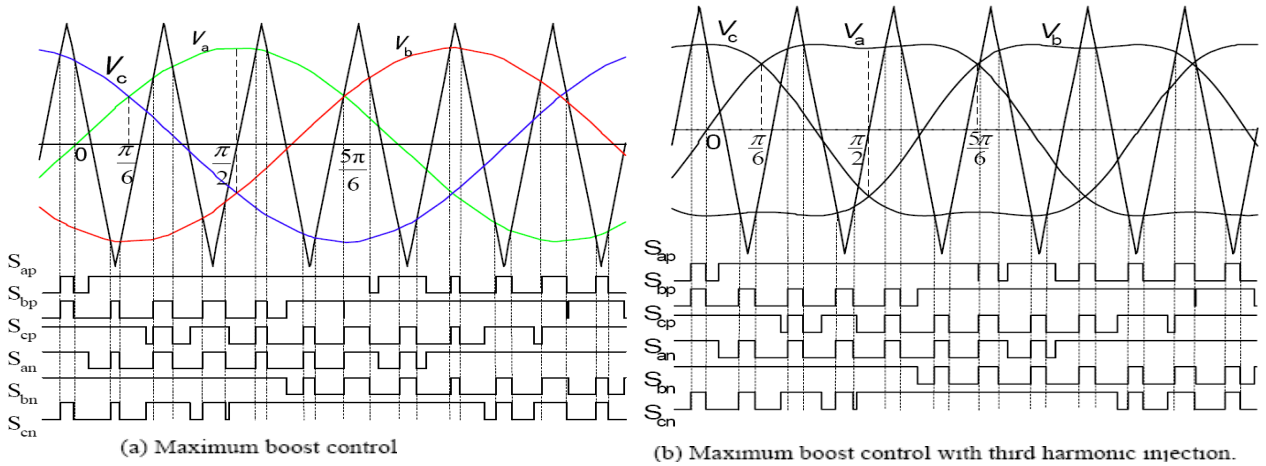


Figure 3. 6: Sketch map of maximum boost control [36], [37]

3.2.5.3 Maximum constant boost control

This control method achieves maximum boost while maintaining a constant ST duty ratio throughout; thus it results in no line frequency current ripple through the inductors. The PWM control map of maximum constant boost control is shown in Figure 3.7(a) and map of maximum constant boost control with third harmonic injection is shown in Figure 3.7(b). Using this method the inverter can buck and boost the voltage from zero to any desired value smoothly within the limit of the device voltage [36].

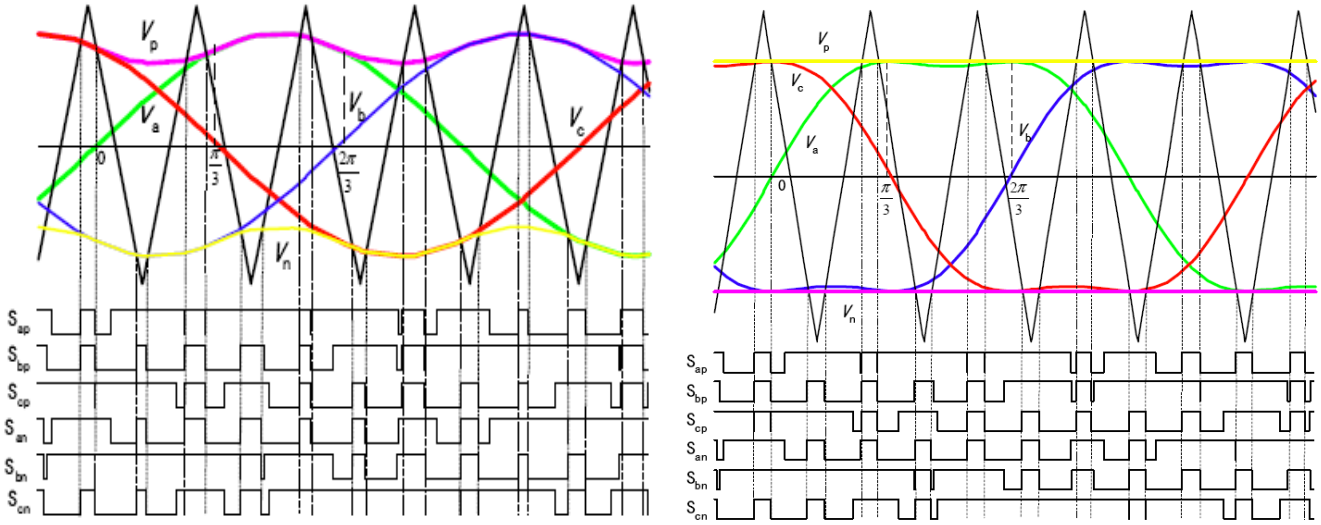


Figure 3. 7: Sketch map of maximum constant boost control [36]

For both Figure 3.7(a) and (b) $\frac{T_o}{T} = 1 - \frac{\sqrt{3}M}{2}$ (3.25) according to [36]

Boost factor and voltage gain:

$$B = \frac{1}{1 - \frac{2T_0}{T}} = \frac{1}{\sqrt{3}M - 1} \text{ and } \frac{\hat{V}_{PN}}{V_{PV}/2} = MB = \frac{M}{\sqrt{3}M - 1} \quad (3.26)$$

Range of M for Figure 3.7(a) is $\frac{1}{\sqrt{3}}$ to 1

Range of M for Figure 3.7(b) is $\frac{1}{\sqrt{3}}$ to $\frac{2}{\sqrt{3}}$ (increased modulation range)

3.2.6 ZSI self-boost phenomenon

According to [26], simulations reveal that, without the insertion of ST, the ZSI has a voltage boost when operated at low modulation index and low load power factor.

This can be a problem or an advantage depending on the application. This self boost can be controlled using a battery in replacement of the second capacitor in the Z network, C_2 [26].

While the Z-Source operates in normal mode (non-ST), inductor is assumed to have a pure dc current flowing through it and the output voltage can be calculated for the system shown in Figure 3.3, $V_{LL} = \frac{\sqrt{3}V_{DC}M}{2\sqrt{2}}$ where V_{LL} is the rms line to line voltage and $V_{DC} = V_{PV} =$ "PV input voltage".

The total power of the three-phase system is $P = \sqrt{3}V_{LL}I_{LL}\cos\phi$,

Calculate inductor current I_L :

$$I_L = I_{L1} = I_{L2} = \frac{P}{V_{PV}} = \frac{\sqrt{3}\left(\frac{\sqrt{3}V_{PV}M}{2\sqrt{2}}\right) * I_{LOAD} * \cos\phi}{V_{PV}} = \frac{3M * I_{LOAD} * \cos\phi}{2\sqrt{2}} \quad (3.27)$$

Where $I_{LOAD} = I_{LL}$ (line to line current) and $\cos\phi$ is the load power factor.

Maximum value of the I_i (load current) on Figure 3.8 is equal to the maximum load current:

$$\text{Max}\,(I_i) = \sqrt{2} I_{LOAD} \quad (3.28)$$

I_i can also be expressed in terms of I_d and I_L from Figure 3.8:

$$I_i = I_{L1} - I_{C1} = I_{L1} - I_{C2} = I_{L1} - (I_d - I_{L1}) = 2I_L - I_d \quad (3.29)$$

Where $I_{C1} = I_{C2}$ and $I_{L1} = I_{L1} = I_L$

Since the current through the diode cannot be negative (lower than 0), the maximum $I_i = 2I_L$.

$$\text{Max}\,(I_i) = \sqrt{2} I_{LOAD} = 2\text{I}_\text{L} = \frac{3M * I_{LOAD} * \cos\phi}{2\sqrt{2}} * 2 = \frac{3M * I_{LOAD} * \cos\phi}{\sqrt{2}} \quad (3.30)$$

However maximum load current can be higher than 2I_L when the product of the modulation index and the load power factor is lower than 2/3 as shown below:

$$\sqrt{2} I_{LOAD} > \frac{3M * I_{LOAD} * \cos\phi}{\sqrt{2}}$$

$$M\cos\phi < \frac{2}{3} \quad (3.31)$$

During this condition the inverter has new operating modes as shown below in Figure 3.8.

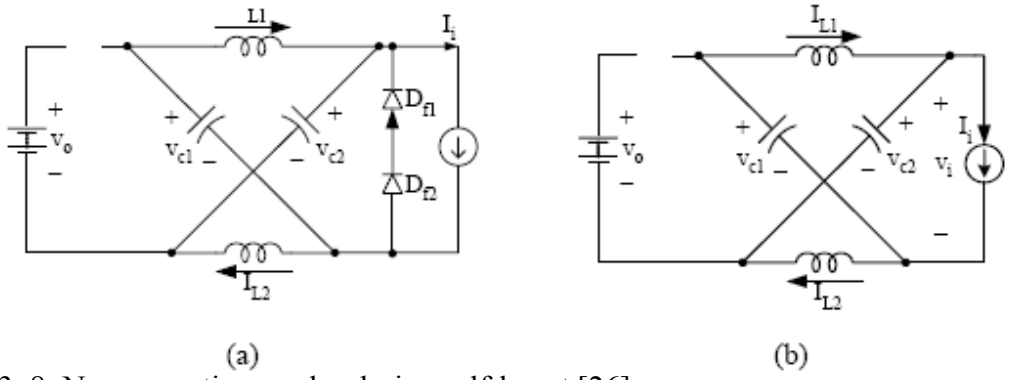


Figure 3. 8: New operation modes during self-boost [26]

The load current I_i is zero during zero states, while during an active state when the condition in (3.31) is met, the load current I_i is larger than what is available ($2I_L$). The freewheeling diodes D_{f1} and D_{f2} are turned on to provide the load with required current, which in turn puts the inverter into a ST mode as shown in Figure 3.8(a) (I_L increases linearly at ST until $2I_L =$ required I_i, i.e., $2I_L$ is larger)

Then the inverter goes into the active state, where the input diode is still reversed biased as shown on Figure 3.8(b*)* and the load current is provided by the capacitor until next switching action (zero or active state). Voltage is boosted by this unwanted ST (self boost) [26]. This self boost can be controlled using a battery as explained in [26].

3.3 Simulations of VSI (with boost) and ZSI

The boost with VSI and ZSI were both simulated in Simulink. Table 3.1 below gives the common parameters and the parameters specific to each of the boost converters.

Figure 3.9 shows the results obtained from the simulation of boost with VSI. Figure 3.9(a) shows the load current, Figure 3.9(b) inductor voltage, Figure 3.9(c) inductor current, Figure 3.9(d) capacitor current, Figure 3.9(e) dc link voltage maintained at 928V and Figure 3.9(f) load voltage maintained at 230V ac rms. In Figure 3.9: (b) inductor voltage, (c) inductor current and (d) capacitor current are zoomed in from 0.03s to 0.032s for better clarity.

Figure 3.10 shows the results obtained from the simulation of ZSI. Figure 3.10(a) shows load current, 3.10(b) inductor current (IL1), 3.10(c) inductor voltage (VL1), 3.10(d) capacitor current (IC1), 3.10(e) capacitor voltage (VC1) maintained at 664V as calculated in Table 3.1, 3.10(f) capacitor voltage (VC2) maintained at 664V, 3.10(g) inductor voltage (IL2) and 3.10(h) load voltage maintained at 230V ac rms. In Figure 3.10: (b), (c) and (g) are zoomed in from 0.03s to 0.0325s for better clarity.

Figure 3.11 shows the inductor voltage (VL1) and capacitor voltage (VC1) on the same time axis, it can be noted that during shoot through, difference between the two voltages is zero.

Figure 3.12(a) shows the dc link voltage of the ZSI and Figure 3.12(b) shows a zoomed in figure of this dc link voltage from 0.03s to 0.0325s. It is seen that the dc link voltage is quite pulsating for which reason direct control of dc link is not feasible. Full schematic diagrams of the two different circuits used for simulations are shown in Appendix 2 and 3.

Table 3. 1: Simulation parameters for boost with VSI and ZSI

<table>
<tr><th colspan="2">Simulation parameters for Boost with VSI and ZSI</th></tr>
<tr><td colspan="2">Power: 1680W, Three-phase load, Phase voltage Vac L-N: 230V rms
Iac phase: 1680W/3 = 560W, 560W/230V = 2.43A rms (3.44 A Pk)
Vdc Input for both cases: 400V dc
M=0.7, dc link of inverter required for both cases: 928V
Boost factor required : 2.32
Carrier frequency =10 kHz, Carrier triangle with +10 and -10V Pk-Pk is used
PWM frequency =10 kHz</td></tr>
<tr><th>Boost with VSI</th><th>ZSI</th></tr>
<tr><td>L> $(1-D)^2$*DR/2f
C> DVo/V_rRf
dc side : 1680W/928V=1.81A,
R= 928V/1.81A=512.6Ω
Vo= output voltage (928V), V_r= capacitor voltage ripple = 27.84V (3%)
Vout/Vin= 1/1-D
Duty cycle = 57%
Therefore : L= 2.69mH and C=3.71μF</td><td>$C = \frac{\overline{I_L} T_0}{\Delta V_C}$ $L = \frac{V * T_0}{\Delta I}$
dc side: 1680W/400V= 4.2A
Average inductor is expected to be 4.2A with 60% ripple
Capacitor voltage : 664V with 3% ripple
$\frac{T_0}{T} = \frac{B-1}{2B} = 0.284$, ST time per cycle $T_0 = 28.4\ \mu s$, T=1/10 kHz= 100μs.
Therefore: L1=L2=7.48 mH, C1=C2= 5.99 μF</td></tr>
</table>

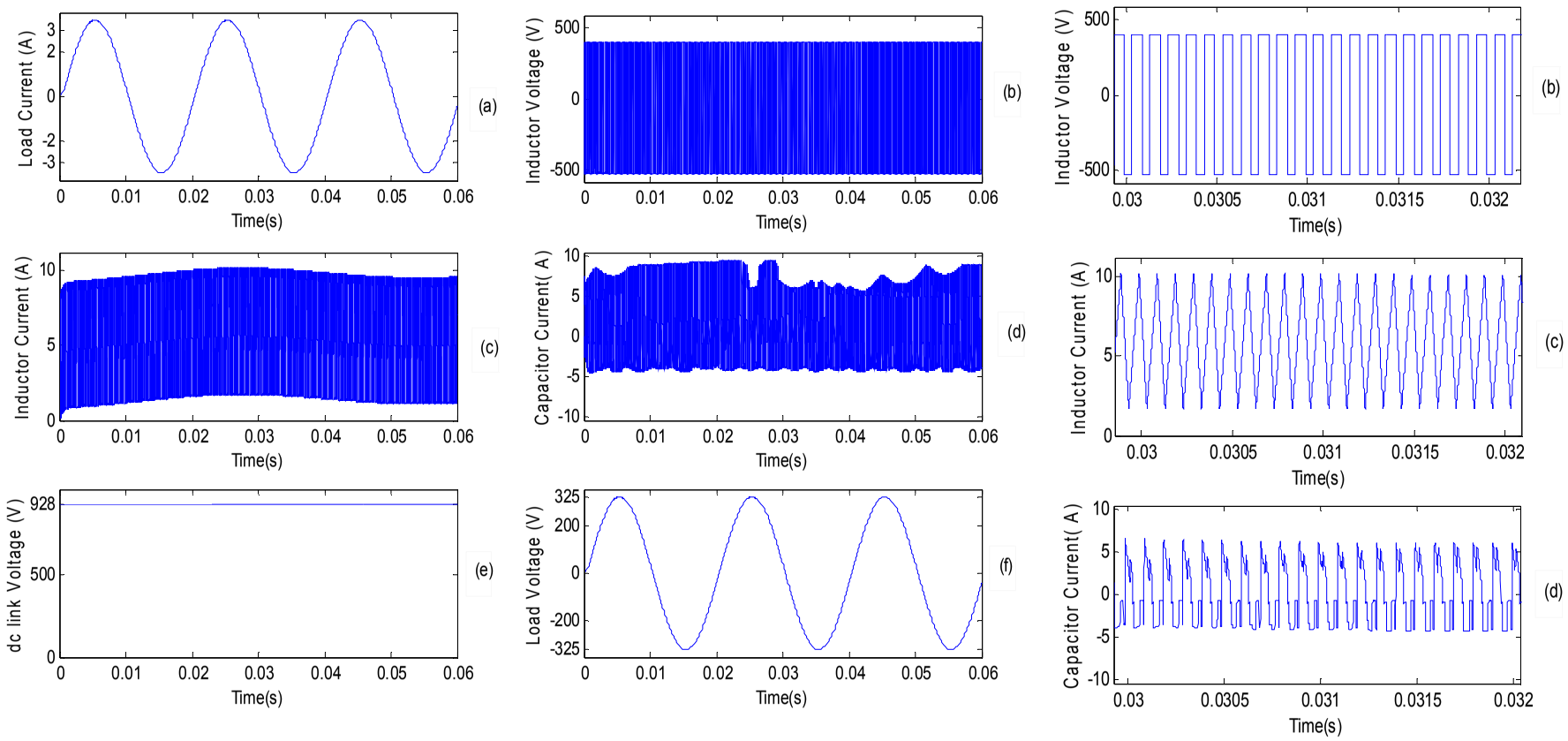


Figure 3. 9: VSI with boost converter simulation results

(a) load current, (b) inductor voltage ,(c) inductor current,(d) capacitor current,(e) dc link voltage and (f) load voltage

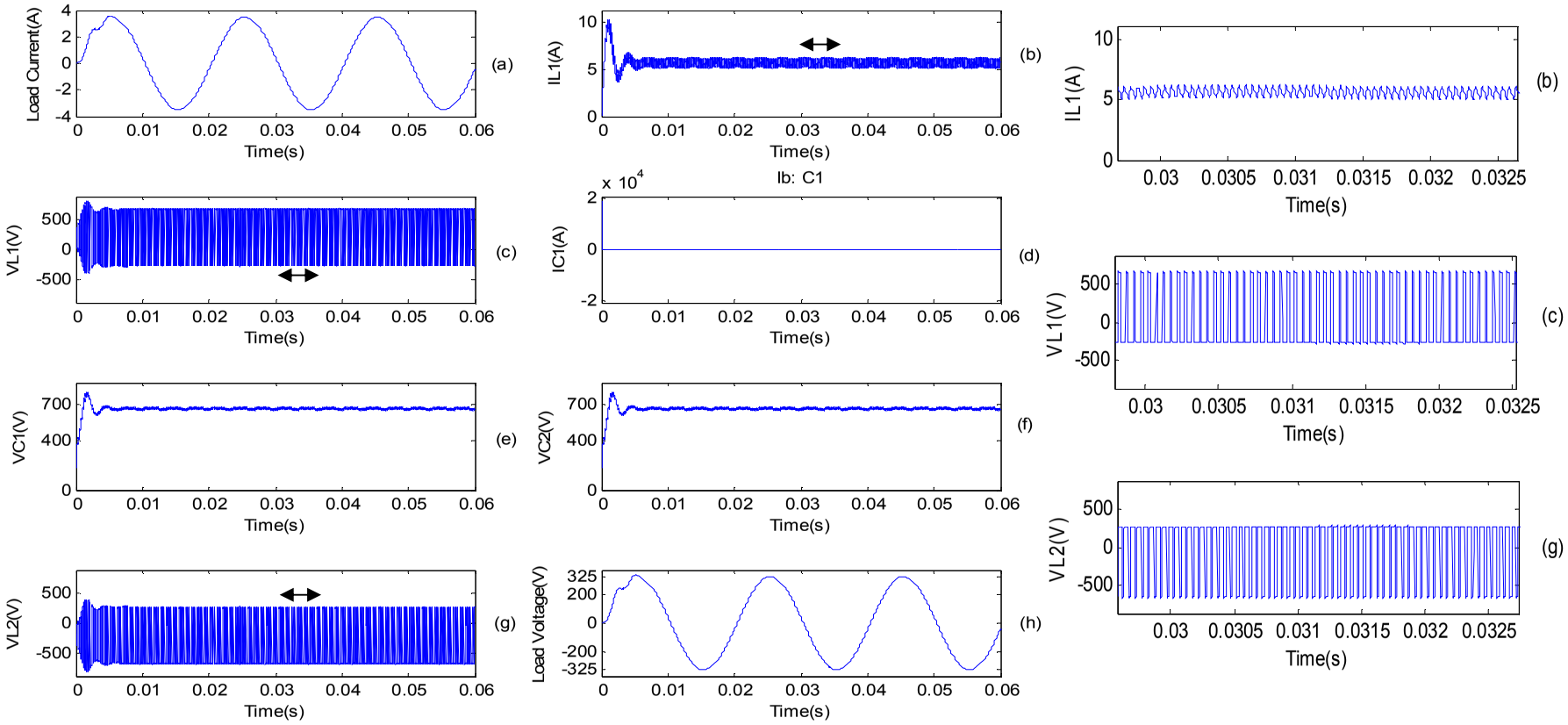


Figure 3. 10 : ZSI simulation results

(a) load current, (b) L1 current ,(c) L1 voltage ,(d) C1 current, (e) C1 voltage, (f) C2 voltage, (g) L 2 voltage and (h) load voltage

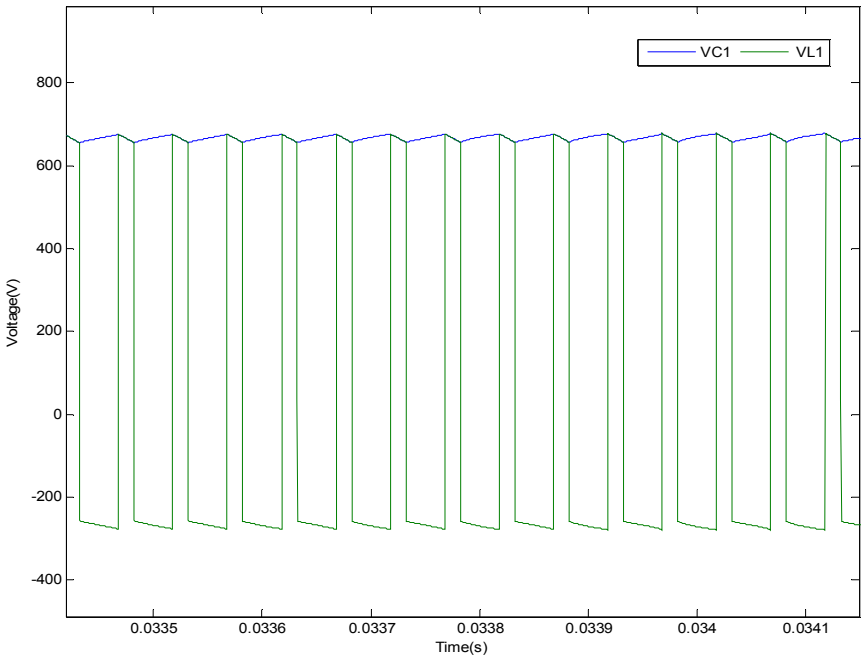


Figure 3. 11 : VL1 and VC1 during shoot through

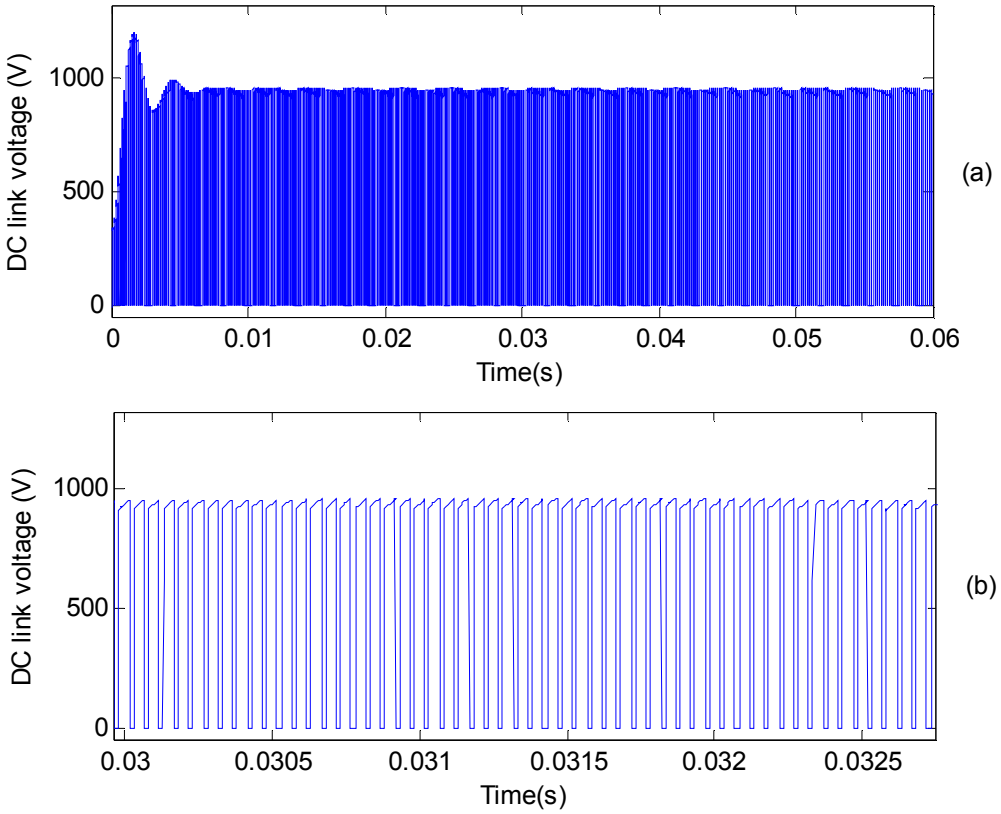


Figure 3. 12: (a) DC link voltage of the ZSI (b) zoomed in from 0.03s to 0.0325s

3.4 Comparison of VSI (with boost) and ZSI

Both converter topologies have their own merits and demerits which are compared in the Table 3.2 below. The output quality from both inverters is comparable, ZSI output voltage experiences less distortion as no dead bands are incorporated but direct control of the dc link voltage is complex (see Figure 3.12). Hence, capacitor voltage is usually employed to retrieve the I_{ref} when MPPT algorithm controls the boost factor during grid connected mode (see section 4.2.3 for further explanation).

Table 3. 2: Merits and demerits between boost with VSI and ZSI

Boost with VSI	**ZSI**
1 large capacitor, 1 large Inductor 1 extra switch which also requires an extra gate driver circuit	2 small capacitor, 2 small inductors (slightly large in total) [26]
Traditional Sine PWM used	Traditional Sine PWM used with modification to zero states (shoot through inserted)
Unwanted shoot through can cause damage to inverter, dead band needs to be incorporated	Shoot through deliberately inserted and causes no damage, can handle unwanted shoot through
Dead band causes distortion	No dead band, no distortion
Efficiency quite high (weighted average about 90%)	Efficiency comparable at high loads, but low at low loads due to higher circulating

	power in Z-source network (weighted average is slightly lower), efficiency comparable
Modulation index and Boost factor are not directly dependent	Modulation Index (M) and Boost factor (B) are directly dependent on each other, a higher M, reduces B. This is because the peak of the modulating wave decides the minimum value the upper shoot through reference can take in simple boost control)
No self boost	$M\cos\phi < 0.67$ causes self boost, where $\cos\phi$ is the displacement factor of the load
Control of dc link voltage is simple	dc link voltage is pulsating, direct control is complex, and hence control of capacitor voltage is considered.

3.5 Choice of boost converter for the hardware prototype

In summary the ZSI offers comparable efficiency to the boost with VSI and only marginal savings in hardware complexity at the expense of greatly increased control complexity. The increased control complexity has further impact on a Simulink / dspace implementation as follows:

Shoot through for a ZSI requires implementation of modified PWM (conventional PWM merged with shoot-through). The conventional PWM Block available in Simulink/dSPace (DSP Board) cannot be used to identify the shoot-through 'insertion points'. Shoot-through insertion point is the situation where top three switches or bottom three switches are 'on'. The dSpace conventional PWM Block requires duty cycle values as input, to create 'centred PWM'. This centred PWM output feature cannot be used to merge the shoot-through with the conventional PWM output (creates unwanted shoot-through).

Implementing the modified PWM in Simulink is only possible by using a high frequency carrier, modulating references and two shoot-through references (for top and bottom switch) per phase as explained in Section 3.2.5.1.

In order to sense the shoot-through points from the high frequency carrier and the shoot-through references (to obtain shoot-through duty cycle), a much higher sampling frequency is required. This very high sampling frequency makes the DSP go into an overrun condition. Nevertheless this method is adopted for only simulation purposes. This problem is taken as one of the limitation of the existing dSpace DSP software which has dedicated conventional PWM control blocks only to be used with conventional VSI

inverters. For these reasons it was decided to proceed with a dc-dc boost with VSI topology for this work.

3.6 Conclusion

Two different boost topologies dc-dc boost converter with VSI and ZSI suitable for grid connected inverter application were investigated in detail. ZSI being a new topology was analysed in terms of circuit equations, operation modes, control methods and component design. Simulation results for both the converters were produced in a Simulink environment and a concluding comparison table was laid down. Choice of boost converter topology that is used within the prototype was justified with reasons to support the ease of implementation using the selected dSpace DSP.

Chapter 4

4. NEW MAXIMUM POWER POINT TRACKING APPROACH BASED ON PERTURB AND OBSERVE METHOD

4.0 Introduction

Section 2.1 and 2.2 of Chapter 2 discussed the P-V and I-V characteristics of a PV cell and the need for a MPPT algorithm. Photovoltaic cells produce a low dc output voltage which depends on the insolation and the load. Thus, they are unable to connect to the utility directly. However, they can be interfaced and supply power to the utility by means of power electronic converters [40]. PV panels are put together in series to achieve a high output voltage but it is not always feasible to have sufficient panels in series to give the dc voltage required by the inverter system. Therefore a dc-dc boost circuit is usually employed to increase the voltage at the inverter dc link. In order to interface with the nominal 230V Irish (European) low voltage grid the inverter has to produce a peak voltage of 325V at the ac output terminals.

Adjusting the control of the dc-dc boost front end also allows us to vary the operating point of the solar cell in order to achieve the maximum power transfer at any given level of solar insolation. In other words the dc-dc boost circuit is used to acquire the maximum power out of the PV panels at all times by implementing a maximum power point tracking (MPPT) algorithm. If a ZSI was used, the 'boosting stage' of the circuit is done by the Z impedance network; the 'maximum power transfer' could be controlled by the shoot-through reference and the inverter ac current (I_{ref}) can be controlled by the dc link controller.

4.1 Maximum power point tracker review

A controller that tracks the maximum power point locus of the PV array is known as a MPPT controller. There are several algorithms to track the MPP and a few common maximum power point tracking algorithms have been reviewed. For optimal operation, the load line must match the PV arrays MPP locus and if the particular load is not using the maximum power, a power conditioner should be used in between the array and the load [13],[14],[41].

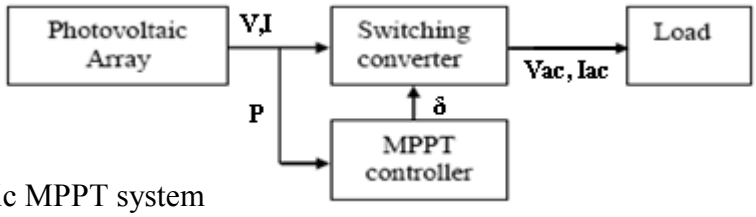


Figure 4. 1: Basic MPPT system

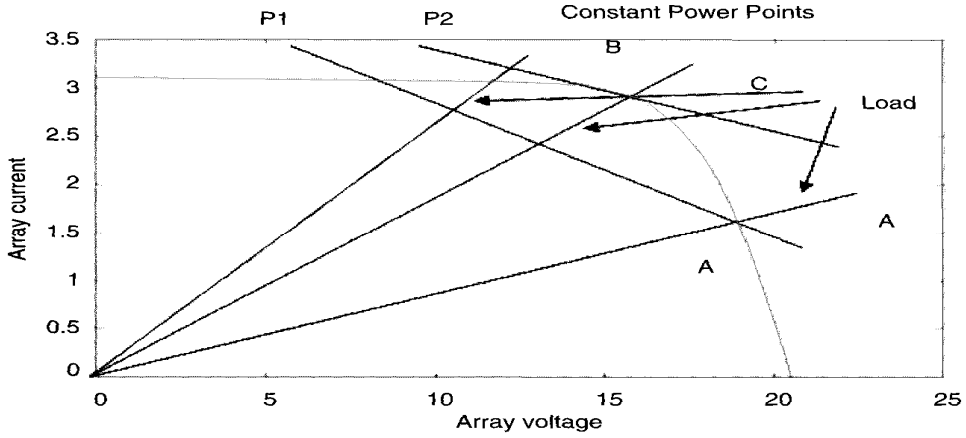


Figure 4. 2: PV array and load characteristics

Some of the frequently discussed MPPT techniques in the literature are as follows:

- Fractional short circuit current (Isc), a current based MPPT
- Fractional open circuit voltage (Voc), a voltage based MPPT
- Perturb and Observe (P&O) /Hill climbing
- Incremental Conductance Technique (ICT)
- Constant Reference Voltage(CRV)

4.1.1 Fractional open circuit voltage/voltage based MPPT technique

This is the one of the most conventional, but it is considered to be a fast, practical and powerful method for MPP estimation without the need for a powerful DSP. It is based on the observation that the MPP voltage (V_{mpp}) can be approximated by a linear function of the open circuit voltage (V_{oc}) [13], [14]. For instance $V_{mpp} = M_v V_{oc}$.

where M_v = voltage factor = 0.76 (for instance).

In order to use this method V_{oc} is measured periodically by open circuiting the cell string. Then, the appropriate V_{mpp} can be calculated from a simple voltage divider ($V_{mpp} = M_v V_{oc}$). A voltage control loop shown below controls the MPP.

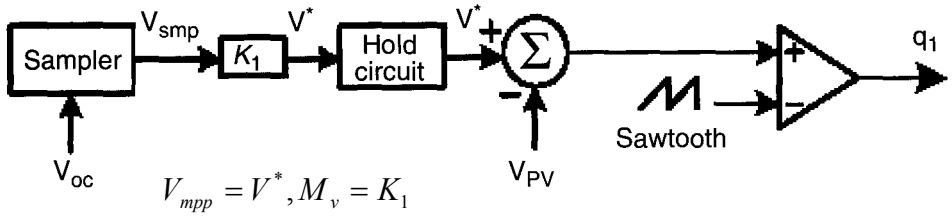


Figure 4. 3: Conventional MPPT controller using open circuit voltage Voc

4.1.2 Perturb and observe (P&O)

This is where the duty cycle (δ) of the switching converter is periodically increased or decreased controlling the array power (P). The power can be sampled periodically and compared with its previous value ($p_k - p_{k-1}$). If the power has increased then the δ is stepped up in the same direction, otherwise δ is stepped in the opposite direction until the MPP is reached [15]. P&O and the hill climbing method both rely on the gradient $\frac{dP}{dV}$. If $\frac{dP}{dV}$ tends to zero or equals to zero then the power is at its maximum point (MPP). If it is

positive, then the operating point is on the left of MPP and negative implies the operating point is at the right of MPP.

This technique could cause power loss when there are very rapid changes in solar radiation but this is not very common.

4.1.3 Incremental conductance technique (ICT)

MPP can be written as $\frac{dp}{dv} = \frac{dvi}{dv} = i + v\frac{di}{dv} = 0$

The ICT algorithm checks for $\frac{\Delta i}{\Delta v} = -\frac{i}{v}$ by saving previous sampled values i_b and v_b i.e., current and voltage values, respectively. The following are calculated, $\Delta i = i - i_b$, $\Delta v = v - v_b$ where i and v are current sample values of current and voltage, respectively.

If $\frac{\Delta i}{\Delta v} > \frac{i}{v}$ then the operating point is left of MPP, and $\frac{\Delta i}{\Delta v} < \frac{i}{v}$ means the operating point is right of MPP [14], [15].

The control V_{ref} changes depending on this check, it is adjusted to move the array operating voltage towards the MPP and at MPP $\frac{\Delta i}{\Delta v} = -\frac{i}{v}$. When MPP is reached, the operation is held at that point V_{ref}, unless a change in Δi is detected. This change will mean the weather conditions have changed and hence the MPP.

4.1.4 Constant reference voltage (CRV)

CRV compares the PV array voltage or current with a constant V_{ref} or I_{ref} respectively, which corresponds to photovoltaic V or I at MPP under specific conditions. The error signal drives the power conditioner that interfaces the PV array to the load.

4.1.5 Discussion of the MPPT control techniques

Incremental conductance is a very good technique for coping with changing atmospheric conditions contrary to the P&O/CRV, but ICT requires complex mathematical calculations compared to P&O/CRV [13]-[15]. P&O is quite good but it causes power losses with rapid solar variation. But with the advancement of DSP's both ICT and P&O can be implemented without a problem. CRV is simple to implement but it is not accurate as different weather conditions with changes in temperature/isolation are not considered.

4.2 MPPT technique

Perturb and Observe, being the most widely used MPPT technique in literature, was simulated and analysed in Chapter 2 (see Appendix 1 for the simulation model). Achieving the maximum power (MPPT control) and control of the voltage dc link are interconnected, for which reason the control of the inverter current is also discussed. Maximum power point tracking is done using an algorithm (using P&O method in this case) that perturbs the duty cycle of the dc-dc boost circuit (see Figure 4.4) and observes the change in power. The duty cycle is then increased or decreased in the direction of increasing power [15].

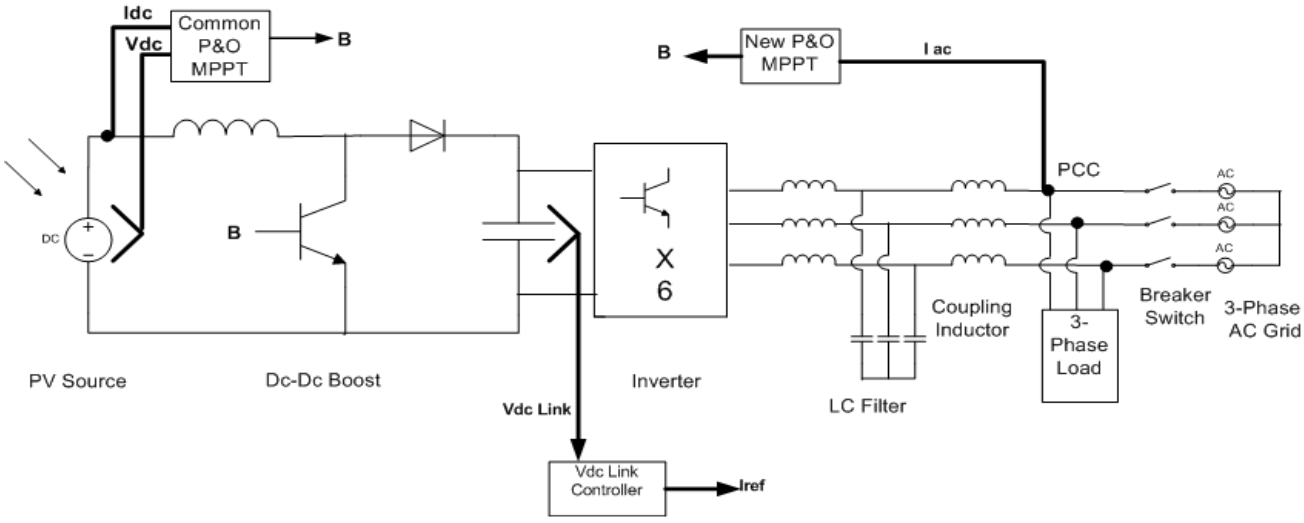


Figure 4. 4: MPPT controller for the conventional method and novel proposed approach

According to equation (2.3), $I = \frac{V_{inv}\angle\delta - V_g\angle\beta}{Z\angle\phi}$, the inverter ac side current, I, will depend on $V_{inv}\angle\delta$ since V_g and Z (impedance) are fixed in a grid connected system. V_{inv} and δ can be controlled according to the I_{ref} (inverter reference current) to deliver the available power into the grid.

4.2.1 Conventionally adopted P&O method

The dc-dc boost circuit could be used to extract maximum power from the PV panel. Power at the dc side is measured and the duty cycle of the boost circuit is increased. Power is measured again and the duty cycle is perturbed accordingly (see Figure 4.4). This extracted power changes the dc link voltage. The dc link controller uses the sensed dc link voltage value and compares it to a reference value of 780V (in the simulation) and changes the inverter reference current I_{ref} accordingly, which in turn regulates the PWM switches of the inverter.

Here the boost circuit extracts the maximum power independently, while the dc link controller maintains the dc link voltage by controlling the inverter current [16], [42].

Figure 4.5 shows the MPPT controller run at 50Hz to track the power using measured dc values. Full schematic diagram of the simulation model with conventional P&O MPPT is shown in Appendix 1

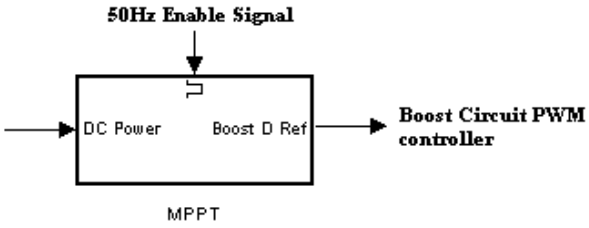


Figure 4. 5: MPPT controller for the conventional method

4.2.2 Novel AC side P&O MPPT technique

DC power at the PV side has always been used in literature for MPP tracking as discussed above. Power at the ac side has never been considered. In this research study, power (current) at the ac side could be measured to track the MPP, and the proposed method takes advantage of this interesting concept which is discussed below.

A sketch of the I-V and P-V characteristic at the PV side and the inverter side is shown in Figure 4.6.

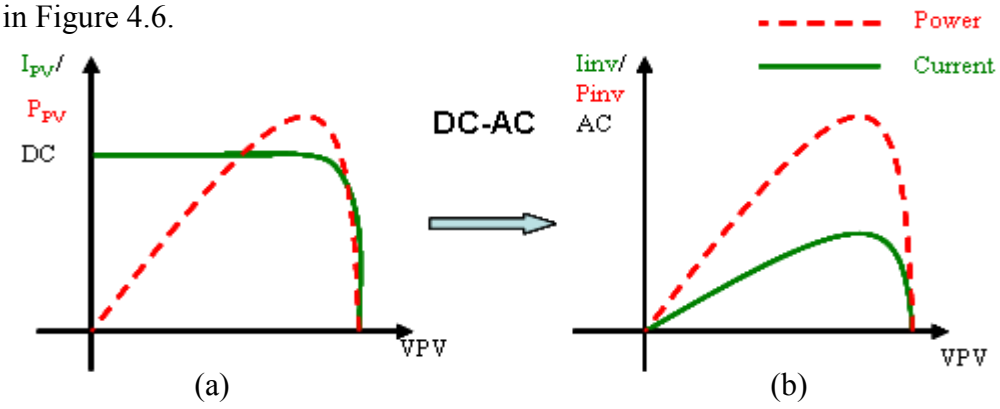


Figure 4. 6: Sketch of I-V and P-V characteristic of a PV panel and inverter

From Figure 4.6 it can be deduced that for a three phase inverter:

$P_{INV} = (P_{PV} - \text{Losses})$ (4.1)

$$I_{INV} = \frac{P_{INV}/3}{V_g} \quad (4.2)$$

Where:

P_{INV} is inverter output power

P_{PV} is input PV power

I_{INV} is inverter output current

V_g is grid voltage

The left (PV side) of Figure 4.6(a) shows the usual I_{PV}-V_{PV} and P_{PV}-V_{PV} characteristic of a PV Panel. This special power curve characteristic is utilized in the conventionally used P&O MPPT approach to extract the maximum power at the point when $\frac{dP}{dV} = 0$. When looking at the ac side (inverter side) as in Figure 4.6(b), the P_{INV}-V_{PV} and I_{INV}-V_{PV} characteristics seem to be linearly related as shown on the right of Figure 4.6 (losses are assumed to be fixed). This special I-V characteristic at the ac side can now be used to track the MPP by measuring the output current of the PV inverter since the grid voltage, V_g, at PCC is constant).

The new concept uses the same P&O MPPT algorithm explained for the conventionally used MPPT approach, except that it no longer measures the dc power (I_{dc} and V_{dc}). Instead the ac current output is acquired to perturb the duty cycle of the boost circuit as shown on Figure 4.7. Section 4.2.4 lists the advantages of this approach.

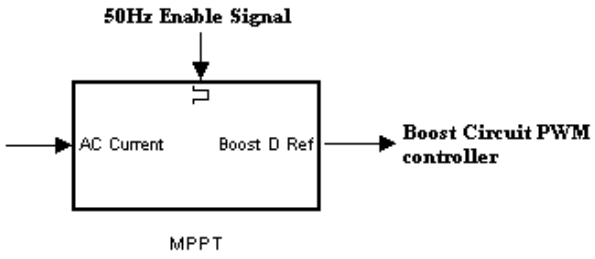


Figure 4. 7: MPPT controller for the novel approach

4.2.3 Algorithm for MPPT

AC side current rms (inverter output) is measured and the duty cycle of the boost circuit is increased. The rms current is measured again and the duty cycle perturbed accordingly in the direction of increased rms current (power) as shown in the control flow chart in Figure 4.8. This extracted power changes the dc link voltage. The dc link controller uses the sensed dc link voltage value and compares it to a reference value of 780V(in this case) and changes the reference current (inverter side) I_{ref} accordingly, which in turn regulates the PWM switches of the inverter.

Here the inverter side current extracts the maximum power with the use of the boost circuit, while the dc link controller maintains the dc link voltage by controlling the inverter current. The boost circuit depends on the inverter output current rms, to control the MPP. This novel method reduces the dc side sensor requirement for MPP tracking. See Appendix 4 for a full simulation model.

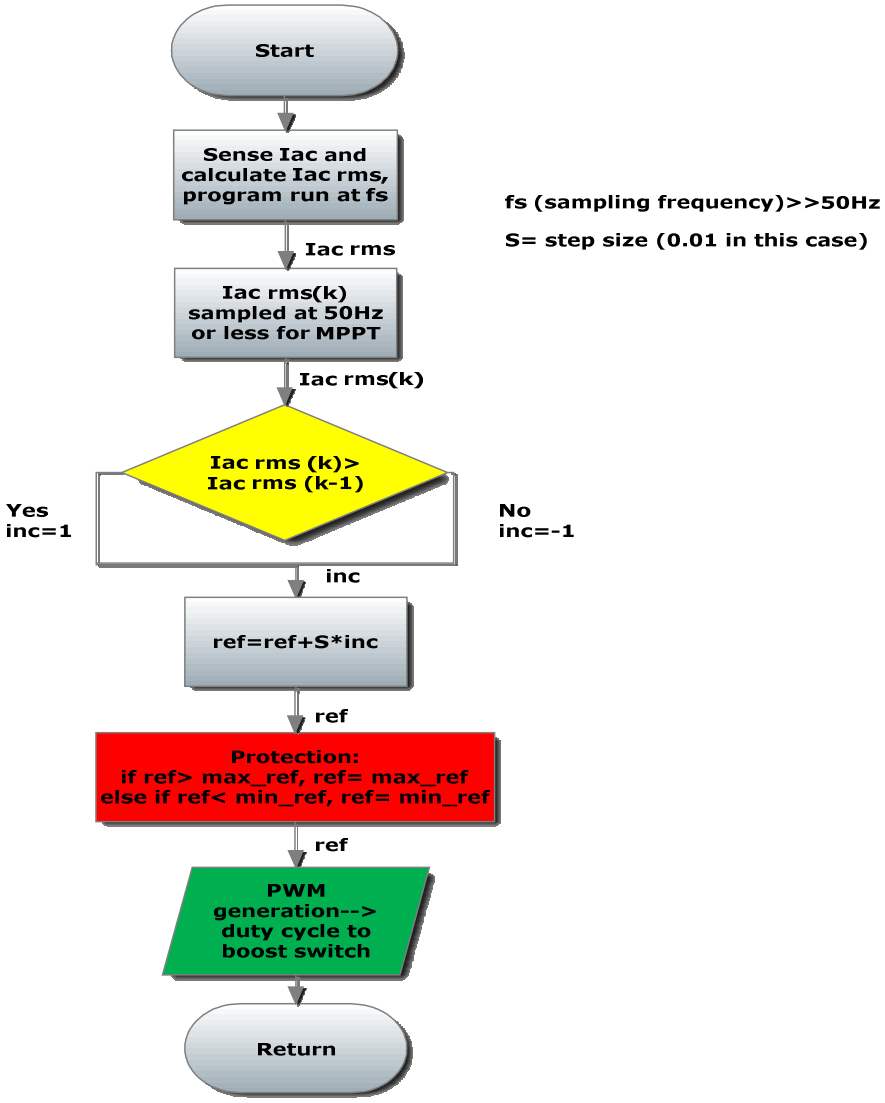


Figure 4. 8 : Control flow chart of the novel P&O MPPT method

4.2.4 Advantages of the new MPPT approach

- Only one ac current sensor is required to sense ac inverter current output for MPPT purpose in a balanced three-phase system.
- No dc sensors required, nor multiplier required to reveal the power in digital control. This simplifies algorithm and computation.
- Since no voltage (no power) measurement is required, this avoids additional software filtering for the oscillating PV voltage.
- For a three-phase system, a sensor of smaller rating is required compared to the conventional method as whole dc power is not measured, instead ac current in one of the phases (which reflects ac power) is sensed, which is small.

4.3 Simulation results

A PV curve of 3.4kW peak is used to simulate the photovoltaic source. Both the conventionally used MPPT approach and the novel approach are simulated in Simulink (tracking MPP at 50Hz) for a three-phase photovoltaic grid connected inverter whose results are shown below. Simulation models are shown in Appendix 1 and 4. Inverter V_{dc} link controller, controls the I_{ref} to keep the capacitor voltage (V_{cap}) to 780V as close as possible as shown in Figure 4.9.

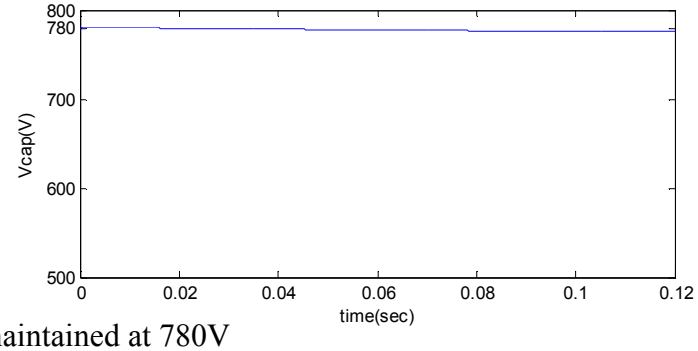


Figure 4. 9: V_{cap} maintained at 780V

Figures 4.10 and 4.11 show the power extracted using the conventional and novel approach, respectively. The dc power calculated in Figure 4.10 is used for MPP tracking, while the dc power shown in Figure 4.11 is just calculated to show that the novel approach extracts maximum power without any dc sensors.

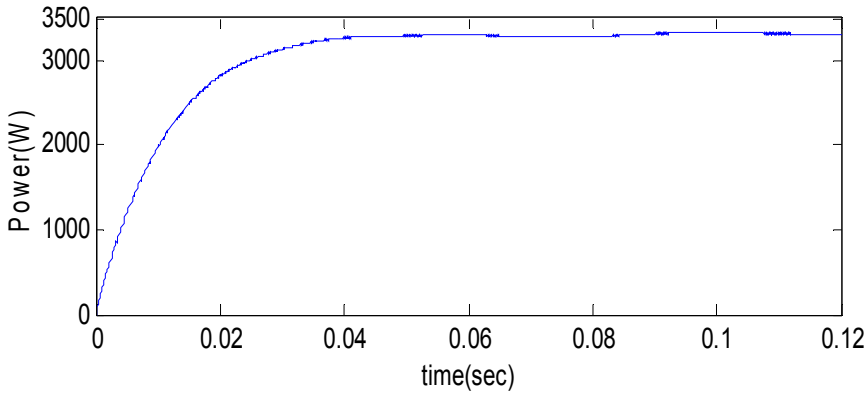


Figure 4. 10: Power from PV tracked using the MPPT algorithm using the conventionally used approach.

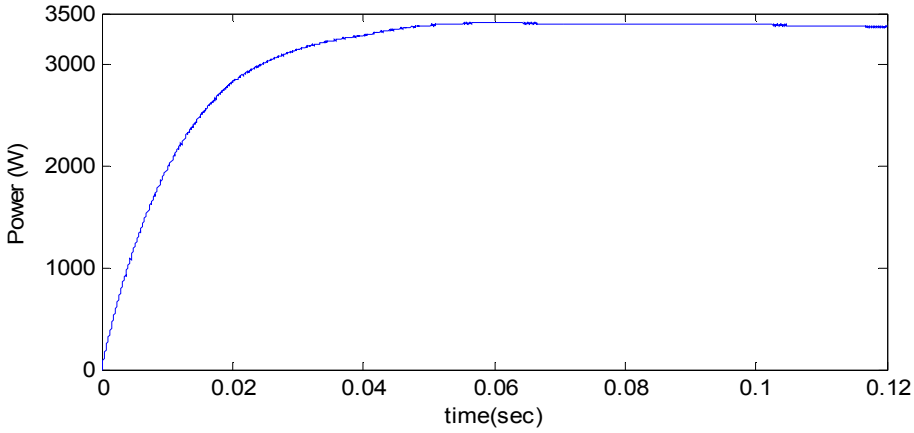


Figure 4. 11: Power from PV calculated to show the tracked MPP using the novel approach.

The simulation is run again with 1.7kW PV and 3.4kW PV, where the switching of the curve takes place at 0.4s. Figure 4.12 shows the extracted power from the panels using the novel approach, the power here is calculated only for verification purposes. Figures 4.13 and Figure 4.14 show the operating Vpv and Ipv against time respectively. Figures 2.19 to 2.21 of Chapter 2 showed results of the conventional approach under similar conditions.

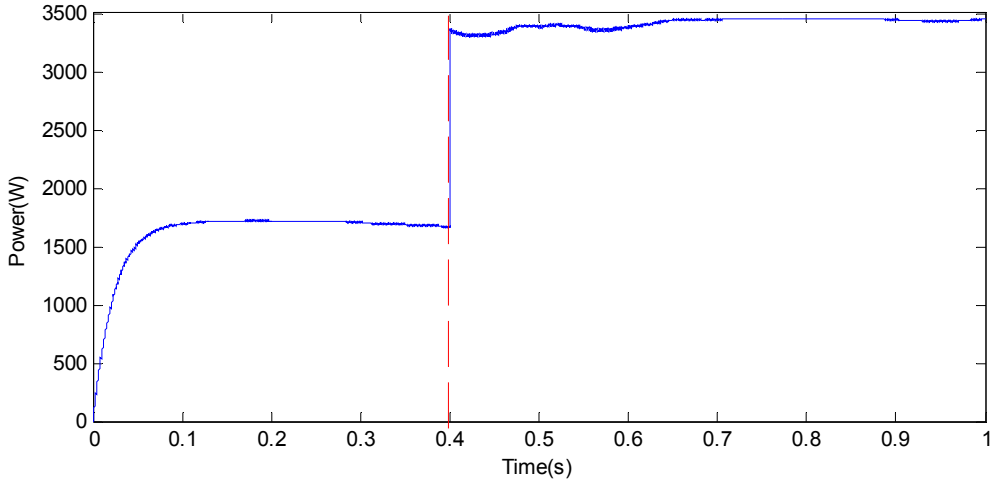


Figure 4. 12: Power from PV calculated to show the tracked MPP using the novel approach

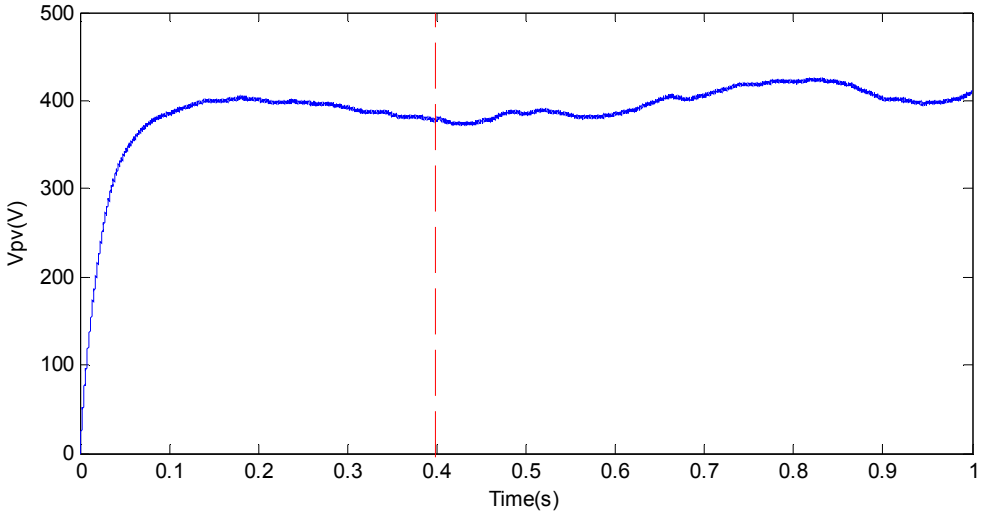


Figure 4. 13: Vpv operating point against time

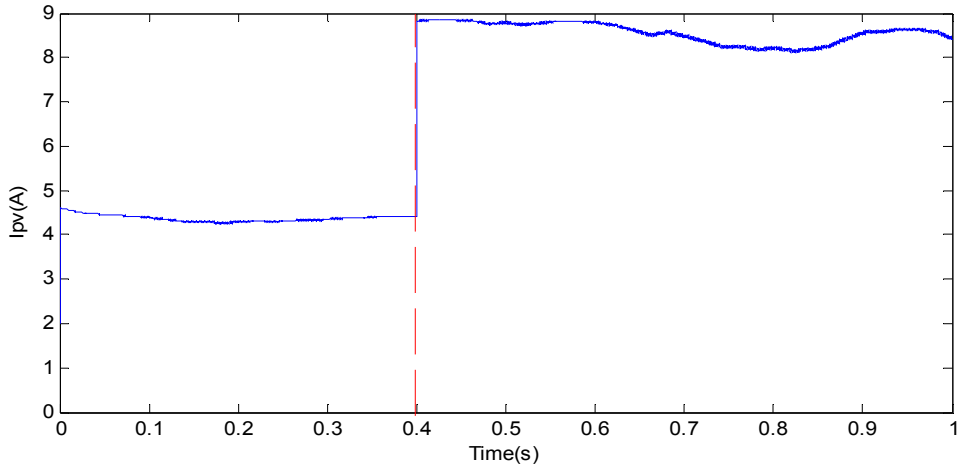


Figure 4. 14 Ipv operating point against time

4.4 Conclusion

The Chapter discussed the various MPPT techniques from literature and the need for a boost circuit to increase the voltage level and MPP tracking. It also discusses the conventional method for MPPT and then proposes a new ac side P&O MPPT approach.

The new proposed method brings a master-slave principle approach, where the inverter and the boost circuit are looked at as two different controlling stages. One of them can act as the master while the other as a slave. Both of them can be used vice versa to control the overall transfer of maximum power to the grid from a PV source.

Simulation results for both the conventional and novel approach show the working model of the system. The new proposed approach uses only ac side grid current for MPPT. The injected grid current is normally sensed in a grid connected system. As a result the new method does not require any additional dc side measurements, making it a dc sensor-less MPP tracking approach. Furthermore, no compromises are made in the power tracking capability (compare Figure 4.10 with 4.11 and 2.19 with 4.12) and serving some further advantages as mentioned in Section 4.2.4.

Chapter 5

5. IMPLEMENTATION OF THE THREE-PHASE GRID CONNECTED INVERTER: HARDWARE, SOFTWARE AND CONTROL

5.0 Introduction

Chapters 2 and 3 show simulations of the power electronic systems, and their significance in the analysis and design of the entire three phase grid connected inverter system.

However computer simulations cannot be taken as a substitute for a hardware prototype. Power electronics computer simulation and a hardware prototype are complementary to each other. A laboratory prototype of a three phase grid connected dc-ac inverter has been constructed in order to validate the simulated grid connected system and to test the proposed anti islanding technique. The software control program developed in Simulink is run on dSpace DSP DS1104.

This Chapter reports the development of the laboratory prototype, the necessary interface circuits, the software control algorithm and the GUI (graphical user interface) developed. The Chapter concludes with experiment results of the grid connected inverter system, interface circuits and a discussion of the interaction between hardware and software.

5.1 Implementation of a laboratory prototype

5.1.1 Power circuit configuration and components parameters

A 5.625 kW, 25A, 50 Hz three-phase grid connected inverter with a rectified dc source was built with the necessary control and protection circuitry. The rectified dc source is used in place of the PV Panel for experiments. A dc-dc boost converter is incorporated between the dc source and the inverter. The 400V L-L grid is stepped down to 130V L-L using a three-phase isolated transformer, so that the minimum boosted dc link voltage level required to operate the inverter can be set at 265V and the normal controlled voltage level is set to 300V. The power circuit layout of the grid connected inverter prototype is shown in Figure 5.1. Figure 5.1 shows the full inverter system along with the necessary interface ciruits. The three-phase transformer has the capability of stepping down the 400V L-L to 87V L-L (3.75 kW), 130V L-L (5.625 kW) and 173V L-L (7.5kW). All components are designed for the full power range of 5.625 kW but experiments have been carried out only up to 2 kW. Figures in Appendix 6 show the hardware setup in progress for the project.

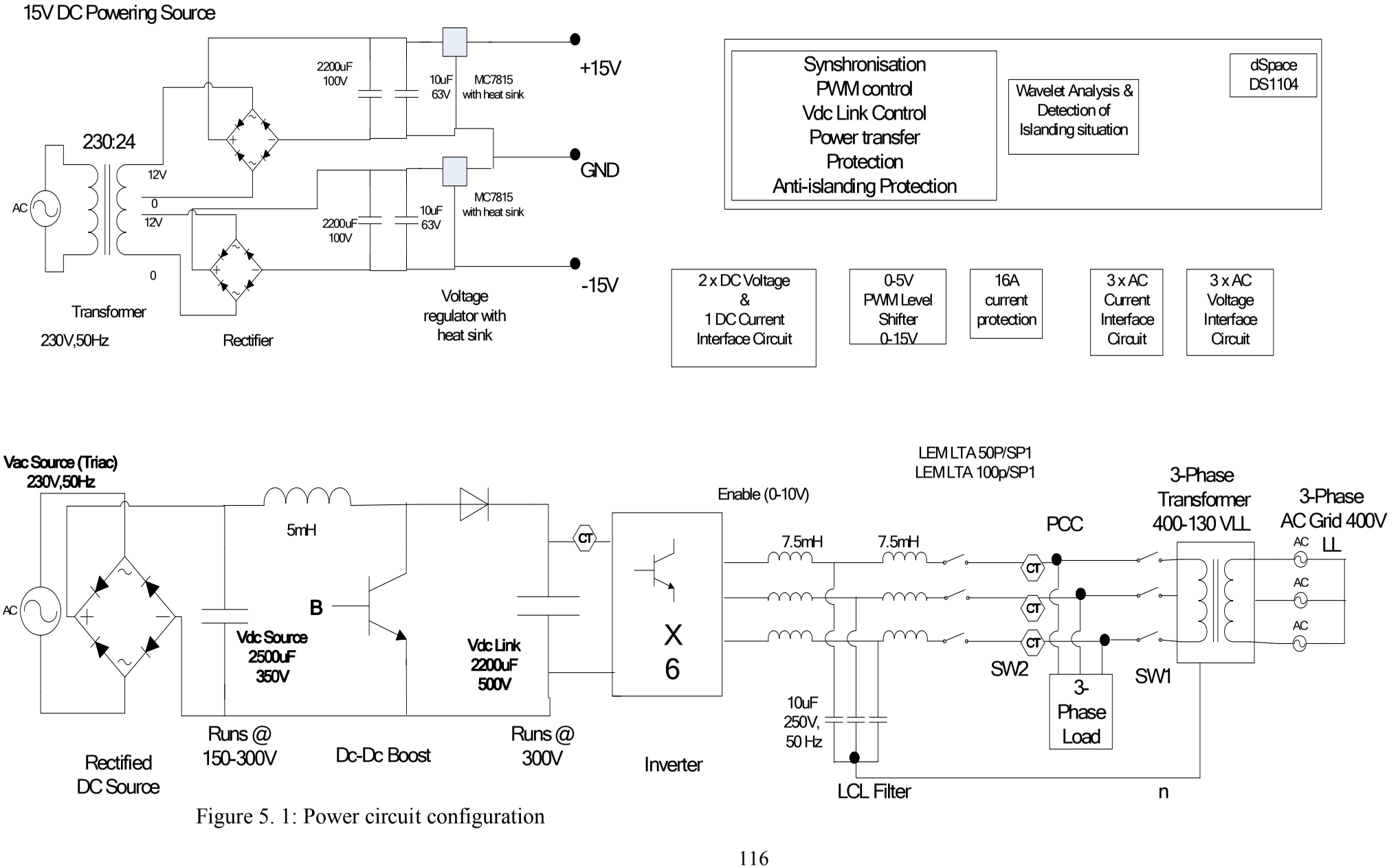


Figure 5. 1: Power circuit configuration

5.1.2 Variable rectified dc source

A 230V ac voltage variac is used to generate the dc source using a single phase full bridge rectifier and a 2500μF, 350V electrolytic capacitor as shown in Figure 5.1. By varying the ac output of the variac the rectifier can produce a variable dc source in the range 150V to 300V. When the dc voltage is below 300V the boost converter is used to step it up to 300V.

5.1.3 Inverter

The inverter was a three phase inverter from SmartPower ATE Ltd (see www.smartpowerate.com). This is a standard six-switch voltage source inverter based on TOSHIBA MG150J2YS50 (600V,150A) IGBT devices which is run in voltage control mode. The IGBT device comes as a dual IGBT module that can each form a single leg of the inverter. Four 630V, 4.7μF high frequency dc bus decoupling capacitors are used to overcome lead inductance between the large dc bus electrolytic and the transistor modules. The maximum dc link voltage is kept below 450V in order to allow a generous safety margin on the IGBT voltage. This dc link voltage does not allow us to directly connect to a 400V line to line AC mains so a three-phase transformer has been used. This transformer also provides isolation to break the loop between the non-isolated rectifier output and the mains. A PWM level shifter is designed and built to match voltage levels of the switching signals generated by the DSP with the inverter's gate driver card.

5.1.4 Boost switch and diode

Another TOSHIBA MG150J2YS50 IGBT device (one leg consisting of two switches) is used to provide the boost switch and diode. The bottom switch with the anti-parallel diode of the leg is used to represent the boost switch while the top anti-parallel diode represents the diode of the boost circuit. The top transistor is disabled by tying both the gate and the emitter of the transistor together. The PWM level shifter is used to match voltage levels of the boost switching pulses generated by the DSP with the boost switch gate driver card.

5.1.5 Boost inductor and capacitor

The boost capacitor in Figure 5.1 which is also the dc link capacitor serves two main purposes:

1. It maintains the dc voltage with a small ripple in steady state.
2. It serves as an energy storage element to supply the power difference between the available source power and injected power.

The average voltage across the dc capacitor is maintained constant. The inductor is used to extract power from the lower voltage source when the boost switch is on and dump this power into the high voltage capacitor when the switch is off, thereby serving as an energy storage between the two voltages. The average voltage across the inductor is zero.

According to equations (3.6) and (3.7) from Chapter 3:

@ full power: $I_{out} = \frac{P_{out}}{V_{out}} = \frac{25A*75V*3}{300V} = \frac{5625W}{300V} = 18.75A$, $R = \frac{V_{out}}{I_{out}} = \frac{300V}{18.75A} = 16\Omega$

@ 450W power: $\frac{2A*75V*3}{300V} = \frac{450W}{300V} = 1.5A$, $R = \frac{300V}{1.5A} = 200\Omega$

Therefore:

$$C \geq \frac{0.75*300V}{6*16*20kHz} = 117.2\mu F$$

Where Vr = 6V @ 2% (pk-pk) voltage ripple

and $L \geq \frac{(1-0.5)^2 0.5*200}{2*20kHz} = 1.88mH$

The minimum values required for the boost inductor and the dc link capacitor are 2mH, 25A and 120μF, 500V respectively, to operate in the region of 450W to 5625W with a normally controlled dc link of 300V.

The boost inductor and the dc link capacitor values used for the hardware prototype are L=5mH, 25A and C=2200μF, 500V as they give ample margin.

Now the minimum load required to keep dc link boost continuous when boost converter is operating can be calculated using:

$$R \leq \frac{2Lf}{(1-D)^2 D}, \; R \leq \frac{2*5mH*20kHz}{(1-0.5)^2 0.5} = 533\Omega$$

$$I_{out} > \frac{V_{out}}{R} = \frac{300V}{533\Omega} = 0.56A \text{ dc}$$

Therefore it is concluded that with the available boost inductor value (5mH), to switch on the boost converter, the inverter has to be operating and transferring at least 150W of

active power to the grid. If any power below 150W is transferred using the boost converter, the dc link controller is expected to become unstable, fluctuating quickly between highest and lowest duty cycle in order to maintain the dc link stable.

5.1.6 Step down transformer

The three-phase 400V L-L grid is stepped down using a 5.625 kW, 25A three-phase isolated transformer with delta connected primary windings and four wire star connected secondary windings. The transformer provides voltage matching and isolation between the VSI and grid network. The transformer from Merrimack Transformers Irl. Ltd was designed to have three different secondary voltages that are 87V, 130V and 173V rms L-L (i.e. 50V, 75V and 100V rms L-N respectively) of which 130V LL (5.625 kW) is used as the 'stepped down grid' for the prototype. The primary (high voltage) side is connected to the grid while the secondary side is connected to the inverter. The secondary side produces an isolated neutral which is connected to the isolated neutral generated at the end of LCL filter on the inverter side (see Figure 5.1).

5.1.7 Filter inductors

An LCL filter (T filter) with inductors at input and output was chosen to present a high impedance at switching frequencies to both source (inverter) and load (ac mains). The filter prevents high order switching frequency harmonics produced by the VSI from entering the grid and thereby presenting a clean sinusoidal waveform at the output. The output of the inverter and LCL filter is shown in Figure 5.38. The LCL filter is designed by using six inductors and three capacitors as shown in Figure 5.1. Three inductors

(L=7.5mH and R=0.6Ω) were available in the laboratory. Simulations showed that inductors of this value with the chosen capacitor (see Section 5.1.8) produced acceptable filtering; therefore three more inductors were built. Section 2.10.6 and Figure 2.14 in Chapter 2 discusses the frequency response of the LCL filter. Inductors with parameters 20 A, L= 7.5mH and R=0.6Ω were constructed using iron powdered core type E450-33 produced by Micrometals Inc (see www.micrometals.com). Enameled copper wire is used to wind the bobbins which are then plugged on the middle leg of the E core and fixed using terminals and glue tape appropriately. Approximately 163 to 164 turns are required to achieve the above specifications. The inductors were tested with Stanford Research Systems LCR Meter SR715 (see www.thinksrs.com) at the frequencies 100Hz, 1k Hz and 10k Hz to be precisely calibrated. Iron powder is typically used to produce high "Q" inductors and it is preferred core material due to its stability, high "Q" frequency response and power handling capabilities.

5.1.8 Filter capacitors

The filter capacitors are connected in star by linking one terminal of each of the capacitor between the two inductors on each phase, and joining the three other terminals of each capacitor together to form a three-phase LCL filter. The chosen filter capacitor value is 10μF, 250V, 50Hz. The value reflected a compromise made to reduce the size of L to keep it compact and reduce C in order to reduce the reactive current component absorbed by the filter capacitors. The LCL filter is connected to the secondary side of the transformer (PCC) via a circuit breaker SW2, before the I and V sensors as shown on Figure 5.27.

5.1.9 Switching device protection

During testing a resistor of 12.7 Ohms, 10 A is used to connect the dc link capacitor to the inverter dc link terminals in order to protect the six switches from unintentional shoot-through fault.

5.1.10 Cabinet and front measurement panel

A cabinet with five shelves to hold all the components was built. A front see-through PVC plastic sheet is cut and appropriately drilled so that the panel meters and terminals could be mounted.

Five analogue voltmeters and three analogue ammeters have been mounted on the front panel. Two dc voltmeters indicate the dc source and dc link capacitor voltages. Three (one per phase) ac voltmeters indicate the voltages at PCC (point of common coupling/ synchronized voltage). The three ammeters (one per phase) measure the currents injected into the grid.

One three-phase digital multimeter model M850-MP1 produced by Howard Butler Ltd (see http://www.hobut.co.uk) has been mounted for measuring and displaying phase and line volts, phase amps, frequency, active, reactive and apparent powers, active and reactive energies, power factor, voltage and current distortion and other parameters. Current transformers (in each phase) are used for connecting the multimeter. The transformation ratio is 25:5.

Terminals that can be used for direct sensing of dc and ac voltages (for verification purposes) at different nodes of the power circuit have been mounted. Terminals to get

access for connections from interface circuitry to the DSP controller have been mounted as well. (See Appendix 6 for pictures of the full cabinet and front measurement panel).

5.1.11 Interface circuits

The dc voltages and ac voltages (PCC) are brought into the DSP controller through the dc and ac voltage measurement interface cards respectively.

LTA 50P/SP1 and LTA 100P/SP1 (with 1:1000 transformation ratio) transducers produced by LEM (see www.lem.com) are used for measuring the dc side and ac injected currents. 23 Ω resistors have been used at the output of the transducers to transform the current signal into a voltage signal, which corresponds to 23mV/A. Two windings have been used which makes the final output 46mV/A in all cases. Transducer output signals are brought into the DSP controller through the dc and ac current measurement interface cards respectively.

Six PWM pulses from the CP1104 controller panel reach the inverter via the PWM level shifter. One boost switch pulse from the CP1104 controller reaches the boost switch via the PWM level shifter. Two enable signals (one to the boost and one to the inverter) directly reach the inverter and boost in order to enable (10V) and disable (0V).The design of different interface circuits is looked at in detail under the Sections 5.1.15 and 5.1.16.

5.1.12 Auxiliary dc source to power the circuits

An auxiliary dc source that can provide +15V, -15V @ 1A and ground, is used to power the inverter gate driver, boost gate driver, the current and voltage interface circuits, PWM level shifter and the current protection circuit. The single phase 230V, 50Hz supply is stepped down using a 230:12-0-12 (2A) transformer and two bridge rectifiers, capacitors and MC7815 voltage regulators are used to produce the dc outputs as shown in Figure 5.2.

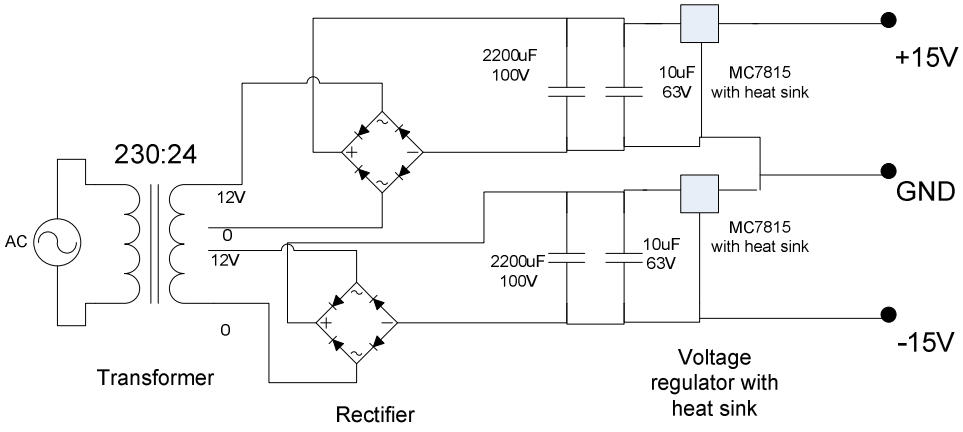


Figure 5. 2 : DC source to power the circuits

5.1.13 Circuit breakers

Two dedicated circuit breakers SW1 and SW2 are used in the setup shown in Figure 5.27. The grid can be disconnected from the inverter when ever required by opening SW1. SW1 is opened to put the inverter into islanded mode; it is used to carry out the tests on the anti-islanding algorithm.

Circuit breaker, SW2 is used to manually synchronize the inverter on to the grid voltages, when the inverter generated voltages are within its synchronization error limits (+/-5V).

5.1.14 Design and fabrication of the current protection circuit

The laboratory three phase supply is protected by a 16A miniature circuit breaker but as an electromechanical circuit breaker cannot operate quickly enough to protect the semiconductor devices, so a fast 16A hardware based current protection circuit is designed and constructed to protect the inverter switches, wiring and the power system as a whole. The voltage out from the LEM current transducer (dc side, 2 windings x 23mV/A) is compared to the 16A reference voltage (16A*46mV/A≈0.714V) using a comparator LM339AN, whose output goes through a series of NAND gates, before going to the inverter. The reference voltage of 0.714V is created at the midpoint of a voltage divider circuit of 1k and 20k Ω resistors connected in series to the 15V dc supply. The enable signal from the DSP controller is tied to the over current protection part of the circuit which enables the inverter if the current is within the operating limits. A reset switch (with a LED light indicator) is incorporated to reset the circuit after over current protection has tripped the inverter output. The circuit diagram is shown in Figure 5.3.The circuit has been tested by giving voltages corresponding to the over current voltage reference (16A, 0.714 V) and responds as expected, protecting the hardware by disabling the inverter from state “1” to state “0”.

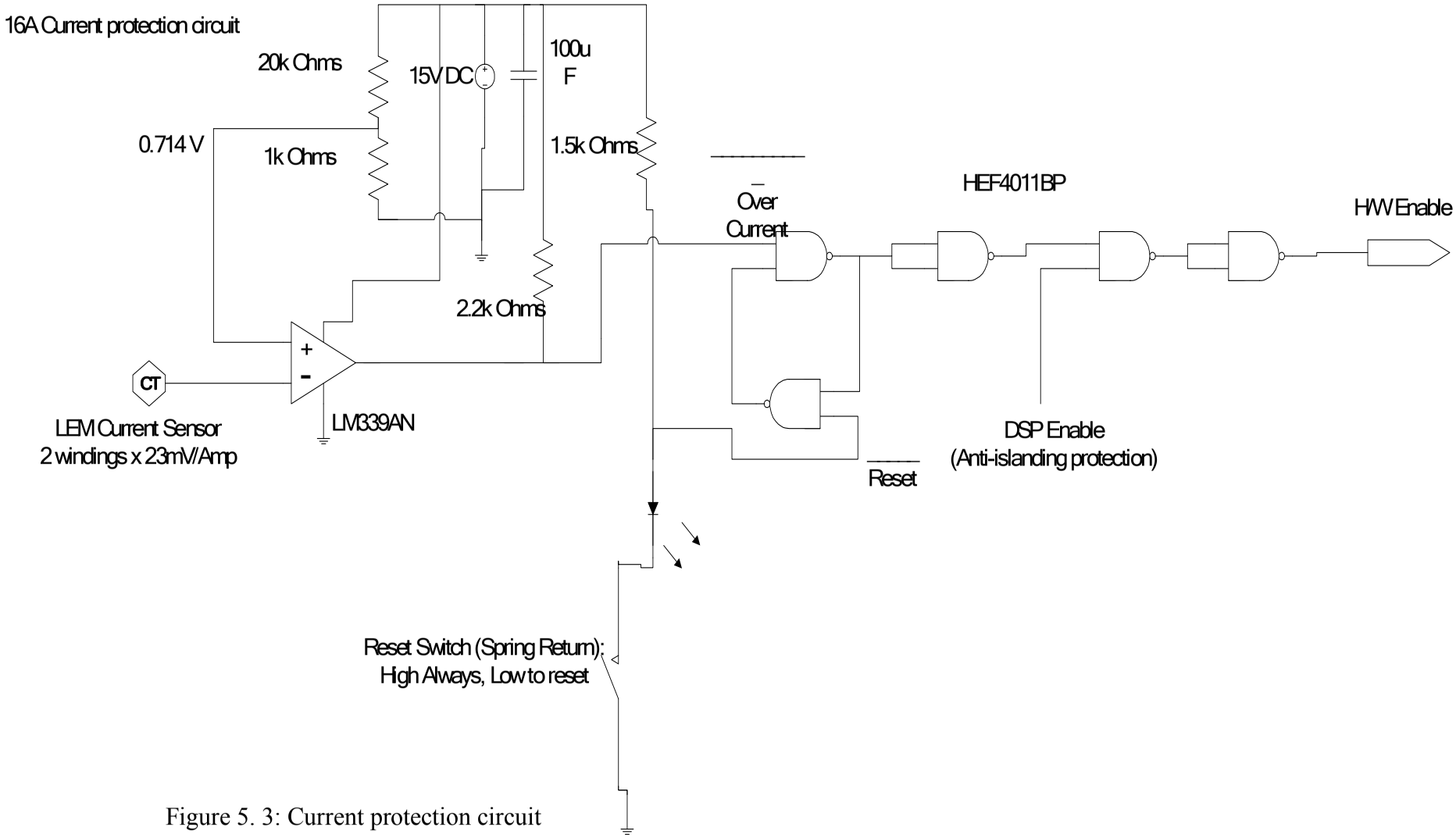


Figure 5. 3: Current protection circuit

5.1.15 Design and fabrication of the measurement interface circuitry

This section provides a description of the hardware circuits developed for the DSP controller to communicate with the constructed inverter. Measurement signals that are sensed for control purposes need conditioning before being fed into the DSP and actuator signals that are given to the inverter by the DSP need to be appropriately conditioned to be fed into the inverter and the boost gate drivers.

The measurement interface card, as the name suggests is the interface between different current and voltage signals used for control purposes and the DSP, as represented in Figure 5.4. Eight different current and voltage signals have to be fed in to the DSP for control and monitoring purposes.

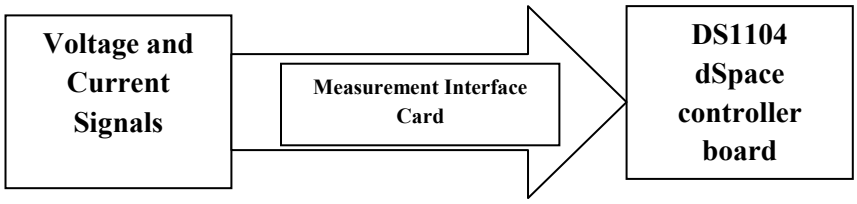


Figure 5. 4: Measurement interface card

The DSP used for this purpose (DS1104) can handle only -10V to +10V input signals. Therefore an interfacing circuit is required, which can output appropriate voltage signals. Interface cards have to be designed for handling eight measurements:

a) 400 V ac Pk - grid phase voltages (for each phase)

b) 1000V dc -for inverter dc link

c) 600V dc- for dc source voltage

d) 25A ac Pk - for injected currents (per phase)

e) 25A dc- for dc source current

The voltage and current signals are passed through this circuitry for conditioning and then acquired at the ADC sampling frequency (5 kHz). The attenuator stage of the measurement interface circuits provides a high impedance barrier with built in redundancy for safety. Figure 5.5 shows the different steps involved in conditioning the signals.

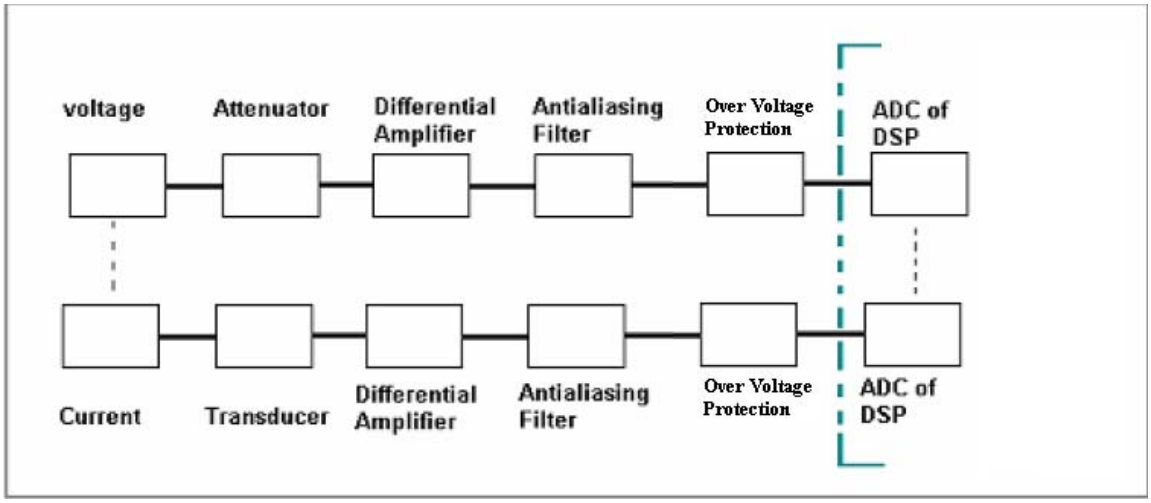


Figure 5. 5: Measurement interface card circuitry

The purpose of each stage is explained in the following section:

1. Attenuator/transducer: The voltage signal is sensed and passed through a resistive network where it is attenuated to a lower level. The live and neutral of each phase are measured differentially therefore the same resistive network exists on both terminals. 1 % precision resistors are chosen to give accurate measurements and this resistive network avoids use of bulky and costly transformers for the attenuation stage. The current signal is passed through a current transducer (LEM, LTA 200-S) and a voltage signal proportional to that is obtained.

2. Differential amplifier: The difference of the signals at inputs is amplified at this stage. The Common Mode Rejection (CMR) property of this stage helps to reduce the incoming noise and only the signal of the interest is amplified. The circuit design of the differential amplifier (TL084) is shown here in Figure 5.6.

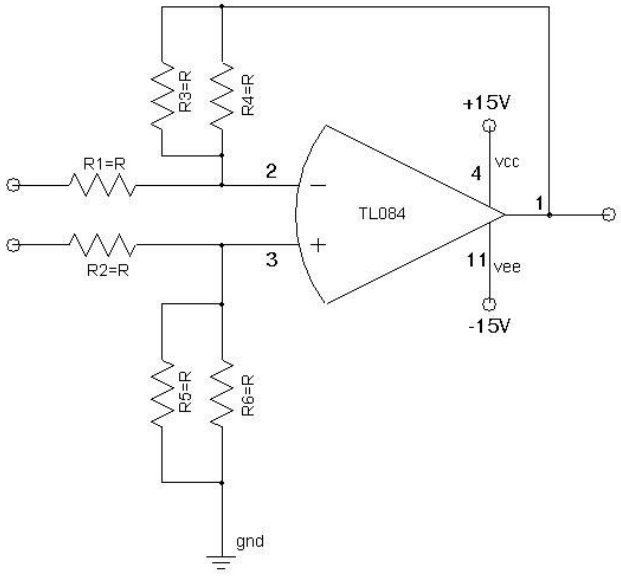


Figure 5. 6: Differential amplifier stage

The ac gain of this stage is designed to be 0.5 for the voltage channels and 1 for the current channels.

3. Anti aliasing filter: This low pass filter helps to remove the high frequency noise, which can cause aliasing effects upon sampling of the signal. This filter was designed to remove any noise signals above 500 kHz (–40 dB amplitude distortion) keeping in mind the sampling frequency of the analogue to digital converter (ADC) channels of DSP. It was decided to build Butterworth filters because of their smooth response in pass band frequency range. The cutoff frequency of the filter is given by equation below:

$$F_c = \frac{1}{2\pi RC}$$

The value of R and C can be designed based on this equation by fixing the cutoff frequency. The gain of the filter is given by equation below:

$$G = 1 + \frac{R_f}{R_1}$$

For voltage measurement

The ac gain of the third order filter stage is 2.96. Based on this value the resistors R_1 and R_f can be decided (see Table 5.1). A third order filter was designed to pass 2.5 kHz (50^{th} Harmonic of 50 Hz signal) signal with magnitude error of 0.04% and phase error of 3.96^{o} for the voltage measurement channels. The circuit diagram of the third order filter is shown in Figure 5.7.

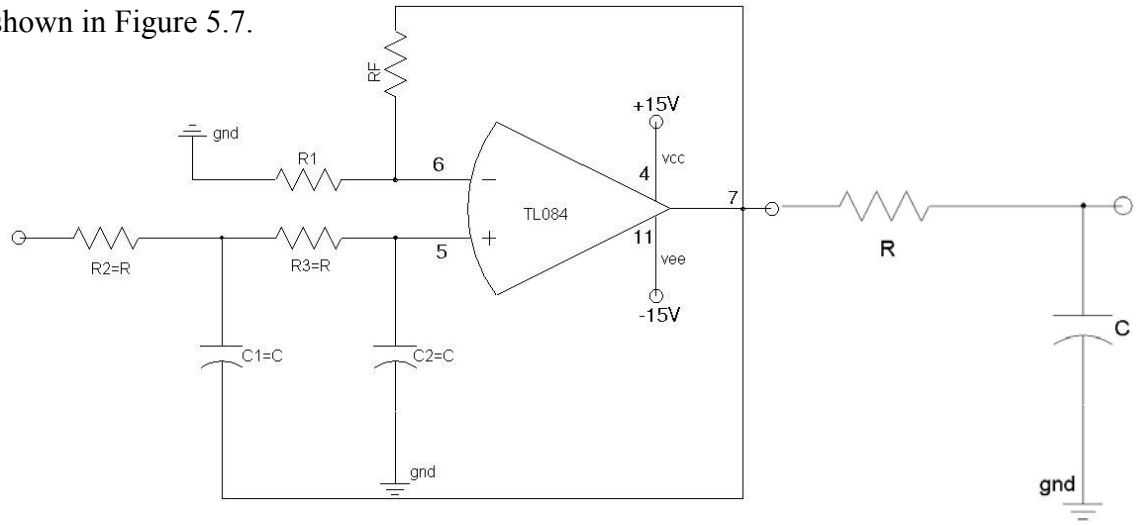


Figure 5. 7: Circuit diagram of 3rd order Butterworth filter

For current measurement

A fifth order filter was designed to pass 20 kHz signal with magnitude error of 6% and phase error of 27^{o} for the current measurement channels. A fifth order filter with a high cutoff frequency is necessary in order to measure and replicate the current waveforms. The circuit diagram of the fifth order filter is shown in Figure 5.8. The ac gains of the fifth order filter are 1.152 and 2.235 (see Table 5.1).

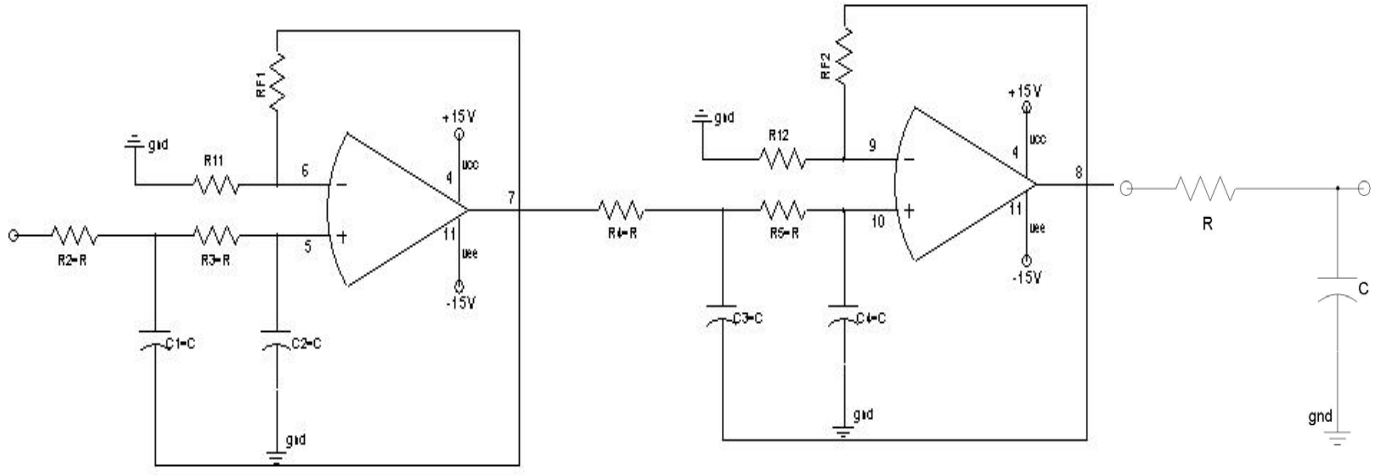


Figure 5. 8: Circuit diagram of 5^{th} order Butterworth filter

Any high frequency noise that might have entered the circuit is removed by keeping the low pass filter stage at the end of the Butterworth filters and at the point where signal is read by the DSP. A 470 kΩ, ¼W resistor is added in series at the point where the probes connect the circuit to the ADC unit in order to read clean sinusoidal signals.

4. Over voltage protection

The signals pass through an over-voltage protection circuit shown in Figure 5.9 before they are read by the ADC ports of the DSP. The ADC of DSP is very sensitive to voltage input other than the specified level. Therefore, the protection circuit ensures to keep the output voltage between -10 and +10 Volts. Resistors of 1% precision and zener diode BAT85 based voltage clamping circuit is added to the end, of each of the measurement interface circuits.

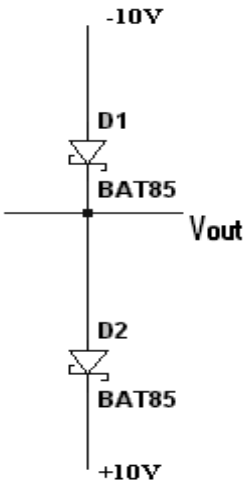


Figure 5. 9: Over-voltage protection circuit

The simulation study of the designed circuits has been carried out in the simulation package LT Spice. The schematic diagrams of the five different measurement circuits and their simulation results are given in Figures 5.10 to 5.20.

Each stage of the circuit was built and tested individually and then put together for a breadboard testing. Differential mode and common mode tests were carried out on each of the measurement channels of the circuit to ensure their reliable operation. The test results were satisfactory and show the input signals are conditioned as expected; also ac and dc gains of the circuits were consistent in the tests carried out. Also differential and

common mode frequency tests were carried out on the circuit. Finally they have been built on the Vero Board whose hardware test results are shown in Figures 5.28 to 5.30 in Section 5.4. The hardware circuit implementations are shown in Appendix 6.

Table 5.1 below gives the Figure number, parameters and the respective Figure numbers showing results, for all the different measurement interface circuits.

Table 5. 1: Measurement interface circuit parameters

Figure	**Interface circuit**	**Anti-aliasing filter gain** $G = 1 + \frac{R_f}{R_1}$, **R_f,R_1-Ω**	**Low pass filter, R-Ω,C-μF**	**Simulation result shown in Figure**
5.10	ac voltage	R_f=100k, R_1=51k, G=2.96	R=180 C=0.01	5.11 and 5.12
5.13	dc link	R_f=33k, R_1=51k, G=1.65	R=180 C=0.01	5.14
5.15	dc source	R_f=100k, R_1=51k, G=2.96	R=180 C=0.01	5.16
5.17	ac current	R_f=20k,R_1=130k, G=1.152 R_f=160k, R_1=130k, G=2.235	R=100, C=0.01	5.18
5.19	dc current	R_f=20k, R_1=130k, G=1.152 R_f=160k, R_1=130k, G=2.235	R=100, C=0.01	5.20

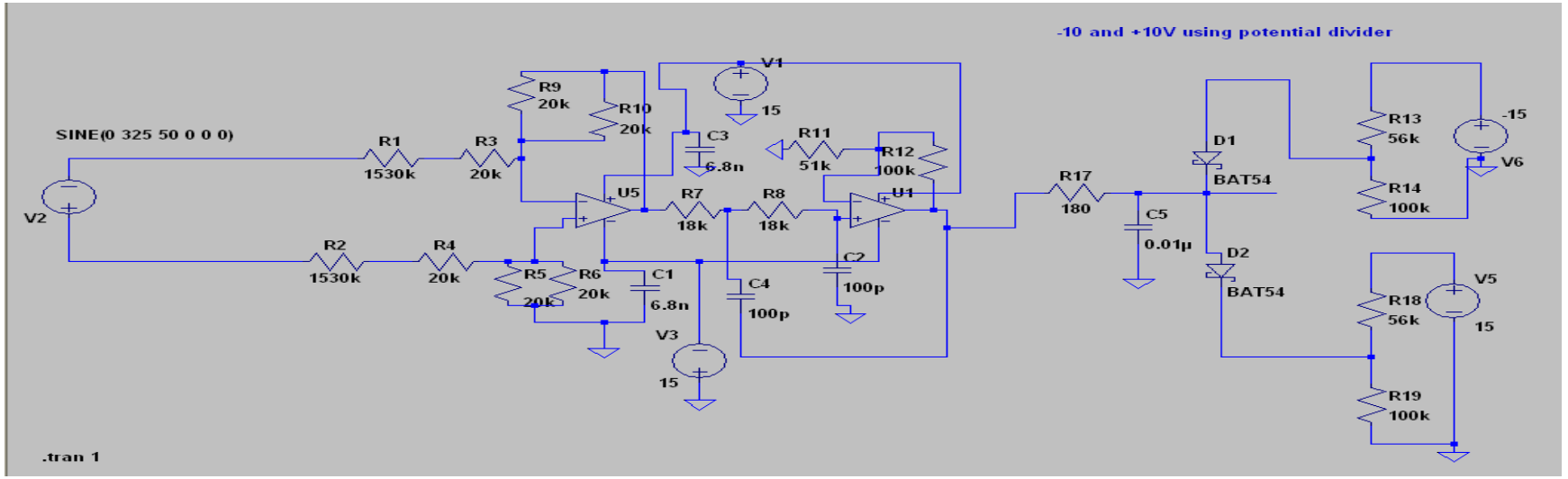


Figure 5. 10: AC voltage interface circuit

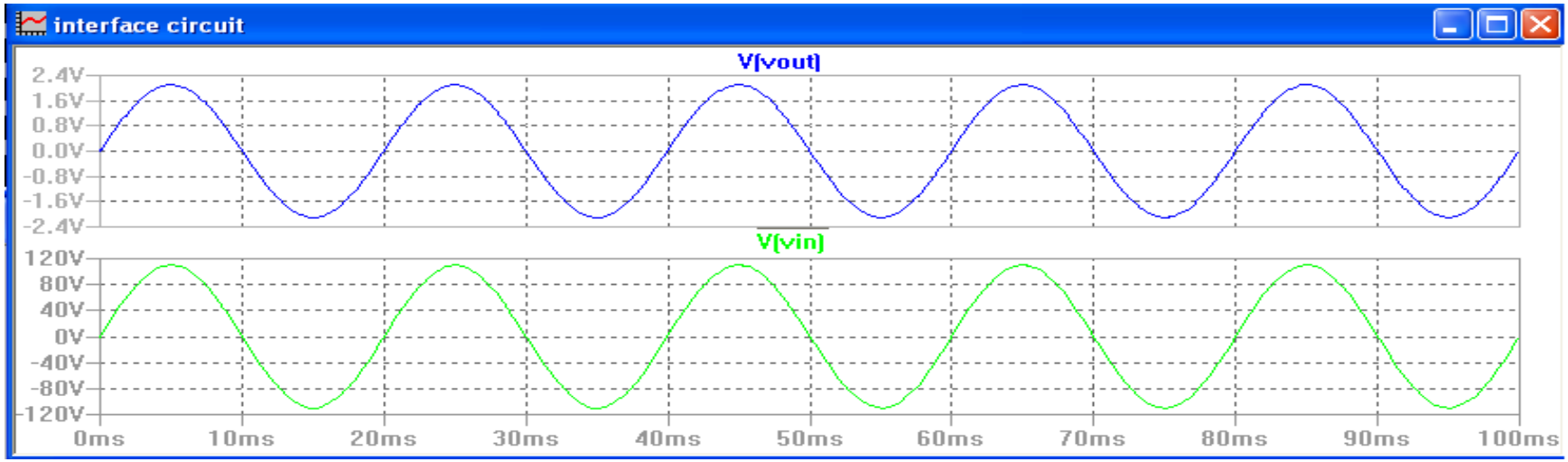


Figure 5. 11: Simulation result of the ac voltage interface circuit

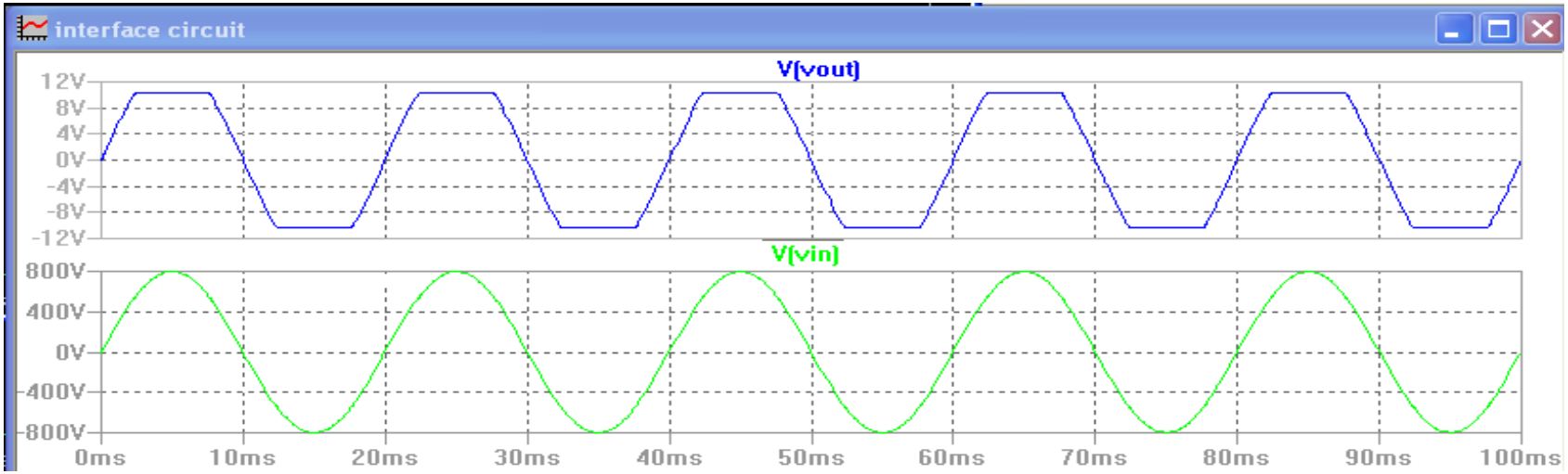


Figure 5. 12: Reaction of ac voltage interface circuit to high voltage, over voltage protection circuit in action

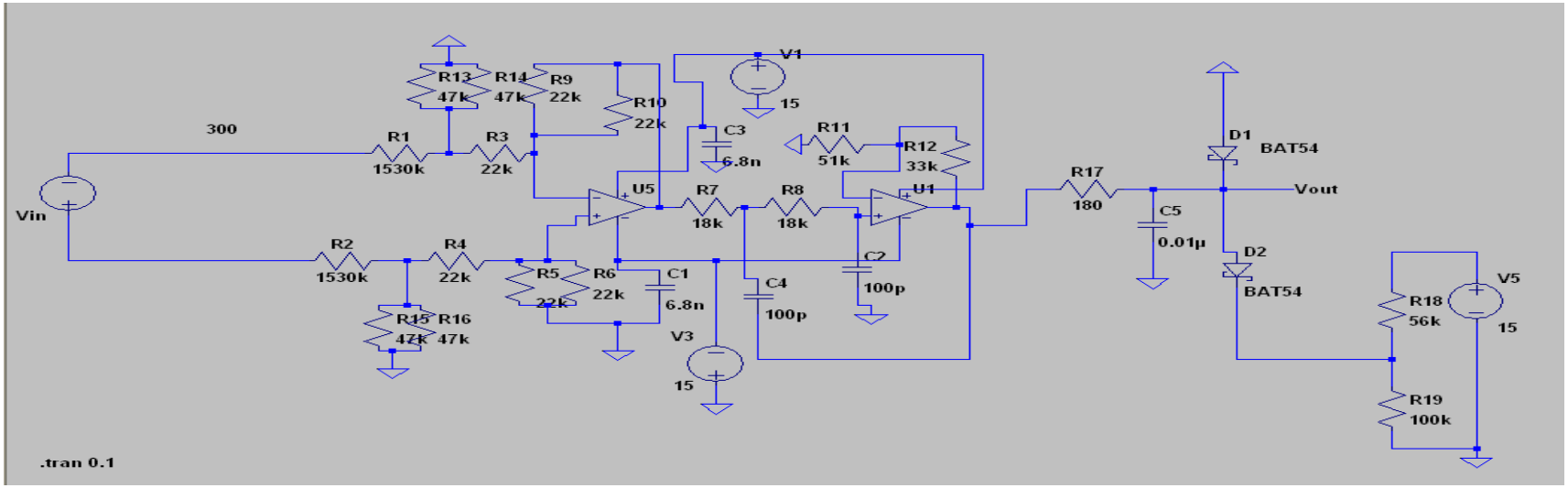


Figure 5. 13: DC link interface circuit

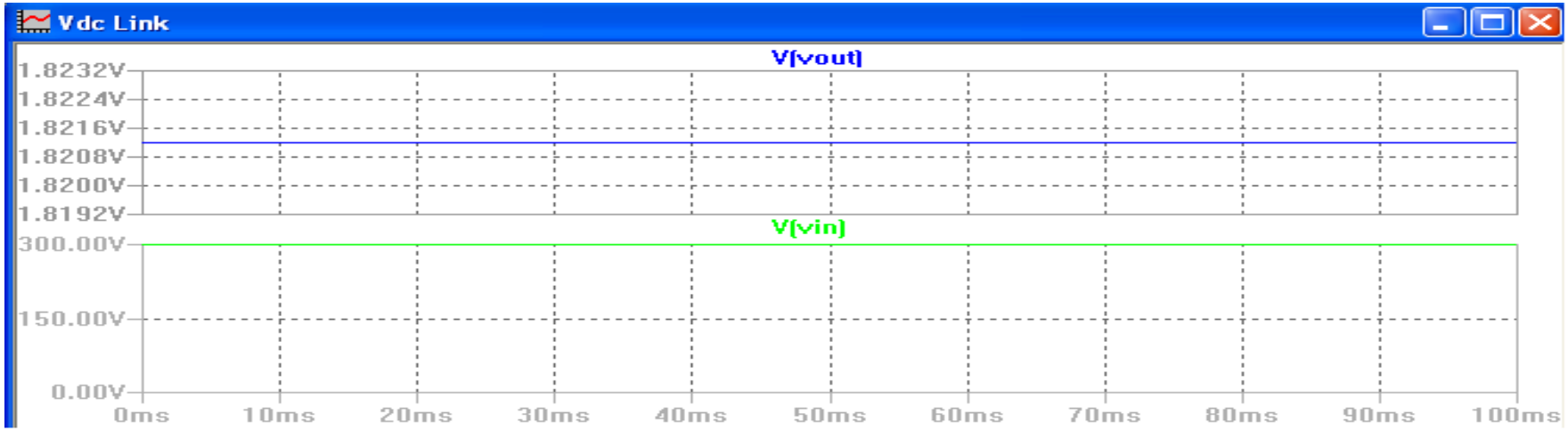


Figure 5. 14: Simulation result of the dc link interface circuit

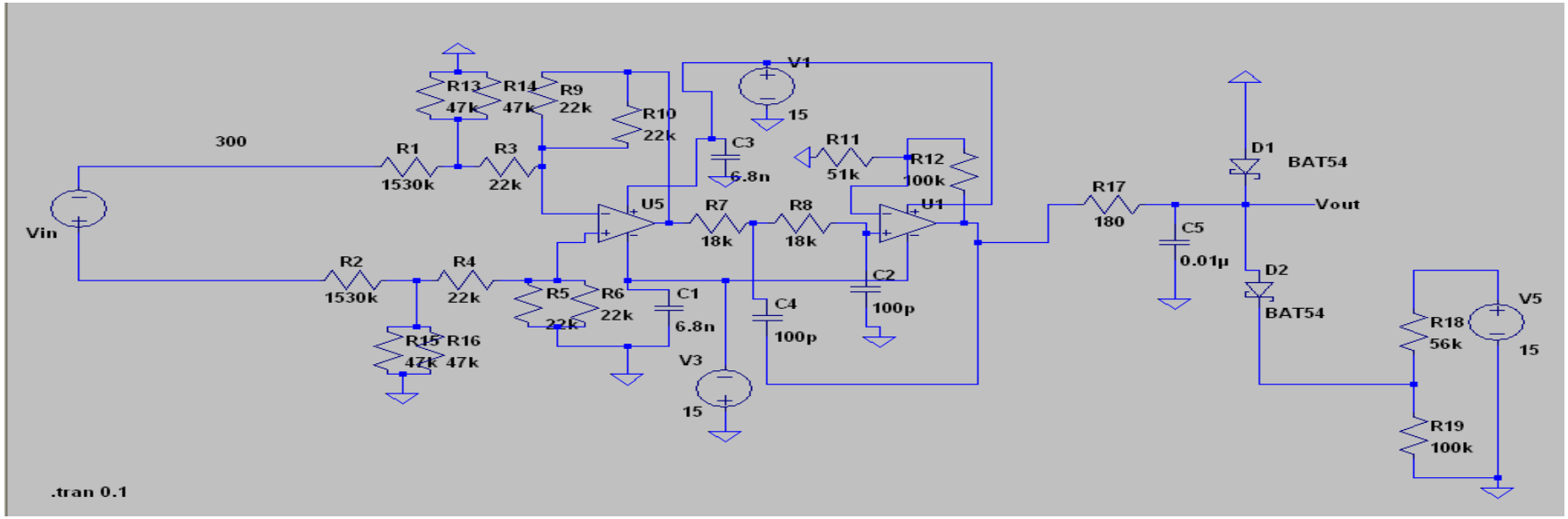


Figure 5. 15: DC source interface circuit

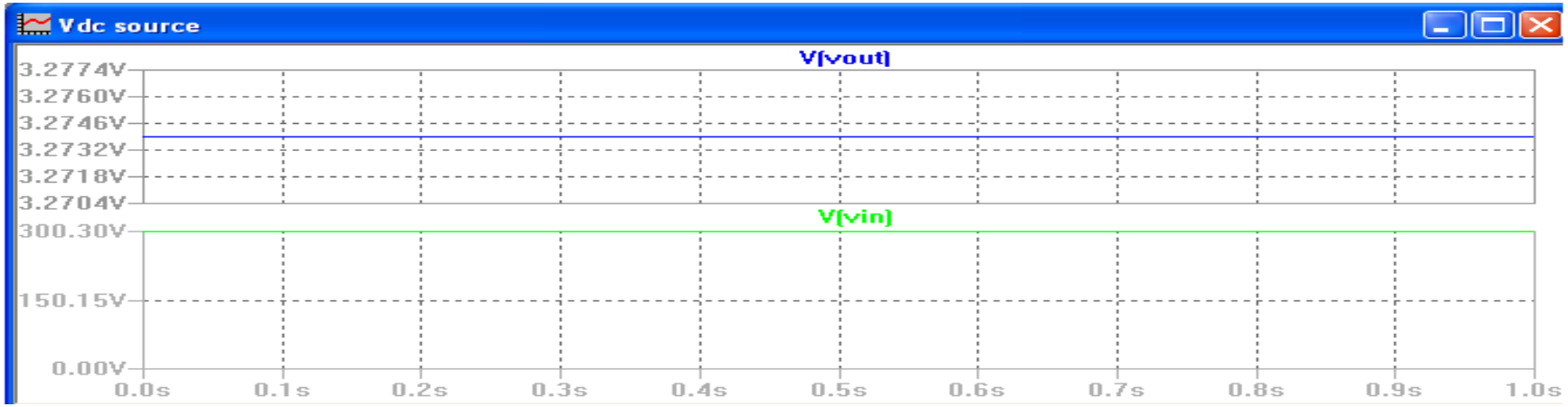


Figure 5. 16: Simulation result of the dc source interface circuit

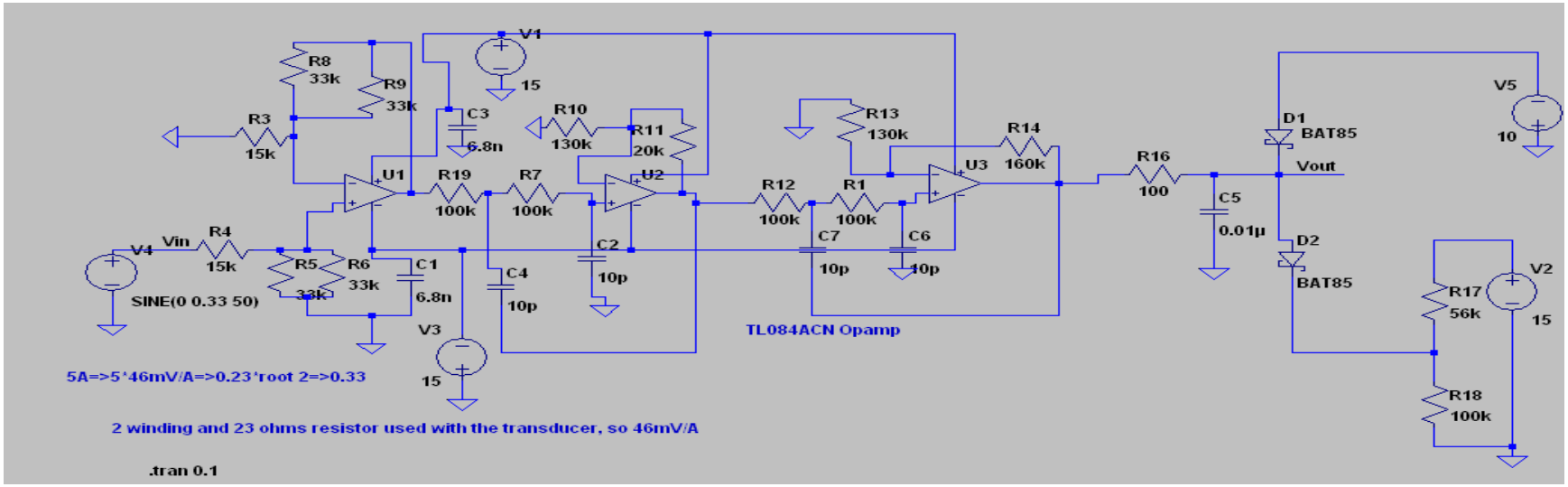


Figure 5. 17: AC current interface circuit

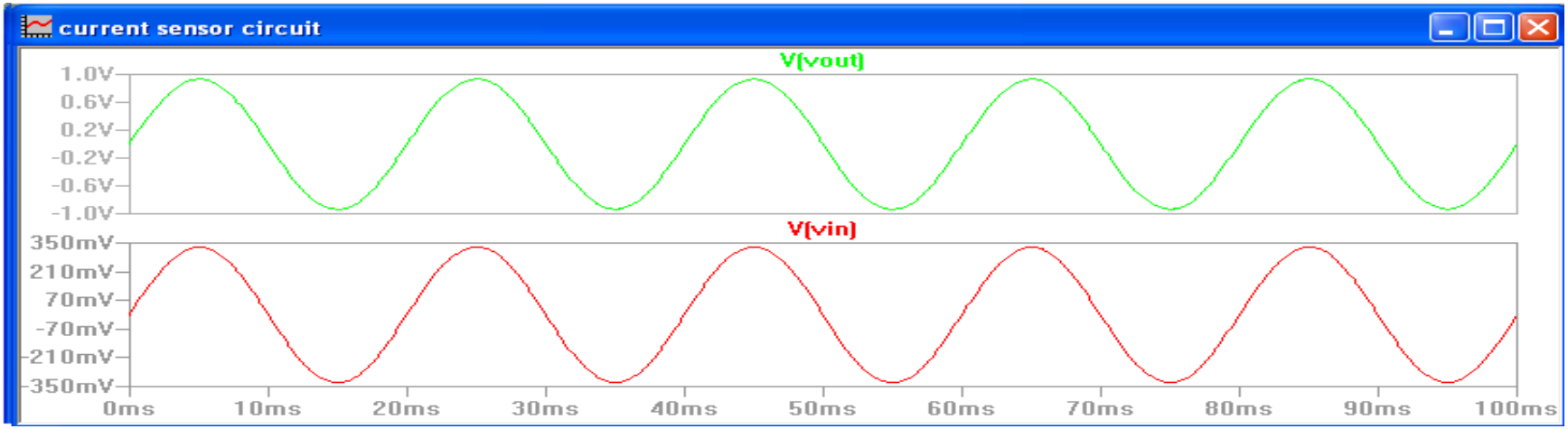


Figure 5. 18: Simulation result of the ac current interface circuit

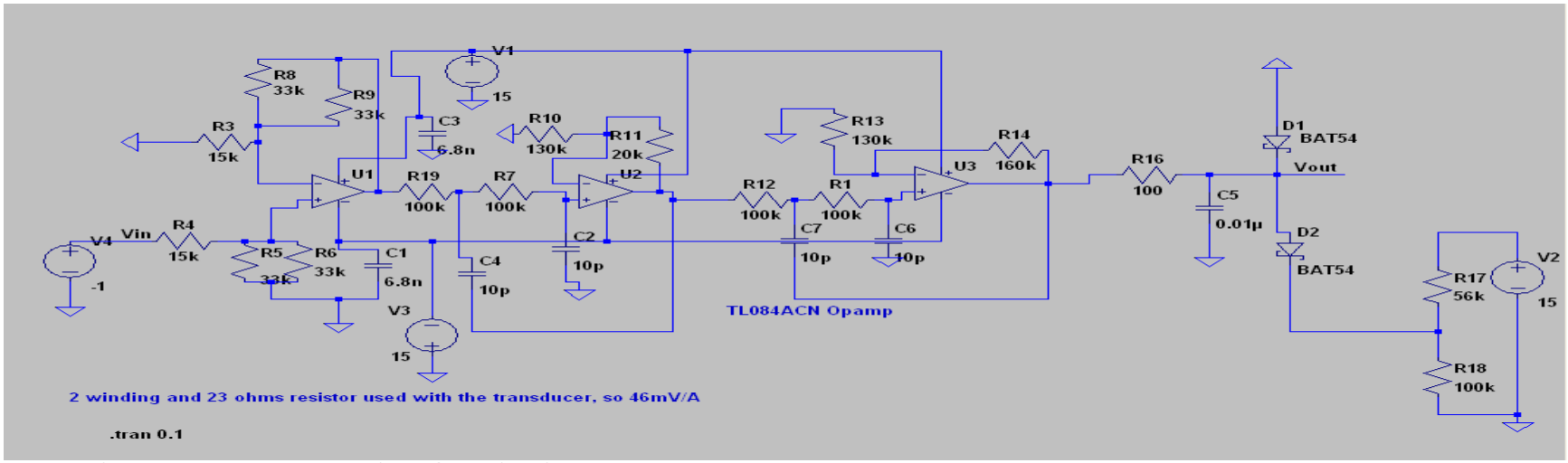


Figure 5. 19: DC current interface circuit

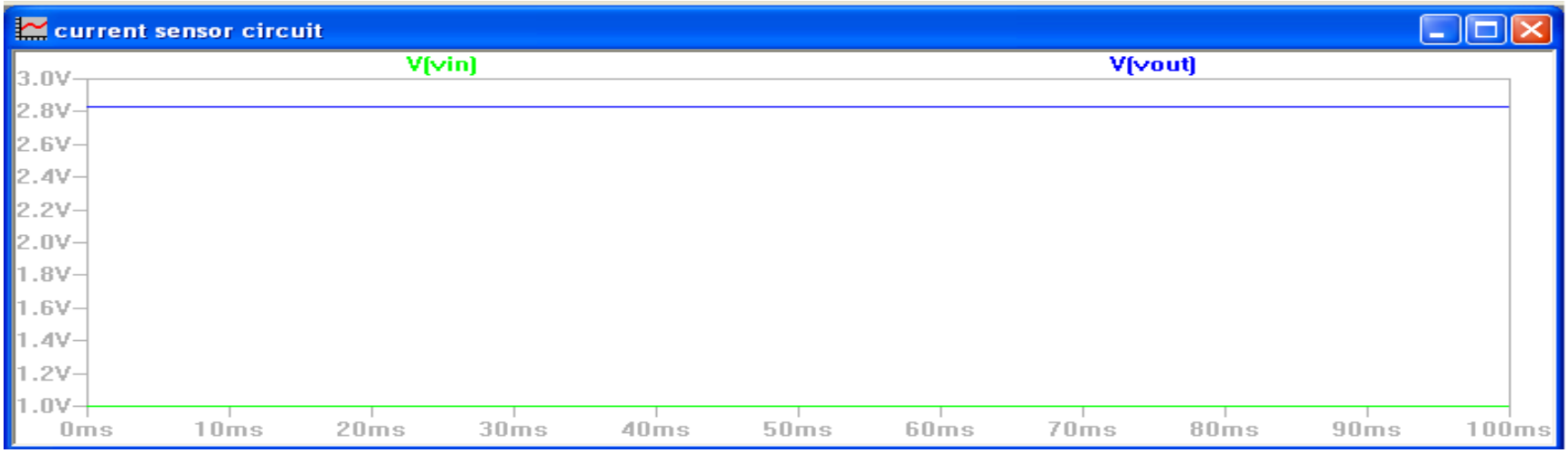


Figure 5. 20: Simulation result of the dc current interface circuit

5.1.16 Design and fabrication of the PWM level shifter

The three phase inverter is controlled using six PWM signals, three PWM signals for the top switches and their complements for the bottom switches with dead band (for protection against shoot-through fault). The boost IGBT switching signal requires a single PWM signal depending on the boost duty cycle calculated by the dc link controller.

The dSpace PWM blocks can create high frequency PWM with 1-5µs dead band as required. These PWM signals from the DSP are of TTL Logic, 0-5V. These have to be converted to 0-15V to be accepted by the gate driver of the inverter and the boost switch. This calls for a PWM level shifter circuit whose simulation design is done using LT Spice. The 0-5 V PWM pulse is compared using a fast comparator (LM339N) to a precise reference (using 1% resistors) of 0.5V to get matching 0-15V PWM pulses. Figures 5.21 and 5.22 show the circuit simulated and the result expected of the hardware circuit (see Figure 5.30 for the hardware circuit test result). The hardware circuit is shown in Appendix 6.

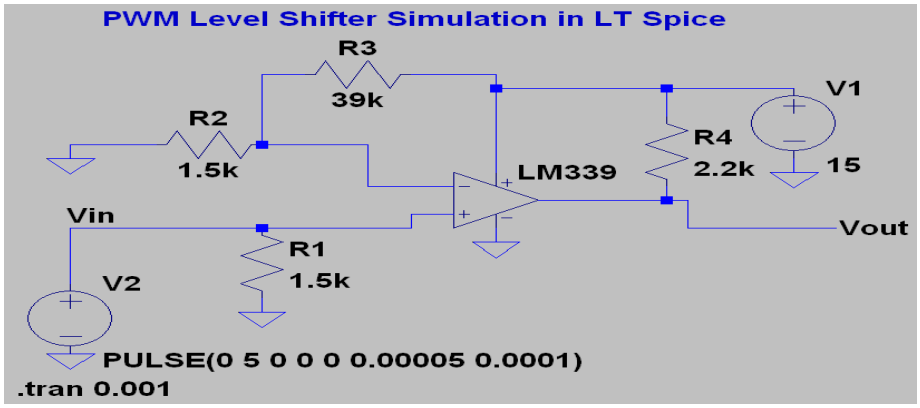


Figure 5. 21: PWM level shifter circuit

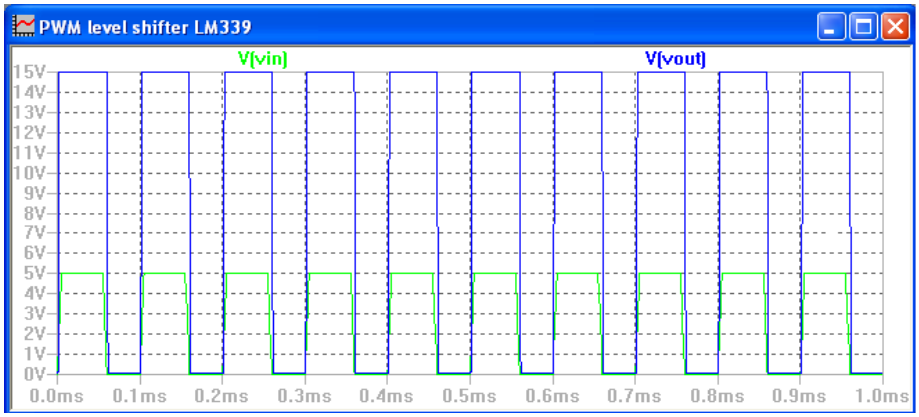


Figure 5. 22: Simulation result of the PWM level shifter circuit

These 0-15V PWM signals taken by the inverter and the boost switch are conditioned (using high frequency isolating transformers) within their respective gate driver circuits that are selected for operation. Firstly they are modulated with a very high frequency carrier and then isolated using an isolation transformer. This protects the DSP controller board from any damage.

5.2 Software control (Simulink control program and dSpace DS1104 controller)

Modern power electronic systems require, sophisticated high speed control, fast triggering protection schemes and data communication systems. The control complexity of the three-phase dc-ac grid connected inverter requires a microprocessor or a digital signal processor to test its various algorithms run together. A DSP based digital controller is developed to control the hardware prototype.

A DS1104 controller board (DSP board) along with the CP1104 panel (that interacts with the signals) has been used to run the Simulink algorithm, to control the constructed hardware prototype.

The objective of the power electronic converters for utility interconnection is to supply high quality power output to the utility grid. In compliance with the IEEE Std. 929-2000 [3], the IEEE Std. 1547-2003 [4] and EN50438 European standard [5], the real power output is maintained constant to minimize current and/or voltage harmonic distortion at the point of interconnection and the reactive power output is regulated to zero to achieve power factor near unity.

Synchronisation to the grid is a vital function of the grid tie inverter during start up, to avoid faults with mismatched voltage (as discussed in Chapter 2). This synchronisation information from the grid is also used to run the inverter at unity power factor (i.e. current produced by the inverter is in phase with the grid voltage).

The next section describes the control program and the respective flow chart is given below in Figure 5.23. There are further discussions on how the Simulink program is developed, downloaded on to the DSP processor and the GUI designed to interact with the user in real-time.

5.2.1 Control program

The control program is written in Simulink with Sim Power System, dSPace and other relevant block sets. Maximum step size achieved without making the processor go into over run situation is 0.0002 s for the whole program. All ADC's are sampled at 5000 Hz in the control program running all blocks at the same speed, except the block that calculates M and δ which is sampled at 50Hz. This is because the inverter output takes time to reflect the new reference and a high sampling frequency is not required. Even though a 5000 Hz program sample rate is sufficient for the developed control algorithm with all the protections and anti islanding scheme running, it is noted as a drawback of the dSpace system DS1104 that it cannot achieve a very high sampling rate with larger Simulink programs. Full Simulink control program with its subsets is shown in Appendix 5.

The three-phase grid voltages (75V rms L-N) are sensed at 5000 Hz (100 samples per frequency cycle giving an uncertainty of 3.6°) and they are expected to be sinusoidal with a peak value of 106V on the secondary side of the three-phase step down transformer. 400V L-L, 230V L-N three-phase utility grid is connected on the primary side. These sensed voltage signals go through a series of steps and calculations in order to make appropriate control decision for transfer of real power to the grid from the inverter. The main steps involved in the control program (Figure 5.23 in Section 5.2.4) are discussed below.

The RMS and peak value $(RMS \times \sqrt{2})$ of these acquired grid voltages are calculated continuously. The sensed grid signals are divided by the fixed peak value (106V) to get a sinusoidal normalised to 1V Pk-Pk, which is the normalised grid voltage signal. Any

voltage distortion, sag or swell is directly reflected on the normalised grid signal with this process. Positive sequence component is retrieved for the above three-phase voltage signals which go through a PLL.

The three-phase discrete PLL is then used to retrieve the frequency and phase information (ωt) of these normalised grid voltage signals. The RMS of the three grid voltages, along with the I_{ref} (inverter ac current reference), V_{dc} (dc link voltage) and Z (value of coupling impedance of LCL filter), are used to calculate the V_{inv} Pk (required inverter peak voltage) and δ (lead angle) continuously, using the power flow theory discussed earlier in Section 2.4 of Chapter 2. The V_{dc} is sensed simultaneously. The M (modulation index) is calculated using V_{dc} to produce the required V_{inv}.

V_{inv}, δ and M along with the ωt information is used to generate three sinusoidal reference signals for generation of three PWM pulses at 20 kHz that switch the three top switches of the inverter block. Inverted sinusoidal references are used to generate three inverted 20 kHz switching pulses that switch the three bottom switches. A 3μs dead band (blanking time) is added to the bottom switching signals to avoid shoot through.

5.2.2 DC link voltage control

The dc link controller is based on a programmed embedded Matlab script which keeps the dc link voltage within the band 285-305V by controlling the duty cycle of the boost switch accordingly. If dc link voltage below 285V is sensed, the duty cycle is increased in steps of 0.0001 and if voltage above 305V is sensed then duty cycle is decreased in steps of 0.0001. This step size is carefully chosen in order to keep up with the 5000 Hz sampling frequency of the control program. Minimum dc link voltage required to operate

safely without boosting is 265V and the minimum dc source voltage expected is 150V when the boost stage is operating. Figure 5.37 shows the response of the dc link voltage control algorithm that adjusts the boost converter's duty cycle accordingly depending on the applied dc source voltage (a big step of 210V to 286V in the dc source voltage is made). The step response of the dc link controller shows that the dc link voltage is quickly (within 1 second) adjusted to the reference band. The controller always stops perturbing in the same direction after reaching a predefined maximum duty cycle (30-50% user defined maximum value) and does not boost beyond this for safety reasons. See A.5.8 in Appendix 5 for the algorithm.

5.2.3 Inverter protection

To protect the inverter from operating beyond nominal frequency and voltages, embedded Matlab scripts are used to stop the inverter when one of the following occurs:

1. Passive islanding protection: Any of the phase voltages are out of +/-10% voltage range
2. Passive islanding protection: Frequency is out of the range of 48 to 50.5 Hz
3. DC link voltage exceeds 450V
4. User Enable is '0' instead of '1'
5. Proposed anti-islanding protection algorithm output is '0' instead of '1' (This new technique is described in the Chapter 6 of this thesis)
6. DC side current exceeds 16A

Frequency protection algorithm is shown below, rest of the protection algorithms developed (which are similar in nature) are shown in A.5.8 of Appendix 5.

```
function [y,T] = Freq_protection(u,T1)
% This block supports the Embedded MATLAB subset.
% See the help menu for details.
y=1; T=50;

if (u>50.5 || u<48)% once threshold reached, upper limit (+1%), lower limit (-4%),switch is put to zero, 48 to 50.5 for 50Hz
   y=0;
   T=u;
end

if (T1>50.5 || T1<48)
   y=0;
   T=T1;
end
T1=T; %T1=T=0 until U>th, then T1=T=U and it keeps the switch to zero(i.e inverter is disabled continuously)
```

5.2.4 Control flow chart

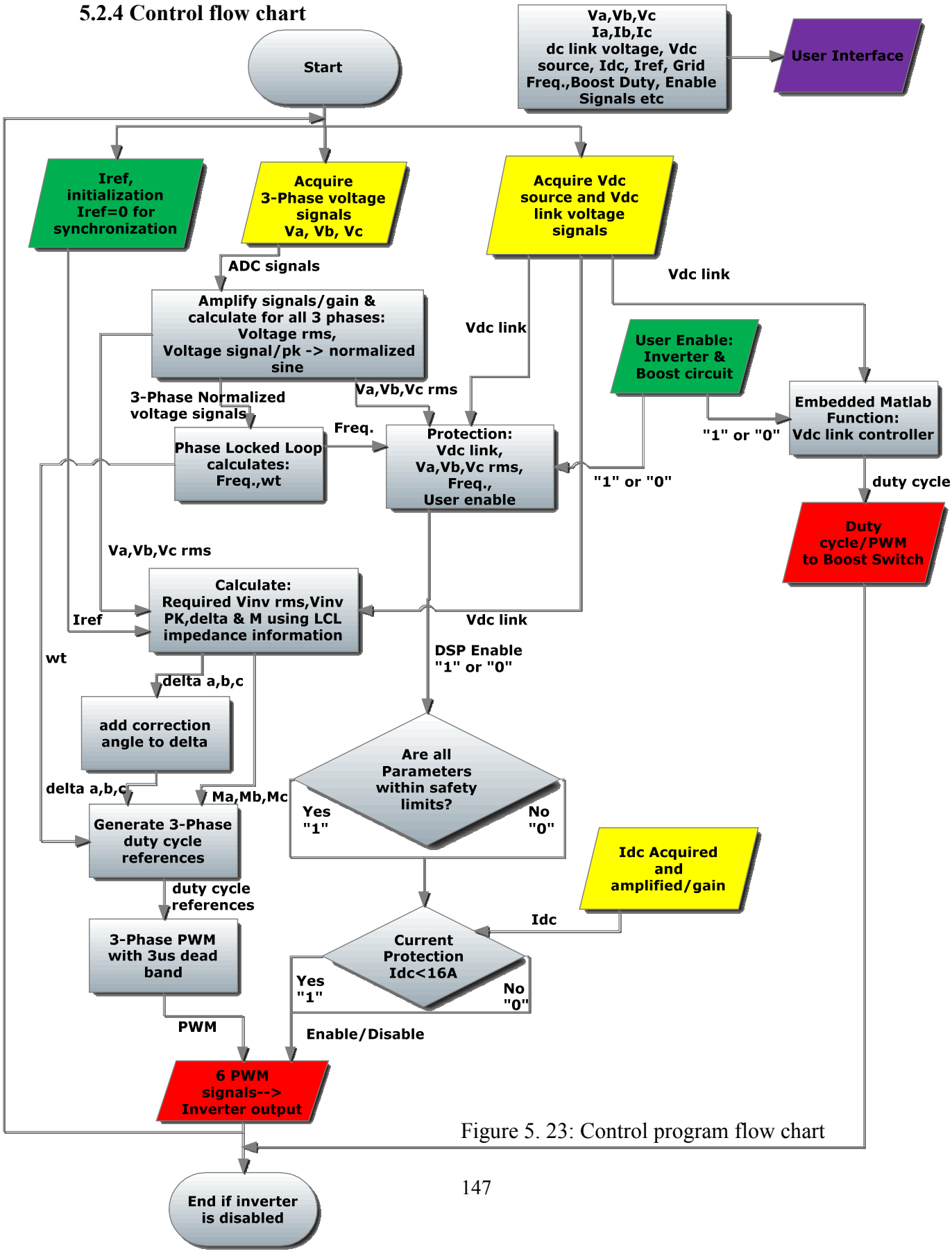


Figure 5. 23: Control program flow chart

5.2.5 Software development

The software that runs on the DS1104 controller board are the simulink files that are created for simulation purposes, but unlike in simulation; many blocks have been replaced and modified with blocks from the 'dSPace tool box' to communicate with the real signals from the hardware.

Two simple examples of the many changes made to the Simulink simulations are:

1. The simulated program contained a "three-phase grid block'' from Sim Power Systems blocksets in Simulink. This now is replaced by connecting the real utility grid. PCC voltages acquired using the ADC port passes through a gain of 10 before appropriate gain (real signal which was conditioned and attenuated by the interface circuit needs to be amplified within the control program) is utilised.
2. Carrier based sinusoidal PWM was generated by comparing high frequency carrier against a sinusoidal reference to generate PWM for each switch, during simulations. This is now replaced by generating duty cycle references 0-1 V, i.e a continuous product of shifted sinusoidal reference (0-1 V) with the modulation index, M, is fed into the "dSpace PWM block" that controls the inverter. The sampling frequency for simulation purposes was 125 kHz while for the final control program is only 5 kHz.

Various changes, calculation and gains required by specific blocks, have been made precisely in order to make the final program compatible with the dSPace controller. The solver settings have been made such that Real Time Workshop can be used to transform

the Simulink program into dSpace code, that can be successfully downloaded on to the processor.

A screen shot of part of the main control program is shown in Figure 5.24. See Appendix 5 for the detailed Simulink program. Figure 5.24 below shows the PWM block from the dSPace tool box, which replaces the PWM generation subsystem in simulation.

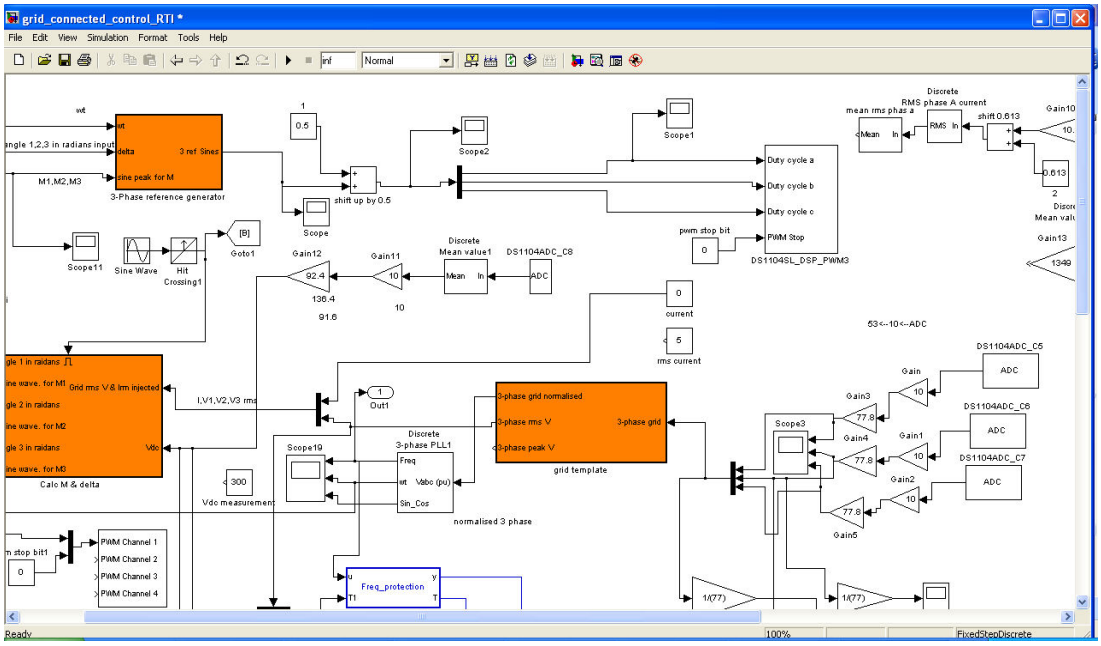


Figure 5. 24: Shows part of the control program that outputs PWM pulses

A graphical user interface (GUI) has been developed using Control Desk from dSPace which interacts with the user in real-time. The layout and control tools on the GUI is linked to the Simulink program so that the changes made on the GUI reflect the experiment in real-time. A screen shot of the GUI in edit/design and test mode is shown in Figures 5.25 and 5.26 respectively. Explanation of the displayed blocks of the developed GUI is discussed in the experimental results Section 5.5.

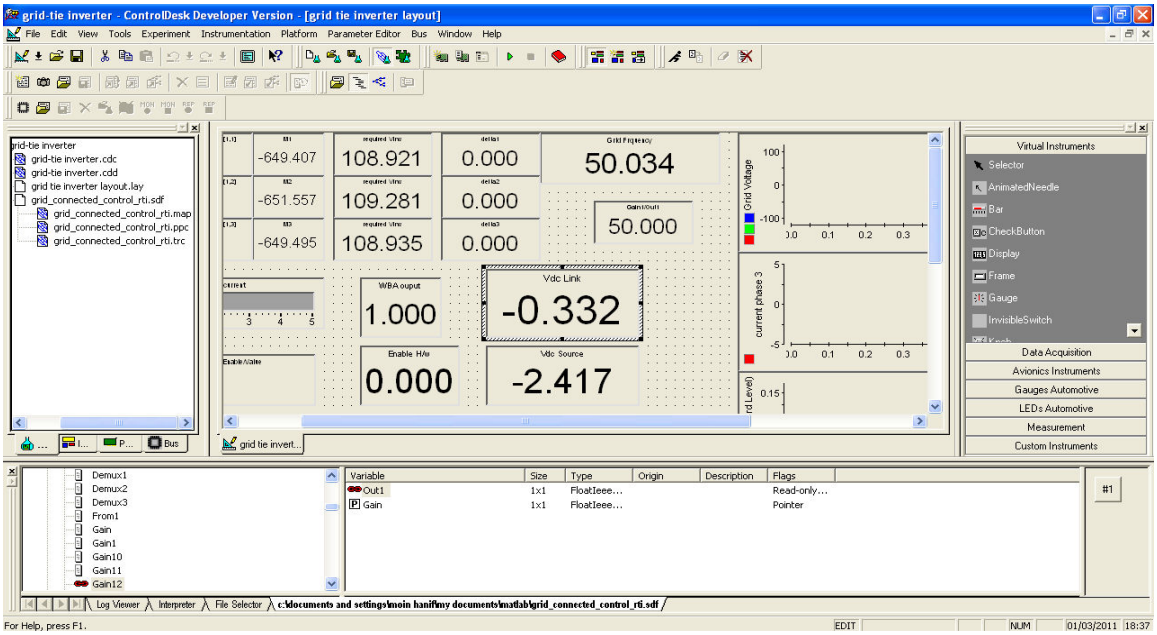


Figure 5. 25: GUI in Control Desk (design mode)

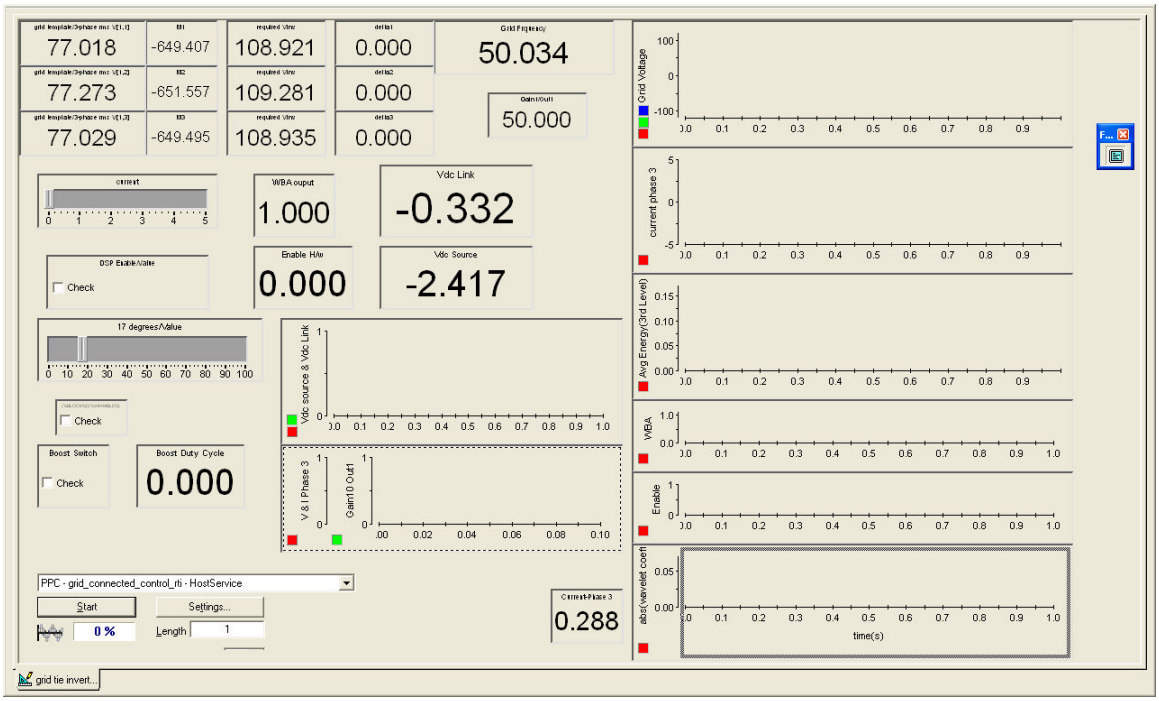


Figure 5. 26: GUI in Control Desk (Test Mode)

5.3 Construction and testing

The prototype construction and testing has been performed stage by stage in the following sequence, in order to prepare the system to be able to run the experiments:

- Building of the interface circuits and testing
- Building of the main components of the inverter system, cabinet and testing
- Software development, testing and interaction with hardware
- Procurement of the cabinet, components, materials and tools
- Wiring and marking

A schematic diagram of the full experimental setup with all the measurement sensors, circuits and DSP is shown in Figure 5.27. Pictures of the prototype at different assembling stages are presented in Appendix 6. This work on the prototype construction, involved practical experience and required manufacturing and engineering skills such as mounting, assembling, wiring, programming and testing.

Testing of the prototype was done in a systematic manner. Each section and component was tested individually before putting them together. Debugging of certain problems was time consuming but was adopted in a modular fashion to achieve goals.

Various tests were carried out to verify safe operation of each part of the laboratory prototype before any experiment could take place as listed below:

- Voltage and current measurement interface circuits are tested to match with simulation results. Gains presented by hardware matched the simulation.
- LEM transducers are tested to confirm their operation and ratio of output.

- Inductors have been tested at four different frequencies, 100Hz, 120Hz, 1k Hz, 10k Hz using Stanford Research Systems Model SR715, LCR Meter.
- ADC input range and internal attenuation (+/-10V=>+/-1V) and DAC output range has been tested.
- Voltage and current measurement are calibrated and internal gains within the control software are adjusted according to two different multimeters and oscilloscopes
- Basic PWM output is tested by using software generated grid voltages and then sensing real grid voltages both before and after the PWM level shifter.
- The reliability of generated dead bands is confirmed if they give the appropriate and exact width for the selected dead band before and after the PWM level shifter.
- Current protection circuit is tested by applying equal and greater voltages to the over current reference voltage.
- Boost circuit is tested by applying dummy duty cycle values before it is connected as part of the grid connected inverter system.
- DC link controller is tested to see the change in duty cycle and the maximum duty cycle reached (protection of dc link) with lower dc source voltages (295<V>305).
- Protection algorithms written are tested with software generated over/under frequency and voltages into the main control algorithm.
- Inverter output voltages are tested if they generate the calculated voltages.

- Harmonic content/ Fourier transform of both grid and inverter voltages is analysed using the PQ monitor
- Synchronization error between grid and inverter voltage before connection is analysed if it is within the +/-5V range.

Summary of safety measures for the experimental setup

Safety of components, hardware prototype as a whole, laboratory and human health was given close consideration. Some important measures taken to protect them all are briefed as follows:

- Resistor network at the attenuation stage with built in redundancy within the interface circuits
- 12.7 Ω high power resistor in series between the dc link capacitor and inverter input
- Three-phase step down and isolation transformer
- Choice of L and C values with ample margin than the calculated values
- Choice of operating dc link voltage
- Ultra fast 5A fuse between the variable ac source and the rectifier
- User defined maximum boost duty cycle (30-50%) for the dc link controller
- Fast 16A hardware based current protection circuit
- Software protection that disables the inverter based on 6 different signals (see Section 5.2.3)
- Wooden cabinet

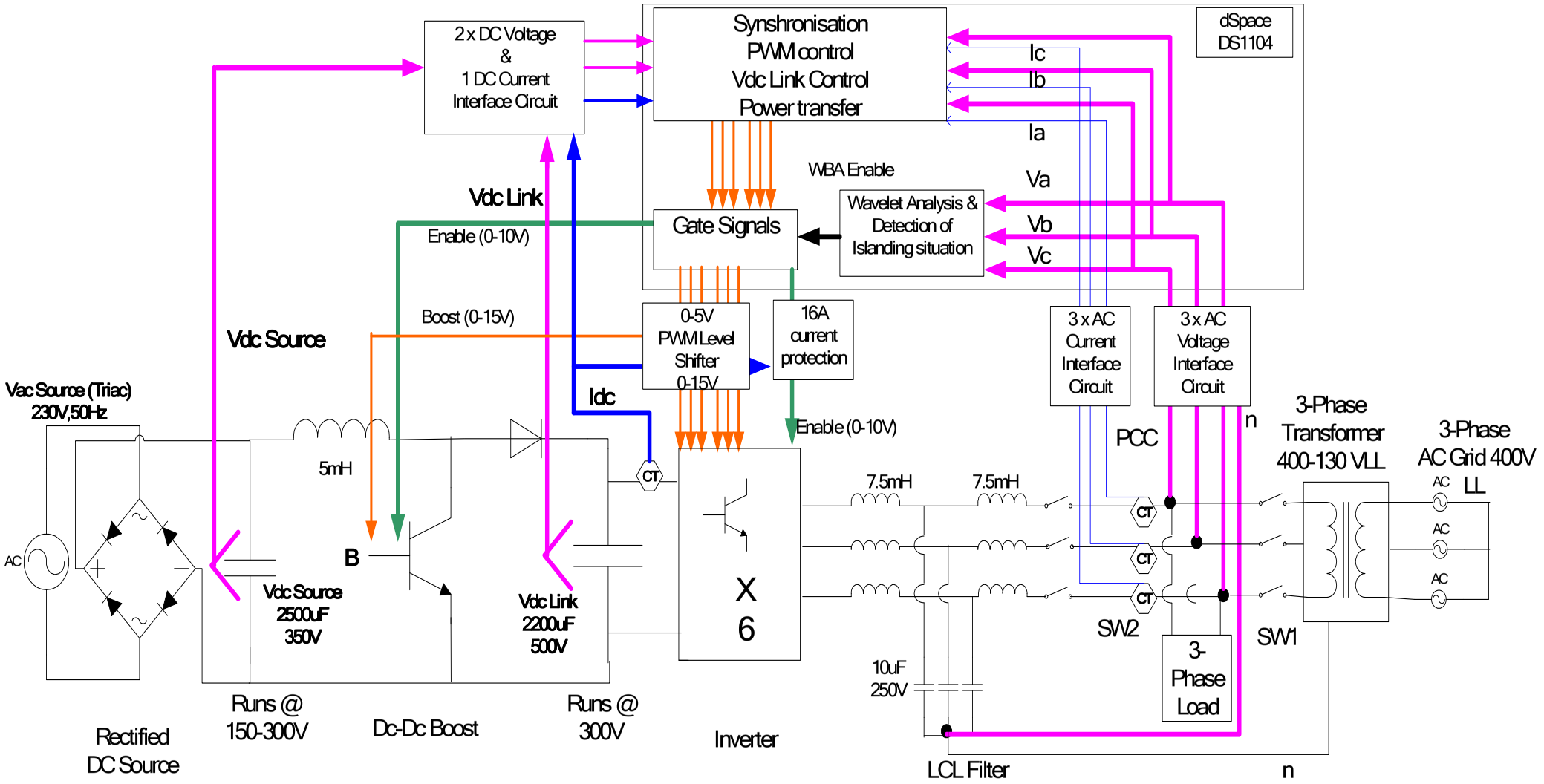


Figure 5. 27 : Experimental setup

5.4 Experimental results of the interface circuits

The hardware system and the interface circuits have been built and tested in the laboratory. Measurements have been performed using LEM LTA 50P/SP1 & LTA 100P/SP1 current transducers, Tektronix oscilloscope type TPS 2024, Tektronix oscilloscope type THS720P, Farnell 2 x 15V dc source E30-2BT, variable rectified dc source that was built in the laboratory for the setup, single phase 230V 50Hz grid supply and three-phase step down transformer 400:130V L-L has been used in the experiment.

Figure 5.28 shows the hardware result obtained from the ac voltage interface circuit and Table 5.2 gives the attenuation factors from the test performed on the ac voltage interface circuit. Figure 5.29 shows the hardware result obtained from the dc source voltage interface circuit and Table 5.3 gives the attenuation factors from the test performed on the dc source voltage interface circuit. Table 5.4 and Table 5.5 show the attenuation and gain factors of the tests performed on the dc link voltage interface circuit and current interface circuit respectively. Figure 5.30 shows the hardware result obtained from the PWM level shifter circuit. Experimental test results below show interface circuits built on the veroboard are complying with the simulation results and the gains of the circuits have been consistent throughout the tests.

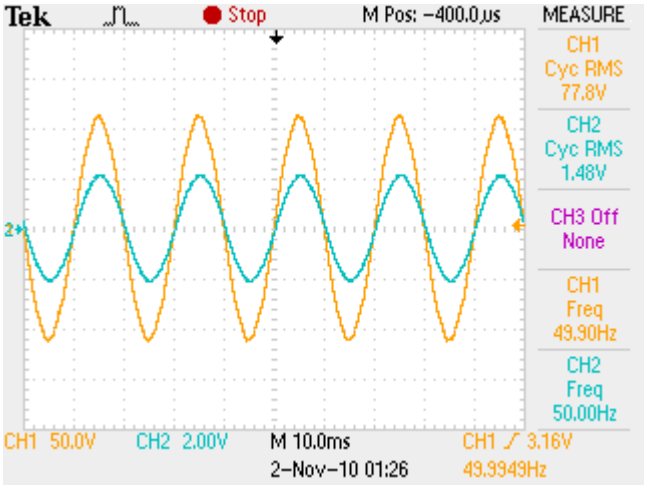


Figure 5. 28: Test result of ac voltage interface circuit, CH1: Input, CH2: Output

Table 5. 2: Attenuation of voltage interface circuit

Input to Circuit (V rms)	**Output from Circuit (V rms)**	**Attenuation factor**
221.7	4.17	53.2
225.5	4.23	53.3

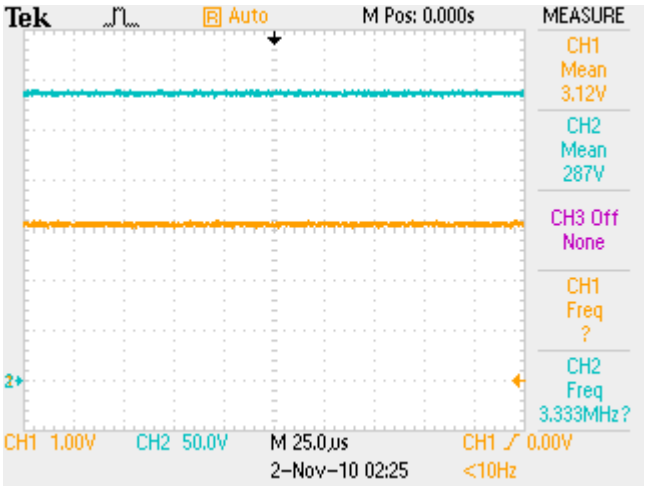


Figure 5. 29: Test result of dc source voltage interface circuit, CH2: Input voltage, CH1: Output voltage

Table 5. 3: Attenuation of dc source interface circuit

Input to Circuit (V rms)	**Output from Circuit (V rms)**	**Attenuation factor**
287	3.12	92
300	3.27	91.7

Table 5. 4: Attenuation of dc link interface circuit

Input to Circuit (V rms)	**Output from Circuit (mV rms)**	**Attenuation factor**
50.6	365	138.6
50.8	366	139
100	730	137
100.2	732	136.8
127.4	934	136.4

Table 5. 5: Gain of current interface circuit

Input to Circuit (V rms)	**Output from Circuit (V rms)**	**Gain factor**
3	8.59	2.86
1	2.85	2.85

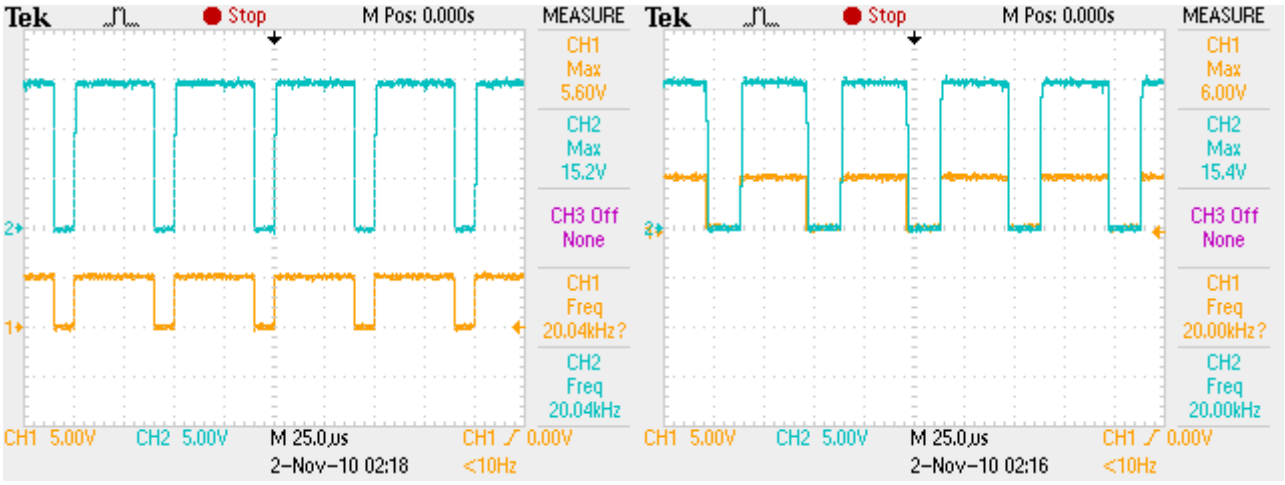


Figure 5. 30 : Test result of PWM Level shifter circuit, CH1: Input 0-5V PWM, CH2: Output 0-15V PWM

5.5 Experimental results of the system

The grid voltages Va, Vb, Vc, Vdc source, Vdc link voltage, grid frequency and the current flowing through phase A are acquired and displayed (see Figure 5.34). Figure 5.31 shows a close view of the sensed grid voltages during a period of 0.02s. Figure 5.31 shows: (a) the voltage signal sensed by ADC, (b) gain of 10 applied on the ADC signal (dSpace has an internal attenuation of 10), (c) normalized grid voltage signal that is fed into the PLL and (d) sensed ADC signal scaled to achieve full grid voltage signal that is used for calculations. Figure 5.34 and 5.35 show the screen shots of dSpace Control Desk GUI in acquisition mode, while the inverter is up and running.

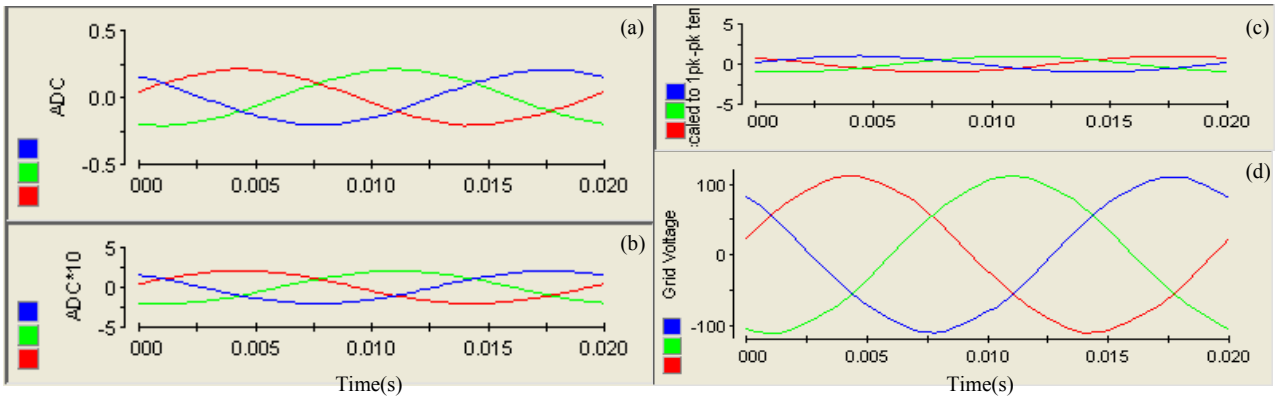


Figure 5. 31: Close view of the sensed ADC voltages

(a) ADC signal, (b) ADC with gain of10 (c) Normalized grid voltage (d) Grid voltage-appropriate gains applied to retrieve real signal

Calculated values for each phase that include RMS voltages at PCC, required inverter peak voltage, modulation index and lead angle to transfer 0 Amps (synchronization mode) are displayed at startup. The user has the option to start the inverter by clicking on 'DSP Enable'. This allows the inverter to generate matching voltages to the PCC. The synchronization error can be checked on the oscilloscope to be in the limits +/-5V RMS before connecting to the grid as shown in Figure 5.32. Once the synchronization error is within the limits, the synchronization manual circuit breaker SW 2 is closed and the inverter is ready to transfer power as shown in Figure 5.33.

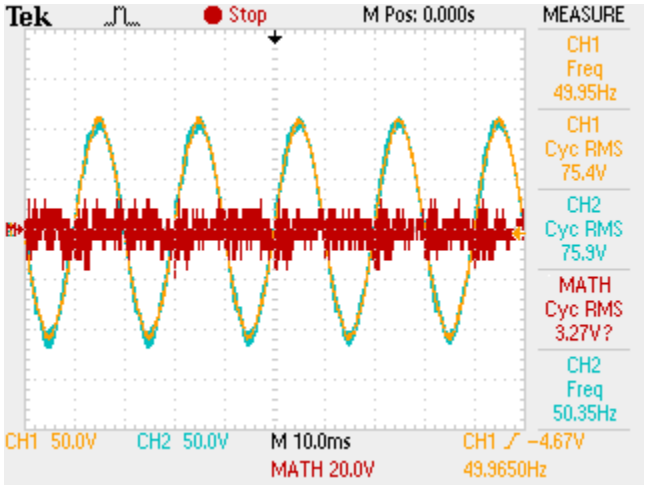


Figure 5. 32 : Synchronization of inverter and grid voltages before closing SW 2

CH1-Grid voltage, CH2- Inverter voltage, CH3- Synchronization error (CH1-CH2)

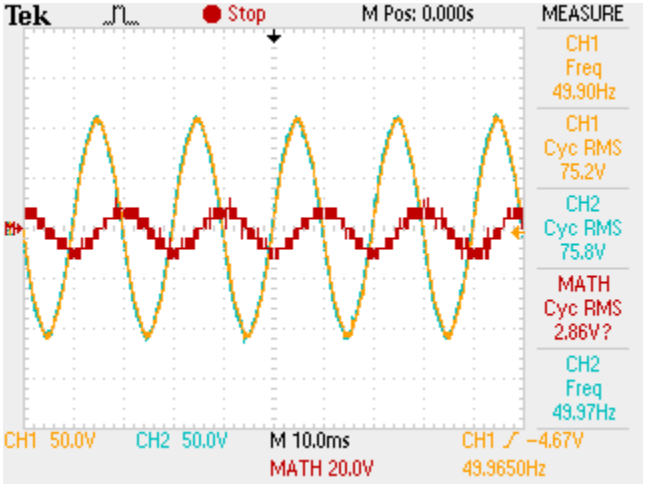


Figure 5. 33 : Inverter synchronized to the grid, after closing breaker SW 2

CH1-Grid voltage, CH2- Inverter voltage, CH3- Synchronization error (CH1-Ch2)

Depending on the level of reference current, corresponding current is transferred into the grid as shown in Figure 5.34. The calculations are made continuously in real time for the new reference current and updated on the GUI. In this case 1.85A current is flowing in each phase of the power circuit from the inverter to the grid.

If the boost circuit is switched ‘On’ within the GUI, then the dc link voltage is boosted to voltages between 285V and 305V. Also, the required duty cycle fed to maintain the dc link voltage is displayed as shown in Figure 5.35. Figure 5.36 shows the close view of the sensed, real dc source voltage and the real boosted dc link voltage when boost circuit is operating.

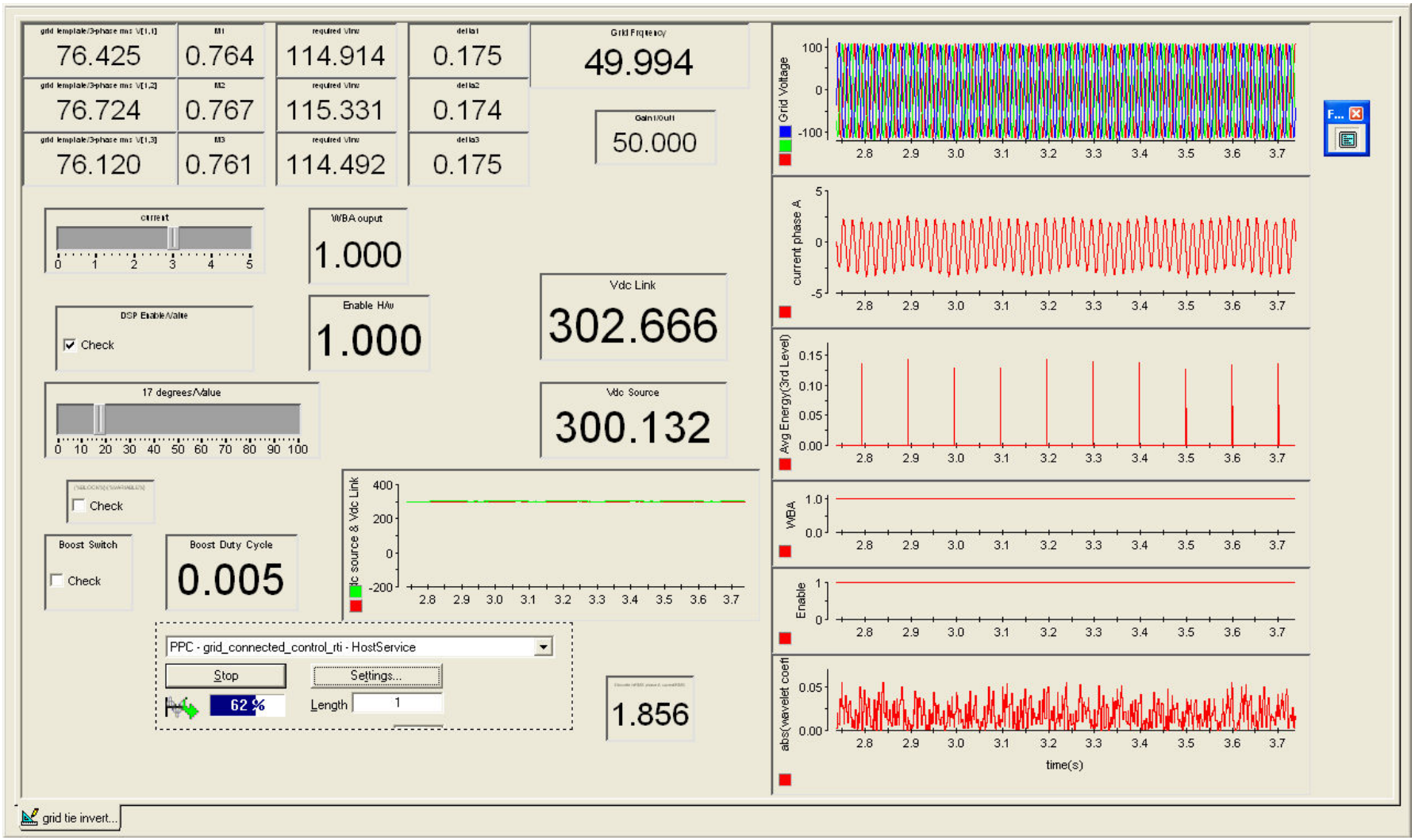


Figure 5. 34: Experimental Result: Power transfer into grid with 300V dc source voltage

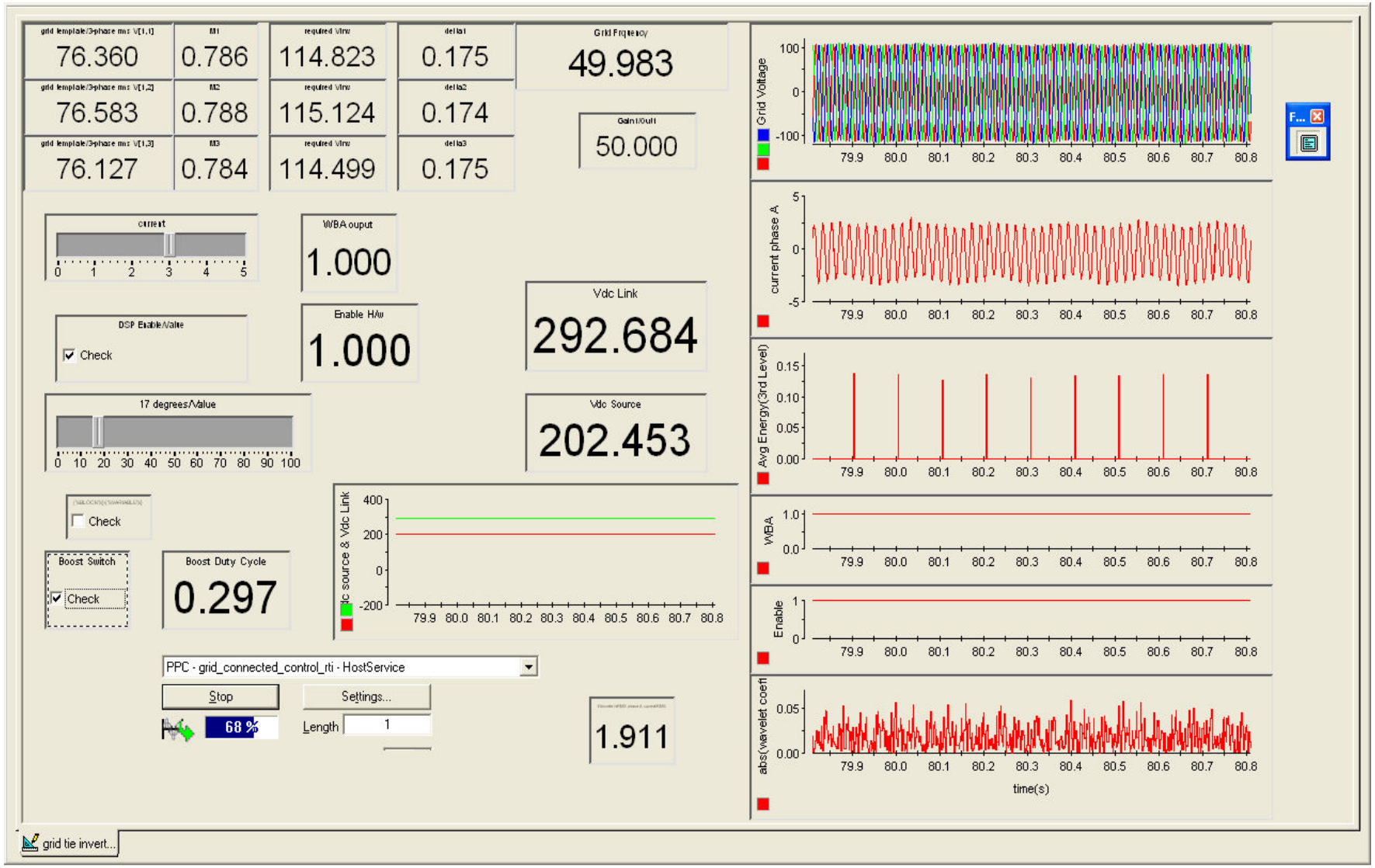


Figure 5. 35: Experimental Result : Power transfer with 200V dc source voltage, boost circuit in action

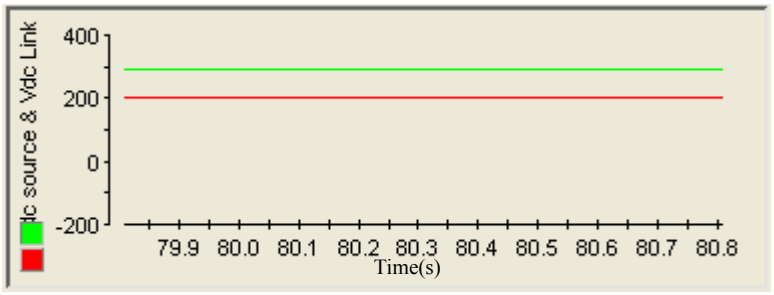


Figure 5. 36: Close view of real dc source voltage and real boosted dc link voltage

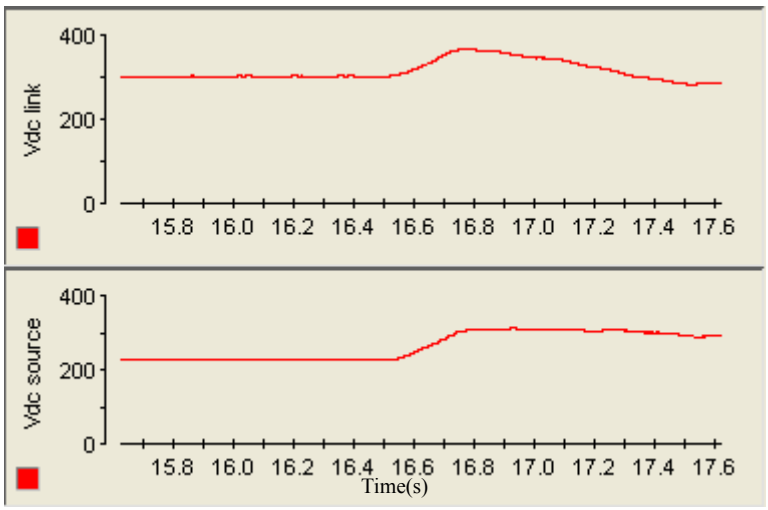


Figure 5. 37: Response of the dc link controller to a step change in dc source voltage from 210V to 286V

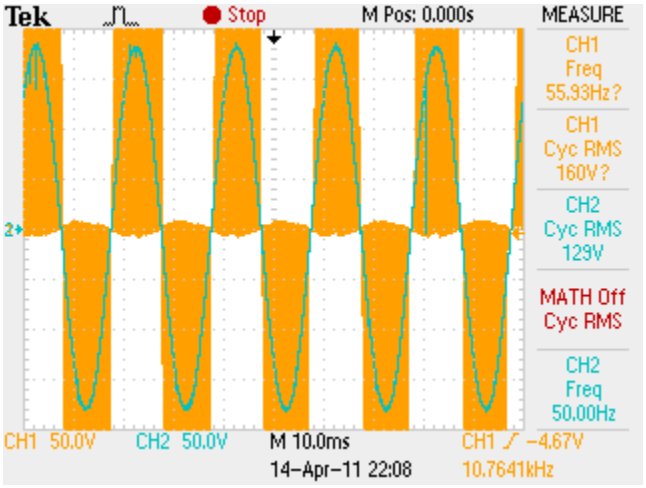


Figure 5. 38: Inverter output (CH1: voltage L-L) and LCL filter output (CH2: voltage L-L)

5.6 Conclusion

The Chapter detailed the selection of components, calculations and designs necessary for the grid connected inverter prototype. The details of the interface circuit design and their circuit configuration used between the hardware and DSP are provided. Simulation results and hardware test results of the respective circuits are produced and compared. The developed software control algorithm is described in detail with a flow chart and the development of the program for the chosen DSP has been explained. Full experimental results of the working system are produced with the designed GUI in dSpace Control Desk. The phase locked loop performed better than expected in tracking the zero crossings and transferring a steady current into the grid (i.e. having a 3.6° sampling uncertainty should allow at least 1A fluctuation at inverter current output). The experimental results show the successful completion of the three phase grid connected inverter hardware construction, software control program and their smooth interaction. Results are as expected and proven to be satisfactory according to the EU EN50438 standard. The experimental setup is ready to perform more tests on the proposed anti islanding scheme which is discussed next in Chapter 6.

Chapter 6

6. NOVEL ANTI-ISLANDING TECHNIQUE PROPOSED USING WAVELET ANALYSIS

6.0 Introduction

Islanding of grid-connected PV inverters occurs when the local network containing such inverters is disconnected from the main utility, but the PV inverters continue energizing the local load without control and/or supervision of utility. This phenomenon can result in a number of potential hazards [58], [59].

- Maintenance staff may be harmed when arriving to service the energized isolated network.
- Utility customer's equipment/devices may be damaged due to uncontrolled voltage and frequency excursion outside nominal range.
- Switching and measuring devices may be damaged due to unsynchronized out of phase re-closure.
- Islanding may interfere with automatic reclosing devices of the utility (devices may malfunction).

Basic passive protection schemes include over-current, over- and under-voltage, and over- and under-frequency (OV/UV and OF/UF) functions to remove a grid connected inverter from the utility grid for the abnormal condition in the grid. Also, anti-islanding schemes must be incorporated into protection control. The above OV/UV/OF/UF schemes are able to detect islanding operation of the grid connected inverter. In case of PV (DG), however, inverter generation being balanced with local load, it is impossible to

detect islanding using basic schemes (non-detection zone, NDZ), and hence at least one active anti-islanding scheme must be included in protection (to eliminate NDZ) [44]. This active islanding scheme injects certain signals (perturbation to variables like voltage and frequency) in order to detect the islanding situation which degrades the output power quality [46], [55], [56].

In response to the above mentioned problem, a detailed literature survey is conducted on the present islanding detection schemes. Then a new anti-islanding technique which uses wavelet modulation is proposed. The Wavelet Modulation technique is used to look at the physical measurements (voltage, frequency, voltage unbalance) in a higher dimension, to see the changes in parameters in a passive environment rather than injecting any perturbation.

6.1 Review of islanding detection

A detailed review revealed several islanding detection methods [44]-[60], which can be classified as passive, active and other methods. Their significant strengths and weakness are discussed below.

6.1.1 Passive methods

6.1.1.1 Under/over voltage and under/over frequency detection

In over/under voltage and over/under frequency detection (OVP/UVP and OFP/UFP), the voltage at the point of common coupling (PCC) and the frequency of the inverter at PCC (node a in Figure 6.1) are continuously monitored [49], [59]. The inverter should be disconnected to prevent damage to both the inverter and utility, when the voltage or the

frequency are out of specified thresholds (207V ≤ V ≤ 253V) and (48 Hz ≤ f ≤50.5 Hz) specified by the EN 50438 [5].

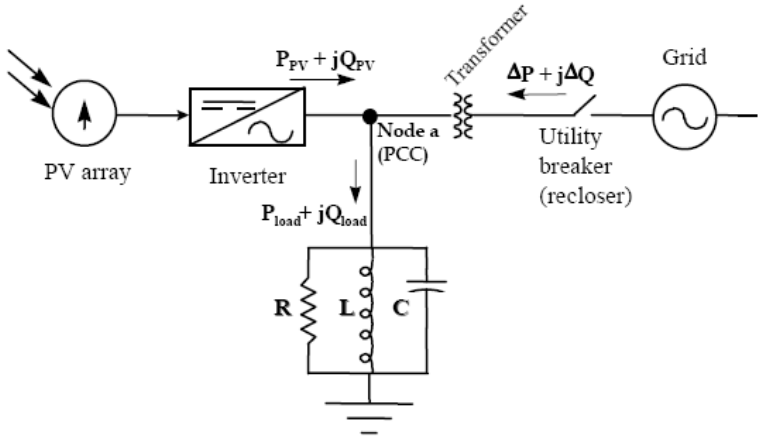


Figure 6. 1: Power flow diagram (real and reactive power mismatch)

Figure 6.1 shows a power flow diagram, where real and reactive power mismatch at the instant utility is disconnected can be analysed. Real and reactive power mismatch is the difference between real and reactive power consumed by the load and real and reactive power supplied by the PV inverter, just before utility is disconnected. This can be expressed as (6.1) and (6.2):

$$\Delta P = P_{Load} - P_{PV} \tag{6.1}$$

$$\Delta Q = Q_{Load} - Q_{PV} \tag{6.2}$$

If the PV inverter was transferring power at unity power factor, then

$Q_{PV} = 0$ And $\Delta Q = Q_{Load}$

It is usually assumed that the load can be modeled as a parallel *RLC* circuit as shown in Figure 6.1. For most islanding detection methods, it is some type of *RLC* load that causes the most difficulty in detection. General nonlinear loads such as harmonic-producing loads or constant-power loads do not exhibit as much difficulty in islanding prevention.

RLC loads with a high *q (Quality factor)* are most problematic for islanding detection. The quality factor can be expressed as (6.3):

$$q = R\sqrt{\frac{C}{L}} \tag{6.3}$$

The parameters R, L and C give the relative amounts of energy storage and energy dissipation.

Real and reactive power of the load can be expressed as (6.4) and (6.5):

$$P_{Load} = \frac{V_{PV}{}^2}{R} \tag{6.4}$$

$$Q_{Load} = V_{PV}{}^2 (\frac{1}{\omega L} - \omega C) \tag{6.5}$$

Real and reactive power supplied by the PV inverter can be expressed as (6.6) and (6.7):

$$P_{PV} = V_{PV} I_{PV} Cos\theta \tag{6.6}$$

$$Q_{PV} = V_{PV} I_{PV} Sin\theta \tag{6.7}$$

Where V_{PV}, I_{PV} are RMS values and $Cos\theta$ is the displacement factor

At the instant when island is formed (utility disconnected), the system behavior depends on ΔP and ΔQ as follows:

(ΔP>0): The inverter terminal voltage will increase above the nominal system voltage.

(ΔP<0): The inverter terminal voltage will decrease below the nominal system voltage.

(ΔQ>0): The frequency will increase until reactive power supplied by the capacitor C balances with that consumed by the inductor L.

(ΔQ<0): The frequency will decrease below nominal system frequency.

Generally the power mismatches are large (ΔP > ±20% or ΔQ > ±5%), causing the voltage or frequency to go out of the nominal range detecting islanding. But if the mismatch is quite small leaving the voltage and frequency within the nominal range, would make the islanding detection impossible causing a large non detection zone (NDZ). Also, if the threshold range is set small, nuisance tripping could occur, hence this detection method on its own is not sufficient for anti islanding protection [49], [50].

6.1.1.2 Voltage phase jump detection

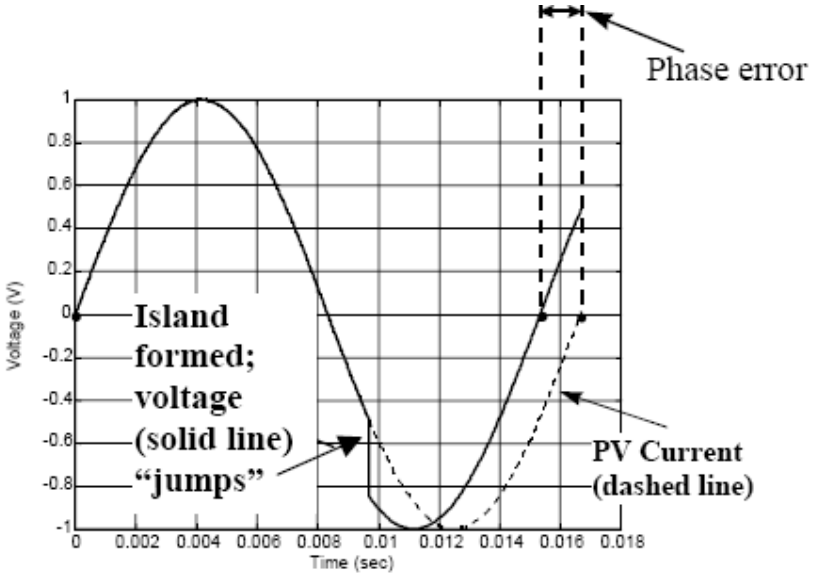


Figure 6. 2: Operation of phase jump detection

This technique monitors the phase difference between the system utility voltage and inverter output current [44], [46]. The output current is usually synchronized with the utility voltage at unity power factor (using a PLL). Soon after the utility is disconnected, if there is a sufficiently large power mismatch, inverter voltage is shifted to match the difference in power and to maintain the phase angle of the load. This causes a voltage phase jump as shown in Figure 6.2. This phase jump can be detected if it goes out of the nominal range, again setting the threshold too small would case nuisance tripping [59].

6.1.1.3 Voltage harmonic detection

Total harmonic distortion of the system voltage at node a in Figure 6.1 is continuously monitored [47]. With the presence of utility, the system voltage is stiff and sinusoidal (THD close to zero), this make the inverter produce a sinusoidal current. The current harmonics produced by a grid connected converter should be less than 5% according to EN 50438 [5]. The current harmonics being small, interact with the small grid impedance producing small distortion in voltage at node a (Figure 6.1). When the utility is disconnected, a large impedance of the load interacts with the small current THD, produces large distortion in voltage making it go out of the threshold range and hence detecting islanding situation. THD threshold should be set appropriately in order to operate without nuisance tripping. This method fails when the islanded load is having a high q factor, which acts as a low pass filter in reducing the harmonic content of the output current. Resistive load usually makes the detection easier since 5% of THD in current causes 5% of THD in voltage and the THD limit should be less set than 5%. This

method also fails if the PV inverter delivers very high quality current, which produces high quality voltage even during the presence of resistive load [46], [47].

6.1.2 Active methods

6.1.2.1 Output power variation and impedance measurement

These two active methods are put together in this survey as they work on the same principle of changing the output power periodically and observing the changes on the voltage at PCC (node a in Figure 6.1).

Output current can be expressed as $i_{PV} = I_{PV} Sin(\omega_{PV} t + \phi_{PV})$ (6.8)

The parameters frequency (ω_{PV}), phase (ϕ_{PV}) and amplitude (I_{PV}) can be perturbed in the expressed current equation. Usually the current amplitude is perturbed and the voltage change respective to current is observed ($\frac{dv_{PV}}{di_{PV}}$), for this reason it is also called the impedance measurement detection [59], [60].

Impedance measurement: If impedance is observed specifically rather than the output voltage, then a threshold for impedance needs to be set to a small value since the grid impedance is not exactly zero. Any impedance observed below the set value indicates grid is still connected unless the impedance of the load is below the set point which is very rare unless the load is a high power load (approaching a short circuit).

Output power variation: Change in current amplitude (I_{PV}) causes a change in output power. Change in current or power causes a change in voltage at PCC, which when islanded shows a significant change and gets out of the nominal threshold range. This behavior can be used to detect the islanded situation.

The minimum current shift required for islanding detection is equal to the full UVP/ OVP (Under Voltage Protection/ Over Voltage Protection) window size. For instance, with grid connected UVP/OVP at +/-10% of rated voltage, a 20% change in current is required.

This method works quite well with a single grid connected inverter reducing the NDZ close to zero, but fails with multiple inverters connected. When multiple inverters are connected, change in current from one inverter is not significant and effectiveness of this method decreases, unless the variation from all the inverters is some how synchronized (which degrades the power quality greatly) [58], [59].

6.1.2.2 Sliding mode frequency shift (SMS)

The three parameters of the voltage at node a in Figure 6.1, to which positive feedback can be applied are amplitude, frequency, and phase. SMS applies positive feedback to the phase of the voltage at PCC (to the reference waveform in practical implementation) as a method to shift the phase. The phase angle between the inverter output current and the PCC voltage is controlled to be zero (or as close to it as possible) usually in a PV inverter (unity power factor operation). But with SMS applied, the current-voltage phase angle of the inverter is made to be a function of the frequency of the PCC voltage, instead of being controlled to zero [59], [60].

The utility provides the operating point at the line frequency by providing a stable phase and frequency reference. If an island is formed, the intersection of the load line and inverter phase response curve gives the new operating point. The load line of the unity power factor load (resistive load) is shown in Figure 6.3. The intersection at the point

labeled B, is at a frequency of 50 Hz (zero phase). This is the operating point while the utility is connected. If the utility was disconnected and any small perturbation away from 50Hz of the frequency of voltage at PCC, would cause the phase error to increase (not decrease), due to the S- shaped phase response curve of the inverter. This is due to the positive feedback mechanism, which causes a classical instability. This instability drives the system to a new operating point, either at point A or C depending on the direction of the perturbation. If the inverter phase curve has been properly designed for the RLC load in Figure 6.3, points A and C would be at frequencies outside the OFP/UFP trip window, and the inverter would shut down due to frequency error.

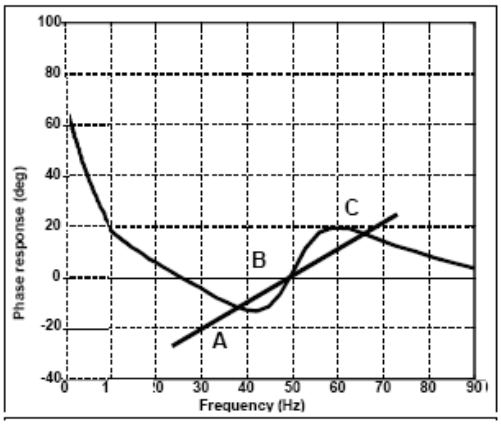


Figure 6. 3: Plot of the current-voltage phase angle vs. frequency characteristic of an inverter utilizing the SMS islanding prevention method

This method is shown to be highly effective to detect islanding situations and is capable of reducing the non-detection zone (NDZ) near to zero. It provides good compromise between effectiveness and output power quality. This method also works well in the multiple inverter case; however, it does fail to detect an island if the starting phase angle matches with the load phase angle at frequency located within the threshold. It also fails,

if the rate of change of the starting phase angle with respect to the frequency is less than that of the load line [60].

6.1.2.3 Active frequency drift (AFD)

Active frequency drift method is to force the frequency of PV inverter output, up or down using positive feedback to accelerate the frequency of the inverter current [52]-[54]. An island is confirmed, if the frequency is out of the OFP/UFP trip window (48 Hz $\leq f \leq$ 50.5 Hz).

In Figure 6.4: T_{Vutil} is the period of the utility voltage, T_{Ipv} is the period of the sinusoidal portion of the 'PV inverter current output', and t_z is a dead or zero time.

The chopping fraction (cf) is expressed as (6.9):

$$cf = \frac{2t_z}{T_{Vutil}} \tag{6.9}$$

The PV inverter current output is a sinusoid with a frequency slightly higher than that of the utility voltage during the first half cycle. The inverter output current remains at zero for time t_z before beginning the second half cycle as shown on Figure 6.4. The PV inverter output current is a negative sinusoid with a frequency slightly higher than that of the utility voltage during the second half cycle and again reaches zero. It remains at zero until the rising zero crossing of the utility voltage. The zero time in the second half cycle is not fixed and need not be t_z.

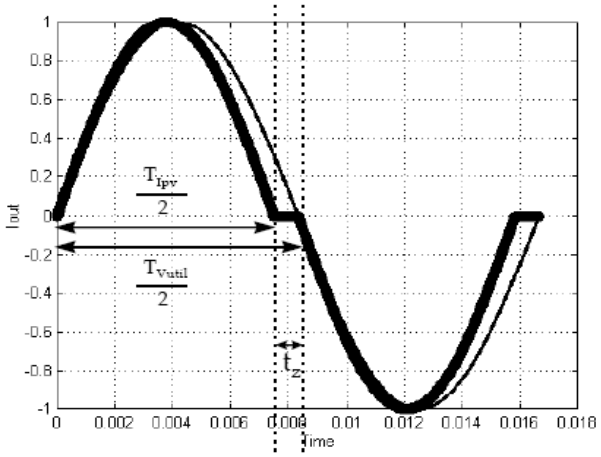


Figure 6. 4: Output current waveform (upward active frequency drift) compared to pure sine wave

During an islanding situation, if this current is applied to a resistive load, the voltage would go to zero for a shorter time (T_{Vutil} - t_z), as voltage follows the distorted current. This causes the rising zero crossing of the voltage at PCC to occur sooner than normal operation, giving rise to a phase error between PCC voltage and inverter current output. The PV inverter then increases the frequency of current in order to eliminate the phase error. This makes the voltage of the resistive load again have its zero crossing advanced in time with respect to where it was earlier, and the PV inverter still detects a phase error and increases its frequency further. This cycle continues until the frequency has deviated far enough to be detected by the OFP/UFP trip window [59].

This method slightly degrades the output power quality and also fails with multiple inverter case unless all the inverters agree to drift their frequencies in the same direction. This method reduces the non-detection zone compared to the passive methods but it is not as good as the other active methods.

6.1.2.4 Sandia frequency shift (SFS)

Sandia Frequency Shift (SFS) is an extension of the AFD method, and it uses positive feedback to prevent islanding.

In this method, it is the frequency of voltage at PCC to which the positive feedback is applied.

Using positive feedback, the 'chopping fraction' is made to be a function of the error in the line frequency. While the utility is connected, the stable phase frequency reference prevents any instability in the frequency. During an island, the chopping fraction increases with slight increase in the frequency of the voltage at PCC, it continues until the OFP/UFP trip window detects the frequency is out of range.

Publications [59] and [60] state that this is one of the best active methods so far, but reduces the power quality slightly during the grid connected mode as positive feedback amplifies the changes on the grid.

6.1.2.5 Mains Monitoring Units with Allocated All-Pole Switching Devices Connected in Series (MSD)

Mains monitoring units are automatic isolating facilities consisting of two independent, diverse parallel mains monitoring devices with allocated switching devices connected in series which are independently controlled. A few islanding methods are used together in order to detect the islanding scenario [53], [60]. Impedance detection, over/under voltage and frequency trips are commonly used in such units. Islanding is confirmed, if grid impedance is higher than 1.25 ohm ($Z > 1.25\Omega$) or if there is a sudden change (within a short period) in grid impedance larger than 0.5 ohm ($\Delta Z \geq 0.5\ \Omega$).

This method has similar pros and cons compared to the output power variation and impedance measurement method, but additional hardware switches involved increase the cost of the system.

6.1.2.6 Other methods

Other methods include: Reactance insertion, Power line carrier communication and Supervisory control and data acquisition methods. These methods are implemented at utility level and since they are beyond the scope of this project they are not discussed.

6.2 Analysis of mismatched power during islanding

-The islanding frequency ω_i is a function of the inverter real power P_{PV}, reactive power Q_{PV} and resonant frequency of the load ($\frac{1}{\sqrt{LC}}$) according to [49].

$$\omega_i = \frac{1}{\sqrt{LC}}\left(1 + \frac{Q_{PV}}{2qP_{PV}}\right) \tag{6.10}$$

The inverter terminal voltage V_i at the instant utility is disconnected, is a function of the ratio of real power of the PV inverter and the load as expressed in (6.11)

$$V_i = \sqrt{\frac{P_{PV}}{P_{LOAD}}V_n} \tag{6.11}$$

where V_n = nominal system voltage

The worst case islanding condition occurs when the real power of the PV inverter is equal to the real power of the load, i.e., $P_{PV} = P_{LOAD}$, and the corresponding reactive power is also equal, i.e., $Q_{PV} = Q_{LOAD}$. For this condition, the voltage and the frequency

at the inverter terminal continues to be the same as when the utility was connected. Under this condition, the PV inverter fails to notice the disconnection of utility and continues to operate, hence causing islanding. When the above described conditions are nearly met, the variations in the voltage and the frequency may be small and may escape the detection. This zone is called a non-detect zone (NDZ) and is shown in Figure 6.5. Some islanding scenarios are examined as follows [48]-[51], [61].

When ΔP is large: Inverter terminal voltage will vary widely and since voltage should be outside the nominal operating voltage range for detection, islanding condition can be detected effectively only if $\Delta P > \pm 20\%$.

When ΔP is small and ΔQ is large: Islanding frequency will vary and the frequency has to go out of nominal limit to be detected. For islanding protection, the inverter will fail to disconnect when the load has $q \geq 2.5$, $\Delta P = 0$, and $\Delta Q < \pm 5\%$.

When ΔP and ΔQ are small: if ΔP (< ±20%) and ΔQ (< ±5%) then this results in insufficient change in inverter terminal voltage and frequency respectively, which islands the inverter within the non-detection zone (NDZ).

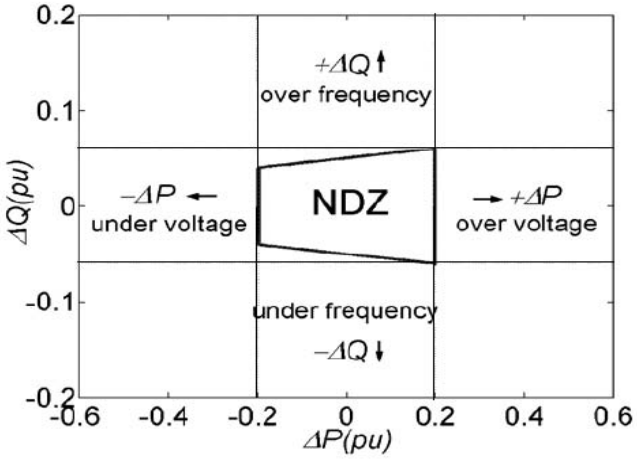


Figure 6. 5: NDZ for UVP/OVP and OFP/UFP

6.3 Proposed anti-islanding technique using wavelet analysis

Active islanding schemes usually inject certain signals (perturbation to variables like voltage and frequency) in order to detect an islanding event. This injection degrades the output power quality [59]-[61]. EN50438 [5] provides requirements relevant to the performance, operation, safety, testing and maintenance of interconnections. A summary of the essential interconnection specifications and requirements is given in Table 1 on page 7 of [24]. According to Table 1 on page 7 [24], any active islanding technique that involves injections is not allowed. In response to the above mentioned detection problems and the requirements specified by EN50438, a new technique is proposed to build an anti-islanding scheme.

The main emphasis of the proposed scheme is to reduce the NDZ to close to zero and to keep the output power quality unchanged. The new method for islanding detection is based on voltage measurements that are sensed at the PCC and their analysis using discrete wavelet transform. The new method helps to reduce the NDZ without any perturbation that deteriorates the output power quality.

6.3.1 Wavelet transform

Wavelets are functions, used to efficiently describe a signal by decomposing it into its constituents at different frequency bands (or scales) [62]. Wavelet techniques have been used in several power system applications e.g. detection, feature extraction, de-noising and data compression of power quality waveforms, power system protection etc. [63]-[65], [67]. Wavelet theory is well documented in several research publications related to power engineering applications but an explanation of the wavelet theory relevant to islanding application is provided in this section.

Discrete wavelet transform (DWT) based on Mallats' pyramid algorithm [66], also known as dyadic wavelet transform is the most frequently used method owing to its simplicity and non-redundancy. A dyadic DWT of discrete time sequence $x(n)$ of length N is essentially a decomposition of the spectrum of $x(n)$; $X(\omega)$ into orthogonal sub-bands defined by,

$$\frac{1}{2^{m+1}T} \le \omega \le \frac{1}{2^{m}T}\ ,\ m = 1, 2.....J \tag{6.12}$$

where, T is the sampling period associated with $x(n)$ and J represents the total number of decomposition levels. DWT is implemented by specially designed bank of high pass and low pass discrete filter units, h and g. The filters are half band filters with a cutoff frequency of F_s / 4, a quarter of the input sampling frequency. As the input sequence $x(n)$ propagates through the low pass and high pass filters, the filter bank, at each stage, decomposes the signal into low-pass and high-pass components through convolution (and subsequent decimation) with filters g and h, respectively. The DWT representation is composed of scaling coefficients, $c_J(n)$, representing coarse or low-pass signal

information at level $m = J,$ and wavelet coefficients (also called detail coefficients), $d_m(n),$ which represents signal detail at levels $m = 1,.....,J,$ as shown in Figure 6.6. Formally,

$$c_m(n) = \sum_n g(2n-k)c_{m-1}(k)$$
$$d_m(n) = \sum_n h(2n-k)c_{m-1}(k). \qquad (6.13)$$

At level *m*, both $c_m(n)$ and $d_m(n)$ are composed of $2^{-m}\ N$ coefficients, forming a tree-like relationship between the coefficients at successive scales. The resulting signal decomposition $[d_1, d_2, ..., d_J, c_J]$ is the dyadic DWT representation of signal $x(n)$.

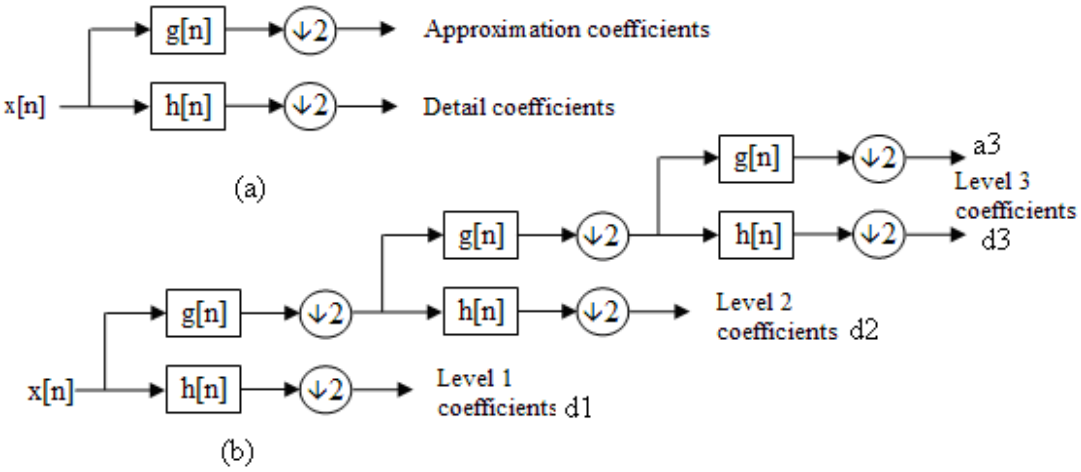


Figure 6. 6: (a) Analysis wavelet filter banks (b) 3-stage DWT decomposition

6.3.2 Proposed algorithm

To resolve the problem of non-detection zone associated with passive islanding detection methods, wavelet analysis is proposed and included with passive techniques in this Chapter. The key idea is to utilize the spectral changes in the higher frequency components of the PCC voltage during islanding. When islanding takes place under NDZ conditions, conventional passive methods which are based on threshold violations of certain PCC voltage and frequency parameters, fail to recognize it as these parameters are well within the threshold limit. Wavelet techniques examine the spectral changes occurring at higher frequency components of the PCC voltage due to islanding, thus enabling the islanding detection in the NDZ even without injecting any signal. In the proposed method, three phase PCC voltage signals are decomposed up to a chosen decomposition level J using dyadic DWT signal decomposition and analysis method described in the previous section.

Consider $V_a(t)$, $V_b(t)$ and $V_c(t)$, which are the time domain signal measurements at PCC, and $[d_{a1}, d_{a2}, ..., d_{aJ}, c_{aJ}]$, $[d_{b1}, d_{b2}, ..., d_{bJ}, c_{bJ}]$ and $[d_{c1}, d_{c2}, ..., d_{cJ}, c_{cJ}]$ are the resulting DWT decomposition outputs. Where d_{ak}, d_{bk} and d_{ck} are respectively the set of wavelet coefficients corresponding to strength of $V_a(t)$, $V_b(t)$ and $V_c(t)$ at the k^{th} frequency wavelet band. A study was carried out for a grid connected inverter system on Simulink using wavelets and an islanding scenario with matched load intentionally created. It is found that the drift in the PCC voltage is not sufficient to reach the threshold limit of UVP/OVP detector. As shown in Figure 6.10 the RMAC (root mean absolute of the wavelet coefficients) at higher frequency band details show considerable change due to the reduction of 7^{th} harmonic in the PCC voltage after islanding as shown

in Figure 6.11(a) and (b). This change can be used for islanding detection by choosing appropriate threshold settings for wavelet coefficients.

But, appropriate measures should be taken to avoid nuisance tripping due to occurrence of any transient disturbance or noise during normal operation of the system, which may produce sufficient change in magnitude of the wavelet coefficients at these frequency bands. Hence, use of a simple threshold setting based on wavelet coefficient magnitude would be risky and may lead to undesirable nuisance tripping scenarios. From extensive simulations, third level wavelet coefficients (d_3) have been found to distinguish the islanded scenario well, compared to other bands for the chosen sampling frequency, fs=5 kHz. Third level wavelet coefficients are least affected by noise which is more dominant at level 1 and are independent of varying grid impedance. Therefore, the use of the root mean absolute of the wavelet coefficients, RMAC of third decomposition level calculated once in every two cycle is proposed. Three RMAC values namely E_a, E_b, and E_c (per two cycles) of the third level wavelet coefficients corresponding to three phase PCC voltages are calculated as

$$E_p = \sqrt{\left[\sum_{i=1}^{i=L} abs(d_{p3}(i))/L\right]} \tag{6.14}$$

where, $p \in \{a, b, c\}$ and , L is the number of coefficients per two power cycles. Islanding is detected when one or more of these calculated RMAC parameters becomes lower than a set threshold. The above comparison to threshold is immediately done after the RMAC is calculated, hence not requiring any peak detector unlike in [68], making the proposed algorithm computationally less of a burden on the DSP.

Daubechies “db4” mother wavelet [62], has been used because of its compactness, and localization properties. Mother wavelet Db4 performs well in detecting power system disturbances according to [69], [70].

It was noted that the 3rd decomposition level (312.5-625Hz) was not only the most suitable level in terms of distinguishing the islanded scenario, but also independent of varying grid impedance (due to the presence of 5th and 7th harmonics in the grid voltage). This above statement is supported by introducing an operator $DRMAC\left(\left[E_p\right]_{on} - \left[E_p\right]_{off}, d_m\right)$, which can be applied on any one of the PCC voltages a, b or c to determine the most suitable decomposition level/frequency band for anti-islanding detection purposes.

DRMAC gives the difference in root mean absolute of the wavelet coefficients for the selected decomposition level d_m, where m=1, 2, 3 and 4 for this case. The RMAC for grid connected and islanded mode is represented as $[E_p]_{on}$ and $[E_p]_{off}$ respectively.

$$DRMAC = \left| \sqrt{\left[\sum_{i=1}^{i=L} abs(d_{pm}(i))/L \right]_{on}} - \sqrt{\left[\sum_{i=1}^{i=L} abs(d_{pm}(i))/L \right]_{off}} \right| \qquad (6.15)$$

where, $p \in \{a, b, c\}$, $m = 1,.....,J$, and L is the number of coefficients per two power cycles. By applying this operator, the results shown in Table 6.1 are obtained.

Table 6. 1: Results of DRMAC applied to phase 'A' of voltage at PCC using simulation

Decomposition Level	**DRMAC(Va)**
1st (1250-2500 Hz)	|0.0271-0.0222| = 0.0049
2nd (625-1250 Hz)	|0.045-0.051| = 0.006
3rd (312.5-625 Hz)	|0.119-0.09| = **0.03**
4th (156.25-312.5 Hz)	|0.23-0.25| = 0.02

As a higher value of DRMAC implies large difference between grid connected and islanded mode, hence the 3rd decomposition level (312.5-625Hz) is the most appropriate decomposition level/frequency band for islanding detection.

It is also stated in [68] that resistive variations of the grid impedance have a higher impact compared to inductive variations and the frequency band 200-400 Hz can be used to obtain the best possible resolution and independence from the characteristics of the PCC (grid impedance). Therefore 3rd decomposition level is chosen for islanding detection purposes in the proposed technique.

6.3.3 System setup

To test the performance of the proposed wavelet based islanding scheme, the grid connected inverter system shown in the Figure 5.27 of Chapter 5 has been simulated on Matlab/Simulink platform with the proposed anti islanding scheme. The system in Figure 5.27 is exactly the setup that is used for experimental purposes. The full control program flowchart, run with the incorporated anti-islanding protection on the prototype is shown in Figure 6.7. The main part of the control program flowchart has already been described in Chapter 5 (Section 5.21) which is extended with the additional anti-islanding protection scheme as described in Section 6.3.2. The rectified dc source (with dc-dc boost stage) is interfaced to the grid using a three phase pulse width modulated six-switch dc-ac inverter (switched at 20 kHz). As the inverter is based on three MG150J2YS50 IGBT devices (600V, 150A), the maximum dc link voltage established is 400V. The normal operating voltage of the dc link is set at 300V. In order to connect to the grid using this dc link, a three-phase step down isolation transformer 400:130 V L-L is used. The inverter is connected to the low voltage side which presents a grid of 75V rms. Circuit breaker, SW2, is closed to connect the synchronized inverter to the grid while circuit breaker, SW1, is opened to experience grid failure (islanding). For simulation to experience almost a real grid, the harmonics spectrum of the grid voltage was acquired from power quality monitor PowerXplorer-PX5 of Dranetz-BMI. 5^{th} and 7^{th} harmonics are typically around 1.6% and 0.7% respectively with THD <5%. These two harmonics were added on the 75V rms, 50 Hz grid voltage within the simulation. Power flows from the inverter to the grid depending on the user defined current reference.

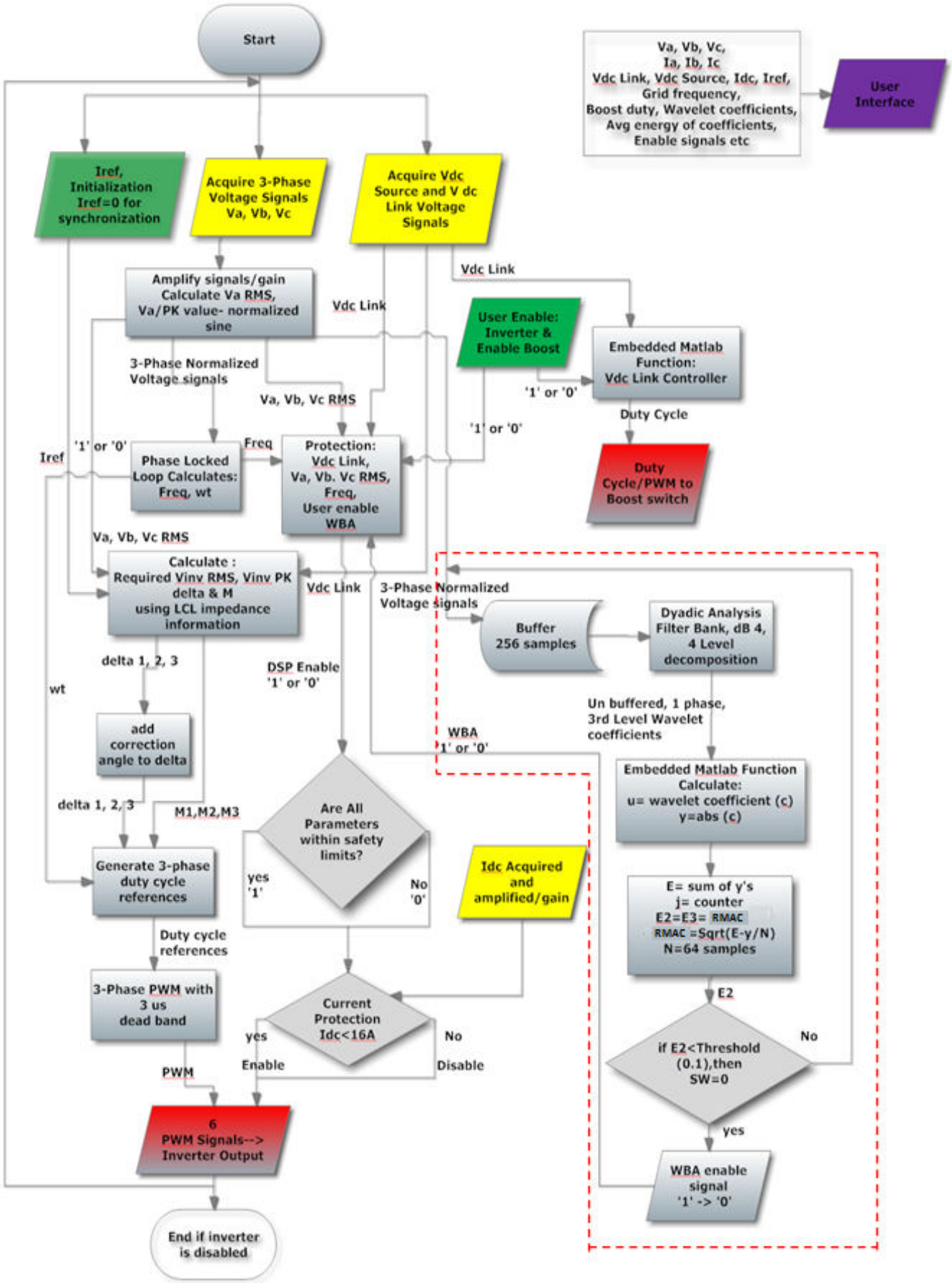


Figure 6. 7: The control program extended with the proposed anti-islanding scheme

6.3.4 Simulation results

In the simulation, the inverter supplies power to a maximum load of 1.4 kW. The power transferred to the grid changes with change in local load power demand. The power frequency of the simulated system is 50Hz and PCC voltage measurements are converted to per unit values before these are processed through the wavelet islanding detection block.

Different islanding scenarios (islanding with large power mismatch, close to zero power mismatch NDZ etc.) have been created using the three phase breaker circuit (SW1) and by changing the power demand of local load connected to the system. During normal operating condition, the wavelet islanding detection block generates a constant inverter enable signal of value '1' and upon detecting islanding the value of the enable signal is changed to '0' thus halting the inverter operation. Since DG is usually expected to supply active power, the inverter is forced to operate at unity power factor; only active mismatch of power is considered.

For the first case, (case 1) an island is created at 0.3 seconds with large power mismatch condition (i.e. $\Delta P > \pm 20\%$). The local load demand in this case is 2.5 kW out of which 1.4 kW is supplied by the inverter and rest by the grid. For brevity, results for only one phase are shown in Figure 6.8 A large power mismatch due to islanding causes the voltage at PCC to drift away from the nominal operating range within two cycles as shown in the Figure 6.8(e), thus enabling the OVP/UVP relays to detect the islanding condition easily. (a), (b), (c), (d), (e) and (f) of Figure 6.8, Figure 6.9 and Figure 6.10 indicate: (a)inverter current, (b) grid current, (c) load current, (d) PCC voltage , (e)

voltage RMS and (f) frequency. The red dotted lines indicate the voltage and frequency tolerance limits.

In the second case, (case 2) islanding is created with 'close to zero' power mismatch (i.e. in NDZ) where, the local power demand is 1.4 kW as shown in Figure 6.9. It can be seen from Figures 6.9 (e)-(f) that after islanding (at 0.3s) the PCC voltage and frequency remains within the operating range. Thus, confirming that the passive methods based on the OVP/UVP and OFP/UFP relays fail to detect islanding under such conditions.

This 'close to zero' power mismatch (case 3) islanding scenario is also tested using the proposed wavelet based method as shown in Figure 6.10. Depicted in Figures 6.10(g) and 6.10(h) are the third level wavelet coefficients (absolute values) and corresponding RMAC values calculated as per equation (6.14). It can be observed from the Figure that there is a considerable change both in the magnitudes of wavelet coefficients and in calculated RMAC values after islanding event.

The wavelet coefficient showed a reduction in RMAC value (reducing peak) in the (most suitable) 3rd decomposition level. A simple method in the algorithm is used to detect the reduction instead of using advance pulse triggering methods or a peak detector as used in [68] to distinguish the higher peaks from the lower ones.

The inverter enable signal which was set to '1' (for normal operation) is forced to '0' by the wavelet detection module once the RMAC value decreases below the set threshold (0.1), ceasing the inverter operation and power delivery to the load as shown in Figure 6.10(i). The response time of the proposed method in simulation is found to be around 2.5 cycles which is fast enough to comply with the standards.

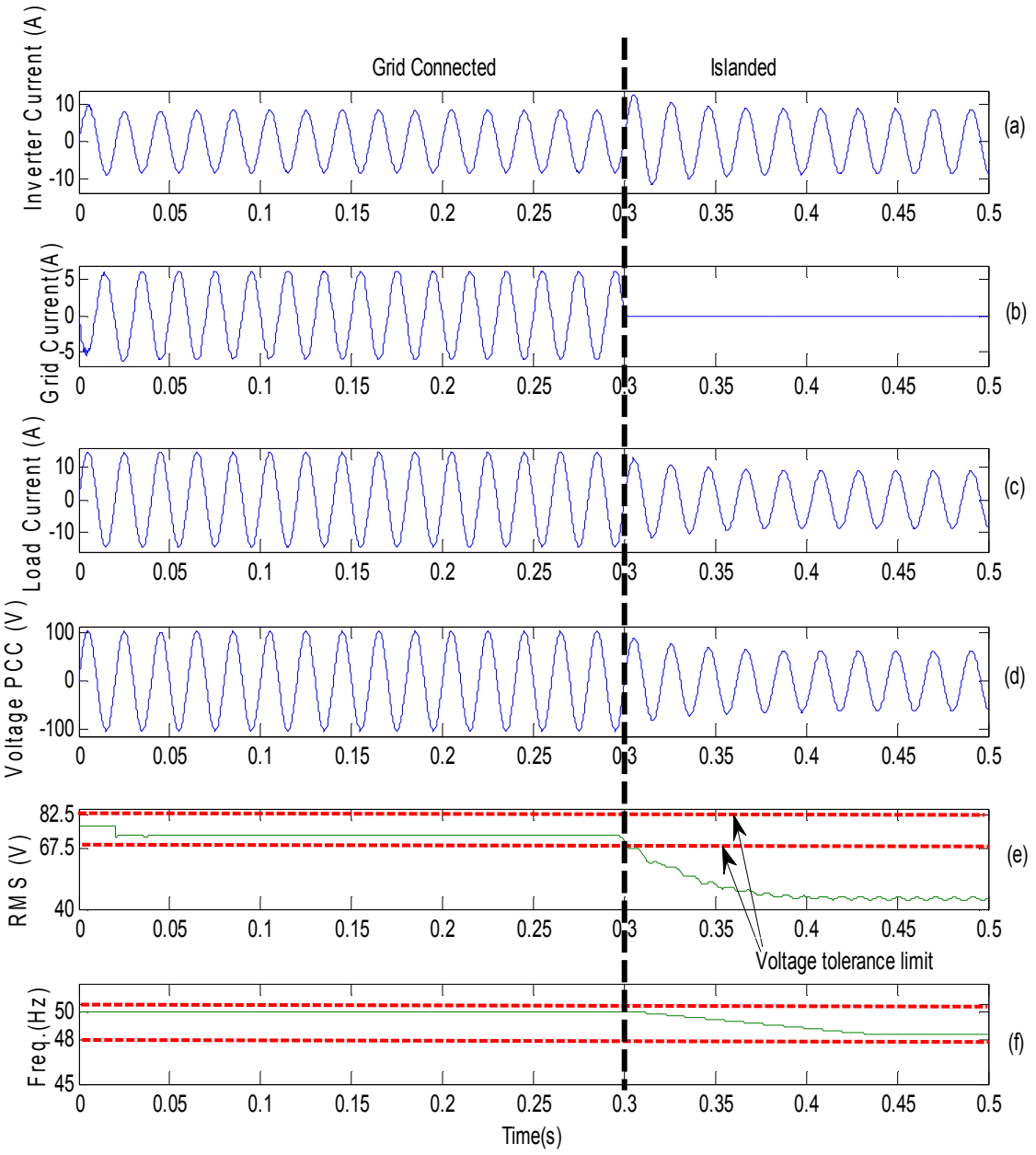


Figure 6. 8: Case of large power mismatch with passive method

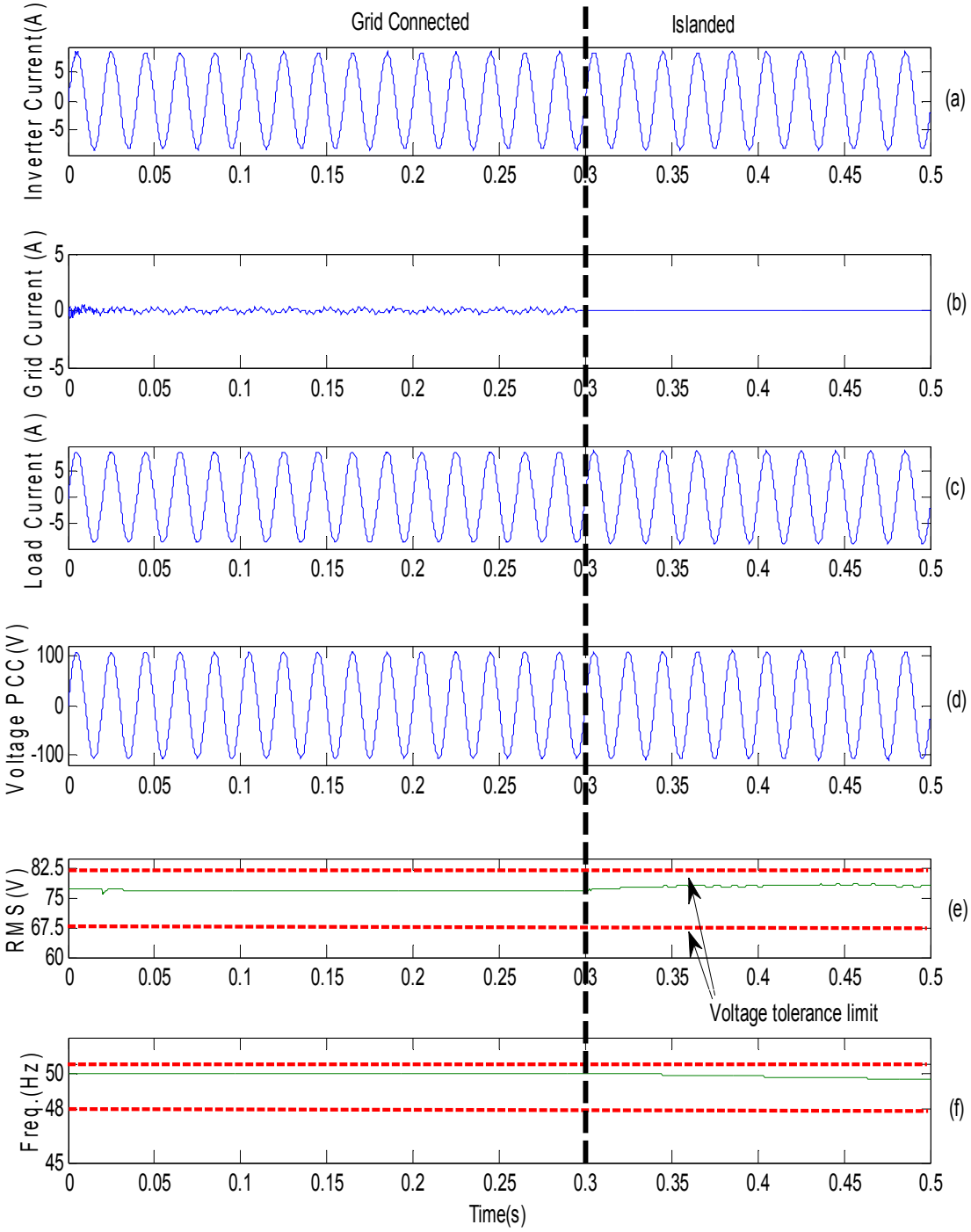


Figure 6. 9: Case of "close to zero" power mismatch (NDZ) with passive method

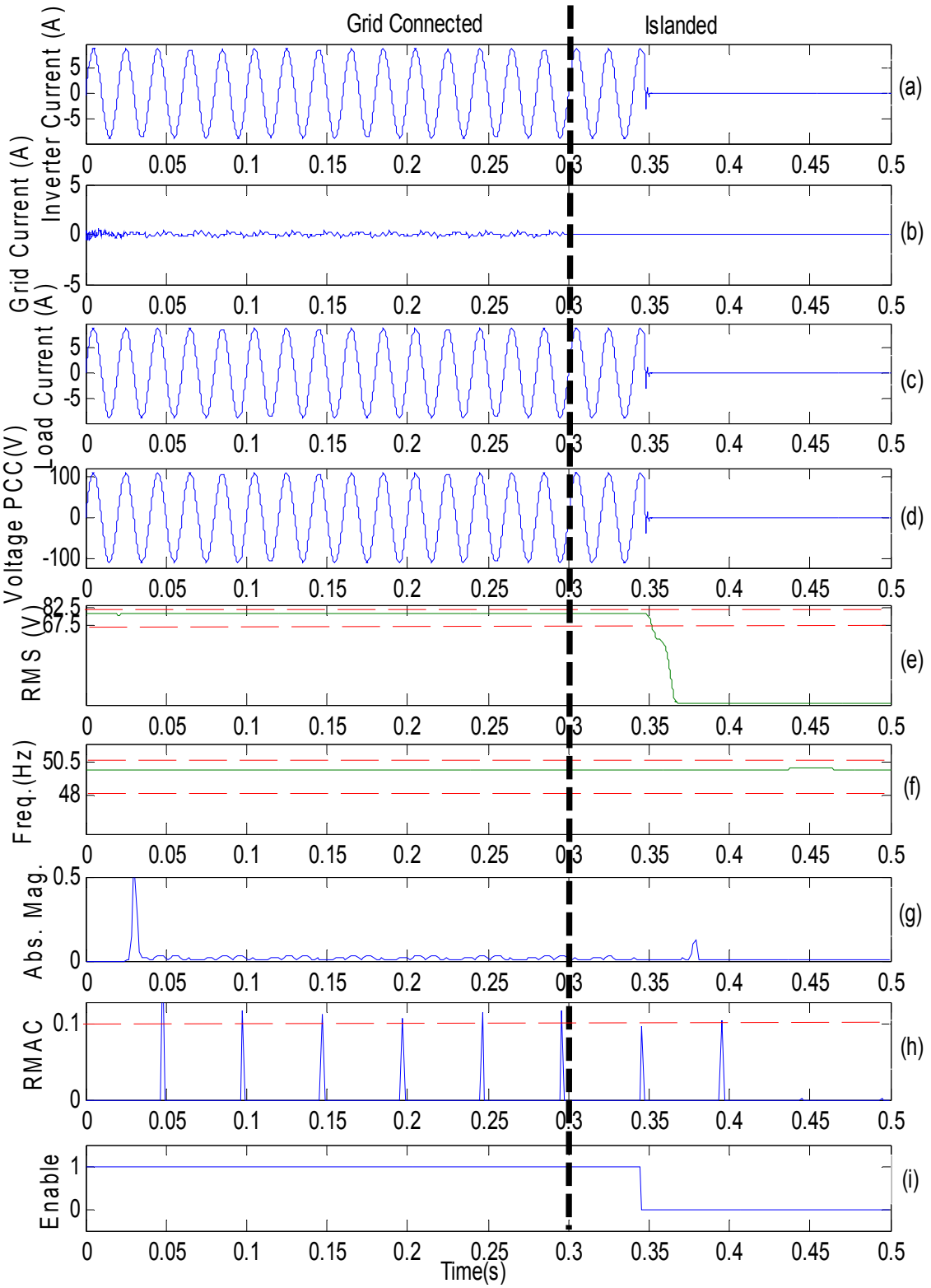
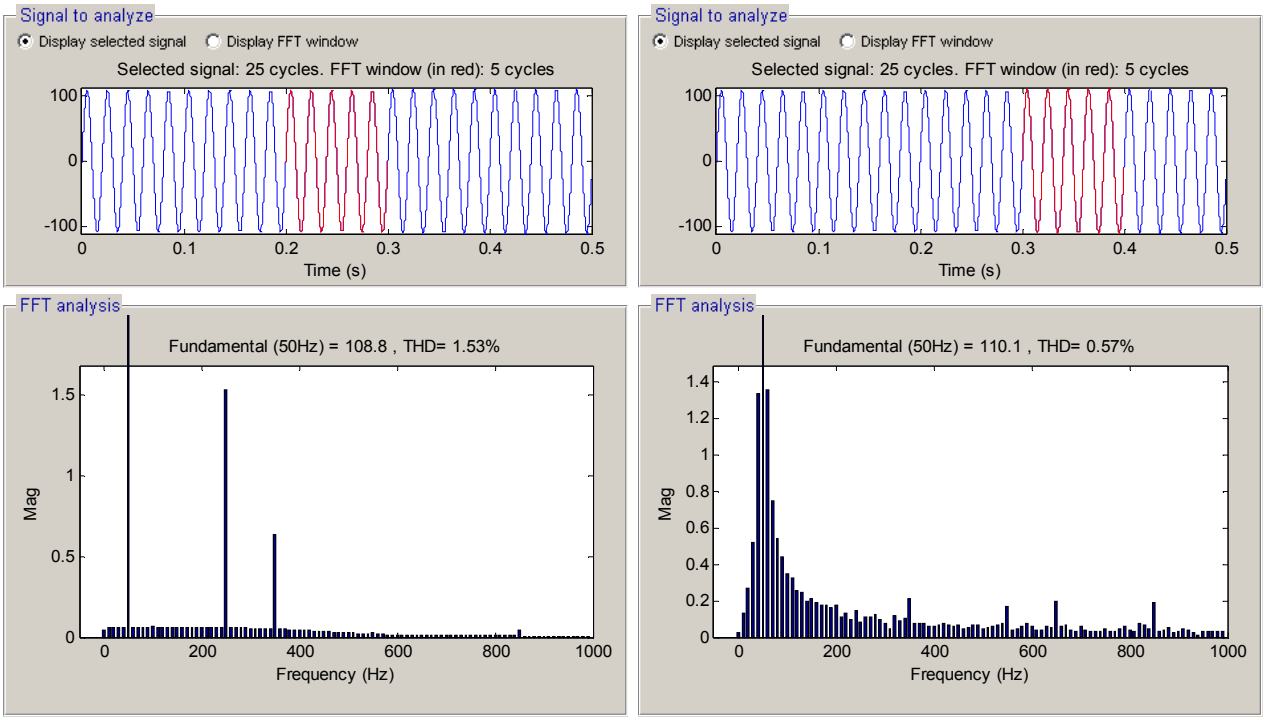


Figure 6. 10: Case of "close to zero" power mismatch (NDZ) with wavelet-based detection scheme



(a) Before islanding (b) After islanded

Figure 6. 11: Harmonic spectrum of the PCC voltage

6.3.5 Experimental results

In order to test this proposed technique experimentally on a real three-phase grid connected inverter system using dSpace DS1104 DSP , experiments are carried out on the 5.625 kW prototype that was built. Figure 5.27 of Chapter 5 shows the system diagram with component values of the experimental setup and appropriate sensors used for control purposes. The maximum sampling frequency achieved was fs=5 kHz. The three cases seen for simulation are again verified by hardware experiments. (a),(b),(c),(d),(e) and (f) in Figure 6.12, Figure 6.13 and Figure 6.14 represent: (a) grid voltage (stepped down via transformer) ,(b) current flowing through phase A, (c) RMAC of 3^{rd} level wavelet coefficients ,(d) wavelet based analysis(WBA) enable signal, (e) inverter enable and (f) absolute values of 3^{rd} level wavelet coefficients

Figure 6.12 shows the experimental result of case 1 where a large mismatch of power occurs after islanding and conventional passive techniques are able to detect the situation. The islanding scenario is manually generated by opening the breaker (SW1) on the grid side at 62.76s in Figure 6.12.

Figure 6.13 shows the result of case 2 where power mismatch after islanding (at 31.59s) is very small and conventional passive techniques are unable to prevent islanding.

Figure 6.14 shows case 3 where the proposed wavelet based technique detects islanding with a very low level of power mismatch which occurs at 29.5s. The wavelet based scheme detects islanding within 2.5 cycles.

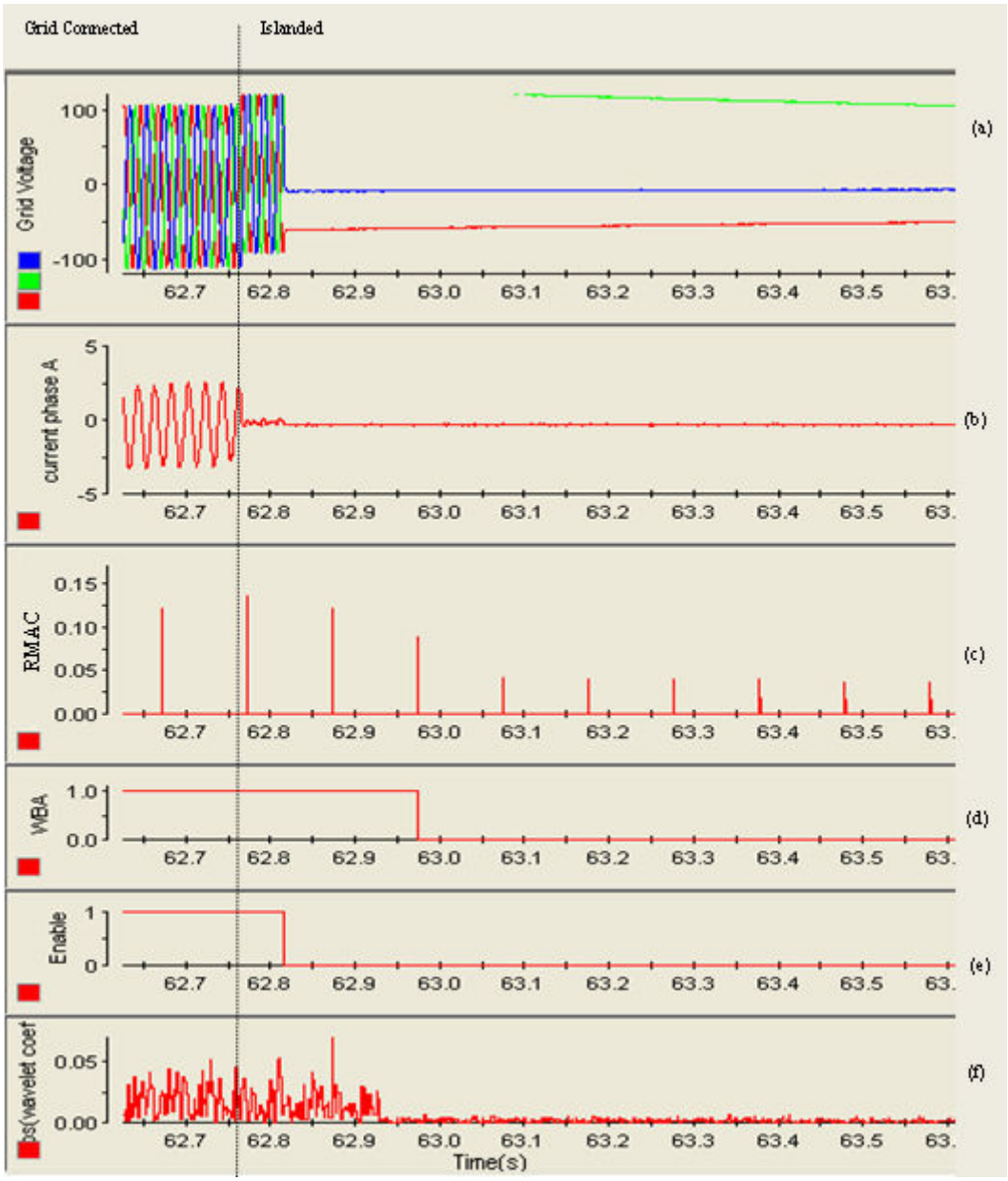


Figure 6. 12: Experiment result: Case of large power mismatch with passive method

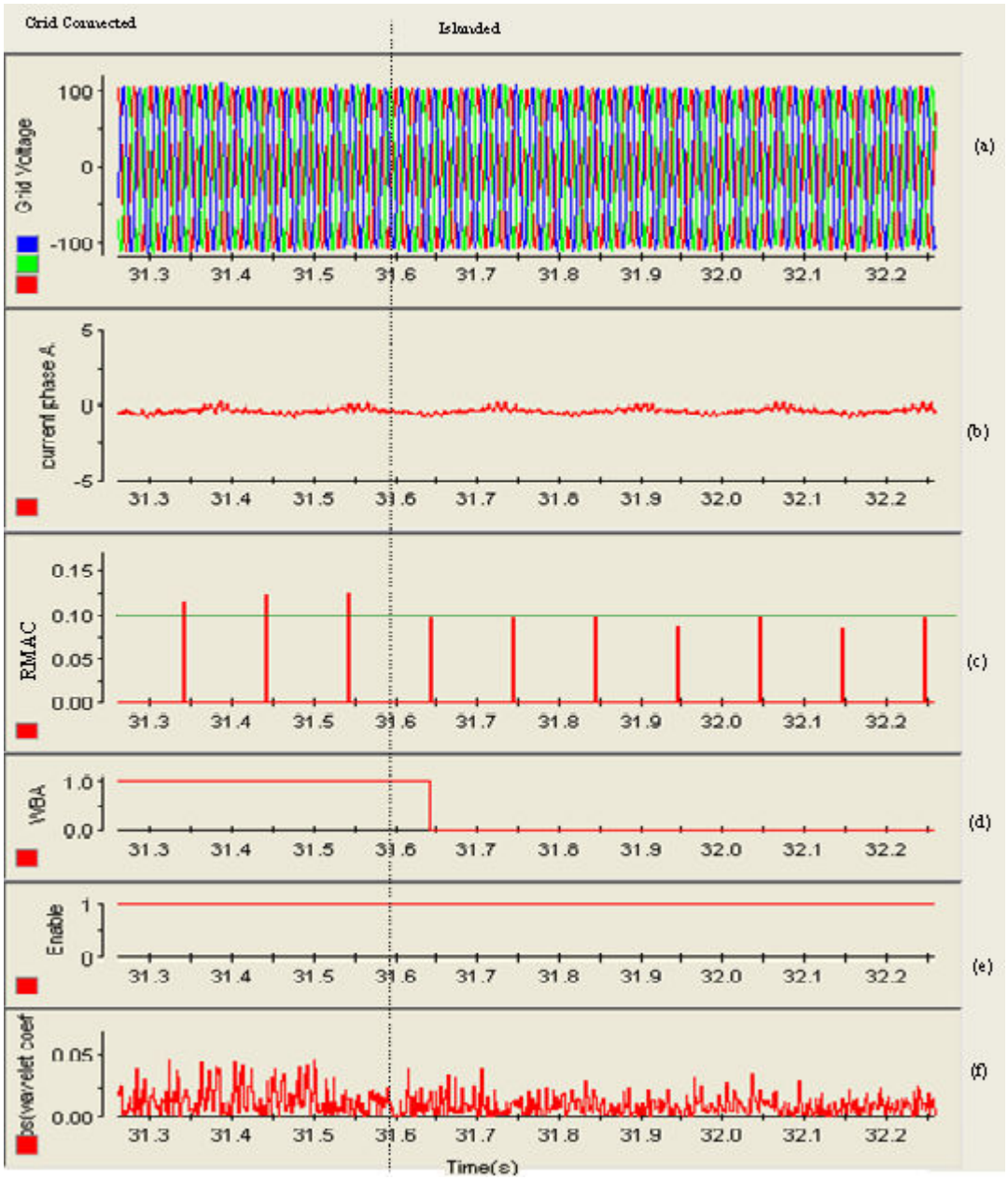


Figure 6. 13: Experimental Result: Case of "close to zero" power mismatch (NDZ) with passive method

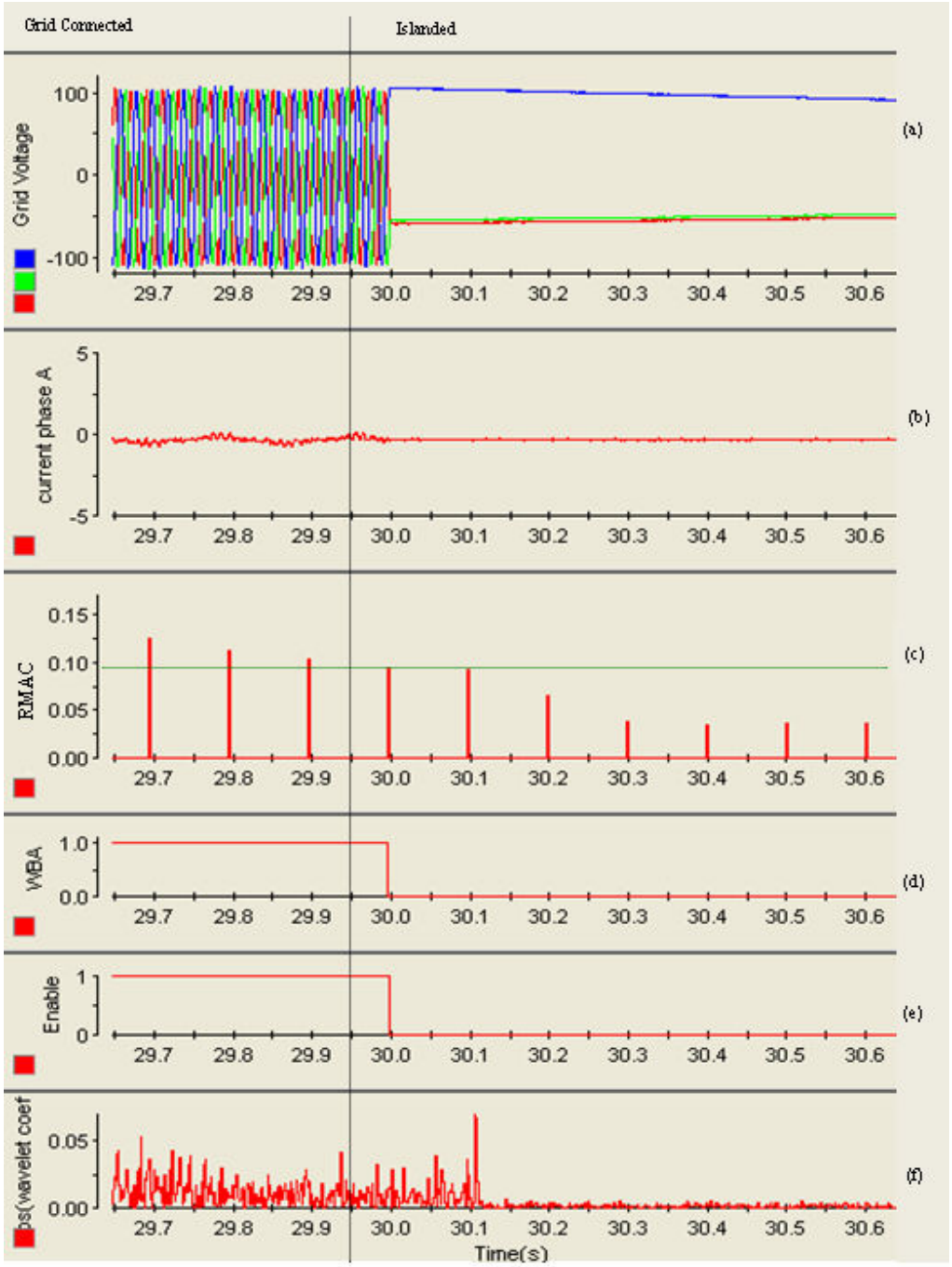


Figure 6. 14: Result: Case of "close to zero" power mismatch (NDZ) with wavelet-based detection scheme

6.4 Conclusion

Islanding situations need to be prevented with distributed generation for safety reasons and to maintain the quality of power supplied to customers. The Chapter looked into various passive and active islanding techniques in terms of their capability to reduce the NDZ, significant strengths and weaknesses. The power mismatch between the load and the PV (DG) was analysed to help better understand the islanding scenario. A large mismatch of power shows the voltage at PCC drifting away from the nominal operating range within few cycles but "close to zero" mismatch of power shows the voltage within the nominal range, making it difficult to detect by OVP/UVP and OFP/UFP relays in a passive environment. The proposed scheme operates on the PCC voltage measurement and is able to detect the islanding condition within an average of 2.5 power frequency cycles. To avoid nuisance tripping due to transient disturbances, which may result if wavelet coefficient thresholds are used directly, a new parameter namely RMAC of the 3^{rd} level wavelet coefficients are proposed to detect the islanding condition. The results presented clearly demonstrate the effectiveness of the proposed islanding detection scheme even under the worst case scenario i.e. 'close to zero' power mismatch condition. The experimental results match the simulation results in all cases as expected. Only up to three levels of decomposition are required in the technique developed, and no peak detector is being used. This reduces the burden on the processor and allows rapid decisions to be taken in the event of grid failure. For best results, initial grid harmonic voltage content information could be utilised to determine the most suitable level of RMAC to indicate the islanding scenario. It can be noted that if the grid voltage is completely harmonic free, the present method proposed will not work. However, in a distributed network environment, this possibility is highly unlikely.

Chapter 7

7. CONCLUSION AND FUTURE WORK

7.1 Conclusion

The main objective of this research work was to improve the control and operation of a three-phase photovoltaic grid connected inverter for enhanced performance. Four major sections were identified for improvement where the detailed research work and contributions have been highlighted within this thesis.

The objectives laid down for this PhD thesis have been successfully realized through analysis, simulation and experimental investigations. As part of this research activity a 5.625 kW prototype of a three-phase grid connected inverter has been constructed and tested with the necessary interface circuits. Also, a three-phase grid connected photovoltaic inverter simulation model has been built in Simulink which was used to design the prototype and to develop new control solutions. The completion of the three-phase grid connected inverter and the effectiveness of the proposed techniques has been proved through numerous simulation and experimental results.

A thorough comparison of the dc-dc boost with voltage source inverter and the Z-Source inverter has been reported. A design guide along with a clear understanding of the working principles, equations and control methods for the Z-Source inverter has been presented.

The proposed ac side P&O maximum power point tracking algorithm requires only a small ac current sensor (dc sensor-less) compared to two large dc voltage and current sensors required by the conventionally used P&O method. The proposed method

has been simulated and its effectiveness proved by comparing the results to the more commonly used P&O method under the same conditions. The proposed method is expected to present the same drawbacks faced by the conventionally used method during photovoltaic panel shading and presence of multiple power peaks as discussed in [71]; but has the advantage of detecting the maximum power point using only inverter ac current. Furthermore this technique seems well suited for controlling the boost stage of both dc-dc boost with VSI and Z-Source inverters in order to track the MPP. Unlike in the conventional P&O method no continuous perturbation of power is required, so there is no oscillating voltage that requires additional software filtering.

The novel passive islanding detection scheme proposed using wavelet analysis has been demonstrated in simulation and experimentally on the hardware prototype. The satisfactory disabling of the inverter within 2.5 to 5 power cycles during grid failure has been demonstrated using both simulation and experimental results. The proposed scheme is designed to work during very small mismatch of the power between the DG and the load bringing the non detection zone close to zero. The presence of fifth and seventh harmonics during the availability of grid voltage and the absence of these harmonic contents at inverter output after the grid has failed, has been utilized for anti islanding protection using wavelets. The islanding protection scheme proposed along with the UVP/OVP/UFP/OFP, dc link protection and over current protection have been tested and prove sufficient for overall inverter protection during islanding and non islanding conditions.

A working prototype of a three-phase grid connected inverter was developed to demonstrate the new techniques and the performance of the hardware and control

algorithms met our design targets. The dc link controller and the three-phase software PLL performed very well.

It is hoped that the theoretical and the experimental investigations reported in this thesis will help in establishing new designs and control schemes for grid connected inverters. It is further hoped that application engineers will be able to utilize the concept and results reported in this thesis for further enhancement of the operation and control of grid connected inverters under real photovoltaic and adverse grid supply conditions.

7.2 Future work

There are several important points, which need to be investigated but could not be included in this current research work. The following issues have been identified as some possible topics for future work in this area:

1. The control of the inverter can be extended to realize a current controlled strategy rather than voltage control and also blanking time compensation could be investigated.
2. Further testing could be carried out comparing the conventional and the proposed ac side P&O MPPT algorithm in Chapter 3 under real PV and DSP implementation to validate their effectiveness under normal and shading conditions. Also the proposed scheme could be investigated with different grid conditions, as ac current is used for tracking the MPP.
3. Further studies could be carried out to utilise the analysis of the proposed wavelet based technique in Chapter 6. The inverter control algorithm could be modified to operate in both active and reactive power transfer mode so that the PV inverter could provide var compensation and local voltage support (needs to comply with the future standards).
4. The developed system can be extended for micro grid applications, where the inverter can run both in stand alone and in grid connected mode.

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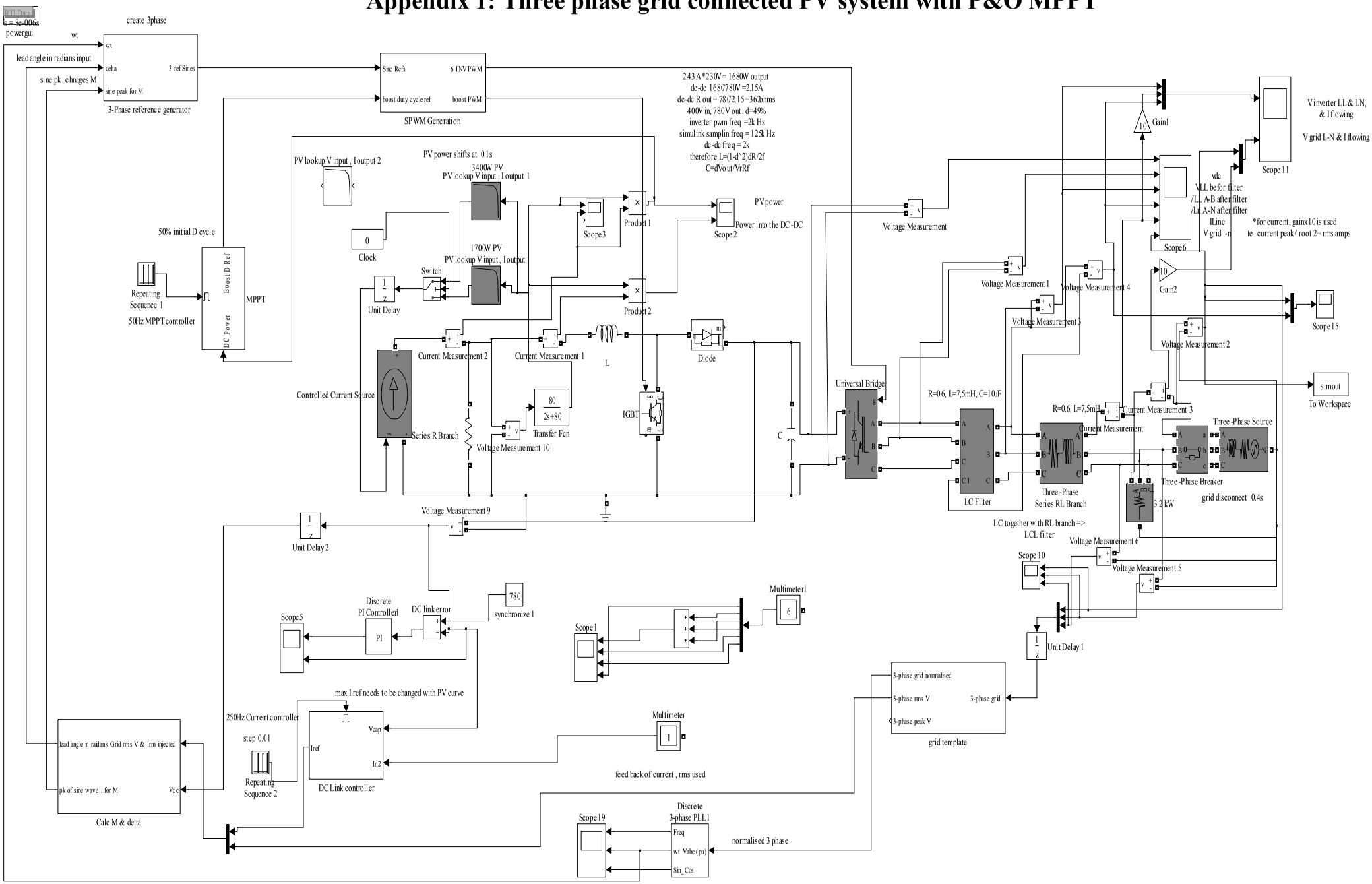
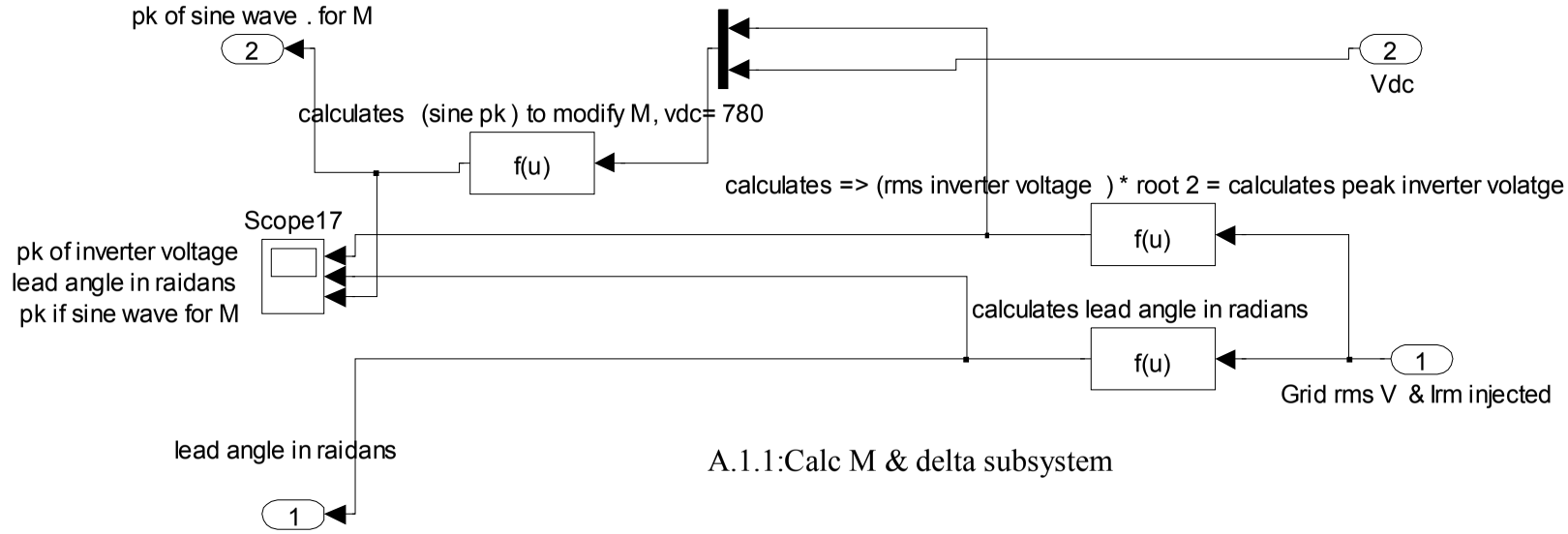
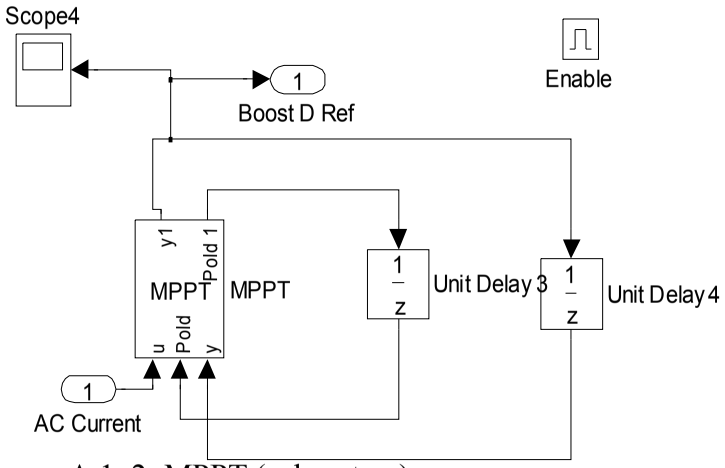
Appendix 1: Three phase grid connected PV system with P&O MPPT

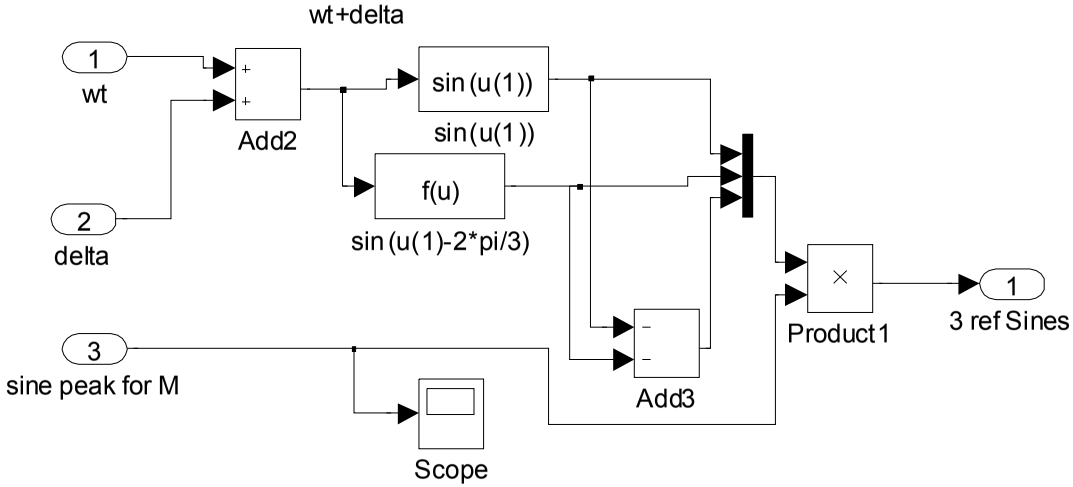




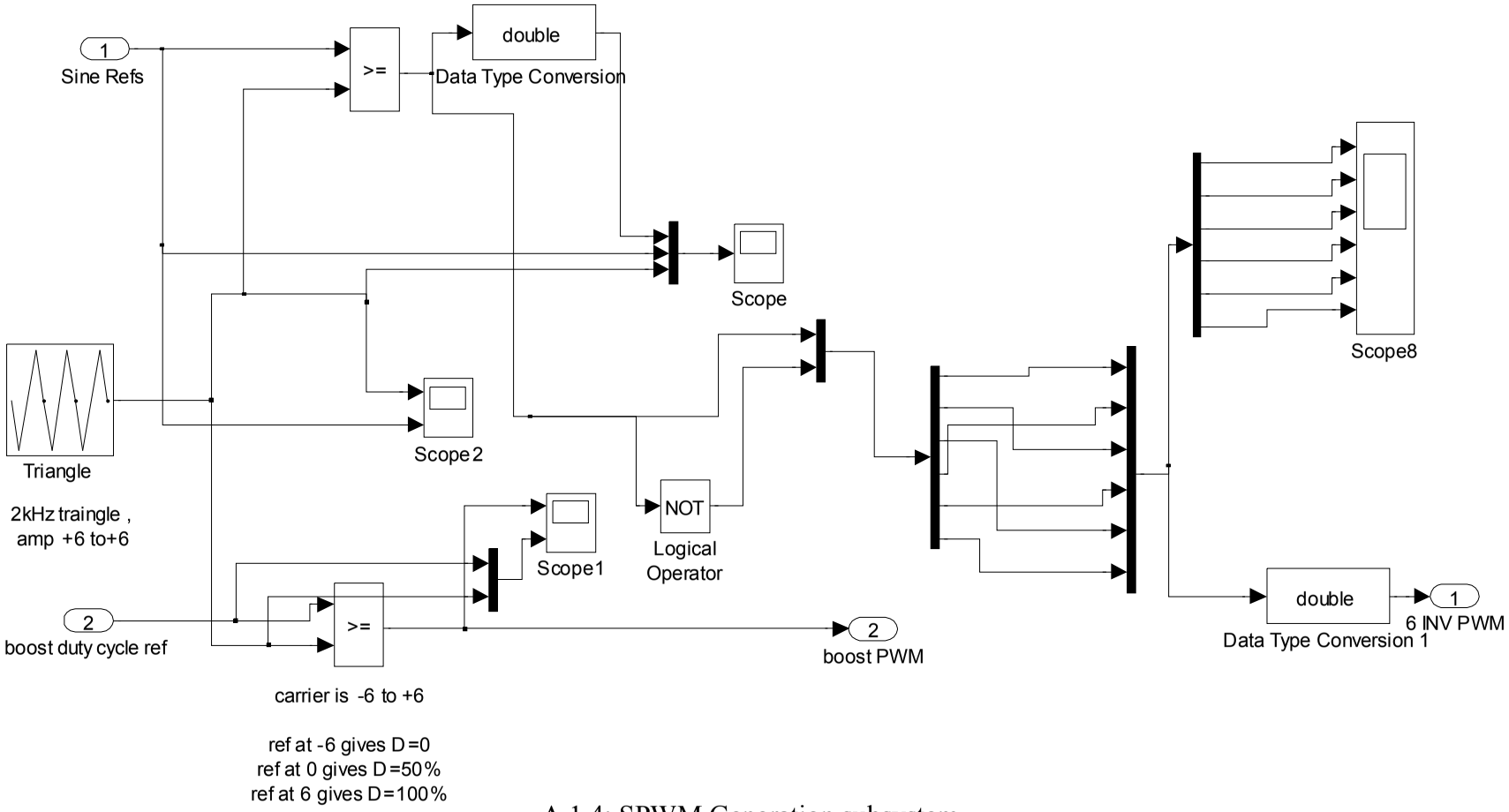
A.1.1:Calc M & delta subsystem



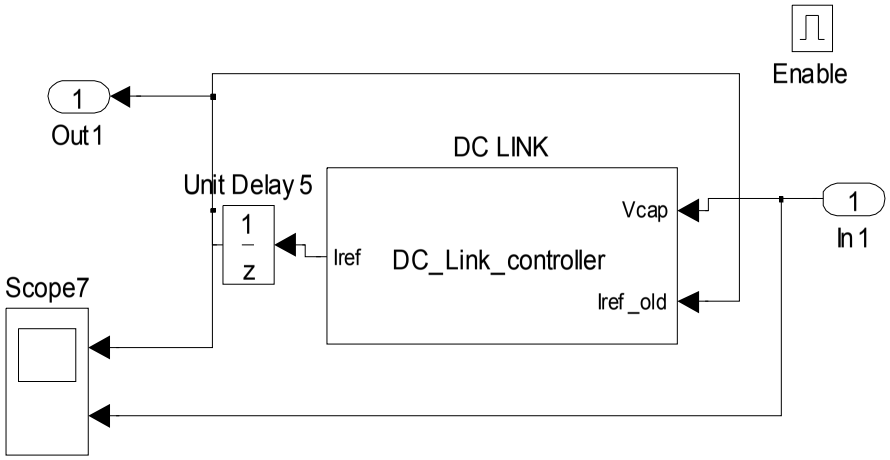
A.1. 2: MPPT (subsystem)



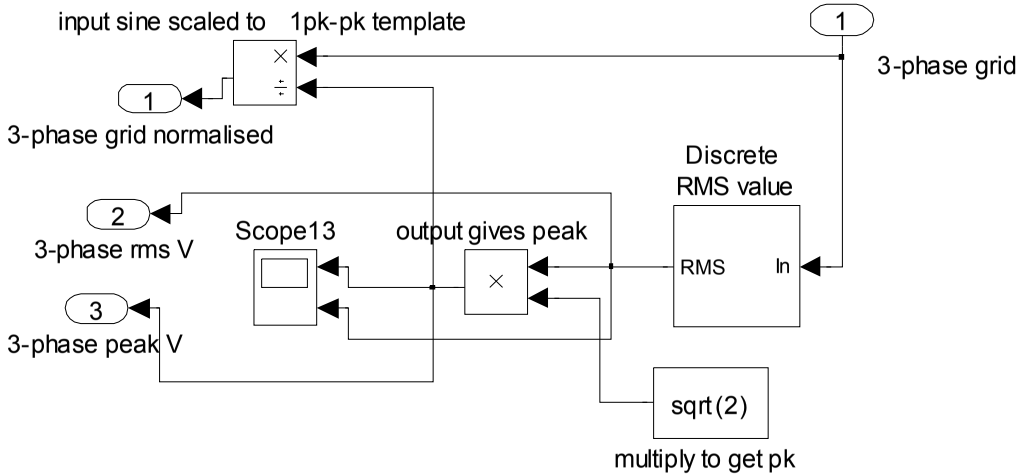
A.1.3: 3-Phase reference generator subsystem



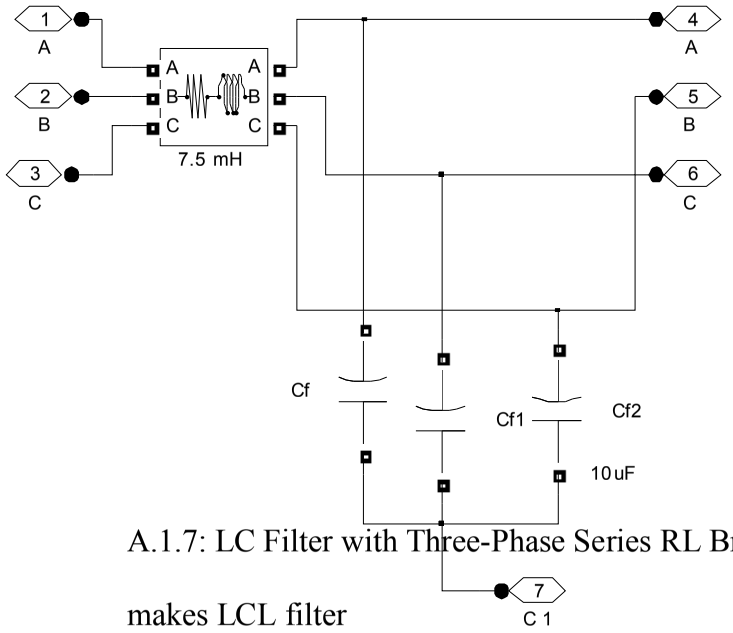
A.1.4: SPWM Generation subsystem



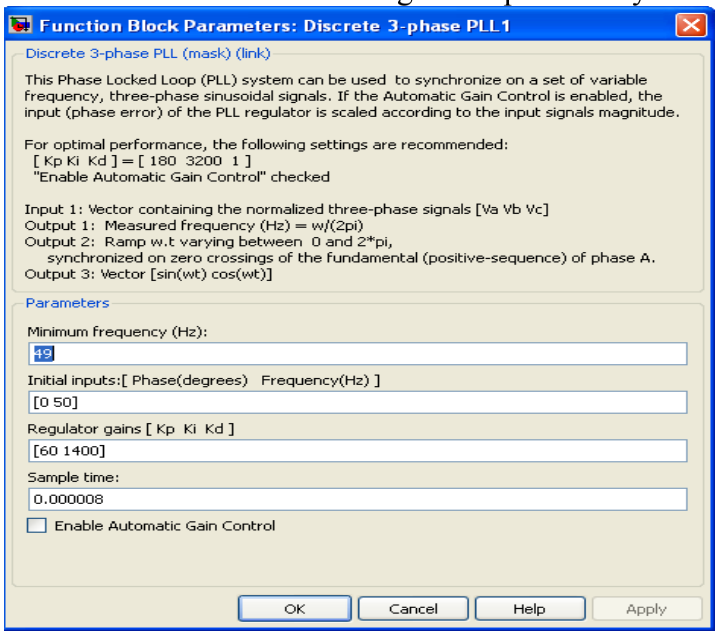
A.1.5: Vdc Link Control subsystem



A.1.6: grid template subsystem

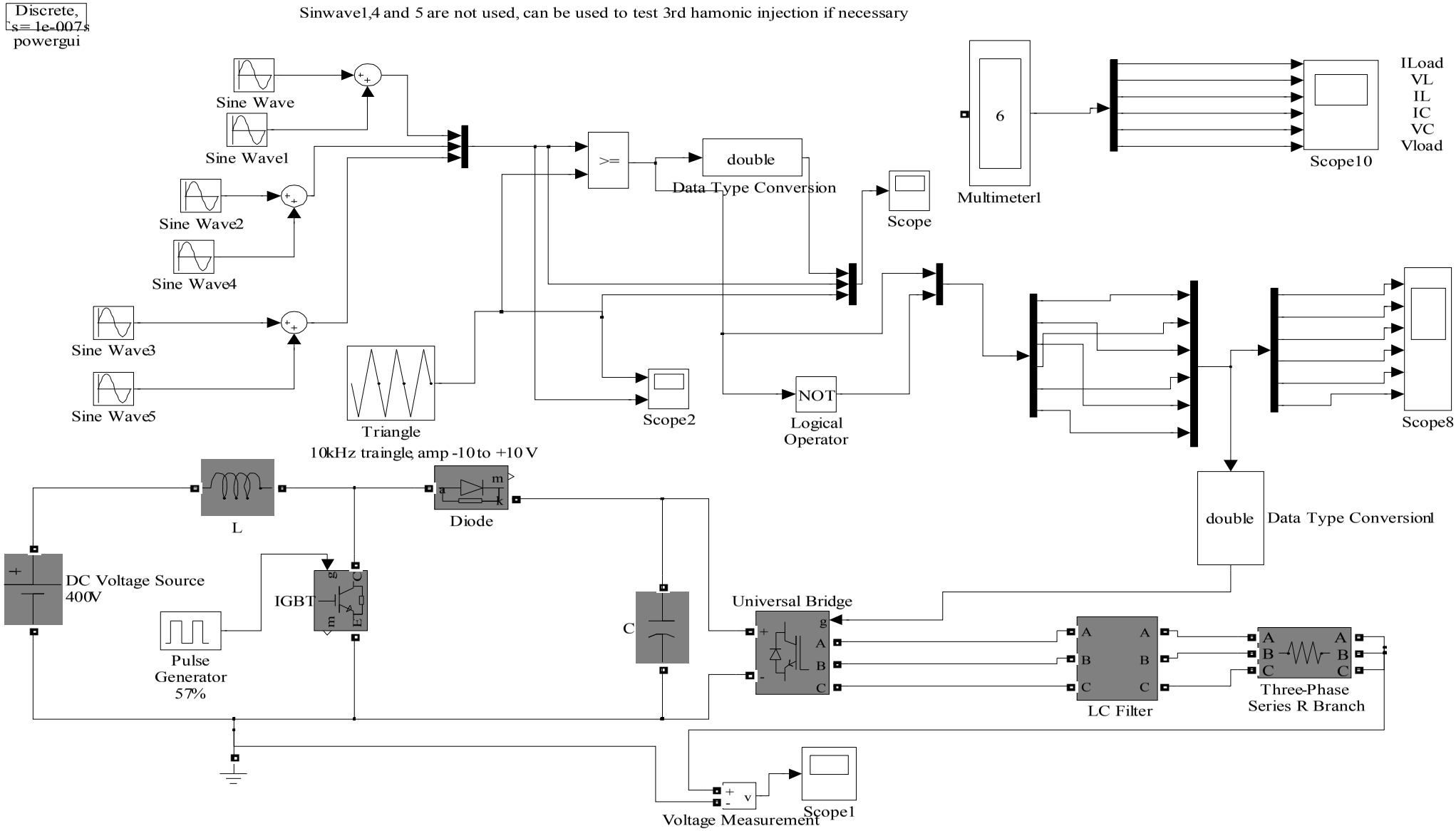


A.1.7: LC Filter with Three-Phase Series RL Branch makes LCL filter

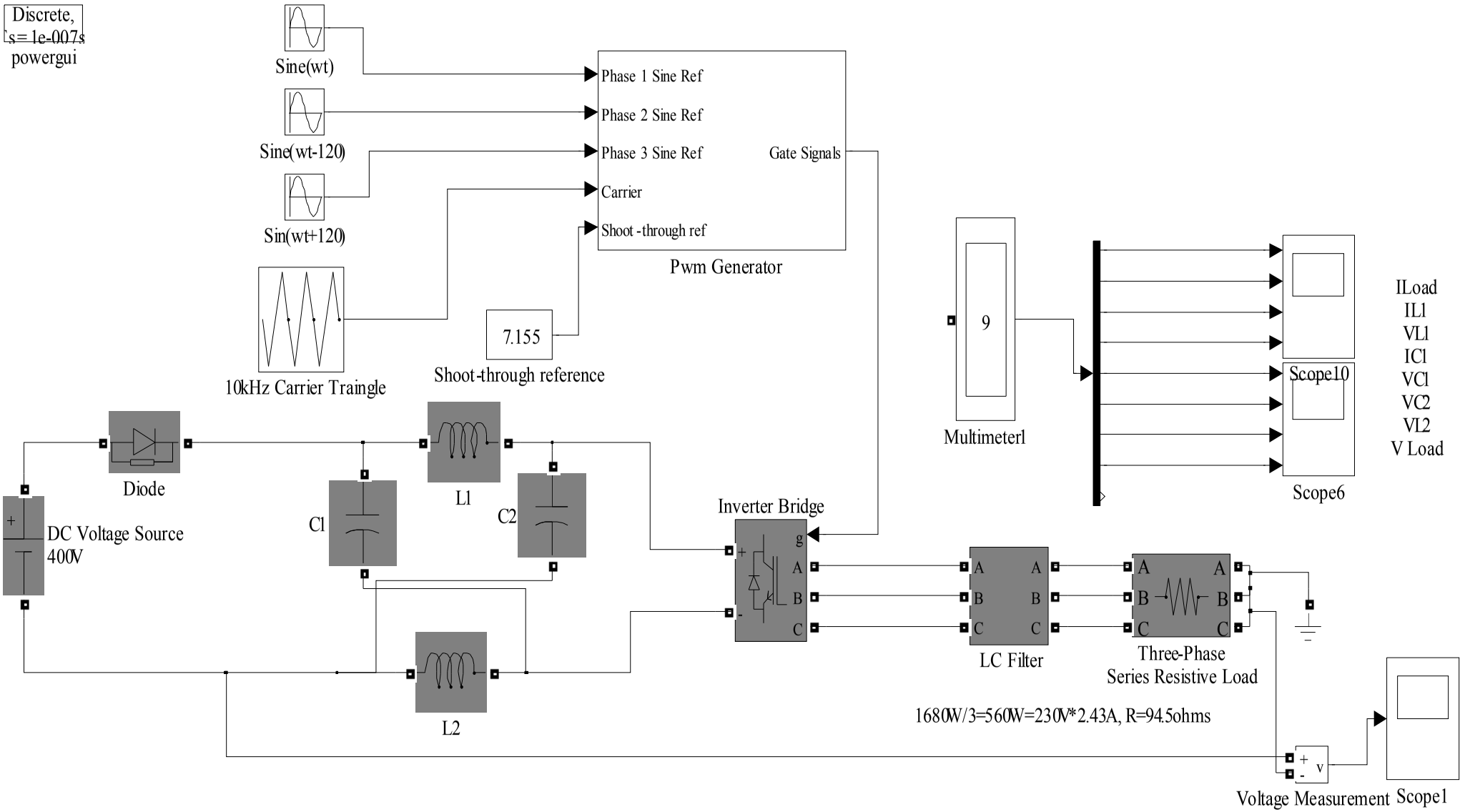


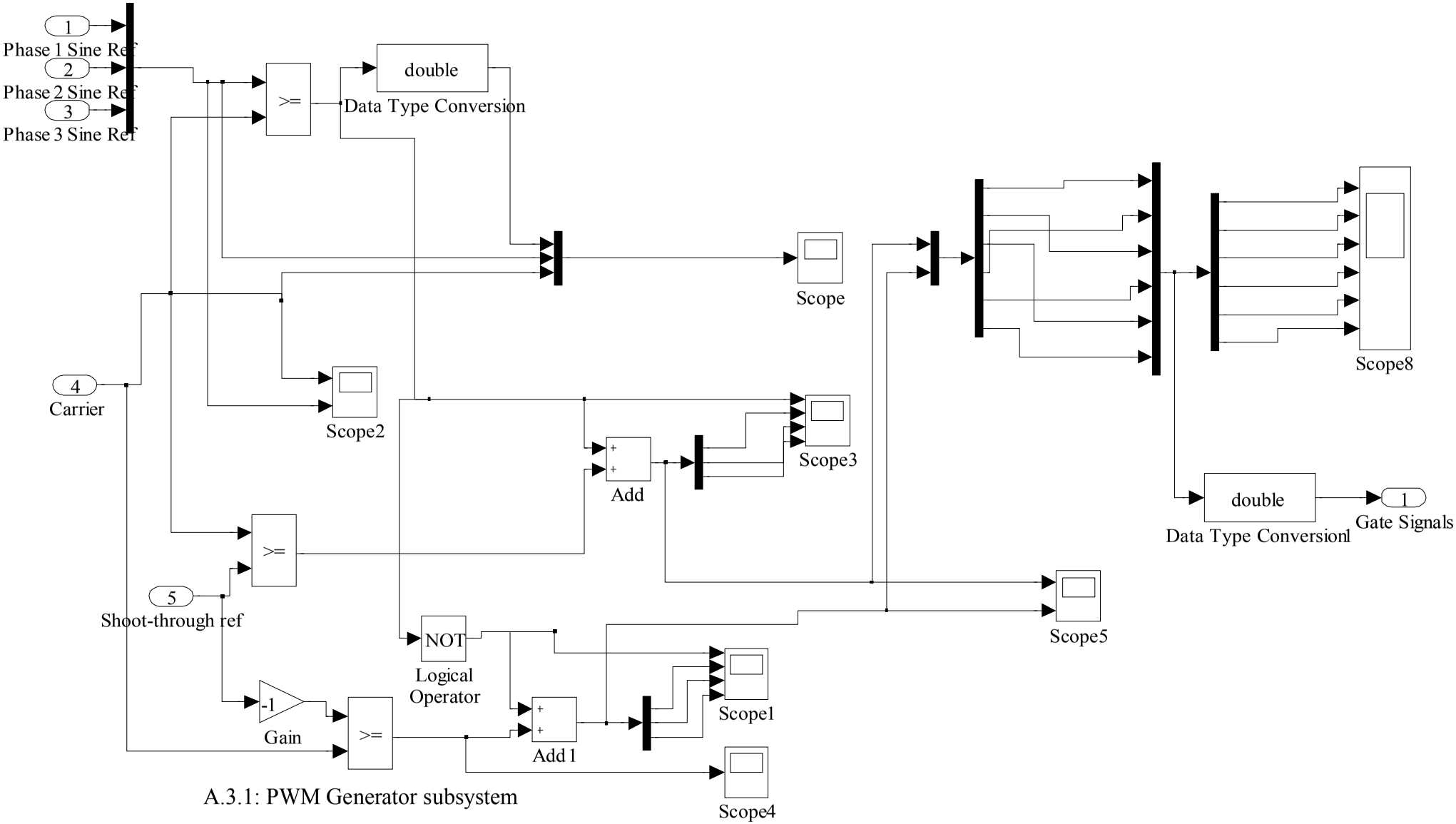
A.1.8 Discrete 3-phase PLL1

Appendix 2: dc-dc boost with VSI



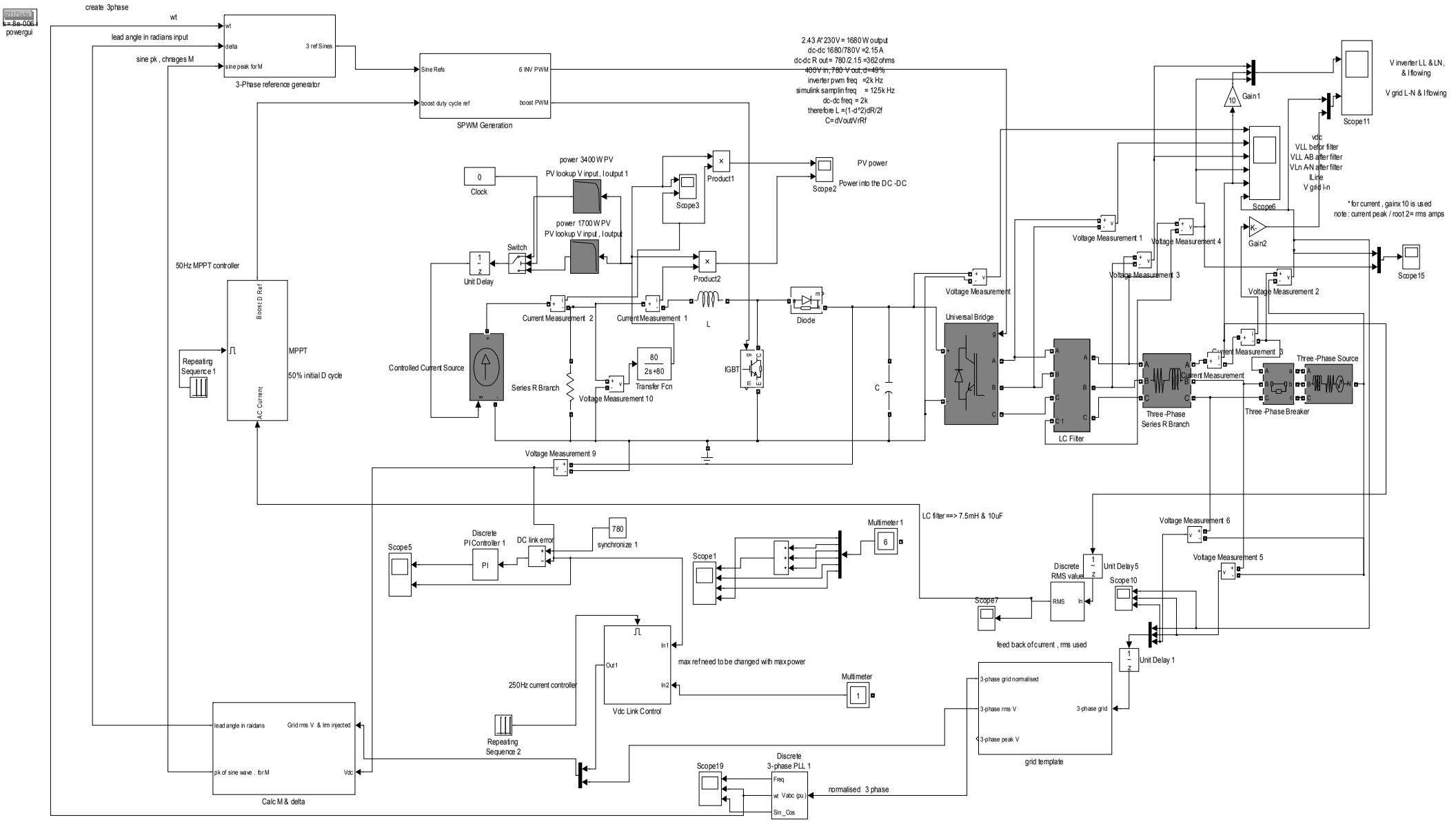
Appendix 3: Z-Source Inverter



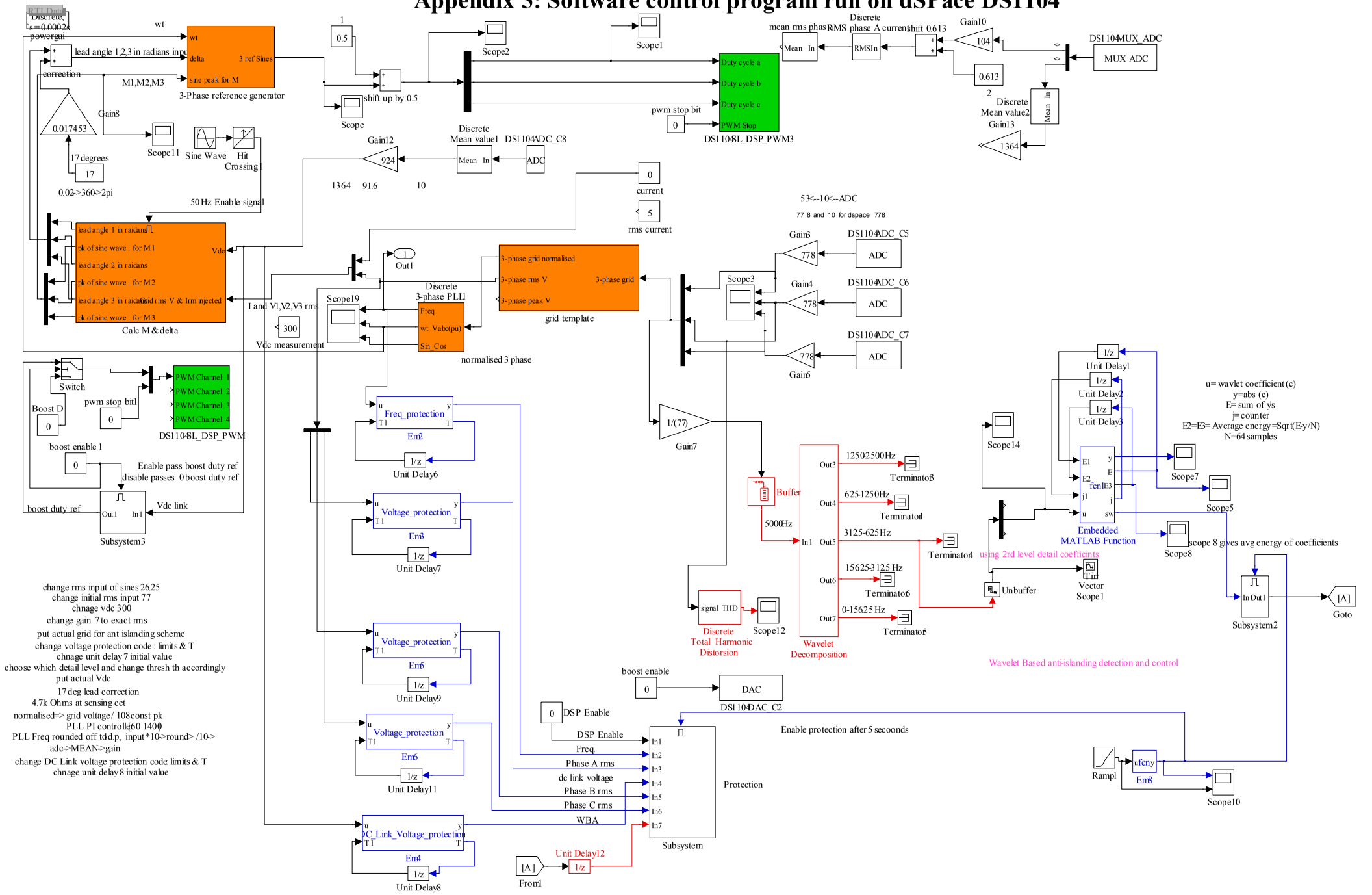


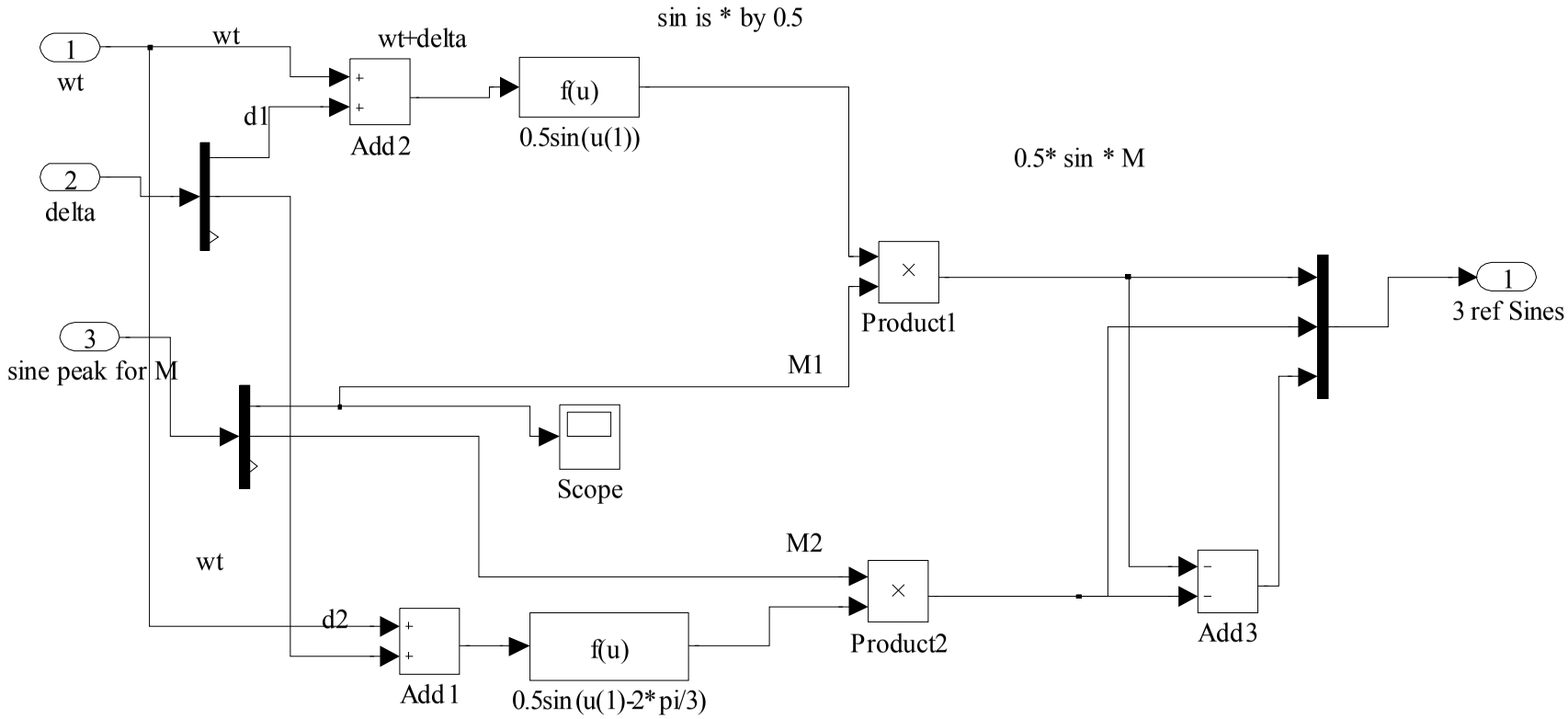
A.3.1: PWM Generator subsystem

Appendix 4: Three phase grid connected PV system with novel AC side P&O MPPT

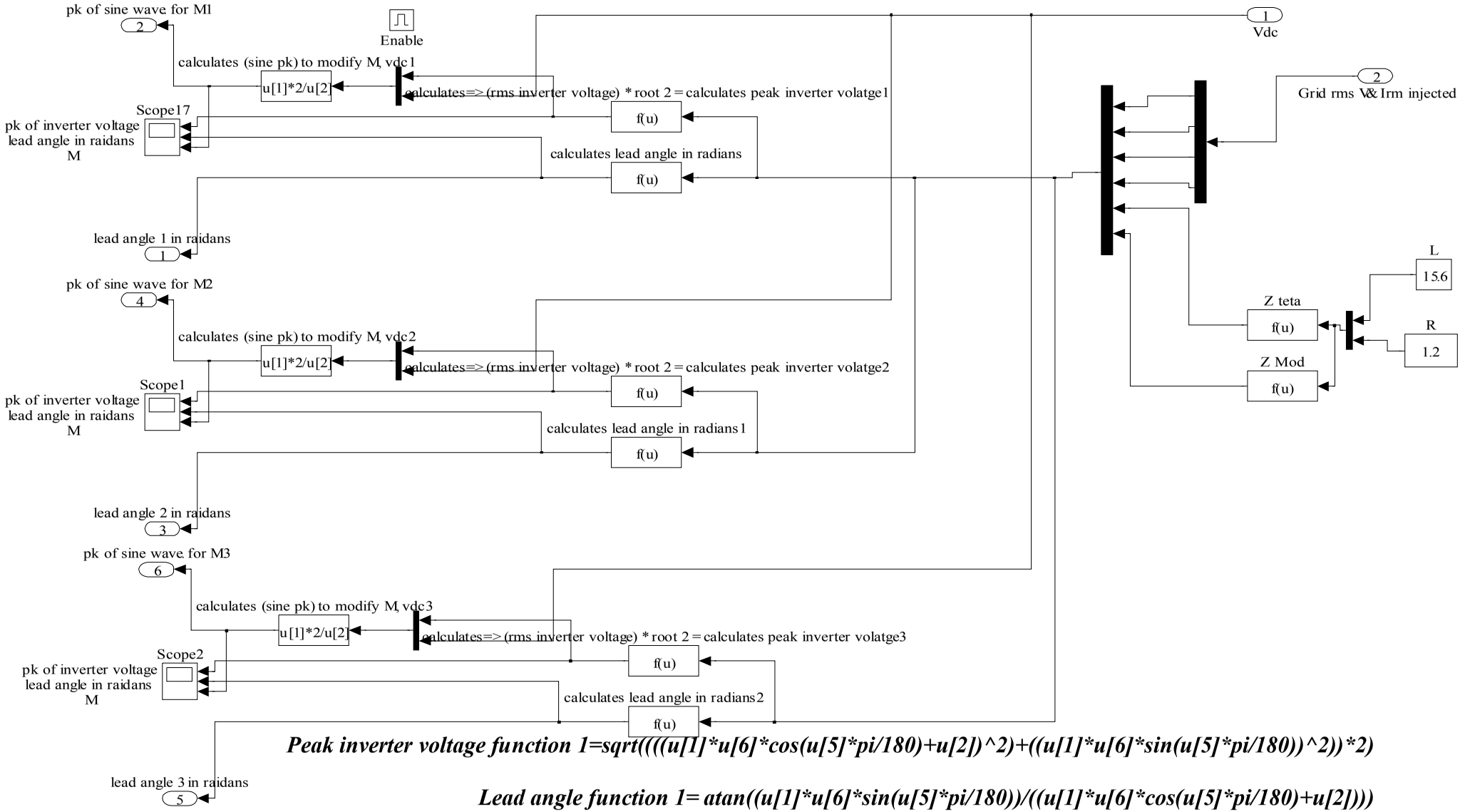


Appendix 5: Software control program run on dSPace DS1104





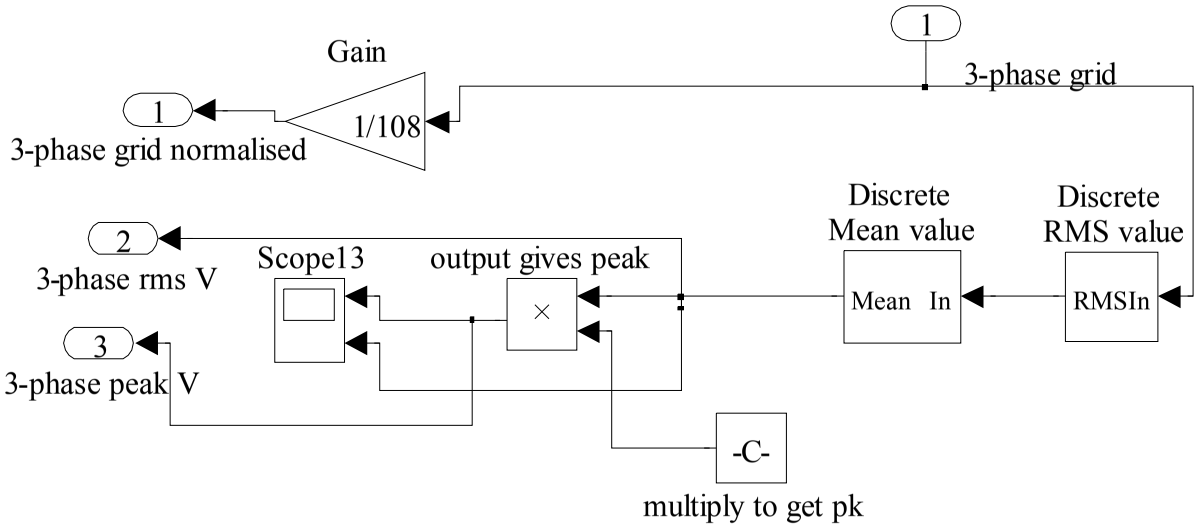
A.5.1: 3-Phase reference generator (control program subsystem)



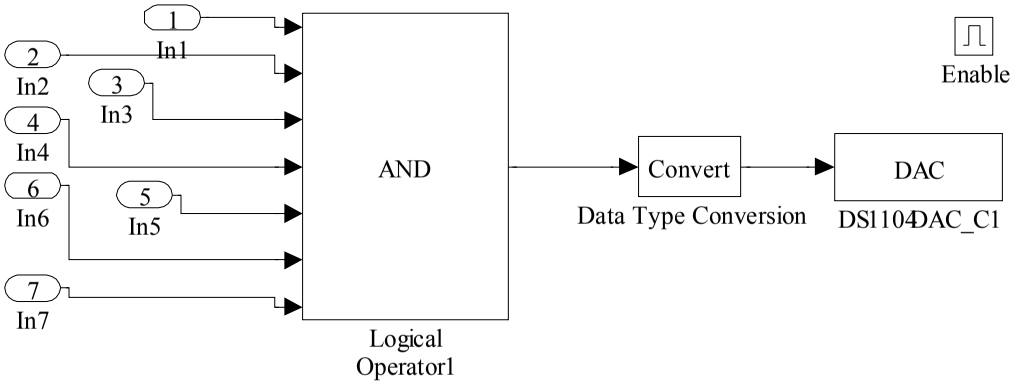
Peak inverter voltage function 1=sqrt((((u[1]*u[6]*cos(u[5]*pi/180)+u[2])^2)+((u[1]*u[6]*sin(u[5]*pi/180))^2))*2)

Lead angle function 1= atan((u[1]*u[6]*sin(u[5]*pi/180))/((u[1]*u[6]*cos(u[5]*pi/180)+u[2])))

A.5.2: Calculate M & delta (control program subsystem)

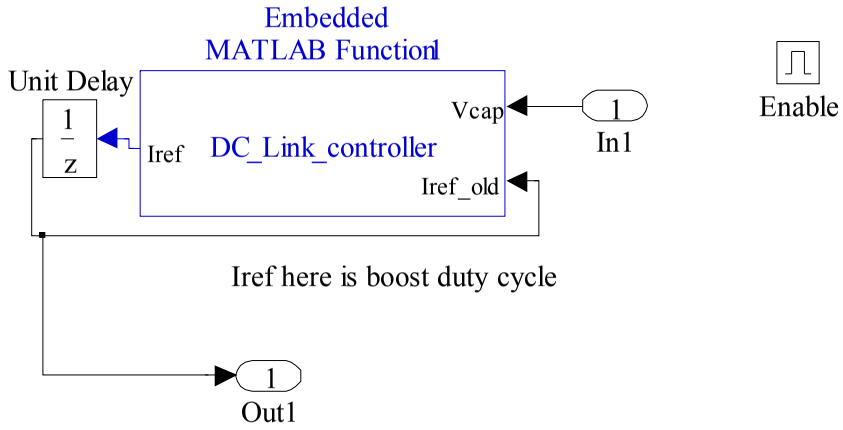


A.5.3: grid template (control program subsystem)



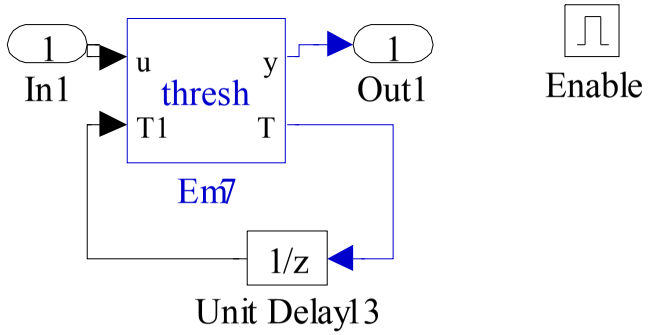
A.5.4: Subsystem (control program subsystem)

```
function Iref    = DC_Link_controller(Vcap,Iref_old)
% This block supports an embeddable subset of the MATLAB language.
% See the help menu for details.

if (Vcap>305)
   inc=-1;
else if(Vcap<285)
   inc=1;
   else
      inc=0;
   end
end
 ref = Iref_old +(0.0001*inc);
 if (ref>0.3)
   ref=0.3;
else if (ref<0)
      ref=0;
   end
end
Iref=ref;
```



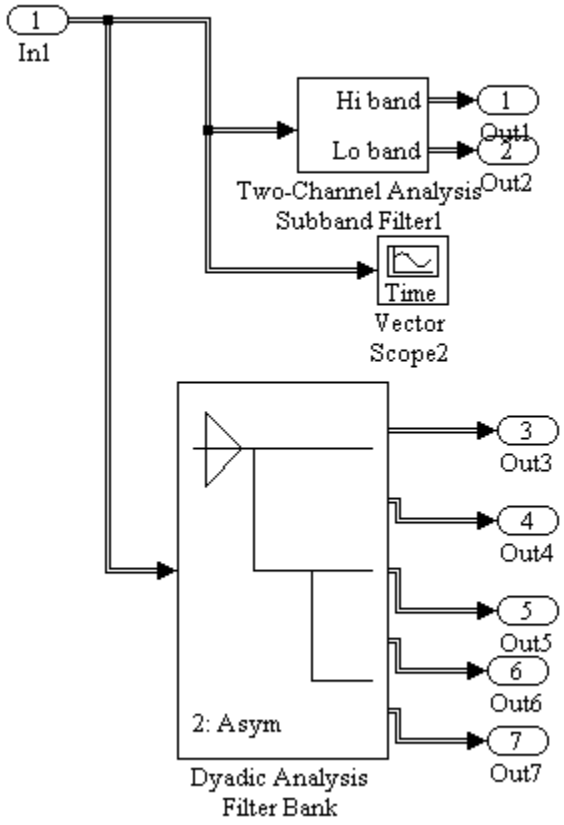
A.5.5: Subsystem 2 with the embedded Matlab Code (control program subsystem)

```
function [y,T] = thresh(u,T1)
% This block supports the Embedded MATLAB subset.
% See the help menu for details.
y=1; T=1;
th=0.5; %threshold
% y = u;
if (th>u)% once threshold reached switch is put to zero
   y=0;
   T=u;
end
if (th>T1)
   y=0;
   T=T1;
end
T1=T; %T1=T=0 until U>th, then T1=T=U and it keeps the switch to zero(i.e inverter is put to off continously)
```



A.5.6 Subsystem 3 with the embedded Matlab Code (control program subsystem)

```
function [y,E,E3,j,sw] = fcn1(E1,E2,j1,u)
% This block supports the Embedded MATLAB subset.
% See the help menu for details.
E=0; j=1; E2=0; N=64;sw=1;
 y = abs(u); % absolute value of coefficient
 E=E1+y;%Energy calculated==>adding all the absolute coefficients
  j=j1+1;
if(j>=N)
   E2=sqrt((E-y)/N);% calculating average energy during 1 cycle (divided by N )
  j=1;
  E=0;
  if(0.1>E2)
      sw=0;
  end
end
j1=j;
E1=E;
E3=E2;
```



A.5.7: Matlab Embedded function Fcn1 (control program) and Wavelet Decomposition (control program subsystem)

A.5.8 : Embedded Matlab Codes for inverter protection

EM2 code (control program)

```
function [y,T] = Freq_protection(u,T1)
% This block supports the Embedded MATLAB subset.
% See the help menu for details.
y=1; T=50;
if (u>50.5 || u<48)% once threshold reached,upperlimit (+1%), lower limit (-4%),switch is put to zero, 48 to 50.5 for 50Hz
   y=0;
   T=u;
end
 if (T1>50.5 || T1<48)
   y=0;
   T=T1;
end
T1=T; %T1=T=0 until U>th, then T1=T=U and it keeps the switch to zero(i.e inverter is put to off continously)
```

EM 3,5 and 6 code (control program)

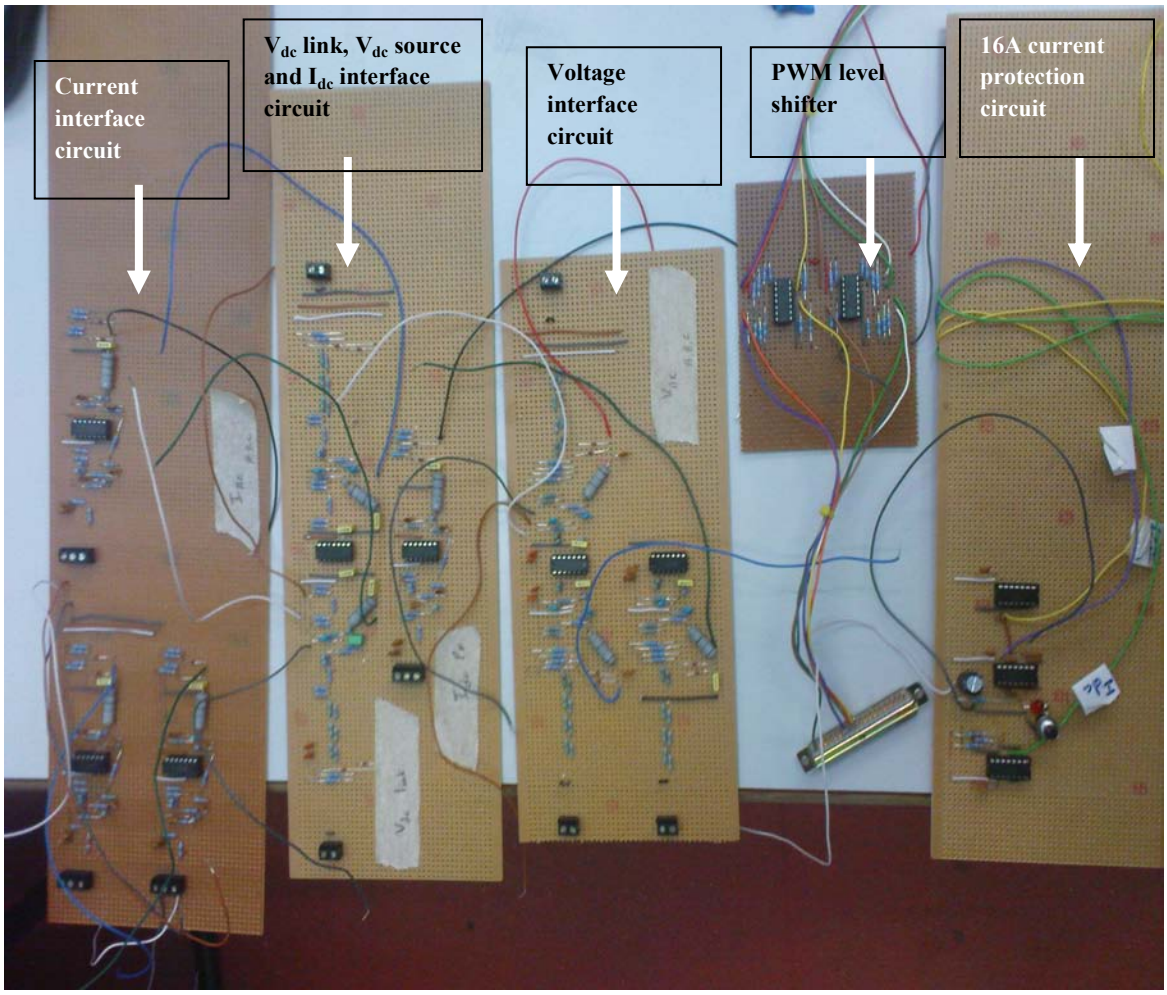
```
function [y,T] = Voltage_protection(u,T1)
% This block supports the Embedded MATLAB subset.
% See the help menu for details.
y=1; T=77.5;
if (u>85.25 || u<69.75)% once threshold reached, upperlimit (+10%), lower limit (-10%), switch is put to zero, 207V to 253V for 230V rms
   y=0;
   T=u;
end
% 14.3V rms to 17.5V rms,
```

```
 if (T1>85.25 || T1<69.75)
    y=0;
    T=T1;
end
T1=T; %T1=T=0 until U>th, then T1=T=U and it keeps the switch to zero(i.e inverter is put to off continously)
```

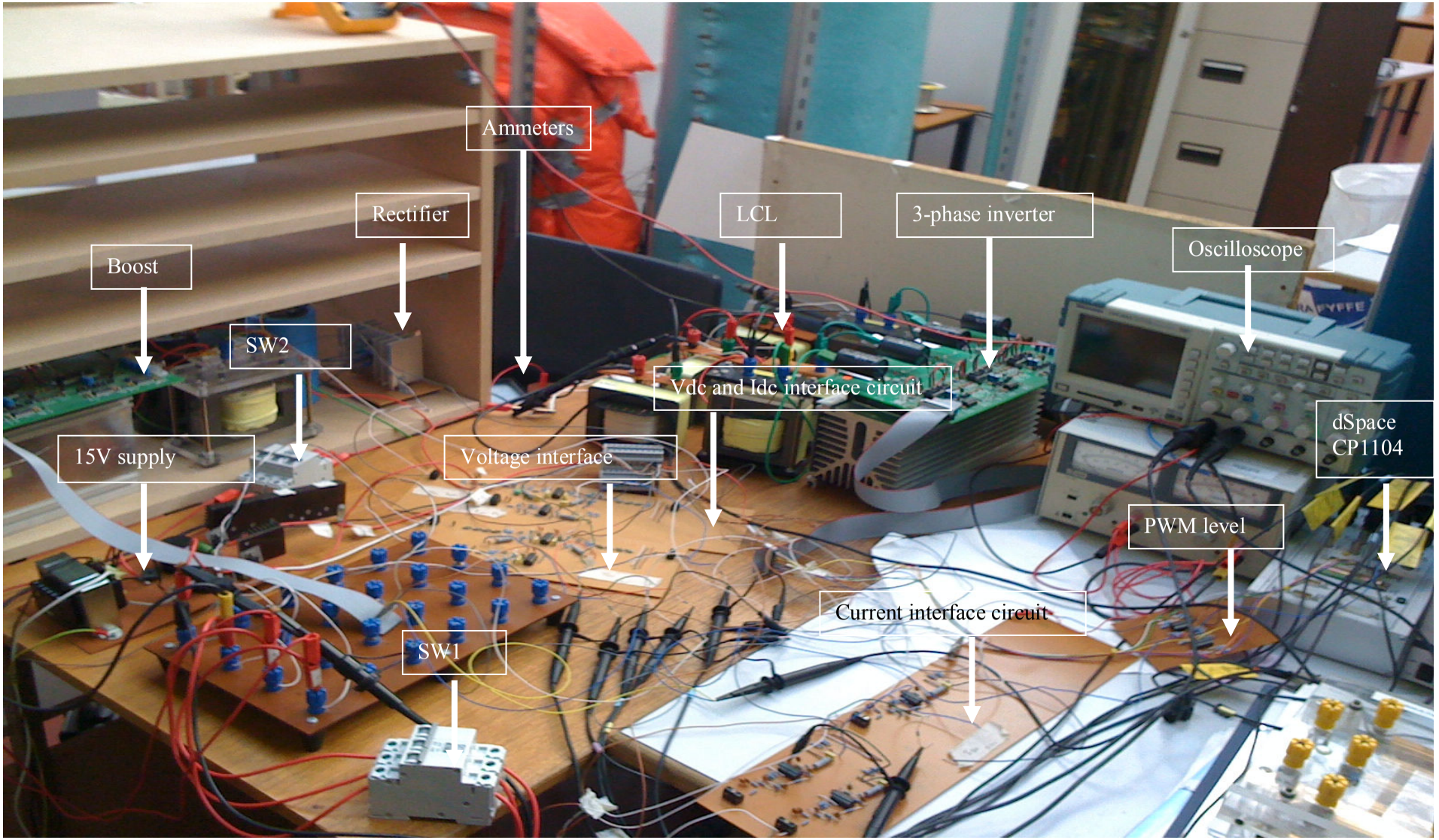
EM4 code(control program)

```
function [y,T] = DC_Link_Voltage_protection(u,T1)
% This block supports the Embedded MATLAB subset.
% See the help menu for details.
y=1; T=300;

if (u>450)% once threshold reached, upperlimit 450V DC, switch is put to zero,
    y=0;
    T=u;
end

if (T1>450)
    y=0;
    T=T1;
end
T1=T; %T1=T=0 until U>th, then T1=T=U and it keeps the switch to zero(i.e inverter is put to off continously)
```

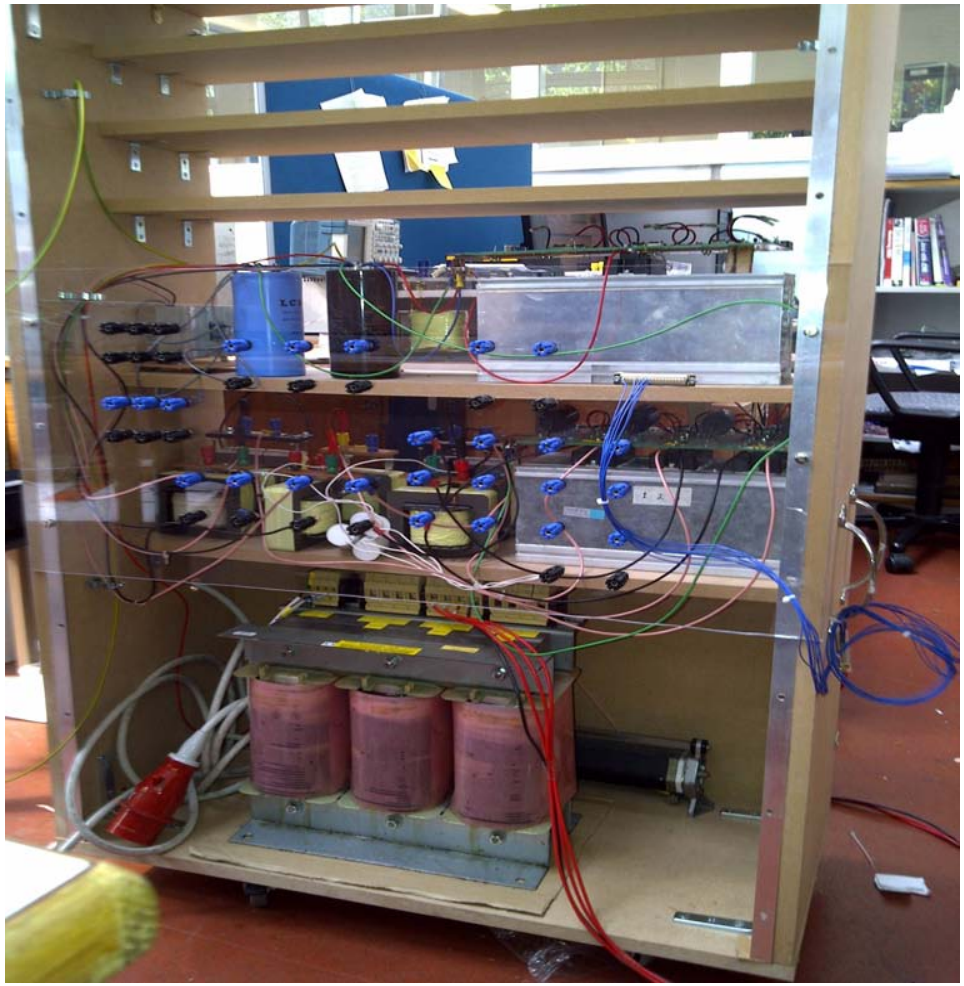
Appendix 6: Hardware



A.6.1:Interface circuits and current protection circuit

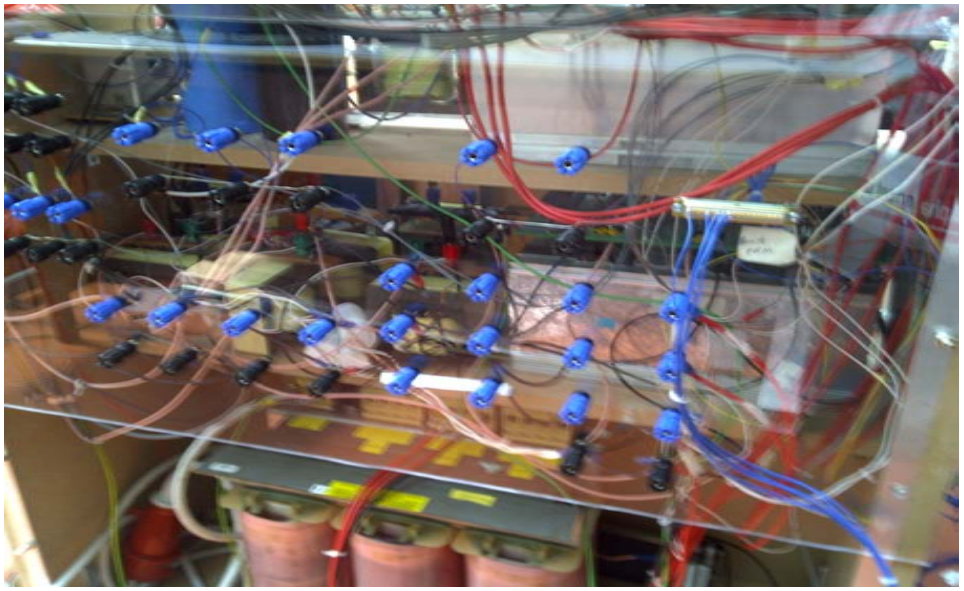


A.6.2: Full hardware system in action (Three phase grid connected inverter system)



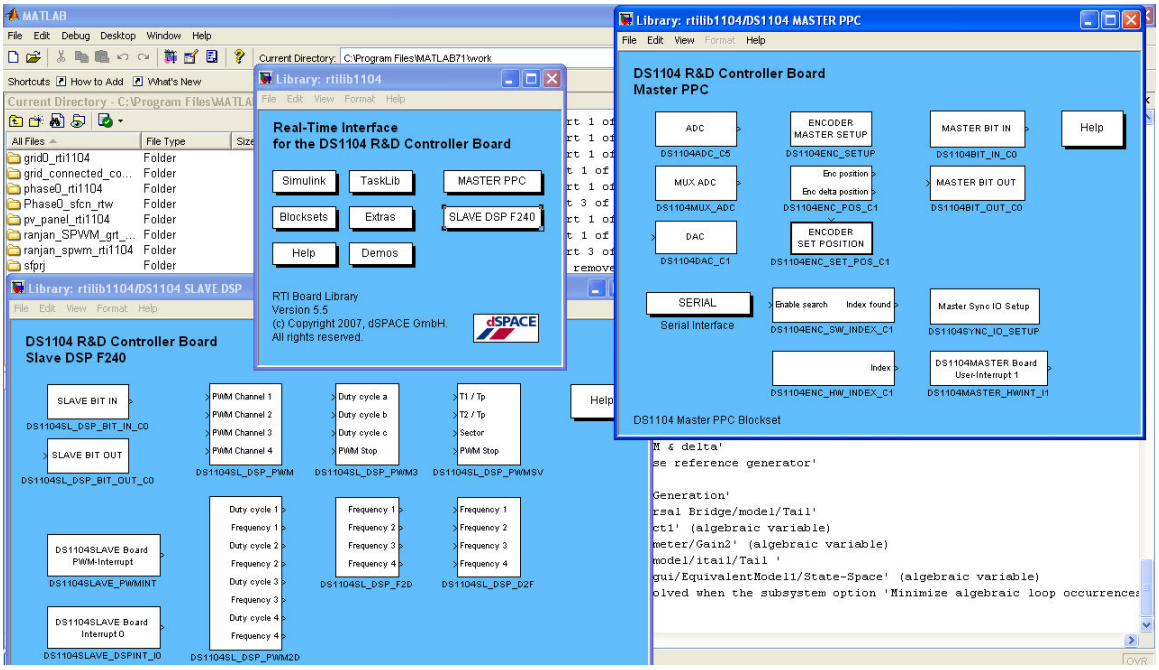
A.6.3 : Cabinet in the making

A.6.4 Front and back of the cabinet

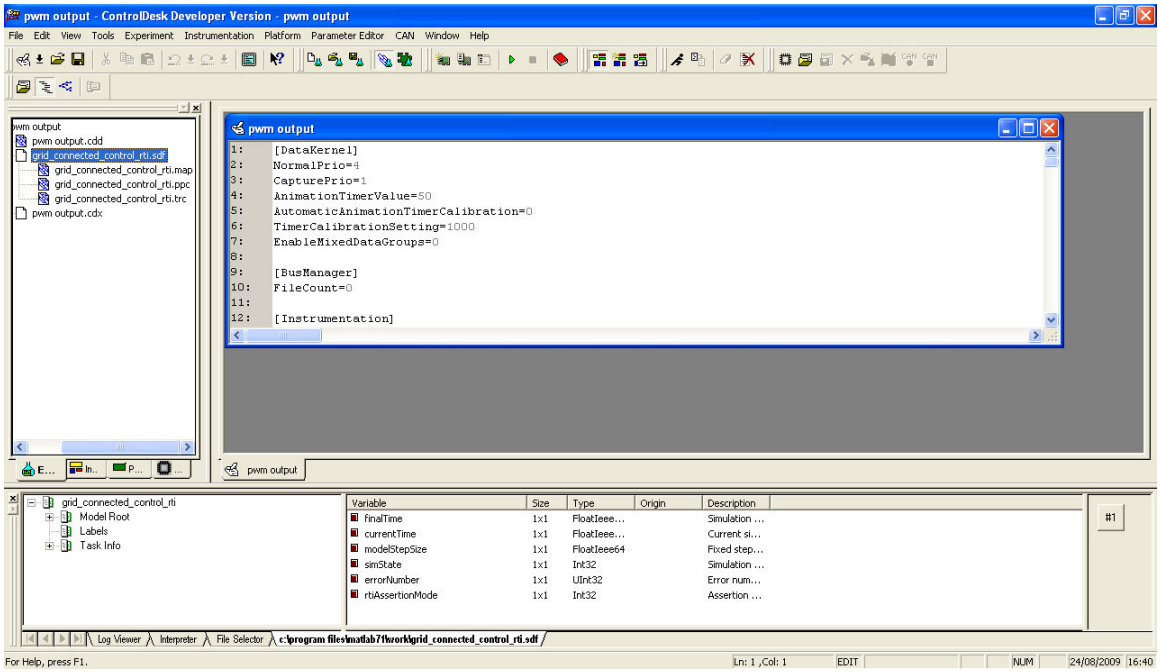


A.6.5 Close view of the cabinet before makings

Appendix 7: dSpace block set and Control Desk



A.7. 1: Screenshot of dSPace library and blocks



A.7. 2: DSP software: Control Desk

Appendix 8: List of publications

Conferences

M. Hanif, M. Basu and K. Gaughan,: **"Novel AC side P&O Maximum Power transfer control for Grid Connected Photovoltaic Systems"**, *International Conference on Renewable Energies and Power Quality (*ICREPQ), 2010 , 23th to 25th March, 2010

M. **Hanif,;** U.D. Dwivedi,; M. Basu,; K. Gaughan,; , "**Wavelet based islanding detection of DC-AC inverter interfaced DG systems**", *Universities Power Engineering Conference (UPEC), 2010 45th International* , vol., no., pp.1-5, Aug. 31 2010-Sept. 3 2010

M. Hanif, M. Basu and K. Gaughan,**: "A Discussion of Anti-islanding Protection Schemes Incorporated in a Inverter Based DG",** *International Conference on Environment and Electrical Engineering (EEEIC) 2011, 10th International,* 8-11 May 2011

Journals

M. Hanif; M.Basu; K.Gaughan; **, "Understanding the operation of a Z-source inverter for photovoltaic application with a design example,"** *Power Electronics, IET* , vol.4, no.3, pp.278-287, March 2011

M. Hanif, M. Basu, K. Gaughan "**Wavelet Based Islanding Detection of Three-Phase DC-AC Inverter Interfaced DG Systems**", ready to be submitted