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Wireless system for the measurement of bioelectric signals using capacitive electrodes

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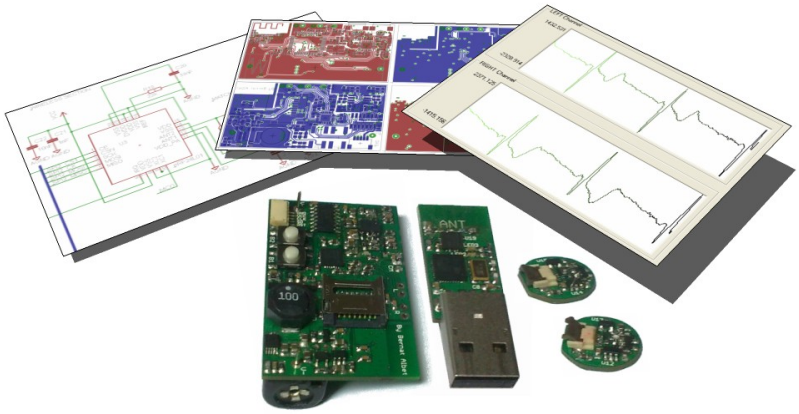

En aquest projecte s'ha volgut arribar fins a l'etapa d'implementació i verificació. En un projecte teòric, els agraïments solen anar destinats a aquells qui aporten ajuda/suport moral, però en aquest projecte també han estat d'especial importància aquelles persones que han fet possible la realització de l'aparell gràcies a una petita inversió. Així doncs, vull agraïr especialment el suport de pares, germana i a la Meritxell.

També a aquella gent que ha cregut en el projecte tot i no conèixer-me, i que ha col·laborat desinteressadament amb donacions a través de la pàgina web.

Finalment, agrair a Starlab la oportunitat i la confiança dipositada pel fet d'haver cregut en la idea.

Contents

1. Introduction

This project turns around capacitive electrodes which measure charge changes at the surface of any conductive surface with enough coupled capacitance, although the specific application is to measure bioelectric signals. The whole wireless system has been designed to fit the desired requirements.

This project would be too extensive if everything had to be explained. That's why neither the firmware nor the software is shown or commented, because there is a lot of code behind this project. Thus, what the code does in general terms is shown, and the details can be reviewed at the source code found at the files attached with the project.

1.1 Basics of bioelectric signals and EEG

From the electronics point of view, the different physiological electrical signals can be classified in function of its frequency and amplitude range, like in the following figure:

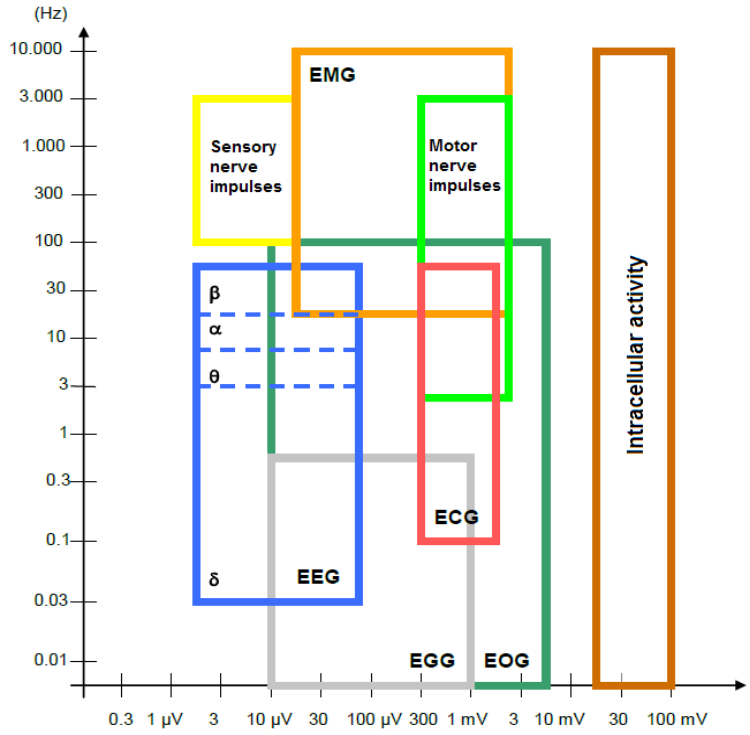

Figure 1. Frequency and amplitude range for several bioelectric signals [1]

In this figure we can observe how the EEG, together with the sensory nerve impulses, has the lower amplitude (about 2μV) of the known bioelectric signals. This is a problem, since most EEG devices are designed to be low noise, and the capacitive electrodes are really noisy. The amplitude of the EEG signal may reach up to 100μV, and the bandwidth of a normal EEG equipment, from about 0.1Hz to 100Hz.

EEG stands for *Electroencephalography*, and it is the procedure in which the signals generated by the firing of the neurons are acquired. It is measured at the scalp, using electrodes.
The EEG is usually split in different frequency bands, since each band represents a different state of mind:

- Delta – Up to 4Hz – Associated with deep sleep
- Theta – From 4Hz to 8Hz – When you are idle; can be related with drowsiness
- Alpha – From 8Hz to 13Hz – Dominant when awake/relaxed. It increases when the eyes are closed.
- Beta – From 13Hz to 30Hz – Focused mental activity
- Gamma – From 30Hz – Short term memory; vision recognition

The signal is usually used for diagnosis. A clear example is the epilepsy, where some spikes appear at the recording, but also to evaluate sleep disorders, brain tumors, long-term memory difficulties, and some others.

1.2 Introduction to biofeedback

The biofeedback is the process in which you become aware of an specific physiological function. This awareness, with some practice, becomes in a higher control of that specific function.
The neurofeedback is a specific type of biofeedback, the one which uses the EEG to feedback the brain information for its own regulation. It may seem weird, but it is nothing but the same learning process we all constantly use, where the feedback comes from our eyes, ears, tact, and so on. Despite this, it is clear you can not be aware of your own brainwaves without a specific device.

Successful studies have been carried out to prove the efficiency of neurofeedback with great results, mainly for ADHD (Attention deficit hyperactivity disorder) [2], ASD (Autism Spectrum Disorders) [3], or just for peak performance training (to be more focused, to increase the resilience to stress, and so on) [4].

There are several protocols [5]. The key of the neurofeedback is about how to process the EEG data to provide certain feedback information (or stimulus). As a matter of example, there is a protocol which tries to promote/inhibit the amplitude of some specific frequency bands in function of a previous comparison with normalized EEG databases.

The stimulus signal can be sound, images, or even functions (e.g. limiting the speed of a car in a simulator when the brainwaves are different than the required pattern).

1.3 Motivation of the project and objectives

Although the system can be used for any bioelectric surface measurement, it was specifically designed to read EEG. The main motivation was the neurofeedback.

Despite this, there are lots of devices to perform electroencephalograms. So, in order to give a more interesting approach to the project, the current problem of the EEG devices was tried to be improved: the electrodes work using conductive gel. With the implemented solution, there is an easy application of the electrodes (with no gel), and that is the reason of the *EasyEEG* name of the designed device.

So, capacitive electrodes were used for that purpose. They already exist, but are less common, there is less information about it, and few companies commercialize them. Furthermore, it was desired to find out the problems related with designing an entire semi-complex system like this, where it is involved analog/digital/PCB/firmware and software design, apart from verification and solving the problems which appear on the way.

Thus, the main goal of this project is to measure EEG for neurofeedback purposes using capacitive electrodes. If this approach doesn't work, and since the motivation is the

neurofeedback, the capacitive electrodes can be replaced by active electrodes and the use of gel without having to change anything else, although it is out of the scope of this project.

1.4 Philosophy of the project

This project was realized under the *open project* concept. It means the most important part of the project, as well as schematics, PCB, and so on, have been published on the web (www.easyeeg.com). As such, there is a donation section, since in hardware design, certain investment is required for the implementation. In this sense it differs from the typical *open source* software projects, where the donations are not really a requirement. In this way, the main idea is to show the information and concepts, and who becomes interested could contribute with the implementation.

Once a stable hardware version was achieved, the idea was to create an *open source* software/firmware project to finish developing the application, since this project may be too much for a single person. That's why the device was designed with lots of features, even if they are not used right now and for this project (like the SD card or the audio implementation).

1.5 Environment

This project was mostly developed by myself at home. Once I had the hardware designed and implemented (the PCBs already soldered), and part of the firmware working, I found *Starlab*, a company related with space and neuroscience.

I showed them what I did, and I started working there in this project (for 4 month). So, at *Starlab* I finished to implement the firmware, the software, and verify that everything was working, as well as solving some problems.

1.6 State of the art

Capacitive electrodes for bioelectric measurements (using a pure capacitance) was first reported in 1968 and patented in 1970. Despite this, the electronics available at such a time made that they needed a capacitance of about 1nF. It was achieved by using exotic materials which caused skin irritation at the patient [6]. In the measure electronics evolved, and new semiconductor techniques were discovered/improved, better approaches could be performed.

Some capacitive electrodes already exist in the market. The best example found is the QUASAR IBE (Insulated BioElectrode), which indeed can measure EEG. This will be the reference electrode to compare the final performance of the designed device, as we will see at its corresponding section.

However, the best method until now continues to be the typical approach of using conductive gel with a common electrochemical electrode (like the Ag/AgCl). The lack of capacitive electrodes at medical devices is in part due to the movement artifacts, which makes this kind of electrodes not enough reliable. Even if the system has some kind of correct-contact monitor, the data acquired while the movement appears is already lost.

Despite this, they offer some great advantages, like long term captures (useful to read the EEG for the entire night while the patient is sleeping), without having gel smearing problems. They are also used in low performance systems, like the heart rate monitors in sport monitoring devices. The advantages and problems are explained at next section.

2. Types of electrodes and comparison

The main characteristics of each type of electrode are summarized at table 1. Here it is justified why the capacitive electrodes were chosen.

	Advantages	Disadvantages
Wet Type	- Close to non-polarisable - Reduced motion artifacts - Common, available "off the shelf"	- Electrolyte required - Gel smearing - Requires time for impedance to drop
Dry Type	- No electrolyte required - Easy construction - Easy application	- Highly polarisable - Requires long time for impedance to drop - Movement artifacts
Capacitive Insulating Type	- No electrolyte required - Easy application - No impedance settling time - No skin preparation - Reusable - Suitable for long term captures	- High input impedance - Static interferences - Movement artifacts - Requires active and local buffers

Table 1: Comparison between different types of electrodes [7]

First of all, a quick explanation about the polarisation of electrodes. They are classified into polarisable or non-polarisable in function of its behavior when a direct current is going through them. At the perfectly polarisable electrodes, no charge passes through the electrode/electrolyte interface when current is applied. The flow is only by displacement current, thus the electrode behaves capacitively. On the other hand, in a perfectly non-polarisable electrode, the current go through the electrode/electrolyte interface thanks to an electrochemical reaction, with no dissipated energy (that is, with zero potential across it).

Wet type:

By far, the silver/silver chloride (Ag/AgCl) is the most common electrode, and it belongs to this group. It just usually shows 0.2 to 5mV of offset. The fact of using gel electrolyte makes this approach useful to reduce motion artifacts, since the gel allows a little movement keeping a good contact.

Despite this, the gel smearing and even absorption is a problem. For patients with sleep problems, or for any other kind of long term monitoring, the use of gel is tedious, since it has to be replaced periodically due to the signal degradation over time. There are systems with automatic dispensation of gel, but they need tubes and a little pump, and it becomes an expensive and a quite sophisticated mechanical solution.
Furthermore, to perform a QEEG (quantitative EEG), where it's common to place 21 electrodes, it is also tedious and time consuming to have to place gel at 21 different places.

Dry type:

Into this group we can find the inert metals, since they are difficult to oxidize and dissolve. Platinum or gold are two quite used materials. They offer a faster skin implementation, but you need direct contact with the skin anyway. In this sense, there can't be hair between the scalp and the electrode, and unless you are bald or you just use gel, you can't use these electrodes to measure EEG.

This type of electrodes are also capacitive, but since there is a direct contact with the skin, the capacitance is much higher than in the capacitive insulating electrodes.

Capacitive insulating type:

This type of electrodes seems the best in terms of advantages. But they also offer the worst disadvantages... The static interferences and movement artifacts are the major problems.

The charge movement detected by this kind of electrodes is produced by means of capacitance, coupled between the skin and the electrode. This capacitance is purely dependent on the area, the distance and the permittivity of the material found between the scalp and the electrode. A lot of variables. If a tiny movement is done, the distance changes, and so the voltage does. This problem is not a big deal when the electrode is touching the skin, since the distance is always close to zero. The problem appears when there is hair in between, which is the usual case in an EEG device. In this case, a movement not only changes that distance, but also the movement itself generates triboelectric effects, which in fact are charge movements, and so, undesired noise.

The main difference with the dry electrodes is that the capacitance is better controlled in this type by means of a non-conductive dielectric separator. Although being better controlled, the main problem is that this dielectric reduces a lot the capacitance, and so, the electrodes must be active. Otherwise, the capacitance of the cable itself and the interferences would make impossible to read any signal.

3. The capacitive electrode

As we saw at Table 1, a capacitive electrode must be active, to buffer the signal and avoid picking up some external noise. So, the component which requires more attention is the operational amplifier. Unfortunately, the op amp topology we use has several implications over its non-ideal characteristics, each one with its own pros and cons.

First, the most important characteristics we need will be reviewed.

3.1 Requirements for the operational amplifier

- ***High DC input impedance***

It has a higher impact in the non-inverter topology, and it will be better explained there. Just to say that the common problem in both topologies is a side effect: the op amps with low DC input impedance usually have higher input bias currents.

- ***Low input bias current***

There are two main problems due to the bias current:

1. We have to add an extra current path to give a working point to the op amp. Otherwise it would saturate, since the bias current is almost constant, and it shows an integrating voltage effect when the load is capacitive.
2. Higher input bias currents means higher current noise (intrinsic op amp noise, as well as shot noise due to the extra path to give the working point).

The first point is always required to avoid the saturation (with exception of some amplifiers, which tend to go to 0V by themselves, like the INA116 [8]).

About the second point, it is the intrinsic op amp current noise, and there is nothing we can do to reduce it. Furthermore, the extra current path will add noise when the bias current of the op amp go through it (shot noise).

So, it is clear the lower the input bias current the better, from a noise point of view.

- ***Low input current noise***

We already have seen we need a very high input impedance to be able to measure any signal. But in fact, it is a huge problem as far as input current noise is concerned: the higher the input impedance, the higher the noise. There are some tables where it is shown the total output voltage noise in function of input impedance, and usually the total output voltage noise contribution is the higher one due to the input current noise when the input impedance is higher than about 100KΩ – 1MΩ.

So, in our case, the input DC impedance is huge. When dealing with CMOS op amps, it may reach to be as high as 10^{13} Ω. Under this situation, the AC impedance (the input capacitance) is the unique element which attenuates the current noise.
In this way, it is the most important requirement for the op amp. The noise can be reduced by increasing the input capacitance, but it would mean having to increase the electrode size to keep the same gain.

The voltage noise will always be lower almost for sure, and so it won't be a problem at all.

There is another huge problem related with current noise density: just few datasheets show the current noise density over frequency, they just show this noise density at a single frequency (usually 1kHz or 10kHz). But this information is not enough to deduce where the 1/f corner frequency starts. It is important because the current noise density, as well as the voltage noise density, has a 1/f corner frequency, where it starts to increase. Thus, since we want to measure EEG signals where its low frequency content is found into that 1/f noise bandwidth, we need to reduce the 1/f current noise as much as we can.

This lack of information limits a lot the noise analysis, since we can only choose the operational amplifier in function of the lowest noise at that single frequency, although it doesn't mean to be the best... As an example: an op amp with 1fA/√Hz at 1kHz with a corner frequency at 100Hz would be better than let's say 0.8fA/√Hz at 1kHz with a corner frequency at 1kHz, since the total integrated noise under the area between 1Hz and 30Hz (the desired EEG content) would be lower for the first case.

- ***Low voltage supply***

This is another great restriction for the op amp selection. Being a portable system, the electrodes of this project are being supplied at a low voltage and single supply. JFET technology offers very good features, but usually higher voltages are required, like ±15V. For lower voltages, the JFET characteristics becomes worst than CMOS ones. So, the best approach is the CMOS technology. The bipolar technology is directly discarded due to the high input bias current and high input current noise density.

A second problem related with the low voltage op amps is the input voltage range. When a non rail-to-rail input op amp is used, the input range should be from Gnd – 0.3V to Vcc-1V, or from Gnd+1V to Vcc+0.3 (these are common values, and may vary in function of the device). The kind of range will vary depending on the input stage (if they use PMOS or NMOS).
To solve this problem and get a rail-to-rail input op amp, 2 differential CMOS input stages are used in parallel. It means there is a transition point where one transistor starts to conduct and the other stops. In such a situation, the performance of the operational amplifier is affected, mainly due to strange transitions with the input offset voltage in function of the input common mode voltage. Since we want to measure an EEG signal with an amplitude much lower than the possible coupled 50Hz of the mains, this 50Hz signal could appear with harmonics at the output of the op amp. It would mean that a notch filter at 50Hz would not be enough to filter the noise of the mains. In our case it won't be a problem, since we want to measure up to 30Hz, and the harmonics would appear over the 50Hz, but there are research groups who study EEG frequencies up to 100Hz.

3.2 Operational amplifier topology

In this section, the most important features, pros and cons for each topology will be reviewed.

3.2.1 Non-inverter

A simplified schematic of the non-inverter topology is shown at the next figure:

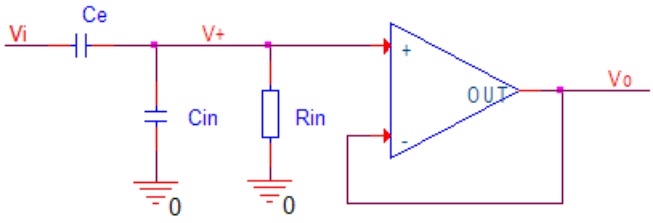

Figure 2. Schematic of the non-inverter op amp

The main feature is that the output voltage is in phase with the input voltage. But what makes a big difference between both topologies is that in the non-inverter the voltage at V+ and V- nodes changes, while in the non inverter they are constant.

The first consequence of having a non constant voltage at the input pins is the input DC impedance (the real part of the usually called *common mode input impedance*). We want to measure low frequencies through a tiny capacitance. If that DC impedance is not high enough then it would appear a high pass filter which could filter EEG data. If the coupled capacitance, C_e, were of 10pF (the best case is about 22pF), and supposing we want a worst case high pass filter of 1Hz, then:

$$R_{input} > \frac{1}{2 \cdot \pi \cdot 1\text{Hz} \cdot 10\text{pF}} = 159\text{M}\Omega$$

Eq 1. Minimum required input impedance

That coupled capacitance may change, and so, it would be like having a variable frequency high pass filter in function of the capacitance. Despite this, it is easy to find op amps with higher DC impedance than 160MΩ.

This is just DC impedance. But operational amplifiers also has an input capacitance (translated into an AC impedance). So, the second problem about using this topology is that the input capacitance is acting as a capacitive voltage divider, and so, attenuating the input voltage.

$$Vo = V+ = Vi \cdot \frac{C_e}{C_e + C_{\text{in}}}$$

Eq 2. Capacitance voltage divider

There would be no problem if C_e was much higher than C_{in}, but in a pure (isolated) capacitive electrode that's not true at all. With a C_e of about 22pF and C_{in} of 8pF (common values), the attenuation ratio is of 0,73.

The third issue is about the noise. With this topology, the current noise is decreased thanks to the input capacitance and the electrode capacitance. It means that the noise is dependent on the coupled capacitance, which is not critical but makes more difficult to foresee the response.

Finally, the fourth problem was about the voltage range. Two solutions could be used:

- Imagine the supply ranges from Gnd to 2.5V. With a non rail-to-rail input op amp, the input common mode voltage would allow a maximum of about 2.5V-1V=1.5V, and so, the input common mode voltage could range from Gnd to 1.5V. In this way, the working point could be set at 1.5/2=0.75V.
- Using a rail-to-rail op amp, having into account that a “high” amplitude interference (such as the mains) may add harmonics to the signal. Despite this, the offset change in function of the input common mode voltage changes from op amp to op amp, and one which reduce this effect could be chosen.

About the input impedance seen by the skin:

$$Z_{in} = \frac{1}{Ce \cdot s} + \frac{R_{in}}{R_{in} \cdot C_{in} \cdot s + 1}$$

Eq 3. Impedance seen by the skin in a non-inverter op amp

3.2.1.1 Adding bootstrapping techniques

One of the problems we have seen in this topology is the input capacitance attenuation, due to the capacitive voltage divider. To reduce C_{IN} and so, to increase the input impedance, a bootstrapping technique may be used [9]. An example is shown here:

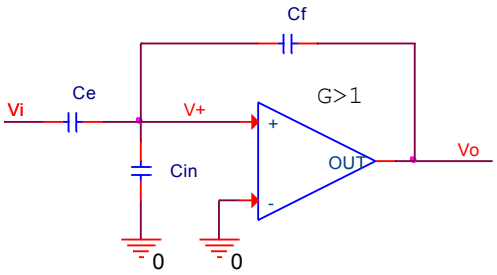

Figure 3. Schematic of the non-inverter amplifier with bootstrapping

In this case an amplifier with a gain higher than 1 (e.g. a non inverter op amp) must be used instead of a unity gain buffer. The function of C_f is to compensate the input capacitance C_{IN}. The higher the gain, the lower the feedback capacitance should be. Since the input capacitance usually varies from amplifier to amplifier, some kind of trimming is needed.

With this setup, the impedance in module (that is, real and imaginary parts) is really high. To show this, we can use the equation 3. If C_{IN} could (theoretically) be totally compensated, then it would be 0, and so the new impedance would be:

$$Z_{in} = \frac{1}{Ce \cdot s} + R_{in}$$

Eq 4. Impedance seen by the skin in a non-inverter + perfect bootstrapping

This means that whatever the frequency is, the input impedance would always be at least as high as R_{IN}, and as already seen, can reach to be as high as 10^{13} Ω in CMOS or some JFET op amps.

The problem about using the bootstrapping is that the noise is higher, since part of the output is fed into the input node. Despite this, thanks to that huge impedance, it allows you to read voltages with just few coupled capacitance, since C_{IN} is not attenuating that voltage anymore.

3.2.2 Inverter

In this configuration, all the input nodes have a fixed voltage. The schematic is shown here:

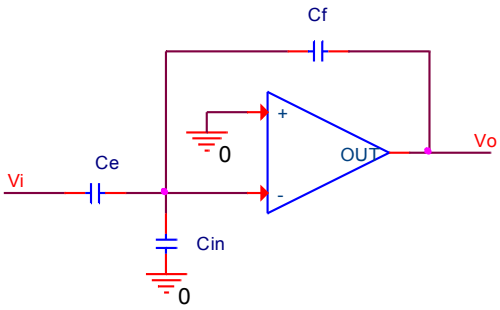

Figure 4. Schematic of the inverter op amp (charge detector)

This configuration is also called a charge detector, or charge amplifier if C_e is higher than C_f. The key of using this configuration is that the input pins V+ and V- are fixed at a given voltage. It means that given a C_e, it will attenuate less the V_i signal than using a non-inverter (without bootstrapping). Furthermore, the input common mode voltage will always be into a correct voltage range (set by design); of course, when the op amp is not saturated.

About the impedance seen by the skin, it is given by the coupled capacitance:

$$Z_{in} = \frac{1}{Ce \cdot s}$$

Eq 5. Impedance seen by the skin in an inverter op amp

3.2.3 Final selection

Each configuration has pros and cons. The discussion is between a non-inverter + bootstrapping or the inverter one. The non-inverter without bootstrapping is already discarded, because of the higher attenuation.

At first seen, it seems that the bootstrapping technique is the best, since the input impedance is the highest one. One problem is the low voltage supply, which brings us to a little input working range. Another one, the complexity of having to add some kind of trimming, which will increase the electrode board size.

On the other hand, the attenuation of the signal in an inverter is ideally not affected by the input capacitance of pin V-, or even PCB stray capacitances (which can be modeled by a C_{stray} capacitance in parallel with C_{in}). It can work within a fixed input voltage (so we don't have rail problems), and no adjustment is required in function of the input capacitance (unlike in the bootstrapping solution).

Furthermore, using the inverter topology, the noise is almost constant and varies just a little with the input capacitance (unlike what happens in a non-inverter). Despite this, the SNR is always worst in both cases when the coupled capacitance decreases:

- In the inverter case, when the coupled capacitance is lower, the gain is lower, but the noise is the same. It means the SNR decreases.
- In the (ideal) non-inverter with bootstrapping case, a lower coupled capacitance doesn't change the gain, but it increases the output noise because the current noise is seeing a higher impedance (a lower capacitive load). So, the SNR also decreases.

So, as a first approach, it seems the simplest solution, which is good to get a tiny electrode, is the inverter one.

3.3 Electrode model

3.3.1 Input impedance and gain

The input impedance was seen at Eq 5. So, we will have the lowest impedance (worst case) when we have the maximum input capacitance and the highest EEG frequency (about 30Hz). So, the minimum impedance at such a situation will be of:

$$Z_{\text{in}} = \frac{1}{Ce \cdot s} = \frac{1}{22\text{pF} \cdot 2 \cdot \pi \cdot 30\text{Hz}} = 241\text{M}\Omega$$

Eq 6. Minimum impedance seen by the skin

About the gain, it depends on the ratio between C_e and C_f, like shown at Eq 7:

$$G = \frac{C_e}{Cf}$$

Eq 7. Gain of the electrode

In fact, having a variable gain in function of the coupled capacitance is a problem. That is why it was decided to add a feature to detect the gain. It will be deeper explained later,but summarizing, a common mode signal of a known frequency and amplitude is added, and measuring back its amplitude through the electrodes. The ratio between the measured amplitude and the known one will be the gain of the electrode.

3.3.2 Noise

To make the noise analysis, the following model will be used:

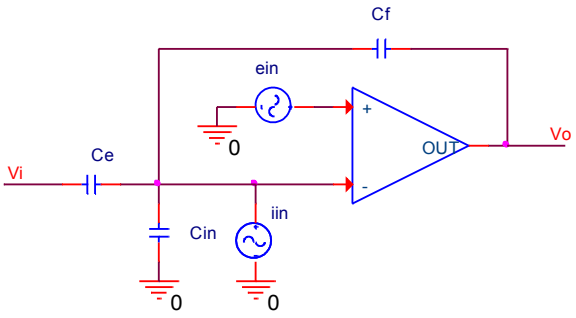

Figure 5. Schematic of the op amp noise model

The current noise source at the positive input pin of the op amp was not drawn because its path has low impedance. There is also a resistive element in parallel to C_f, but was not drawn either because it is higher than Z_{cf} into the range of interest.

In this analysis, it is supposed that the op amp has an infinite open loop gain. V_i is connected to ground to know the total output voltage when there is no input signal (the noise). In this way, the electrode capacitance C_e will be in parallel with the input capacitance C_{in}.

To calculate the total output noise, the superposition principle is used. Thus, the independent results are quadratically added, having into account the addition of independent noise sources. In this way, to measure the partial output voltage noise due to the voltage noise source e_{in}, the current noise source i_{in} is supposed to be noiseless (replacing it by an open circuit); and to measure the output voltage noise due to the current source i_{in}, the voltage noise is the one which is supposed to be noiseless (replacing it by a short).

Therefore, the output noise will be:

$$\overline{E_{vn}^2} = \int \left(e_{\text{in}} \cdot \left(1 + \frac{C_e + C_i}{C_f} \right) \right)^2 df$$

$$\overline{E_{\text{in}}^2} = \int \left(i_{\text{in}} \cdot \frac{1}{C_f \cdot 2 \cdot \pi \cdot f} \right)^2 df$$

$$E_{rms} = \sqrt{\overline{E_{\text{vn}}^2} + \overline{E_{\text{in}}^2}} = \sqrt{\int \left(e_{\text{in}}^2 \cdot \left(1 + \frac{C_e + C_i}{C_f} \right)^2 + i_{\text{in}}^2 \cdot \left(\frac{1}{C_f \cdot 2 \cdot \pi \cdot f} \right)^2 \right) df}$$

Eq 8. Development to reach the final output voltage noise Eq 9

$$E_{rms} = \sqrt{e_w^2 \cdot \left(f_{enc} \cdot \ln\left(\frac{f_H}{f_L} \right) + F_H - F_L \right) \cdot \left(1 + \frac{C_e + C_i}{C_f} \right)^2 + i_w^2 \cdot \left(\frac{\ln\left(\frac{F_H}{F_L} \right)}{2 \cdot \pi \cdot C_f} \right)^2 \cdot \left(f_{inc} \cdot \ln\left(\frac{f_H}{f_L} \right) + F_H - F_L \right)}$$

Eq 9. Output noise due to voltage and current noise sources [10]

In the previous equation 9, e_w is the white noise voltage in V/√Hz, f_{enc} is the voltage noise 1/f corner frequency, f_L and f_H, the lower and the higher frequency of the bandwidth (from 1Hz to 30Hz), i_w is the white current noise in A/√Hz, and f_{inc} is the current 1/f corner frequency.

To reach the equation 9, the frequency in the equation 8 was integrated from f_L to f_H. In the case of the voltage noise, the gain formed by C_e, C_i and C_f doesn't depend on the frequency (since they form a capacitance voltage divider), but in the current noise something different happens. Even if i_{in} was constant over frequency (without 1/f noise), the output voltage noise wouldn't be constant, since the impedance of a capacitor decreases in frequency, and so, the output noise also decreases.

In this way, we would like to have a C_f as high as possible to decrease the noise, but then, we should increase the coupled electrode capacitance to keep the unity gain (the gain is 1 when C_e and C_f are equal). In other words, the lower the total output voltage noise due to the input current noise, the higher the electrode size must be to keep the same gain.

Let's give some numbers to know the amount of total noise we expect from this analysis. To calculate this, some common values from generic low noise CMOS op amps will be used:

- Input voltage noise density: 23 nV/√Hz (flat band)
- 1/f corner frequency: 1kHz
- Input current noise density: 0.6 fA/√Hz (at 1kHz)
- Current noise corner frequency: 1kHz

$$E_{rms} = \sqrt{23\text{nV}^2 \cdot \left(1\text{KHz} \cdot \ln\left(\frac{30\text{Hz}}{1\text{Hz}}\right) + 30\text{Hz} - 1\text{Hz}\right) \cdot \left(1 + \frac{22\text{pF} + 10\text{pF}}{22\text{pF}}\right)^2 + \\ + 0.6\text{fA}^2 \cdot \left(\frac{\ln\left(\frac{30\text{Hz}}{1\text{Hz}}\right)}{2 \cdot \pi \cdot 22\text{pF}}\right)^2 \cdot \left(1\text{KHz} \cdot \ln\left(\frac{30\text{Hz}}{1\text{Hz}}\right) + 30\text{Hz} - 1\text{Hz}\right)}$$

$$E_{rms} = \sqrt{1.09 \cdot 10^{-11} + 7.48 \cdot 10^{-7}} = 865\,\mu\,\text{V}_{\text{RMS}}$$

Eq 10. Output noise due to voltage and current noise sources

Here we can appreciate the problem: the highest noise comes from the input current noise rather than the input voltage noise (in 2 to 3 orders of magnitude). And the added problem: the total output voltage noise depends a lot on the current noise corner frequency, which is unknown in most op amps (the manufacturer doesn't usually give that parameter).

Three examples are shown here:

- Corner frequency: 10Hz → Total output noise voltage: 117 μV_{RMS}
- Corner frequency: 100Hz → Total output noise voltage: 284 μV_{RMS}
- Corner frequency: 1kHz → Total output noise voltage: 865 μV_{RMS}

On the other hand, if we repeat the calculations considering to have no input current noise, the total output voltage noise is of just 3 μV_{RMS}. It is approximately what it is expected, since at the datasheet it is said that the peak-to-peak voltage noise from 0.1 to 10Hz is of 6.1μV_{PP} (about 1.5μV_{RMS} if we consider 2σ → probability of the signal to be into the 6.1μV_{PP} of 95.4%).

In other words, without the proper information about the input current noise, it is really difficult to figure out the total amount of output voltage noise. In fact, when we measure the total output voltage noise over the real capacitive electrode, we will see that the total amount of noise is much lower even than the best case of 117 μV_{RMS}.

When the inverter op amp topology was reviewed, it was seen that the total output voltage noise just depends a bit on the coupled electrode capacitance. It is what we saw: a change in C_e capacitance means a little increase in the output voltage noise due to input noise; but since the highest noise is due to the input current noise, and that one is not affected by C_e, it is a good approximation to say that the output voltage is kept almost constant regardless of C_e.

4. Design of the whole system

In this section, all the parts of the system will be explained, arguing the reason of each choice.

4.1 Electrodes

4.1.1 Introduction

Since this electrode is an insulated one, there is no electrical contact from the electrical surface of the electrode and the skin. Thus, a plastic with a thickness of 0.1mm was used to insulate it.

The maximum capacitance should be known to have an idea about the range we are dealing with. This capacitance can't be calculated if we don't know the permittivity of the dielectric used as insulator. That's why it has to be measured.

To do so, this setup will be used:

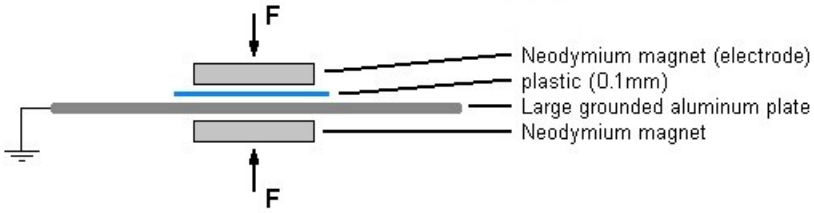

Figure 6. Setup where the capacitance will be measured

Neodymium magnets have been used, which are coated with nickel to protect the magnet from corrosion. Fortunately, nickel has a resistivity as low as 69.3 nΩ·m, a great conductor, and so, the top magnet will simulate the electrode. This magnet was placed over a large aluminum plate, and between both, it was placed the thin 0.1mm plastic film.

On the other side of the large aluminum plate, another magnet was placed to keep the electrode pressed against this plate. Then, the aluminum plate is grounded, and the capacitance between the top magnet and the plate is measured. See the next figure:

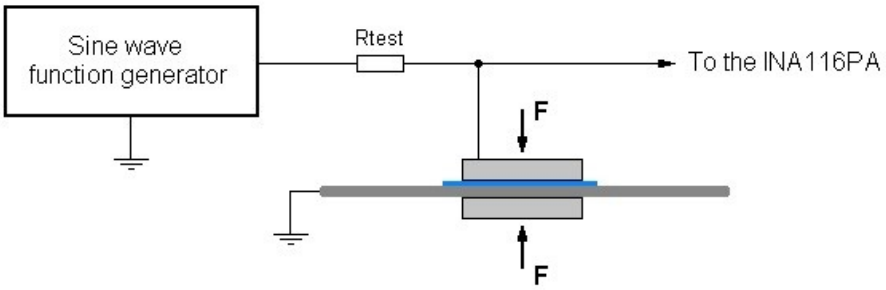

Figure 7. Assembled setup with the measurement system

In figure 7 the whole setup is shown. To measure the capacitance, *Rtest* is used, and the frequency is changed until the attenuation due to the *Rtest·C* is -3dB the amplitude of the sine wave generator. This attenuation is read thanks to an INA116PA, an instrumentation amplifier. The model is shown here:

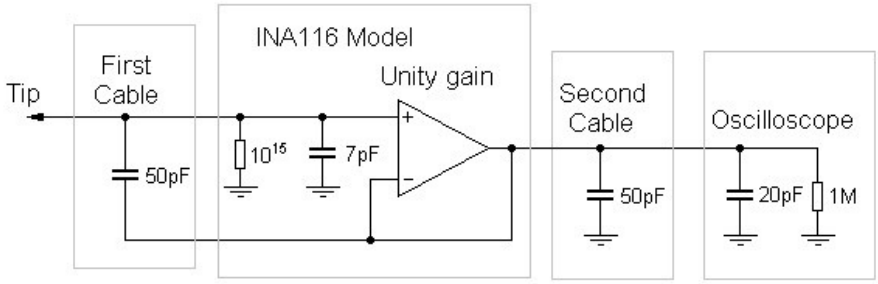

Figure 8. Model of the measurement system + oscilloscope probe cables

The *First Cable* and the *Second Cable* are oscilloscope probes. Since we want a few input capacitance to be able to measure the tiny electrode capacitance, and each probe has about 50pF (1.2 meters, HP2060), an active probe system is used. The pins surrounding both the V+ and the V- pins of the INA116 are low impedance unity gain buffers, usually used to avoid leakage currents when high impedance is required (they act as ring guards). So, connecting the ground of the probe to that pin (like shown in the model schematic of the figure 8), the

effective capacitance of the probe is decreased a lot. Furthermore, the INA116 has a unity gain stability for capacitive loads of up to 1nF, and so, it's not a problem to directly drive the second cable probe plus the input capacitance of the oscilloscope.

Now we should measure the total input capacitance, to make a real model of our measurement system. To do so, the following setup was used:

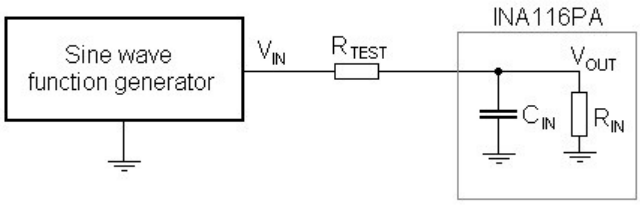

Figure 9. Test of the input capacitance of the INA116 setup

R_{IN} is supposed to be infinite, since it is of about $10^{15}\Omega$ (according to the datasheet). So, C_{IN} is easy to find out. We will use an R_{TEST} of 2.22MΩ. Monitoring the output of the sine wave function generator with a two channel oscilloscope, and using the second channel to watch the output of the INA116, we have to find the frequency for which the output of the INA116 is -3dB the amplitude of the output of the function generator.

Then we can apply the next formula:

$$C_{IN} = \frac{1}{2 \cdot \pi \cdot f \cdot R_{TEST}} = \frac{1}{2 \cdot \pi \cdot 16\text{KHz} \cdot 2.22\text{M}\Omega} = 4.48\text{pF}$$

Eq 11. Calculation of C_{IN}

So, when we use the measurement system to know the capacitance of the electrode (C_e), the input capacitance of the measurement system (C_{IN}=4.48 pF) will be in parallel with this capacitance to be measured. In this way, the electrode capacitance, which is the one we want to know, can be found using:

$$F_{CUTOFF} = \frac{1}{2 \cdot \pi \cdot R_{TEST} \cdot (C_e + C_{IN})} \quad \rightarrow \quad C_e = \frac{1}{2 \cdot \pi \cdot F_{CUTOFF} \cdot R_{TEST}} - C_{IN}$$

Eq 12. Calculation of C_{TEST}

Apart from applying pressure, 5 rounded magnets with different diameters were used, with the main goal of calculating the capacitance in function of the magnet (electrode) area:

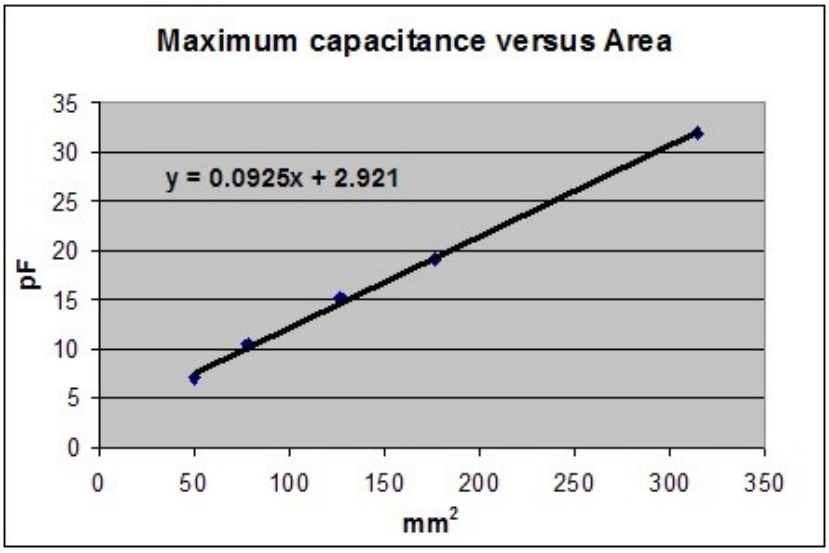

Figure 10. Capacitance vs area

The final version of the electrode has a diameter of about 15mm. It means an area of 177mm^2, and according to the equation, a capacitance of almost 20pF. In this way, a feedback capacitance for the inverter op amp of about 22pF will be used, to ensure a gain of 1 when the maximum capacitance is achieved (although this condition hardly ever happens).

Thus, another interesting test is to know how this capacitance varies in function of different conditions, mainly due to the hair. For this new test, a 20mm diameter electrode was used, and it was placed on a headphone to avoid any movement. Then, the headphone was placed over the head, and the body was acting as the grounded metal plate of figure 7, repeating the operations to measure C_{TEST} at equation 12. To avoid any electric shock risk, the sound card of the laptop was used and the laptop was operated with batteries, as well as the oscilloscope, which is a digital/portable one.

Condition	R_{TEST} [Ω]	Cutoff Frequency [Hz]	Measured capacitance [pF]
With the maximum amount of hair as possible	1.52M	9000	7,15
Placing the headphone normally	742K	13500	11,41
Trying to keep the maximum amount of hair out	742K	11000	15,02
The same, but pressing the electrode onto the head	742K	7500	24,12

Table 2: Table to show the coupled capacitances in different situations

This test was done with a 20mm diameter electrode, what means a maximum ideal case of 24pF. In this case, 24pF has been measured as a maximum value. It is the 75% of the maximum capacitance. Furthermore, when we place the headphone normally, we can see a 36% of the maximum capacitance. These are not good news, since it means that the SNR of the ADC will be quite worse when the headphone is placed normally, because the gain will be lower than 1.

4.1.2 Schematic

Before the current implementation, another interesting approach was tried. The previous design schematic can be seen at figure 11.

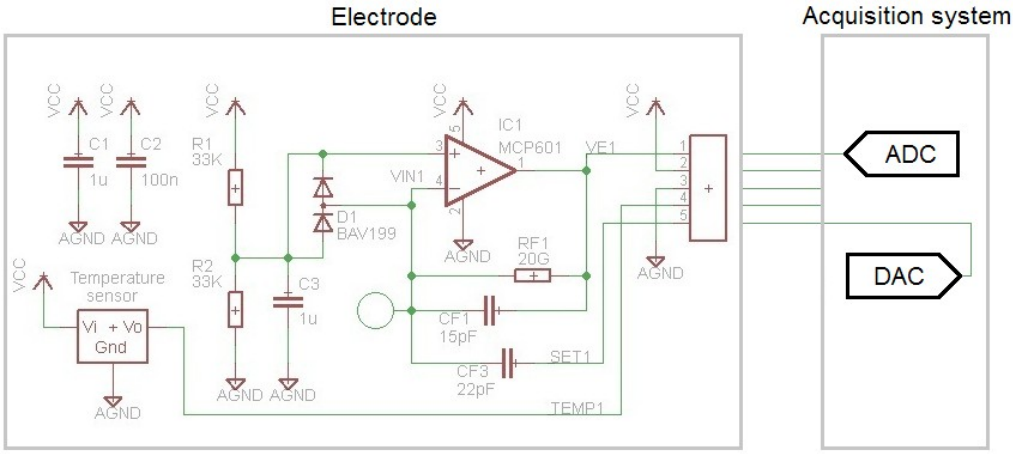

Figure 11. Initial schematic design for the electrodes

It used a very large and expensive resistor of 20G, which was used to provide a bias current path to the operational amplifier, and it would form a high pass filter together with CF1. According to this approach, and giving it enough time, the output of the op amp should reach to Vcc/2. But since the time constant of the RF1·CF1 is quite high, a fast setting feature was implemented. To do so, a third capacitor (CF3) was added, which is connected to the inverter pin of the op amp on one side, and to a DAC (a Digital to Analog Converter) on the other side. This DAC is placed at the main board. So, in normal conditions, CF3 would do nothing, since the SET1 node would be at a fixed voltage, and so, CF3 could be simplified by placing it in parallel with the input capacitance of the op amp.

The idea was that when a movement artifact made the op amp to be in saturation (or in other words, that the inverter pin became different than Vcc/2), the DAC could add or remove just the amount of charge removed or added by the movement artifact, through the capacitor CF3.

Despite this, the thermal noise of that resistor was too high, and so the output voltage had a lot of noise. As it will be seen at the 4.2.2.6 section (Input stage), there will be more repercussions.

To solve the noise problem, the resistor was replaced by two back-to-back diodes, which offer a really high DC impedance when the voltage across them is small (see figure 12):

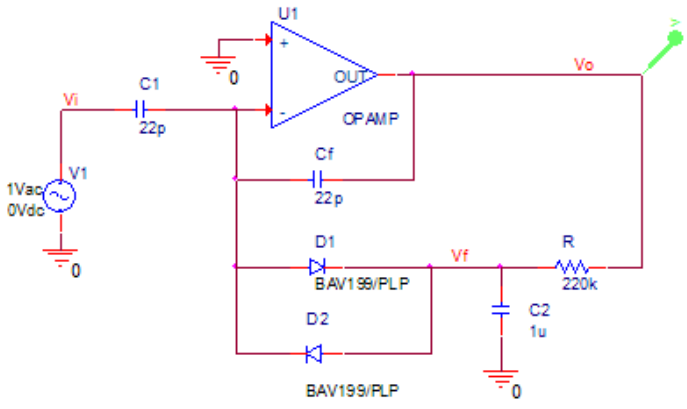

Figure 12. Current design: improvement to reduce the resistor noise

These diodes just need the necessary forward voltage to compensate the bias currents of the op amp.

With this new approach, the fast setting voltage feature is no longer required, since the op amp can never be saturated. It is because of the exponential current characteristics of the diodes: the higher the output voltage versus the V- voltage pin (that is, V_f), much larger the current will be.

Instead of connecting the V+ pin of the operational amplifier at ground, it is connected to Vcc/2 through two resistors of the same value (a voltage divider). The ground was used just because it is easier to develop the circuit analysis.

The function of *R* and *C2* is to bootstrap the capacitance of the diodes above the $2 \cdot \pi \cdot R \cdot C2$ frequency (that is, about 1Hz). If the *Vf* node was directly connected to *Vo*, the diodes would be in parallel with Cf, and it could be a problem, since the capacitance of the diodes change with the forward voltage, and it would even be a much more difficult circuit to analyze.

At section 3.3 (Electrode model) this circuit was analyzed without the diode. Now the results are simulated using PSpice, since it uses a very accurate model for the diode. Here is shown the result of an AC sweep:

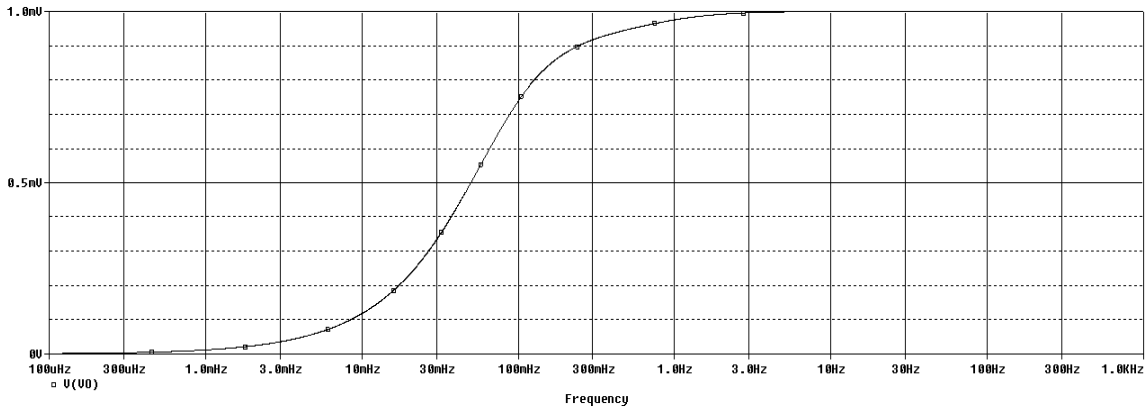

Figure 13. PSpice simulation of the non-linear system response

4.1.3 PCB design

One of the keys of using the inverter topology is that the stray capacitances found at the negative node have no influence in the electrode gain. In this way, all the entire internal bottom layer is connected to a low impedance source (to Vcc/2), and it is used as a screen against external interferences. This copper layer increases the capacitance of the op amp negative input, but as already said, it doesn't attenuate the signal.

Three layers would be enough to screen the electrode copper layer, but the manufacturer only offers 2 or 4 layers, so we must jump to 4. These 4 different layers of the PCB are shown here:

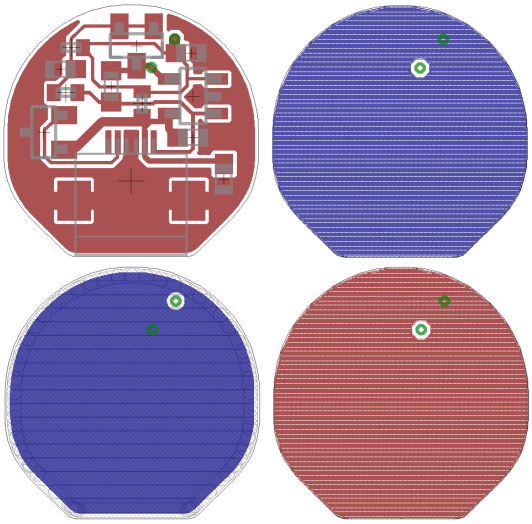

Figure 14. From top-left and clockwise: Top layer – Top internal layer – Bottom internal layer – Bottom layer

4.1.4 Assembling

Once the components were soldered, the thin plastic was sanded and glued to the copper at the bottom side of the PCB (using epoxy), and applying heat to reduce the curing time.
Two 0402 resistors were used, and they are quite difficult to solder. Usually, 0603 resistors and capacitors are used, which are bigger, and so, easier to solder.

An FFC (Flat Flexible Cable) connector was used. In this way, a single 'click' connects the 6 way FFC cable to the main acquisition board. The main problem of this cable is that it is not too robust, but it is good enough if you don't mistreat it.

4.2 Acquisition device

This device performs a very important part of the job of the whole system. It amplifies and digitizes the data of the electrodes, it makes some processing and packing, and it sends it through a wireless link. A broader view of the whole system can be seen at the next block diagram:

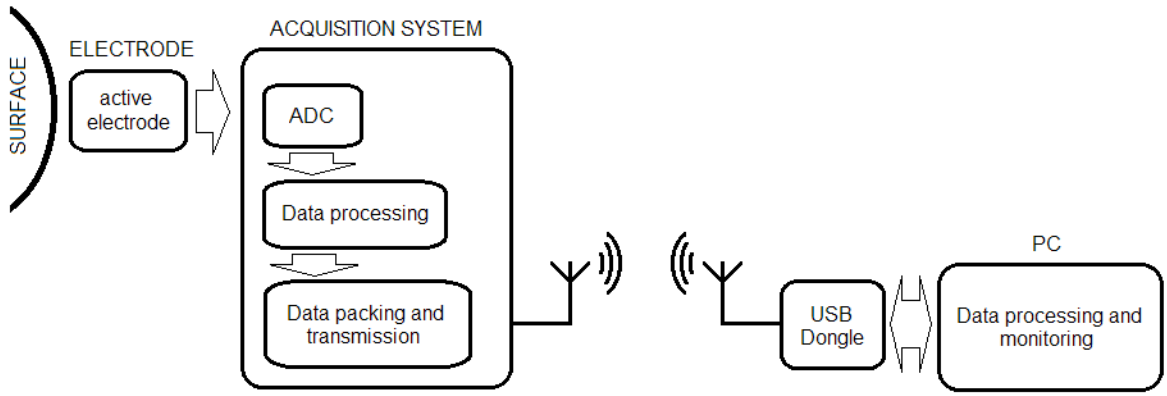

Figure 15. Block diagram of the whole system

4.2.1 Introduction

The desired features of this device are shown here:

- It should work with a single AAA battery, being compatible with rechargeable NiMH batteries
- Auto-power off capability
- Low power 2.4GHz wireless system
- Micro SD card to store large amounts of data, used for example when wireless is not available

- Audio (stereo) capabilities, to provide the feedback signals (for neurofeedback). This feature is desired to provide a full portable system, without having to depend on a computer
- A voltage and current monitor to know the total amount of energy consumed, and so, to estimate the life of the battery
- 2 buttons and 1 LED for a simple interface
- 2-channel ADC with internal PGA (Programmable Gain Amplifier)

Everything should be contained in a small 4 layer PCB, double sided assembling. The AAA battery held in a 2 lead PCB battery holder, integrated at the same PCB.

4.2.2 Schematic and explanations

4.2.2.1 Microcontroller

An STM32F103 from ST Microelectronics was chosen because it had the required peripherals (SPI, I2C, I2S, ADC, DAC and SDIO) and even more. It uses a quite powerful MCU (a Cortex-M3), with some DSP characteristics/instructions. The Cortex-M3 is the evolution of the ARM7TDMI. Furthermore, the programmer/debugger, as well as the software to compile/link/debug, and part of the initialization routines were already available. It is much faster to develop the microcontroller application if you are already familiarized with it, its architecture and features.

The first thing which must be done once you find the microcontroller which fits you needs, is to map its pins. Most pins have more than one function. The pins which only have one function are the supply pins, and some specific pins, like the ones used to program the device.

So, from all the possible pin-peripheral mappings, we have to find which will be used for what. For example, the SPI peripheral can be found at 2 different locations, but one of this locations is also shared by another peripheral we need. Furthermore, it will also be easier to route the PCB if we have into consideration the location of the different surrounding devices to communicate with.

The final mapping is shown here:

Pin number	Pin name	Function	Description
5	PD0	OSC_IN	The 16MHz crystal is connected here
6	PD1	OSC_OUT	
17	PA3	Timer	Provide the common mode signal
20	PA4	DAC1	Provide the analog signal for the left and right audio signal
21	PA5	DAC2	
41	PA8	MCO	Master Clock Output → 16MHz clock for the wireless IC
43	PA10	GPIO	Button detection, with input pull-up resistor
28	PB2	GPIO	LED output
59	PB7	GPIO	Auto-power off
45	PA12	GPIO	Enables the SD card by supplying it through a MOSFET
46	PA13	SWDIO	SWD (Serial Wire Debug), used to program the flash memory and debug the code
49	PA14	SWCLK	
7	NRST	NRST	
50	PA15	I2S3-WS	Data interface with the ADC chip. It uses the I2S protocol: Word Select, Clock, Serial Data, and Master Clock
55	PB3	I2S3-CK	
57	PB5	I2S3-SD	
38	PC7	I2S3-MCK	
61	PB8	I2C1_SCL	Configuration interface for the ADC and the audio chip. It uses the I2C protocol: Serial Clock, and Serial Data
62	PB9	I2C1_SDA	
26	PB0	ADC	Analog input to read the voltage of the battery
27	PB1	ADC	Analog input to read the total current consumption
14	PA0	ADC	Pins used to read the DC output voltage of the electrode
16	PA2	ADC	
22	PA6	ADC	Pins used to read the temperature of the electrodes
15	PA1	ADC	
24	PC4	GPIO	Pins used to switch on and off the analog switches
23	PA7	GPIO	
34	PB13	SPI2_CK	SPI, used to communicate with both the wireless IC and the dual DAC (shared peripheral). The pins are the
35	PB14	SPI2_MISO	

36	PB15	SPI2_MOSI	Clock, Master-Input Slave-Output, and Master-Output
44	PA11	GPIO	Pins used to handle the Chip Enable, Chip Select and an input IRQ (interrupt) pin of the wireless IC
37	PC6	GPIO	
33	PB12	GPIO	
4	PC15	GPIO	Pins used to handle the Chip Select, the Shut-down and the Load pin of the dual DAC
3	PC14	GPIO	
2	PC13	GPIO	
53	PC12	SDIO_CLK	SDIO peripheral, to interface the micro SD card. The pins are: Clock, Command, and Data[3..0]
54	PD2	SDIO_CMD	
39	PC8	SDIO_DAT0	
40	PC9	SDIO_DAT1	
51	PC10	SDIO_DAT2	
52	PC11	SDIO_DAT3	

Table 3: Pin mapping of the microcontroller

The schematic of the microcontroller is not shown because of its simplicity: you just have to ensure to place the 4 bypass capacitors as close as possible to the supply pins. The only thing to design here are the values for the capacitors of the crystal oscillator.

First of all, it should be explained that two components need a crystal oscillator: the microcontroller, and the wireless IC. That's why a single crystal oscillator was used, driven by the microcontroller, and which uses an output pin (the MCO) to provide the clock to the wireless IC.

The crystal oscillator used has a tolerance of ±50ppm. This is enough to fit the specifications of the wireless IC, which according to the manufacturer of the nRF24L01 must be a worst case of ±60ppm. It is because it has a PLL to increase this frequency up to 2.4GHz, and so, it is important in order not to get frequencies out of the range of each predefined channel.

Unfortunately, the oscillation frequency of a crystal oscillator doesn't depend on the crystal itself, but also on the lead/PCB/load capacitances. Usually, in a digital system, these capacitances are not critical, while kept between certain margin, but in this case we need the maximum accuracy.

Two capacitors must be placed in parallel to the crystal leads [11], like in this figure:

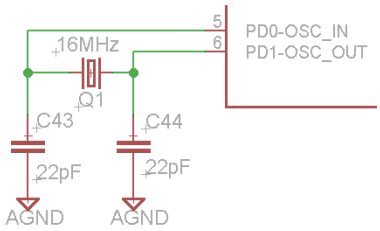

Figure 16. Oscillator and its capacitors

The function of these capacitors is to provide the feedback phase shift, which is required for the oscillator to run. Stray capacitances are often enough, but for a good design and to achieve an accurate frequency, these capacitors are required.

So, the capacitances for C43 and C44 which are best suited to get the nominal frequency of the crystal, are determined using this equation:

$$C_L = \frac{[C_{L1} + C_{in}] \cdot [C_{L2} + C_{out}]}{C_{L1} + C_{in} + C_{L2} + C_{out}} + C_{PCB}$$

Eq 13. Equation to calculate the total load capacitance of the crystal

C_L is the load capacitance (a value which gives the manufacturer of the crystal), C_{L1} and C_{L2} are the values for the C43 and C44 capacitors, C_{in} and C_{out} the input and output capacitance of the microcontroller pins, and C_{PCB} are the stray capacitances of the PCB traces.

Looking at the crystal datasheet (ABM3B series, from Abracon) we can see C_L is of about 18pF. And looking at the datasheet of the microcontroller, the input capacitances are of about 5pF. Furthermore, the PCB stray capacitances are supposed to be around 4pF. So:

$$18\text{pF} = \frac{[C_{LC} + 5\text{pF}] \cdot [C_{LC} + 5\text{pF}]}{2 \cdot C_{LC} + 10\text{pF}} + 4\text{pF} \quad \Rightarrow \quad C_{LC} = 23\text{pF}$$

Eq 14. Calculation for C43 and C44

The closest standard value is 22pF, this will be the value for C43 and C44.

4.2.2.2 Power supply

As already said at the introduction, a system able to work with a single AAA battery is desired. To achieve this, we need a DC/DC step up converter to boost that voltage. In this way, the step up converter gives 3.3V, regulated but with some switching noise. That's why these 3.3V are not used directly, and a LDO (low dropout linear regulator) is used to supply the digital components at 2.8V (it will be seen in a while).

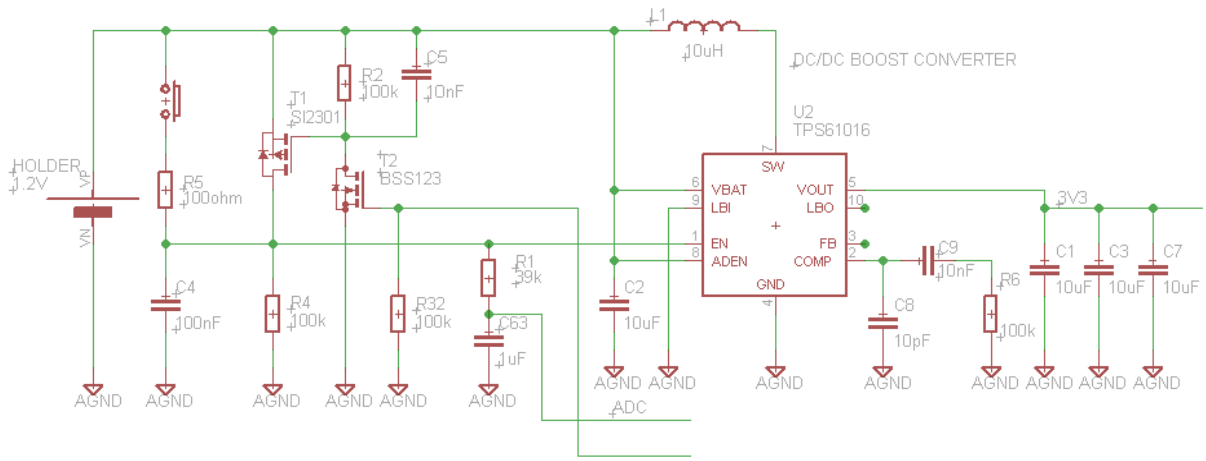

Figure 17. DC/DC power supply and auto-power off system

The DC/DC converter is a TPS61016 (a high efficiency converter). It needs a compensation network, connected at the COMP pin, and which values were taken from the datasheet application circuit. The output is formed by three capacitors in parallel, to decrease the ESR (Equivalent Series Resistance).

The circuit from the left side of the converter is used for the auto-power off feature. When the button in series with the resistance R5 is pressed, the enable pin of the converter is set to VBAT, and so, it starts working.

What happens next is as follows:

- When the output of the TPS61016 node is high enough, the LDO also starts working, supplying the digital section
- When the microcontroller starts working, it configures the PB7 pin (the auto-power off pin) as an output, and it is set to a logical high (3.3V). In this way, the NMOS T2 becomes active, and in turn it activates the PMOS T1
- In this state, even if the button is released, the whole system will continue running
- When the microcontroller decides to auto-turn off, it just set the PB7 pin at high impedance, and the R32 will discharge the NMOS gate, and in turn the resistor R2 will discharge the PMOS gate, and then R4 will discharge the capacitor C4, or in other words, will turn off the DC/DC converter by setting the enable pin to 0V.

We need the MOSFET T2 because the microcontroller can't drive directly the gate of T1. It is because all the input pins of the microcontroller have clamp diodes to Gnd and Vcc, and there would appear a current which would discharge the battery.

On the other hand, the wire connected at the capacitor C63 is connected to the ADC, and it measures the voltage of the battery. The resistor R1 is limiting the current when the device is turned of (Vcc=0V) and the button to turn on the device was pressed. If there was no R1, some current would flow through the microcontroller clamp diodes to Vcc (until the DC/DC converter and the LDO turned on).

The MOSFET T1 was chosen so that their V_{SGON} was as low as 1V (voltage which a NiMH battery can be considered discharged). If it were higher, then the device would turn off when the battery voltage reached that new V_{SGON} value.

The second part of the power supply schematic is shown here:

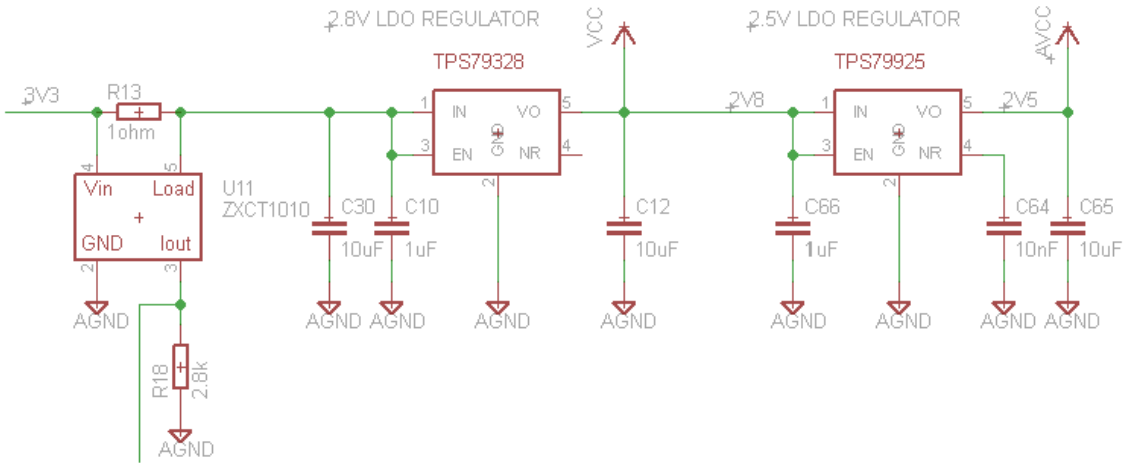

Figure 18. LDO power supply and current monitor

On the left side there is the 3.3V of the DC/DC output stage. A ZXCT1010 high side current monitor is used to sense the current. So, the power is quite easy to calculate, since it will be that current times 3.3V, and apply the efficiency of the DC/DC converter, which usually is about 90 to 95%. This current monitor is giving a current proportional to the differential voltage of R13.

In fact, instead of the ZXCT1010 it was used a ZXCT1041, a pin-compatible current monitor which gives directly an output voltage instead of a current. It is better because it is more linear at low voltages. Before, the resistor R18 acted like a current to voltage converter, but now it is not soldered, since we already have an output voltage.

It provides a gain of 10V/V, and since the resistor R13 is of 1Ω, the output of the current monitor is 10mV/mA. The ADC of the microcontroller is of 12 bits, and supplied at 2.8V. It means he have a resolution of:

$$I_{RES} = \frac{\frac{2.8V}{2^{12}}}{10mV/mA} = 68\mu A$$

Eq 15. Current resolution for the current monitor

About the LDOs. The first one is a TPS79328, which gives 2.8V. The dropout is of 3.3V-2.8V = 0.5V, and so there is no problem, since this LDO can work up to 200mV at 200mA of output current. Some care must be taken when designing these LDOs, since they can be unstable if the output capacitor is no correctly chosen. In this way, a high value - low ESR ceramic capacitor is used, and placed as close as possible to the regulator.

The same happens with the 2.5V LDO regulator, which is only used to supply the analog section. This regulator is a TPS79925, an ultra low noise LDO. In this case, the dropout is of 2.8V-2.5V = 0.3V, but it's also good enough, since it just needs a maximum of 175mV at 200mA output current to work.

To reduce the output noise, a capacitor of 10nF is placed at the NR pin. This capacitor bypasses the noise of the internal bandgap, reducing the noise up to 29.5μV_{RMS}.

4.2.2.3 Wireless link

The wireless section turns around an nRF24L01 IC from Nordic Semiconductor. It is a quite amazing IC, since it has lots of features. The more useful one is the secure channel: it handles the retransmissions by hardware when the packet is lost.

It uses the 2.4GHz ISM band, but it is unable to communicate with another IC rather than another nRF24L01. It is because it uses a specific protocol. When some bytes are sent and the secure channel is enabled, the transmitter changes to receiver, and the receiver to transmitter. Then, the current transmitter sends back an ACK if the CRC of the received packet was correct, and both IC return to its original state. There are other cases: if the packet is lost in one direction, or in the other, and so on. You can find the protocol at the datasheet.

This secure channel feature is really appreciated, because otherwise it should be done by the microcontroller, and a user protocol should be created to handle all the possibilities.

The maximum number of retransmissions can be programmed, as well as the time it waits between each retransmission. If this limit is exceeded, it can generate an interrupt using the IRQ pin. An interrupt also can be generated when a new packet is received.

As already seen before, it works at 16MHz, a clock provided by the microcontroller MCO (Master Clock Output) pin.

This IC can send up to 2Mbps. It has 126 different RF channels, 1MHz non-overlapping channel spacing when sending at 1Mbps, or 2MHz non-overlapping spacing when sending at 2Mbps.

The current consumption is also low: 11.3mA when transmitting, and 12.3mA when receiving. The output power can also be configured, at 0, -6, -12 or -18dBm.

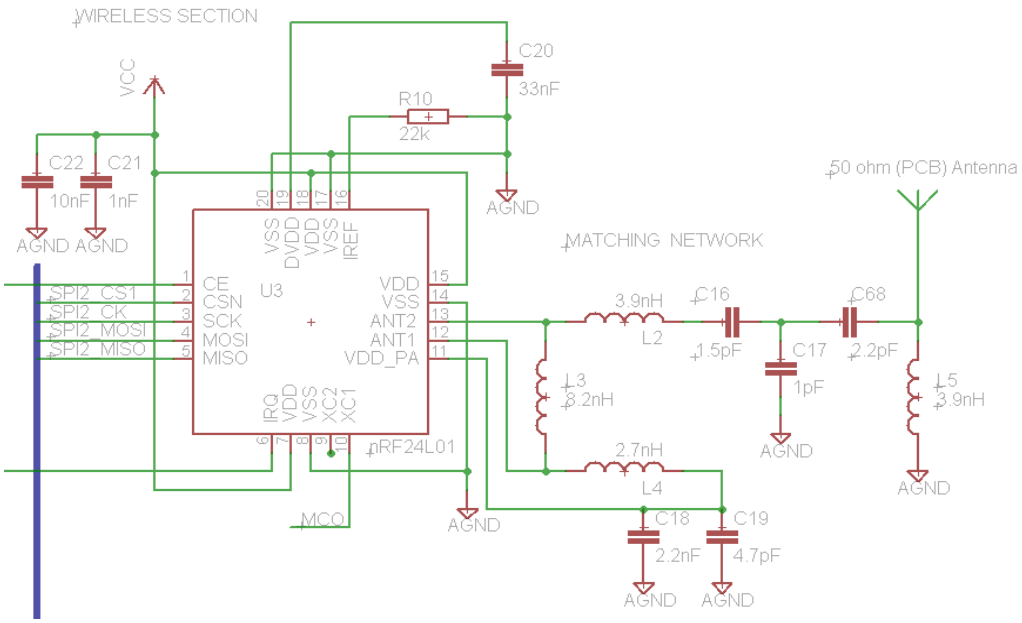

Figure 19. Schematic of the wireless

As seen before, the communication between this IC and the microcontroller is done using the SPI protocol. Each SPI transaction is sent in packets of 8 bits, and the total length depends on the command. It can be sent up to 33 bytes (command + data) in a single transaction when a packet of 32 bytes is transmitted. This mode is only used, because only raw data is sent, although it also has a useful feature: it can send a dynamic packet length. In this mode, you don't need to fill all the remaining bytes until reaching to 32, if you want to send, let's say 5 bytes, the amount of bytes is also sent as part of the packet header, and decoded by the receiver.

Another useful feature: it has a carrier detector, a bit which is set to 1 when a carrier at the same frequency than the selected channel is detected. It means you can do some statistics to know the band occupancy, that is, a simple band spectrum analyzer to change the current channel if the band is too busy.

At figure 19 is shown how we just need few components. The capacitors C20, C21 and C22 are just bypass capacitors and the resistor R10 is used to set an internal reference current. The values are found at the application example of the datasheet.

It is very appreciated that the manufacturer already gives the values of the components of the matching network. This circuit matches the impedance seen by the IC (which is 15Ω+j88Ω) at 50Ω for the antenna. They also provide the layout for the antenna, which has been implemented in the PCB.

The high frequency field is very specific, and if you are not used to it, much more difficult than 'conventional' electronics. It requires a lot of experience. In this way, this information is really helpful.

4.2.2.4 Audio

Although a complete audio IC is used, just few parts of it are used. It has a sigma delta DAC, which is interfaced using the I2S interface. Despite this, this IC was just used as an earphone buffer, and to control the volume of the signal. A little PCB was desired, and it means that the lower the component number the better.

The first reason the I2S interface is not used because the I2S peripheral is already used by the ADC. This microcontroller has two I2S peripherals, but one is shared with one SPI, and the SPI used by the wireless IC. The second reason is that this IC has a quite “high” current consumption when the dual DAC is used. In this way, it is disabled, and the two internal DACs of the STM32 microcontroller are used, which are of 12 bit each one. The signal is bandpass filtered using R3/C69 and C57/Internal resistance for the left channel, and using R8/C58 and C56/Internal resistance for the right channel. They can be placed in series

because the cutoff frequency of the low pas filter is more than 2 decades away from the cutoff frequency of the high pass filter; thus, their responses don't interact with each other. The high pass filter was set at 15,9Hz, and the low pass filter at 15.9kHz. Despite this, the attenuation at 20kHz (the maximum audible frequency) is still little, since the filter is a first order one.
So, the main function of this IC is to set the output of the signal at low impedance to directly drive the earphone. On the other hand, the volume, as well as the mute and some DAC features, can be programmed by the I2C bus (the bus shared with the ADC).

Here a mistake was committed. It was relied on the internal pull up resistors of the microcontroller pins (which all of them have), but when the pins are configured to be internally connected to the I2C peripheral as an *alternate function*, the internal pull up capability is not available. To avoid having to solder two resistors at each line (where there almost was no space), both pins were configured as open drain GPIOs with the internal pull up resistor, and the I2C protocol was programmed by firmware. It is not an elegant solution, but this I2C line is just used initially (when the ADC and the audio IC are configured). So, it is not a huge problem at all.

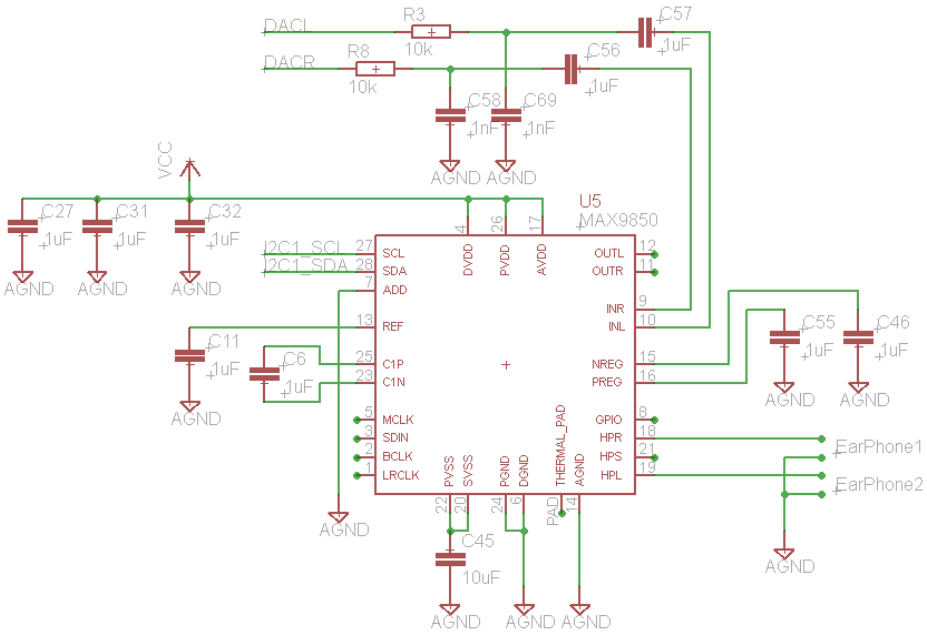

Figure 20. Schematic of the audio section

The advantage of using this IC is that it produces a ground-biased analog audio output from a single supply. Most amplifiers/buffers need capacitors at the output to block the DC signal, and they have to be very large because then a high pass filter is formed between these capacitors and the low DC impedance of the earphones (16, 32 or 64Ω). So, some space is saved at the PCB when these capacitors are not used. Furthermore, this IC is also offered in QFN package (5mm x 5mm). The earphone output power can reach up to 30mW.

4.2.2.5 ADC

This is one of the most important parts of the design. An EEG has an amplitude of few tenths of microvolts, and so, a low noise design should be achieved to succeed.

The schematic is shown at next figure 21:

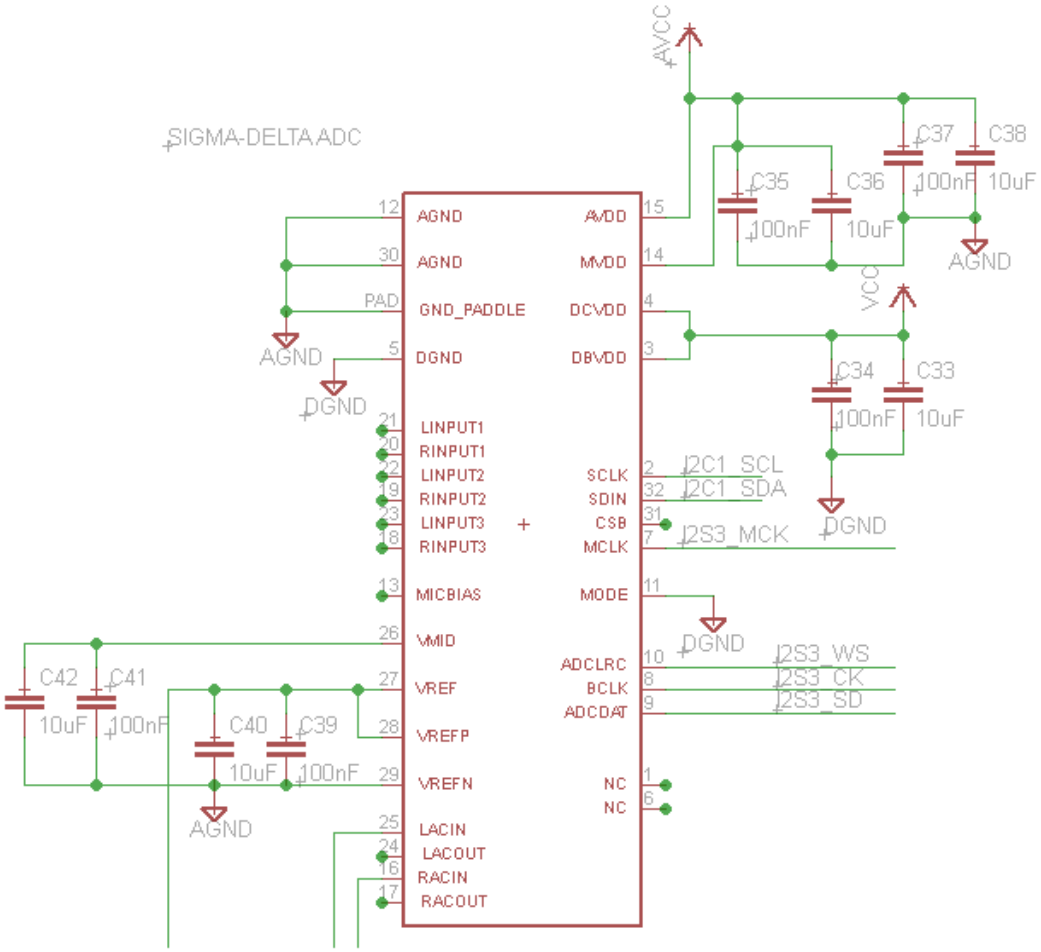

Figure 21. Schematic of the WM8737 ADC

First of all, it can be seen how the digital and the analog supplies are split. The digital supply (Vcc of 2.8V) supplies the digital interface of the ADC, as well as the decimation filter of the sigma delta ADC. On the other hand, the AVcc (of 2.5V) supplies the analog section, that is, the PGA (Programmable Gain Amplifier), the reference voltage, and so on.

The reference voltage is generated internally by the ADC, and it was taken as a reference for the rest of the analog circuitry. Taking the same reference can reduce the noise, rather than taking another reference or an absolute one (like ground).

All the bypass capacitors were placed according to the datasheet of the manufacturer.

In a normal SAR ADC, the quantum bit and the resolution is a quite straightforward way to deal with. But in a 24 bit sigma delta it is a bit different. The fact of having a data throughput with a length of 24 bits doesn't mean that the resolution of the ADC is the reference voltage divided by 2^{24} like in a SAR one. Instead, it basically depends on the sampling frequency. The only thing which can be used to compare a SAR ADC and a sigma delta one, is the SNR (Signal to Noise Ratio). The higher the SNR, higher the dynamic range by keeping the same resolution.

This sigma delta ADC is an audio (stereo) ADC. It means it has 2 embedded ADCs working in parallel, with great SNR characteristics (to be so cheap...). It also has an embedded microphone preamplifier, but it is not used because a high enough SNR using the second PGA stage was achieved. The input of this preamplifier is connected to the L/RINPUTn pins (they are multiplexed), and its output to the L/RACOUT. Usually, a capacitor is placed between this output and the L/RACIN to block the DC, but it was directly connected the EEG signal to the L/RACIN pins. It was also used the internally generated VREF as a reference for the external analog circuitry.

One of the problems about trying to use an audio ADC to measure low frequencies is that most of them have a digital filter to high pass filter the data. In this ADC, this feature can be disabled by means of the I2C configuration.

According to the datasheet, the SNR with an AVDD of 2.5V from line inputs to ADC, with the PGA gain set at 0dB, is of about 94dB Typ.

Since the ADC is an audio one, the full scale is measured in V_{RMS}. It is not said the input full scale for an AVDD of 2.5V, but it is said for 3.3V (which is of $1V_{RMS}$) and for 1.8V (which is of $0.545V_{RMS}$). A simple interpolation is telling us that for an AVDD of 2.5V we have $0{,}758V_{RMS}$, or in other words, $1.07V_P$ ($2.14V_{PP}$).

Putting all this together, we find out the resolution, which will be of:

$$SNR_{\text{dB}} = 20 \cdot \log_{10}\left(\frac{A_{\text{signal}}}{A_{\text{noise}}}\right)$$

$$94\text{dB} = 20 \cdot \log_{10}\left(\frac{2.14\text{V}}{A_{\text{noise}}}\right) \rightarrow A_{\text{noise}} = 42.7\,\mu\text{V}$$

Eq 16. Voltage resolution for the ADC with gain=1

This resolution is quite high, having into account a full scale of 2.14V. Despite this, we can see how we need to adjust the PGA gain to achieve a better resolution. This PGA can be programmed from -97 to 30dB, in steps of 0.5dB.

So, 30dB is a gain of about 32V/V, what means the resolution would increase up to $1.35\,\mu V$, enough to read EEG. Furthermore, remember that we will be acquiring at a higher sampling rate (3kHz) to read the gain of the electrodes, and then average the data to get an effective sampling rate of 250SPS. This average process is giving us an extra resolution, since in fact we are oversampling at a rate of 12x.

$$SNR_{\text{oversampling}} = 10 \cdot \log_{10}\left(\frac{f_{\text{oversampling}}}{f_{\text{Nyquist}}}\right)$$

$$10 \cdot \log_{10}\left(\frac{3\text{KHz}}{250\text{Hz}}\right) = 10.8\text{dB}$$

Eq 17. Increase of SNR due to oversampling [12]

And furthermore, the SNR found at the datasheet was measured with a low pass filter at 20kHz (the maximum audible frequency). In this case, the bandwidth is much lower, and so, the SNR should be higher.

Despite this, we will see that due to the high output voltage noise of the capacitive electrode, this relatively "high" resolution is even too much, since this voltage noise is already reaching the ADC. In other words, with less resolution it would be enough. But remember that having this resolution, the capacitive electrodes could be replaced by normal electrodes (or an improved capacitive one) and the whole device could be reused with almost no changes.

4.2.2.6 Input stage

The first analog stage is shown at the next figure 22. The input of this stage is directly the output of the electrodes. There are two of this stages, one for each electrode, although in this figure it is only shown a single one:

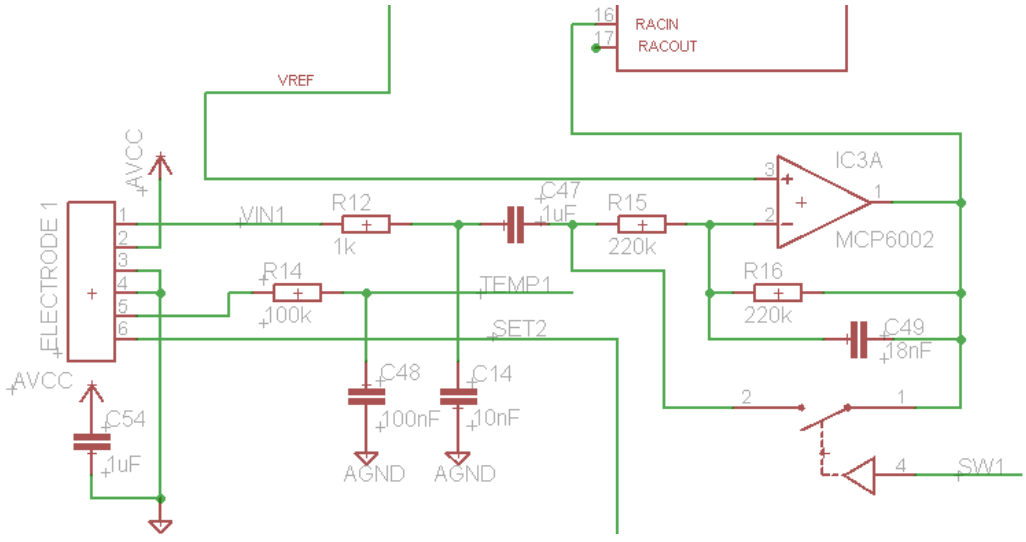

Figure 22. Schematic of the analog stage

The piece of component at the upper part of the schematic is the ADC. The connector is the same FFC type used in the electrode, and so, there is a direct pin to pin connection.

As already commented at the Electrodes section, the fact of having changed the initial design of the 20GΩ resistor had several repercussions. Since now we don't need the DAC anymore, the sixth pin of the connector (whose node is named SET2) can be released. But there is another problem. The initial design also provided a fast setting voltage feature, using the analog switch SW1. The main idea was that when a movement artifact was detected, the ADC would saturate almost for sure. Then, the DAC would compensate the electrode op amp charge to get about Vcc/2 at its output (by reading directly the output voltage of the electrode VIN1), but it wouldn't be a warranty for the ADC to leave the saturation, because there is a high pass filter formed by C47 and R15. That is why an analog switch was used.

When the microcontroller decides to close the switch, the capacitor C47 sees a low impedance source, with a voltage of Vcc/2 (in fact, VREF) at the right lead. On the other capacitor lead, there is an impedance of 1K, which is the value of the resistor R12. This resistor has 2 functions: to filter EMI noise (together with C14), and to avoid the op amps to oscillate. Op amps may be unstable when there is a capacitive load directly connected to the output, because it produces a phase shift at the frequency response. The unity gain configuration is the most prone to oscillate. Well, since at node VIN1 it is connected the output of the op amp of the electrode, we need a resistor to prevent this oscillation, as well as preventing a little peak current which would happen if R12 was a short.

Thus, before using this method, the time constant of the input stage was approximately of C47·R15. When the switch is closed, the new time constant is of C47·R12. Since R15 is 220 times higher than R12, the time constant is 220 times lower when the switch is closed. In this way, the fast voltage setting feature would accelerate 220 times that setting voltage process.

Another way to see how this works: when the switch is closed, the capacitor C47 is charged at such a voltage that once opened, there will already be Vcc/2 at the negative input pin of the IC3A op amp, and at its output. Thus, the ADC will be at half its full scale voltage.

In practice, now this system won't be used, because the DAC fast system feature was neither used. The analog switch is always opened.

The resistor R16 and the capacitor C49 form a low pass filter with a cutoff frequency of 40Hz, while the capacitor C47 and the resistor R15 form a high pass filter at 0.7Hz. This bandwidth is enough for neurofeedback purposes.

4.2.3 PCB design

The 4 layers of the PCB are shown at figure 23. The holes used to make contact between the different layers are called vias, and they are classified as buried, blind or through vias, depending on if the hole is internal, on if it starts to the top or bottom layer and ends into an internal layer, and on if they go through the whole PCB, respectively.

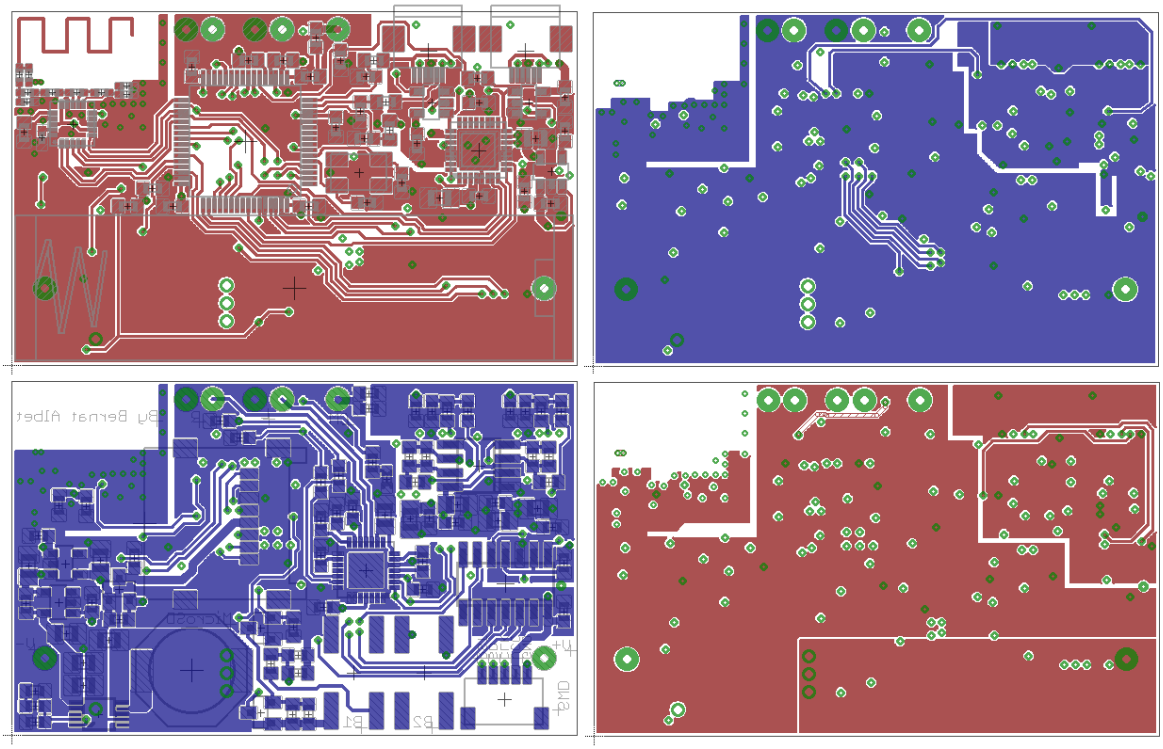

Figure 23. From top-left and clockwise: Top layer – Top internal layer – Bottom internal layer – Bottom layer

All the vias/holes used in this PCB go from the top to the bottom layer (through vias). More effort must be done, because sometimes a via from one layer may overlap a path at the other layer, and so, you have to move the component, or move the via. But the disadvantage of

using blind or buried vias is huge: the PCB is much more expensive. So, it was worth to spend some time trying to avoid overlappings.

Although the supply copper layers (GND and Vcc) are also at both top and bottom layers, the most important conductive area is the top internal layer for the GND, and the bottom internal layer for the Vcc. The main function of the top and bottom layers is to connect the different ICs between them.

It can be seen how an effort was done to separate the analog from the digital ground, and joining them into a single point (it can be seen at the top internal layer, at the right-mid position). Above this point, at the top layer, we can find the voltage regulator, which will supply 2.5V for all the analog devices from the 2.8V of the digital devices.

Furthermore, the wireless IC was placed as far as possible from the analog signal acquisition section, to prevent any possible noise to be picked up due to induction in some possible loop conductors when the radio transmission takes place. There are no layers below the antenna, to allow the high frequency signal to propagate through the space. The matching network components were placed according to the files which you can download at the web of the manufacturer. The traces, as well as the length and the shape of the antenna, was also taken from these files. So, these files were imported into a temporary layer of the Eagle Layout Editor software, and draw the traces into the layer of interest.

About the DC/DC switching converter. The conductor from the inductor to the pin of the IC was kept as short as possible, because the voltage is being switched from 0 to 3.3V+V_f of the diode, at a speed of several tenth of kHz. It means it could induce some noise if the trace were too long.

Finally, both buttons and the LED where placed at the bottom layer. The top layer should be face to face with the head, and so, the buttons and the LED must be to the other layer to be accessible.

The final board measures 3.2 x 5.1cm.

4.2.4 Assembling

A little and portable device was desired by design, but it also has its disadvantages. The major one is the size of the components to solder. There are QFN packages, LQFP, SOIC (the easiest to solder), and about resistors and capacitors, most of them are 0603, although there are 0402 packages as well.

A magnifier lens is a must, to check if there are shorts, or if the pin became well soldered. About the soldering iron, a common and cheap 30W solder was used.

To solder, a thin 0.2mm solder wire was used, mainly for the LQFP. It turns out that a QFN is easier to solder than a LQFP... It doesn't seem so, but since the QFN doesn't have leads, it's more difficult to short them. The solder paste was also used for some components.

In a company, the usual thing is to pay the manufacturer for a PCBA (a PCB + assembly), and so, you don't have to solder by hand. But it is quite expensive, and if it can be done by hand because you just need one prototype to test, the better (mainly when there is a lack of resources).

4.2.5 Firmware

The microcontroller is first initialized to a defined state. When the device is turned on, a POR (Power On Reset) is carried out, and leaves the device in a reset state. Among other things, this reset sets the PC (Program Counter) at a defined memory position (the reset vector), and it uses the internal clock of 8MHz to run the device. So, first of all, an assembler file is used to give all the low level information, and to fill all these vectors (not only the reset vector, but all the other interrupt vectors).

In a higher level, we can start programming the microcontroller in the typical *main()* function. First of all, it is switched from the internal 8MHz oscillator to the external 16MHz crystal oscillator. Indeed, it is just a crystal oscillator (not an active oscillator), and so, the driver of this crystal (mainly an inverter gate) is kept into the microcontroller. This new frequency is

divided by 2 to get again 8MHz, but this time it is much more precise in timing than the internal 8MHz RC oscillator. Then, the 8MHz go through the PLL (Phase Lock Loop) to be increased up to 24MHz, the main frequency used for the MCU and the rest of the peripherals.

The initial 16MHz (before being divided) are used to drive the clock of the wireless IC, using the MCO (Master Clock Output pin).

After the clock initialization, the GPIOs (General Purpose Input/Output) pins are configured. Each one can be used as a GPIO, but you must tell the microcontroller when you want an alternate function, like the SPI, the I2C, or an analog pin to be internally connected to the ADC. At this point, we are ready to control all the devices.

From a general point of view, it is described here what the microcontroller does when you press the button:

- It generates a 250Hz PWM signal, which is a higher frequency than the EEG bandwidth, and which is added as a common mode voltage
- It acquires data from the sigma delta ADC at 3kHz, which is 12 times higher than the 250Hz of the common mode voltage
- This raw data, on the one hand, is passed through an IIR peaking filter at 250Hz of central frequency. Then, the peak-to-peak amplitude is measured to know the effective gain of the electrodes.

  On the other hand, 12 samples from this raw data are averaged, to achieve an effective sampling rate of 250Hz
- The gain, as well as the samples, are packed into a user defined protocol, and send it through wireless to the USB board

This process runs forever, unless you press the button. Then, the LED blinks 2 times, and the device auto-powers off.

4.3 USB Wireless Dongle

4.3.1 Introduction

The USB Dongle has the task of receiving the wireless data from the acquisition board and send it through the USB. Two approaches were used to interface the PC, a virtual COM Port, and a HID (Human Interface Device). This discussion will be carried out at section 6 (Software).

4.3.2 Schematic

The wireless section of the USB Dongle is exactly the same than the one at the acquisition device. That's why it isn't shown at the schematic, and only the most important parts are shown:

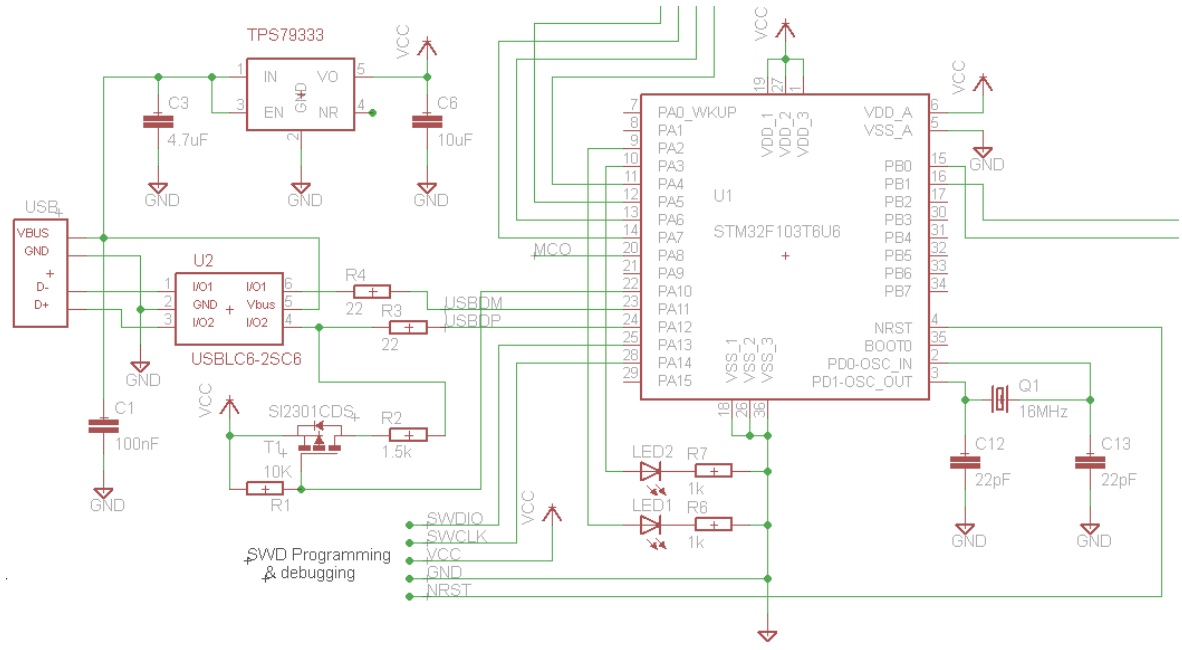

Figure 24. Schematic of the wireless Dongle

The microcontroller used is from the same STM32 family, although cheaper, since it doesn't need as much peripherals nor pins nor memory as with the acquisition device. The pin mapping is shown at this table:

Pin number	Pin name	Function	Description
2	PD0	OSC_IN	The 16MHz crystal is connected here
3	PD1	OSC_OUT	
20	PA8	MCO	Master Clock Output → 16MHz clock for the wireless IC
9	PA2	GPIO	Red and Green LEDs output
10	PA3	GPIO	
25	PA13	SWDIO	SWD (Serial Wire Debug), used to program the flash memory and debug the code
28	PA14	SWCLK	
4	NRST	NRST	
12	PA5	SPI2_CK	SPI, used to communicate with the wireless IC. Pins are the Clock, Master-Input Slave-Output, and Master-Output Slave-Input
13	PA6	SPI2_MISO	
14	PA7	SPI2_MOSI	
16	PB1	GPIO	Pins used to handle the Chip Enable, Chip Select and an input IRQ (interrupt) pin of the wireless IC
15	PB0	GPIO	
11	PA4	GPIO	
22	PA10	GPIO	Pin to enable/disable the USB by hardware
23	PA11	D-	USB Peripheral
24	PA12	D+	

Table 4: Pin mapping of the microcontroller

The crystal oscillator is the same than in the acquisition device, and so, the values for the capacitors C12 and C13 remain the same. About the LEDs, they were used to debug, and to visualize whether the wireless transmission is correctly going on or not.

The USB connector is a type A SMT, and it provides the 5V for the USB Dongle. These 5V are regulated to 3.3V thanks to the linear voltage regulator, and all the components are sourced at that voltage.

The last thing to comment about this schematic is about the USB. The U2 IC contains diodes from both D+ and D- lines to Vcc and Gnd. They protect the microcontroller against electrostatic discharges. It is important that these diodes had low capacitance, since the USB is a fast protocol (up to 480Mbps with the High speed USB 2.0). Despite this, this microcontroller only supports the full speed USB 2.0, what means a maximum speed of 12Mbps [13].

The MOSFET T1 has the function of pulling the D+ line up to 3.3V through the resistor R2 of 1.5KΩ. It has two functions:

1. The pullup resistor is used by the PC to detect the presence of a plugged device. The problem about connecting directly this resistor to 3.3V (without T1) is that the computer would detect and would try to communicate with the microcontroller even if it is not ready yet. The microcontroller has to configure the PLL for the USB peripheral (it works at 48MHz), and the USB peripheral itself before a correct communication can be carried out. Using T1, the microcontroller enables the USB when it is fully configured.
2. The speed of the USB is determined by where that pullup resistor is connected. If it is connected to D+, it sets the speed at Full Speed, while if connected to D-, it is set to Low Speed (1.5Mbps). So, R2 is also configuring the USB hub to work at Full Speed.

Since the microcontroller in reset state has all the GPIOs in high impedance state, the resistor R1 keeps the MOSFET T1 turned off. When the microcontroller wants to turn the USB on, it just have to set the GPIO as an output, and at low state.

4.3.3 PCB design

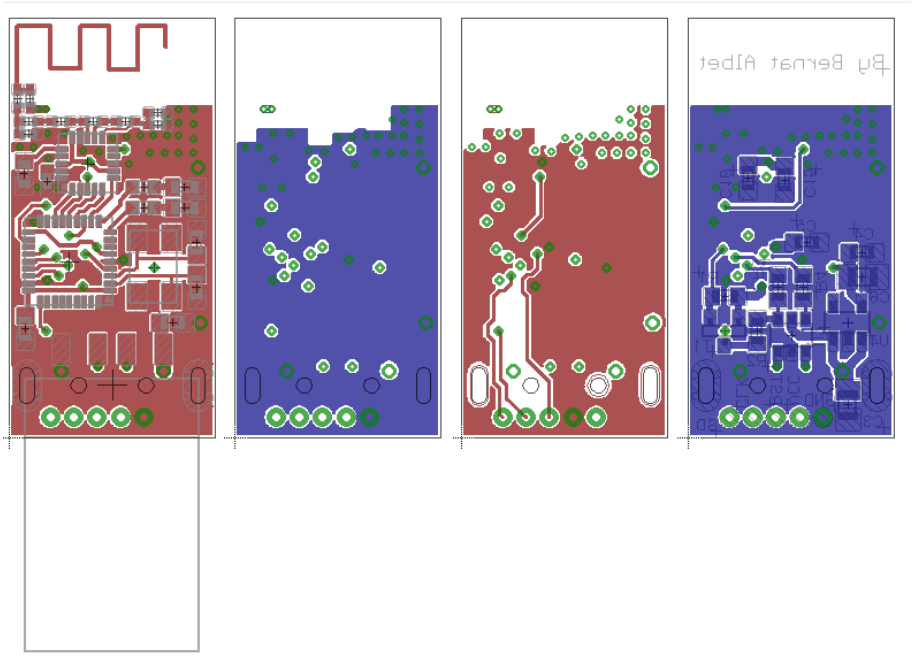

Figure 25. From left to right: Top – Top internal – Bottom internal – Bottom layer

The size of this board is of just 14x29mm (14x43mm measuring the USB connector). It is like a pen drive. The STM32 microcontroller, in this case, is a QFN36, which saves a lot of space.

The through holes below the USB connector are the SWD lines, to program and debug the microcontroller. A five way cable was soldered there; a connector was not considered to be necessary just to program it. In the case of the acquisition board, it wasn't a big deal to use a connector, since the board was much larger than the connector size, but adding a connector in this board would increase the size just for nothing.

In this way, the board fits into the plastic case of a pen drive, giving a better isolation (safety) and appearance.

4.3.4 Firmware

The firmware just takes the data which arrives from the acquisition device, and put it to another array (the USB array). Once this USB array is full, a packet counter variable is increased. Before understanding this, we should understand what the USB is doing.

The USB is a polling protocol. It means the microcontroller can never start a transaction. There is a field at the device descriptor which is telling at the computer how often it should ask for data, and how many data there is in each transaction. On the other hand, the USB peripheral of the microcontroller uses a pointer to the array of data, and it already knows the amount of bytes per transaction to send.

What happens now at a higher level (at the application layer) is that when the PC Software calls the function *readfile()* to read the data from the HID device, you receive the data, but you don't know if that data is new or you already have read it. That is why a packet counter was added, and then the software can know whether the read data is new or not in function of whether the packet counter is one unit higher than the current one, or the same. In this last case, the data is discarded.

All this is useful for the HID protocol, although as we will see later, another approach was used: using a virtual COM Port to send data like if it was a serial port. In this case, the firmware has to pack the data in a standard protocol used to communicate with the BrainBay software, an open source software to deal with EEG/ECG and other kind of data. This protocol was found at the documentation of the program (since it is open source).

Summarizing, at the attached files you can find two different projects, created with Keil uVision: one for the HID, and another one for the virtual COM Port. You can check the code for further details.

The wireless routines were reused from the acquisition device, since we are dealing with the same IC.

4.4 PCB manufacturing

In a 2 layer PCB it is possible to create your own boards at home, even having QFN packages. The problem is that it is not possible when you have 4 layers. That's why a cheap PCB manufacturer was searched, and that service was found at the Internet. The company is called *OurPCB*, and you can send them the files, then they make a quotation, you pay, and in about 3 weeks you get the PCB at home.

Since there are lots of different PCB software, the files to send to the manufacturer should be standard. These files are called the Gerber files, and all the PCB manufacturers accept them.
So, a Gerber file is basically an ASCII file, with a short command and a [X,Y] coordinate per line. All these command lines together form the image of one layer. A PCB design consist of several of these layers; here are described the files sent to the manufacturer:

- Filename.top ***(Top layer):*** This is the top copper layer, including the vias and paths
- Filename.toi ***(Top internal layer):*** The copper layer closer to the top one. The final board is 1.6mm thick, and the distance between this layer and the top one is 0.2mm
- Filename.boi ***(Bottom internal layer):*** The same than with the top internal. The distance between this layer and the bottom one is about 0.2mm
- Filename.bot ***(Bottom layer)***
- Filename.tsm ***(Top solder mask):*** The solder mask is a lacquer, usually green, which covers everything excepts the solder paths. These solder paths will subsequently be tinned. This lacquer prevents the copper oxidation, as well as a useful way to prevent electrical shorts at the soldering process of the components (due to its surface tension).
- Filename.bsm ***(Bottom solder mask):*** The same, but for the bottom layer
- Filename.tss ***(Top silkscreen):*** The silkscreen is an ink printing of something useful (like names/numbers/references or shapes), once the PCB is finished
- Filename.bss ***(Bottom silkscreen):*** The same, but for the bottom side
- Filename.out ***(Dimensions):*** This is the outline of the boards. Since 4 PCB were stacked together in the same PCB project (to avoid having to pay 3 times the tooling charges), this *out* file is important to delimit the edges of each board. In this way, they can mill the boards when they finish

- Filename.drd **(*Excellon drill data):*** This file contains the position and the tools used for each hole in the board
- Filename.drl **(*Drill sizes):*** In the previous file, the tools are defined as T01, T02... In this file, it is defined the diameter of the tool (for example: T01 0.3mm)

Apart from this, you must tell the manufacturer if you want the holes to be platted. By default, they are platted like a via. The main difference is they perform the holes before or after platting the PCB.

Finally, since there are no standard extensions for the Gerber files, you have to send them the description (like described before) for what each file extension means.

The remaining characteristics of the board are shown here:

- Board material: FR-4
- Solder mask: green / Silk screen: white
- Copper thickness: 1 oz (0.035mm)

4.5 Device assembling

In the company where the PCBs were manufactured, they also accept PCBA projects (PCB + Assembling). At the end, it is the cheaper way to proceed if you want to do, let's say, more than 10 boards (because they use pick and place machines and reflow techniques to solder the components). But to test a single prototype, the cheaper option is to solder it by hand. The problem of the PCBA project is that you must pay an extra 120 USD cost for the stencil (used to apply the solder paste to the paths). If then the prototype doesn't work, this extra cost was a waste.

But on the other hand, soldering such a tiny devices is not always simple. For example, a QFN package has a distance between pins of 0.5mm. The advantage of the QFN packages is that it is difficult to make a short circuit, because there are no pin leads. In this way, a LQFP is more difficult to solder, because the distance between pins is also of 0.5mm, but the pin leads allow a possible short, which is difficult to undo once it is done.

What it is really useful is using the solder paste used in the reflow process, even if you solder the components by hand. Thus, you can apply the exact amount of solder paste as you want with the dispenser (usually a syringe). For the shorts, it is also useful the flux, a liquid to decrease the surface tension of the tin and so, to electrically separate both leads.

4.6 BOM and costs

All the components were bought at the generic distributor (www.farnell.com). All the components with their price and quantities are shown here. They are organized in function of the board where they are soldered.

2 x Electrode

ITEM	DESCRIPTION	Farnell Code	QTY	UNIT PRICE	PRICE
MCP6001T-I/OT	OP AMP, CMOS 1MHZ 1.8V, SMD	4974992	2	0,300 €	0,60 €
TC1047AVNBTR	TEMPERATURE TO VOLT CONVTR, SMD, 1047	9762531	2	0,740 €	1,48 €
C0603C150J5GAC	CAPACITOR, 0603, 15PF, 50V, NP0	1414614	2	0,030 €	0,06 €
C0603C104K5RAC	CAPACITOR, 100NF, 50V, X7R	1288255	2	0,028 €	0,06 €
C0603C105K4PAC-TU	CAPACITOR, 1UF, 16V, X5R	1463388	6	0,022 €	0,13 €
MC 0.0625W 0402 1% 33K	RESISTOR, 0402 1% 33K	1358083	4	0,044 €	0,18 €
RT0603FRE07220KL	RESISTOR, 0603, 1% 50PPM 220K	1500613	2	0,030 €	0,06 €
BAV199	DIODE, DUAL, LOW LEAKAGE, SOT-23	1156415	2	0,084 €	0,17 €
FH12-6S-0.5SH(55)	SOCKET FFC/FPC, ZIF, 0.5MM, 6WAY	1324538	2	1,890 €	3,78 €
98266-0062	CABLE, FLAT, FFC, 6WAY, 152MM	1519837	2	0,670 €	1,34 €
				Total:	**7,85 €**

USB Dongle

ITEM	DESCRIPTION	Farnell Code	QTY	UNIT PRICE	PRICE
MC32605	PLUG, USB, TYPE A, SMT	1696546	1	0,870 €	0,87 €
USBLC6-2SC6	ESD PROTECTION, SMD, SOT-23-6	1269406	1	0,570 €	0,57 €
SI2301CDS-T1-GE3	MOSFET, P-CH, 20V, 3.1A, SOT23	1779260	1	0,310 €	0,31 €
TPS79333DBVRQ1	LDO REG, 200MA, ULTRA LO NOISE, SOT23-5	1624393	1	0,680 €	0,68 €
NRF24L01G	TRANSCEIVER, 2.4GHZ, SMD	1346268	1	5,980 €	5,98 €
STM32F103T6U6	MCU, 32BIT, ARM CORTEX M3, 36VFQFPN	1606328	1	4,440 €	4,44 €
ABM3B-16.000MHZ-B2-T	CRYSTAL, 16M, 18PF CL, 5X3.2 SMT	1611813	1	1,010 €	1,01 €
SML-LX0603SRW-TR	LED, SMD, 0603, RED	7608226	1	0,172 €	0,17 €
ASMT-RF45-AN002	LED, SMD, 0603, YLW-GRN	1652078	1	0,164 €	0,16 €
MC 0.063W 0603 1% 22R	RESISTOR, 0603 22R	9330844	2	0,017 €	0,03 €
CRCW06031K00FKEA	RESISTOR, 0603, 1KR, 1%	1469740	2	0,031 €	0,06 €
CRCW06031K50FKEA	RESISTOR, 0603, 1.5KR, 1%	1469743	1	0,031 €	0,03 €
CRCW060310K0FKEA	RESISTOR, 0603, 10KR , 1%	1469748	1	0,031 €	0,03 €
RC0603FR-0722KL	RESISTOR, RC22H 0603 22K	9238646	1	0,026 €	0,03 €
500R07S1R0BV4T	CAPACITOR, 0402, 1pF	1650784	1	0,033 €	0,03 €
500R07S1R5BV4T	CAPACITOR, 0402, 1.5pF	1650787	1	0,054 €	0,05 €
CC0402CRNPO9BN2R2	CAPACITOR, 0402, 2.2PF, 50V	3019123	1	0,044 €	0,04 €
GRM1555C1H4R7CZ01D	CAPACITOR, 0402, 4.7PF, 50V	8819661	1	0,024 €	0,02 €
C0603C220J5GACTU	CAPACITOR, 0603, 22PF, 50V, NP0	1414622	2	0,031 €	0,06 €
C0603C102K5RACTU	CAPACITOR, 0603, 1NF, 50V, X7R	1414608	1	0,022 €	0,02 €
C0402C222K5RACTU	CAPACITOR, 0402, 2.2NF, 50V, X7R	1414582	1	0,021 €	0,02 €
C0603C103K5RACTU	CAPACITOR, 0603, 10NF, 50V, X7R	1414609	1	0,022 €	0,02 €
C0402C333K4RACTU	CAPACITOR, 0402, 33NF, 16V, X7R	1414591	1	0,061 €	0,06 €
C0603C104K5RACTU	CAPACITOR, 100NF, 50V, X7R	1288255	4	0,029 €	0,12 €
LMK212BJ475KG-T	CAPACITOR, 0805, 4,7uF, MLCC	1611958	1	0,077 €	0,08 €
JMK212BJ106KD-T	CAPACITOR, 0805, 10UF, 6.3V, X5R	1463377	1	0,200 €	0,20 €
36501E2N7JTDG	INDUCTOR, 0402 CASE, 2N7, 5%	1265396	1	0,430 €	0,43 €
LQP15MN3N9W02D	INDUCTOR, 0402 CASE, 3.9NH, +/-0.1NH	1515363	2	0,122 €	0,24 €
HK10058N2J-T	INDUCTOR, MULTI-LAYER SMD, 8.2nH, 5%	1612124	1	0,037 €	0,04 €
				Total:	**15,83 €**

TOTAL:	**73,11 €**

A&P					
ITEM	**DESCRIPTION**	**Farnell Code**	**QTY**	**UNIT PRICE**	**PRICE**
2466	BATTERY HOLDER (AAA Type)	1702632	1	0,910 €	0,91 €
460DE08C3	CONNECTOR, MICRO SD, HINGED	1686452	1	1,410 €	1,41 €
FH12-6S-0.5SH(55)	SOCKET FFC/FPC, ZIF, 0.5MM, 6WAY	1324538	2	1,890 €	3,78 €
SM05B-SRSS-TB(LF)(SN)	HEADER, R/A, 5WAY, SMT	1679121	1	0,570 €	0,57 €
ASMT-RF45-AN002	LED, SMD, 0603, YLW-GRN	1652078	1	0,164 €	0,16 €
EVQQ2503W	SWITCH, SPNO, SMD	9962913	2	0,300 €	0,60 €
TPS61016DGS	BOOST CONVERTER, ADJ, SMD, 61016	8457816	1	2,040 €	2,04 €
TPS79328DBVRG4	V REG, LDO 200MA, SMD, SOT-23-5, 2.8V	1287687	1	0,360 €	0,36 €
TPS79925DDCT	V REG LDO 0.2A +2.5V, 79925, SOT-5	1135400	1	0,610 €	0,61 €
ZXCT1041E5TA	CURRENT MONITOR, BIDIRECTIONAL, 1041	1461566	1	1,530 €	1,53 €
STM32F103RDT6	MCU, 32BIT, CORTEXM3, 384K FLASH, 64LQFP	1624137	1	12,340 €	12,34 €
ABM3B-16.000MHZ-B2-T	CRYSTAL, 16M, 18PF CL, 5X3.2 SMT	1611813	1	1,010 €	1,01 €
NRF24L01G	TRANSCEIVER, 2.4GHZ, SMD	1346268	1	5,980 €	5,98 €
WM8737LGEFL/R	ADC, STEREO, 24BIT, MIC AMP, 32QFN	1776266	1	4,240 €	4,24 €
MAX9850ETI+	STEREO AUDIO DAC, 28TQFN	1593410	1	3,250 €	3,25 €
TS5A4594DBVR	ANALOG SWITCH 5V SOT23-5	1755412	2	0,250 €	0,50 €
MCP4922-E/SL	12BIT DAC DUAL, SPI I/F, SOIC14	1332114	1	3,170 €	3,17 €
MCP6002-I/SN	OP AMP, 1.8V, 1MHZ, DUAL, SOIC8	1292246	1	0,370 €	0,37 €
BSS123	MOSFET, N, SOT-23, 150mA	1510764	1	0,100 €	0,10 €
SI2301CDS-T1-GE3	MOSFET, P-CH, 20V, 3.1A, SOT23	1779260	2	0,310 €	0,62 €
LRCS0603-1RFT5	RESISTOR, 1R 1% 0603	1506136	1	0,057 €	0,06 €
CRCW0603100RFKEA	RESISTOR, 0603, 100R , 1%	1469752	2	0,031 €	0,06 €
CRCW06031K00FKEA	RESISTOR, 0603, 1KR, 1%	1469740	3	0,031 €	0,09 €
MC 0.063W 0603 1% 2K8	RESISTOR, 0603 2K8	1170832	1	0,019 €	0,02 €
CRCW060310K0FKEA	RESISTOR, 0603, 10KR , 1%	1469748	4	0,031 €	0,12 €
RC0603FR-0722KL	RESISTOR, RC22H 0603 22K	9238646	1	0,026 €	0,03 €
RC0603FR-0739KL	RESISTOR, RC22H 0603 39K	9238670	1	0,026 €	0,03 €
CRCW0603100KFKEA	RESISTOR, 0603, 100KR, 1%	1469649	9	0,031 €	0,28 €
RT0603FRE07220KL	RESISTOR, 0603, 1% 50PPM 220K	1500613	4	0,030 €	0,12 €
500R07S1R0BV4T	CAPACITOR, 0402, 1pF	1650784	1	0,033 €	0,03 €
500R07S1R5BV4T	CAPACITOR, 0402, 1.5pF	1650787	1	0,054 €	0,05 €
CC0402CRNPO9BN2R2	CAPACITOR, 0402, 2.2PF, 50V	3019123	1	0,044 €	0,04 €
GRM1555C1H4R7CZ01D	CAPACITOR, 0402, 4.7PF, 50V	8819661	1	0,024 €	0,02 €
CC0603DRNPO9BN6R8	CAPACITOR, 0603, 6.8PF, 50V	721943	2	0,051 €	0,10 €
GRM1885C1H100JA01D	CAPACITOR, 0603, 10PF, 50V	8819815	1	0,046 €	0,05 €
C0603C220J5GACTU	CAPACITOR, 0603, 22PF, 50V, NP0	1414622	2	0,031 €	0,06 €
C0603C102K5RACTU	CAPACITOR, 0603, 1NF, 50V, X7R	1414608	6	0,022 €	0,13 €
C0402C222K5RACTU	CAPACITOR, 0402, 2.2NF, 50V, X7R	1414582	1	0,021 €	0,02 €
C0603C103K5RACTU	CAPACITOR, 0603, 10NF, 50V, X7R	1414609	6	0,022 €	0,13 €
CC0603KRX7R9BB183	CAPACITOR, 0603, 18NF, 50V	3019743	2	0,044 €	0,09 €
C0402C333K4RACTU	CAPACITOR, 0402, 33NF, 16V, X7R	1414591	1	0,061 €	0,06 €
C0603C104K5RACTU	CAPACITOR, 100NF, 50V, X7R	1288255	18	0,029 €	0,52 €
C0603C105K4PAC-TU	CAPACITOR, 1UF, 16V, X5R	1463388	17	0,022 €	0,37 €
JMK212BJ106KD-T	CAPACITOR, 0805, 10UF, 6.3V, X5R	1463377	13	0,200 €	2,60 €
36501E2N7JTDG	INDUCTOR, 0402 CASE, 2N7, 5%	1265396	1	0,430 €	0,43 €
LQP15MN3N9W02D	INDUCTOR, 0402 CASE, 3.9NH, +/-0.1NH	1515363	2	0,122 €	0,24 €
HK10058N2J-T	INDUCTOR, MULTI-LAYER SMD, 8.2nH, 5%	1612124	1	0,037 €	0,04 €
SRU1038-100Y	INDUCTOR, SMD POWER, 10UH, 3.80A	1612718	1	0,063 €	0,06 €
				Total:	**49,43 €**

Table 5: Components and prices of the whole system

This is the total for the components, but we should add the PCB costs. The cost of the 4 boards which form the entire system is as low as 1.16 USD. But in a PCB project, the tooling charge is the higher cost, which only has to be paid once. So, for the first board, the cost is 353.48 USD, plus 30 USD for the shipping costs. It leads to a total cost for the first PCB of:

- 275€ (353+30 USD) + 73.11€ = **348.11€**

Despite this, and having into account the boards are worth 1.16USD each, the whole device would only cost 0.83€ (1.16USD) + 73.11€ = **73.94€**.

Despite the low cost of the device itself, the most expensive part of this project is the time devoted for the design. About a total of 250 hours were required to perform the following tasks: thinking about the problem, thinking about the solution, designing the chosen solution, drawing the schematics, designing the PCB, and defining all the PCB process with the manufacturer.

About the manufacturing (soldering) time, about 10 hours were required to solder everything. Just have in mind that in a real situation, a PCBA project is usually the first choice. Soldering SMD components by hand can be a source of problems, and also expensive for the companies.

And finally, about 200 hours to develop and debug the firmware, to develop the PC software, and to perform all the required tests, as well as analyzing the results (noise, and so on).

If we define the design engineer cost per hour at 80€/hour (from the company point of view), and the manufacturing engineer cost per hour at 50€/hour, then:

- 80€/hour · 450hours = 36000€
- 50€/hour · 10hours = 500€

This would mean a total of about **36500€**.

4.7 Environmental impact

All the components used in this device are RoHS compliant. It was an easy task, since all the components were bought at Farnell, and you can check a check box at their web site to only find RoHS compliant components. It was another design restriction.

RoHS means Restriction of Hazardous Substances directive. It is also called lead-free directive. It basically defines a list of substances which the manufacturer must use in less than a defined limit, depending on the substance. For example, lead, mercury or hexavalent chromium are permitted in a 0.1% by weight of homogeneous material, and cadmium just in a 0.01% [14].

Furthermore, the device was designed to work with a battery voltage as low as 1V. It means that a single 1.2V NiMH rechargeable battery can be used.

The PCB manufacturer was also paid by an extra amount of 20 USD for a lead free process.

5. Safety

The standard to apply to this EEG equipment is the IEC 60601-1 [15].

According to the class:

Class III → It is sourced with a battery of 1.2V DC, and 3.3V AC (due to the DC/DC converter) are internally generated. The limits to be considered a Class III device are: lower voltage than 24V AC, and lower than 50V DC.

According to the type:

Type BF → In this type, the device is floating (it is a wireless system). Furthermore, we must ensure the current in normal conditions is lower than 100μA, and lower than 500μA in fault condition.

Apart from being a wireless system, the electrode is an isolated one, what means that no DC current goes through it. In fault condition (in case the plastic used as a isolator was broken), we would find the input of the operational amplifier, which has a huge DC impedance. In fact, most medical devices are directly connected to that input pin. The AC impedance is also huge, although lower than the DC.

In other words, it is a really safe device.

6. Software

The software to interface the device is of vital importance, since we need a PC to process/view the acquired data of the electrodes. In this way, we have several approaches, each one with its own pros and cons.

6.1 Custom software approach

This approach seems to be the best for the project, since it is possible to achieve a high degree of freedom to deal with data. That is, the device is not a simple device which sends raw data. It can also send information about battery voltage, battery current, quality of the signal, it could be possible to implement a protocol to upgrade the firmware through a bootloader, to change the radio channel in case of too much packet loss due to too much traffic, and lots of other features. In this way, a very specific protocol is required to interface the device, and that protocol can be defined using this approach.

The cons are also clear: a lot of effort must be done to implement any simple function. For example, if you want to know the power spectrum density of your data, you need a lot of time to understand how to do the FFT (such as how to deal with Windows dynamic link libraries), time to implement it, and to plot the data in a graph.

The next figure 26 shows a screen capture of the current Visual C++ program. This project was developed using Visual Studio 2008, although it gets successfully converted to a Visual Studio 2010 project.

The *Device* list box shows the HID devices found at your system. So, once plugged, you should select the *EasyEEG*. It is a simple interface, since it is just used to take acquisitions and see that everything works fine. Once running, you can save the data to a text file (checking the box), and then, you can use Matlab for further analysis. You can also filter the 50Hz of the mains using the second check box.

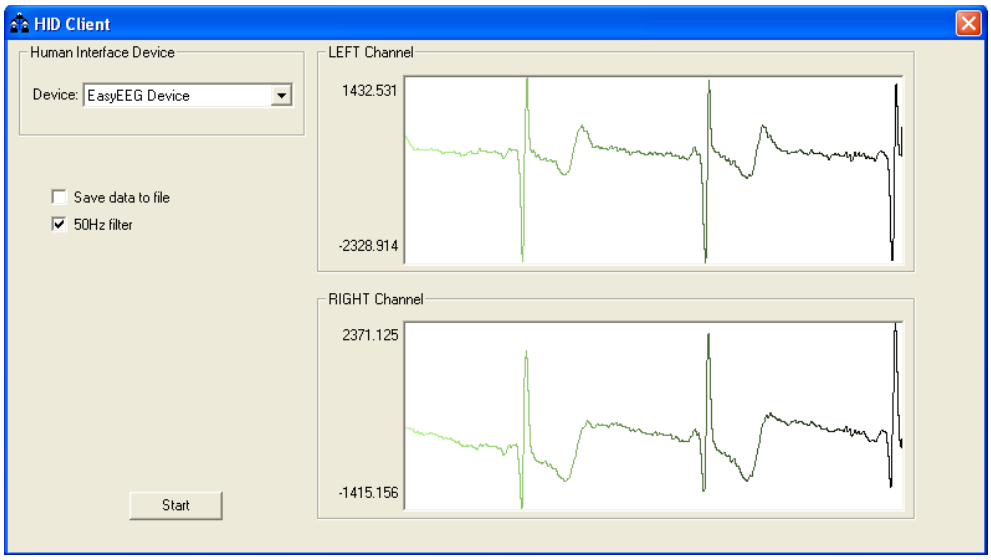

Figure 26. Screen capture of the custom program approach

Although the implementation time is quite high, you can achieve exactly what you have in mind: it is highly customizable. In this way, each channel is shown in a graphic where it auto adjusts the window zoom according to the maximum and minimum peak of the signal, it shows a sliding effect (the signal goes from right to left) while changing the color in the measure the time of the acquired signal is higher (light green at the left).

It offers other advantages. The main one is that an HID device doesn't need any driver. It is a true plug and play device. The second one, this program doesn't need any installation process, you just execute it and it runs. So, it is really fast to use the device: plug it to the USB, and execute the program.

Summarizing, the main problem is the development time. Related with it, a second problem is the lack of modularity; that is, if you want to add a new feature, or change something, you may need a lot of time. This problem is easily solved using the next approach.

6.2 Block design approach – BrainBay

The key of this approach is the modularity you have to implement whatever you want. BrainBay is an open source software, based on wiring blocks (like Simulink). There are blocks to process, to save data into a file, to visualize the signal, to send it via a server, and lots of other features.

In this way, if you want to see the frequency spectrum of the signal, you just have to drop a block and wire it from the data source to the FFT block.

The main problem is also clear: the interface between the USB Dongle device and this software. It accepts some devices and protocols, but it doesn't accept HID devices. For example, the *ModularEEG* is an EEG device, with an open hardware platform, and BrainBay support it. It uses an FTDI chip to convert the UART protocol to USB transactions, and in turn, it behaves as a virtual COM port.

So, the way the device was interfaced with BrainBay was programming the USB Dongle to also behave as a virtual COM port. The problem about doing this is that we need to install the virtual COM port driver. It is not a problem at all, but it is not as comfortable nor quick as with the HID approach. Furthermore, the BrainBay software is an open source project, and it is not fully stable; some little problems were found, although in general terms it works great.

In the next figure 27 it is shown the screen capture of BrainBay with an input signal of a $200\mu V_{PP}$ sine wave. You can see how easily you can wire the blocks and get the desired information from the signal. In this example, the signal of the channel 2 was shown directly to the first channel of the scope. This same signal was passed through a high pass filter and then through a low pass filter, and shown to the second scope, as well as showing its spectrum.

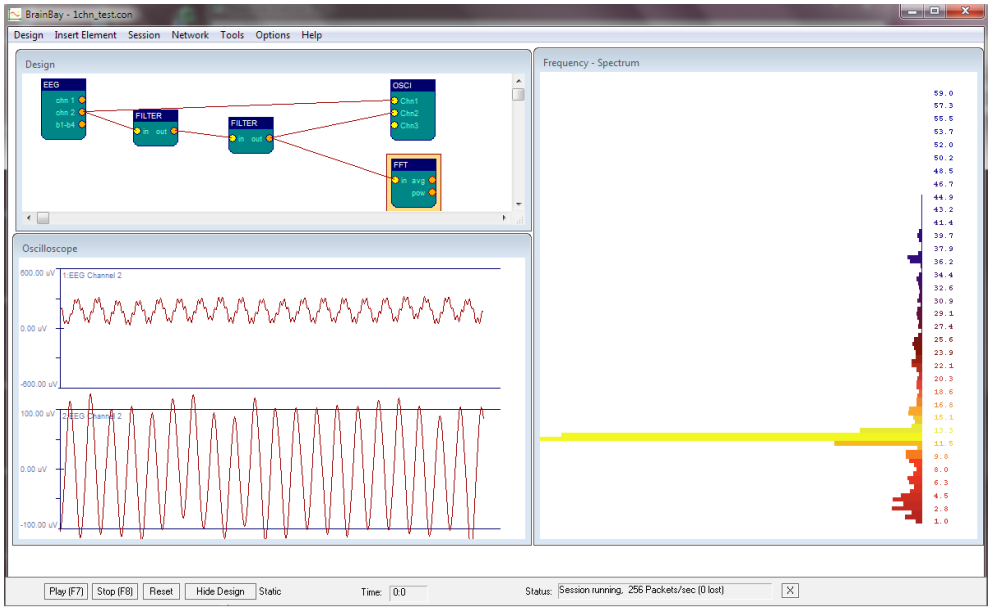

Figure 27. Screen capture of the BrainBay approach

6.3 A trade-off

Given both approaches, it seems everyone could choose which one fits better their needs: functionality (custom software) versus modularity (BrainBay). If a company has really clear the target of their device, they possibly would choose the first approach. On the other hand, the second solution seems better in terms of fast time-to-market, as well as giving different solutions to different acquisitions signals using the same device; that is, it is not the same to process the alpha signal of an EEG to give neurofeedback stimulus, than measure the heart rate. Both processes could be quickly developed in the second approach, and it would require much more effort in the first one.

Despite this, a mixed approach seems possible, although it implies more work: since BrainBay is an open project, it could be a good idea to implement a new block with its inputs and outputs, to model this device. In this way, you could add all the mentioned functionalities (voltage & current monitoring, firmware upgrade, and so on) to a really modular program. It was said that a lot of work was required because before starting to write code, you need to understand everything in the project. It is well documented, so it should not be a problem at all. Just a matter of time.

7. Functionality test

7.1 Measuring the bandwidth of the system

The response of the device is shown at next figure 28:

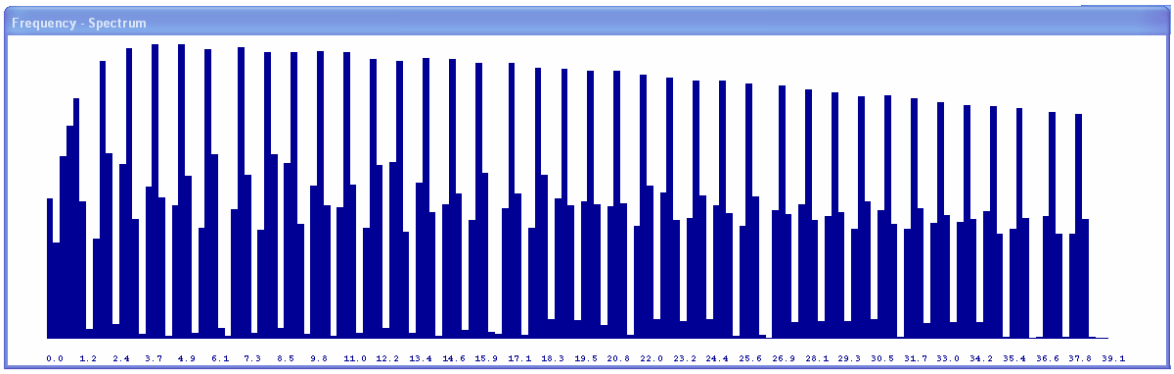

Figure 28. Screen capture of the BrainBay approach

- High pass cutoff frequency (-3dB): 0.7Hz
- Low pass cutoff frequency (-3dB): 37Hz
- Amplitude of the signal: 500uVpp
- Sweep from 0.5Hz to 39Hz (non logarithmic axis)

A function generator was used for the sweep. A metallic piece was placed touching the capacitive electrode to ensure the maximum coupling capacitance. This metallic piece was connected to the function generator, and all this setup was closed into a grounded metallic box to avoid interferences.

7.2 Real ECG measurement

The figure 26 (in the previous chapter) can also be used to see an ECG capture. The signal observed is quite good, although there is a problem with it. The system was designed to have a bandwidth from 0.7 to about 40Hz (the neurofeedback band of interest). Reading ECG with this device means that we are cutting frequencies of interest. The bandwidth of an electrocardiograph must range from 0.05Hz to 100Hz.

8. Noise analysis

This section is of special importance, because the main target (reading EEG signals) can't be accomplished due to the noise. So, the main goal of this section is to identify the source of the problem.

In all subsequent graphics, a real EEG data acquisition (with the electrode placed at *Cz*, according to the international 10-20 System) with the eyes opened is overlapped to see graphically the noise threshold we want: all the noise measurements above the EEG data, means we can't read EEG.

8.1 Noise of the measurement system

One of the first things to do is to measure the noise of the measurement system without the electrode. This step is necessary to be sure the acquisition device is working with a low enough noise to read EEG, and to be sure that the problem is mainly due to the capacitive electrodes. To do so, we will connect the ground to the first input channel, and measure the data (the floor noise):

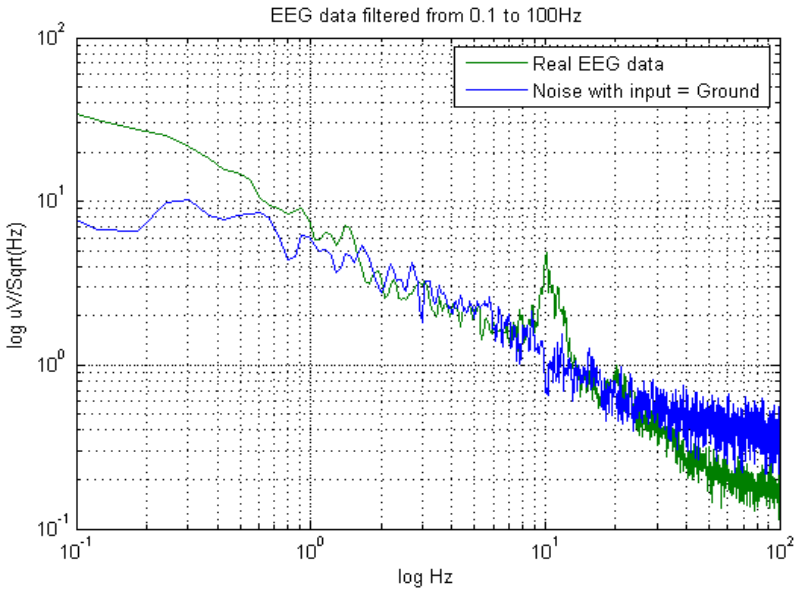

Figure 29. Noise when we use the ground as reference

Here we can see the first problem (although not a problem at all). The noise is higher than the EEG signal, but the cause is we are doing an absolute measurement, not a differential one. Back to the figure 22 (Schematic of the analog stage), we can see we take the reference voltage given by the ADC. Internally, this voltage is generated using a voltage divider, with 2 simple resistors. It means it is not stabilized. So, all the measurements not referred to the reference voltage itself (or canceled out) will have noise. In our differential two channel acquisition system it is not a problem, because the signal of one channel is subtracted from the other one, and since the noise is the same for both channels, it becomes canceled out.

So, a second capture was performed showing this fact. Instead of taking the signal of both ADC channels and subtract them, it is only measured the noise of a single ADC channel, but referred to the reference voltage. In this way, the output of the reference voltage is directly connected to the input of the channel. Like done at figure 29, but connecting the reference voltage instead of the ground:

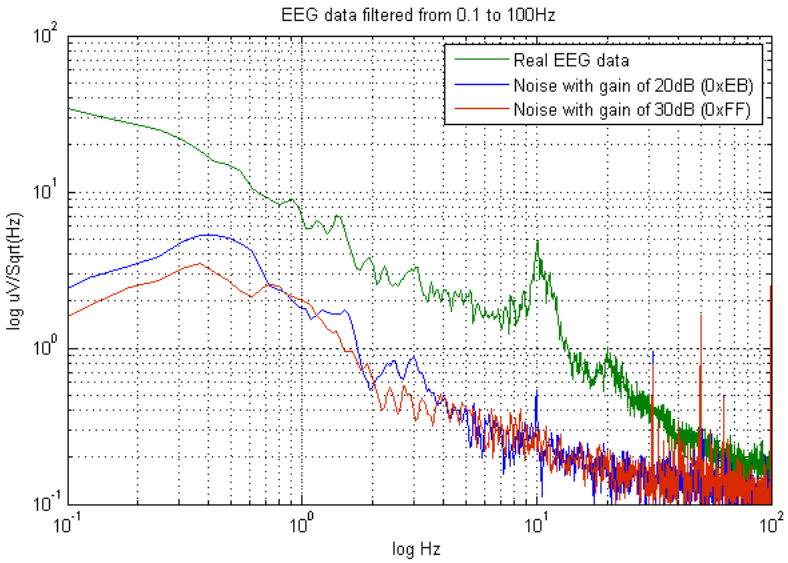

Figure 30. Noise when we use the ADC reference voltage as reference

Figure 30 shows how the noise is highly reduced, just by taking the reference voltage instead of the ground. Now, it is clearly seen how the acquisition system can take EEG acquisitions, since the noise is below the spectrum of the EEG signal.

Note 1: Since the noise is measured using low impedance sources, it is only attributed to the voltage noise of the operational amplifiers and thermal noise of the 220K resistors. At the noise section (3.3.2 Noise), it was analyzed the sources of noise in the electrode. So, the preference in the operational amplifier selection, as already said, was to have a low current noise rather than low voltage noise. That is the reason why the 1/f noise is quite high. But if we want to replace the capacitive electrodes by normal electrodes, we could choose low voltage noise operational amplifiers, with a low 1/f corner frequency, and this noise shown at figure 30 could be much more reduced.

Note 2: Some spikes appears. The data from this plot was measured with the feature to detect the electrode gain turned on. This feature uses a main frequency at 250Hz, and so, the tiny spikes are harmonics. This problem could have been solved if the final noise of the capacitive electrodes hadn't been higher than these spikes...

Note 3: As already explained at the ADC section (4.2.2.5), this ADC has a PGA (Programmable Gain Amplifier). It is configured by the microcontroller through the I2C bus. Two acquisitions were performed: using a gain of 20dB, and using a gain of 30dB. The hexadecimal values written at the ADC are also shown at the plot. Since the lowest noise is achieved with the highest gain, a gain at 30dB will be used for the subsequent measurements.

8.2 Noise of the capacitive electrodes

Once we have characterized the acquisition system, we can proceed to analyze the noise of the electrodes.

The test consists of connecting the electrode to the already analyzed acquisition system. Since the electrodes are highly sensitive, they will be placed into a metal case to create a Faraday cage, and this case connected to the reference voltage.

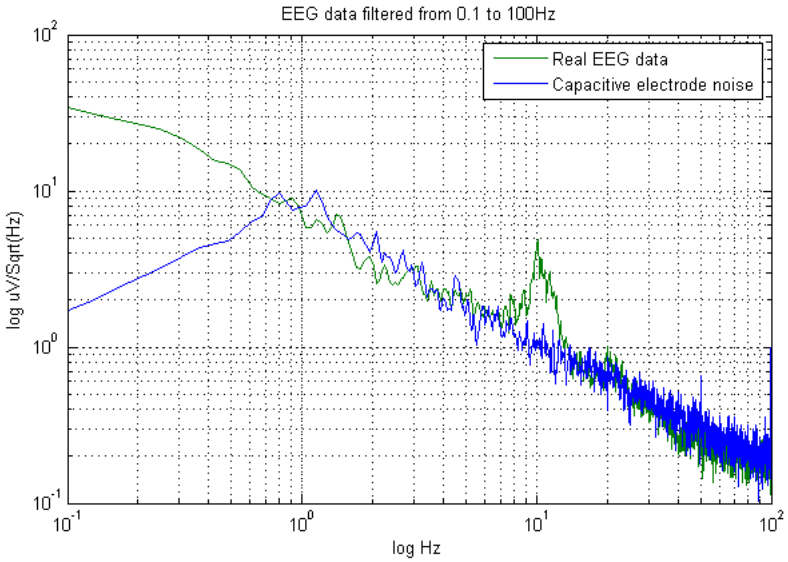

Figure 31. Capacitive electrode noise

It can be seen how close we are to be able to read EEG. It seems a coincidence, but the signal noise almost follows the same EEG spectrum... It can also be seen how linear the noise is (in log/log axis), what means the cutoff frequency of the input current noise is higher than 100Hz.

At the noise section (3.3.2 Noise), we predicted a much higher output voltage noise due to the input current noise. Several possible explanations can be deduced:

- The input current noise which the manufacturer shows at the datasheet is not really measured but a theoretical value
- It is a very restrictive worst case, and the real value is much lower
- It was measured under other conditions (like at high temperature with higher bias currents)
- Or that this measures are only true within a certain range of input impedance, being invalid when the input impedance is so huge

This last explanation seems quite logical, and an example to reinforce the idea is shown here: imagine an ideal non-inverter op amp with bootstrapping, already adjusted to compensate all the input stray capacitances. In this way, a huge (theoretically infinite) impedance should be

seen at that node. If now we add a current source at the input pin (which would model the input current noise), the output voltage noise should be (also theoretically) infinite! And it is true a bootstrapped op amp has a higher noise, but you can never get volts of noise at the output due to the input current noise.
Either way, the total output voltage noise due to all the noise sources, although not as high as expected, is still too high to read EEG. We should have in mind that this noise is constant, while the gain is variable, and lower than 1. So, the situation will be even worse when we have a gain lower than 1 (the SNR decreases even more).

At the State of the art section (1.6), it was said that the electrode performance would be compared with the QUASAR IBE (Insulated BioElectrode). The noise of this electrode could be obtained [6], and it is shown at figure 32:

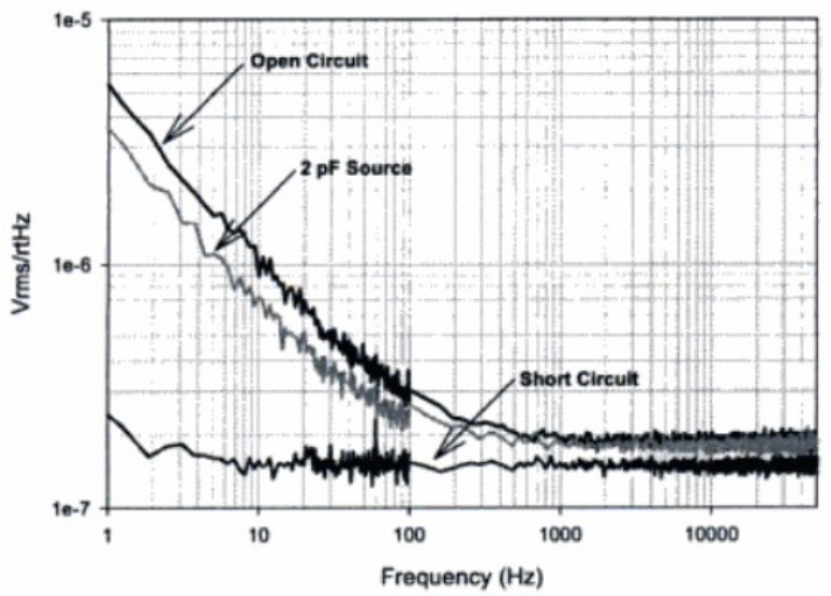

Figure 32. Noise of the QUASAR IBE electrode

This plot shows something really interesting. Compared with the noise of the designed electrode, we see a correlation with the *Open Circuit* case: at 10Hz, we have 1μV/√Hz, the same than in the QUASAR IBE. The slope is different, since at 1Hz we have about 2 times the noise of the QUASAR IBE, and at 100Hz, about the half, but it gives an approximate idea, and it shows that the order of magnitude is about the same.

Putting everything together, it could be deduced that QUASAR IBE is using a non-inverter buffer with bootstrapping. Using a non-inverter buffer because the noise decreases with the input impedance (the coupled capacitance), and using bootstrapping techniques because otherwise the electrode gain would vary in function of the input capacitance. This last statement can't be ensured, since it can not be deduce from the noise spectrum image, but a commercial electrode should be good enough to ensure a constant gain.

9. Problems found and proposal of solutions

The main problems found in this project, as well as the implemented solutions according to the gained experience working with it, are shown here:

- *Output voltage noise too high due to the input current noise*

One way to reduce the output voltage noise is to decrease the input impedance, and so, giving a path to the input current noise. It can be done capacitively, increasing a lot the coupling capacitance to decrease the AC impedance, but it could be unreliable, since the electrode area should be much larger. The problem about having a large area is related with movement artifacts, as follows:

- *Movement artifacts*

One of the problems about using a flat surface electrode is that some hair will remain between this and the scalp. It means a little movement will produce a drift at the output signal. This problem could be reduced a lot if some kind of conductive polymer was used, to mold a shape with spikes, which could reach the scalp. In this way, the amount of hair could be reduced a lot between the tips of the spikes and the surface of the scalp, because most hair would remain between the spikes. Since now these tips could be much close to the scalp (a really low distance) the capacitance would increase a lot, like what happens in a dry electrode.

So, it seems the best approach to solve both problems at once is to use an hybrid electrode, a solution between a fully capacitive electrode and a dry one (with direct contact with the skin, but with no gel). In this way, the contact of the spikes of the electrodes with the scalp would provide a lower capacitive impedance contact which would absorb the input current noise, at the same time the movement artifacts would be reduced a lot. There would also be a DC impedance, which would be really high (since there would be no electrolyte), but it would also help to reduce the input current noise effects even in the MΩ range, because we saw the noise in our very high input impedance (just capacitive impedance) is almost enough to read EEG.

Since a direct contact with the skin is needed to reduce the input current noise effects, we could also use a non-inverter buffer. We can't get a really high input impedance using an inverter op amp (see equation 5 at section 3.2.2 Inverter), since the negative node must remain at a fixed voltage to be into the non-saturation region.

In this way, we should add a bootstrapping technique to the non-inverter operational amplifier to be sure the input stray capacitance of the op amp didn't attenuate the read voltage. According to the problem of trimming the input capacitances, a digital potentiometer could be used, which are currently offered in packages as tiny as SC70-6 (2x1.25mm), and so, they could be placed at the same electrode.

10. Conclusions

The first conclusion is that the noise of the capacitive electrode is too high to measure EEG, but it is low enough to measure ECG.

A general conclusion from this project is that great things can be created with few resources, mainly in the electronics world. The economical investment was relatively low, and the results quite satisfactory. Although the goal couldn't be achieved, we should have in mind this was just a prototype, and as all prototypes, they are used to learn the problems and implement the solutions over a second prototype. It's difficult to achieve a difficult goal at first time.

The solutions to solve the limitations were presented at the last section.

Even without being able to measure the EEG with the capacitive approach, it is an easy task to reuse the whole platform. Thus, to measure EEG we just need to change the capacitive electrodes by normal Ag/AgCl electrodes + a buffer. The signals we need to drive the new Ag/AgCl active electrodes are already available, since the current electrode is already an active one. In this way, both the acquisition board and the USB Dongle could be reused with no changes.

11. Bibliography

[1] Image adapted from: John G. Webster, Medical Intrumentation - Application and Design, ISBN-13 978-0471-67600-3
[2] Holger Gecensleben, Birgit Holl, Birgit Holl et al., Is neurofeedback an efficacious treatment for ADHD? A randomised controlled clinical trial, 2009, DOI:10.1111/j.1469-7610.2008.02033.x
[3] Mirjam E.J. Kouijzer et al., Neurofeedback improves executive functioning in children with autism spectrum disorders, 2008, 10.1016/j.rasd.2008.05.001
[4] John Gruzelier, Tobias Egner and David Vernon, Validating the efficacy of neurofeedback for optimising performance, 2006, 0079-6123
[5] Types of neurofeedback, http://www.brainandhealth.com/Neurofeedback.html at 9/5/2011
[6] Dylan D. Schmorrow, Foundations of Augmented Cognition, 2005, 0-8058-5806-7
[7] Andrew Searle, Electrode performance and signal processing strategies for the discrimination of EEG alpha waves: Implications for enviromental control by unconstrained subjects without training, 2000
[8] Yu M. Chi and Gert Cauwenberghs, Wireless Non-contact EEG/ECG Electrodes for Body Sensor Networks
[9] C. Hoyle, A. Peyon, Bootstrapping techniques to improve the bandwidth of transimpedance amplifiers
[10] Texas Instruments, Noise Analysis in Operational Amplifier Circuits, SLVA043, 1998
[11] ST Microelectonics, Oscillator design guide for ST microcontrollers, AN2867, 2009
[12] Jayanth Murthy Madapura, Achieving Higher ADC Resolution Using Oversampling, AN1152
[13] USB Information, http://www.beyondlogic.org/usbnutshell/ at 11/11/2010
[14] RoHS Directive, http://www.bis.gov.uk/nmo/enforcement/rohs-home/ at 08/11/2010
[15] IEC 60601-1/FDIS, 2005