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Integrated Radio Frequency Synthesizers for Wireless Applications

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Abstract

This thesis consists of six publications and an overview of the research topic, which is also a summary of the work. The research described in this thesis concentrates on the design of phase-locked loop radio frequency synthesizers for wireless applications. In particular, the focus is on the implementation of the prescaler, the phase detector, and the chargepump.

This work reviews the requirements set for the frequency synthesizer by the wireless standards, and how these requirements are derived from the system specifications. These requirements apply to both integer-N and fractional-N synthesizers. The work also introduces the special considerations related to the design of fractional-N phase-locked loops. Finally, implementation alternatives for the different building blocks of the synthesizer are reviewed.

The presented work introduces new topologies for the phase detector and the chargepump, and improved topologies for high speed CMOS prescalers. The experimental results show that the presented topologies can be successfully used in both integer-N and fractional-N synthesizers with state-of-the-art performance.

The last part of this work discusses the additional considerations that surface when the synthesizer is integrated into a larger system chip. It is shown experimentally that the synthesizer can be successfully integrated into a complex transceiver IC without sacrificing the performance of the synthesizer or the transceiver.

Keywords: analog integrated circuit, frequency synthesizer, phase-locked loop, CMOS, BiCMOS, wireless communication, radio transceiver, prescaler, phase detector, chargepump, integer-N, fractional-N

Preface

The work for this thesis was carried out in the Electronic Circuit Design Laboratory of Helsinki University of Technology during 1997-2001, funded by the Technology Development Centre of Finland and Nokia Mobile Phones. The financial support from the Nokia Foundation and the Foundation of Electronics Engineers in Finland is also gratefully acknowledged. During 2000-2001, I also had the privilege to participate in the Graduate School of Electronics, Telecommunications and Automation (GETA), which partially funded the work.

Completing this thesis hasn't been an easy task. As I moved to industry full time in April 2001, I thought that the remaining work for the thesis would be a walk in the park. It wasn't. Finding the motivation and energy to complete the work during evenings and weekends has been a real burden. It has taken a lot of support from colleagues, friends, and especially family to get this work done. I am grateful to you all for that.

I would like to thank my supervisor, Professor Kari Halonen, for the possibility to work on this thesis very independently. His patience with the very slow last phase of the work is also greatly appreciated. I also warmly thank Prof. Mourad El-Gamal and Prof. Timo Rahkonen for reviewing my thesis and for their valuable comments and suggestions.

Thanks belong to all the staff of the laboratory for making it an effective and fruitful research community, and also a pleasant workplace. My colleagues at Spirea deserve thanks for significantly broadening my view of IC design.

Big thanks to all of my friends for keeping me busy with other things. When lacking motivation for writing, there was always something else to do. Sometimes the lack of motivation might even have been a consequence of having something else to do. Whichever way it was, thank you for standing by me.

My parents, Marketta and Jorma, deserve my gratitude for supporting me throughout my life. Curiosity for everything, a positive look at life, and the will to complete things I've started are only a few of the good things I've learned from you.

Finally, my warmest thanks to my dear wife Essi. Without your support I would never have finished this work. Thank you for sharing both the good and the difficult moments with me.

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Helsinki, April 2005

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Symbols and abbreviations

Symbols

$B_{channel}$	Bandwidth of the channel
B_{PLL}	Bandwidth of the PLL
C_{GD}	Gate-to-drain capacitance
C_{GS}	Gate-to-source capacitance
D_{SNR}	Degradation in signal-to-noise ratio
E_S	Energy of the symbol
f_{OUT}	Output frequency
f_{ref}	Reference frequency
f_T	Unity gain frequency
f_{VCO}	VCO frequency
$G_F(s)$	Transfer function of the loop filter
I_{CP}, I_P	Chargepump current
K_{PD}	Gain of the phase detector
K_{VCO}	Gain of the voltage-controlled oscillator
$L_{close-in}$	Close-in phase noise of the PLL
L_{int}	Integrated phase noise
N	Loop division ratio
N_0	Noise level
P_{wanted}	Power of the wanted signal
$P_{unwanted}$	Power of the interfering signal
S_{IF}	Spectrum of the intermediate frequency signal
S_{LO}	Spectrum of the local oscillator signal
S_{RF}	Spectrum of the radio frequency signal
t_{sw}	Switching time
V_C, V_{CTRL}	Control voltage of the VCO
V_{GD}	Gate-to-drain voltage
V_{GS}	Gate-to-source voltage
δ	Absolute frequency error
$\Delta\theta_e$	Phase error
ξ	Damping factor

ω_c	Crossover frequency
ω_n	Natural frequency
ω_{ref}	Reference frequency (in rad/s)

Abbreviations

ADC	Analog-to-digital converter
BAW	Bulk acoustic wave
BER	Bit error rate
BiCMOS	Bipolar complementary metal-oxide-semiconductor
CDMA	Code division multiple access
CMOS	Complementary metal-oxide-semiconductor
DAC	Digital-to-analog converter
DC	Direct current, zero frequency
DCS	Digital Communications System
DDS	Direct digital synthesizer
DQPSK	Differential quadrature phase shift keying
DSL	Digital subscriber line
EVM	Error vector magnitude
FET	Field effect transistor
FFT	Fast Fourier transform
GFSK	Gaussian frequency shift keying
GMSK	Gaussian minimum shift keying
GSM	Groupe Spéciale Mobile Global System for Mobile Communications
HDTV	High definition television
IC	Integrated circuit
ICI	Inter-carrier interference
IEEE	Institute of Electrical and Electronics Engineers
IF	Intermediate frequency
IFFT	Inverse fast Fourier transform
LAN	Local area network
LNA	Low noise amplifier
LO	Local oscillator

OFDM	Orthogonal frequency division multiplexing
OQPSK	Offset quadrature phase shift keying
PCB	Printed circuit board
PDC	Personal digital communications
PFD	Phase frequency detector
PLL	Phase-locked loop
ppm	Parts per million
QAM	Quadrature amplitude modulation
QPSK	Quadrature phase shift keying
RF	Radio frequency
rms	Root mean square
ROM	Read-only memory
SAW	Surface acoustic wave
SNR	Signal-to-noise ratio
SOI	Silicon on insulator
TDMA	Time division multiple access
VCO	Voltage-controlled oscillator
WCDMA	Wideband code division multiple access
WLAN	Wireless local area network
WPAN	Wireless personal area network

List of publications

- P1** Ahola, R., Vikla, J., Lindfors, S., Routama, J., Halonen, K., “A 2 GHz Phase-Locked Loop Frequency Synthesizer with On-Chip VCO”, Analog Integrated Circuits and Signal Processing, Vol. 18, No. 1, pp. 43-54, January 1999.
- P2** Ahola, R., Routama, J., Lindfors, S., Halonen, K., “A Novel Phase Detector with No Dead Zone and a Chargepump with Very Wide Output Voltage Range”, Proceedings of the 1998 European Solid-State Circuits Conference, pp. 352-355, The Hague, The Netherlands, 1998.
- P3** Ahola, R., Halonen, K., “A 2 GHz $\Delta\Sigma$ Fractional-N Frequency Synthesizer in 0.35 μ m CMOS”, Proceedings of the 2000 European Solid-State Circuits Conference, pp. 472-475, Stockholm, Sweden, 2000.
- P4** Ahola, R., Halonen, K., “A 1.76-GHz 22.6-mW $\Delta\Sigma$ Fractional-N Frequency Synthesizer”, IEEE Journal of Solid-State Circuits, Vol. 38, No. 1, pp. 138-140, January 2003.
- P5** Ahola, R., Halonen, K., “A 4 GHz $\Delta\Sigma$ Fractional-N Frequency Synthesizer”, Analog Integrated Circuits and Signal Processing, Vol. 34, No. 2, pp. 77-88, February 2003.
- P6** Ahola, R., Aktas, A., Wilson, J., Rama Rao, K., Jonsson, F., Hyryläinen, I., Brodin, A., Hakala, T., Friman, A., Mäkinen, T., Hanze, J., Sandén, M., Wallner, D., Guo, Y., Lagerstam, T., Noguer, L., Knuuttila, T., Olofsson, P., Ismail, M., “A Single Chip CMOS Transceiver for 802.11a/b/g Wireless LANs”, IEEE Journal of Solid-State Circuits, Vol. 39, No. 12, pp. 2250-2258, December 2004.

Summary of publications

This chapter gives a brief overview of each publication and the author's contribution in them. The author was responsible for all the work related to publications [P2]-[P5].

P1 A 2 GHz Phase-Locked Loop Frequency Synthesizer with On-Chip VCO

This paper presents an integer-N PLL design in a 0.5 μm BiCMOS process. The prescaler is based on the conventional dual-modulus architecture, and employs traditional ECL-type flip-flops. The first versions of the proposed new phase detector and chargepump topologies are presented in this paper as well. The chip also includes an integrated VCO, which was designed completely by Mr. Jyrki Vikla. Except for the VCO, the entire work was done by the author.

P2 A Novel Phase Detector with No Dead Zone and a Chargepump with Very Wide Output Voltage Range

This paper provides a more detailed analysis of the proposed new phase detector and chargepump topologies. Improved versions of both were designed, and experimental results are presented.

P3 A 2 GHz $\Delta\Sigma$ Fractional-N Frequency Synthesizer in 0.35 μm CMOS

This paper describes the first $\Delta\Sigma$ fractional-N synthesizer designed in this work. The synthesizer employs the phase detector and chargepump topologies developed previously. The prescaler uses the phase-switching architecture, and is designed completely in CMOS. A new D flip-flop topology allows it to function up to input frequencies of over 2 GHz. The prescaler implements eight possible moduli (64...71) that are controlled by an on-chip digital MASH 1-1-1 $\Delta\Sigma$ -modulator. The design is done in a 0.35 μm CMOS process, and the experimental results show good performance.

P4 A 1.76-GHz 22.6-mW $\Delta\Sigma$ Fractional-N Frequency Synthesizer

This paper is based on the same chip as [P3], so the building blocks are the same as above. However, the experimental setup was rebuilt and some of the measurements redone for this paper. This has removed some peculiarities in the experimental results presented in [P3]. The results presented in this paper are state of the art: the close-in phase noise is -81dBc/Hz at an offset frequency of 10 kHz, and the spurious level is lower than -85 dBc.

P5 A 4 GHz $\Delta\Sigma$ Fractional-N Frequency Synthesizer

This paper provides a more detailed theoretical analysis of the close-in phase noise requirements of the synthesizer in different systems. It employs the same phase detector and chargepump topologies as the previous papers, but provides a more detailed discussion on the tradeoffs in their design. This design also includes a BiCMOS prescaler based on the phase-switching architecture, implementing eight moduli (128...135). The prescaler operates up to an input frequency of 4.3 GHz. The experimental results show that the design works relatively well, although the performance is not as good as that of the 2 GHz synthesizer presented in [P4].

P6 A Single Chip CMOS Transceiver for 802.11a/b/g Wireless LANs

This paper describes a complete transceiver chip that fulfills the IEEE 802.11 a, b, and g standards. The key features of the chip include a new dual conversion architecture that avoids image rejection filtering, and an extremely flexible interface towards the baseband chip, allowing the chip to operate with multiple different baseband chips. In addition to these features, this chip also had challenging frequency synthesizer design requirements. The chip includes two PLLs that have to operate simultaneously with each other, and with a multitude of other circuit blocks on the same die. Even the reference crystal oscillator is integrated on the same chip. The experimental results show excellent PLL performance; the two PLLs have a combined integrated phase noise of -34 dBc, which equals an rms phase error of 1.1° .

In this part of the work, the author was responsible for specifying the requirements of the blocks, including the PLLs. The author was also responsible for interface and integration issues that are inevitably faced when integrating an entire system on a single chip. In addition to these, the author had the responsibility for the technical management of the entire project, including detailed reviewing of all the blocks. The paper itself is completely written by the author.

1 Introduction

1.1 Background

The growth of mobile telecommunications has been extremely rapid during the last decade. The cellular phone penetration rates in Finland have gone from 20% in 1995 to almost 100% in 2004. In July 2004, Sweden was the first country to exceed 100% penetration, i.e. there are more cell phone subscriptions than there are people. But not only has the market for mobile speech grown; during the last couple of years, all kinds of previously wired connections between home and office appliances have gone wireless as well. The cellular phone has a calendar function that synchronizes automatically with the desktop calendar through a Bluetooth connection, the laptop computer accesses the Internet through a WLAN connection, the wireless mouse sends information to the desktop computer through a proprietary wireless connection, etc.

The wireless connections come in a vast variety of flavors, depending on the application. Smooth web browsing requires data rates thousands of times higher than monitoring the temperature in an apartment. On the other hand, a cellular phone requires at least hundreds of times longer range than a wireless mouse. There is a multitude of different wireless standards for different applications. However, common to almost all of these standards is that the data to be transferred is somehow modulated on a radio frequency (RF) carrier, and the modulated signal is then transmitted over the air, and received and demodulated in the receiving end. In both the transmitting and the receiving end, an accurate RF carrier signal must be generated. Therefore, a radio frequency synthesizer is always required, regardless of the wireless standard.

More recently, the digital convergence has presented additional challenges to the design of the radio transceivers, including the frequency synthesizers. One handheld unit may now include for example a dual-mode, quad-band cellular phone, a Bluetooth radio, and a WLAN radio. From a cost point of view, it would of course be beneficial to share as much of the hardware as possible between the different radio standards. Sharing parts of the hardware, however, often means that the chosen shared component is not the optimal one for all the standards. As an example, the crystal oscillator might be shared between all the radio standards in the above example. The same crystal oscillator frequency will not be optimal for all standards, though, resulting in more challenging frequency synthesizer design.

As the wireless standards evolve, users expect higher and higher data rates. The available frequency spectrum is limited, though. Therefore, the new standards must employ more complex modulation types to increase the number of bits transmitted over a fixed bandwidth. The more complex modulation types, however, normally require a higher signal-to-noise ratio as well, resulting in tougher requirements for the analog building blocks of the radio.

Although the advances in the performance of integrated radio frequency synthesizers have been overwhelming in the recent years, there is still a lot of work to be done in the field. The digital convergence and the ever more complex standards keep pushing the requirements of the synthesizer further and further.

1.2 Research contribution

The research described in this thesis focuses on the design of radio frequency synthesizers for wireless applications. Both integer-N and fractional-N phase-locked loop (PLL) designs are presented and discussed. In the case of fractional-N PLLs, the different methods for reducing the fractional spurs are discussed. On the circuit level, the work focuses on three key building blocks of the PLL, namely the prescaler, the phase detector, and the chargepump.

In the prescaler designs, the main focus has been on implementing the required functionality with as low power as possible. In the fractional-N designs, different methods to implement multiple moduli were studied as well. In the phase detector design, the focus has been on finding new ways of eliminating the dead zone problem. The new phase detector topology presented in this thesis has been awarded both Finnish and U.S. patents. The chargepump designs presented in this thesis have focused on developing new topologies that would maximize the usable output voltage range. The presented PLLs prove that the designed building blocks can be combined to form a radio frequency synthesizer with state-of-the-art performance.

The last part of this thesis concentrates on the additional challenges that emerge when the RF synthesizer is integrated as a part of a much larger transceiver IC. The possible negative effects caused to the PLL by the rest of the system are analyzed, as well as the interference caused by the PLL to the rest of the system.

1.3 Organization of the thesis

This thesis is divided into two parts. In the first part, an introduction to the issues of integrated radio frequency synthesizer design is given to summarize the work that has been carried out. In Chapter 2, different radio transceiver architectures are briefly introduced, mainly to put the rest of the work into context. Also, different frequency synthesis techniques are reviewed. The various requirements set by the wireless standard on the frequency synthesizer are examined in Chapter 3. Chapter 4 introduces the special issues encountered when going from integer-N PLLs to fractional-N PLLs. In Chapter 5, the building blocks of a PLL are discussed. Different implementation alternatives are introduced, and some of the previously published work is reviewed. Finally, Chapter 6 focuses on the additional issues when the synthesizer is integrated into a larger system on a chip. The second part of this thesis contains the published papers.

2 Frequency synthesizers in radio systems

The first part of this chapter will briefly introduce different radio transceiver architectures that have been used in recent years. The main focus is not on the properties of different architectures, but in motivating the rest of this work. The second part of the chapter will introduce shortly different methods to generate a tunable local oscillator signal. Although the focus in the rest of this work is on phase-locked loops, other methods of completing the same task are also reviewed.

2.1 Radio transceiver architectures

Since Edwin H. Armstrong presented his superheterodyne radio receiver in the 1920's [17], several different architectures for implementing both the receiver and the transmitter sides of it have been developed. Most of them share the need for a tunable *local oscillator* signal, i.e. a signal whose frequency can be accurately set. The different architectures are discussed in a number of textbooks [18][19], and will be explained here only briefly for the sake of completeness and to motivate the work. In short, the required frequency selectivity can be implemented either by tuning the local oscillator frequency or by tuning the intermediate frequency (IF) filter. The IF filter is usually a passive surface acoustic wave (SAW) filter, and thus not tunable, which leaves a tunable local oscillator as the only choice.

The most widely used receiver architecture, the superheterodyne receiver, is shown in Figure 2.1. The received signal is first amplified and filtered to suppress the image frequency, and then downconverted to an intermediate frequency. The actual frequency selectivity is then implemented with the IF bandpass filter. Now, achieving the required selectivity at the IF frequency (usually from tens to more than one hundred MHz) has at least up to date been possible only with a discrete (SAW, BAW, etc.) filter, which is by nature centered on a fixed frequency. To be able to downconvert all desired frequencies to a fixed IF frequency, the LO signal must be tunable.

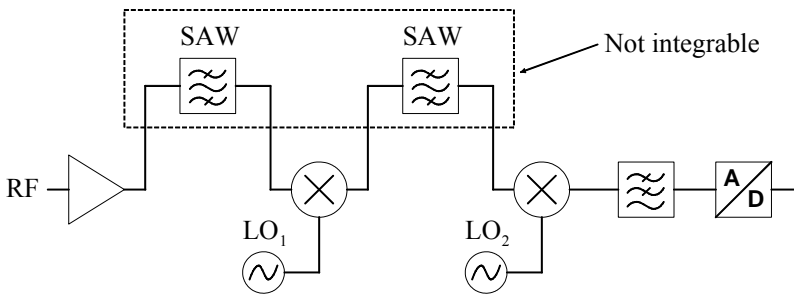


Figure 2.1 The superheterodyne receiver architecture.

Although the superheterodyne architecture is still used in most of the world's radio receivers, it is very poorly integrable due to the SAW filters. Therefore, the research in recent years has focused on alternative receiver architectures, mainly the direct conversion receiver (Figure 2.2), which can be completely integrated on a single die [20]. Now, the received signal is converted directly down to around DC, and the

bandpass filtering that caused problems in the superheterodyne architecture is translated into lowpass filtering. Again, to be able to downconvert all the desired radio frequencies to the same frequency (DC), the LO signal must be tunable.

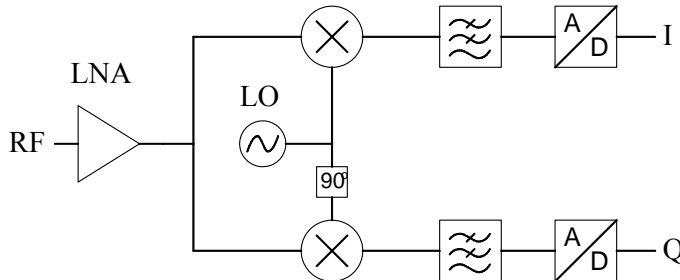


Figure 2.2 *The direct conversion receiver architecture.*

The transmitter part of a radio is much more straightforward than the receiver. Basically, the signal to be transmitted can be upconverted in one or more steps, the one-step or direct conversion approach (Figure 2.3) being dominant in today's radio transmitters. Again, to be able to upconvert the modulated baseband signal to the desired RF frequency, the LO signal must be tunable.

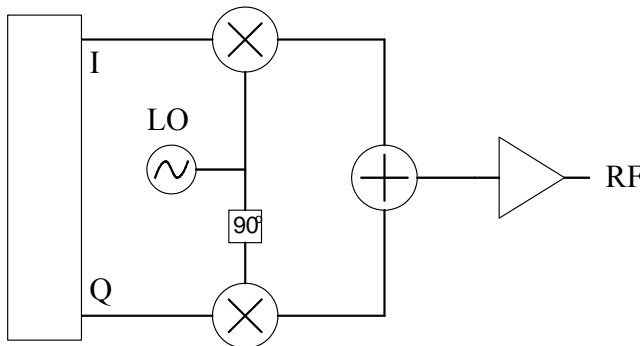


Figure 2.3 *The direct conversion transmitter architecture.*

2.2 Frequency synthesis techniques

Several different frequency synthesis techniques have been presented in the literature over the years. They can be quite clearly divided into three separate categories, namely direct analog synthesis, direct digital synthesis, and indirect analog synthesis. In this context, “indirect” refers to a system based on some kind of a feedback action, whereas “direct” refers to a system having no feedback.

The three categories of frequency synthesis techniques will be introduced in the following three sections. The fourth section will introduce different combinations of these techniques.

2.2.1 Direct analog synthesis

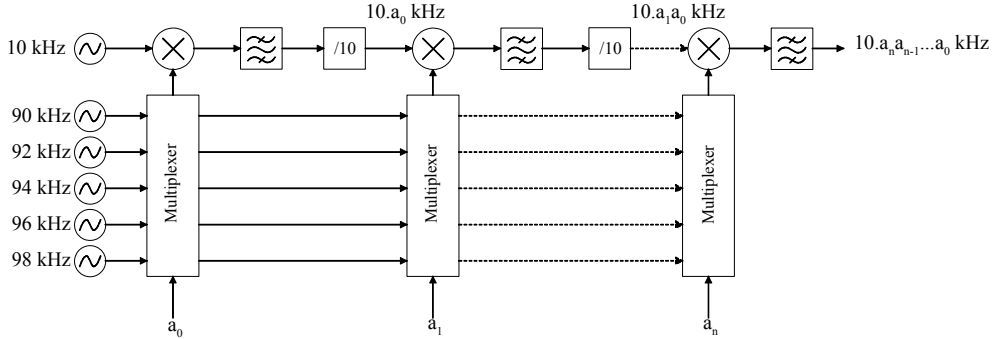


Figure 2.4 The block diagram of a direct analog synthesizer.

Figure 2.4 shows an example of a direct analog synthesizer [21]. The frequency resolution is achieved by mixing signals of certain frequencies, and then dividing the resulting frequency down. Theoretically, this process can be repeated arbitrarily many times to achieve a finer frequency resolution.

Advantages of the direct analog synthesis are very fast switching times and, in theory, arbitrarily fine frequency resolution. However, this technique requires a very large amount of hardware, as can clearly be seen even from the simple example block diagram (Figure 2.4). Also visible in the figure is the fact that the synthesized frequency is lower than the highest input frequency (in this example, approximately an order of magnitude lower). Therefore, the use of direct analog synthesis techniques in high-frequency applications is severely limited.

Also noise is a problem in direct analog synthesis. To achieve a reasonably low-noise output signal, all input frequencies (left side of Figure 2.4) will have to be low-noise crystal oscillators, resulting in a lot of external components. Moreover, all the mixers, bandpass filters, and dividers are in the signal path, meaning that their noise will also contribute to the phase noise in the synthesized frequency.

For the reasons mentioned above, the use of direct analog synthesizers is limited to low frequencies and to applications that are not too sensitive to noise. Even in these applications, they are relatively expensive compared to the synthesis techniques presented in the following sections. Therefore, very few direct analog synthesizers, if any, are used in commercial applications.

2.2.2 Direct digital synthesis

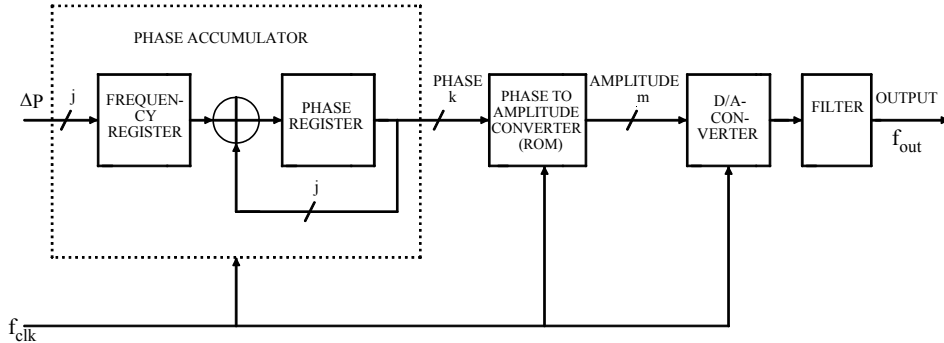


Figure 2.5 The block diagram of a direct digital synthesizer.

Figure 2.5 shows the basic principle of direct digital synthesis [23]. The desired output frequency is fed to the phase accumulator as a digital word. The phase accumulator increments its output value by this word once every clock cycle. When the full scale of the accumulator is reached, it wraps around. The output of the phase accumulator is thus a digital ramp signal, whose period is the same as that of the desired output frequency. In other words, the phase accumulator output contains information about the instantaneous phase of the synthesized frequency.

The amplitude of a sinusoidal signal at different phase values is stored in the sine read-only memory (ROM). The instantaneous phase of the desired output signal is used as the address to the ROM, and the output is the instantaneous amplitude of the synthesized signal.

To get an analog output signal, the amplitude information has to be converted to the analog domain in the digital-to-analog converter (DAC). The output of the DAC contains a lot of spurious tones, harmonics, etc., that have to be filtered out before the signal can be used. The smoothing filter in the output of the DAC attenuates the harmonics to an acceptable level, but the in-band spurious tones still remain. Their frequencies are predictable, but as they are in the signal band, they will not be attenuated by the filter.

Direct digital synthesis has some very strong advantages. It has arbitrarily fine frequency resolution and a very high switching speed. Also, different phase, frequency, and amplitude modulations can be implemented in the digital domain, and require only a small amount of extra hardware. Due to the fact that most of the signal processing is done in the digital domain, direct digital synthesis also lends itself very well to full integration in a CMOS or BiCMOS technology.

Until recently, the main disadvantage of direct digital synthesis has been the speed requirement and the huge power dissipation in the digital parts of the circuit, i.e. the phase accumulator and the sine ROM. However, with modern deep submicron CMOS technologies, the power dissipation has been dramatically reduced, and the achievable

speed has become fairly high. Now, the bottleneck in the direct digital synthesizer is the DAC. Demands on the DAC clock frequency, resolution, and linearity are overwhelming. This limits the use of direct digital synthesizers in high-frequency applications. However, they have become de facto standard in high-performance low-frequency signal generators (e.g. [22]). Recently, they have also found use in cellular base station applications.

Direct digital synthesis has been applied to quite a few commercial products, as well as investigated widely in the literature. Good examples of the strong sides of the technique are a frequency resolution of 0.0349 Hz in [23], the modulation capabilities in [24], and the generation of multiple modulated carriers in [25]. On the other hand, some examples of the downsides have also been published: a power dissipation of 3 W in [26], and a spur level as high as -30 dBc in [27].

2.2.3 Indirect analog synthesis

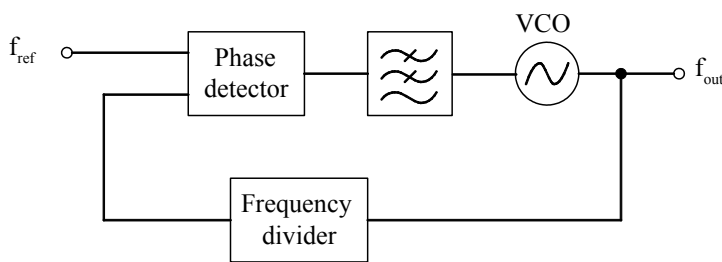


Figure 2.6 The block diagram of a simple phase-locked loop.

Figure 2.6 shows the block diagram of the phase-locked loop, i.e. an indirect analog synthesizer, at its simplest. Here, the synthesis is based on the feedback action of the loop. The output frequency is divided down in the frequency divider. The phase of the output signal of the divider is compared with the phase of a reference signal in the phase detector. The output of the phase detector is lowpass filtered to generate a control voltage for the voltage-controlled oscillator (VCO). If the phase of the frequency divider output lags the phase of the reference frequency, the phase detector steers the VCO to a higher frequency, and vice versa.

Indirect analog synthesis, or the phase-locked loop, is the most suitable technique for the synthesis of high-frequency sinusoidal signals. No block has to operate at a frequency higher than the output frequency. Also, the only component that is necessarily external is the reference frequency oscillator (or at least the crystal used as the resonator in the oscillator).

The basic configuration of the phase-locked loop (PLL) has a few disadvantages, too. For example, the frequency resolution equals the reference frequency. On the other hand, the loop bandwidth has to be significantly lower than the reference frequency, which results in relatively slow switching. Thus, the finer the frequency resolution of the PLL, the slower the switching speed.

2.2.4 Hybrid synthesizers

In addition to the three basic synthesis techniques introduced above, several modifications or combinations of them have been published. Most of these synthesizers are modifications of the PLL, aiming to allow a wider loop bandwidth and a finer frequency resolution than the basic principle.

The interpolating PLL synthesizer [28] uses controllable delay lines in front of the phase detector inputs, allowing a frequency step smaller than f_{ref} . However, the measured results [29] show that imperfections in the delay lines generate spurious tones, and the noise of the delay line adds to the total synthesizer noise, increasing the noise floor of the synthesizer.

Several multi-loop architectures have also been proposed. The simplest approach would be to generate the reference frequency to the main loop by another phase-locked loop [30]. The bandwidth of the main loop can be increased without losing frequency resolution, if the reference loop is programmable, too. The drawback of this architecture is that the close-in phase noise will be the product of the phase noise contributions of the two loops. However, with careful design, reasonably low noise levels have been demonstrated [31].

Also, much more complicated multi-loop architectures have been published [32]. In addition to the huge complexity (several bandpass filters, mixers, etc.), the performance of this synthesizer is quite limited, and it is quite useless in practical applications.

Another proposed hybrid solution is generating the reference frequency of the phase-locked loop by a direct digital synthesizer [33]. The DDS allows a fine frequency resolution while the bandwidth of the PLL is relatively large. However, all the spectral impurities in the output of the DDS will appear in the output of the synthesizer multiplied by the loop division ratio. Thus, the output of the DDS must be bandpass filtered, adding to the synthesizer's complexity.

Although none of the above solutions has yet gained widespread acceptance as a 'good' solution, some of them seem quite promising, and worth further investigation.

3 Frequency synthesizer requirements

The principle of phase-lock was invented a long time ago. The first publication that can be clearly identified as a description of a phase-locked loop is de Bellescize's article "*La Reception Synchrone*", dating back to 1932 [34]. However, there were practically no applications for PLL's until they became necessary in synchronizing the red, green and blue color sweeps in television receivers in the 1940's and 1950's [35][36][37]. Today, phase-locked loops are used in innumerable applications ranging from data regeneration circuits in subscriber line interfaces to frequency synthesizers in microprocessors, radio transceivers, etc. Some very comprehensive books on the theory of phase-locked loops have been published over the years (e.g. [38][39][40][41]). The basic theory will not be discussed in more detail in this work.

This chapter deals with the requirements set on the frequency synthesizer by modern telecommunications systems. The implications of these requirements on the synthesizer design will be viewed from a phase-locked loop point of view, but the actual requirements can be generalized to any kind of frequency synthesizer.

The radio receiver or transmitter, in which the frequency synthesizer is used, is typically a part of a larger radio system. These systems, e.g. GSM, DCS-1800 or Bluetooth, are accurately specified to ensure interoperability between radio units from different manufacturers.

For the receiver, the purpose of the specifications is to ensure that the receiver is able to receive the wanted signal correctly in an environment where other users of the frequency spectrum are causing interference. The specifications typically include the minimum power of the wanted signal that the receiver should still be able to receive correctly ("correctly" in this context meaning reception with a bit error rate (BER) smaller than a specified maximum). Also specified are the interfering signals that the receiver is required to tolerate while still correctly receiving the wanted signal. The interferers can be much higher in power than the wanted signal. For example in the DCS-1800 system, the interfering signal can be as much as 66 dB higher than the wanted signal.

For the transmitter, the purpose of the specifications is to restrict the amount of interference caused by the transmitter to other users of the frequency spectrum, and to ensure that the quality of the transmitted signal is good enough to be received correctly with a receiver fulfilling the specifications of the same system. Typically, the specifications include a *spectral mask*, i.e. the maximum power level of the components of the transmitted spectrum at different offset frequencies. The frequency accuracy of the transmitted signal is also normally specified. Depending on the type of modulation used, a measure of the modulation quality is also specified. In phase modulated systems, e.g. GSM, this is typically the maximum phase error of the actual transmitted signal with respect to the ideal one. In more complex modulation types, the typical measure of modulation quality is error vector magnitude (EVM), which takes into account both the phase error and the amplitude error of the actual transmitted signal with respect to the ideal one.

This chapter will introduce the specifications relevant for frequency synthesizer design in more detail. The translation of the specifications of the radio system to the specifications of the frequency synthesizer will be explained. Most of the examples in this chapter will be based on the specifications for the DCS-1800 system [42]. When the requirement is specific to an OFDM system, the specifications of the IEEE 802.11a wireless LAN system [46] are used.

The output signal of an ideal frequency synthesizer is a pure sinusoid, i.e. a delta function in the frequency domain. The output spectrum of a real synthesizer, however, consists of a number of nonideal components in addition to the sinusoidal component. Figure 3.1 illustrates these components, as well as other parameters, whose specifications will be derived in the following sections.

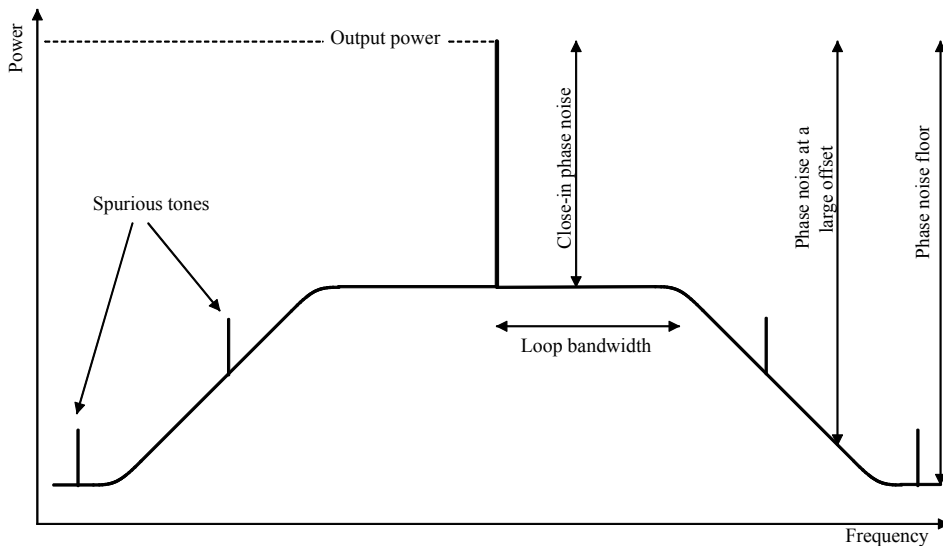


Figure 3.1 Nonideal components in the output spectrum of a PLL frequency synthesizer.

3.1 Functional requirements

The basic requirement set for a frequency synthesizer by any telecommunications system is that the synthesizer must be able to generate all required frequencies with a sufficient accuracy. In other words, the synthesizer must be able to cover the entire frequency range of the system, it must be able to generate the channel frequencies required by the system, and the frequency accuracy of the synthesizer must be good enough.

The frequency range is mainly a design parameter for the VCO and the prescaler. The channel spacing requirement sets the frequency resolution of the synthesizer, and is thus an important parameter in the selection of the synthesizer architecture. The frequency accuracy requirement has different consequences for an integer-N PLL than for a fractional-N PLL. For an integer-N PLL, the accuracy requirement merely sets the limit to when the loop can be considered locked, and thus affects the switching time specification. For a fractional-N PLL, the frequency accuracy requirement may also

come into play in determining the minimum word length of the frequency control word. If the fractional frequencies generated are not exactly coincident with the channel center frequencies, then the frequency resolution must be fine enough to keep the frequency error still within specifications.

In the DCS-1800 system, the frequency range is 1710...1880 MHz, and the channel spacing is 200 kHz. The carrier frequency must be accurate to within 0.1 ppm (171 Hz).

3.2 Phase noise at small offset frequencies

Many of today's telecommunications systems, e.g. GSM, use phase modulation techniques. In these systems, it is essential that the received symbols have a low enough phase error to maintain a useful bit error rate. Therefore, a maximum phase error is normally specified for the transmitted signal. Typically, both root mean square (rms) and peak phase error limits are specified. In the DCS-1800 case, the specified limits are 5 degrees rms, and 20 degrees peak phase error.

In systems employing more complex modulation schemes, e.g. quadrature amplitude modulation (QAM), error vector magnitude (EVM) is used as a measure of modulation quality. Not only phase error, but also amplitude noise, distortion, quadrature mismatch, etc., contribute to the EVM. Therefore, the maximum phase error can not be determined directly from the standards. The specification is a tradeoff between the phase error and other nonidealities.

In the transmitter, the major contributor to the phase error is the frequency synthesizer generating the local oscillator frequency. The close-in phase noise manifests itself as random fluctuations in the phase of the local oscillator signal, which then translate directly to fluctuations in the phase of the transmitted signal, i.e. random phase error.

Let us assume that the frequency synthesizer is a second-order PLL, i.e. the phase noise rolloff is -40 dB per decade for offset frequencies beyond the loop bandwidth. Let us also assume that the phase noise floor of the synthesizer is low enough to be ignored as a contributor to the total integrated noise. This assumption is only valid for narrow band systems, where the PLL bandwidth is only about an order of magnitude smaller than the channel bandwidth. Let us denote the phase noise at small offset frequencies by $L_{close-in}$, the phase-locked loop bandwidth by B_{PLL} , and the channel bandwidth of the system in question by $B_{channel}$. We can now approximate the square of the phase error with

$$\phi_e^2 \approx \int_{-B_{channel}/2}^{-B_{PLL}} L_{close-in} \left(\frac{-B_{PLL}}{f} \right)^4 df + \int_{-B_{PLL}}^{B_{PLL}} L_{close-in} df + \int_{B_{PLL}}^{B_{channel}/2} L_{close-in} \left(\frac{B_{PLL}}{f} \right)^4 df. \quad (3.1)$$

Solving for the close-in phase noise, we get

$$L_{close-in} \leq \frac{3}{8} \frac{\phi_e^2 B_{channel}^3}{B_{PLL} (B_{channel}^3 - 2B_{PLL}^3)} \quad (3.2)$$

Equation (3.2) shows that increasing the PLL bandwidth leads to a tighter specification for the close-in phase noise. In the DCS-1800 system, for example, the channel bandwidth is 200 kHz, and the maximum rms phase error is 5 degrees. In practice, a portion of the total phase error has to be allocated to other sources of error. The maximum close-in phase noise as a function of the PLL bandwidth is plotted in Figure 3.2 for three different values of phase error contribution from the synthesizer.

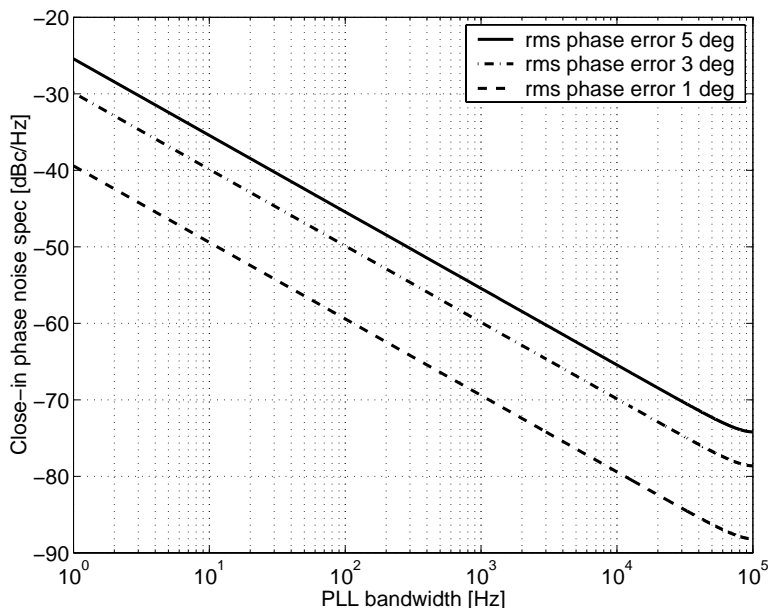


Figure 3.2 The maximum close-in phase noise versus the loop bandwidth for three different rms phase error specifications.

For example, allocating 3 degrees of the total phase error for the frequency synthesizer (the middle curve), and assuming a PLL bandwidth of 20 kHz, which would be a typical value for a DCS-1800 integer-N PLL, the close-in phase noise of the synthesizer has to be below -73 dBc/Hz.

3.3 Phase noise at large offset frequencies

The phase noise of the frequency synthesizer at large offset frequencies is almost always specified. The reason for this is a phenomenon commonly referred to as *reciprocal mixing*. The phase noise tail of the local oscillator signal mixes with undesired interfering signals, and the mixing result ends up at the same intermediate frequency as the wanted signal, thus impairing the signal-to-noise ratio. The reciprocal mixing phenomenon is illustrated in Figure 3.3.

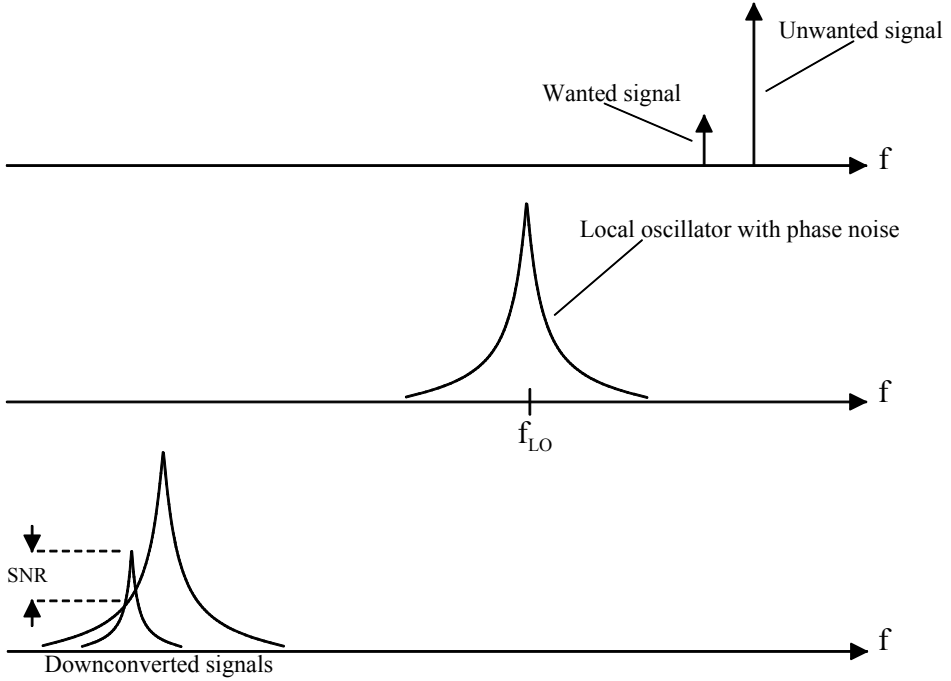


Figure 3.3 Reciprocal mixing.

The spectrum converted to the intermediate frequency can be represented as the convolution of the received RF spectrum and the spectrum of the local oscillator signal (Equation (3.3)).

$$S_{IF}(\omega) = S_{RF}(\omega) \otimes S_{LO}(\omega) \quad (3.3)$$

Since the interfering component can be much stronger than the wanted signal, the phase noise power of the local oscillator at the same offset frequency must correspondingly be much lower to maintain a useful signal-to-noise ratio of the downconverted signal. The specification for the local oscillator power at a given offset frequency can be derived from the power levels of the wanted signal and the interfering signal, and the signal-to-noise ratio required to guarantee signal reception at the desired bit error rate:

$$L(\Delta f) \leq P_{wanted} - P_{unwanted} - SNR_{required} - 10 \cdot \log(B_{channel}) \quad (3.4)$$

The last term of the equation is an approximation, assuming that the mean value of the phase noise over the channel bandwidth can be approximated with the phase noise value at the center point of the channel.

In the DCS-1800 system blocking specifications, the wanted signal is 3 dB over the reference sensitivity level, i.e. at -99 dBm. The largest allowed blocking signals are -43 dBm, -33 dBm, and -26 dBm at offset frequencies of 600 kHz, 1.6 MHz, and 3.0 MHz, respectively. Detecting the GMSK modulated signal with a 0.1% BER requires a signal-

to-noise ratio of approximately 8 dB, and the channel bandwidth is 200 kHz. Inserting these values into Equation (3.4) leads to the phase noise specifications shown in Table 3.1.

Table 3.1: *Phase noise specifications for the DCS-1800 system.*

Offset frequency	Phase noise requirement
600 kHz	-117 dBc/Hz
1.6 MHz	-123 dBc/Hz
3.0 MHz	-134 dBc/Hz

In practice, a few decibels of safety margin have to be added. Phase noise specifications shown in the literature for the DCS-1800 system are typically in the range of -120...-123 dBc/Hz at a frequency offset of 600 kHz.

At large offset frequencies, the phase noise properties of a PLL based frequency synthesizer are normally dominated by the voltage-controlled oscillator, since the noise from the rest of the loop components is lowpass filtered. However, in the case of $\Delta\Sigma$ fractional-N synthesizers, the shaped quantization noise from the $\Delta\Sigma$ -modulator increases with frequency offset, and may dominate over VCO phase noise at large offset frequencies unless properly filtered.

The phase noise specifications shown in Table 3.1, especially the specification at 600 kHz offset frequency, are quite tough for a VCO. State-of-the-art performance examples are -129 dBc/Hz for a discrete VCO [50], and -125 dBc/Hz for an integrated one [51]. Due to the better performance, most cellular products today use discrete VCO's. However, the push towards smaller devices has supported a vast research in the field of integrated VCO's, and the state-of-the-art is fairly close to being commercially usable.

3.4 Phase noise in OFDM systems

In orthogonal frequency division multiplexing (OFDM), the data stream to be transmitted is divided into multiple data streams with lower bit rates. Each low bit rate data stream is then individually modulated on a subcarrier, and the subcarriers are combined to form the OFDM signal. The subcarriers are spectrally orthogonal, i.e. at the center frequency of a subcarrier, all other subcarriers have spectral nulls (see Figure 3.4). Ideally, each subcarrier can then be demodulated with no interference from the other subcarriers. A more comprehensive analysis of the OFDM signals and systems can be found for example in [43].

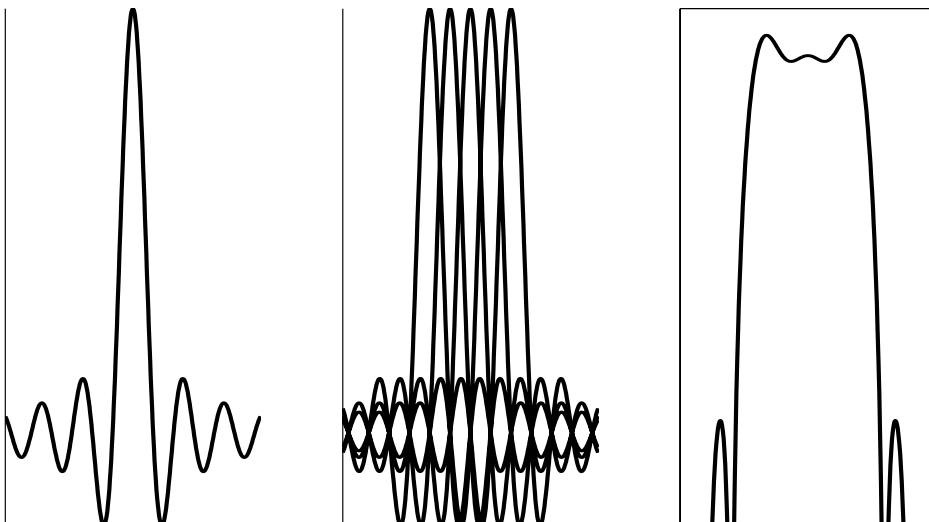


Figure 3.4 A single OFDM subcarrier in frequency domain (left), a combination of multiple subcarriers (middle), and the combined power of the subcarriers in logarithmic scale (right).

In comparison with other modulation types at the same data rate, OFDM signals are extremely tolerant against multipath fading channels, as well as narrowband interferers. However, the FFT and IFFT operations required for modulating and demodulating the OFDM signal are computationally very heavy, and only recent advances in digital technology have made it possible to use OFDM in practical applications. Currently, OFDM is used as the modulation format in the xDSL systems [44], high-definition television (HDTV) systems [45] as well as in the IEEE 802.11a and 802.11g wireless LAN systems [46][47].

One of the largest drawbacks of OFDM is its relatively high sensitivity to phase noise. However, the phase noise of the local oscillator signal affects the OFDM systems in a slightly different way than it affects single-carrier systems. The channels are typically very wide (e.g. 20 MHz in IEEE 802.11a [46]), and thus the mixing of the neighboring channels with the LO phase noise tail is not a problem. Practically any local oscillator will have low enough phase noise at an offset of 20 MHz. The wanted signal, however, now consists of several subcarriers. Phase noise at small offset frequencies ($<10\%$ of the subcarrier spacing) can be considered common to all subcarriers, and is relatively easy to handle by means of tracking techniques or differential detection. Phase noise at larger offset frequencies, however, will introduce inter-carrier interference (ICI), i.e. the subcarriers will not be perfectly orthogonal any more. The mixing products of each subcarrier and the phase noise tail of the LO signal will end up on top of every subcarrier, thus impairing the signal-to-noise ratio of the other subcarriers.

Analytically determining the LO phase noise specification for an OFDM system is not as straightforward as it is for single-carrier systems. In [48], it is assumed that the free-

running (i.e. not phase-locked) local oscillator has a Lorentzian phase noise spectrum given by

$$L(\Delta f) = \frac{1/\pi f_{-3dB}}{1 + \left(\frac{\Delta f}{f_{-3dB}} \right)^2}, \quad (3.5)$$

where f_{-3dB} is the -3 dB bandwidth of the oscillator. It is shown in [48] that the degradation in signal-to-noise ratio caused by the phase noise spectrum of Equation (3.5) can be approximated with

$$D_{SNR} \approx \frac{11}{6 \ln 10} 4\pi f_{-3dB} T \frac{E_S}{N_0}, \quad (3.6)$$

Where $1/T$ is the spacing of the OFDM subcarriers in the frequency domain, and E_S/N_0 depends on the modulation type of the subcarriers.

For the fastest data rate of the IEEE 802.11a WLAN system (54 Mbit/s), the subcarriers are 64-QAM-modulated, requiring an E_S/N_0 of 19dB to achieve a bit error rate less than 10^{-6} . The subcarrier spacing is 312.5 kHz. Using these values, and requiring that the SNR degradation must be negligible (less than 0.1 dB), we can calculate the maximum -3 dB bandwidth of the oscillator to be 39 Hz. According to Equation (3.5), this corresponds to a phase noise of -109 dBc/Hz at an offset of 1 MHz from the carrier.

The Lorentzian phase noise model in [48] assumes a free-running oscillator. In practice, however, the oscillator is always locked to a stable reference frequency by means of a phase-locked loop. The phase noise spectrum will no longer follow the simple Lorentzian model, but will have a shape resembling that in Figure 3.1. A first order approximation for the phase noise specification can be derived by requiring that the total integrated phase noise power of the PLL must be equal to the integrated phase noise power of a Lorentzian oscillator with a bandwidth of 39 Hz. As explained earlier, the phase noise at offsets smaller than 10% of the subcarrier spacing is essentially common to all subcarriers, and does not contribute to the ICI. Therefore, it should also be removed before the integration to get correct results. Integrating Equation (3.5), we get

$$L_{int} = \int_{f_1}^{f_2} \frac{1/\pi f_{-3dB}}{1 + \left(\frac{f}{f_{-3dB}} \right)^2} df = \frac{\pi}{2} \left[\text{atan} \left(\frac{f_2}{f_{-3dB}} \right) - \text{atan} \left(\frac{f_1}{f_{-3dB}} \right) \right] \quad (3.7)$$

Using, again, the IEEE 802.11a WLAN system as an example, the phase noise of the LO signal should thus be integrated from approximately $f_1=30$ kHz (<10% of the subcarrier spacing of 312.5 kHz) to $f_2=20$ MHz (channel spacing). These values result in an integrated phase noise specification of -27 dBc.

For a practical PLL, the total integrated phase noise is a much more useful specification than the bandwidth of the Lorentzian model. The phase noise can easily be measured and integrated to check if the device performance meets the requirements.

In addition to [48], a few other attempts have been made to analytically quantify the effects of the local oscillator phase noise on an OFDM signal. For instance in [49], the LO signal is no longer modeled as a free-running oscillator, but an assumption of a PLL-like phase noise spectrum is used. However, several simplifications and assumptions are still used that degrade the generality of the analysis; the phase noise close to the carrier is not removed, although it will result in a phase error common to all carriers that can be easily corrected for. Also, the analysis does not take into account the fact that the first and the last subcarriers will contribute less to the total noise due to the fact that half of their phase noise will not overlap other subcarriers. This assumption will be reasonably accurate when the number of subcarriers is very large (e.g. 8192 in the HDTV system), but for a smaller number of subcarriers (e.g. 52 in the IEEE 802.11a WLAN standard) the error will be larger. All in all, it can be said that no model accurately and generally predicting the effects of local oscillator phase noise on an OFDM signal has been published to date.

3.5 Spurious tones

Spurious tones are unwanted components in the frequency synthesizer output spectrum that are not noise-like. The VCO is essentially a frequency modulator, and periodic signals at the VCO control line will result in an output signal with discrete FM sidebands.

The requirement for the maximum spurious power derives from the blocking specification of the telecommunications system. A spurious tone at a given offset mixes the neighboring channel at the same offset down to on top of the wanted channel. The spurious power must therefore be low enough to provide an adequate signal-to-noise ratio (SNR) in the output of the receiver.

Telecommunications systems normally have different blocker power specifications for different offset frequencies. Also, the reference sensitivity level and the SNR required depend on the system. In the DCS-1800 system, the wanted signal is 3 dB above the reference sensitivity level of -102 dBm, and the SNR required is approximately 8 dB. The blocker at 600 kHz offset, for example, can be as high as -43 dBm, leading to a maximum spurious power of -64 dBc. Table 3.2 shows the maximum spurious power levels at different offset frequencies for a synthesizer in a DCS-1800 mobile station receiver.

Table 3.2: Spurious power specifications for DCS-1800.

Offset frequency	Maximum spurious power
$600 \text{ kHz} \leq f_{\text{offset}} < 800 \text{ kHz}$	-64 dBc
$800 \text{ kHz} \leq f_{\text{offset}} < 1.6 \text{ MHz}$	-64 dBc
$1.6 \text{ MHz} \leq f_{\text{offset}} < 3.0 \text{ MHz}$	-74 dBc
$f_{\text{offset}} \geq 3.0 \text{ MHz}$	-81 dBc

A number of nonidealities in the PLL itself will generate interfering signals in the VCO control line. All of these phenomena will result in periodic signals at the PLL reference frequency, and thus in spurs at an offset of f_{ref} from the carrier. The dominant spurious-generating nonidealities in a typical PLL are mismatch between the up and down currents in the chargepump and charge injection through the switches in the chargepump. Also, the leakage currents of the chargepump and the VCO may be significant contributors.

Figure 3.5 shows how the mismatch between the up and down currents in the chargepump results in a periodic signal in the VCO control line. In this case, the up current is slightly larger than the down current. The PLL feedback mechanism tries to keep the mean value of the VCO control voltage (V_C) constant, and therefore the down pulses from the phase detector will be slightly longer to compensate for the smaller current. The resulting net output current of the chargepump (I_{CP}) is then low pass filtered in the loop filter. Despite of the filtering, the VCO control voltage still clearly shows a periodic beat at the reference frequency, which will in turn result in spurious tones.

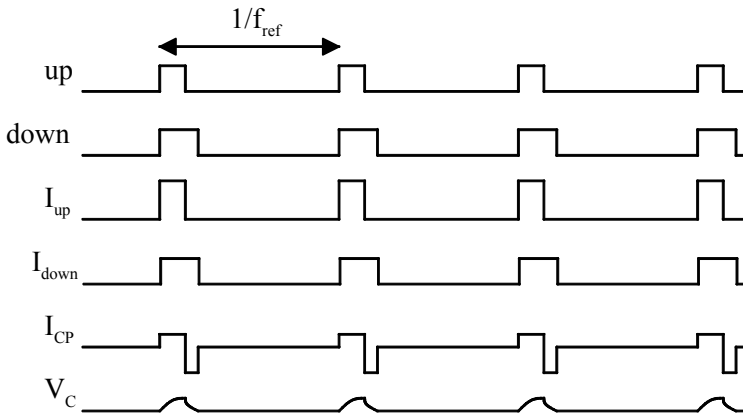


Figure 3.5 Periodic signal generated by the chargepump mismatch.

The charge injection through the chargepump switches is illustrated in Figure 3.6. The digital up and down signals from the phase detector will have relatively fast rise and fall times, and thus harmonic components at very high frequencies. Some of these high-

frequency components will be injected to the chargepump output node through the gate-source and gate-drain capacitances (C_{GS} and C_{GD}) of the switch transistor. The capacitances C_{GS} and C_{GD} depend on the gate-to-source and gate-to-drain voltages V_{GS} and V_{GD} , respectively. Therefore, the charges injected through the up and down switches will depend on the chargepump output voltage. The up and down charges will be equal for one single output voltage value. For all other output voltages, there will be a net charge injected to the output of the chargepump. The PLL will compensate for this excess charge very much in the same way as the chargepump mismatch in Figure 3.5, and a periodic beat at the reference frequency is generated.

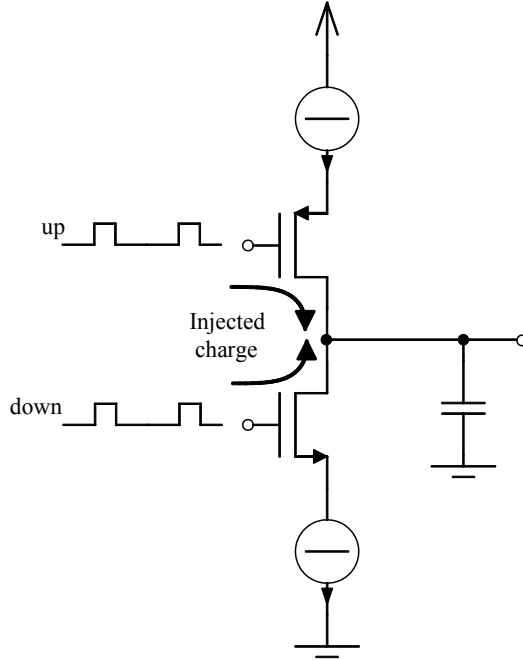


Figure 3.6 Charge injection in the chargepump switches.

The third phenomenon typically generating reference spurs is the loop filter leakage. When the PLL is locked, the chargepump is neither pumping up nor down for most of the time. Ideally, a chargepump in this state represents an infinite impedance towards the loop filter. Likewise, the input impedance of the VCO control node is ideally infinite. In practice, however, both the chargepump switches and the VCO control node (typically connected to a varactor diode) will have finite impedances, and there will be a small leakage current that will change the control voltage of the VCO slightly either up or down. The PLL will compensate for the leakage, and thus a periodic beat at the reference frequency is again generated. In PLL's using a discrete loop filter, the leakage currents are normally not a problem. The loop filter capacitors are very large, and a small leakage current will change the loop filter voltage only negligibly. In fully integrated PLL's, however, the leakage may become a problem, since the loop filter capacitors are significantly smaller due to integration limitations.

Quantifying the mechanisms explained above is very difficult, since the spurious power will depend on the actual shape of the interfering waveform. An approach that is relatively accurate and gives useful insight to the problem is given in [19]. It is first assumed that the disturbance on the VCO control line appears as narrow, rectangular pulses having a width Δt and a height ΔV . Inserting the Fourier series expansion of the rectangular waveform into the time domain representation of the VCO output waveform yields the following equation for the VCO output:

$$v_{out}(t) = V_0 \cos \left[\left(\omega_0 + K_{VCO} \frac{\Delta V \Delta t}{T_{ref}} + K_{VCO} V_{CTRL} \right) t \right] - K_{VCO} \left[V_{CTRL} \sum_{n \neq 0} \frac{a_n}{n \omega_{ref}} \sin(n \omega_{ref} t + \theta_n) \right] \sin \left[\left(\omega_0 + K_{VCO} \frac{\Delta V \Delta t}{T_{ref}} + K_{VCO} V_{CTRL} \right) t \right] \quad (3.8)$$

Equation (3.8) indicates sidebands at $\pm n \omega_{ref}$ from the carrier, where ω_{ref} is the phase comparison frequency. Typical approaches to reducing the problem are using large capacitors in the loop filter (to keep ΔV to a minimum), and minimizing K_{VCO} to minimize the modulation index. However, both remedies have their downsides as well: increasing the loop filter capacitance requires increasing the chargepump current proportionally; K_{VCO} cannot be lowered indefinitely, because the tuning range still needs to cover the desired frequencies plus process, temperature and supply voltage variations.

Table 3.3 shows the reported spurious powers from a few recently published radio frequency synthesizers. Clearly, with a careful design, the spurious specifications of the DCS-1800 system can be met with a margin.

Table 3.3: Spurious power levels of published frequency synthesizers.

Author	Spurious power	Offset frequency	Type
Rategh et al. [52]	-45dBc	11 MHz	Integer-N PLL
Yan et al. [31]	-79.5dBc	1.6 MHz	Dual-loop integer-N PLL
De Muer et al. [53]	-75 dBc (ref spur) -100 dBc (fractional spur)	500 kHz 26 MHz	Fractional-N PLL
This work [P4]	-85 dBc	400 kHz	Fractional-N PLL
Saul et al. [27]	-30dBc	N/A	Direct digital synthesizer

3.6 Harmonic tones

Harmonic tones, i.e. signal components at integer multiples of the carrier frequency, are practically always present at the output of the voltage-controlled oscillator. If the output signal is not perfectly sinusoidal, it will always have some power at the harmonic frequencies. The harmonics as such are seldom a critical design parameter for the

system, since the frequencies are typically far outside the band of interest. However, the harmonic content at the output of the local oscillator does affect the quadrature generation, and thus the harmonics must be kept below a certain limit.

Most modern radio systems require quadrature LO signals, i.e. signals with a 90 degree phase difference with respect to each other, to be generated for both the receiver and the transmitter. Any deviation from exactly 90 degrees will deform the signal constellation, and thus adversely affect the bit error rate of the system. The quadrature signals are typically generated either by a passive RC-CR network or by a divide-by-two circuit, both of which are sensitive to the harmonic content of the input signal.

Perhaps the simplest way to generate quadrature signals is to use a passive RC-CR network, the simplest version of which is depicted in Figure 3.7. The signal in the upper branch is shifted by -45° and the signal in the lower branch by $+45^\circ$, resulting in a phase difference of 90° between the outputs. A single RC-stage gives the desired, symmetrical amplitude and phase response only at a single frequency. Therefore, multistage polyphase filters with wider bandwidth are typically used in practice. However, as shown in [54], the output phase of the polyphase filter is very sensitive to the harmonics of the input signal. Harmonics will shift the zero crossings of the differential signal, thus corrupting the phase relationship of the outputs.

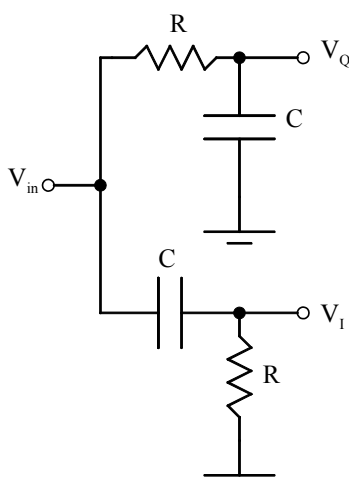


Figure 3.7 A simple RC-CR network generating quadrature signals.

Another frequently used method for quadrature generation is frequency division. Dividing the input frequency by two with a standard master-slave flip-flop will result in signals with 90° phase difference between the master and the slave latch outputs. The major drawback of this technique, however, is the fact that the VCO and the frequency divider now need to run at twice the local oscillator frequency, which will increase the power dissipation of the synthesizer, or may even be impossible due to technology limitations. The phase accuracy is also dependent on the symmetry of both the frequency divider itself and the loads seen by the divider. Any mismatch will introduce a phase error in the output. The frequency division technique is also sensitive to the harmonic

content of the input signal. The phase accuracy is dependent on having an input signal with exactly 50% duty cycle. Any second harmonic present in the VCO output will deviate the duty cycle from 50%, and will thus introduce a phase error. However, if the VCO is on the same chip with the frequency divider, the signal between the two is likely to be differential, and thus it will have a very low second harmonic.

3.7 Settling time

In modern telecommunications systems, the synthesizer often has strict requirements for settling time, defined as the time it takes for the synthesizer to settle to a given accuracy after a frequency step. In time division multiple access (TDMA) systems, the settling time specification is mostly due to the desire to use the same synthesizer for both transmit and receive modes, thus saving power and area. In frequency hopping systems, the relatively frequent changing of the channel frequency is used to make sure that enough packets are received correctly even if a part of the frequency band would be blocked by strong interferers. Independent of the reason for changing the transmit or receive frequency, the system specifications usually set a limit on how fast this needs to be done, and this can be directly translated into a synthesizer settling time requirement.

In the phase-locked loop, being a low-pass control system by nature, the settling time is always inversely proportional to the loop bandwidth. Other constraints, such as stability, reference suppression, and close-in phase noise normally set the upper limit for the loop bandwidth. On the other hand, the settling time specification typically sets the fundamental lower limit.

Using the standard notation of feedback theory, a second-order loop has a closed-loop transfer function of

$$H(s) = \frac{2\xi\omega_n s + \omega_n^2}{s^2 + 2\xi\omega_n s + \omega_n^2}, \quad (3.9)$$

where ξ is the damping factor, and ω_n is the natural frequency. From the step response of the closed-loop transfer function we can derive the minimum required natural frequency for the loop to settle within a given maximum relative frequency error δ (absolute frequency error divided by the total frequency step) in a given switching time t_{sw} to be

$$\omega_n = \frac{-\ln\left(\delta\sqrt{1-\delta^2}\right)}{\xi t_{sw}}. \quad (3.10)$$

Assuming the damping factor ξ to have a value of 0.707 (optimal value in most cases), we can express the minimum loop crossover frequency as

$$\omega_c = \frac{-\ln\left(\frac{\delta}{\sqrt{2}}\right)}{t_{sw}}. \quad (3.11)$$

In a DCS-1800 handset, the maximum frequency step occurs when switching from the lowest transmit channel to the highest receive channel, and is equal to 170 MHz. The frequency has to settle within ± 0.1 ppm, i.e. 180 Hz, in three time slots, i.e. 1730.7 μ s. To leave some margin, we use a switching time requirement of 1500 μ s, resulting in a minimum loop bandwidth of 1.5 kHz.

While the handset settling time requirements are relatively relaxed, a base station synthesizer needs to settle significantly faster. In the worst case, the base station communicates with a different handset during every time slot, having only the guard time between slots (30.5 μ s) for channel switching. Based on Equation (3.11), this would give a minimum loop bandwidth of 462 kHz. However, with a channel spacing of 200kHz, the reference feedthrough requirement typically sets the maximum loop bandwidth to approximately 20kHz. These conflicting requirements call for more complex frequency generation techniques. A typical method in base stations is the so called ping-pong synthesizer. The base station has two separate synthesizers, allowing one to switch to a new channel during a time slot, while the other one is being used. During the slot guard time, the synthesizers switch roles, and during the next slot, the other synthesizer is used.

3.8 Other requirements

In addition to the performance requirements set by the radio system, there are requirements set on the frequency synthesizer by the commercial aspects of the product. Especially in mobile applications, size and battery life time play a very important role in marketing the product. For the IC designer, these requirements can be reduced to power dissipation and external component count.

The battery life time is an increasingly important parameter in mobile applications. For instance in GSM handsets, the typical standby times have increased from 18 hours (Nokia 880) to 430 hours (Nokia 6310) in the last ten years. At the same time, the handsets, and consequently their batteries, have become significantly smaller and lighter. The power that is available to implement a function, for example frequency synthesis, has decreased dramatically.

As the integrated circuits in a mobile device contain larger and larger functional entities, the size of the entire device is more and more determined by the number of external components required by the IC's. For example, the Nokia 6161 cell phone has a printed circuit board area of 40 cm², which contains only 15 integrated circuits but a total of 405 external passive components (232 capacitors, 149 resistors, and 24 inductors) [55]. It is obvious that the board area and thus the minimum achievable phone size is determined by the number of passives, not the number of IC's. Therefore, minimizing the number of external components should be a very important design target in any IC design project.

4 Fractional-N phase-locked loops

Conventional integer-N PLL synthesizers divide the output frequency by an integer number to produce the phase comparison frequency. Consequently, the output frequency can only be an integer multiple of the phase comparison frequency. This limitation can be very troublesome in some applications, as will be further explained in Section 4.1.

A solution to the problems posed by the integer division is the fractional-N phase-locked loop. In a fractional-N loop, the divisor N is not constant, but varies between integer values in such a way that the average divisor can be a fractional number. This approach has several advantages that are discussed in Section 4.2.

Although the fractional division eliminates some of the problems caused by integer division, it also creates new problems. These will be discussed in Section 4.3, and some proposed solutions to these problems in Section 4.4.

4.1 Problems of integer-N synthesizers

In most digital telecommunications systems, the channel spacing is very small compared to the carrier frequency, e.g. 200 kHz in GSM and DCS-1800, or 25 kHz in the Japanese PDC system. To be able to synthesize all the required channel frequencies, the reference frequency of an integer-N synthesizer must be equal to or smaller than the channel spacing. This leads to very high values for the divisor N . For example in the DCS-1800 system, the carrier frequency is between 1710 and 1880 MHz, resulting in N varying from 8550 to 9400.

The large division ratio leads to a need for an extremely high quality reference. The noise transfer function from the reference to the output multiplies the reference noise by N at offset frequencies smaller than the loop bandwidth. An N of 9400 means that the reference noise close to the carrier is amplified by almost 40dB. To make sure that the reference oscillator does not dominate the performance of the entire synthesizer, its specifications must be at least 50-60dB tougher than the specifications for the voltage-controlled oscillator. In practice, this means that the reference must be a high-quality crystal oscillator. The noise of the phase detector is amplified by the same factor as the reference noise, and therefore the phase detector noise must be very low as well. However, phase detectors are typically not very noisy, and the crystal oscillator noise normally always dominates over the phase detector noise.

The fact that the reference frequency must be very low leads to several difficulties. In all real PLL's the reference frequency is to some extent fed through to the output, causing spurious tones at offsets of $\pm n \cdot f_{ref}$ from the carrier frequency. These spurious tones lie in the middle of the adjacent channels, and thus must be suppressed as much as possible. To guarantee enough of suppression, the loop bandwidth must be kept below approximately one tenth of the reference frequency.

When switching from one channel to another, the switching time of the synthesizer is inversely proportional to the loop bandwidth, i.e. the smaller the loop bandwidth, the longer the switching time. Together, the specifications for the reference suppression and

the switching time strongly limit the choice of the loop bandwidth. The bandwidth must be small enough to suppress the reference feedthrough. On the other hand, the loop bandwidth must be large enough to allow fast switching. In some systems, the range of possible loop bandwidths between these bounds can be very small or even nonexistent.

Even more serious problems arise in larger systems, where two or more telecommunications standards are implemented in the same unit. In a standalone GSM solution, for example, the crystal oscillator frequency is always an integer multiple of the channel spacing. Thus, the phase comparison frequency can be generated by a simple digital divider. However, when implementing for example Bluetooth capability in a US-CDMA cellular phone, the crystal frequencies are fundamentally incompatible (13 MHz for Bluetooth and 19.68 MHz for US-CDMA). For cost reasons, it would be highly beneficial to have only one crystal oscillator in the system, but if the frequency synthesizers for both Bluetooth and CDMA are integer- N , this is not possible.

These problems, although usually not insurmountable, limit the applicability of the conventional integer- N synthesizer. The most well accepted solution to these problems is the fractional- N architecture.

4.2 Advantages of fractional- N over integer- N

In a fractional- N phase-locked loop, the division ratio N is switched between two or more integer values in such a way that the *average* value of N can be a fractional number. Consequently, the phase comparison frequency can be much higher than in integer- N synthesizers, and thus the division ratio can be much lower. For example in the DCS-1800 system, a phase comparison frequency of 13 MHz would result in N ranging from 131 to 145. A channel spacing of 200 kHz then requires the ability to change the division ratio in steps of $200/13000 \approx 0.0154$.

A reference frequency of 13 MHz, or 65 times higher than in the integer- N synthesizer, also (theoretically) enables up to 65 times higher loop bandwidth. This in turn results in up to 65 times faster switching. In practice, however, the maximum loop bandwidth is limited by factors other than the reference feedthrough, and cannot be increased as much. Still, the designer now has more freedom in choosing the loop bandwidth. If, for example, a very good reference suppression is required, the loop bandwidth can be made significantly smaller while still meeting the switching time requirements. In short, using a fractional- N PLL instead of an integer- N one loosens the coupling between the choice of loop bandwidth and the choice of the reference frequency.

Also, since the division ratio is smaller than in integer- N synthesizers, the phase noise of the reference oscillator is not amplified as much. In the above example, the reference frequency was increased from 200 kHz to 13 MHz. This reduces the amplification of the crystal oscillator phase noise in the DCS-1800 system from 40dB to 22dB.

4.3 Problems of fractional- N synthesizers

The main source of problems in fractional- N synthesizers is the fact that although the *average* division ratio is a fractional number, the *instantaneous* division ratio must still always be an integer. In practice, the fractional division is typically performed by using

an accumulator, i.e. a digital adder that adds a fraction F of its full scale value to its contents once every reference clock cycle. During the accumulation, the prescaler divides its input frequency by N . Every time the accumulator overflows, the prescaler divides by $N+1$ for one cycle. The average output frequency will now be

$$f_{out} = (N + F)f_{ref}. \quad (4.1)$$

During the accumulation, the divided VCO frequency seen at the phase detector input is

$$f_{VCO} = f_{ref} + \frac{F}{N} f_{ref}. \quad (4.2)$$

On the other hand, the reference frequency seen at the other phase detector input is always f_{ref} . Thus, the phase error at the input of the phase detector increases at a rate of

$$\Delta\theta_e(t) = 2\pi \frac{F}{N} \frac{t}{T_{ref}}. \quad (4.3)$$

When an overflow occurs in the accumulator, the prescaler divides by $N+1$ for one period, corresponding to a 2π decrease in the phase error at the phase detector input. The resulting phase error has a sawtooth shape.

The sawtooth shaped phase error, also known as a “beat note”, causes spurious tones in the output spectrum at offsets of $\pm K \cdot F f_{ref}$, where $K = \{0, 1, 2, \dots\}$, i.e. at integer multiples of $F f_{ref}$. These spurious tones, having a large energy in a very small bandwidth, are well above the phase noise of the PLL, causing significant problems in almost all applications. What magnifies the problem is the fact that spurs occur at fractional multiples of f_{ref} , i.e. they can occur well within the channel bandwidth, and inside the PLL bandwidth as well.

4.4 Spur cancellation techniques

Only the very first implementations of the fractional-N divider [57] operated as above. The spurious tones limit the performance of the synthesizer so much that it is practically unusable in most applications. Different methods to eliminate the sawtooth phase error, and thus the spurs, have been presented in the literature. These methods will be discussed in the following subsections.

4.4.1 Analog compensation

The first proposed means of correcting the sawtooth phase error was injecting an opposite ramp signal somewhere in the loop so that the sawteeth cancel each other. In the first fractional-N synthesizer publication [58], the synthesizer has two identical digital accumulators, one controlling the prescaler modulus, and the other one controlling a “sideband reduction circuit”. The sideband reduction circuit generates a sawtooth signal with an opposite polarity than the sawtooth at the input of the phase

detector. This correction signal is then added to the VCO control voltage node. Ideally, the VCO control voltage is now constant when the loop is in lock.

In [56], the beat note compensation is applied to the input of the loop filter. A compensating precision current source is used in parallel with the chargepump. Since the beat note frequency is always the same with a given fractional part, the fractional divider input word can be directly used to control the compensating current source. Again, the arrangement ideally cancels the beat note, and no spurs should occur.

In both of the solutions mentioned above, precision analog components are needed. In [58], the accumulator output is fed to a frequency discriminator that controls the ramp generator. Any error in the frequency discrimination, or any mismatch between the actual loop and the compensating ramp generator will immediately result in an imperfect cancellation of the beat note, and thus spurious tones will reappear in the output spectrum. In [56], the accuracy of the compensating current sources directly affects the quality of the cancellation. Any error will again result in spurious tones. Controlling the compensation signal with the D/A converted output of the accumulator has also been proposed [59]. Again, any inaccuracy of the D/A converter will result in the spurs reappearing in the output spectrum.

All of the approaches described above, although ideally perfect, are very difficult to implement in a mass production integrated circuit. The large production quantities prevent individual tuning of the circuits, and the process variations in the high precision analog parts will result in a far too imperfect cancellation of the beat note signal. However, in some commercial applications with extremely high performance requirements, these techniques have been used (e.g. [60]).

4.4.2 Dithering

The spurious tones in the output frequency are a result of the periodicity of the beat note signal. Intuitively, breaking this periodicity somehow would then reduce the spurs. The simplest way to affect the periodicity is to dither the input of the accumulator [61]. Dithering is performed by adding a small pseudorandom signal to the accumulator input word. This causes small variations in the period of the sawtooth ramp, and consequently breaks the energy of the spurious tones to a number of offset frequencies. Thus, a single tone has much smaller energy than without dithering. If the dithering is strong enough, no tones can be distinguished, but the energy is spread over the entire frequency range. However, the total noise power integrated over the entire bandwidth of interest is larger than without dithering, since dithering essentially means adding noise to the input signal.

Another spur reduction method comparable to dithering is to select suitable initial values for the accumulators. In [62], the specific initial value for each output frequency is looked up in a read-only memory (ROM). The initial values are chosen so that the spurious tones occur at offset frequencies suitable for the application. This method has a very limited application range, and it is certainly not usable in telecommunications applications. Moreover, the synthesizer is not at all flexible, at least the ROM contents have to be redesigned for each new application.

4.4.3 $\Delta\Sigma$ -modulation

Although the first published work used the compensation methods described above, almost all of the recently published fractional-N PLL's use $\Delta\Sigma$ -modulation to eliminate the fractional spurs. The basic principles of the digital $\Delta\Sigma$ -modulation will be presented in the following.

4.4.3.1 Fundamentals

The accumulator used to control the modulus of the prescaler can be viewed as the digital counterpart of a first-order analog $\Delta\Sigma$ -modulator. Figure 4.1 shows the accumulator, i.e. an adder with a one clock cycle delay in the feedback path, with the corresponding signals. The frequency control word is fed into the A input, and added to the B input to produce a sum output Σ . When the adder overflows, the carry out bit c is set.

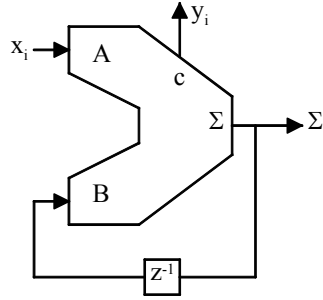


Figure 4.1 The digital accumulator with the corresponding input and output signals.

Let us denote the frequency control signal fed to input A by x_i , and carry output c of the accumulator by y_i . When an overflow occurs, the contents of the accumulator are “flipped over”, which can be viewed as subtracting the full scale of the accumulator from its contents.

The output of the accumulator at an arbitrary time is the sum of its input at that time and its contents one clock period earlier. If an overflow occurs, the full scale of the accumulator is subtracted. The output can thus be expressed as

$$\Sigma_i = x_i + \Sigma_{i-1} - y_i \quad (4.4)$$

$$\Leftrightarrow y_i = x_i + (\Sigma_{i-1} - \Sigma_i) \quad (4.5)$$

$$\Leftrightarrow y_i = x_i - (\Sigma_i - \Sigma_{i-1}). \quad (4.6)$$

The z -transformation of Equation (4.6) is

$$Y(z) = X(z) - \Sigma(z)(1 - z^{-1}) \quad (4.7)$$

Let us now look at the signal flow diagram of a first-order analog $\Delta\Sigma$ -modulator shown in Figure 4.2. The input is again denoted by x , and the output by y . The operation performed in the dashed box is the quantization, and e denotes the quantization error.

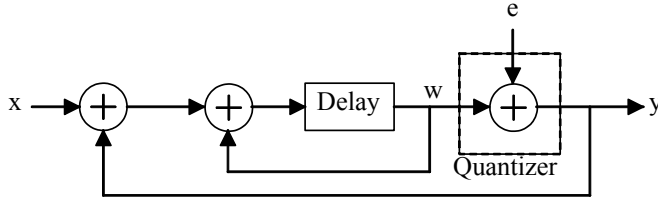


Figure 4.2: The signal flow diagram of a first-order analog $\Delta\Sigma$ -modulator.

The above modulator is described by the following equations:

$$\begin{aligned} w_i &= w_{i-1} + x_{i-1} - y_{i-1} \\ y_i &= w_i + e_i \end{aligned} \quad (4.8)$$

Combining these two, we get

$$y_i - e_i = y_{i-1} - e_{i-1} + x_{i-1} - y_{i-1} \quad (4.9)$$

$$\Leftrightarrow y_i = x_{i-1} + (e_i - e_{i-1}). \quad (4.10)$$

The z-transformation of Equation (4.10) is

$$Y(z) = X(z)z^{-1} + E(z)(1 - z^{-1}) \quad (4.11)$$

Comparing Equation (4.7) with Equation (4.11) shows great similarity. Ignoring the latency of one clock period in the signal path of the analog $\Delta\Sigma$ -modulator, and treating the contents of the digital accumulator as the negative of the quantization error, the equations are identical.

The analogy between the digital accumulator and the analog $\Delta\Sigma$ -modulator is very useful. A vast amount of papers and books have been published on $\Delta\Sigma$ -modulators (e.g. [63][64]), and their well-known properties can be almost directly applied to digital accumulators as well.

A $\Delta\Sigma$ -modulator shapes the quantization noise in a high pass fashion. In other words, the quantization noise is pushed to higher frequencies, and the signal-to-noise ratio at low frequencies can be very high. Figure 4.3 shows the output spectrum of an analog first-order $\Delta\Sigma$ -modulator with a low frequency input.

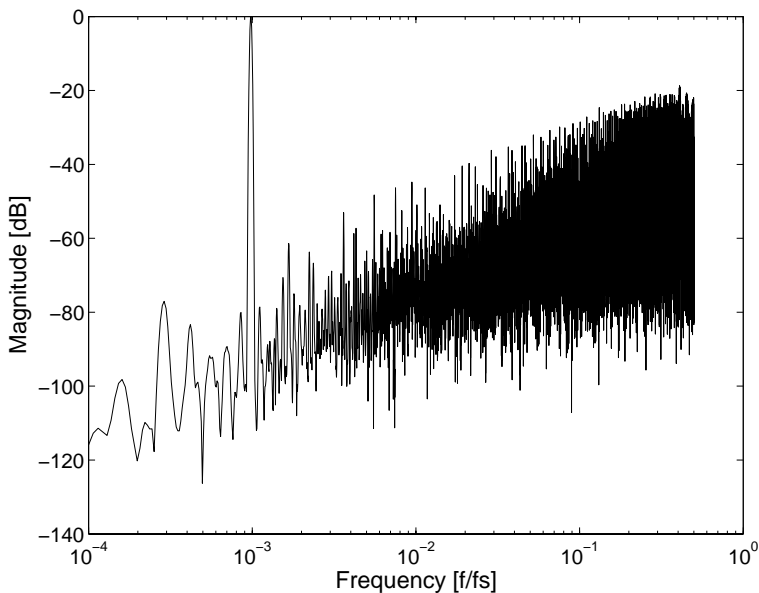


Figure 4.3: *The output spectrum of an analog $\Delta\Sigma$ -modulator with a low-frequency input signal.*

Looking at Figure 4.3, it would seem that the quantization noise is originally white, and then shaped into higher frequencies. The white noise assumption, however, holds only for “sufficiently busy” input signals. In fractional-N synthesizers, the input signal is normally constant, and the quantization noise is no longer white [65]. The quantization noise power is concentrated into a finite number of spurious tones. The spurious performance combined with the relatively poor noise shaping (20dB/decade) make the first order $\Delta\Sigma$ -modulator quite useless in practical applications.

4.4.3.2 Cascaded (MASH) modulators

As explained above, the spurious tones at the output of the modulator result from the input being DC. The signal in the Σ -output of the accumulator, however, is no longer at DC, although it is periodical. Now, this signal can be fed into the input of another accumulator, whose output will be much less periodic than the output of the first accumulator. Combining the c outputs of the two accumulators in a suitable way (see Figure 4.4), the quantization noise of the first accumulator can be canceled.

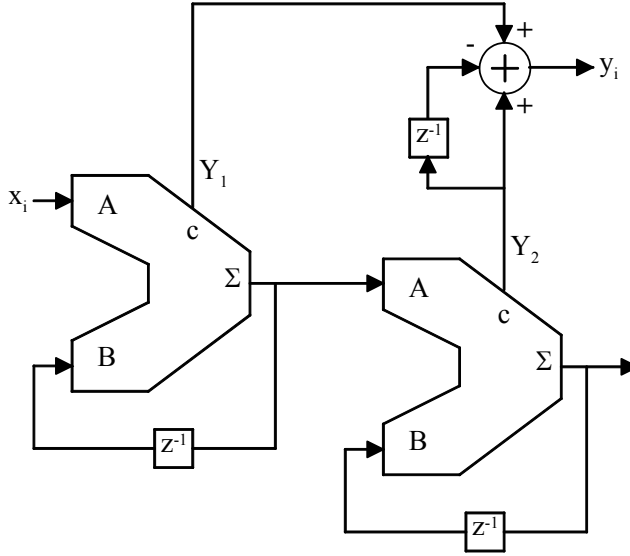


Figure 4.4: The block diagram of a second-order MASH modulator.

As shown in Equations (4.4) to (4.7), the output of the first accumulator is

$$Y_1(z) = X(z) - \Sigma_1(z)(1 - z^{-1}) \quad (4.12)$$

Feeding the Σ -output of the first accumulator into the input of the second one, the output of the second accumulator is

$$Y_2(z) = \Sigma_1(z) - \Sigma_2(z)(1 - z^{-1}) \quad (4.13)$$

Combining the outputs of the accumulators as shown in Figure 4.4, we get the following as the output of the entire modulator:

$$Y(z) = Y_1(z) + Y_2(z) - Y_2(z)z^{-1} \quad (4.14)$$

$$\Leftrightarrow Y(z) = Y_1(z) + Y_2(z)(1 - z^{-1}) \quad (4.15)$$

$$\Leftrightarrow Y(z) = X(z) - \Sigma_1(z)(1 - z^{-1}) + \Sigma_1(z)(1 - z^{-1}) - \Sigma_2(z)(1 - z^{-1})^2 \quad (4.16)$$

$$\Leftrightarrow Y(z) = X(z) - \Sigma_2(z)(1 - z^{-1})^2. \quad (4.17)$$

As Equation (4.17) shows, the quantization noise of the first accumulator cancels out. This greatly improves the spurious performance of the modulator, since the first accumulator is the one with the more periodical output. Also, as Equation (4.17) shows,

the noise transfer function is now a second-order highpass function. Thus, the signal-to-noise ratio at low frequencies is higher than in a first-order modulator.

This concept, called the cascaded modulator or the MASH modulator, was first introduced by Matsuya et al [66]. MASH modulators of any order are unconditionally stable if individual modulators comprising the MASH are stable. In this case, the individual modulators are first-order ones, and thus always stable. Hence, the order of the MASH modulator can be increased at will without causing any stability problems.

In digital $\Delta\Sigma$ -modulators, increasing the order of the modulator improves the spurious performance and the low-frequency SNR basically unrestrictedly. However, a higher-order noise transfer function of the modulator causes problems in the design of the loop filter. The quantization noise of the modulator is pushed to higher frequencies, and rises with frequency at a rate of 20 decibels per decade per modulator order. For example, the quantization noise of a third-order modulator rises at a rate of 60 dB/decade. To suppress this noise, the loop filter rolloff must be at least the same. Thus, the loop filter required in a loop with a third-order modulator must be at least third-order, too.

4.4.3.3 *Multibit single-loop modulators*

In an integer-N PLL, the division ratio N is constant. When the loop is in lock, only nonidealities in the loop (leakage currents etc.) will cause phase errors at the input of the phase detector. That is, the instantaneous phase error that the loop typically corrects for is very small. In a fractional-N PLL, on the other hand, the division ratio is constantly changing, and the loop is actually never properly locked. The instantaneous phase error at the input of the phase detector can vary as much as ± 10 degrees [53]. A large instantaneous phase error results in a longer chargepump on-time, which in turn results in a larger noise contribution from the chargepump (current source noise, power supply noise, etc.), and thus a higher close-in phase noise. Moreover, nonlinearities in the phase detector and the chargepump, i.e. in the conversion from phase difference to chargepump current, will cause the fractional spurs and noise from around $f_{ref}/2$ to fold back to low offset frequencies.

These considerations, especially the large variation of the instantaneous phase error, have directed researchers towards using alternative modulator topologies. While the MASH modulator topology was clearly dominant in the early $\Delta\Sigma$ fractional-N PLL's, multibit single-loop modulators have gained acceptance in the last 2-3 years. The multibit $\Delta\Sigma$ -modulator (an example shown in Figure 4.5) results in a smaller spread of instantaneous phase error (e.g. ± 5 degrees for multibit vs. ± 10 degrees for MASH in [53]), and has hence potential for lower overall close-in phase noise of the synthesizer. The multibit modulator also shapes the noise slightly differently than the MASH modulator: the MASH modulator has better SNR properties at low frequencies, but the multibit modulator exhibits lower noise at high frequencies. The lower high-frequency noise is a clear benefit if the downconversion of noise around $f_{ref}/2$ to low frequencies is an issue.

A few fractional-N synthesizers with direct modulation capabilities have been published [67][68][69]. Table 4.1 shows the key features in each one. In [68], the limitation of the loop bandwidth is further reduced by high-pass filtering the data before applying it to the PLL. The overall transfer function for the data is now flat, whereas all other perturbations are treated just as in an ordinary PLL. The drawback in this implementation is that the lowpass filtering is analog, and the highpass filtering is digital. Matching the corner frequencies of these filters in a mass production IC will be very difficult.

Table 4.1: *Performance comparison of published synthesizers with modulation capabilities.*

Author	Frequency	Modulation	Power dissipation	Technology
Filiol et al. [67]	902-928MHz	GMSK	32.1 mW	BiCMOS/CMOS, linewidth not available
Perrott et al. [68]	1.8GHz	GFSK, 2.5Mbps	27 mW	0.6 μ m CMOS
Pamarti et al. [69]	2.4GHz	GFSK, 1Mbps	88mW	0.18 μ m CMOS

The direct modulation of the frequency synthesizer seems to be a viable solution, and should result in power savings in many applications, as the usually quite power hungry upconversion mixer can be omitted.

5 PLL building blocks

Since phase-locked loops have been around for decades, most of the published PLL's were built with discrete components. Only recently, integrated PLL's have taken over. This section will review the published implementation possibilities of different PLL building blocks with the focus on integrated or integrable solutions.

5.1 Prescaler

As shown in the previous chapter, the output frequency of the phase-locked loop synthesizer is $f_{out} = Nf_{ref}$. Thus, with a fixed reference frequency, the controllability of the output frequency depends on the controllability of the division ratio N . Complete programmability of N in an arbitrary range is easily implementable with standard CMOS logic. However, if the output frequency is high, e.g. in the gigahertz range, implementing the divider completely in standard CMOS logic is not possible. Therefore, a simple prescaler is usually used in the front to lower the operating frequency of the actual programmable divider.

5.1.1 Fixed modulus prescalers

The simplest implementation of the prescaler is a fixed modulus high-speed divider. A high-speed architecture is used to lower the frequency to some extent before the actual programmable divider. However, dividing the output frequency by a fixed factor A means that N can only be chosen in steps of A , limiting programmability.

The limited programmability could, of course, be compensated for by decreasing the reference frequency by the same factor, but this would have some very detrimental effects on the overall performance of the synthesizer. Using a lower reference frequency would force the loop bandwidth to be smaller, too, resulting in slower settling of transients and worse suppression of the VCO phase noise. Also, with a given output frequency, lowering the reference frequency would force the division ratio N to be higher. The noise of the reference oscillator, the phase detector, the chargepump, and the loop filter is seen in the output multiplied by N . Thus, increasing N would significantly tighten the requirements for the rest of the PLL building blocks.

In spite of all the abovementioned problems, the fixed modulus prescaler is used in some extremely high-frequency applications. Adding any programmability to the divider inherently lowers the maximum reachable speed. Thus, a fixed divide-by-two structure is always the fastest divider that can be constructed in a given technology. Consequently, fixed modulus prescalers have been used in extremely high-frequency applications, but also as speed demonstrators for new technologies. Performances of some recently published fixed modulus prescalers are compared in Table 5.1.

Table 5.1: Comparison of recently published fixed modulus prescalers.

Author	Modulus	Maximum frequency	Power dissipation	Supply voltage	Technology
Kurisu et al. [68]	16	28 GHz	590 mW	5 V	Si bipolar, $f_T = 40$ GHz
Fujishima et al. [71]	2	2.5 GHz	150 μ W	2 V	0.1 μ m SOI CMOS
Razavi et al. [72]	2	13.4 GHz	28 mW	2.6 V	Partially scaled 0.1 μ m CMOS
Wang [73]	2	16.8 GHz	3 mW	1.8 V	0.25 μ m CMOS
Wurzer et al. [74]	2	53 GHz	303 mW	6.3 V	SiGe bipolar, $f_T = 80$ GHz
Knapp et al. [75]	2	25 GHz	44 mW	1.5 V	0.12 μ m CMOS
Lee et al. [76]	4	40 GHz	31mW	2.5 V	0.18 μ m CMOS
Wong et al. [77]	2	5.2 GHz	2.5 mW	1 V	0.35 μ m CMOS

5.1.2 Dual modulus prescalers

Because of the many drawbacks of the fixed modulus prescalers, a vast majority of the practical prescalers use the principle of dual-modulus division. Now, the actual programmable divider is used to switch the modulus of the prescaler between two consecutive values, e.g. between 64 and 65. If the programmable divider divides by C , and the prescaler is made to divide by $(P+1)$ for A cycles and by P for the rest $(C-A)$ cycles, the total division ratio will be

$$N = A(P+1) + (C - A)P = CP + A. \quad (5.1)$$

The dual-modulus division limits the range of possible division ratios, as Equation (5.1) only holds as long as $C > P$. This, however, is not a problem in most cases, as the range of necessary output frequencies is far more limited than this.

Having two possible moduli instead of one increases the complexity of the prescaler only slightly, and none of the problems of increasing N and decreasing the reference frequency occur in this case. Consequently, the dual-modulus prescaler is almost always preferred over the fixed modulus prescaler.

5.1.2.1 Conventional dual modulus architecture

Conventionally, the dual modulus prescaler has been implemented by using a synchronous divide-by-4/5 stage followed by asynchronous divide-by-two or divide-by-

four stages. The modulus of the divide-by-4/5 stage is controlled by the outputs of the asynchronous stages and the modulus control input signal in such a way that the total modulus of the prescaler can be switched between two consecutive integer values. The conceptual block diagram of a complete 64/65 dual-modulus prescaler is shown in Figure 5.1.

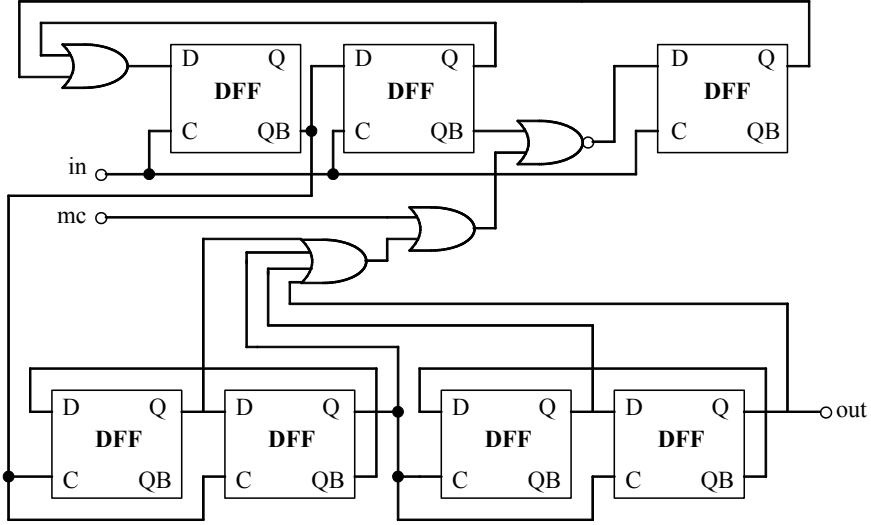


Figure 5.1: The schematic of a conventional dual-modulus prescaler.

The synchronous divide-by-4/5 stage operates as follows: if the control signal from the asynchronous block is low, the loop is closed over two flip-flops, causing the stage to divide by four. When all the outputs of the asynchronous counters and the modulus control input signal are high, the control signal to the synchronous stage goes high, causing the loop to close momentarily over three flip-flops instead of two. This makes the stage divide by five instead of four for one period. In practice, the timing of the feedback signal from the asynchronous dividers can be critical, and special attention must be paid to the design of the OR-gates in the feedback path.

The maximum operating frequency of this prescaler is naturally limited by the synchronous divide-by-4/5 stage, since the rest of the circuit operates with a speed of one fourth of the input frequency, or lower. Compared with a fixed divide-by-two stage, the OR and NOR gates in the signal path inevitably slow down the operation. For example in [84], a comparison between a fixed divide-by-two stage and a divide-by-2/3 stage shows an 11% decrease in maximum operating frequency (from 1.57 GHz to 1.40 GHz).

The division between synchronous and asynchronous stages used above is not the only possible one. Synchronous divide-by-8/9 stages have also been used, but a divide-by-4/5 is the most common solution. The main reason for this is the power dissipation. All the flip-flops and gates in the synchronous stage have to operate at the full input frequency, and thus their number must be as small as possible to minimize the power dissipation of the prescaler.

Some of the recently published prescalers based on the conventional architecture are compared in Table 5.2.

Table 5.2: Comparison of recently published dual modulus prescalers based on the conventional architecture.

Author	Modulus	Maximum frequency	Power dissipation	Supply voltage	Technology
Yang et al. [78]	128/129	1.80 GHz	52.9 mW	5 V	0.8 μm CMOS
Mizuno et al. [79]	128/129	1.16 GHz	4.9 mW	3 V	Si bipolar, $f_T = 28$ GHz
Cong et al. [80]	128/129	4.2 GHz	95 mW	3.5 V	0.4 μm CMOS
Seneff et al. [81]	64/65	1.5 GHz	2.41 mW	2.6 V	0.8 μm Si bipolar
Ohhata et al. [82]	256/258	4.5 GHz	100 mW	3 V	0.5 μm GaAs FET
Maemura et al. [83]	128/129	1.1 GHz	25 mW	5 V	1.0 μm GaAs FET
Rogenmoser et al. [84]	8/9	1.16 GHz	45 mW	5 V	1.2 μm CMOS
Rogenmoser et al. [85]	64/65	1.4 GHz	34.5 mW	5 V	1.2 μm CMOS
Kado et al. [86]	128/129	2.0 GHz	7.2 mW	2 V	0.4 μm SOI CMOS
Foroudi et al. [87]	15/16	1.5 GHz	13.2 mW	5 V	1.2 μm CMOS
Chang et al. [88]	128/129	1.22 GHz	25.5 mW	5 V	0.8 μm CMOS
Larsson [89]	8/9	1.90 GHz	38 mW	5 V	0.8 μm CMOS
Maeda et al. [90]	256/258	14.5 GHz	22 mW	0.6 V	0.2 μm $n\text{-AlGaAs}/i\text{-InGaAs}$ IS ³
Singh et al. [91]	10/11	2.4 GHz	15 mW	1.2 V	0.7 μm GaAs FET

5.1.2.2 Phase switching architecture

In the conventional dual-modulus divider architecture, the number of blocks operating at the full input frequency is quite high, resulting in a high power dissipation. In 1996, Craninckx et al. presented a new prescaler architecture that uses only one flip-flop at the full input frequency (see Figure 5.2) [92].

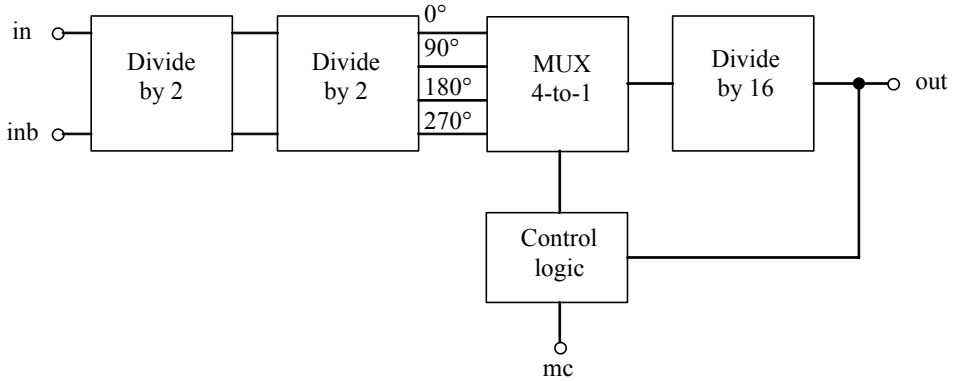


Figure 5.2: The block diagram of the phase switching prescaler.

The phase-switching architecture makes use of the internal structure of the D flip-flop. A divide-by-two stage is usually a flip-flop consisting of two latches, a master latch and a slave latch. The outputs of these latches have a 90 degree phase difference with each other. Now, the second divide-by-two flip-flop has four outputs: the “usual” D flip-flop outputs after the slave latch (0° and 180°), and the quadrature outputs after the master latch (90° and 270°).

Modulus 64 is accomplished by selecting one of the signals at the output of the second divide-by-two flip-flop (e.g. the 0° signal), and dividing this signal further by 16. The total modulus will thus be $4 \cdot 16 = 64$.

Modulus 65 is accomplished by switching the signal directed to the divide-by-16 stage once per output period. The switching is done so that the selected new signal always lags the previous one by 90° , e.g. from the 0° signal to the 90° signal. Switching 90 degrees forward at one fourth of the input frequency corresponds to switching 360 degrees forward at the input frequency, i.e. swallowing one input pulse. If one input pulse is swallowed once per output period, the final modulus will be $(4 \cdot 16) + 1 = 65$.

A downside of the phase switching prescaler architecture is that mismatches in the second divide-by-two stage will result in spurious tones at the output. If the actual phases of the output signals are not exactly 0° , 90° , 180° and 270° , but for example 0° , 89° , 180° and 179° , a spurious tone will appear at a fraction of the output frequency. This problem can be minimized, however, with careful design and layout.

Recently published dual modulus prescalers based on the phase switching architecture are compared in Table 5.3.

Table 5.3: Comparison of recently published dual modulus prescalers based on the phase switching architecture.

Author	Modulus	Maximum frequency	Power dissipation	Supply voltage	Technology
Craninckx et al. [92]	128/129	1.75 GHz	12 mW	3 V	0.7 μ m CMOS
Shu et al. [94]	15/16	3.5GHz	8mW	2.5V	0.35 μ m CMOS

5.1.3 Multiple modulus prescalers

In fractional-N frequency synthesizers, the modulus of the prescaler must often be controllable over a wider range than only two consecutive values. The modulus control could be for example a three-bit word, which would require a prescaler that has $2^3 = 8$ possible moduli.

The phase-switching architecture presented above is well suited also for multiple modulus prescalers. Instead of switching the selected phase just once per output period, it can be switched more often, resulting in a larger number of swallowed input pulses, and thus a larger total modulus.

The selected phase could in principle be switched at one fourth of the input frequency, enabling for example a 16-modulus prescaler with moduli 64...79. This is not, however, usually necessary, and as it results in a more complex phase-switching logic, the number of moduli should be kept as small as possible for a given application.

Multiple modulus prescalers can also be based on the conventional architecture. If the asynchronous divide-by-two or divide-by-four stages are replaced with divide-by-2/3 or divide-by-4/5 stages, the total modulus can be programmed almost at will. For example in [68], the prescaler has 64 moduli (32...63.5 in steps of 0.5).

Recently published multiple modulus prescalers are compared in Table 5.4.

Table 5.4: Comparison of recently published multiple modulus prescalers.

Author	Modulus	Maximum frequency	Power dissipation	Supply voltage	Technology
Craninckx et al. [93]	64...71	1.99 GHz	12 mW	3 V	0.4μm CMOS
Perrott et al. [68]	32...63, step 0.5	1 GHz	22 μW	3 V	BiCMOS
Tiebout et al. [95]	212...217	13GHz	40 mW	1.5V	0.13μm CMOS
This work [P3]	64...71	2.1 GHz	12.5 mW	2.7V	0.35μm CMOS
This work [P5]	128...135	4.3GHz	17.6 mW	2.7V	0.35μm BiCMOS

5.2 Phase frequency detector

The phase detector is a block that compares the phases of its two input signals, and gives an output proportional to the phase difference between the input signals. This section will discuss different types of phase detectors, and compare their performances. First, multiplier-type phase detectors will be discussed. Then, a commonly used phase detector, the XOR gate, will be considered. Finally, phase frequency detectors based on sequential logic will be discussed, with special attention paid to a problem common to almost all of them, i.e. the dead zone.

5.2.1 Multiplier-type phase detectors

The simplest possible phase detector is an analog multiplier. Let us consider two analog input signals with the same frequency ω_l but with a phase difference of ϕ_e :

$$\begin{aligned} v_1(t) &= V_1 \sin(\omega_l t) \\ v_2(t) &= V_2 \cos(\omega_l t - \phi_e) \end{aligned} \quad (5.2)$$

Multiplying the input signals with each other yields the following output signal:

$$v_{out}(t) = \frac{1}{2} K_m V_1 V_2 \sin(\phi_e) + \frac{1}{2} K_m V_1 V_2 \sin(2\omega_l t - \phi_e), \quad (5.3)$$

where K_m is the voltage gain of the multiplier. Due to lowpass filtering in the loop, only the first term will remain, and thus the output of the multiplier-type phase detector will be

$$v_{out}(t) = \frac{1}{2} K_m V_1 V_2 \sin(\phi_e). \quad (5.4)$$

Thus, the output voltage of the multiplier-type phase detector is proportional to the phase difference between the inputs. However, as Equation (5.4) shows, the dependence is not linear, i.e. the gain of the phase detector K_m is not constant throughout the phase difference range, and thus the PLL loop gain is not constant.

The gain of the phase detector is reasonably constant only over a small range of phase differences around zero ($\sin\phi_e \approx \phi_e$ only if ϕ_e is small). In addition to that, the gain changes polarity at $\pm\pi/2$, causing potential instability in the loop. Thus, the multiplier-type phase detector can only be used in a phase difference range smaller than $-\pi/2 \dots +\pi/2$.

In spite of the above-mentioned limitations of the multiplier-type phase detector, it is sometimes used in PLL's requiring extremely high phase comparison frequencies. An analog multiplier, e.g. a Gilbert cell, can be operated up to gigahertz frequencies, making it suitable for these applications.

5.2.2 The XOR gate as a phase detector

If the inputs of the multiplier are strongly over-driven, i.e. the inputs are no longer sine waves but square waves, the multiplication operation becomes equivalent to a logic exclusive-OR (XOR) function. The dependence of the output voltage on the amplitudes of the inputs in Equation (5.4) vanishes, and the sinusoidal response becomes piecewise linear.

The gain of the phase detector is now constant over the entire phase difference range $-\pi/2 \dots +\pi/2$. If the phase difference is extended beyond that, the gain polarity will again change, resulting in instability.

The XOR phase detector locks to a 90° phase difference between its inputs. Consequently, the VCO frequency is steered downwards half of the period and upwards the other half, causing a strong sideband at a frequency offset of $2f_{ref}$ from the carrier. If the duty cycle of the input signals is not 50%, the XOR phase detector will also cause frequency components at f_{ref} . These sidebands limit its use in high-performance frequency synthesizers.

The simple XOR phase detector cannot tolerate missing input transitions. If transitions are missing, it steers in the wrong direction. Thus, it is not by itself useful in clock recovery PLL's, where the incoming data (non-constant by definition) is used as the reference.

Although the simplest case of the XOR phase detector is not very useful in practice, some improved versions of it have been presented, and widely used. The classical phase detector used in clock recovery PLL's, the Hogge phase detector [96][97], is basically an extension of the simple XOR phase detector. The linear range of this phase detector is $-\pi/2 \dots +\pi/2$. Recently, some improvements to the Hogge phase detector have been presented in [98], mainly to reduce the complexity and power dissipation of the phase detector.

Clock recovery PLL's also use different combinations of phase detectors and frequency detectors, depending on the type of data coding used in the transmission. For example the return-to-zero coded data always includes a frequency component at the clock frequency, i.e. no reference transitions are missing.

5.2.3 Phase frequency detectors

In frequency synthesis applications it is desirable to add some frequency sensitivity to the phase detector, i.e. extend the useful phase difference range beyond $-\pi/2 \dots +\pi/2$. This can be done by adding a third state to the phase detector output. Now, in addition to steering the VCO frequency either up or down, the phase detector also has a high impedance state in which it is not steering in either direction. Such phase detectors, independent of the topology used, are commonly called phase frequency detectors or PFD's.

The linear range of the PFD is wider than that of pure phase detectors, $-2\pi \dots +2\pi$. It must be noted that the frequency detection feature prevents the use of the PFD in cases where input transitions might be missing, e.g. in clock recovery PLL's.

Although better than the phase detectors discussed in previous sections, the PFD also has some nonidealities that have to be taken into account when designing the synthesizer. Firstly, some digital PFD's, e.g. [99], suffer from race problems. The PFD is asynchronous by nature, and is thus susceptible to problems originating from different propagation delays through different circuit blocks. Unless special precautions are taken, this causes the output to glitch through several intermediate states before reaching its final value. These glitches depend on temperature, process variations, etc., and their effect on the overall performance of the synthesizer is extremely difficult to predict.

Secondly, and more severely, almost all digital PFD's suffer from a dead zone. It is a region of very low, zero, or unpredictable gain near zero phase difference. The origin of the dead zone is the inability of digital logic to generate infinitely short pulses. The PFD generates pulses to steer the VCO frequency either up or down. Ideally, no steering will be needed once the loop has reached lock. In practice, small corrections are needed all the time. However, finite rise and fall times of the PFD output signals forbid generating infinitely short output pulses. Therefore, the VCO frequency can fluctuate randomly between certain bounds given by the shortest pulse the PFD is able to generate.

The dead zone causes the PLL to run essentially open-loop part of the time. This effect is time-varying, but on the average it increases the close-in phase noise of the synthesizer. Moreover, in $\Delta\Sigma$ fractional-N PLL's, the dead zone in the phase detector forms a nonlinear element in the feedback path, causing the high pass shaped quantization noise from around $f_{ref}/2$ to mix down around DC, further increasing the close-in phase noise.

A commonly used method for eliminating the dead zone problem is to generate both up and down pulses in every cycle. When the phase difference between the inputs of the phase detector is zero, both pulses have a minimum width. When one of the pulses trails the other one, the corresponding output pulse is widened, while the other one maintains the minimum width. Thus, the net pulse width is always directly proportional to the phase difference between the inputs of the phase detector.

In fact, this method itself does not remove the problem of dead zone, but passes it over to the chargepump. However, since the output current of the chargepump is usually controlled by switches that are independent of each other, generating net output current pulses with infinitely small area is possible.

Previously published phase frequency detectors (e.g. [100]) generate the short pulses by adding a delay element in the feedback path of the PFD. This method, although ideally perfect, relies on matching between the forward path elements. The new PFD topology proposed in this work, on the other hand, implements the delay elements in the forward path of the PFD, and is insensitive to process, temperature and supply variations. In general, all possible variations in the proposed PFD lead to a slightly higher reference feedthrough than in the ideal case, but they can never introduce a dead zone.

5.3 Chargepump

The chargepump is a block that, as the name suggests, either sources constant current (adds charge) to the loop filter or sinks constant current (removes charge) from the loop filter. The chargepump receives control signals from the phase frequency detector to pump either *up* or *down*. If neither one of these control signals is active, the chargepump represents an infinite impedance towards the loop filter. An ideal chargepump consists of two switched current sources, as shown in Figure 5.3.

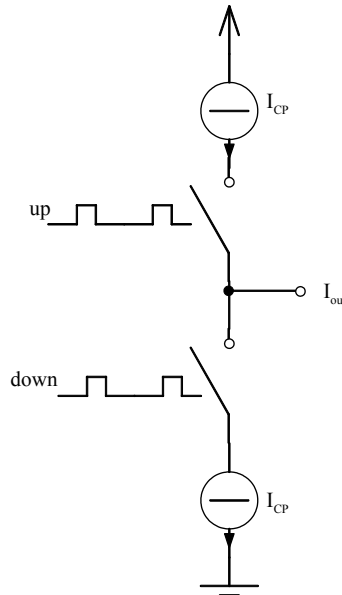


Figure 5.3: The schematic of an ideal chargepump.

An ideal chargepump has several properties that can not be realized: it has infinitely fast reaction time to the control signals, the current sources have an infinite output impedance (i.e. the current is perfectly independent of the output voltage), and the current sources are perfectly matched. The limitations of real chargepumps will be discussed in the following.

The chargepump should have as wide output voltage range as possible. To lower the sensitivity of the PLL to external interference as well as internal noise sources, it is desirable to keep the VCO gain (in Hz/V) as low as possible. However, the VCO must cover the entire operating range of the system it will be used in, and it must cover process, temperature and supply variations. This requirement sets a lower limit for the frequency tuning range. Given this limitation, the VCO gain can only be reduced by increasing the tuning voltage range used to achieve the frequency range. With all passive loop filters, the output voltage of the chargepump is equal or directly proportional to the control voltage of the VCO. Thus, if the tuning voltage range of the VCO is increased, the output voltage range of the chargepump must increase as well. On the other hand, the output voltage range is always limited by the supply voltage of the chargepump, and some headroom required for the current source.

To keep the reference spurs at an acceptable level, the mismatch between the up and down currents in the chargepump should be minimal. This conflicts with the wide output voltage range requirement, since current sources requiring low headroom tend to have low output impedances as well, thus giving a worse current matching over the output voltage range.

Recently published chargepumps have approached the current matching problem from different angles. Some have simply ignored the output voltage range problem, and employ cascaded current sources to provide a high output impedance (e.g. [69]). Some use high swing cascades to slightly reduce the problem (e.g. [101]). Some have chosen to ignore the matching issue, and employ simple current mirrors with a low output impedance (e.g. [102]). Some try to calibrate the up and down currents to minimize the mismatch caused by simple current sources (e.g. [103]). In the chargepump proposed in this work, the output voltage range is maximized while still keeping a high output impedance.

5.4 Loop filter

With very few exceptions, almost all commercial PLL synthesizers employ off-chip passive loop filters. To reduce the current noise from the chargepump and the reference feedthrough, the loop filter capacitors are typically large, in the order of several nanofarads or more. The capacitance density that can be achieved on chip is normally around 1 nF/mm^2 , and thus a large loop filter capacitor would be very expensive in terms of silicon area. Another reason for using an external filter is the better absolute accuracy of discrete passive components. In a typical IC process, the spread of absolute capacitance values is around $\pm 15\%$ between lots, and the spread of resistance values can be as high as $\pm 25\%$. On the other hand, discrete passives with $\pm 1\%$ tolerances are readily available.

In some applications, where the phase noise requirements are less stringent, it may be feasible to implement a passive loop filter on chip. If a higher close-in phase noise can be tolerated, the chargepump current can be reduced, and thus the capacitance required in the loop filter is reduced as well. For example [104] implements a differential passive loop filter on chip. The resulting die area is small, but on the other hand the close-in phase noise performance is quite poor.

Active loop filter implementations, e.g. Miller capacitance multipliers, would allow bringing the large capacitances on chip without a significant increase in silicon area. On the other hand, an active loop filter typically has worse noise performance than a passive one. In some applications, however, the loop filter is not the dominant noise contributor, and a slightly higher noise can be accepted. For example in [95], an active loop filter implementation is used, and the close-in phase noise performance is still very good.

Another potential benefit of an active loop filter would be that the input of the filter is typically the input of an operational amplifier, i.e. a virtual ground node. This is a large benefit for the chargepump design, since the chargepump no longer needs to pump constant and matched currents over a large output voltage range.

An interesting combination of an active and a passive loop filter, called the dual-path loop filter, is presented in [105]. The large loop filter capacitor is implemented using a capacitance multiplier, while the rest of the filter is purely passive. This filter achieves excellent noise performance, and the silicon area is small enough to be economically feasible.

5.5 Voltage-controlled oscillator

The design of integrated voltage-controlled oscillators (VCO's) is a broad research topic in itself. Countless VCO designs have been published in the recent years. A more detailed analysis of the VCO is beyond the scope of this work. The sole intention of this section is to briefly show what kind of performance can be expected from a state-of-the-art integrated VCO.

The simplest and most area efficient way to implement the VCO would be a ring oscillator. Ring oscillators are almost exclusively used in clock generation PLL's for microprocessors and other types of digital circuits. Ring oscillators, however, suffer from an inherently poor phase noise performance, and are therefore almost never used in communications applications. Practically all frequency synthesizers in communications applications employ some type of harmonic oscillator, a simple example of which is shown in Figure 5.4.

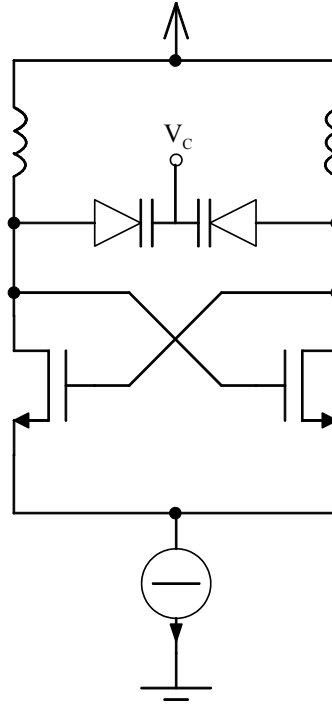


Figure 5.4: The schematic of a simple harmonic oscillator.

The phase noise of the harmonic oscillator is determined by the quality factor Q of the resonance tank (the parallel connection of the tunable capacitors and the inductors). In integrated resonators, the overall tank Q is normally dominated by the Q of the inductors. Motivated by this fact, a significant amount of work on modeling the inductors and optimizing their Q -values has been published over the last couple of years (e.g. [106][107][108][109]).

The phase noise performance of integrated VCO's has improved rapidly over the recent years, and fully integrated VCO's start to appear in the marketplace. Almost all of today's WLAN (802.11a/b/g) and WPAN (Bluetooth) radio IC's include a fully integrated VCO. In cellular systems (GSM, WCDMA), on the other hand, the phase noise requirements are even tougher, and the majority of commercial designs still use discrete off-chip VCO's. However, several fully integrated VCO's exceeding the cellular performance requirements have already been published, and it should not take long before integrated VCO's take over on the cellular side as well. Table 5.5 compares the phase noise performance of some recently published integrated VCO's.

Table 5.5: Comparison of the phase noise properties of some recently published voltage-controlled oscillators.

Author	Center frequency	Phase noise @ offset frequency	Technology
Craninckx et al. [108]	1.76 GHz	-115 dBc/Hz @ 200 kHz	0.7 μ m CMOS
Rofougaran et al. [110]	0.9 GHz	-85 dBc/Hz @ 100 kHz	1 μ m CMOS
Craninckx et al. [111]	1.8 GHz	-116 dBc/Hz @ 600 kHz	0.7 μ m CMOS
Jansen et al. [112]	2.2 GHz	-99 dBc/Hz @ 100 kHz	Si bipolar, $f_T=15$ GHz
Razavi [113]	1.8 GHz	-100 dBc/Hz @ 500 kHz	0.6 μ m CMOS
Soyuer et al. [114]	2.4 GHz	-92 dBc/Hz @ 100 kHz	BiCMOS, $f_T=12$ GHz
Nguyen et al. [115]	1.8 GHz	-88 dBc/Hz @ 100 kHz	BiCMOS, $f_T=10$ GHz
Hajimiri et al. [116]	1.8 GHz	-121 dBc/Hz @ 600 kHz	0.25 μ m CMOS
Park et al. [117]	0.9 GHz	-101 dBc/Hz @ 100 kHz	0.6 μ m CMOS
Dauphinee et al. [118]	1.5 GHz	-105 dBc/Hz @ 100 kHz	0.8 μ m BiCMOS, $f_T=11$ GHz
De Muer et al. [51]	2 GHz	-125 dBc/Hz @ 600 kHz	0.65 μ m BiCMOS
Vancorenland et al. [119]	1.57 GHz	-133 dBc/Hz @ 600 kHz	0.25 μ m CMOS
Gierkink et al. [120]	5 GHz	-125 dBc/Hz @ 1 MHz	0.25 μ m CMOS

5.6 Noise contributions of the building blocks

Due to the noise shaping properties of the PLL, different blocks dominate the overall phase noise of the PLL at different offset frequencies from the carrier. Typically, the phase noise very close to the carrier is dominated by the reference source, i.e. the crystal oscillator. The close-in phase noise, i.e. the phase noise up to the loop bandwidth, is then usually dominated by either the loop filter or by the chargepump. Finally, the phase noise at large offset frequencies is practically always dominated by the VCO. This section will take a closer look at how the overall phase noise of the PLL is built up.

The reference clock source in a frequency synthesizer PLL is normally a very high quality crystal oscillator with a very low phase noise. A typical phase noise specification for the crystal oscillator would be e.g. -120 dBc/Hz at an offset of 100 Hz [121].

However, the transfer function of the PLL from the reference input to the high-frequency output multiplies the reference noise by the loop division ratio N . For example in an integer- N synthesizer for the DCS-1800 system, N can be as high as 9400, amplifying the phase noise of the reference by almost 40dB. Assuming the PLL has a close-in phase noise of -80 dBc/Hz, the phase noise of the crystal oscillator will thus dominate at offset frequencies lower than 100 Hz.

The phase noise at offsets lower than 100 Hz is seldom very interesting. However, the assumption of a very high quality crystal oscillator module is not always valid. In modern, highly integrated RF circuits, it is often desirable to integrate the crystal oscillator on the same chip as well, leaving the crystal resonator as the only external component. In this case, the process technology and the operating conditions of the crystal oscillator cannot always be chosen optimally, and the resulting phase noise performance is typically worse than that of a separate crystal oscillator module. In these cases, the phase noise of the crystal oscillator can become an issue.

The close-in phase noise, i.e. the phase noise at offsets lower than the loop bandwidth (see Figure 3.1), is normally dominated either by the chargepump current noise or by the thermal noise of the loop filter resistor. The noise contribution of the chargepump depends on the noise of the current sources as well as the on-time of the chargepump. As discussed in the previous sections, both the *up* and the *down* currents of the chargepump are usually connected to the loop filter for a fraction of each reference cycle to avoid dead zone problems. During this time, however, the noise of both current sources contributes to the total noise of the PLL. That is, from a noise point of view, it would be beneficial to keep the on-time of the chargepump as short as possible. The noise contribution of the loop filter resistor is directly proportional to the resistor value.

Increasing the magnitude of the chargepump current will normally decrease the noise contribution of the chargepump, as the noise current will increase less than the output current. Increasing the current, however, has implications on the loop filter components as well: to keep the same loop dynamics, the capacitors in the loop filter must be increased and the resistor decreased (the assumption here is that the PLL is a second-order loop with a compensating zero, implemented using a passive loop filter). Decreasing the resistor value in the loop filter will further reduce the close-in phase noise, but increasing the capacitor values might not be desirable. Especially if the loop filter should be integrated on the chip, the larger capacitor values might not be economically realizable. In most commercial frequency synthesizers, the phase noise requirements mandate the capacitor values to be too high to be integrated, and therefore an external loop filter is used. Typical chargepump currents range from tens of microamps to a few milliamps.

At offset frequencies larger than the loop bandwidth, the phase noise is practically always dominated by the VCO, although the noise from the chargepump and the loop filter resistor can have noticeable contributions as well. In $\Delta\Sigma$ fractional- N synthesizers, however, the highpass shaped quantization noise of the $\Delta\Sigma$ -modulator can contribute significantly to the phase noise at large offsets, unless properly filtered. To avoid these issues, $\Delta\Sigma$ fractional- N PLLs are typically designed so that the loop order is higher than the $\Delta\Sigma$ -modulator order.

5.7 Power dissipation of the building blocks

The power dissipation of the frequency synthesizer is an important parameter, especially in mobile applications. In systems with high output power levels, like GSM, the power amplifier will always dominate the overall power dissipation. However, in shorter-range systems, the frequency synthesizer can be a major contributor to the overall power dissipation. In some systems, like IEEE 802.11a WLAN, the system timing requirements are so tight that the synthesizer can seldom be turned off to save power. In these cases, the importance of the PLL power dissipation is even larger.

In an RF synthesizer, the power dissipation is normally dominated by the blocks running at the highest frequency, i.e. the VCO and the prescaler. In VCO design, there is typically a tradeoff between supply current and phase noise; if a worse phase noise performance can be accepted, the power dissipation can be lowered often quite significantly. Since VCO design is not within the scope of this work, these tradeoffs will not be discussed in more detail here.

In prescaler design, the power dissipation cannot usually be traded with anything. With a given technology and a given range of required operating conditions (temperature, supply voltage, input frequency, etc.), the only ways to reduce power dissipation are architectural choice and careful design. As discussed in Section 5.1, the phase switching prescaler architecture generally consumes less current than the conventional architecture, because it has fewer components running at the input frequency. However, this lower consumption comes at a price of some potential unwanted effects, such as spurs at a fraction of the reference frequency.

When the overall architecture of the prescaler is chosen, the power dissipation is further affected by the topologies used in the building blocks of the prescaler (typically D flip-flops). Traditionally, prescalers were usually built using ECL-type (in bipolar technology) or CML-type (in CMOS) flip-flops. More recently, different CMOS flip-flop implementations have gained popularity, since the shrinking linewidths of CMOS technologies have allowed them to run faster and consume less power. It is not clear, however, whether a CMOS implementation always has an advantage over an ECL-/CML-implementation. The pros and cons of each will have to be evaluated case by case. The CMOS flip-flop has a clear advantage, though, in some special applications requiring an extremely large range of operating frequencies (an order of magnitude or even more); the power dissipation of the CMOS flip-flop is directly proportional to the operating frequency (i.e. the consumption will be smaller at lower operating frequencies), whereas the ECL-/CML-type flip-flop will consume constant current (which has to be dimensioned according to the highest operating frequency) at all operating frequencies.

The phase detector normally consists of a few standard digital cells running at a relatively low frequency. Thus, the power dissipation of the PFD is practically always negligible. The chargepump, on the other hand, can be a noticeable contributor to the overall power dissipation of the synthesizer. To avoid excessive glitching during switching, it is quite common to keep the current sources of the chargepump on all the time. During switching, the current is then just directed either to the output or to a dummy branch. While allowing for much better spurious performance, this method

increases the power dissipation of the chargepump significantly. Instead of supplying the output current for a small fraction of time, the chargepump now has to constantly supply the entire output current, which can be in the order of several milliamperes. However, if switching the current sources off is not an option, not much can be done to avoid the problem. Slight decreases in power dissipation can be achieved, however, by designing current sources that draw as little current as possible in addition to the output current.

In $\Delta\Sigma$ fractional-N synthesizers, the digital $\Delta\Sigma$ -modulator can be a noticeable contributor to the overall power as well. The power dissipation of the modulator depends on the modulator order and the internal word length (i.e. the total number of gates), the clock frequency of the modulator (usually the reference frequency), and the technology used (smaller linewidth technologies normally consume less current). A $\Delta\Sigma$ -modulator with typical specifications can have a power dissipation comparable to the chargepump. Both the modulator and the chargepump, however, normally consume much less than the VCO and the prescaler.

6 Synthesizers in integrated systems

In an increasing number of communications applications, especially in the WLAN and WPAN markets, the frequency synthesizer is no longer a standalone integrated circuit. Instead, it is integrated as a part of a much larger entity, such as a complete WLAN transceiver [P6], or even a complete Bluetooth system including the digital baseband (more than one million digital gates) [122]. With the synthesizer as a part of a larger integrated system, all of the synthesizer requirements discussed in the earlier chapters obviously still apply. In addition, however, the fact that the synthesizer no longer operates in a closed environment sets some further requirements on it. The synthesizers will pick up interfering signals from its environment, and it will cause some interference to the blocks around it. This chapter will discuss the additional requirements set for the synthesizer in an integrated system.

6.1 Local oscillator pulling

Perhaps the most well-known problem of other parts of the system disturbing the synthesizer is called frequency pulling. The power amplifier used in the transmitter will have a high output power, and some of that power can be unintentionally fed back to the synthesizer (typically to the VCO inductor) through inductive or capacitive coupling. This would not be a problem if the output signal was a pure sinusoidal signal. However, the output is normally a modulated signal, and the modulation will be fed back to the VCO. This will cause the VCO signal to be slightly modulated as well, which is definitely not a desired effect.

The frequency pulling problem is not unique to integrated systems. In many applications, the output power of the power amplifier is so large that the pulling phenomenon can be very clearly seen even if the VCO and the power amplifier are on separate chips, and separated by a relatively large distance on the PCB. Thus, it has been a known problem for years, and several remedies have been developed.

The first, and most obvious, remedy to the pulling problem is to realize that there will be significant coupling to the VCO only at or very near the oscillation frequency. That is, if the VCO frequency is chosen to be something else than the output frequency, pulling will not be an issue. This fact makes the superheterodyne architecture and similar architectures immune to the problem. Another frequently used method is to use a double-frequency VCO to avoid pulling problems. The frequency divider can then be used to generate the required quadrature signals as well. This approach, however, is not suitable for all applications because of technology limitations. For example in the 802.11a WLAN system, the highest channels are at 5.825GHz. A double-frequency synthesizer would have to run at up to 11.65GHz, which is not an easy task.

The offset PLL transmitter architecture (see Figure 6.1) is often used in systems employing constant envelope modulation types. In the offset PLL in Figure 6.1, neither one of the local oscillator signals f_1 and f_3 is at the carrier frequency, and thus will not suffer from pulling. Another benefit of the offset PLL architecture is that the output of the VCO is more or less directly connected to the power amplifier, allowing for a very low noise floor that is required in some applications (e.g. GSM base station transmitters).

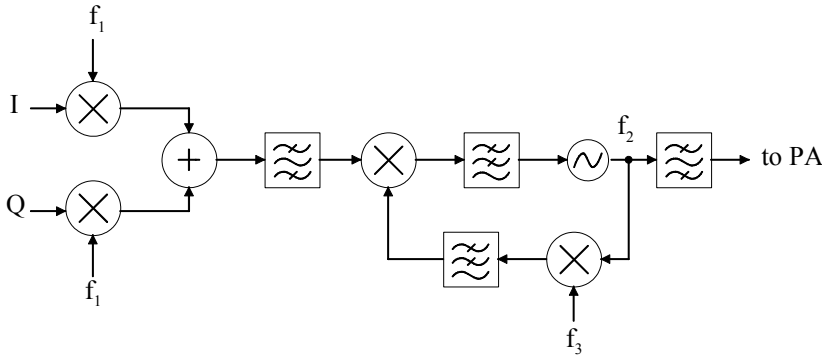


Figure 6.1: Transmitter with an offset PLL.

6.2 Frequency stability during switching transients

Transceiver chips designed for mobile applications typically have different power saving modes. The chip might for example be almost completely turned off during idle times, maybe only providing a clock signal to another chip in the system. The most typical power saving strategy, though, is to turn off the transmitter during receive, and the receiver during transmit. This feature is relatively straightforward to implement, and can result in significant power savings.

In some systems, the switching from receive mode to transmit mode must be quite fast. In the 802.11a WLAN system, for example, the transceiver must be able to switch between the two modes in less than $2\mu\text{s}$. This requires the turn-on and turn-off times of the receiver and the transmitter to be fast, which may result in switching transients. On the other hand, a typical PLL settling time in the 802.11a WLAN system is in the order of $200\mu\text{s}$. Clearly, the PLL must stay locked through all switching transients that might occur. If the loop falls out of lock, there is not enough time to reacquire lock.

The transmit mode current in [P6] is 137mA, and the transmitter needs to switch on and off in less than $1\mu\text{s}$. To have enough of margin in the worst case process, temperature and supply corner, the typical turn-on and turn-off times of the transmitter are approximately 150ns. The supply voltage of the transmitter is connected to the chip through two parallel bondwires, each having approximately 2nH of inductance. Assuming that the current is ramped up and down linearly, the di/dt bounce in the chip supply voltages is approximately 0.9mV. However, the linear ramping is a best case assumption; with real ramping profiles, the di/dt bounce can be several millivolts. The chip ground is not an ideal ground, either, although it is connected through several shorter bondwires, and the ground bounce is significantly smaller than the supply bounce.

In addition to the di/dt bounce caused by the inductive connections to supply voltages, the resistive IR drop in the supply paths can result in switching transients. If the on-chip supply paths are routed in a tree topology, the synthesizer supply current will share some of the paths with the transmitter supply current, and hence the effective supply voltage seen by the PLL will depend on whether the transmitter is on or not. This problem can be

easily avoided, though, by using completely separate supplies for the PLL. The ground, however, cannot be completely separated, since the chip substrate (connected locally to the separated ground nodes) is conductive.

Changes in the chip supply voltages and ground potentials, whether caused by inductive or resistive mechanisms, will affect the bias voltages and currents as well. Typically, the bias voltages and currents are generated centrally for the entire chip in a bandgap voltage reference circuit. While the output voltage of the bandgap circuit is ideally independent of the supply voltage, real implementations will have some supply dependence. Hence, when the supply voltage bounces, the bias voltages and currents to the PLL will bounce slightly, too.

Why would changes in the supply voltage and the bias voltages and currents affect the PLL, then? First of all, the effective control voltage seen by the VCO may change when the supply and ground voltages bounce. The VCO control voltage is typically single-ended, and refers to a ground potential. If the control voltage is constant, but the ground potential bounces by 1mV, the effective control voltage bounces by 1mV. With a typical VCO gain of 150MHz/V, this would result in a 150kHz shift in the VCO center frequency. This problem can be mitigated, though, by treating the control voltage and its reference ground as differential signals, so that most of the interfering signals would connect identically to both nodes, and thus cancel out.

Secondly, the VCO will have a number of nonidealities. An ideal VCO has only one control terminal, i.e. the output frequency is determined by the control voltage alone. A real VCO, however, is sensitive to the supply voltage and bias current as well, although the gain through these ports is lower than through the actual control port. When the gain through the intentional control port may be 150MHz/V, the supply dependence could be in the order of 5MHz/V, and the bias dependence in the order of 0.2MHz/ μ A. That is, a 3mV supply bounce, for example, would result in a 15kHz shift in the VCO center frequency.

None of the nonidealities listed above are normally big enough to cause significant problems on their own. However, if proper attention is not paid to these issues in the design phase, the combined effect of all the nonidealities may well result in settling time problems when switching from mode to mode.

6.3 Spurious tones caused by coupling

An integrated system typically has data converters and/or a large amount of digital circuitry on the same chip with the frequency synthesizer. The clocking of the digital parts is typically synchronous, and the clock signal is required to have very fast transitions. Such a square wave signal with fast transitions will have significant harmonic power even at very high harmonic numbers, i.e. at very high frequencies.

The clock signals and their harmonics can couple to the frequency synthesizer through several mechanisms. Inductive and capacitive coupling are easier to manage, since the coupling gets weaker with increasing distance between the interfering block and the synthesizer. Coupling through power supplies and the conductive substrate can be much more difficult to manage. Especially the substrate coupling is extremely difficult to

model accurately, and therefore it is hard to predict exactly how much trouble the coupling will cause. Tools for predicting the supply coupling have started to emerge (e.g. [122]), but their accuracy and capacity are not yet very good.

Whatever the coupling mechanism, the coupled clock signal and its harmonics will appear as spurious tones in the synthesizer output. Especially the VCO control line should be protected as well as possible, because any disturbance coupled to it will have a high gain to the output of the synthesizer, and will appear at small offset frequencies from the carrier.

6.4 Coupling of LO harmonics to other blocks

The output of the frequency synthesizer will not only contain the wanted frequency, but harmonics of it as well. In a well designed PLL, the harmonic content in the differential output signal is fairly low, but there will typically be quite high common mode signals containing the even harmonics of the LO. Any imbalance in the consequent stages (mixers, power amplifiers, baluns) will convert some of the common mode signal into a differential signal again. Also, the supply voltage line of the VCO will inevitably have a quite high content of the even harmonics of the LO signal.

Depending on the radio architecture used, the harmonics of the synthesized frequency may fall into bands of interest. For example in [P6], the 4th harmonic of the second LO signals will fall onto the upper edge of the 5GHz band, and special care must be taken to make sure the amplitude of the harmonic does not exceed regulatory requirements.

The harmonics of an RF synthesizer are, however, at known very high frequencies, and spaced widely apart in the frequency domain. Therefore, they can be effectively attenuated by on- or off-chip filtering. Filtering is impossible, though, if the LO harmonic falls too close to, or coincides with, the wanted signal. The harmonics must therefore be taken into account when designing the frequency plan of a transceiver.

6.5 Coupling of LO reference frequency to other blocks

The reference spurs of the LO, i.e. the spurs at $\pm n f_{ref}$, are naturally visible in the output spectrum of a transmitter through the intentional mixing process. However, the reference frequency and its harmonics may couple to the transmitter or the receiver through other mechanisms as well.

As an example, in [P6], the 120th, 121st, etc. harmonics of the 20MHz reference clock can be distinguished from the 2.4GHz output spectrum. They are not high enough to cause any problems, but nevertheless distinguishable. In this case, there are significant harmonic components of the 20MHz reference frequency in the chargepump supply line. To lower the close-in phase noise, the chargepump attempts to make the edges of the output current pulses as sharp as possible. The current is drawn from the supply line, and consequently there will be sharp edges (and hence high-order harmonics) in the supply line as well. The supply line of the first LO passes the load inductors of the transmit RF mixer at a distance of less than 100 μ m. It could be shown that the source of the spurious tones at the output was the harmonics of the reference frequency coupling inductively from the LO supply line to the load inductors of the mixer.

Maybe the best way to reduce problems of this kind is to improve the decoupling of the blocks causing the interference. In the example case above, the spurs at the output of the transmitter were reduced 15-20dB by simply adding a small local decoupling capacitor very close to the chargepump. The high-order harmonics will now be shorted through the decoupling capacitor, and will not travel in the supply line, and hence will not couple to other blocks, either.

7 Summary of publications

This chapter gives a brief overview of each publication and the author's contribution in them. The author was responsible for all the work related to publications [P2]-[P5].

[P1] A 2 GHz Phase-Locked Loop Frequency Synthesizer with On-Chip VCO

This paper presents an integer-N PLL design in a 0.5 μm BiCMOS process. The prescaler is based on the conventional dual-modulus architecture, and employs traditional ECL-type flip-flops. The first versions of the proposed new phase detector and chargepump topologies are presented in this paper as well. The chip also includes an integrated VCO, which was designed completely by Mr. Jyrki Vikla. Except for the VCO, the entire work was done by the author.

[P2] A Novel Phase Detector with No Dead Zone and a Chargepump with Very Wide Output Voltage Range

This paper provides a more detailed analysis of the proposed new phase detector and chargepump topologies. Improved versions of both were designed, and experimental results are presented.

[P3] A 2 GHz $\Delta\Sigma$ Fractional-N Frequency Synthesizer in 0.35 μm CMOS

This paper describes the first $\Delta\Sigma$ fractional-N synthesizer designed in this work. The synthesizer employs the phase detector and chargepump topologies developed previously. The prescaler uses the phase-switching architecture, and is designed completely in CMOS. A new D flip-flop topology allows it to function up to input frequencies of over 2 GHz. The prescaler implements eight possible moduli (64...71) that are controlled by an on-chip digital MASH 1-1-1 $\Delta\Sigma$ -modulator. The design is done in a 0.35 μm CMOS process, and the experimental results show good performance.

[P4] A 1.76-GHz 22.6-mW $\Delta\Sigma$ Fractional-N Frequency Synthesizer

This paper is based on the same chip as [P3], so the building blocks are the same as above. However, the experimental setup was rebuilt and some of the measurements redone for this paper. This has removed some peculiarities in the experimental results presented in [P3]. The results presented in this paper are state of the art: the close-in phase noise is -81dBc/Hz at an offset frequency of 10 kHz, and the spurious level is lower than -85 dBc.

[P5] A 4 GHz $\Delta\Sigma$ Fractional-N Frequency Synthesizer

This paper provides a more detailed theoretical analysis of the close-in phase noise requirements of the synthesizer in different systems. It employs the same phase detector and chargepump topologies as the previous papers, but provides a more detailed discussion on the tradeoffs in their design. This design also includes a BiCMOS prescaler based on the phase-switching architecture, implementing eight moduli (128...135). The prescaler operates up to an input frequency of 4.3 GHz. The experimental results show that the design works relatively well, although the performance is not as good as that of the 2 GHz synthesizer presented in [P4].

[P6] A Single Chip CMOS Transceiver for 802.11a/b/g Wireless LANs

This paper describes a complete transceiver chip that fulfills the IEEE 802.11 a, b, and g standards. The key features of the chip include a new dual conversion architecture that avoids image rejection filtering, and an extremely flexible interface towards the baseband chip, allowing the chip to operate with multiple different baseband chips. In addition to these features, this chip also had challenging frequency synthesizer design requirements. The chip includes two PLLs that have to operate simultaneously with each other, and with a multitude of other circuit blocks on the same die. Even the reference crystal oscillator is integrated on the same chip. The experimental results show excellent PLL performance; the two PLLs have a combined integrated phase noise of -34 dBc, which equals an rms phase error of 1.1° .

In this part of the work, the author was responsible for specifying the requirements of the blocks, including the PLLs. The author was also responsible for interface and integration issues that are inevitably faced when integrating an entire system on a single chip. In addition to these, the author had the responsibility for the technical management of the entire project, including detailed reviewing of all the blocks. The paper itself is completely written by the author.

8 Conclusions

In the last decade, we have witnessed an incredible growth in the number of wireless handheld devices. During the first half of the decade, the main focus was on reducing the size and weight of the device, as well as on improving the battery life time. In most devices, however, these qualities have now improved so much that the benefit of additional improvement gets smaller and smaller. A cell phone, for example, is already as small as it can comfortably be, and has more than two weeks of standby time without charging. Because of this, the focus is shifting towards adding more and more functionality into a single device. Cell phones, for example, are no longer marketed with the technical qualities of the phone function itself; it is the additional functionality (camera, Bluetooth, etc.) that differentiates between phones.

From a circuit designer's point of view, however, the old targets of small size and low power still remain. The user wants the additional functionalities, but does not want his cell phone to grow larger or to have a shorter standby time. That is, the size and power available per function are still shrinking. In addition, implementing multiple functions in a single device adds another dimension of complexity to the design. To save in total cost, the different functions should share as much hardware as possible. Moreover, the different functions are physically so close to each other that they can no longer be considered completely independent. The possible interference from one system to the other must be taken into account in the design phase.

This thesis concentrates on the radio frequency synthesizer, which is a key building block of any radio transceiver, independent of the wireless standard or the radio architecture. In particular, the focus has been on the implementation of three key building blocks of a phase-locked loop frequency synthesizer, namely the prescaler, the phase detector, and the chargepump. As most thesis works, this work, too, can be viewed as an evolutionary process. Already the first circuit implementations present first versions of the proposed phase detector and chargepump topologies, although the circuits themselves are relatively simple integer-N PLLs. In the next phase, the new blocks are used in more complex fractional-N PLLs. The fractional-N designs also called for new prescaler implementations. In the last phase of the evolution, the synthesizers are no longer standalone circuits, but parts of a much more complex transceiver IC.

The presented experimental results show that the designed circuit blocks can be used to build both integer-N and fractional-N PLL synthesizers with state-of-the-art performance. It is also shown that these synthesizers can be further integrated into a large transceiver chip. In particular, the last paper shows that, with careful design, the integration of the synthesizer into a larger chip does not necessarily degrade its performance.

In the future, the emerging high data rate wireless standards will set tighter and tighter performance requirements on the synthesizer. On the other hand, the digital convergence will require the synthesizers to be more and more flexible to reduce the total cost of the system. These often conflicting requirements mandate further research in the field of radio frequency synthesizers in the future as well.

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