# Bypassing the CAMAC Data Bus to Read Out FERA Data at Higher Rates

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*Abstract*

The CAMAC standard offers flexibility by providing power and a data bus for various modules, but it is limited to a 1 Mword/sec bandwidth. LeCroy Research CAMAC modules with an auxiliary data bus, FERA, provide a 10 Mword/sec data transfer without CAMAC controller intervention. We have used a National Instruments digital I/O board (PCI-DIO-32HS) as a FERA bus-to-host bridge. The board provides hardware handshaking, a 20 Mword/sec bandwidth, bus master scatter-gather DMA, and can control up to 2 FERA busses asynchronously. Multiple boards may reside on the same PCI or Compact PCI bus. A 300 MHz Pentium II running Windows NT 4.0 sustains >3.4 MB/sec throughput in 8255 emulation mode. These capabilities are being exploited in our prototype small animal planar and PET imaging system where 32 ADC channels (16 bits each) and 3 scaler channels (32 bits each) define an event.

## I. Introduction

A common means of acquiring data is by analog-to-digital conversion under computer control. The ANSI/IEEE Std 583-1982 Modular Instrumentation and Digital Interface System standard (CAMAC) serves this purpose by combining the flexibility of NIM (DOE-TID- 20893) modularity with digital control and data lines (Dataway). The Dataway has a specified bandwidth of 1 MHz that limits the data throughput to 1 Mword/sec, for both 16 and 24 bit words [1].

LeCroy Research Systems has developed a family of CAMAC-compatible modules with an auxiliary data bus, the Fast Encoding and Readout ADC (FERA), with a 10 Mword/sec data transfer rate (16 bit words) [2]. The FERA bus supports a driver module which synchronizes other FERA modules without CAMAC controller intervention thereby boosting data throughput. However, even with FERA-compatible double-buffering with CAMAC memory modules, the data must still pass through the Dataway to reach the host computer, reducing the effective throughput of the system. In our laboratory, for example, such a system (Jorway 73A SCSI Crate Controller, Sparrow Kmax software and a 300 MHz Power Macintosh 9600 with 640 MB RAM) achieved a maximum throughput of 1 MB/sec to a RAM disk. This rate, though adequate for many bench top experiments, is insufficient in some real applications, such as a prototype small animal imaging device now under development in our laboratory.

## II. Methods and Materials

To circumvent the bandwidth limitation of the CAMAC Dataway, we assembled a FERA-compatible, differential ECL-to-TTL level translator to interface the FERA bus to an inexpensive, off-the-shelf digital I/O board (National Instruments PCI-DIO-32HS) [3]. This board was chosen because it provides six different modalities of hardware handshaking, two independent 16 bits wide channels, a maximum 80 MB/sec bandwidth and bus master scatter-gather DMA. By configuring the board as two 16 bit wide independent channels, up to two FERA systems can be controlled asynchronously. Multiple boards may also reside on the same PCI or Compact PCI bus. In our implementation we used the 8255 emulation handshake mode. The characteristics of this mode are shown on Table 1. The system consists on two FERA ADC 4300B plus a 2366 scaler, driven by a 4301 module (Figure 1).

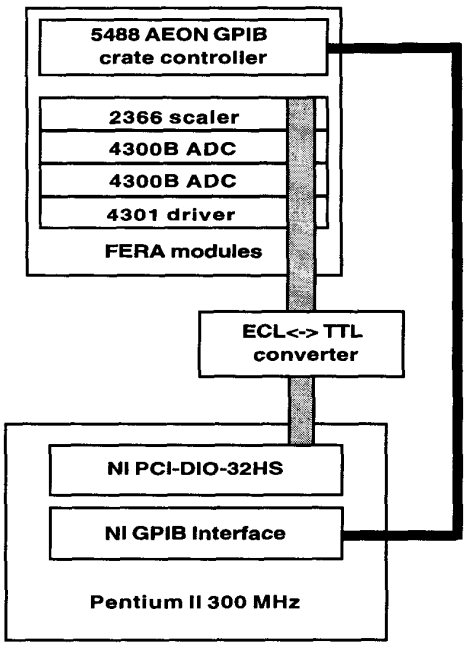


Figure 1. System schematics.

CAMAC control is established via a GPIB controller that resides on the same PC host. In such configuration, each event is comprised of 38 words (16 bit) that have to be transferred to the host. The ECL-to-TTL conversion is done in an external module using standard drivers. The host is a 300 MHz Intel Pentium II PC running Windows NT 4.0, with 512 MB RAM and 9 GB SCSI hard disk). It is used to initialize and configure the CAMAC modules via the GPIB controller and to start the acquisition, which is either terminated by reaching a preset time condition or by the user.

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Table 1.
Handshaking protocols for the NI PCI-DIO-32HS and data rates.

| Protocol | Peak Rate (MSample/s) | | Type |
|---|---|---|---|
| | 1m cable | 2 to 5 m cable | |
| 8255 Emulation | 5 | 2.67 | Asynchronous |
| Burst Mode | 20 | 10 | Synchronous |

Asynchronous mode adjusts automatically to cable length. Appropriate speed for the cable length has to be selected for synchronous mode at configuration time.

Currently, no real time processing has been implemented except for an optional data compression that reduces the amount of disk space needed to store the list mode file.

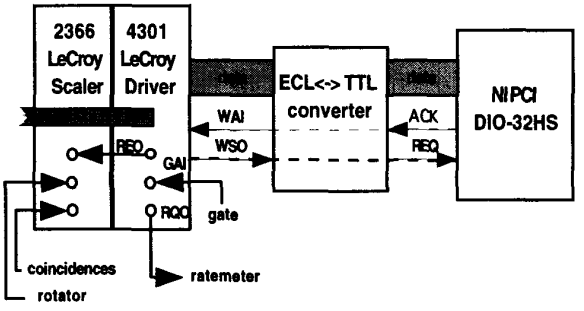


Figure 2. FERA to DIO interface.

Figure 2 depicts the details of the FERA-to-NI-DIO protocol conversion as well as the additional connections required for dead-time correction, gating and tomography. The REO ("request output") signal is fed into a scaler to count the number of events processed, while a second scaler is counting the number of events detected by the coincidence module; the ratio of these two values is used to correct for dead time.

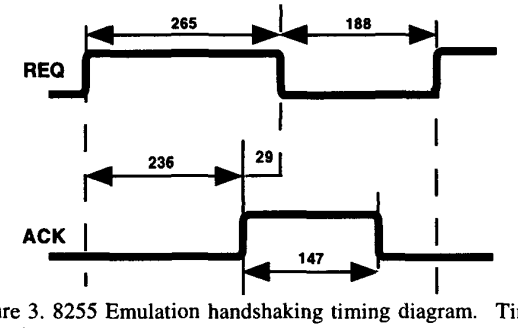


Figure 3. 8255 Emulation handshaking timing diagram. Times are given in ns.

The 'rotator' scaler keeps track of the rotator position in tomographic acquisitions, or it serves as a time marker generator for dynamic studies.

## III. Results and Discussion

Preliminary tests of a system based on this I/O board operated in 8255 emulation mode sustained a data throughput of 3.4 MB/sec. This value corresponds to acquiring >45,000 events/sec (5 µs for the A/D conversion plus 17.2 µs for transferring to the host) from a prototype imaging system consisting of 32 x 16 bit digitizers and 3 x 32 bit scalers (76 bytes per event total). Figure 3 shows the timing diagram for a parameter transfer. This diagram reveals that the most relevant limiting factor is the 236 ns delay between the rising edge of REQ and the rising edge of ACK signal: this is the time needed by the DIO board to acknowledge a parameter. A reduction of this time can only be achieved by using synchronous handshaking (burst mode in Table 1). Figure 4 shows the measured event rates as a function $^{18}$F-source activity between the two detectors, as well as the deadtime-corrected events rates. The deadtime-corrected event rates follow a straight line, which indicates that the deadtime correction is working properly.

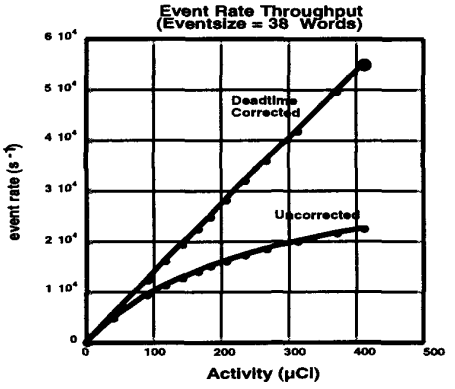


Figure 4. Measured system performance as a function of F-18 source activity.

## IV. Conclusion

This study suggests that this DIO board may provide a high speed, low cost option for a FERA data acquisition system. Various hardware improvements, implementation of the burst mode protocol, and making use of the second channel should further improve throughput.

## V. Acknowledgments

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## VI. References

[1] CAMAC Instrumentation and Interface Standards, IEEE, 1982

[2] Fast Encoding and Readout AD (FERA) System, Driver Manual, LeCroy Research, 1983

[3] DIO 6533 User Manual, National Instruments, 1997