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IEICE Transactions on Information and Systems
Volume E100D, Issue 10, October 2017, Pages 2478-2492

The performance evaluation of a 3D torus network using partial link-sharing method in NoC router buffer (Article)

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Abstract

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The high performance network-on-chip (NoC) router using minimal hardware resources to minimize the layout area is very essential for NoC design. In this paper, we have proposed a memory sharing method of a wormhole routed NoC architecture to alleviate the area overhead of a NoC router. In the proposed method, a memory is shared by multiple physical links by using a multi-port memory. In this paper, we have proposed a partial link-sharing method and evaluated the communication performance using the proposed method. It is revealed that the resulted communication performance by the proposed methods is higher than that of the conventional method, and the progress ratio of the 3D-torus network is higher than that of 2D-torus network. It is shown that the improvement of communication performance using partial link sharing method is achieved with slightly increase of hardware cost.

Author keywords

Interconnection network Multiport memory Network-on-chip (NoC) Router

Indexed keywords

Engineering controlled terms: Hardware Interconnection networks (circuit switching) Routers Servers

Compendex keywords: Communication performance Conventional methods Hardware resources High performance networks Multi-port memory Network-on-chip(NoC) NoC architectures Torus networks

Engineering main heading: Network-on-chip

Funding details

Funding number	Funding sponsor	Acronym	Funding opportunities
JP17K00087			

Funding text

A part of this research was supported by JSPS KAKENHI Grant Number JP17K00087.

ISSN: 09168532 **DOI:** 10.1587/transinf.2017EDP7031
CODEN: ITISE **Document Type:** Article

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