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Architecture and Network-on-Chip Implementation of a New Hierarchical Interconnection Network

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A Midimew-connected Mesh Network (MMN) is a minimal distance mesh with wrap-around links network of multiple basic modules (BMs), in which the BMs are 2D-mesh networks that are hierarchically interconnected for higher-level networks. In this paper, we present the architecture of the MMN, addressing of node, routing of message, and evaluate the static network performance of MMN, TESH, mesh and torus networks. In addition, we propose the network-on-chip (NoC) implementation of MMN. With innovative combination of diagonal and hierarchical structure, the MMN possesses several attractive features, including constant degree, small diameter, low cost, small average distance, moderate bisection width and high fault tolerant performance than that of other conventional and hierarchical interconnection networks. The simple architecture of MMN is also highly suitable for NoC implementation. To implement all the links of level-3 MMN, only four layers are needed which is feasible with current and future VLSI technologies.

Keywords: Massively parallel computer; hierarchical interconnection network; MMN; static network performance; network on chip.

1. Introduction

Increasing demand for computational power is a constant picture over the last 50 years[1] and it keeps going upwards. To maintain some very complex task as prediction of climate change, rush hour traffic control, or even solving some principle equations of mathematics, physics and chemistry; pushing the development of technology in a rapid speed. In addition, to pursue the answer of some grand challenge like, the explanation of origin of the universe, plate tectonics of earth, examine planetary movements, are yet to be answered. To solve these problems, computation power of petaflops or even exaflops level is required. Conventional sequential computer can not meet this power level and already has been reached saturated. Hence, massively parallel computer (MPC) is a possible solution for high performance computing. In MPC, interconnection network dominates the system performance.[2] In nearby future MPC will contain 10–100 millions of processing elements (PE)/nodes[3] with computing capability at tens of petaflops or exaflops level. To arrange these huge numbers of nodes, conventional topologies of interconnection network are not suitable, hence an efficient topology is required. Hierarchical interconnection network (HIN) is a plausible alternative way to interconnect the future MPC[4] systems. Nevertheless, performance of the proposed HIN does not yield any obvious choice of a network for MPC. Among a lot of HINs, several k-ary n-cube-based HIN have been proposed[5–8] for better performance. Nonetheless, among them no HIN is found as grand winner. Hence, new topology for future generation MPC is still adventurous.

Current trends suggest that network for next generation MPC will contain a huge amount of processing units. According to the Moore's Law, number of transistors in integrated circuits doubles approximately every two years. Followed by the International Technology Roadmap for Semiconductors (ITRS),[9] microprocessors designed for high performance are expected to contain over 17 billion transistor by the year of 2020. Nevertheless, until in the middle of 2013 the transistors within a single chip counted are over 2.27 billion (Intel Sandy Bridge E 6C) with latest technologies. Recent invention of single-atom transistor[10] shows the precise possibility to break the over-billions barrier of transistors in a single processor. This rapid development is dominated by todays increasingly application driven[11] technology. This technology is focused on low cost and high performance as the steering concern. This concern emerge the system-on-chip (SoC) in which the implementation and integration of an entire system (microcontroller, memory blocks, timers, voltage regulators, and else) onto the same silicon die has become technically feasible. Consequently, the complexity of communication between these intellectual property blocks has also increased due to the shrinking geometry of the SoC. As a result, global interconnects are becoming the performance bottleneck for high performance system.[12,13] These long interconnections are actually acting as the performance barrier in terms of communication latency and power consumption. Specially, for the local interconnection the performance is good whereas for global interconnection of a network consisting of

high number of nodes, that is a nightmare. Moreover, global interconnects are affected in terms of noise, scalability and reliability. To resolve the communication problem of global interconnects, network-on-chip (Noc) is introduced.

The NoC[14] is an efficient on-chip communication architecture for SoC which enable of integrating a massive number of computational and storage blocks on a single chip. NoC as a revolutionary methodology solving the performance limitations arising out of long interconnects, outperforming more mainstream bus architectures.[15] NoC implementation of any interconnection network must address the following problems[16]:

- Scalability: It is essential to accommodate a large number of transistors and reduce the design productivity gap[17] on a single system, in order to provide scalability. NoC can improve the design productivity gap by supporting modularity and reuse of complex cores.[18] On-chip networks will likely use networks with lower dimensionality to keep wire lengths short.[19] However, the scalability of currently proposed solutions, including honeycomb structure,[20] 2-D mesh[21] and butterfly fat tree structure,[22] is either insufficient or unexplored.
- Energy-efficiency: Interconnection network is responsible to consume a considerable amount of power, research[17] suggest that over 50% of system power is consumed by the interconnections and its global wires.[23] Hence, the concern of energy efficiency relies on addressing power consumption of the system.
- Customizability: It is prior demand to have a customizable NoC design in order to have best negotiation with the application. Also to compromise the network with the given power and area.
- Fault-tolerance: The PEs and communication links could fail without any prior notice. On this concern, it is highly desirable to have a NoC design which can provide certain protection of the system under node/PE or link failures.
- Planarity: Planarity suggests the availability of the network topology on a flat surface. The nature of the network topology greatly facilitates the layout of the chip and it should be considered in the design.[24,25]

Vertical and horizontal or combined with diagonal interconnection architecture, both were considered for VLSI implementation.[26] For example, HTN[27] is a vertical and horizontal architecture where as RDT,[16] King topology,[28] THIN,[29] MMN[30] are combined with diagonal architecture implemented for NoC.

The main objective of this paper is to find a suitable network for interconnecting a large number of nodes while keeping small diameter. It has already been shown that, mesh network is the simplest network and also easy to implement on a VLSI area. In case of minimal distance mesh with wrap (midimew)-around links network, it is an optimal topology in the sense that there is no direct symmetric network of degree 4 with lower diameter or average distance.[32] With this key motivation, we propose a

HIN called midimew connected mesh network (MMN). MMN consists of multiple basic modules (BM) which is a 2D-mesh network. The BMs are hierarchically interconnected by midimew network.[32] It is shown that, the MMN possesses several attractive features, including constant degree, small diameter, low cost, small average distance, moderate bisection width, and high fault tolerant performance than that of other conventional and hierarchical interconnection networks. In addition, to implement the level-3 MMN, only four layers are needed on a VLSI area.

In this paper, we address the architectures of the MMN, evaluate its static network performance. In addition, we have implemented the level-3 MMN on a NoC VLSI area. We also propose a routing algorithm for MMN. The static network performance will be evaluated in terms of node degree, network diameter, cost, average distance, bisection width, and arc connectivity.

This paper is organized as follows. Section 2 presents detail description of basic structure of the MMN. Static network performance of MMN is discussed in Sec. 3. In Sec. 4, the NoC implementation of the level-3 MMN and the properties of a MMN are discussed. Finally, Sec. 5 concludes this paper.

2. Midimew-Connected Mesh Network

The MMN[31] is a HIN consisting of multiple BMs that are hierarchically interconnected for a higher level network. The initial building block or BM for MMN is a 2D mesh network. BM is refereed to level-1 network. Higher level network is formed as a midimew network by consisting multiple BMs.

2.1. *Structure of MMN*

2.1.1. *Basic module of MMN*

The BM of the MMN is a 2D-mesh network of size $(2^m \times 2^m)$. It consists of 2^{2m} PE or nodes with 2^m rows and 2^m columns. Here m is a positive integer. Value of m could be any number but preferable one is $m = 2$. If $m = 1$, then the network degenerates to a hypercube network. Diameter of hypercube network increases with network size; hence it is not a suitable network for massive operation. On the other hand, $m = 2$ makes the network suitable for hierarchical architecture because it has better granularity than the large BMs. In addition, $m \geq 3$ makes the network larger and the granularity of the family of networks is coarse. If $m = 3$, then the size of the BM becomes 8×8 with 64 nodes. Correspondingly, the level-2 network would have 64 BMs. In this case, the total number of nodes in a level-2 network is $N = 2^{2\times3\times2} = 4096$ nodes, and level-3 network would have 262,144 nodes. Clearly, the granularity of the family of networks is rather coarse. In the rest of this paper, we consider $m = 2$, therefore, we focus on a class of MMN $(2, L, q)$ networks. Node degree for the network of the BM is bounded by 4. Total possible links without increasing the degree of BMs is $2 \times 2^{(2m)}$. The assigned number of links for connecting nodes in BM

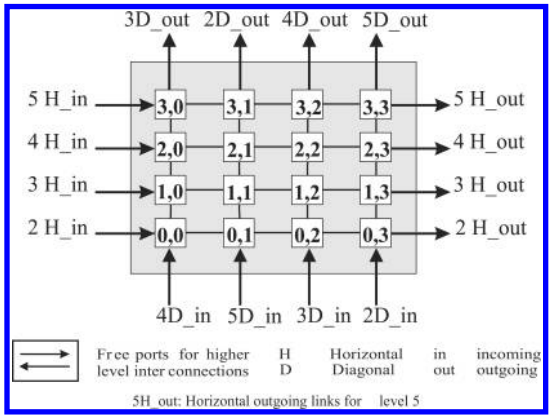

Fig. 1. BM of MMN.

or level-1 network are $2 \times 2^m(2^m - 1)$. As a result the BMs have some free links at the contours. Figure 1 shows a (4×4) BM of MMN with its free links assignment. The free links of BMs are assigned for higher level interconnection. Each BM has $2^{(2+m)}$ free links for higher level interconnection. Based on the location of the nodes the free links of the BM are two types, interior and exterior free links. All free links, typically one or two of the exterior PEs are used for inter-BM connections to form higher level networks. All links of the interior nodes are used for intra-BM connections.

2.1.2. *Higher level networks of MMN*

Midimew-around links network is a class of circulant graphs of degree 4.[32] Midimew is a mesh-based network with wrap around links. Midimew network with same number of nodes like a mesh network has $2^m + 2^m$ wrap around links with $2 \times 2^m(2^m - 1)$ mesh based links. That gives $2 \times 2^{(2m)}$ in total links for midimew network. Midimew network is minimum diameter and average distance of all degree 4 networks. With this motivation, the midimew network is used for higher level interconnection in MMN.

Higher level networks of MMN are the combination of mesh and midimew network. Successively higher level networks of MMN are built by recursively interconnecting 2^{2m} immediate lower level sub-networks in a $(2^m \times 2^m)$ midimew network. Let us consider, BMs of 16 nodes with four rows and four columns mesh network. Now, we consider a midimew network of 16 nodes with four rows and four columns as well. As the midimew network is assigned for higher level interconnection, now each node of midimew network is a BM of 16 nodes. Hence, a level-2 MMN is composed of 16 BMs. Similarly level-3 MMN have 16 level-2 MMN or 64 BMs. The expansion of MMN for level-4 and level-5 is done in the same manner. Figure 2 illustrates the architecture of level-2 MMN originated by combining mesh and midimew network.

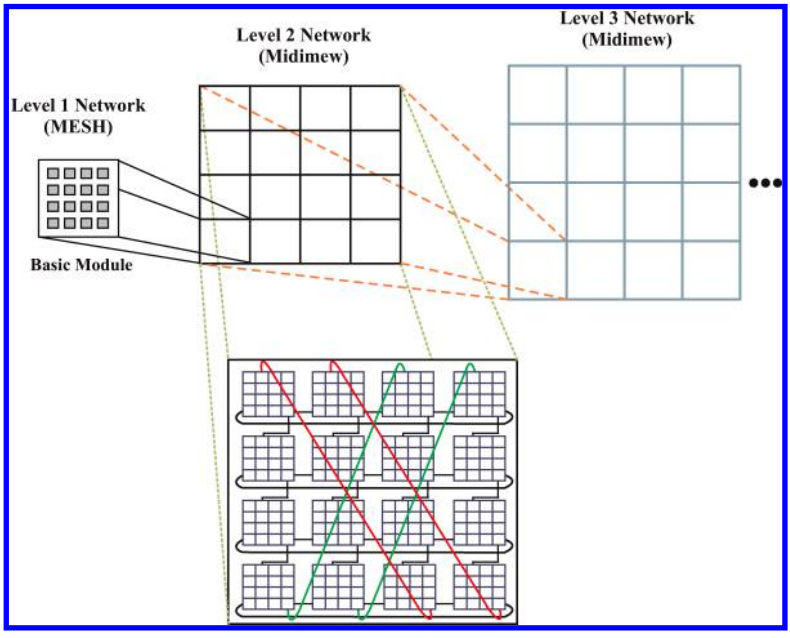

Fig. 2. Hierarchy of MMN.

It is useful to note that for each higher level interconnection, a BM uses $4 \times 2^{2q} = 2^{q+2}$ of its free links, 2^{2q} free links for diagonal interconnections and 2^{2q} free links for horizontal interconnections. Here, $q \in \{0, 1, \ldots, m\}$ is the inter-level connectivity. $q = 0$ to minimal inter-level connectivity, while $q = m$ leads to maximum inter-level connectivity.

The highest level network which can be built from a $(2^m \times 2^m)$ BM is $L_{\max} = 2^{m-q} + 1$ with $q = 0$ and $m = 2$, $L_{\max} = 5$, BM has $2^{q+2} = 16$ free links. With $q = 0, 4$ free links are used for each higher level interconnection. So without increasing the degree of the network maximum level 5 could be interconnected within this network. Hence, level-5 is the highest possible level. The total number of nodes in a network having $(2^m \times 2^m)$ BMs is $N = 2^{2mL}$. If the maximum hierarchy is applied then number of total nodes which could be connected by MMN (m, L, q) is $N = 2^{2m(2^{m-q}+1)}$. For the case of 4×4 BM with $q = 0$, a MMN network can contain over 1 million nodes.

2.1.3. *Addressing of nodes*

Processing elements (PEs) or nodes in the BM of MMN are addressed by two base-4 numbers based on direction, X-direction and Y-direction. Nodes in the BM are addressed by two digits, first one is representing row index or coordinate of X-direction and second one is representing column index or coordinate of Y-direction. Nodes in higher level network are addressed by combination of that particular

level with subsequent lower level. In general for a level-L MMN, the node address is:

$$\begin{aligned} A &= A^L A^{L-1} A^{L-2} \dots A^2 A^1 \\ &= a_{n-1} a_{n-2} a_{n-3} \dots a_2 a_1 a_0 \\ &= a_{2L-1} a_{2L-2} a_{2L-3} a_{2L-4} \dots a_3 a_2 a_1 a_0 \\ &= (a_{2L-1} a_{2L-2})(a_{2L-3} a_{2L-4}) \dots (a_3 a_2)(a_1 a_0), \end{aligned} \tag{1}$$

where the total number of digits is $n = 2L$. The first group $(a_1 a_0)$ contains address of level-1, second group $(a_3 a_2)$ of level-2 and $(a_{2L-1} a_{2L-2})$ for level-L. So any node address for BM consists of one group with only two digits only as $(a_1 a_0)$, for level-2 network address of a node consists of four digits with two groups and so on. More precisely, an address of a node in BM can be $(x, y) = (3, 1)$, only two digits. For level-2 the address of nodes need another set of coordinate as $(X, Y)(x, y) = (2, 2), (3, 1)$. The detailed architecture of MMN was presented in Ref. 31.

The construction of higher level MMN from lower sub-level network is defined by the assignment of free links of BM. This process has been done quite carefully so as to minimize the higher level traffic through the BM and also to maintain short route. The connecting nodes to connect lower subnetworks to form higher level networks are assigned based on free links assignment. For example, if we consider a (4×4) BM and $q = 0$, then 4 out of 16 free links of each BM will be used to connect the immediate higher level network and so on. The address of a node n^1 encompasses in BM_1 is represented as $n^1 = a^1_{2L-1} a^1_{2L-2} a^1_{2L-3} a^1_{2L-4} \dots a^1_3 a^1_2 a^1_1 a^1_0$. The address of a node n^2 encompasses in BM_2 is represented as $n^2 = a^2_{2L-1} a^2_{2L-2} a^2_{2L-3} a^2_{2L-4} \dots a^2_3 a^2_2 a^2_1 a^2_0$. In MMN, the node n^1 in BM_1 and n^2 in BM_2 are connected by a link if the following condition is satisfied,

$\exists i\{a^1_i = (a^2_i + 1) \bmod 2^m \wedge \forall j(j \neq i \rightarrow a^1_i = a^2_i)\}$
where $i\%2 = 0, i, j \geq 2$
$\exists i\{a^1_i = (a^2_i + 1) \wedge \forall j(j \neq i \rightarrow a^1_i = a^2_i)\}$
where $a^1_i = (2^m - 1), i\%2 = 1, i, j \geq 2$
$\exists i\{a^1_i = (a^2_i + 1) \bmod 2^m \wedge \forall j(j \neq i \rightarrow a^1_i = a^2_i + 2)\}$
where $i\%2 = 1, i, j \geq 2$

In a level-2 MMN, a BM connects with its four neighbors by four links (two for horizontal and two for diagonal neighbors) according to the assignment of free links of BMs. Figure 1 shows the assignment of free links. Let us consider a BM having address $(0, 0)(x, y)$. This BM will be connected with its four neighbors, BM $(0, 1)(x, y)$ and $(1, 0)(x, y)$ with general links, $(3, 2)(x, y)$ and $(0, 3)(x, y)$ with wrap-around links. For a BM $(2, 2)(x, y)$, the connecting links exist with BM $(2, 3)(x, y)$, $(2, 1)(x, y)$, $(1, 2)(x, y)$ and $(3, 2)(x, y)$. Here $(x, y) = 0$ to 3. The rest BMs are connected in the same manner.

```
1.Routing of MMN (s,d);
  Source, s=(s2L-1, s2L-2),(s2L-3, s2L-4) ,..... (s3, s2),(s1, s0);
  Destination, d=(d2L-1, d2L-2),(d2L-3, d2L-4) ,..... (d3, d2),(d1, d0);
  Tag, t=(t2L-1, t2L-2),(t2L-3, t2L-4) ,..... (t3, t2),(t1, t0);
5.Group, g;
  Route Direction, RD;
      for j= 2L down to 2;
           if j = even && {(dj - sj + 2^m) mod 2^m} ≤ 2^m/2
                RD = positive;
10.        else if j = odd && | dj - sj |+| dj-1 - sj-1 |<2^m
                RD = positive;
           tj = (dj - sj + 2^m) mod 2^m;
           else
                RD = negative;
15.        tj = {2^m-(dj - sj + 2^m) mod 2^m};
           g = get_Group_number (s, d, RD);
           While (tj = 0) do
                if (j mod 2)=0
                     outlet_node = outlet_x(g,⌊j/2⌋+1, Horizontal, RD);
20.                  outlet_node = outlet_y(g,⌊j/2⌋+1, Horizontal, RD);
                endif;
                if (j mod 2)=1
                     outlet_node = outlet_x(g,⌊j/2⌋+1, Diagonal, RD);
                     outlet_node = outlet_y(g,⌊j/2⌋+1, Diagonal, RD);
25.             endif;
                BM_routing(outlet_node , outlet_node );
                if RD = positive
                     send packet to next BM;
                else
30.                  send packet to previous BM; endif;
                tj = tj - 1;
           endwhile;
     endfor;
     BM_routing(t1, t0);
35.end.
1.   BM_routing(tx,ty);
     Source; (s1, s0);
     Destination; (d1, d0);
     tag; (t1, t0);
5.        t1 = d1 - s1;
          t0 = d0 - s0;
          while(t1 != 0) do
                if t1 > 0
                     move packet to upper node; t1 = t1 - 1; endif;
10.             if t1 < 0
                     move packet to lower node; t1 = t1 + 1; endif;
          endwhile;
          while(t0 != 0) do
                if t0 > 0
15.                  move packet to right node; t0 = t0 - 1; endif;
                if t0 < 0
                     move packet to left node; t0 = t0 + 1;
                endif;
          endwhile;
20.  end.
```

Fig. 3. Routing algorithm of MMN.

2.1.4. *Routing algorithm for MMN*

Routing of messages in the MMN is performed from top to bottom fashion as in TESH network.[8] Routing of highest level is done first, the lower level routing at last. BM has outlet/inlet port for higher levels. When a particular transaction of packet is set up from a source to destination, first the shortest path is calculated. Based on the shortest path, outlet port for source and inlet port for destination are fixed. The packet uses the outlet port to reach at highest level sub-destination and continue to move through the sub-network to lower level sub-destination until it reaches its final destination. Horizontal routing is performed first, once the packet matches the destination column then diagonal routing starts.

To keep the routing simple, we have considered deterministic strategy. We have followed XY routing or dimension order routing (DOR) for MMN. In DOR, the order of dimension is strictly increasing or decreasing depends on the direction of source to destination. Hence, DOR is very simple and inexpensive to implement, allows the topology to use less hardware. It also provides fast router.

Routing in the MMN is strictly defined by the source node address and the destination node address. Let a source node address be $s = s_{2L-1}, s_{2L-2}, s_{2L-3}, s_{2L-4}, \ldots s_3, s_2, s_1, s_0$, a destination node address be $d = d_{2L-1}, d_{2L-2}, d_{2L-3}, d_{2L-4}, \ldots d_3, d_2, d_1, d_0$,

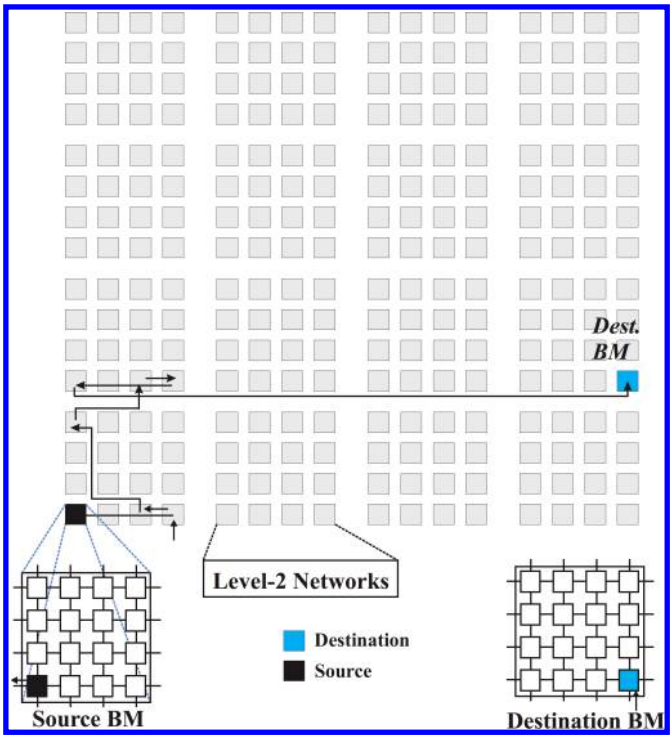

Fig. 4. An example of routing.

and a routing tag be $t = t_{2L-1}, t_{2L-2}, t_{2L-3}, t_{2L-4}, \ldots t_3, t_2, t_1, t_0$ where, $t_i = d_i s_i$. Figure 3 shows the routing algorithm for the MMN. The function *get_group_number* gets a group number and arguments are s, d and routing direction.

Let us consider an example in which a packet is to be routed from source node 000000 to destination node 130303. In this case, routing is to be done at level-3, therefore the source node sends the packet to the outlet node of level-3, 003030, whereupon the packet is routed at level-3, as shown in Fig. 4. To avoid clutter diagonal wrap-around links are not shown in Fig. 4. After the packet reaches the level-2 (1, 1) network, then routing within that network continues until the packet reaches the BM (1, 0). Finally, the packet is routed to its destination. Here we assumed that, all the links of MMN are bidirectional full-duplex links. Figure 4 illustrates the routing from source node 000000 to destination node 130303.

3. Static Network Performance

Several topological properties and performance metrics of interconnection network are closely related to many technological and implementation issues. The static network performances do not reflect the actual performance but they have a direct impact on network performance. In this section, we discuss about several performance metrics. For the performance evaluation, we have considered mesh, torus, TESH network and the proposed MMN. For fair comparison, all considered networks have degree of 4. Some performance metrics like diameter and average distance of MMN and TESH were evaluated by simulation, the other metrics like Wiring Complexity, cost were evaluated by their corresponding equations. Most of these properties are derived from the graph model of the network topology.

3.1. *Node degree*

Node degree is the maximum number of neighbor nodes are directly connected with a node. It refers to the number of links at a node. Constant node degree is preferable for networks. Network with constant degree is easy to expand. Also the cost is related to the node degree proportionally. For fair comparison, we have considered degree 4 network. It is shown in Table 1 that the degree of the mesh, torus, TESH

Table 1. Network performance evaluation.

Network	Degree	Diameter	Cost	Average distance	Arc connectivity	Bisection width	Wiring complexity
2D Mesh	4	30	120	10.67	2	16	480
2D Torus	4	16	64	8	4	32	512
TESH (2, 2, 0)	4	21	84	10.47	2	8	416
MMN (2, 2, 0)	4	17	68	9.07	2	8	416

and MMN are equal, it is 4. Node degree of these networks are independent of network size.

3.2. *Diameter*

Diameter refers to the maximum distance between any pair of source and destination. In other words, the number of maximum links to cross for any transaction with a pair of nodes in a given network is diameter. Diameter indicates the locality of the network. Latency and message passing time depend on the diameter. Small diameter gives better locality to the network. Hence, smaller diameter is convenient. We have evaluated the diameter of the TESH and MMN network by simulation and mesh and torus network by their static formula and the results are presented in Table 1. Clearly, the MMN has a much smaller diameter than that of TESH and mesh networks and a slightly large diameter than that of torus networks.

3.3. *Cost*

Cost is one of the important parameter for evaluating an interconnection network. Though the actual cost of a system depends on the implemented hardware and network in total but node degree and diameter effect the performance metrics of the network including message traffic density, fault tolerance and average distance. If the node degree is increased, the router cost is increased of the network. In correlation, the diameter represents the size of a network which translates into cost. Low diameter imposes low cost, small space and better performance, while high diameter requires high cost, large space and low performance. Therefore, the product (diameter $\times$ node degree) is a good criterion to indicate the relationship between cost and performance of a network.[33] Hence, it can give a pre-idea about the network before installation. The cost of different networks is plotted in Table 1. The MMN is less costly than mesh and TESH and slightly higher than torus network.

3.4. *Average distance*

The average distance is the average of all distinct paths in a network. Average distance reflects the ease of communication within the network i.e., average network latency. A small average distance results small communication latency. In store and forward communication which is sensitive to the distance, small average distance tends to favor the network. But it is also crucial for distance-insensitive routing, such as wormhole routing, since short distances imply the use of fewer links and buffers, and therefore less communication contention. We have evaluated the average distances for MMN, and TESH network by simulation and mesh and torus networks by their corresponding formulas and the results are tabulated in Table 1. It is shown that the average distance of MMN is lower than that of mesh and TESH networks, and slightly higher than that of torus networks.

3.5. *Bisection width*

The bisection width (BW) refers to the minimum number of communication links that must be removed to partition or segment the network into two equal halves. Small BW imposes low bandwidth between two parts. Nevertheless, large BW requires lots of wires and is difficult for VLSI design. Hence, moderate BW is highly desirable. BW is calculated by counting the number of links that must to be eliminated from level-L MMN. Table 1 show that, BW of the MMN is exactly equal to that of the TESH network and lower than that of mesh and torus network.

3.6. *Arc connectivity*

The arc connectivity of a network suggests the minimum number of arcs that must be removed from the network to break it into two disconnected networks. It measures the robustness of a network and the multiplicity of paths between nodes over the network. High arc connectivity improves performance during normal operation, and also improves fault tolerance. A network is maximally fault-tolerant if its connectivity is equal to the degree of the network. From Table 1 it is clear that for MMN and TESH, the arc connectivity is exactly equal. Nonetheless, arc connectivity of torus is equal to its degree, thus more fault tolerant than others.

3.7. *Wiring complexity*

The wiring complexity of an interconnection network refers to the total number of links required to form the network. It has a direct correlation to hardware cost and complexity. In a (4×4) mesh network (four rows and four columns), each row has three assigned links and $3 \times 4 = 12$ links for four rows, similarly for four columns 12 links are exist. Hence, a (4×4) mesh network has 24 assigned links. For a (4×4) torus network additional eight links are assigned with (4×4) mesh network as wrap around links, results 32 links in total. Now, a (16×16) 2D-mesh and 2D-torus networks have $\{N_x \times (N_y - 1) + N_x \times (N_y - 1)\} = 16 \times (16 - 1) + 16 \times (16 - 1) = 480$ and $(2 \times N_x \times N_y = 2 \times 16 \times 16) = 512$ links, respectively. N_i represents the number of nodes in the ith dimension. The wiring complexity of a level-L MMN, and TESH networks is $(\#$ of links in a BM $\times\, k^{2(L-1)} \sum_{x=2}^{L} 2(2^q) \times k^{2(L-1)})$. Considering, $m = 2$, a BM of MMN, and TESH network have 24 links. The level-2 networks of MMN and TESH are composed of 16 BMs. Hence, 16 BMs have $16 \times 24 = 384$ links. To connect 16 BMs with each other additional 32 links are required for MMN and TESH. In total, the number of links of a level-2 MMN, and TESH are $384 + 32 = 416$. Table 1 shows that the total number of links of MMN is lower than that of mesh and torus network and exactly equal to that of TESH network.

The static network performance indicates that, torus network has better performance than MMN except in the term of wiring complexity. Now, torus network has

$N_x + N_y$ long wrap-around links, where $N_x \times N_y$ is the network size. In case of MMN, from level-2 to level-L, each level contains $(2^m/2) + (2^m/2)$ wrap-around links. Also the wrap-around links of MMN do not increase with network size, instead they increase with higher levels. But in torus they increase with network size. Hence, the implementation of MMN is easier than torus.

3.8. *Properties of MMN*

3.8.1. *Property 1*

MMN has small diameter and average distance. Now the power consumption of an interconnection design rely on several factors, among them diameter and average distance plays a crucial role. Hence, smaller diameter and average distance possess the characteristics of energy efficiency of NoC design.

3.8.2. *Property 2*

With constant node degree of 4, moderate bisection width, fault tolerant structure and easy routing scheme, MMN provides fault tolerance inherently.

3.8.3. *Property 3*

With very simple structure of BM and higher level networks it is worthy to point out that MMN could be easily customized as per demand.

4. NoC Implementation of MMN

Earlier it has already presented that MMN has simple hierarchical structure, hence suitable for NoC implementation. For routing, necessary guidance is provided by X-architecture. In this section, we study the feasibility of laying out the MMN on a layer with current and future VLSI technologies.

4.1. *Links of BM*

4.1.1. *Links*

A link is a direct connection between two nodes. Link can be established with neighboring nodes. For the wrap around links nodes are connected with its neighbor logically, not with nearest neighbor. Communication links can be two types, either unidirectional or bidirectional. For unidirectional links, transmitting and receiving links are fixed. Packet will be sent through transmit links and packet will received only by receiving links. Bidirectional links uses same links for both transmission and reception of packets.

Table 2. Links of BM.

G#	Direction	Source node	Linking method	Links length	No. of links	NG
1	X	00	$(x, y) \rightarrow (x + 1), y$	1	$N - 1$	N
1	Y	00	$(x, y) \rightarrow x, (y + 1)$	1	$N - 1$	N

4.1.2. *Jump crossing links*

Jump crossing refers to introduction of a junction point where two links intersect with each other but not an end to any of the links. In other words, jump crossing occurs where two wire overlap each other. In VLSI implementation two jump crossing links can not be laid on same layer.

If we assume that all nodes or PEs are on the same layer for MMN then, all links of the MMN can be laid on a small number of layers. Table 2 describes the links of BMs of MMN.

4.2. *Links of level-3 network*

Level-3 MMN consists of 16 level-2 network where each level-2 network contains 16 BM. BMs or level-2 networks are interconnected with its logically adjacent BMs or level-2 networks respectively to form level-3 network.

All the links of level-3 network are categorized into 10 groups based on their BM and level-2 network size. Table 3 describes the links. The first column shows the group no. (#); the second column shows direction (D); the fourth column shows the length of links in each group normalized against the shortest link and the number of links in each group; the last column shows the number of groups (NG) in the MMN. For clarity Fig. 5 introduces the depicted picture. Figure 5 shows that, links having different directions are deemed to be cross jumping with each other. So according to the directions all links can be classified into sets as, horizontal (groups 1, 2, 3, 7); vertical (groups 4 and 8) and diagonal (groups 5, 6, 9, 10). Table 4 presents the set of links for each layer.

But diagonal links have two types based on their angle of direction. So links of MMN level-3 network are distributed into four sets finally.

For clarity Fig. 6 depicts the links on different layers. It is clear from Fig. 6 that link of group 1, 2, 3, 7 can not be laid with group 4 or 8 or 5, 6, 9, 10. This condition of lying also stands for groups 4 and 8 with others. So to implement all the links of level-3 MMN network all these groups can not be laid on layer. Hence, more than one layer is required to implement the level-3 MMN.

4.3. *Layers of level-3 network*

There are four groups of links which are jump crossing to each other. Hence, at least 4 different layers are required lay down the whole level-3 MMN. Table 5 summarizes

Table 3. Description of links of MMN level-3 network.

G#	Direction	Source node	Linking method	Links		NG
				Length	No. of links	
1	Y	$(x,y) \leftrightarrow (0,0)$	$(x,y) \leftrightarrow (x,(y+1))$	1	$N-1$	$N \times N^4$
2	X	$(x,y) \leftrightarrow (0,0)$	$(x,y) \leftrightarrow ((x+1),y)$	1	$N-1$	$N \times N^4$
3	Y	$(x,y) \leftrightarrow (0,3)$	$(x,y) \leftrightarrow (x,(y+1)\%N)$	1	$N-1$	$N \times N^2$
				N^2-1	1	$N \times N^2$
4	X	$(x,y) \leftrightarrow (3,1)$	$(x,y) \leftrightarrow ((x+1)\%N,(y+2))$	$N-1$	$3N/2$	N^2
5	XY	$(x,y) \leftrightarrow (3,1)$	$(x,y) \leftrightarrow ((x+1)\%N,(y+2))$	$\sqrt{(N^4+2N^2+8N+5)}$	$N/2$	N^2
6	XY	$(x,y) \leftrightarrow (3,1)$	$(x,y) \leftrightarrow ((x+1)\%N,(y+2))$	$\sqrt{(N^4-N^2+4N+5)}$	$N/2$	N^2
7	Y	$(x,y) \leftrightarrow (1,3)$	$(x,y) \leftrightarrow (x,(y+1)\%N)$	1	$N-1$	N
				N^3-1	1	N
8	X	$(x,y) \leftrightarrow (3,0)$	$(x,y) \leftrightarrow ((x+1)\%N,(y+2))$	$3N-1$	$N-1$	N
9	XY	$(x,y) \leftrightarrow (3,0)$	$(x,y) \leftrightarrow ((x+1)\%N,(y+2))$	$\sqrt{(N^6+4N^4+8N^3-(25/4)N^2+1)}$	$N/2$	1
10	XY	$(x,y) \leftrightarrow (3,0)$	$(x,y) \leftrightarrow ((x+1)\%N,(y+2))$	$\sqrt{(N^6+N^4+N^3-(9/4)N^2+1)}$	$N/2$	1

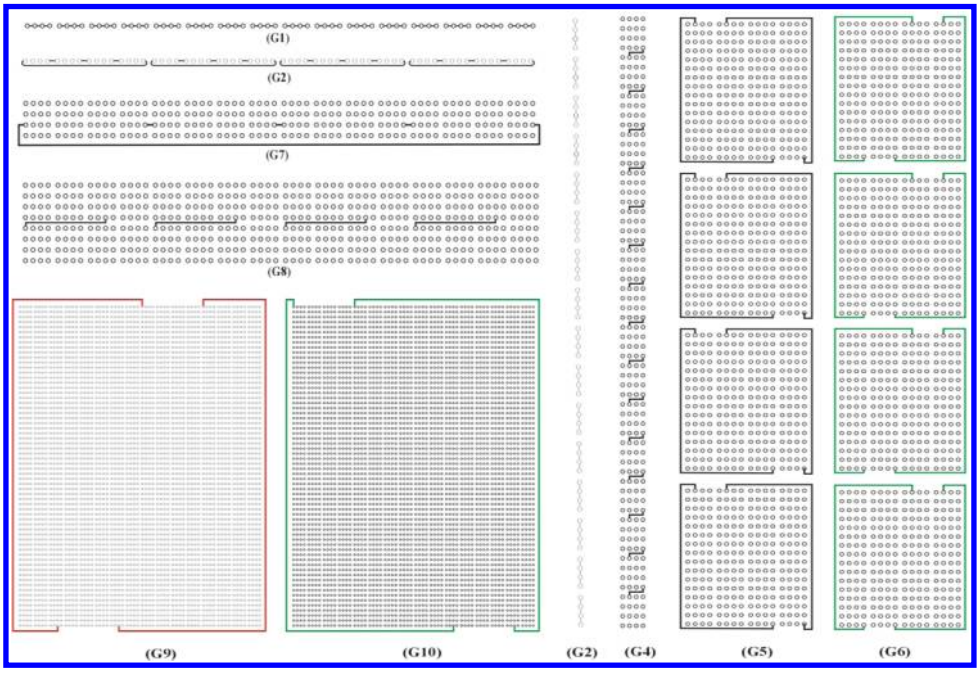

Fig. 5. Links illustration of all groups.

Table 4. Set of link groups based on direction.

Number of set	Direction	Groups
1	Horizontal	1, 2, 3, 7
2	Vertical	4, 8
3	Diagonal ($<90°$)	5, 9
4	Diagonal ($>90°$)	6, 10

the length of lines on each layer of the layout. The intercommunication of the layers is established by additional communication links. These links are bidirectional. Figure 6 shows different layers for the implementation of level-3 MMN.

4.4. *2D versus 3D layers of level-3 network*

The IC size is shrinking and number of PEs in node on a single chip is rapidly climbing up. Consequently, new paradigm for NoC is proposed to compromise with the demand of smart and smaller technology. To compete with the increasing demand of small, 3D transistor[34] is introduced, where a single atom transistor[10] has already come to reality. So 3D paradigm of NoC is also on upcoming track[35,36] for compressing billions of nodes on a small area.

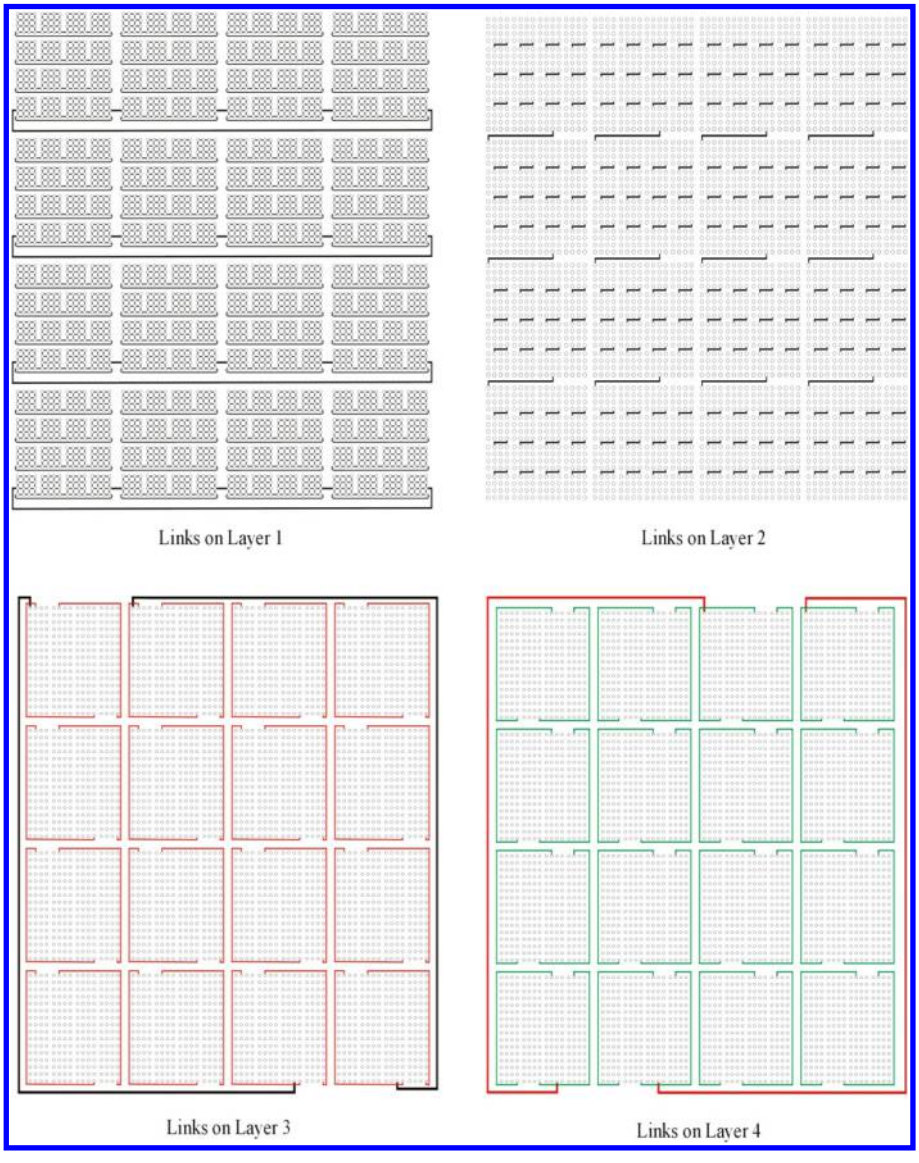

Fig. 6. Links for four different layers. Number below of each set indicating its layer number.

Here Fig. 7 illustrates a 2D communication paradigm of the MMN. Though 2D NoC is much easier to implement and possessing very simple structure, still for large diameter and inefficient average distance makes to think again about NoC paradigm. Figure 7 shows that every communication between inter layer will be performed by layer 1 which is not efficient in the context of power and performance. Though the 3D NoC is beyond the scope of this paper but the necessity of 3D NoC paradigm is well

Table 5. Total length of links on each layer of MMN level-3 network.

Layer	Total length of links
1	$(3N^4 + 3N^3 - 4N^2 + 2)(5N^3 - 2N^2 + 2)/2$
2	$(3N^4 + 3N^3 - 8N^2 + 2N)/2$
3	$(N/2)\{\sqrt{(N^6 + 2N^4 + 8N^3 + 5N^2)}\sqrt{(N^6 + 4N^4 + 8N^3 + (25/4)N^2 + 1)}$
4	$(N/2)\{\sqrt{(N^6 + N^4 + 4N^3 + 5N^2)}\sqrt{(N^6 + N^4 + N^3 + (9/4)N^2 + 1)}$

defined. For clarity, Fig. 8 illustrates a NoC paradigm for 16 node 2D and 3D mesh. It is clear that, 3D design uses less space than 2D.

In our another study,[37] it is shown that the total wire length of the MMN is lower than that of torus network and slightly higher than that of mesh and TESH network. However, the total wiring cost of the MMN is lower than that of mesh, torus and TESH networks. For network implementation there is another method, called 3D Wafer Stack Implementation, which is not used in recent days. In the recent days NoC is widely used. This is why we have chosen NoC implementation for MMN.

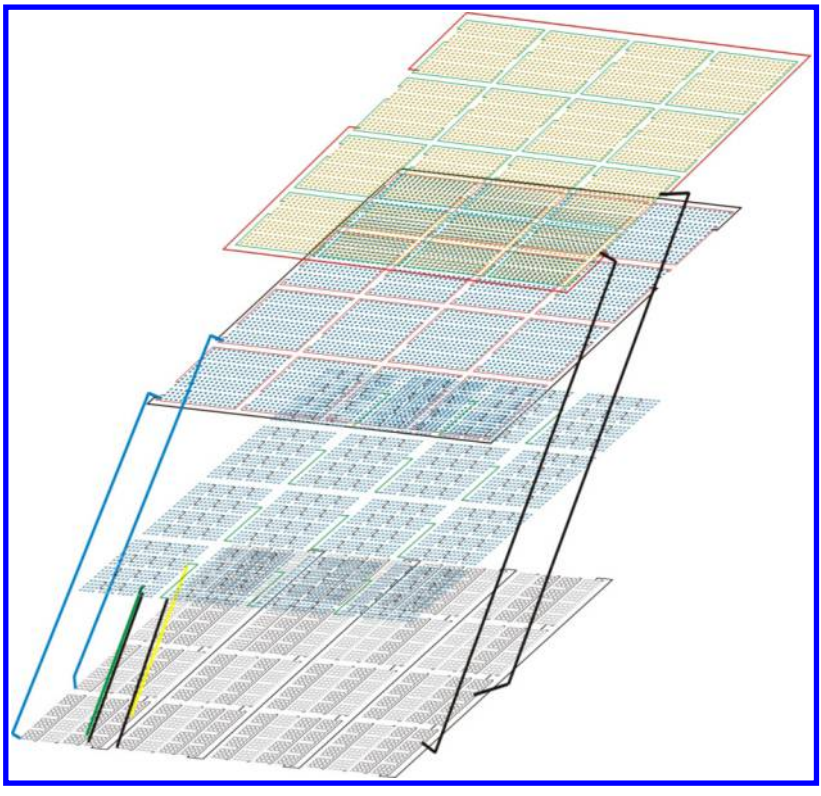

Fig. 7. MMN layer to layer communication via layer 1 (sample view).

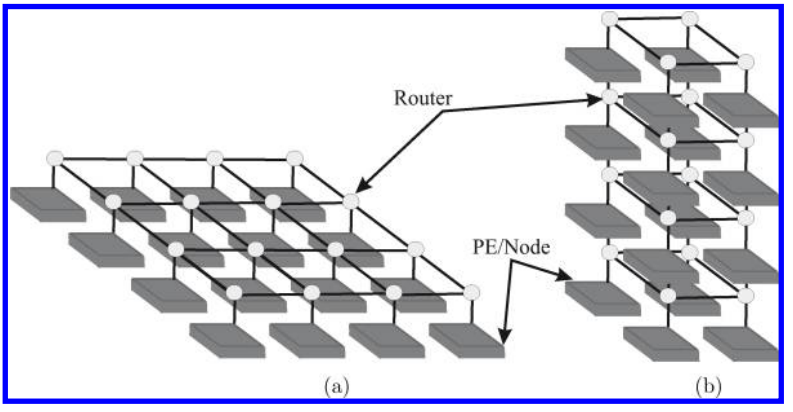

Fig. 8. (a) 2D mesh and (b) 3D mesh.

5. Conclusion

In this paper, we proposed a new hierarchical interconnection network, called MMN. The architecture of MMN, addressing of nodes, and routing of message were discussed in detail. We have also evaluated the static network performance of the MMN, as well as that of several other interconnection networks. From the static network performance, we have seen that with the same node degree, arc connectivity, bisection width, and wiring complexity, the diameter and average distance of the MMN is lower than that of the TESH network. In the context of diameter and average distance, the MMN is lower than that of mesh network and slightly higher to that of torus network. Consequently, we have implemented the MMN for scalable NoC designs. The simple structure of MMN is highly suitable for NoC implementation. We have categorized the links of level-3 MMN into four different sets, such that no links on same layer are jump crossing. It is shown that the level-3 MMN can be laid out with four layers, which is feasible with current and future VLSI technologies.

Future research will imply the dynamic communication performance evaluation of MMN with dimension order routing.

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