

# Improving $\mu$ -wire electro-discharge machining operation of polished silicon wafer by conductive coating

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## Abstract

Micro-Wire Electro-discharge machining ( $\mu$ -WEDM) is a nonconventional machining technology which is extensively used for metal based micro fabrication process. This is a non-contact machining process where material removal is taken place by electro-thermal action.  $\mu$ -WEDM process is difficult to be applied for semiconductor material like Silicon (Si). In this paper a new approach is proposed for machining polished Si (p-type, resistivity 1-50  $\Omega$ -cm) wafer. In this method, initially Si workpiece is coated with a conductive material (gold for this study) and then  $\mu$ -WEDM operation is carried out. Finally, after WEDM operation, the conductive layer is removed from the polished Si substrate without damaging the substrate. WEDM process stability was found to be improved (up to 60 times for certain machining condition) if coated Si wafer is used as compared to uncoated Si workpiece. Material removal rate was also found to be increased by a good margin ( $\sim$  100% maximum) for coated Si wafer. Overall this new method of  $\mu$ -WEDM operation of polished Si wafer has been found to be more efficient and useful.

**Keywords:**  $\mu$ -WEDM, polished Si wafer, Conductive coating

## 1. Introduction

Electrical discharge machining (EDM) is a widely used nonconventional machining process. In EDM, material removal is taken place by means of repetitive electric discharges between the tool and the workpiece where no physical cutting force is involved. Wire EDM (WEDM) is a type of EDM operation where the cutting tool is a rotating wire spool and the electric discharge energy is applied between the wire and the workpiece. WEDM is broadly used for electrically conductive materials because of its physical nature of operation as described above. Micro EDM/WEDM ( $\mu$ -EDM/WEDM) is an emerging machining technology to produce features in micron domain for different engineering applications. The main difference between conventional EDM/WEDM and  $\mu$ -EDM/WEDM lies in the level of discharge energy and size of the tool used during the operation. In  $\mu$ -EDM/WEDM very low discharge energy with high frequency is used ( $\sim$   $\mu$ -Joule). Further, typical tool and feature size in  $\mu$ -EDM/WEDM are in order of less than or equal to 100  $\mu$ m. Similarly axes resolution needs to be in micron domain for the EDM/WEDM process to work in micro field [1]. Nowadays, this machining method has drawn a lot of attentions by the researchers in the field of micro-mold and complex 3D structures fabrication [2,3]. This technology has not only been used for metals but also in practice for wide range of other conducting materials [4-6]. However, not many efforts have been made to machine semiconductor materials like silicon (Si) by EDM or  $\mu$ -EDM. One of the biggest challenges for machining silicon by EDM is its high surface resistance compared to bulk body resistance. Reynaerts et al. [7] proposed two measures in order to overcome this problem. One solution, as suggested by Reynaerts et al. [7] is to adjust the polarity of doped silicon in such a way so that for p-type silicon electrode is negative and silicon is positive and vice versa for n-type silicon. Another solution for the above mentioned problem is to use of conductive plating on the silicon

workpiece. Previously Luo et al. [8] studied slicing of Si wafer from the silicon ingot by Wire Electro Discharge Machining (WEDM). In order to achieve best cutting performance he proposed nickel plating of the silicon to overcome the surface potential barrier. This technique was further investigated by Peng and Liao [9] and they concluded that it is not efficient to use WEDM method for machining pure silicon ingot (without doping). Okamoto et al. [10] developed a multi wire EDM method to slice wafer from silicon ingot to increase the productivity.

Contouring of doped silicon wafer by WEDM to produce micro structures was investigated by Stauffert et al. [11]. Dinesh Rakwal et al. [12] used  $\mu$ -WEDM technology to fabricate high aspect ratio silicon micro electrode array of different shapes. Pervej Jahan et al. [13] carried out a parametric study on micro-machining of p-type Si wafer by  $\mu$ -EDM. Song et al. [14] also investigated  $\mu$ -EDM performance on highly doped p-type Si wafer. Polished silicon mirrors have vast applications in sensors and optical industries. Complex shaped silicon mirrors with various contours can be fabricated using Wire Electro Discharge Machining (WEDM). The technology was first proposed by Takino et al. [15-16] where conventional EDM power [5 to 30 ampere] was used. However, the degradation of the polished surface due to the spark energy should be kept as minimum as possible in order to maintain required optical quality. This can be achieved more efficiently if  $\mu$ -WEDM is used instead of conventional WEDM to machine polished silicon.

In this paper, authors have studied an improved technology to machine polished (mirror quality) Si wafer (p-type and 1 to 50  $\Omega$ -cm resistivity) by  $\mu$ -WEDM method. In this work authors coated the silicon wafer with conductive material (gold for this study), in order to produce high conductive gold-silicon-gold composite. This enhances the machining rate quite significantly and later the coating can be easily removed by simple wet etching method without having any detrimental effect on the polished surface.

Machining performance of gold coated silicon by  $\mu$ -WEDM has been studied and reported here.

## 2. Experimental setup and procedure

In this research a P-type pre polished [mirror quality] silicon wafer of 650  $\mu$ m thickness was used. The wafer was coated with conductive material (Au in this research) using ion sputtering machine (auto fine coater) on the both side before the start of actual WEDMing process. This machine is not capable for very thick coating. The coating thickness depends on time spent for coating. Three types of samples were prepared for the machining experiment. First group of samples was silicon (Si) without any coating; second and third group were Si coated for 5 minutes and 10 minutes respectively. The conductive coating was removed effectively by wet etching process using dilute Aqua Regia (HCl : HNO<sub>3</sub> : H<sub>2</sub>O = 1 : 0.16 : 1). All three types of samples were machined for a comparative study using the WEDM process.

Fig. 1 shows the photograph of the basic experimental setup. A multipurpose machine-tool [17] capable of carrying out  $\mu$ -WEDM was used for this research. A relaxation type RC based EDM/WEDM power supply was used in this study. The stray capacitance of the system was measured to be 13 Pico-Faraday(PF). The micro EDM/WEDM controller of the machine has two digital outputs, namely short/arcing and discharge. The short/arcing and discharge output are activated when the EDM current reaches some predefined threshold value during the machining process. These two digital outputs were

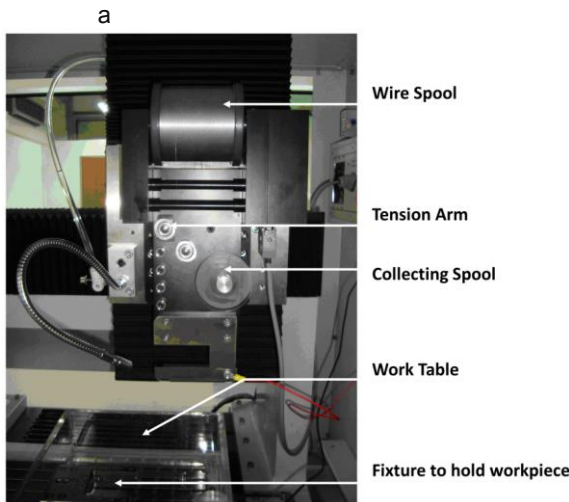


Fig. 1:  $\mu$ -WEDM experimental setup

counted by periodical and manual observation throughout the machining process in order to study the machining stability. The experimental study was performed at different discharge energy level by varying voltage and capacitor combinations both for silicon wafer coated with gold and uncoated silicon wafer. Discharge energy for EDMing process can be defined as follows

$$dE = 0.5 \times C \times V^2$$

where dE is discharge energy  
C is the capacitance value of the RC circuit  
And V is the discharge voltage.

The experimental conditions are given briefly in the table 2.

Table 2: Experimental Conditions

Parameters	Value
Voltage	85V, 95V and 105V
Capacitor	0.1 nF, 1nF and 10 nF
WEDM speed	50micron/second
Wire Material	Zinc coated brass wire
Wire Diameter	70 micro meter
Workpiece	Polished Si wafer coated with gold (Au) for 5 minutes
	Polished Si wafer coated with gold (Au) for 10 minutes
	Polished Si wafer
Programmed length of slot	1mm

Machined samples were characterized using Scanning Electron Microscopy (SEM). SEM imaging was also used to measure the kerf width of the machined slots and to carry out morphological study of the machined surface.

## 3. Results and Discussion

Several experiments were carried out and a number of parameters have been studied (namely material removal rate MRR, stability of machining, surface morphology) in this study.

### 3.1 Study of Machining Stability

In  $\mu$ -WEDM, excess occurrence of short circuit or abnormal arcing will cause slower machining rate. Micro WEDM operation is said to be stable if normal discharge occurs more frequently during machining. In this research short circuit output was monitored periodically for each machining experiment to study machining stability.

Fig. 2 shows occurrence of short/arcing (nos/min), for the machining of gold coated silicon and uncoated silicon at different machining conditions. It was found that  $\mu$ -WEDMing operation is completely impossible at very low discharge energy i.e 0.36  $\mu$ J and 0.45  $\mu$ J, for uncoated Si wafer due to excessive and continuous short circuit detection. Corresponding Voltage and Capacitor value for these energy levels are 85V, 0.1 nF and 95V, 0.1 nF respectively. It can be observed from Fig.2 that almost no short circuit was occurred while  $\mu$ -WEDMing gold coated silicon samples. However, when uncoated silicon is machined the system detects mostly open circuit because of its high resistivity which causes the servo system to follow the forward path and when the wire touches or almost touches the silicon it detects short circuit. Therefore, WEDMing of uncoated silicon generates significant number of short circuits (nos/min) during operation which retards the machining rate and also causes unevenness in the machined slots as explained later in this paper. In Fig. 2 (a) it can be observed that short circuit is higher Si wafer coated with 10 min gold however the difference is insignificant. A possible

reason behind this could be false short circuit detection by the controller due to larger spark for thicker conductive coating.

### 3.2 Study on Material Removal Rate (MRR)

The most important aspect of this study is the machining rate of the polished silicon wafer by WEDM method. In order to study this one mm long slot was machined with various parameters as described in Table 2. The kerf width was measured using SEM and the MRR was calculated accordingly. Fig. 3 shows variation of MRR (uncoated Si, Si coated for 5min, Si coated for 10 min) for different machining condition. All three types of samples show increasing trend of MRR with increasing discharge energy. Moreover, it is clearly evident that machining rate or MRR for gold coated silicon wafer is much higher than uncoated silicon wafer and Si coated with gold for 10 minutes shows higher MRR at low voltage (85V and 95V). The combined resistivity of the Au-Si-Au composite is significantly reduced from bare Si workpiece because of the shunting effect of highly conductive of Au. Mahardika et al. [18] showed in his  $\lambda-\theta-\rho$  theory that resistivity of the workpiece material is a very important

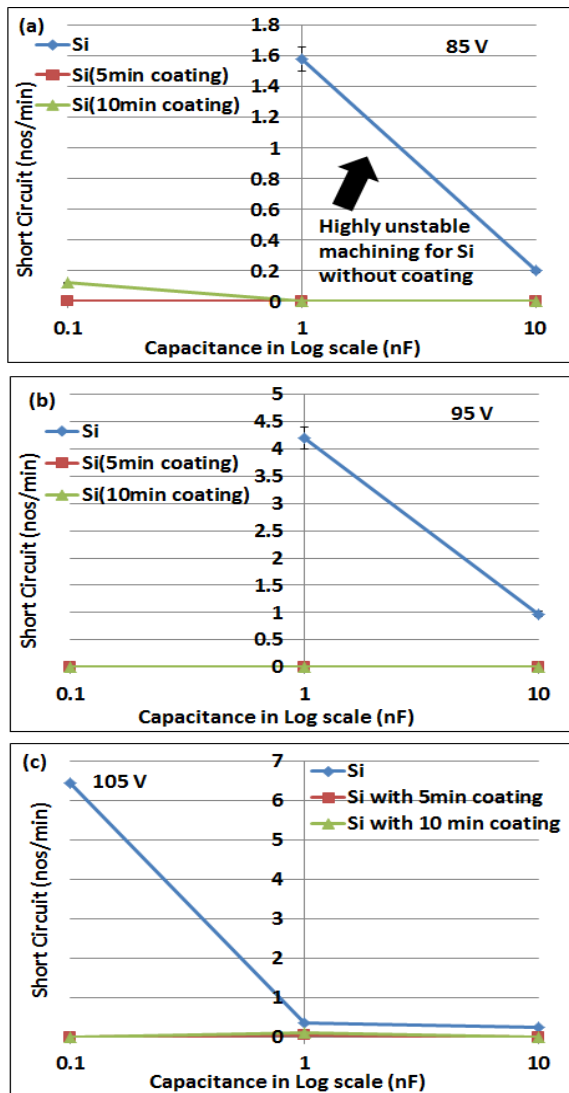


Fig. 2 : Study of stability of WEDM process (for uncoated Si, Si coated for 5minutes and Si coated for 10 minutes )by counting number of short circuits during machining (a)85 V (b) 95V (c) 105V parameter for the machinability study by EDM/WEDM. If the resistivity of the material is decreased the ease of machining by EDM/WEDM is enhanced. The machining rate of gold coated silicon is observed to be much higher because of the above mentioned phenomenon. Another, key factor behind this result is unstable machining for uncoated Si wafer. As discussed earlier (3.1) short circuit detection is significantly high for WEDMing of uncoated Si wafer which retards the machining rate of the material. It was also observed that at lowest energy level (85V and 0.1 nF; 95V and 0.1nF) machining was not even possible for uncoated Si wafer because of continuous detection of short circuit as explained in the earlier section.

### 3.3 Study of Kerf width

Kerf width is a vital factor to study in micro WEDM related research as this parameter determines the achievable resolution of the fabricated feature. Two effects need to be considered during the study of kerf width of the machined slots by WEDM. First is the average value of kerf width and secondly the evenness or uniformity of the slot.

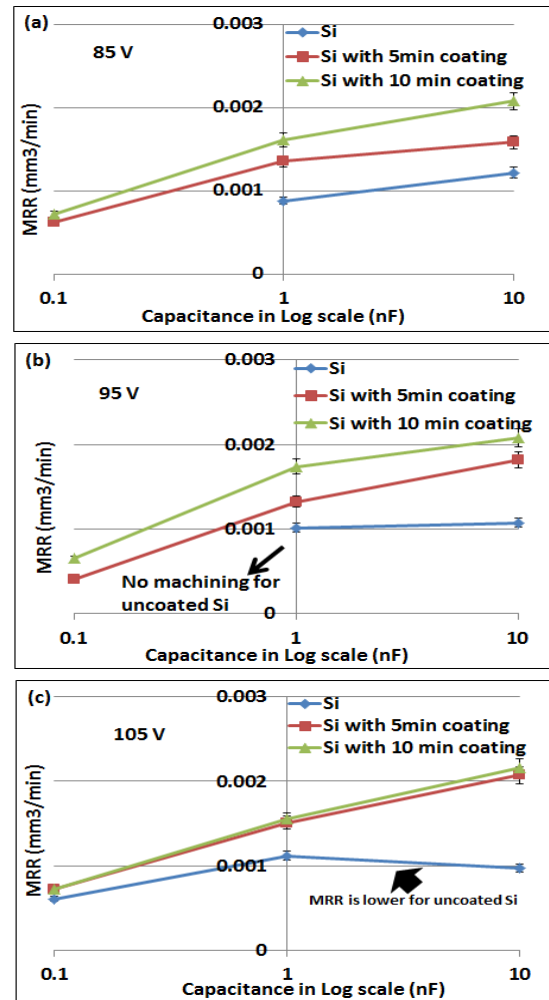


Fig. 3 : Study of Material Removal Rate (MRR) of WEDM process (for uncoated Si, Si coated for 5 minutes and Si coated for 10 minutes) by counting number of short circuits during machining (a) 85 V (b) 95V (c) 105V

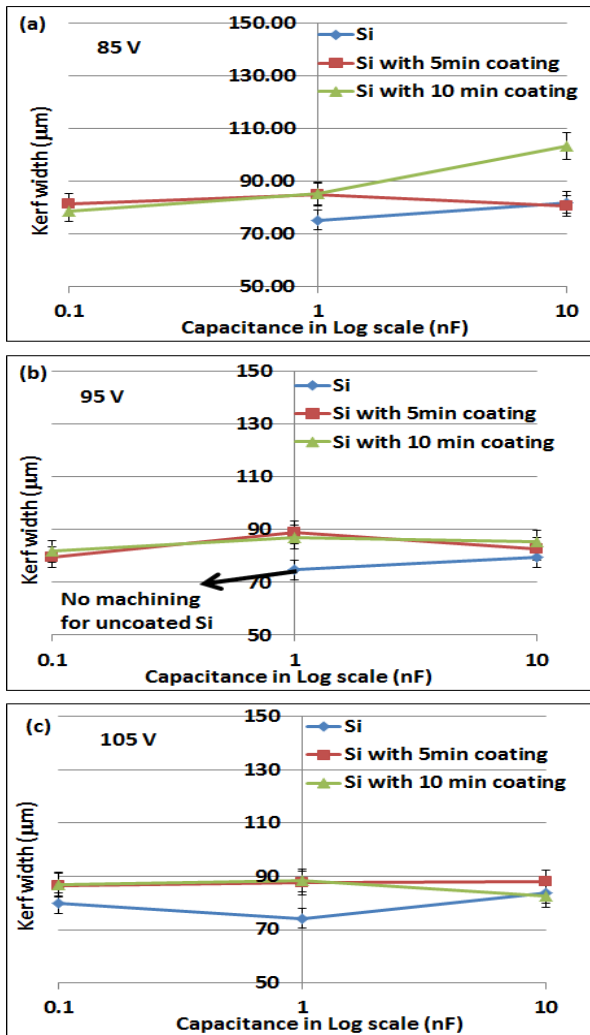


Fig. 4 : Study of kerf width of WEDM process (for uncoated Si, Si coated for 5minutes and Si coated for 10 minutes) by counting number of short circuits during machining (a)85 V (b) 95V (c) 105V

In this study kerf width was measured using SEM microscopy at five different points of each slot. A parameter named as unevenness factor of the slot has been calculated which is the standard deviation of these five values of width of the single slot. Higher value of this factor indicates more uneven slot. Fig. 4 shows the variation of kerf width of the machined slot for different machining conditions for three different samples. The result shows that for the case of coated silicon wafer the average slot width is somewhat higher compared to uncoated Si wafer. The probable reason behind this could be as follows, coating causes the reduction in resistance for overall WEDM setup as mentioned earlier. Therefore, this helps to generate bigger sparks which result in larger kerf width. Interestingly, study of unevenness factor for three different samples

shows (Fig. 5) uncoated Si produces significantly uneven slots as compared to coated Si (~ 3 times higher than Si coated for 5 mins and ~ 1.5 times higher than Si coated for 10 mins). During machining of uncoated Si by WEDM, the system behaves erratically with significant detection of short circuits. This indicates that the probability of physical contact between the wire and Si workpiece is higher and this may cause the wire to be pulled and misplaced. When a spark generates at this condition, machined slots eventually become uneven. However, for the case of Si wafer with 10 minutes coating, the unevenness factor was observed to be higher than Si wafer with 5 minutes coating, which indicates spark size was not consistent for Si wafer with 10 minutes gold coating. Fig. 6 shows the SEM image of machined slots for three samples at an energy level of 105V and 10nF. This figure (Fig.6) also confirms that uncoated Si wafer produces rather wavy and inconsistent slots as compared to coated Si wafer.

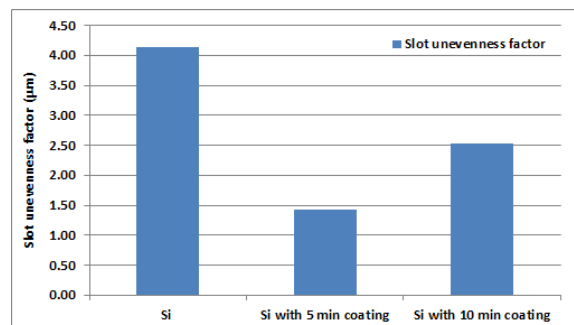


Fig. 5: Study of Unevenness of the Machined Slots by  $\mu$ -WEDM Process for the Three Samples

### 3.4 Morphological Study

To study the morphology of the  $\mu$ -WEDMed surface of coated and uncoated Si wafer, SEM imaging was carried out as shown in Fig. 7. The figure shows the perpendicular surface of the polished Si surface which actually came in contact with the WEDM spark. It is obvious from the figure that the machined surface for uncoated Si wafer is quite rough with visible bumps. Whereas the machined surface for coated Si wafer is remarkably smoother. Further, there is no significant difference between the surface of Si wafer coated for 5 minutes and Si wafer coated for 10 minutes. It was mentioned in section 1 that mirror-quality polished Si wafer was used for this study. The gold coating from the Si wafer was finally removed by a wet etching method using dilute Aqua Regia (HCl, HNO<sub>3</sub> and H<sub>2</sub>O) without damaging the Si substrate. In order to ensure that gold is completely removed, EDX analysis was carried out on the sample after removing gold from the sample. The result of EDX confirms complete removal of gold from the sample.

### 3.5 Application Example ( $\mu$ -Digital Reflector)

This product was machined by the  $\mu$ -WEDM using the temporary coating on Si wafer. Machining conditions were 95 V and 1 nF. This  $\mu$ -digital reflector is used to sense light through reflecting the light or not. This is depending on the structure of the reflector, which includes two parts; one part can reflect the light and the other cannot. Fig. 6 shows the SEM image for the



product.

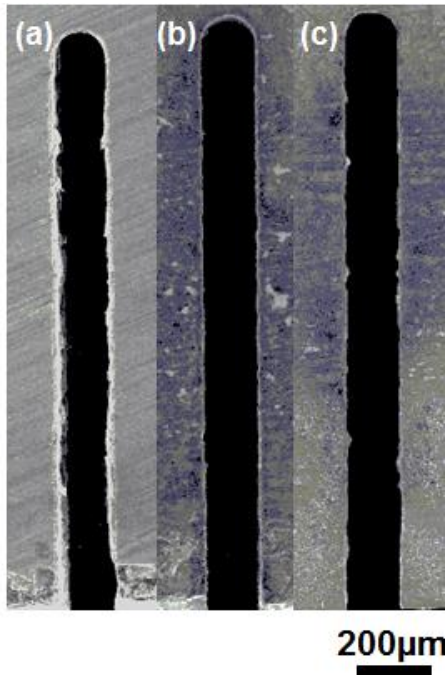


Fig. 6: SEM Image of the Machined Slots by  $\mu$ -WEDM Process (a) for uncoated Si, (b) Si coated for 5 minutes and (c) Si coated for 10 minutes

As shown in the SEM image (Fig.8), the  $\mu$ -reflector machined with high accurate dimensions despite it somewhat designed with a complex shape. The  $\mu$ -reflector length is 3.6 mm and 400  $\mu$ m width as well as it has three trapezoidal cams; the average pitch width of each cam is 500  $\mu$ m. The trapezoidal shape for the cam provides two degrees of freedom in measurement. This trapezoidal shape causes changing in the width of shining part (which senses and reflect the light) during the vertical and horizontal movement for the reflector.

#### 4. Conclusions

This study proposes a new method of  $\mu$ -WEDMing of polished silicon wafer to create silicon based micro features. In this method the wafer is coated with a conducting material like gold and then machining is carried out. Finally gold is completely removed from the end product by wet etching without having any detrimental effect on the machined samples. This new method enhances the machining performance by increasing the material removal rate MRR up to  $\sim$ 100%. Further, the  $\mu$ -WEDM process was observed to be very stable without any significant short circuit detection when gold coated Si wafer sample was used. Finally morphological study of the  $\mu$ -WEDMed surface shows coated Si wafer generates significantly smoother surface as compared to uncoated Si samples. This method of polished Si wafer machining will be very useful for prototyping of miniature sensors and other MEMS based devices.

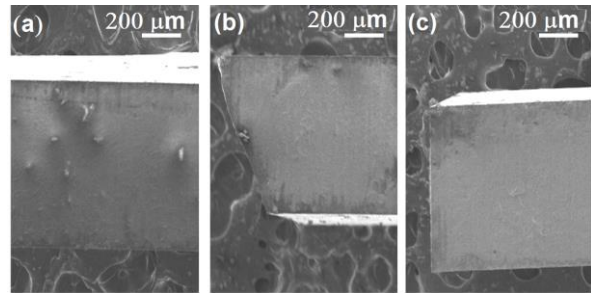


Fig. 7: SEM image of the cut surface of the machined slots by WEDM process (a) for uncoated Si, (b) Si coated for 5 minutes and (c) Si coated for 10 minutes.

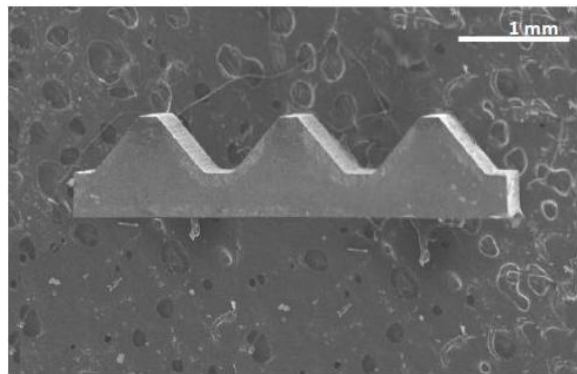


Fig.8: SEM Image of  $\mu$ -Digital Reflector with Machining Condition of 95 V and 1 nF

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