STATISTICAL TIME DIVISION MULTIPLEXING ARCHITECTURES AND DESIGN

15 mU

Sel

Asadullah Shah Asadullah Shaikh Muniba Shaikh Zeeshan Bhatti Nuha Abdullah Zammarh Dini Oktarina Dwi Handayani Zoya Shah



20mV

200mU

Q1 500ns%

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Editors

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18.0 Abstract

A great number of speech coding has been developed in recent years and many others are in their advanced level of development. Most of these encoding algorithms use hybrid methodology of waveform coding and voice coding commonly known as (vocoding). The speech quality of these coders is comparable with Pulse Code Modulation (PCM); a popular encoding technique used in digital telephony.

In this chapter many such encoding algorithms are detailed and compared in terms of bit rates and quality, using subjective and objective measures.

The summary of the coder is given in Table.5. I. The analysis and synthesis of speech is carried out on a frame of 20 ms (160 samples) of speech sampled at 8 kHz sampling frequency. Where each user is generating 50 frames per second.

The LPC coefficients are transmitted normally into LSFs, and vector quantised, 28 bits are reserved for 10 LSFs. The LPC analysis is carried out once for a frame. The Adaptive Codebook (ACB) index and gain are performed on a sub-frame' by sub-frame basis. Each frame is divided into 4 sub-frames. A frame may consist of more than 4 sub-frames but then extra bits are required for additional sub-frames. For each sub-frame index and gain, 7 and 5 bits are reserved respectively. Similarly for Fixed Codebook (FCB) index and gain, for each sub-frame 8 and 4 bits are reserved respectively. For frame energy 4 bits/frame are transmitted. This makes 128 bits/frame of 20 ms duration. The coder rate is 128 * 50 = 6.4kb/s.

18.1 Coder Performance

Among many low bit rate coders, CELP and variants of CELP provide the best performance in terms of objective and subjective quality comparisons. The PRELP coding algorithms MOS quality scores are reported as high as 4.0, the quality lies in the range of communications quality as given.

18.2 Multiplexer Design