2011 4th International Conference on Mechatronics (ICOM), 17-19 May 2011, Kuala Lumpur, Malaysia

Performance Analysis of Power Control Schemes in CDMA Communication System

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***Abstract*— In CDMA cellular communication system power control is one of the most efficient methods to manage the resources, where the main capacity-limiting factor is co-channel interference. In this paper several closed loop power control algorithms are analyzed considering loop delay to cope with random changes of the radio channel and interference. Adaptive algorithms are considered that utilize ideas from self-tuning control systems. The inherent loop delay associated with closed loop power control can be included in the design process. Another problem in closed-loop power control is that extensive control signaling consumes radio resources, and thus the control feedback bandwidth must be limited. To enhance the performance of closed-loop power control in limited-feedback-case is investigated. The performances of the adaptive algorithms are investigated through both analysis and computer simulations, and compared with well-known algorithms from the literature. After proper investigation and analysis it is anticipated that significant performance improvements are achievable with the adaptive algorithms.**

Keywords- CDMA, Power Control, Closed Loop, Adaptive Control, Self-tuning, and Loop-delay.

I. INTRODUCTION

Wireless cellular communication systems have experienced a rapid growth during the last two decades. The first-generation (1G) systems were analog and provided wireless speech service. The major improvement in the transition to second-generation (2G) systems was the digital transmission technology, which enabled the use of error correction coding and increased service quality and capacity. The 2G systems have evolved further to provide packet-switched data service in addition to the conventional circuit-switched services like the familiar speech service.

In CDMA systems the users transmit their signals simultaneously in the same frequency band. Each user is given a dedicated spreading code, which is used to identify the users in the receivers by correlating the received signal with a replica of the desired user's code. Power control (PC) aims to control the transmission powers in such a way that the co-channel interference is minimized. In this paper the power control techniques are investigated and analyzed.

II. POWER CONTROL IN CDMA

Transmission power control (TPC) is vital for capacity and performance in cellular communication systems, where high interference is always present due to frequency reuse. The basic intent is to control the transmission powers in such a way that the interference power from each transmitter to other co-channel users is minimized [2].

2.1 *The power control model employed in this paper:* The algorithms chosen in this paper are targeted to improve the transmission power control (TPC) performance in the presence of the practical limitations. The assumption behind the preferred algorithms is that the implementation of TPC is done using the combination of open loop, closed loop, and outer loop PC.

The closed loop PC algorithm employed in UMTS and IS-95 systems is a fixed-step power control (FSPC) algorithm. This type of algorithm has been presented in [9]. It is given by

$$p_i(t+1) = p_i(t) + \delta \, sign\,(\gamma_i^t(t) - \gamma_i(t)) \quad (1)$$

where all the variables are in decibels, $p_i(t)$, $\gamma_i^t(t)$ and $\gamma_i(t)$ are the transmission power, signal to interference ratio (SIR) target, and measured SIR, respectively, of user *i* at time *t*, δ is the fixed step size, and

$$sign(x) = \begin{cases} 1 & \text{if } x \geq 0 \\ -1 & \text{if } x < 0 \end{cases} \quad (2)$$

$$\gamma(t) = p(t-n) + g(t) - I(t) \quad (3)$$

where $g(t)$ and $I(t)$ are the channel attenuation and the total interference power at time *t*, all in decibels. The power control system model is illustrated in Figure 1 for uplink. The *n*-sample delay block models the power control loop delay. Note that the integrator in the mobile unit inherently includes a delay of one sample. Hence the total loop delay is $k = n + 1$. At time *t* the base station measures the uplink SIR.

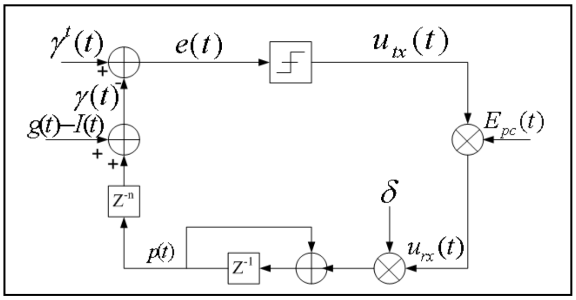

Figure 1: Closed-loop power control with conventional fixed-step controller.

The measurement is compared to the uplink SIR target set by the outer loop control. Based on this comparison, the base

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station sends a command $u_{\text{tx}}(t)$ to the mobile unit to either increase or decrease its power by a fixed step, typically 1 dB. The command is transmitted to the mobile unit uncoded to reduce processing delays, for which reason the command bit error probability can be relatively high, e.g., up to 10 percent. In Figure 1 the bit errors caused by the transmission channel are modeled with multiplication of the transmitted commands with the signal $E_{\text{PC}}(t)$, which has the value 1 with probability $P_{\text{PCE}}(t)$ and -1 with probability 1- $P_{\text{PCE}}(t)$. $P_{\text{PCE}}(t)$ is the probability of bit error in power control command transmission at time t.

2.2 *Distributed Power Control:* A distributed algorithm uses only local measurements to update the transmission powers. Hence it is more suitable for practical implementation than a centralized algorithm. Since in this case a user does not know all the link attenuations, the problem must be iteratively solved. It is necessary to find an iteration that depends only on local measurements, and converges to the optimal solution reasonably fast (faster than the link gains change). Fast convergence can be achieved in two ways: by making the iteration time-step smaller, and by designing iteration with faster convergence property.

2.2.1 *Distributed SIR Balancing Algorithms:* Distributed versions of the SIR balancing problem draw a lot of attention in the 1990's. The starting point was to find iterative algorithms that would be suitable for distributed operation. The first proposal was the Distributed Balancing (DB) algorithm proposed in [2]. It is described in the following.

2.2.1.1 *The Distributed Balancing (DB) Algorithm:* For a feasible system, the DB algorithm converges to the optimal power vector p^* with probability one [2]. However, it suffers from poor convergence speed. Moreover, an improper selection of parameter β may result in ever-increasing (or decreasing) powers.

$$p_i(t+1) = \beta p_i(t)\left(1+\frac{1}{\gamma_i(t)}\right), \quad \beta > 0, t = 0,1,........, \tag{4}$$

An improvement to the DB algorithm in terms of convergence speed was proposed in [3]. They proposed a modified version of the DB algorithm and called it the Distributed Power Control (DPC) algorithm. However, since the term DPC is used for another algorithm (described later), the algorithm of [3] is called the Modified DB (M-DB) Algorithm. It is described as follows.

2.2.1.2 *The Modified DB (M-DB) Algorithm:* The convergence of the M-DB algorithm to the optimal power vector and SIR balance has been proven in the noiseless case [3].

$$p_i(t+1) = \beta \frac{p_t(t)}{\gamma_i(t)}, \quad \beta > 0, t = 0,1,, \tag{5}$$

Also, the convergence speed was shown to be faster than with the DB algorithm. However, the problem of cleverly choosing β still remained. The problem with the normalization procedure was avoided in the algorithm proposed in [4], the Fully Distributed Power Control (FDPC) algorithm. It is given in the following.

2.2.2 *The Distributed Power Control (DPC) Algorithm:*

$$p_i(t+1) = p_i(t)\frac{\gamma^t}{\gamma_i(t)}, \quad t = 0,1,.........., \tag{6}$$

From control theory viewpoint, the DPC algorithm is an integrating P-controller. The convergence of the DPC algorithm in the case where the power updates occur asynchronously was proven in [6].

2.2.2.1 *The Fully Distributed Power Control (FDPC) Algorithm:* Clearly, $\beta \longrightarrow \infty$ corresponds to constant power case (no power control). For very small values of β the FDPC algorithm approaches the M-DB algorithm. The FDPC algorithm can achieve SIR balance with probability one in the noiseless case, if $\beta \le \gamma^*$, where γ^* is the maximum achievable SIR in the system.

$$p_i(t+1) = p_i(t)\frac{\min(\gamma_i(t),\beta)}{\gamma_i(t)}, \quad t = 0,1,.., \tag{7}$$

A drawback of the algorithm is that if $\beta < \bar{\gamma}$ where $\bar{\gamma}$ is the system protection ratio, the powers are ever-decreasing, which is a problem in the noisy case. The algorithm proposed in [5] finally solved the problem of choosing β of the M-DB algorithm in the noisy case. They identified β in the noisy case to be the target SIR which the algorithm is trying to achieve. This algorithm is called the Distributed Power Control (DPC) algorithm in this paper. It is described as follows.

2.2.2.2 *The Distributed Constrained Power Control (DCPC) Algorithm:* With DCPC it can happen that some transmitters are transmitting with the maximum power, thus producing maximum interference to other users, but still do not achieve their SIR target.

$$p_i(t+1) = \min\left(p_i^{\max}, p_i(t)\frac{\gamma_i^t}{\gamma_i(t)}\right), \quad t = 0,1,.., \tag{8}$$

where $p_i^{\max}$ is the maximum allowed transmission power of transmitter i. In [7] a power control algorithm is chosen with faster convergence properties than the DPC algorithm. The algorithm differs from the first-order algorithms described above in the sense that it requires the current and the previous power levels to calculate the next one. The scheme is called the Constrained Second-Order Power Control (CSOPC) algorithm, which is described as follows.

$$p_i(t+1) = \min\left(p_i^{\max}, \max\left(0, p_i(t)\omega(t)\frac{\gamma_i^t}{\gamma_i(t)} + (1-\omega(t))p_i(t-1)\right)\right), \quad t = 0,1,.., \tag{9}$$

III. ADAPTIVE CLOSED-LOOP POWER CONTROL APPROACH

Enhanced algorithms are selected for closed-loop power control in CDMA systems. From the above discussion, the closed-loop PC aims to keep the received SIR in a target set by an outer-loop controller, by sending feedback signals to the transmitter. The simulation result of the difference between the power vector and the optimal power vector p* in multiuser snapshot is shown in Figure 2.

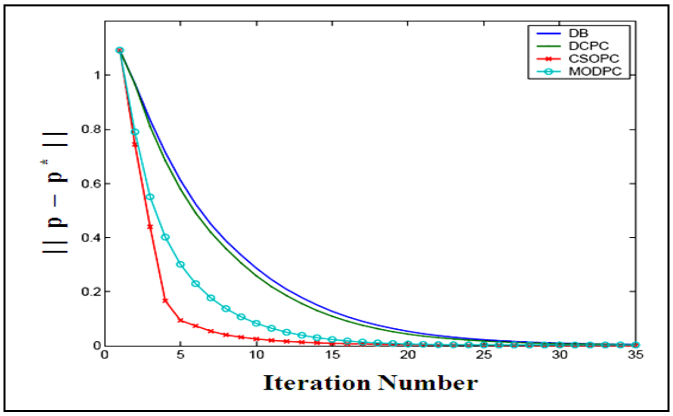

Figure 2: Convergence of the norm of the difference between the power vector and the optimal power vector p* in multiuser snapshot simulation.

To minimize the power control signaling, practical CDMA systems typically employ a simple fixed-step power control scheme that does not take advantage of the power control command and measurement histories. However, due to the time variation of the radio channel and interference seen by a receiver, and the loop delay, the command may already be outdated by the time it can be applied in the transmitter. Even if the feedback information signals are not quantized, the loop delay can cause serious problems to power control algorithms if it is not properly taken into account. The preferred scheme is to model the power control process with a linear process model, and to design an adaptive self-tuning controller to minimize the variance of the process output, which is the SIR at the receiver or its distance to SIR target. Decision feedback versions of the algorithms are also provided. Those algorithms are able to mitigate the undesirable effects of the loop delay without any increase in power control signaling.

3.1 Adaptive controller approach: These algorithms have been derived from a rather theoretical viewpoint, where it is assumed that the iteration converges fast enough so that the channel attenuations can be assumed to be constant during this time. The delays involved in the SIR measurement process, transmission and the processing of the algorithm itself can be long enough so that the channel as well as interference conditions might be considerably changed during the delay.

Loop delay: A typical loop delay situation encountered in WCDMA is illustrated in Figure 3. Since the power control signaling is standardized, the loop delays are in principle known exactly. The slot at time *t - 1* is transmitted using power *p(t - 1)*. The receiver measures the SIR °(t) over a number of pilot and/or data symbols and derives a TPC command. If the SIR measurement window, processing delays, and propagation delays are short enough, as in the example in Figure 3, the loop delay can be as short as one PC period. Otherwise, the TPC command cannot be applied at the transmitter within one-slot-time, resulting in longer loop delays.

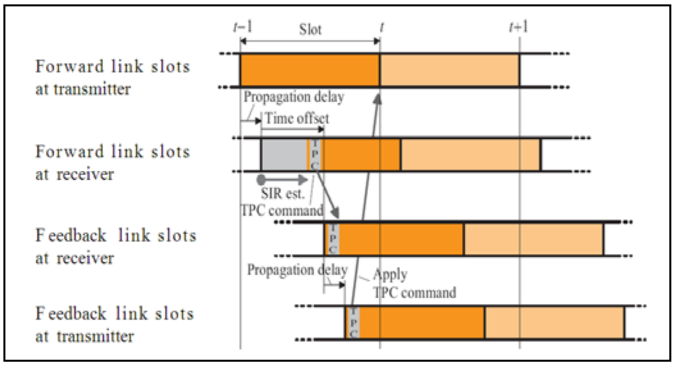

Figure 3: power control timing in WCDMA.

3.2.1 Problems caused by the loop delay: It has been shown that if not properly controlled, the loop delay can cause serious problems to the power control algorithms [9–11]. It has also been shown [12] that the FSPC algorithm converges to a bounded region provided that the power control problem is feasible within this margin.

$$|\gamma_i^t - \gamma_i(t)| \le 2\delta\kappa \tag{10}$$

Here δ is the step size of the algorithm and *k* is the total loop delay. Thus, longer loop delays lead to larger convergence bounds. It has been shown that with the FSPC algorithm time delay compensation the PC miss-adjustment converge to [10]:

$$|\gamma_i^t - \gamma_i(t)| \le 2\delta(\kappa + 1) \tag{11}$$

which should be compared to 6. However, the fact that the bound is tighter does not imply that the variance of the PC misadjustment is smaller.

3.2 Adaptive self-tuning control: Adaptive control is one type of a nonlinear control. The adaptive control theory was originated in early 1950s, when sophisticated controllers were needed for aircraft autopilot systems. The problem was how to control a system having several operating points, which could also be time varying. Adaptive control combines closed-loop identification with control, which makes the problem nonlinear and extremely complex.

3.2.1 Characteristics of adaptive control systems: In adaptive control systems the controller parameters are adjusted all the time, so that they follow the changes of the controlled process. Because the convergence and stability properties of such systems are very difficult to analyze, it is assumed that the process has constant but unknown parameters. When the process is known, the design procedure specifies a set of desired controller parameters.

Figure 4 represents the structure of self tuning control. There is a conceptual difference between adaptive control and self-tuning control. In self-tuning control the controller parameters are updated until the optimal parameter values are reached, after which the parameter updating mechanism can be turned off.

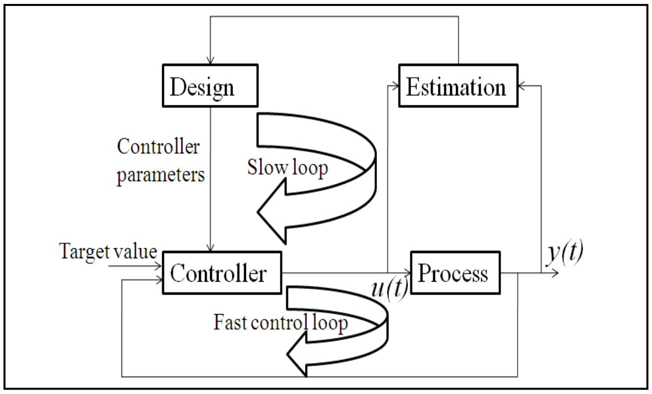

Figure 4: Self-tuning control structure.

3.2.2 Considered adaptive controllers: The disturbances in the power control process are stochastic in nature. Therefore it is natural to use stochastic measures to investigate the performances of various closed-loop power control methods. It is well established in the literature that for reasonable number of users in the system the SIR statistics at the receiver and the power control misadjustment (the difference between SIR target and SIR) are log-normally distributed. A natural optimization criterion is thus to minimize the variance of the power control misadjustment in decibels. Figure 5 shows two hypothetical PDFs of received SIR. Consider that the PDFs result from using power control algorithms (PCAs) 1 and 2 as shown in Figure 5. The SIR threshold is the lowest SIR required for acceptable reception of the signal at the receiver. The outer loop power control sets the SIR targets in such a way that the service quality is achieved up to a specified criterion, e.g., 1% frame error rate.

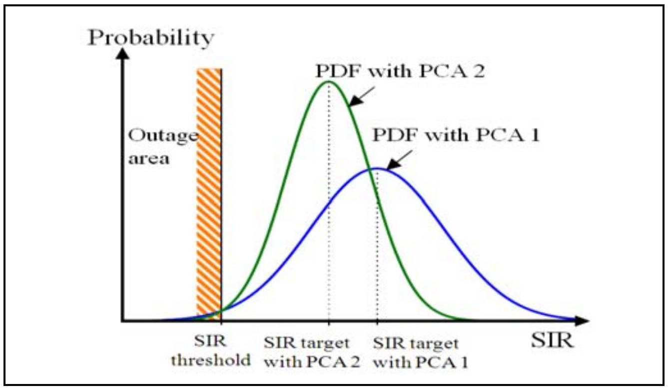

Figure 5: Illustration of the goals in the design of the proposed power control algorithms.

IV. CONCLUSION

In this paper closed-loop power control algorithms have been reviewed and a competent algorithm has been chosen for CDMA cellular communication systems. Moreover, the preferred adaptive step size methods are independent from the actual power control algorithm, and can also be combined with the other adaptive algorithms. The chosen adaptive algorithms are based on self-tuning controllers considered for a linear model of the closed-loop power control process. As presented in the paper, the loop delay inherent in the power control process can seriously degrade the performance of the power control algorithms proposed in the literature that do not take the loop delay into account. The main advantage of the preferred algorithms is that the loop delay can be included in the design process, and the histories of the previous SIR measurements and power control commands can be utilized to minimize the effect of the loop delay.

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