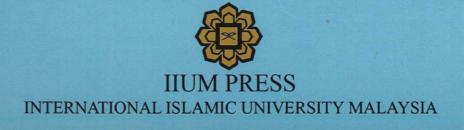
INTERFACING ELECTRONIC FOR MEASUREMENT, SIGNAL PROCESSING AND WIRELESS COMMUNICATION



Edited by

Sheroz Khan, International Islamic University Malaysia AHM Zahirul Alam, International Islamic University Malaysia Anis Nurashikin Nordin, International Islamic University Malaysia



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Chapter 10

CMOS OPERATIONAL AMPLIFIER DESIGN

Ma Li Ya, Sheroz Khan, Anis Nurashikin

In this chapter, we will describe CMOS operational amplifier design which is an important component in the data converter. The fundamental design principle, design procedures, as well as the properties of a traditional operational amplifier (or two-stage op amp) are elaborated in this chapter. (A CMOS 0.13µm two-stage op amp using low power supplies, is specified, designed and simulated with verifying at the same time.) The properties of the op amp can directly control the properties of the integrator and affect the characteristics of the converter. The op amp which serves in the integrator requires a large input-output swing, large DC gain and a high slew rate. The followings are the steps to design an op amp with the user-defined conditions.

- i) Specifying the op amp requirements.
- ii) Choosing the op amp topology to meet the specifications.
- iii) Calculating the devices' size and bias to meet the requirements.
- iv) Circuit simulations to verify that the op amp designed met with the user-defined specifications.

10.1. DESIGN SPECIFICATIONS

The design specifications normally contain the CMOS technology, power supplies, input and output voltages' range, frequency band, open loop gain, power consumption, and so on. Here we give an example to design the simplest op amp topology which is based on $0.13\mu m$ CMOS technology and ± 1.2 V power supplies working in low frequency range, with small power consumption, together with the following design specifications as given in Table 10.1.

Table 10.1: Two-stage op amp design specifications

Specifications	Design Value
Power Supply (V _{dd} and V _{ss})	±1.2V
Signal Bandwidth	10kHz
Phase Margin	75°
Open Loop Gain	≥100
Input Signal Range	-0.7V~0.7V