Proceedings of the 1st International Conference on Recent Innovations in Electrical, Electronics and Communication Systems (RIEECS 2017)

Trends in Renewable Energy
OPEN ACCESS ISSN:2376-2144
futureenergysp.com/index.php/tre

Analysis and Design of Solar Power System Interface Utility Using ZVS Converter

R. G. Deshbhratar* and M. M. Renge

Electrical Department, Shri Ramdeobaba College of Engineering and Management, Nagpur, Maharashtra, India

Received January 16, 2018; Accepted March 15, 2018; Published May 9, 2018

The solar power generation system with minimal losses, high simplicity and easy control is attempted in this work, by developing a grid-tied zero-voltage switching (ZVS) inverter with a less number of power conversion stages and the least count of passive components, for single-phase applications that are suitable for conversion from low-voltage DC (40-60 V) to line voltage AC (230 VAC; RMS) at average power levels of 175 W and below. The ZVS full-bridge inverter fed from a PV panel is working on higher frequency with an asymmetric auxiliary circuit, which guarantees ZVS at the switching instants of the metal-oxide-semiconductor field-effect transistors (MOSFETs) by supplying the reactive current to these full-bridge semiconductor switches and reducing the switching losses. Checking of the constructional workability and analytical feasibility of the proposed topology with the highest efficiency and the simplest control was the target of this work, which was set on the basis of the results obtained in the MATLAB Simulink environment. The control strategies were planned for the optimum value of the reactive current injected by the auxiliary circuit to guarantee ZVS and use of phase shifted pulsewidth modulation (PWM) with varying frequencies for the full-bridge inverter and half-bridge cyclo-converter. The hybrid maximum power point tracking (MPPT) was part of this plan used to set the power at its maximum value against the environmental changes.

Keywords: Full-bridge inverter; Asymmetrical auxiliary circuit; Half-wave cycloconverter; Hybrid MPPT; Phase-shift control; Frequency modulation; Zero-voltage switching (ZVS)

I. Introduction

A. Motivation & Background

The solar energy generation is becoming the most promising day by day, as the conventional resources of energy are depleting swiftly and the rooftop grid tied photovoltaic (PV) panel with the inverter are developing with more and more efficiencies. It is necessary to reduce the complication in the design and control of this PV inverter to make it an economical, user friendly and strong alternative to the fossil fuel electricity. The main duty of the inverter is to convert the photovoltaic direct current (DC) power into grid-synchronized alternating current (AC) output. It may be central inverters, mini central inverters, string inverters, multi-string inverters, and microinverters [1, 2], according to the type of inverter topology. Among these inverter topologies, the microinverter is widely used, as it is suitable for integrating a single solar panel (40–400 W) to the grid. The inverter topology has a great role in deciding the cost

*Corresponding author: deshbhratarrg@rknec.edu

Tr Ren Energy, 2018, Vol.4, No.3, 83-101. doi: 10.17737/tre.2018.4.3.0052

of the solar generation unit, which is now a day a main task behind many studies going on in this field [3-8]. The PV microinverter is very much suitable in this area in order to increase the efficiency by reducing the losses and thus reducing the cost.

The inverter topology receives the maximum DC power from the PV array (by imposing an optimal operating condition onto the solar panel through maximum power point tracking (MPPT)) and supplies this power into the grid at the AC line voltage. Operating the inverter at zero-voltage switching (ZVS) decreases the switching losses and provides a noise-free environment for the control circuit. ZVS is usually achieved by providing an inductive current flowing out of the full-bridge legs during the switch turn-on and by placing a snubber capacitor across each switch during the switch turn-off. An easy way to produce this inductive current is inserting an inductor in series or in parallel with the power transformer [1-8]. In this application, the efficiency and the compactness are the main driving design considerations. There is an extensive body of work on DC to AC power converters, specifically for the grid tied PV applications. A thorough overview and a topology classification are provided in some literature [12-14]. Topologies for different power levels and numbers of phases at the output are also presented in the literature [16-18]. In this paper, the topology of an inverter based on the architecture of Fig. 1, comprising a high frequency inverter, a high-frequency transformer, and a cycloconverter is presented. This general architecture is rarely investigated although it has been long known [2]. The improvement in this architecture that reduces device losses compared to other architectures along with flexible control, enabling very high efficiencies are attempted. All devices operate with resistive on-state drops (no diode drops) under ZVS to achieve high efficiency, and encompassing frequency control and inverter and cycloconverter phase shift control [2].

B. Objective

The main objective of this paper is to analyze and validate the topology and working conditions of the full-wave HF inverter with control strategies of phase shifted pulsewidth modulation (PWM) signal generation at automatically controlled frequencies. The power stage design and the simulation results of the proposed topology in MATLAB Simulink environment are discussed for the confirmation of an inverter that is suitable for utility interfacing, operating from low input voltages (40-60 V DC) to high output voltages (230 Vrms AC) at average power levels of 175 W. Operating at unity power factor, the power into the grid (averaged over a switching cycle) is given by Equation (1). The quantity *Pavg* represents the power injected into the grid, $\boldsymbol{\omega_l}$ is the line angular frequency and Vp is the peak value of line voltage. This quantity can change (*e.g.,* based on solar panel insolation and shading) over a wide range of over 10 to 1.

$$Po = \frac{V_p^2 sin^2\,\omega_l t}{R_{eqv}} = 2P_{avg} sin^2 \omega_l t \qquad (1)$$

II. Design

A. Topology

The proposed inverter topology in Fig. 1 shows a parallelly placed buffer capacitor bank (C_{bf}) with the solar panel providing the necessary twice-line-frequency energy buffering. This buffer may comprise the electrolytic capacitor, in parallel with high-frequency decoupling capacitance to carry the resonant current. The size of this

capacitance is given by (2) where, depending on the input voltage 'V_{in}' and ripple voltage 'v_r', the voltage ripple ratio on the input 'r' is reasonably taken as 0.95. Hence, the required capacitance is approximately 7.38 mF (as dictated by the lowest nominal input voltage).

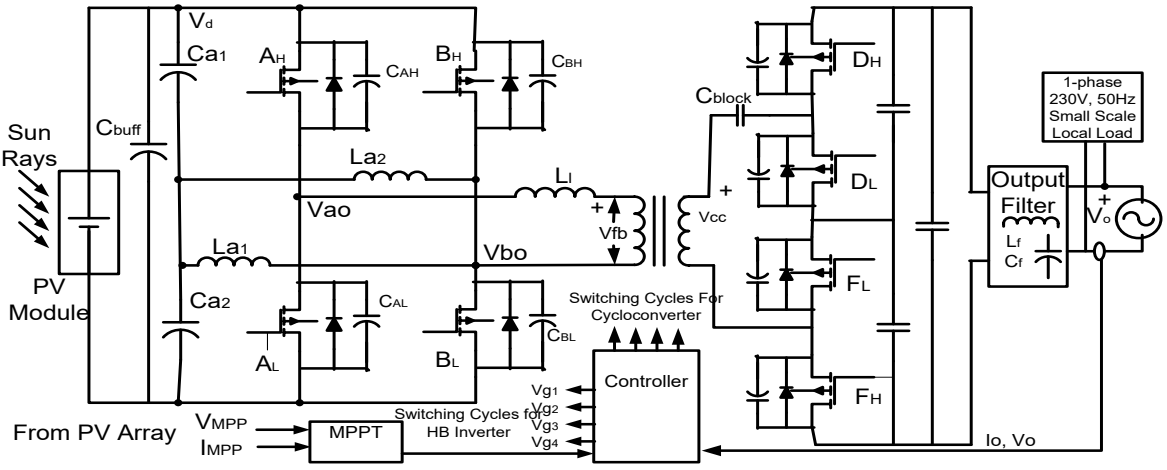

Fig.1. The Proposed Topology

$$r = \frac{V_{in} - v_r}{V_{in} + v_r} \tag{2a}$$

$$C_{bf} \approx \frac{P_{avg}}{2\omega_l V_{in}^2 (1-r)} \tag{2b}$$

A full-bridge inverter, using the reactive current supplied by the auxiliary circuit inductors that are just sufficient to achieve the ZVS at different loadings, is operated under variable-frequency phase-shift control, with the duty ratio controlled by MPPT. The reactive current is controlled by a control policy that regulates the switching frequency according to the varying load. It requires the switching frequency to decrease at low load and vice versa. The metal-oxide-semiconductor field-effect transistors (MOSFETs) A_H and A_L form the 'leading' half-bridge leg and $B_H$and B_L form the 'lagging' leg of the H-bridge inverter. In each half-bridge structure, the subscripts 'H' and 'L' refer to the high and low side device, respectively. These legs are lagging or leading with respect to the phase shift angle $'\theta'$. The parasitic capacitance and body diode are obtained across drain and source of each MOSFET [5]. However, to improve the ZVS characteristic of the H-inverter, some capacitance may be added across the switch (in the lagging leg more advantageous). The HF transformer (1:N) provides the galvanic isolation and voltage transformation. The capacitor C_{block} connected to the secondary side of this transformer at high-frequency quasi-sinusoidal voltage and current of V_{fb} and Ix (full-bridge inverter's output voltage and current), respectively. The high-frequency AC current is converted to the line frequency using a half-wave ZVS cycloconverter, yielding unity-power factor output current at line frequency. Also, the capacitor C_{block} placed on the secondary side of the HF transformer, restrict the entry of DC voltage if present in order to avoid the otherwise possible undue saturation of the transformer core. Its value chosen to be adequately large, so that it will not significantly affect the total effective capacitance of the main circuit. Its presence is intended in this design in such a manner that in the absence of any auxiliary circuit components (which are working as the

resonant components) on the secondary, this capacitance is absorbed into the overall capacitance across the cycloconverter. This cycloconverter improved greatly the layout for high frequency currents, providing reduced total device drop than conventional bidirectional-blocking-switch topologies. The operation of the cycloconverter can be outlined as follows. When the line (grid) voltage V_g is positive (with reference to the given polarity), the two switches F_H and F_L at the bottom of the cycloconverter (Fig. 1) remain on, while the two switches D_H and D_L at the top function as a half-bridge and modulate the average current (over a switching cycle) delivered into the AC line. Likewise, when V_g is negative, the two switches at the top remain on, whereas the two switches at the bottom modulate the average current for proper power delivery. A bypass capacitor is paralleled effectively to every pair of 'on' switches of cycloconverter half-bridge in a particular half cycle, resulting in reduced conduction losses, compared to a single switch of the same configuration. Hence, for this particular time, cycloconverter on state conduction loss results from 1.5 device resistances, as compared to two on state resistances of conventional 'back-to-back switch' half-wave cycloconverter [2, 10]. The cycloconverter switching and gating losses are considerably reduced, since one of the two half-bridges modulates at any given time in this topology. This means that the functional connectivity & the overall condensed nature of the layout of this cycloconverter topology are proven to be greatly advantageous over conventional 'back-to-back switch' cycloconverter topologies in the real life. These topological aspects are implemented in the lay-out of Fig. 1, which aims to achieve high efficiency as well as fewer component counts and yielding a small size, although achieving the large voltage transformation and isolation. As the full bridge inverter and half-wave cycloconverter topologies are able to reduce the required transformer turns ratio, they are compared to using a half-bridge inverter plus a full-wave cycloconverter, in order to achieve the improved efficiency. Similarly, the diode drops are eliminated from main operation of the converter, and by operating all of the devices under zero-voltage switching, low loss operation is achieved by scaling device areas up beyond that which is optimum for hard-switched topologies. For the sake of component count reduction and the integrated design, we are able to deploy the leakage and magnetizing inductances of transformer as part of the auxiliary circuit inductor.

B. Maximum Power Point Tracking

Due to the changes in direction of the sun, solar insolation level and ambient temperature, the output power of the PV module changes drastically. The PV characteristics of the PV module also show a single maximum power point for a particular operating condition. It is desired that the PV module operates close to this point, *i.e.,* the maximum output of the PV module is obtained near to the maximum power point (MPP). The process of tracking of this point in the operation of PV module is called as maximum power point tracking (MPPT). Maximization of PV power improves the utilization of the solar PV module [11]. According to the maximum power point theorem, the output power of any circuit can be maximized by adjusting source impedance equal to the load impedance, so the MPPT algorithm is equivalent to the problem of impedance matching. Many MPPT algorithms are in use now a day. The most common algorithms are the perturb and observe (P&O) and the incremental conductance (IC) method [9]. In the present work, the hybrid MPPT combining 'Perturb and Observe' and 'Incremental Conductance' methods is used. The perturb and observe is the simplest method. In this paper, we use only one sensor that is either voltage sensor or current

sensor to sense the PV array voltage or current, so the cost of implementation is less. The two main problems of the P&O are the oscillations around the MPP in steady state conditions, and poor tracking (possibly in the wrong direction, away from MPP) under rapidly-changing irradiations. The IC method has an advantage over the P&O method, because it can determine the MPP without oscillating around this value.

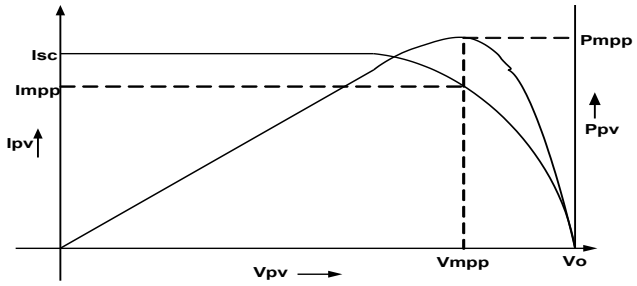

Fig. 2. The I_{pv} vrs V_{pv} and P_{pv} vrs V_{pv} Characteristic of Solar Panel Showing Maximum Power Point Voltage (V_{mpp}), Current (i_{mpp})

However, the IC method can produce unintentional oscillations and perform tracking erratically in wrong direction under rapidly changing atmospheric conditions and low irradiance. Due to higher complexity, the sampling frequency is reduced as compared to the P&O method. Perturb & Observe method and Incremental Conductance method have various advantages and disadvantages. So, our aim and innovation here were to club advantages of both the method and make the controller more flexible and sustainable to various adverse conditions.

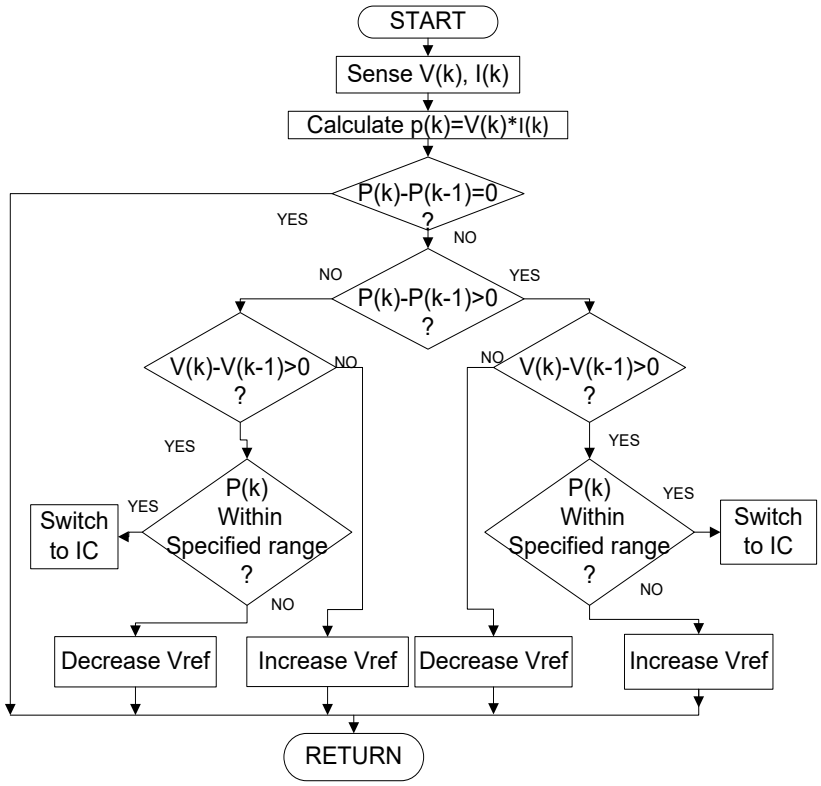

Fig.3. Hybrid Technique *i.e.,* combination of both PO and IC

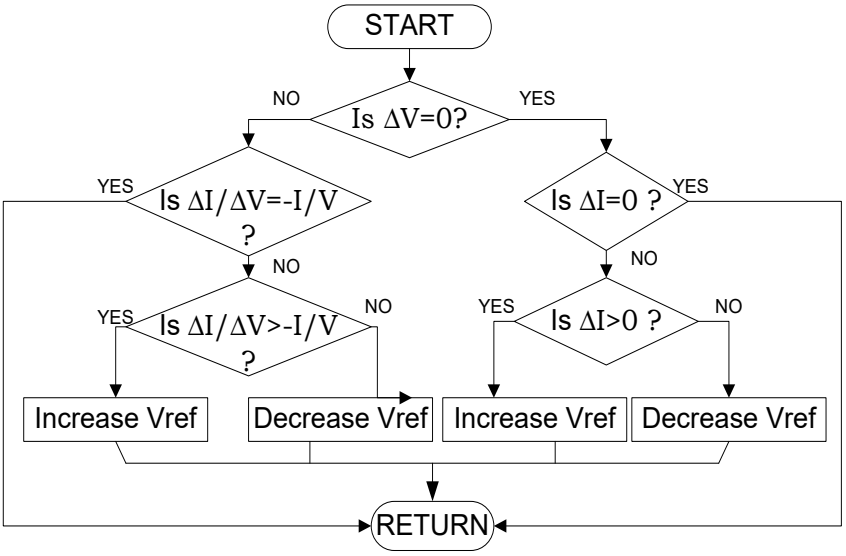

Fig. 4. Flow-chart for Incremental Conductance

The MPPT is tracked using criteria dP/dV (at Vmax, Imax) = 0. A threshold error is normally allowed to make a tradeoff between the convergence speed and the allowable oscillations at the peak point limiting the sensitivity of the tracker. The simulation for MPP tracking is done for a step size of 0.5 V and a threshold acceptable error of 0.002 for an input irradiance of a trapezoidal pattern. The specified range of Pk is 0.95Pmax used for the MPPT change from PO to IC.

Fig. 3 shows the flow chart of this hybrid MPPT, where the main body of flow chart is following the PO method. If the suggested criteria are fulfilled, it switches to the IC method (Fig. 4).

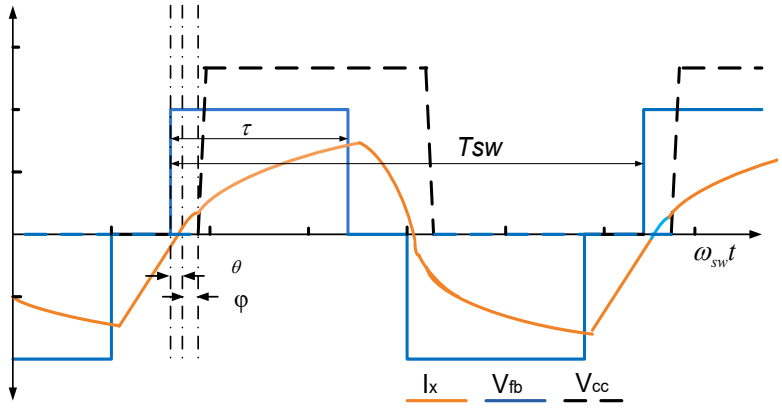

Fig. 5. Ideal waveforms in relationship with ideal angles

C. Idealized waveforms and ZVS

Fig. 5 shows the standard waveforms of interest for this topology, with their nomenclature declared in Fig. 1. For simplicity, the waveforms are dimensionally standardized for the sake of explaining their clear positional relations. So, no clear values are defined on y-axis and attempted to explain relative timing on x-axis. The figure demonstrates the waveforms of v_{fb}, Ix&V_{CC} on the time scale of the switching period (τ_{SW}= 1/fsw = $2\pi/\omega_{sw}$). The instantaneous output voltage can be well approximated as constant, since the switching frequency is much greater than the line frequency during each

switching period. As the practical consequence of the control strategy, this is helpful to prove the proper transfer of power to the grid at any instant. The cycloconverter input voltage 'V_{cc}' is a square wave with the minimum value of 0 and the maximum value of *Vout* (max of instantaneous v_{out}). The angular difference φ is the angle (normalized to the switching period) by which the zero-crossing of current *Ix* leads to the rise of 'V_{cc}'. The 'V_{fb}' is a three-level stepped voltage waveform of the full-bridge inverter (as explained in Fig. 6). The three voltages of this waveform with respect to these three levels are $+V_{fb}$, 0 and $-V_{fb}$. This waveform leads to the zero crossing of the current Ix by angle θ. It should be very clear that the switching frequency of the converters is well above the resonant frequency of the equivalent circuit, and the equivalent impedance of this circuit seen by the full-bridge is inductive with positive angle θ. These optimal values are decided on the basis of iterative simulation results of peak current and input and output voltages, we call them $\theta main$ and $\varphi main$ as the angles equivalent to the instant of time necessary to fully discharge the drain to source capacitance of the full-bridge inverter and the cycloconverter switches, respectively. Operating the inverter at $\theta \geq \theta_{main}$ and $\varphi \geq \varphi_{main}$ was the tentative adjustment for the better results. Operation of the inverter at $\theta \geq \theta_{main}$ and $\varphi \geq \varphi_{main}$ scrupulously implements ZVS on all eight MOSFETs, practically eliminating switching losses to the greater extent [9].

D. Power Transfer Strategy

The equation (3) shows the average power over a switching cycle. Here I_{x1} represents the fundamental (switching) frequency component of the inverter current for the expansion of the integral with Fourier series coefficient notation. The fundamental frequency component of current and the variable angle φ are related with the power transfer with the final approximation. The switching harmonics are neglected here. Since they account for less than 10% of total power transfer for the quality factors that are used here, ignoring harmonics is valid for qualitative purpose [2, 19].

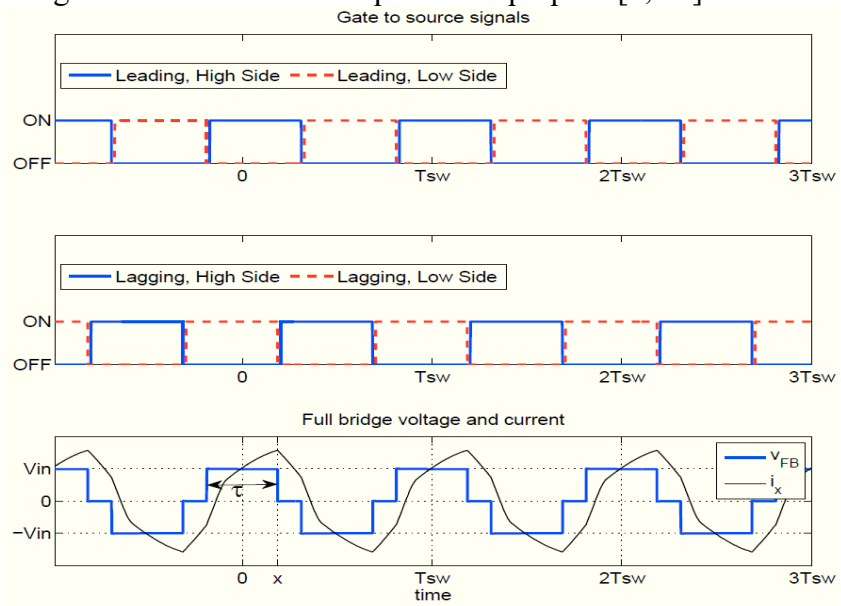

Fig. 6. Full-bridge timing and output voltage V_{fb}. The top two sub figures show the switching signals of the leading and lagging legs. Drain to source voltages (which can be deduced from the gating signals) combine to produce the waveform shown on the bottom figure. Here, τ is the overall 'width' of the positive and negative voltage pulses of V_{fb}.

$$Pout = \frac{1}{2\pi}\int_0^{2\pi} i_x(\tau)d\tau \quad (3a)$$

$$= \sum_n \frac{1}{n}\|Vcc, nIx, n\|Cos\pi(\angle Vcc, n - \angle Ix, n) \quad (3b)$$

Finally,

$$Pout \approx \frac{1}{\pi} i_{x,1} VoutCos\varphi \quad (3c)$$

Following are the three ways used in combination, to implement the control strategies here to control the delivery of the quantity of power to the grid.

1. Switching Frequency Control,

2. *Inverter Phase Shift Control,*

3. Cycloconverter phase Shift Control.

In the present case, the H-bridge inverter connects two legs (leading leg and lagging leg) with the mid-points 'a' and 'b' bearing voltages 'V_{ao}' and 'V_{bo}', respectively, resulting in the inverter output voltage between a and b of V_{fb} (V_{ao} - V_{bo}). The inverter (Full-Bridge) phase shift takes the fundamental component of this V_{fb} as the phase reference for all waveforms of Fig. 5. The Fourier series coefficients of V_{fb} are given by Eq. (4), where $\delta = 2\tau/T$ (shown in Fig. 6). The phase of each component is therefore either 0 or π radians. Each leg of the full-bridge operates at 50% duty ratio. Changing phase shift of the full-bridge can be defined as changing the amount of time between the rise of the voltages of high sides of leading and lagging legs. This directly corresponds to changing τ, the overall 'width' of the positive and negative voltage pulses of V_{fb}, while also affecting θ (however, that relationship also depends on the frequency). According to Eq. (4), changing phase shift changes the magnitude of each harmonic component of the voltage, which in turn changes the current and the overall power transfer.

$$V_{fbn} = 0 \text{ for n} = 2,4,6....$$
$$= \frac{4\text{Vin}}{\text{n}\pi}\sin\frac{\text{n}\delta\pi}{2} \text{for n} = 1,3,5... \quad (4)$$

Using the cycloconverter phase shift changing technique, with a given current amplitude of the fundamental component and output voltage (Eq. 3c), it's evident that, the effect of increasing the cycloconverter phase shift φ is decreasing the instantaneous output power. For a given output power, operating at larger phase angle φ will result in a larger peak (and *rms*) resonant current.

And using the switching frequency control, the magnitude of the reactive current supplied by the auxiliary circuit inductors is controlled. This current supplied to the FB inverter switches should not be of high value, as it may lead to the high voltage spikes on the semiconductor switches due to the delay in the body diode turn-on. The work of the auxiliary circuit is totally independent, does not depend on the system operating conditions and is able to guarantee ZVS from no load to full load. Since the auxiliary circuit should provide enough reactive power to guarantee ZVS at all operating conditions, the peak value of the current flowing through the auxiliary inductor is regulated, which controls the MOSFET conduction losses essentially [5, 6].

Thus, these three techniques are used here simultaneously to regulate the power delivery to the grid as given by equation (3) and make it more efficient as per the requirement. And for achieving the high efficiency control, it is necessary to minimize

the total loss by satisfying the appropriate ZVS constraints. The maximum amount of power that the inverter can deliver (ignoring ZVS requirements) occurs, when it is operated at $\delta = 1$ and $\varphi = 0$. Decreasing the power delivery can be done by increasing *fsw* or φ, or by decreasing δ [1]. An operating point determines the minimum required inverter current and the corresponding minimum cycloconverter phase shift $\varphi = \varphi_{main}$. Any extra cycloconverter phase shift will result in extra loss as a consequence of higher current [12]. The nominal control strategy that minimizes losses appears to operate at the lowest possible cycloconverter phase shift φ, as this results in the lowest *rms* current, while also switching at the lowest allowed frequency and consequently the narrowest pulse width τ on the full-bridge. Essentially the combination of frequency and phase shift modulation is more favorable in terms of loss than cycloconverter modulation, with the preference of lower frequency.

E: Auxiliary Circuit Components

The auxiliary inductor works as a constant reactive current source since the circuit current remains constant during the deadtime. This current discharges the capacitor across A_H and charges the capacitor across A_L. The value of this constant current source is derived as:

$$I_{AUX}=\frac{V_{in}}{8fsw\,.L_{aux}} \tag{5}$$

Therefore, the MOSFET capacitor voltage due to this constant current source is derived as,

$$V_{AH,aux}(t) = V_{in} - \frac{V_{in}}{8fsw\,.L_{aux}}\,(t - t_{\alpha}) \tag{6}$$

Here,V_{in} is the solar panel voltage, L_{aux} is the supplementary inductance, t_{α} is the starting instant of dead-timet_d between A_H&A_L and *fsw* is the switching frequency. The inductor value is designed to provide enough current to make the voltage *Vz* (the value of Va at the end of the dead-time) zero. Hence, the inductor is designed as,

$$I_{AUX1}=\frac{V_{in}\,.t_d}{16fsw\,.C_{AH}(V_{in}+V_Z)} \tag{7}$$

The lagging leg supplementary inductor, ' *L*aux2 ' could be designed by calculating the energy required to discharge the snubber capacitor C_{AH}. It is clear from the waveforms of Fig. 7(b) that, the primary current of the lagging leg is always a positive value, at the most it can be zero. The energy of discharging and charging the snubber capacitors is given by,

$$W\text{Cs} = C_{BH}\ \cdot V_{in}^2 \tag{8}$$

The energy stored in the leakage and supplementary inductances and the peak current of the supplementary inductor are given by,

$$WL = \frac{1}{2}\ \cdot L_{leak}\ \cdot I_p^2+\frac{1}{2}\ \cdot L_{aux2}\ \cdot I_{aux2}^2 \tag{9}$$

Here I_p is the peak current of transformer primary. The peak current passing through the supplementary inductor is,

$$I_{aux}=\frac{V_{in}}{8fsw\,.L_{aux}} \tag{10}$$

In the worst case, *Ip* is equal to zero. Therefore, the lagging leg auxiliary inductance is derived as,

$$L_{aux2} = \frac{1}{128.C_{BH}.f_{sw}^2} \quad (10a)$$

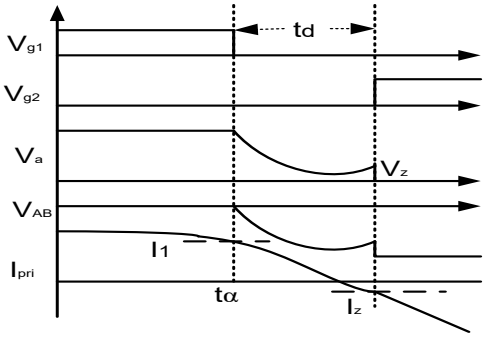

Fig. 7 (a). Key Waveforms of Leading Leg

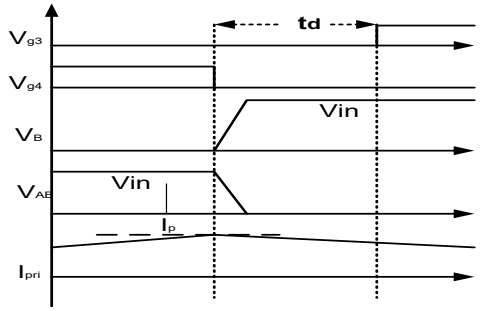

Fig. 7(b). Key Waveforms of Lagging Leg

Also, depending on the load conditions, the inductive current of the auxiliary inductor should be controlled, because excessive inductive current may overcharge the snubber capacitors due to the delayed body diode turn-on and result in an objectionable voltage spike on the MOSFETs. Therefore, a proper control approach is suggested to adaptively control the peak value of the auxiliary circuit current based on the load variations.

Table 1. Circuit Components & Their Values

Component	It's Value	Component	It's Value
Input Voltage	40-50 V	Cbf	500µF
Output Voltage	230 Vrms	Cblock	1000 µF
Output Power	175 W	Lfilter	0.1 µFH
auxiliary Inductor -1	200 µH	Cfilter	4.0 µF
auxiliary Inductor -2	100 µH	Switching Frequency, *fsw*	55-350 kHz
Transformer Turn ratio	1 : 7.66		

The proposed closed-loop control system is shown in Fig. 8. The proposed control system consists of an internal current loop and an external voltage loop (Table 1). The frequency control loop regulates the frequency for the modulation depending upon the variations in loads as shown in Fig. 9. The peak value of the reactive current through the auxiliary circuit is controlled by the switching frequency, which is able to minimize the converter losses. At light loads, the switching frequency is lower to provide enough inductive current to ensure ZVS, and at higher loads, the switching frequency is higher to avoid too much reactive current and reduce the semiconductor conduction losses.

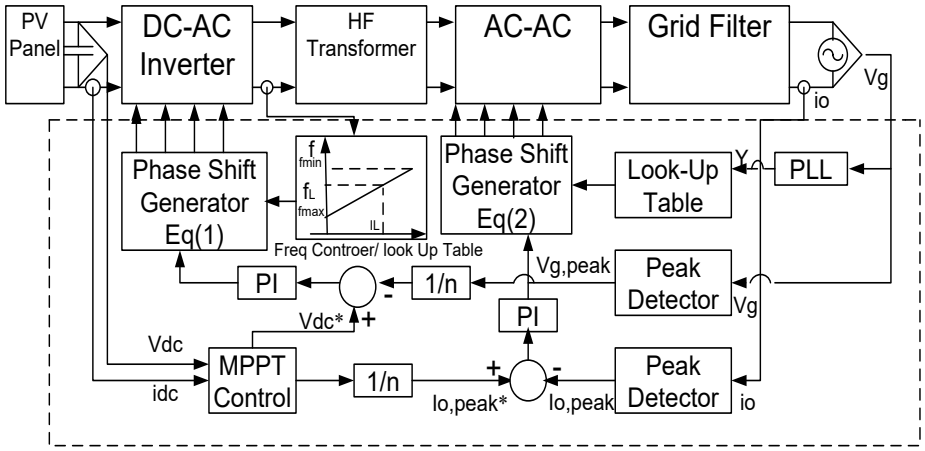

Fig. 8. Proposed Closed-Loop Control System

Fig. 10 shows how the frequency loop works. At light loads, the frequency is lower. Therefore, the voltage across the auxiliary inductor remains for a longer time, and the inductive current at the start of the switching transition is a larger value. For heavy loads, the frequency is higher, which decreases the peak value of the inductive current. The frequency control block is modeled by,

$$g(IL,\ t) = \mu \ \cdot\ IL(t) + fmin \tag{11}$$

$$fmax = \frac{V_{in}.t_d}{16L_{aux1}.C_{s1}.(V_{in}+V_{Z,min})} \tag{12}$$

$$fmin = \frac{V_{in}t_d}{16L_{aux1}.C_{s1}(V_{in}+V_{Z,max})} \tag{13}$$

$$\mu = \frac{f_{\max} - f_{\min}}{I_{L,\max}} \tag{14}$$

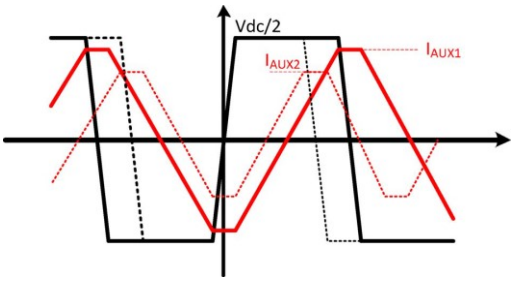

Fig. 9. Voltage and Current Waveform of Auxiliary Circuit Current (Output Current, Io)

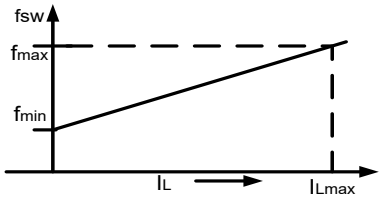

Fig.10. Frequency Control with Load

III. MATLAB SIMULATION MODEL

The micro-converter with the proposed topology along with the control strategy was simulated in the MATLAB Simulink environment. For the PV panel with PV cells, MPPT block was modeled using Simulink and SIM Power systems tool box in MATLAB.

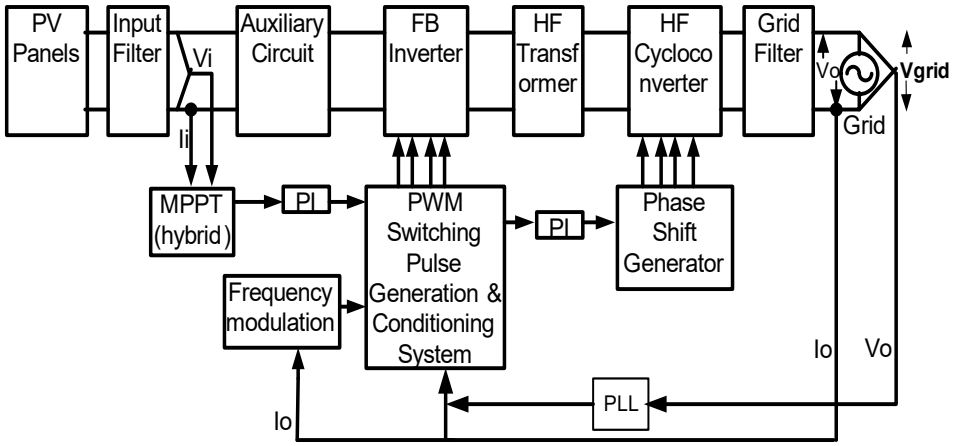

Fig. 11. MATLAB Simulation Block Diagram

The simulation with the Simulink model as shown in the Fig. 11 was carried iteratively for a large number of times with changing the controlling parameters, the frequency (fsw), the FB Inverter phase shift angle (θ) and the cycloconverter phase shift angle (φ). The frequency control was implemented with the help of the PWM switching pulse generation and pulse conditioning system by changing the loading conditions, as it was explained in section II: *D, Power Transfer Strategy*. The FB Inverter phase shift angle (θ) and the cycloconverter phase shift angle (φ) control were implemented independently by assuming one of them constant while another is varying. For all the times the output power with Eq. (1) and the input power (DC power of solar panel) were measured and the efficiency was found (Table 2).

Table 2. Solar Module Parameters

Parameters	Values
No. of Cells in Series, Ns	46
No. of Cells in Parallel. Np	02
Open Circuit Voltage, Vo	44.2V
Short Circuit Current, Isc	4.96 A
Series Resistance	1 Ω
Shunt Resistance	1000 Ω
Reverse Saturation Current	1.1753e-8 A
Ideality Factor	1.3
Voltage at Max Power Point, V_{mpp}	41.25 V
Current at Max Power Point,i_{mpp}	4.242 A
Power at Max Power Point, P_{mpp}	175 W

IV. Results

The converter with the proposed topology was modeled using MATLAB Simulink and the control policy was implemented in the direction to minimize the losses of all the switches as well as all other components of the circuit. The iterative simulation

results were sequenced to study the orientation of the proposed set-up and identify the conditions for the satisfactory performance. The efficiency and the losses were studied for all these iterative results. The achievable efficiency, 98.73% found as a result of ZVS operated H-bridge inverter, is well above the inverter topologies used and reported in some papers [23, 24, 26, 27]. This is possible only due to the fact that, the reactive current is controlled and made sufficient for the loss-less switching of all the switches used in this topology. The different waveforms were plotted along with their angular relationship. It was found that, for the implementation of the ZVS to all the switches, the inverter current Ix should be lagging to the Inverter Voltage $\boldsymbol{V_{fb}}$ by optimal angle $\theta main$ and leading to Vcc by the optimal angle φ_{main}. Fig. 12 shows this relationship. It also shows the maximum values of these quantities. Fig. 13 shows them in a Simplot mode of the GUI facility of Simulink. The use of Hybrid MPPT technique was useful to obtain the smooth and fast settling of the maximum power point which otherwise was very oscillating and sluggish using P&O MPPT as shown in Fig. 17. Hence the time of reaching the P_{max} point was reduced and thus power output and efficiency was increased as shown in Table 3.

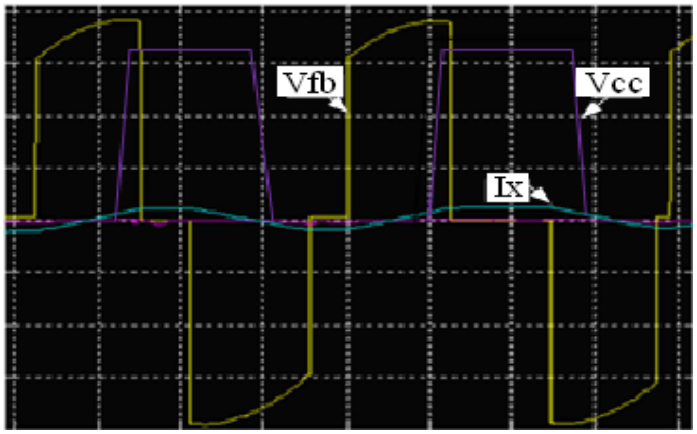

Fig. 12. MATLAB Simulation waveforms taken with the Simulink Model. V_{fb}: 38.6 V, *Vcc,max*=335.09 V, Net efficiency: 98.73%. Switching frequency: 91.41 kHz, Inverter current: Ix,max=3.59A, 5.66 A peak to peak.

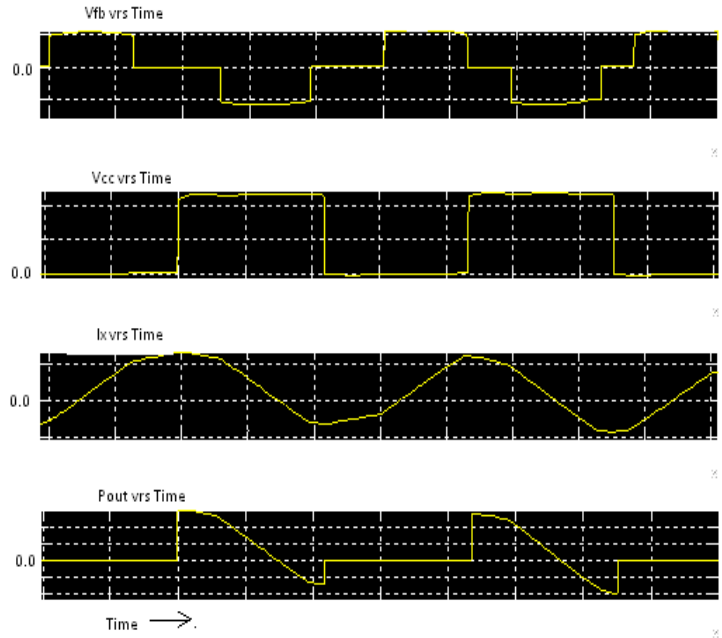

Fig.13. The Simulation resulted Waveforms: V_{fb}, V_{cc}(when V_g is positive half cycle), I_x, and P_o. It is the expanded version for explanation of their inter-relationship.

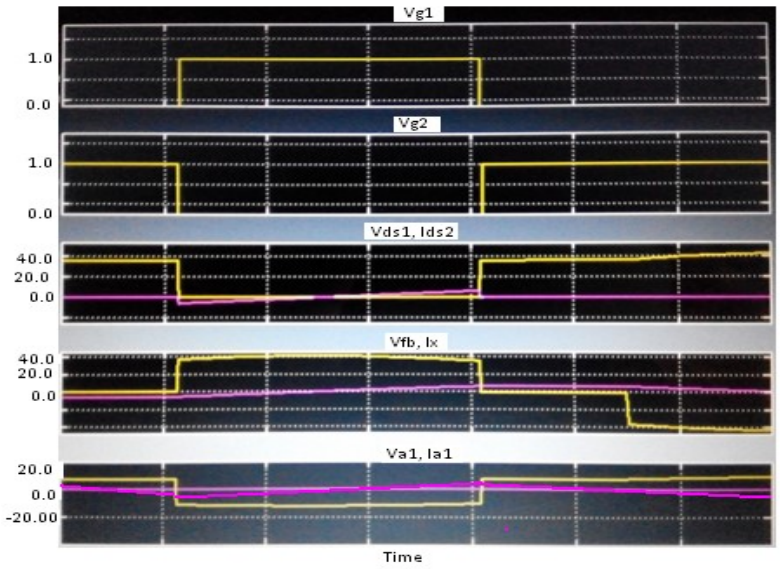

Fig.14. The Photograph of the Simulation Resulted Waveforms 1. Vg1, 2. Vg2; 3. Vds1 & Ids1; 4. Vfb & Ix; 5. Va1 & Ia1.

In the same way, Fig. 14 shows the variation of the % efficiency with the angle φ, fsw=94.41 kHz, θ=22.35 and full load. Fig. 14 shows the switching waveforms Vg1 & Vg2, voltage V_{ds1}& current $I_{ds1}$of the MOSFET no.1, the inverter voltage V_{fb}& current Ix and the voltage across & current through the auxiliary inductor L_{a1}.

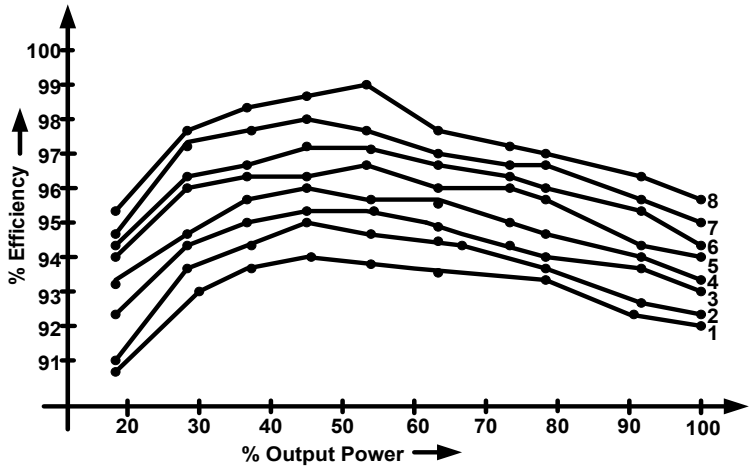

Fig. 15. The variations of % efficiency with respect to the % output power (The rated power of solar panel, 175 W assumed 100%), when the FB Inverter's phase shift angle θ (in degrees) takes values, 1: 106.06; 2: 91.35; 3: 80.15; 4: 63.40; 5: 45.75; 6: 36.15; 7: 16.6 (decreased by exceedingly greater degree than that for sr.no.8); 8: 22.35. Here φ = 12.55 degrees with switching frequency of 94.41 kHz at full load.

ZVS of the cycloconverter depends on the switching sequence of the power switches, as it was explained in the section II Design: Topology. For studying the control, full-bridge phase shift θ is varied from its minimum to maximum value and cycloconverter phase shift φ is also varied from its minimum to maximum value at each step of θ. These variations are shown in the Figures 15 and 16, respectively. The changes in the FB inverter phase shift angle θ were implemented in the simulation with respect to the phase shift time and accordingly the results were obtained iteratively along with the % output power. The rated power of solar panel - 175 W was assumed 100%. The cycloconverter phase shift angle φ = 13.55 degrees and switching frequency of 94.41 kHz were measured. The different angles, 'Θ' were taken starting from 126.15 to 16.6 degrees and it was found that highest efficiency achievable is at Θ = 22.35degrees.

Table 3. The efficiency of the converter under different conditions

Load	Efficiency with PO (%)	Efficiency with IC (%)	Efficiency with Hybrid (%)
30%	76.23	77.06	88.69
50%	80.12	85.52	90.12
100%	91.03	91.35	98.73

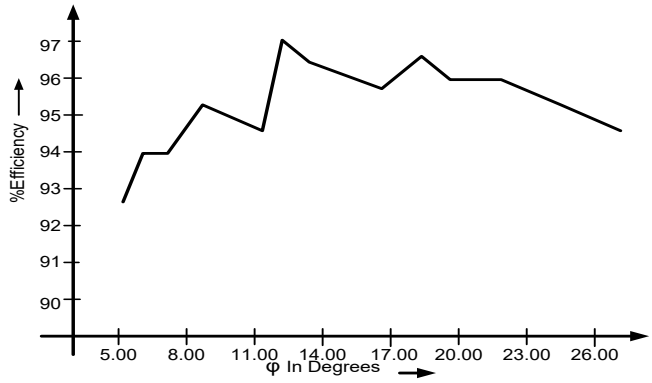

Fig. 16. The variations in efficiency for changes in Cycloconverter phase shift 'φ', with *fsw*=94.41 kHz, *θ*= 22.35 and full Load

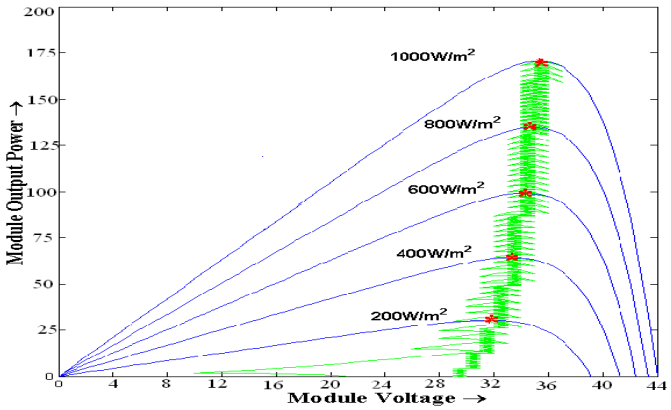

Fig. 17. Tracking of P&O MPPT method.

V. CONCLUSION

This paper introduces a microinverter for single-phase PV applications, which is suitable for conversion from low-voltage (35-50 V) DC to high voltage AC (*e.g.,* 230 V*rms* AC). The topology is based on a full-bridge inverter with auxiliary circuit, a high-frequency transformer, and a novel half-wave cycloconverter. The losses are minimized to a large extent by the application of ZVS for the switches of the inverter and the cycloconverter. For this, the reactive current given by the auxiliary inductor is controlled to an optimum level by using the frequency modulation. The hybrid MPPT helped in fast control and increased efficiency. With the help of the MATLAB simulation, the operational characteristics are analyzed, and a multi-dimensional control technique is utilized to achieve high efficiency, applying the frequency control, inverter phase shift control and cycloconverter phase control, which suggests the highest achievable efficiency of 98.73%.

CONFLICTS OF INTEREST

The authors declare that there is no conflict of interests regarding the publication of this paper.

REFERENCES

[1] D.R. Nayanasiri, D.M. Vilathgamuwa, D.L. Maskell, "Half-Wave Cycloconverter-Based Photovoltaic Microinverter Topology with Phase-Shift Power Modulation," *IEEE Transactions on Power Electronics*, vol. 28, no. 6, pp. 2700-2710, June 2013.

[2] A. Trubitsyn, B.J. Pierquet, A.K. Hayman, G.E. Gamache, C.R. Sullivan, D.J. Perreault, "High-Efficiency Inverter for Photovoltaic Applications", *2010 IEEE Energy Conversion Congress and Exposition*, pp. 2803-2810, Sept. 2010. DOI: 10.1109/ECCE.2010.5618163

[3] M. Pahlevaninezhad, J. Drobnik, P.K. Jain, A. Bakhshai, "A Load Adaptive Control Approach for a Zero-Voltage-Switching DC/DC Converter Used for Electric Vehicles," *IEEE Transactions on Industrial Electronics*, vol. 59, no. 2, pp. 920-933, February 2012.

[4] P.K. Jain, W. Kang, H. Soin, Y. Xi, "Analysis and Design Considerations of a Load and Line Independent Zero Voltage Switching Full Bridge DC/DC Converter Topology," *IEEE Transactions on Power Electronics*, vol. 17, no. 5, pp. 649-657, September 2002.

[5] F.Z. Peng, G.J. Su, L.M. Tolbert, "A Passive Soft-Switching Snubber for PWM Inverters," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 363-370, March 2004.

[6] Gwan-Bon Koo, Gun-Woo Moon, Myung-Joong Youn, "Analysis and Design of Phase Shift Full Bridge Converter with Series-Connected Two Transformers," *IEEE Transactions on Power Electronics*, vol. 19, no. 2, pp. 411- 419, March 2004.

[7] A. Zahedi, "Solar photovoltaic (PV) energy; latest developments in the building integrated and hybrid PV systems," *Renew. Energy*, vol. 31, no. 5, pp. 711–718, Apr. 2006.

[8] L. Zhang, K. Sun, Y. Xing, L. Feng, H. Ge, "A modular grid-connected photovoltaic generation system based on DC bus," *IEEE Trans. Power Electron.*, vol. 26, no. 2, pp. 523–531, Feb. 2011.

[9] R. Teodorescu, M. Liserre, P. Rodr´ıguez, "Grid Converters for Photovoltaic and Wind Power Systems", New York: Wiley, 2010.

[10] H. Krishnaswami, "Photovoltaic microinverter using single-stage isolated high-frequency link series resonant topology," in *Proc. IEEE Energy Convers. Congr. Expo.*, vol. 1, no. 1, pp. 495–500, Sep. 2011.

[11] A. Trubitsyn, B. Pierquet, A. Hayman, G. Gamache, C. Sullivan, D. Perreault, "High-efficiency inverter for photovoltaic applications," in *Proc. IEEE Energy Convers. Congr. Expo.*, vol. 1, pp. 2803–2810, Sep. 2010.

[12] H. Patel, V. Agarwal, "A single-stage single-phase transformer-less doubly grounded grid-connected PV interface," *IEEE Trans. Energy Convers.*, vol. 24, no. 1, pp. 93–101, Mar. 2009.

[13] T. Shimizu, K. Wada, "Flyback-type single-phase utility interactive inverter with power pulsation decoupling on the dc input for an ac photovoltaic module system," *IEEE Trans. Power Electron.*, vol. 21, no. 5, pp. 1264–1272, Sep. 2006.

[14] F. Blaabjerg, Z. Chen, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184–1194, Sep. 2004.

[15] D. Cao, S. Jiang, X. Yu, "Low-cost semi-z-source inverter for single phase," *IEEE Trans. Power Electron.*, vol. 26, no. 12, pp. 3514–3523, Dec. 2011.
[16] W. Yu, J. S. Lai, H. Qian, C. Hutchens, "High-efficiency MOSFET inverter with H6-type configuration for photovoltaic nonisolated AC-module applications," *IEEE Trans. Power Electron.*, vol. 26, no. 4, pp. 1253–1260, Apr. 2011.
[17] K. Chomsuwan, P. Prisuwanna, "Photovoltaic grid-connected inverter using two-switch buck-boost converter," in *Proc. IEEE Photovoltaic Spec. Conf.*, pp. 1527–1530, May 2002. DOI: 10.1109/PVSC.2002.1190902
[18] B. Yang, W. Li, Y. Gu, W. Cui, X. He, "Improved transformerless inverter with common-mode leakage current elimination for a photovoltaic grid-connected power system," *IEEE Trans. Power Electron.*, vol. 27, no. 2, pp. 752–762, Feb. 2012.
[19] S. Funabiki, T. Tanaka, "A new buck-boost-operation-based sinusoidal inverter circuit," in *Proc. IEEE Power Electron. Spec. Conf.*, vol. 4, pp. 1624–1629, 2002.
[20] S.Y. Tseng, H.-Y. Wang, "A photovoltaic power system using a high step-up converter for DC load applications," *Energies*, vol.6, pp. 1068–1100, 2013.
[21] L. Chen, A. Amirahmadi, Q. Zhang, N. Kutkut, I. Batarseh, "Design and Implementation of Three-Phase Two-Stage Grid-Connected Module Integrated Converter", *IEEE Transactions on Power Electronics*, vol. 29, no. 8, pp. 3881 – 3892, August 2014.
[22] A. Mudassar, Y. Xu, H. Liu, L. Hang, G. Li, H. Hu, "Two-Stage Single-Phase Photovoltaic Grid-Tied Micro-Inverter Using Soft-Switching Techniques" *IEEE 2nd Annual Southern Power Electronics Conference (SPEC)*, pp. 1 - 6, 2016. DOI: 10.1109/SPEC.2016.7846048
[23] Y. Zhang, J. Umuhoza, H. Liu, C. Farrell, H.A. Mantooth, "Optimizing efficiency and performance for single-phase photovoltaic inverter with dual-half bridge converter" *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, pp. 1507-1511, 2015. DOI: 10.1109/APEC.2015.7104547
[24] W.J. Cha, Y.W. Cho, J.M. Kwon, B.H. Kwon, "Highly Efficient Microinverter With Soft-Switching Step-Up Converter and Single- Switch-Modulation Inverter", *IEEE Transactions on Industrial Electronics*, vol. 62, no. 6, pp. 3516 – 3523, 2015.
[25] Y. Chen; D. Xu, "Control of ZVS single-phase grid inverter with higher power quality", *2017 IEEE 18th Workshop on Control and Modeling for Power Electronics (COMPEL)*, pp. 1-8, 2017. DOI: 10.1109/COMPEL.2017.8013390
[26] M. Tofighazary, M. Sabahi, E. Babaei, F.A.A. Meinagh, "Modified Single-Phase Single-Stage Grid-tied Flying Inductor Inverter with MPPT and Suppressed Leakage Current", *IEEE Transactions on Industrial Electronics*, vol. 65, no. 1, pp. 221 - 231, 2018. DOI: 10.1109/TIE.2017.2719610
[27] M.I. Munir, T. Aldhanhani, K.H.A. Hosani, "Control of Grid Connected PV Array Using P&O MPPT Algorithm", *2017 Ninth Annual IEEE Green Technologies Conference (GreenTech)*, pp. 52-58, 2017. DOI: 10.1109/GreenTech.2017.14
[28] A. Anzalchi, M. Moghaddami, A. Moghadasi, M.M. Pour, A. Sarwat, " Design and Analysis of a Higher Order Power Filter for Grid-Connected Renewable Energy Systems", *IEEE Transactions on Industry Applications,* vol. 53, no. 5, pp. 4149 - 4161, 2017