PH.D. DISSERTATION

A LOW-NOISE SENSOR INTERFACE FOR OPTICAL PARTICULATE MATTER DETECTORS

미세입자 검출을 위한 저잡음 광학 센서 인터페이스

BY

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이 논문을 공학박사 학위논문으로 제출함

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ABSTRACT

A LOW-NOISE SENSOR INTERFACE FOR OPTICAL PARTICULATE MATTER DETECTORS

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In this study, I propose a low-noise sensor interface for optical particulate matter (PM) detectors. The particles are classified as particulate matter 10 (PM_{10}) (< 10 μm), $PM_{2.5}$ (< 2.5 μm), and PM_1 (< 1 μm) depending on the diameter of them. The optical PM detector uses a photodiode (PD) to measure the amount of light scattered by particles emitted from a light emitting diode (LED) or a laser diode (LD). The received input current signal is converted to a voltage signal at the transimpedance amplifier (TIA), amplified and filtered after removing the DC offset of the input. It is then applied to an analog-to-digital converter (ADC) for digitization. The conventional correlated double sampling (CDS) technique only can be applied to the discrete-time switched-capacitor (SC) circuit that is generally power-consuming and needs large chip area than continuous-time circuits. Another typical method using a current-steering digital-to-analog converter (DAC) generates large intrinsic device noise or requires large power consumption and chip area to reduce the noise. In this study, I propose a DC offset calibration method using an operational amplifier (OPAMP) with embedded DAC only when the light source is turned on. In addition, an average power control (APC) circuit is used to make the light intensity of the LD less sensitive against the external environmental changes or noise. The APC circuit monitors the light intensity using the reference photodiode and controls the bias current of the LD to get the light intensity be constant when it is changed. This enables small-sized particles to be measured with high resolution. The digital post-processing is performed as the following procedure. First, a PM calculation is performed to calculate the concentration by particle size. Then it is low-pass filtered to remove high-frequency noise. The concentration-based curve fitting algorithm is then carried on to make the concentration profile linear. And next, the offset compensation is performed according to the temperature of which information is generated by on-chip temperature sensor. Finally, the gain-compensated output is sent through a digital interface such as pulse-width modulation (PWM), universal asynchronous transmitter (UART), and serial peripheral interface (SPI). The measurement is conducted in a chamber with two types of optical PM detector that uses LED and LD as a light source, respectively. The result is analyzed by comparing the result of the reference mass profiler located in the same chamber. The experimental results showed high accuracy in PM_1, $PM_{2.5}$ and PM_{10}. The square of the correlation coefficient (R^2) showed more than 0.999 in all measurement, and the maximum consistency errors of the LED module and the LD module are +/- 5 % and +/- 1.6 %, respectively, which is much better than other commercial optical PM detectors. All chips were fabricated with a 0.18 μm standard CMOS process. The chip areas are

$6.49\ mm^2$ and $6.27\ mm^2$, and power consumptions are 5 mW and 10 mW (excluding bias current of the light sources) for the LED PM detector and the LD PM detector, respectively.

Keywords: optical particulate matter detector, smoke, dust, offset calibration, average

power control.
Student Number: 2014-30303

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CHAPTER 1

INTRODUCTION

1.1 PARTICULATE MATTER

In recent years, contamination of air due to increase in particles has become serious, threatening people's health. Particles can pose a health risk when they are accumulated in the respiratory system. Air pollutants from fossil fuels such as petroleum and coal, or emissions from automobile soot are known to be the main causes of the particles. The particles are classified as particulate matter 10 (PM_{10}) (< 10 μm), $PM_{2.5}$ (< 2.5 μm), and PM_1 (< 1 μm) depending on the diameter of them. Smaller particles are more likely to be absorbed by the human body and can be a health hazard. For example, PM_1 particles travel into the deep lungs through the cell membranes of the alveoli, damaging the arterial lining and penetrating tissue of the cardiovascular system.

Table 1.1.1 shows the air quality index (AQI) and categories for $PM_{2.5}$ and PM_{10} concentrations according to the United States Environmental Protection Agency (US EPA). The AQI is obtained by measuring the weight of particles accumulated in 1 cubic

Table 1.1.1 Corresponding AQI Categories for $PM_{2.5}$ and PM_{10} concentrations according to US EPA.

$PM_{2.5}$ ($\mu m/m^3$) 24-Hour Average	PM_{10} ($\mu m/m^3$) 24-Hour Average	AQI	Category
0.0 – 12.0	0 – 54	0 – 50	Good
12.1 – 35.4	55 – 154	51 – 100	Moderate
35.5 – 55.4	155 – 254	101 – 150	Unhealthy for sensitive groups
55.5 – 150.4	255 – 354	151 – 200	Unhealthy
150.5 – 250.4	355 – 424	201 – 300	Very unhealthy
250.5 – 350.4	425 – 504	301 – 400	Hazardous
350.5 – 500.4	505 - 604	401 - 500	Hazardous

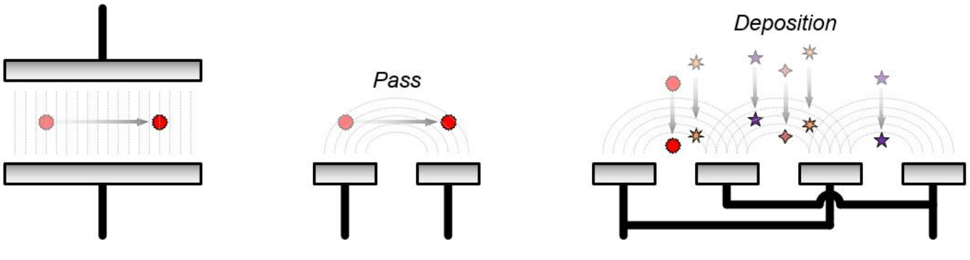
meter for 24 hours, so called gravimetric measurement. This method is suitable for monitoring the average air quality change, but it is not suitable for knowing the instant air quality change. Recently, the real-time measurement of the air quality is strongly required since the PM detecting sensors are widely equipped in the indoor air purifiers or internet-of-things (IoT) devices.

1.2 PARTICULATE MATTER DETECTOR

1.2.1 CAPACITIVE SENSORS

Capacitive PM detecting sensors use the principle of impedance variation measured by a pair of electrodes near the PM stream. Since the relative permittivity of particles is usually larger than the dielectric constant of air, the capacitance between the electrodes increases as the particles are placed between the electrodes [1.2.1]. There are three main configurations of the capacitive sensors: parallel, single coplanar, and multiple interdigitated coplanar as shown in Fig. 1.2.1.

As shown in Fig. 1.2.1 (a), the capacitance change between the electrodes depends on the particle size and the dielectric constant in the parallel-plate electrodes method. This method has the advantage that the distance of particles from the plates and the



(a) (b) (c)

Fig. 1.2.1 Possible configurations of the capacitive sensor of PM in air: (a) parallel-plate microelectrodes for in-flow detection of PM, (b) single coplanar pair of electrodes and (c) multiple interdigitated electrodes [1.2.1].

change of capacitance are independent, but has the disadvantage that the distance between fixed plates limits the size of particles that can be detected. The coplanar electrodes method of Fig. 1.2.1 (b) and (c) has an advantage of being easy to process and suitable for detecting various particle sizes. The capacitance change is shown as a pulse which represents the capacitance change when the particle passes over the electrode in the single coplanar pair structure as depicted in Fig. 1.2.1 (b). The disadvantage of this method is that even if particles of the same size are present, the change in capacitance varies depending on how far away they are from the electrode. In addition, capacitance mismatch between the electrodes is large. As shown in Fig 1.2.1 (c), there is another method of implementing multiple pairs of electrodes on a wide area implemented on the same plane. This method reads the capacitance that is changed by the deposited particles and has the effect of averaging the capacitance mismatch between the electrodes. Also, the distance between the particles and the electrodes does not affect the signal, unlike the single electrode pair since the capacitance between electrodes varies due to the deposited particles. However, there is a disadvantage that particles need to be cleaned periodically.

Fig. 1.2.2 shows the example of the capacitive PM detector which has the CMOS-integrated and interdigitated multiple pairs of electrodes [1.2.2]. The signal-to-noise ratio (SNR) has the relations with other design parameters as follows:

$$SNR \propto \frac{\left(\Delta C V_{ref}\right)^2}{4kT/g_m \cdot \left(C_{elec} + C_{p,amp} + C_{p,stray}\right)^2 ENBW} \qquad (1.2.1)$$

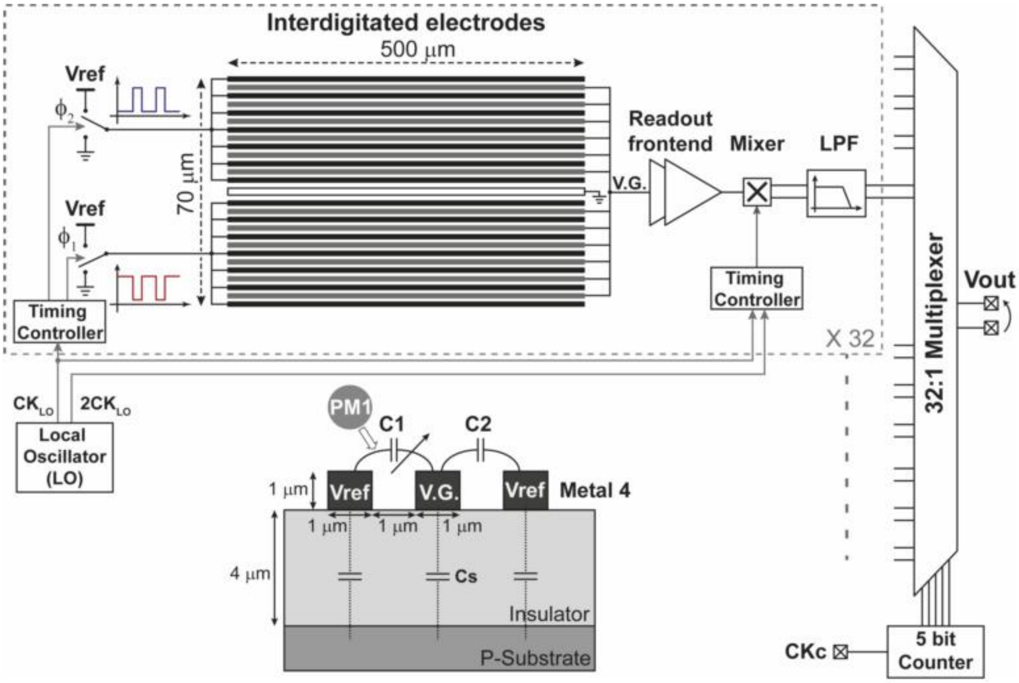


Fig. 1.2.2 Circuit overview of the CMOS capacitive dust sensor with a quoted cross-section of the on-chip electrodes [1.2.2].

where V_{ref} is the voltage applied to the capacitive electrodes, C_{elec} is the capacitance between two electrodes, $C_{p,amp}$ is the input capacitance of the readout front-end, $C_{p,stray}$ is the parasitic capacitance in the connections, and the ENBW is the equivalent noise bandwidth of the readout integrated circuit (ROIC).

Most systems that read minute capacitance changes from aF to zF scale in response to small particles use the lock-in technique [1.2.3] - [1.2.4], as shown in Fig. 1.2.3. In the lock-in technique, a sinusoidal voltage is applied to the impedance and the resulting

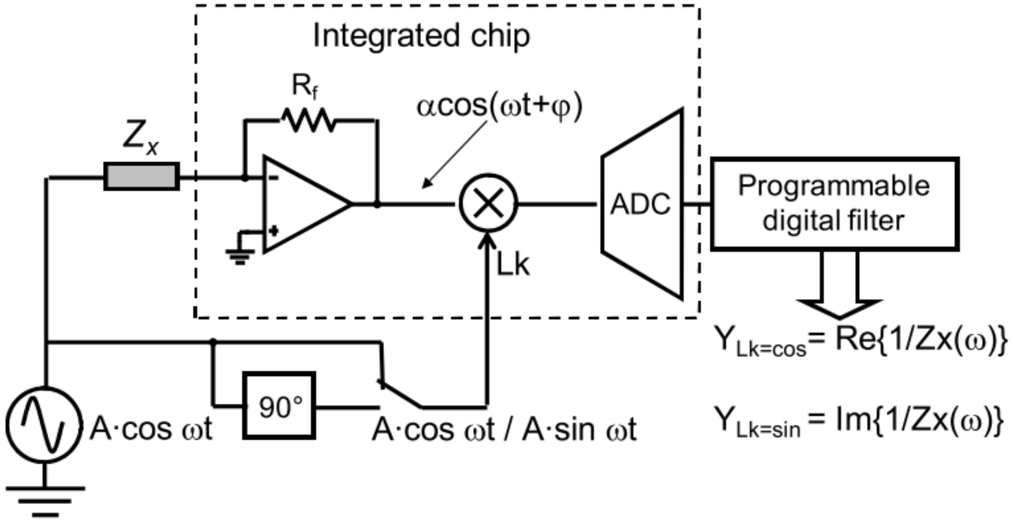


Fig. 1.2.3 Lock-in technique for impedance-characterization system [1.2.3].

current signal is converted to a voltage signal in the transimpedance amplifier (TIA). The converted voltage signal is multiplied by a sinusoidal signal having the same phase difference and a sinusoidal signal having a phase difference of 90 ° applied to the impedance. This is done by analog-to-digital conversion and digital filtering to extract the real and imaginary parts of the signal.

1.2.2 OPTICAL SENSORS

Fig. 1.2.4 shows a sample optical PM detector module [1.2.5]. The operation sequence is as follows. First, air is flowed from the outside by making an air flow while returning to the fan in the PM detector module. The LD that receives the current from the

LD driver in the inside irradiates the light perpendicular to the direction of the air flow. At this time, it is collected on the PD through the lens, so that scattering occurs even on small particles. PD is located in a direction (x-asix) in which light is emitted, in a direction in which air flows (y-asix) and in a direction orthogonal to z-asix, and light scattered by particles reaches PD. Light that does not strike the particle is attenuated in

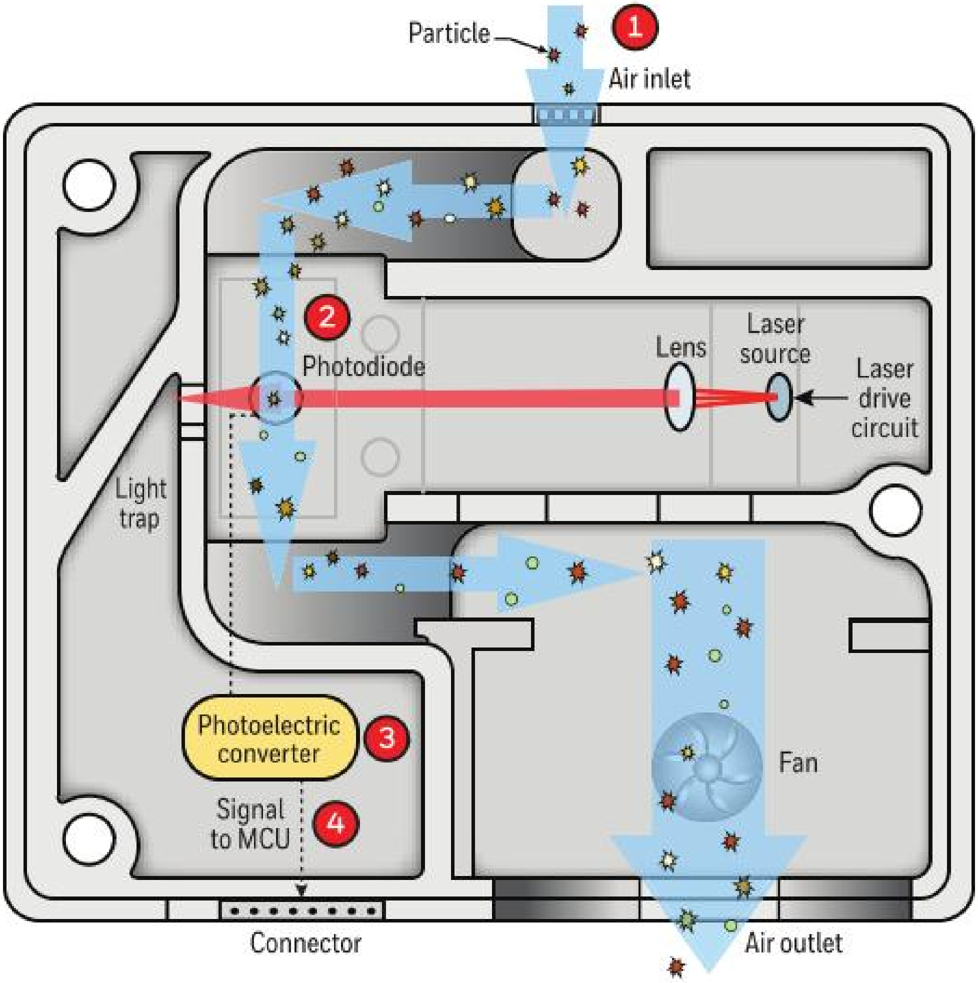


Fig. 1.2.4 A sample optical PM detector module [1.2.5].

the light trap, preventing the reflected light from scattering back into the particle. It is common to use a module black-dyed wall to reduce the reactivity of such reflected light to particles, and to minimize reflection with a lamella-structured wall [1.2.6]. The air then exits the module through the fan. The light reaching the PD generates a current signal and transmits it to the ROIC.

The relationship between general particles and scattering is explained by Mie theory. According to Mie theory, dust concentration is measured using light scattering. It is affected by the scatter receive angle and the wavelength of light and its measurement principle is as follows [1.2.7]:

The scattered light intensity I is,

$$I = \frac{N \cdot I_0 \cdot F(\theta, \varphi)}{k^2 r^2} \qquad (1.2.2)$$

Where I0 is the incident light intensity, r is the radius of a particle, k(=2π/λ) is the wave number, and N is the total number of particles.

The mass concentration of dust particles number is,

$$M_V = \frac{(4\pi^3 r^2 \rho I)/I_0}{3\lambda^2 V \sum_i \frac{[i_1(\theta)+i_2(\theta)]_i \cdot n_r(D_i)}{D_i^3} \cdot \Delta D_i} \qquad (1.2.3)$$

Where V is the air flow with dust and n_r (D) is the normalized frequency distribution function of particle group.

Mie theory suggests a simple model between spherical particles and optical flux, but in reality, Rayleigh scattering and Fraunhofer diffraction occur depending on the size of the particles, resulting in a more complex shape [1.2.8]. Rayleigh scattering is applied to small-sized particles (less than about 0.06 μm), and Fraunhofer diffraction is applied to large-sized particles (about 2.0 μm or more) [1.2.9]. The angular light flux (F) by the single-particle with a diameter of D due to Rayleigh scattering and Fraunhofer diffraction relations are as follows:

$$Rayleigh\ scattering: F \propto D^6 \tag{1.2.4}$$

$$Fraunhofer\ diffraction: F \propto D^2 \tag{1.2.5}$$

In the case of the optical PM detector capable of reading the particle size from PM_1 to PM_{10}, the light flux and the particle diameter formula cannot be expressed only by either Eq. (1.2.4) or (1.2.5). It is expressed as a combination of the two equations as follows:

$$F \propto aD^6 + bD^2 \qquad (1.2.5)$$

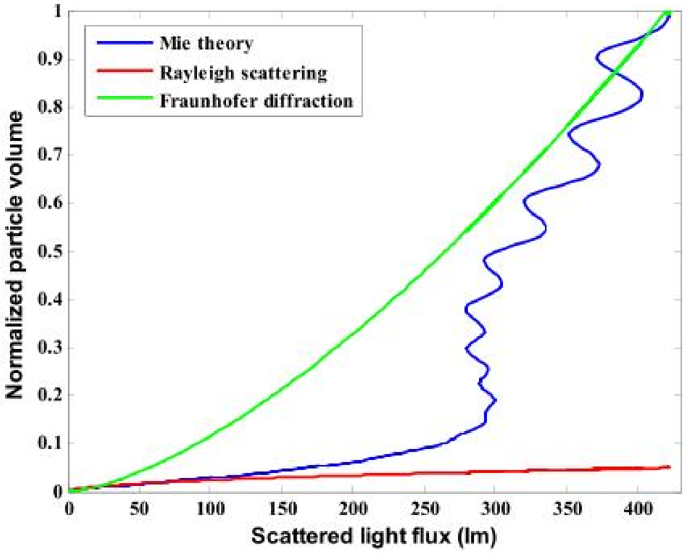


Fig. 1.2.5 Relationships between scattered light flux and corresponding normalized particle volume [1.2.8].

Where a and b are the coefficients for Rayleigh scattering effect and Fraunhofer diffraction, respectively. Fig. 1.2.5 shows the relationships between scattered light flux and corresponding normalized particle volume among Mie theory, Rayleigh scattering, and Fraunhofer diffraction.

1.3 THESIS ORGANIZATION

This paper consists of five chapters on the optical PM detector. The first chapter introduces the concept of PM and a general description of the PM sensor divided into capacitive sensor and optical sensor. Chapter 2 explains the architecture and design considerations of an optical PM detector in terms of analog front-end (AFE) and digital back-end (DBE). This chapter also describes the effectiveness of DC offset and light intensity variation and typical calibration schemes, which are the challenges of the optical PM detector. Chapter 3 introduces the circuit implementation of the proposed optical PM detector. Specifically, this chapter includes an analog DC offset calibration technique to remove the DC offset of the light source, on-chip temperature sensor to make the ROIC less sensitive to the temperature change. And the digital post-processing that includes PM calculation, concentration-based curve fitting, temperature-dependent offset compensation, and gain compensation. And then other power management circuit such as Undervoltage-lockout (UVLO), bandgap reference (BGR), and oscillator (OSC). Chapter 4 discusses experimental setup and results for two different types of the proposed PM detector that uses LED and LD, respectively. Finally, chapter 5 summarizes this study and concludes.

CHAPTER 2

ARCHITECTURE AND DESIGN CONSIDERATIONS OF THE OPTICAL PARTICULATE MATTER DETECTOR

2.1 INTRODUCTION

Fig. 2.1.1 shows the structure of the conventional optical PM detector. The light emitted from the LED or LD is gathered at one point through the lens, and the degree of scattering depends on the size and concentration of the particles passing through this point and the reflection index. The main signal paths of the ROIC are an AFE consisting of a transimpedance amplifier (TIA), a DC offset calibration circuit, a digital-to-analog converter (DAC), programmable gain amplifiers (PGAs), filters, and an analog-to-digital converter (ADC). Strictly, ADCs do not belong to either the AFE or the DBE, but for the sake of simplicity I have included the ADC in the AFE. A microcontroller unit (MCU) that receives and processes signals output from an ADC and controls the AFE and DBE is called a so-called DBE. The MCU extracts concentration information by size from the digitized PM signal and digitally filters it to improve the SNR. Finally, signals are transmitted to the outside through interface circuits such as UART or SPI.

The DAC or DC offset calibration circuit can be replaced with correlated double sampling (CDS) circuit when the AFE is the switched-capacitor (SC) circuit [2.2.1]. Filter stages such as low-pass filters (LPFs) and high-pass filters (HPFs) are required to reduce out-of-band noise. LPFs are usually embedded in TIA and PGAs by feedback RC network. The HPFs often have an external RC network because their cut-off frequency is often as low as several kHz. The DBE of the PM detector is also implemented by an MCU outside the chip. In this case, however, there is a disadvantage in that it is not possible to guarantee an optimal control setting value to compensate for changes in characteristics of the sensor and the AFE.

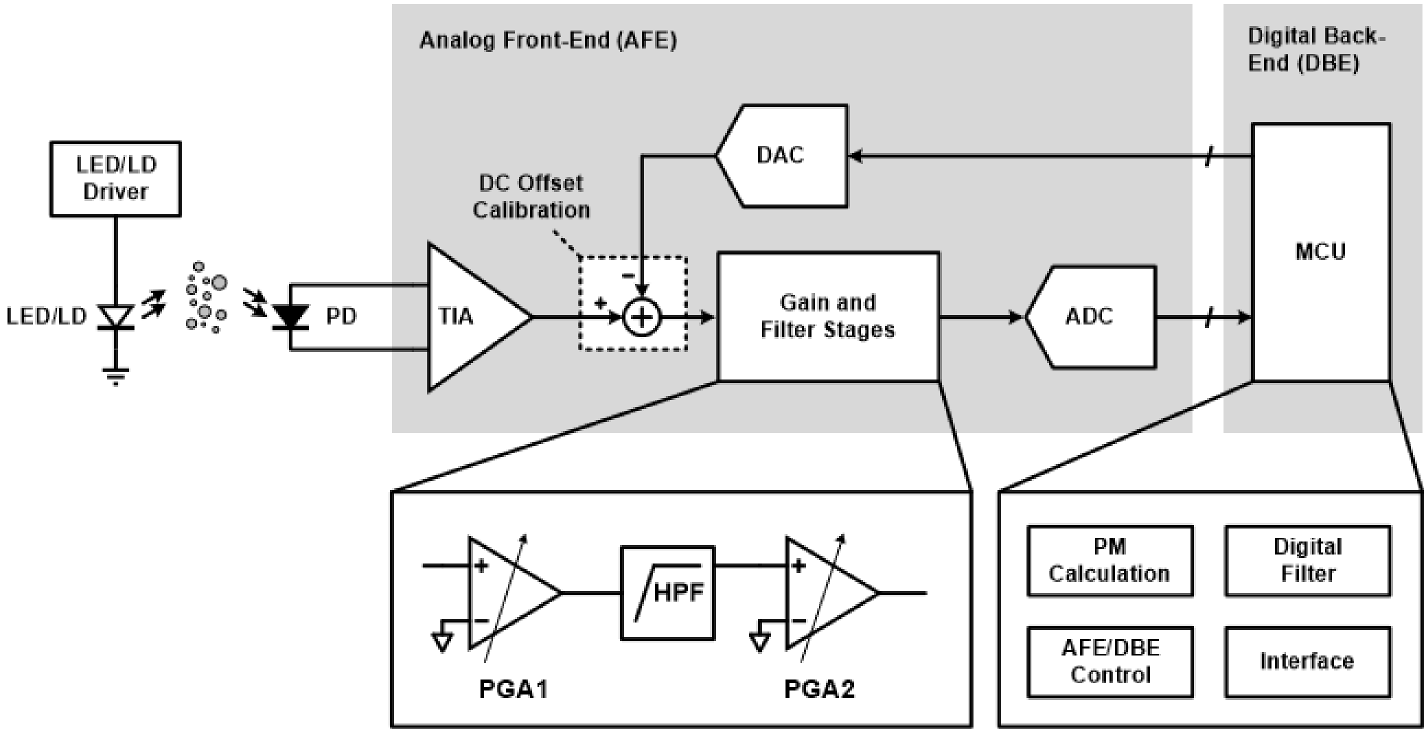


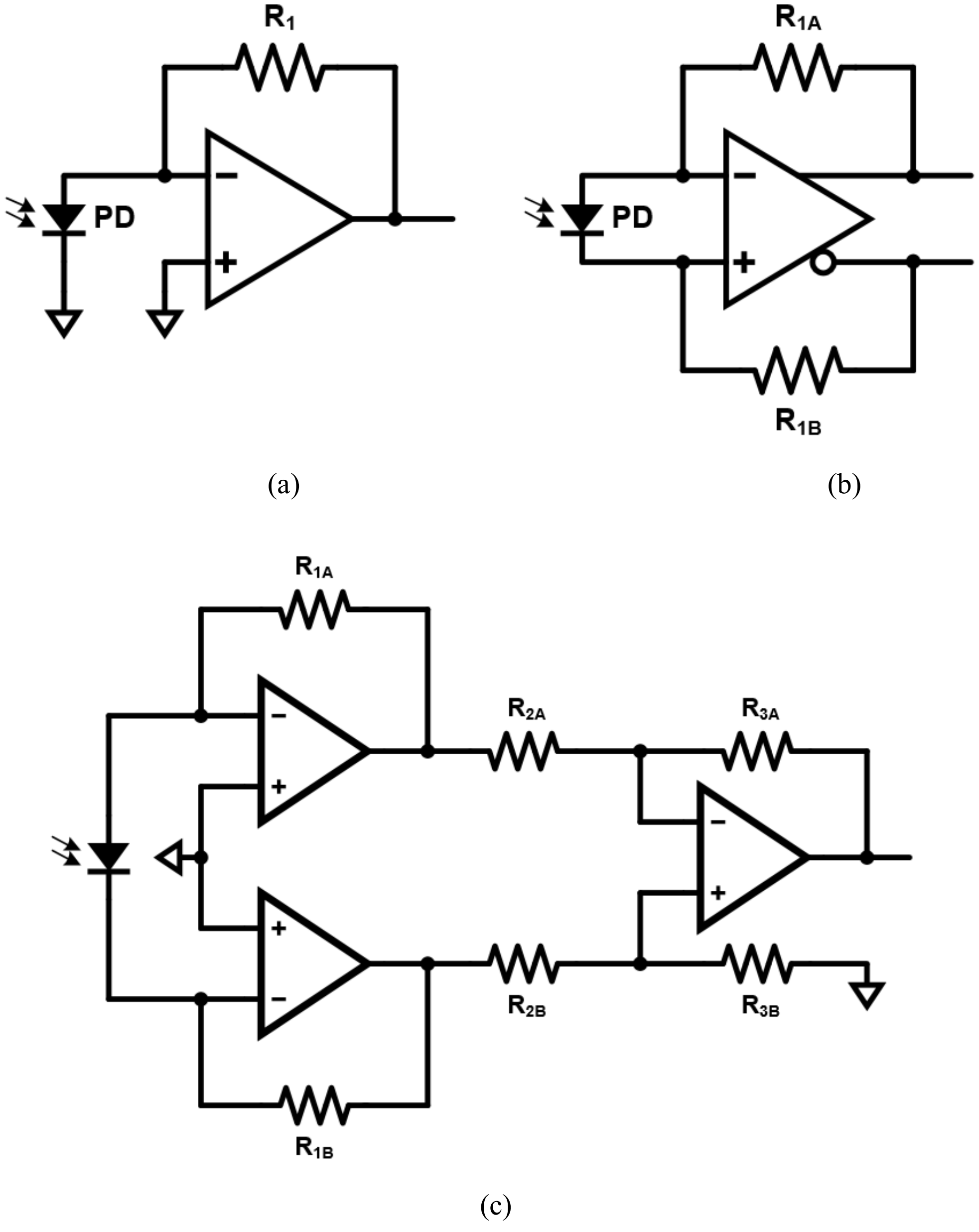
Fig. 2.1.1 Architecture of the optical PM detector.

2.2 ANALOG FRONT-END CIRCUIT

2.2.1 TRANSIMPEDANCE AMPLIFIER

When the light emitted from the light source is scattered by the particles and reaches the PD, a dielectric current is generated in the PD. The TIA is used to convert the current input signal to a voltage signal. Fig. 2.2.1 shows the three topologies of the TIA. First, Fig.2.2.1 (a) is the simplest single-ended TIA and the output voltage is the product of the feedback resistance R1 at the input current when the DC gain of the operational amplifier (OPAMP) is large enough. This structure degrades performance due to power supply noise due to poor power supply rejection ratio (PSRR) characteristics. Fig. 2.2.1 (b) shows the PSRR characteristics due to the balanced structure as a fully-differential structure. In addition, there is an advantage that a reference for biasing of the input PD is not necessary. Fig. 2.2.1 (c) shows the structure of the instrumentation amplifier which is often used for accurate impedance measurement. This method has low DC offset, high input impedance, and high loop gain characteristics.

In this study, it is possible to remove the DC offset of the TIA as well as the input DC offset in the DC offset calibration circuit described later. Also, it is recommended that input impedance and loop gain should be kept at appropriate levels considering power consumption. The supply power of the AFE is primarily regulated by a low-dropout (LDO) regulator, but the differential structure of the TIA is suitable because the intrinsic noise of



(a) (b)

(c)

Fig. 2.2.1 Three topologies of TIA. (a) Single-ended amplifier (b) Fully-differential amplifier (c) Single-ended instrumentation amplifier.

the LDO and BGR circuits cannot be ignored. In this study, The power-efficient and fully-differential TIA of Fig. 2.2.1 (b) was used.

Power supply noise can be attenuated through a fully-differential structure, but the intrinsic noise of the TIA needs to be minimized. Fig. 2.2.2 is the noise model of the single-ended TIA with PD. In general, a feedback capacitor is included to limit the bandwidth of the TIA. This feedback capacitor is included for more accurate noise analysis. Among the total output noise, the voltage noise source of OPAMP has the following contribution:

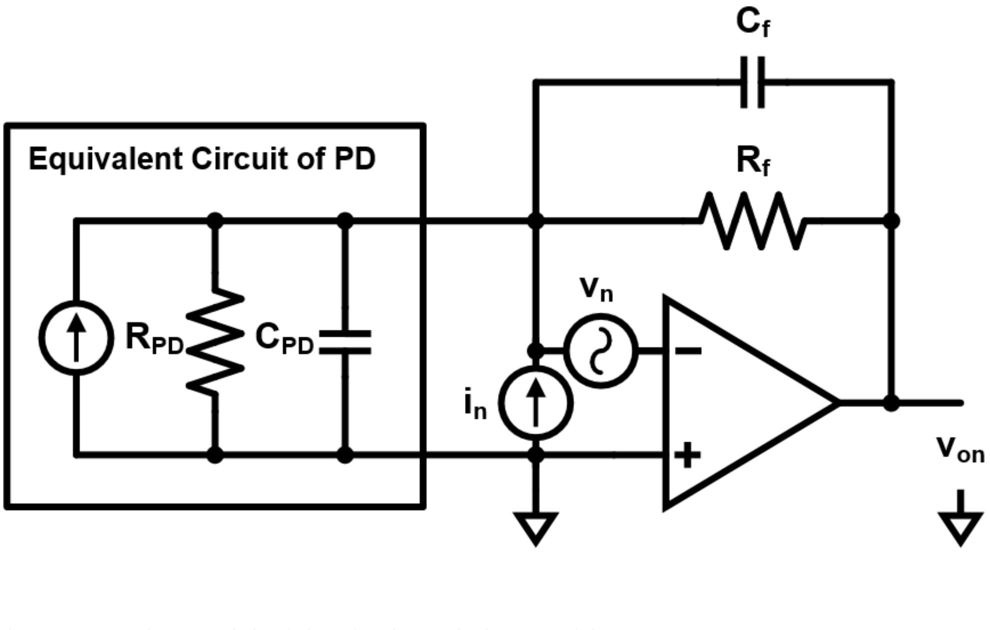


Fig. 2.2.2 Noise model of the single-ended TIA with PD.

$$v_{on,v_n} = \left(\frac{A}{1 + A\beta}\right) v_n \cong \frac{1}{\beta} v_n \qquad (2.2.1)$$

$$\frac{1}{\beta} = 1 + \frac{R_f}{R_{PD}} \cdot \frac{(R_{PD} C_{PD} s + 1)}{(R_f C_f s + 1)} \qquad (2.2.2)$$

Where A is the open-loop DC gain of the OPAMP, β is the feedback factor. The contribution of the current noise source of OPAMP to the output noise is calculated as follows:

$$v_{on,i_n} = R_f C_f s \cdot i_n \qquad (2.2.3)$$

The output noise due to the feedback resistor, R_f, can be calculated as:

$$v_{on,R_f} = \sqrt{4kTRB} = \sqrt{4kTR_f \left(\frac{\pi}{2} \cdot \frac{1}{2\pi R_f C_f}\right)} = \sqrt{\frac{kT}{C_f}} \qquad (2.2.4)$$

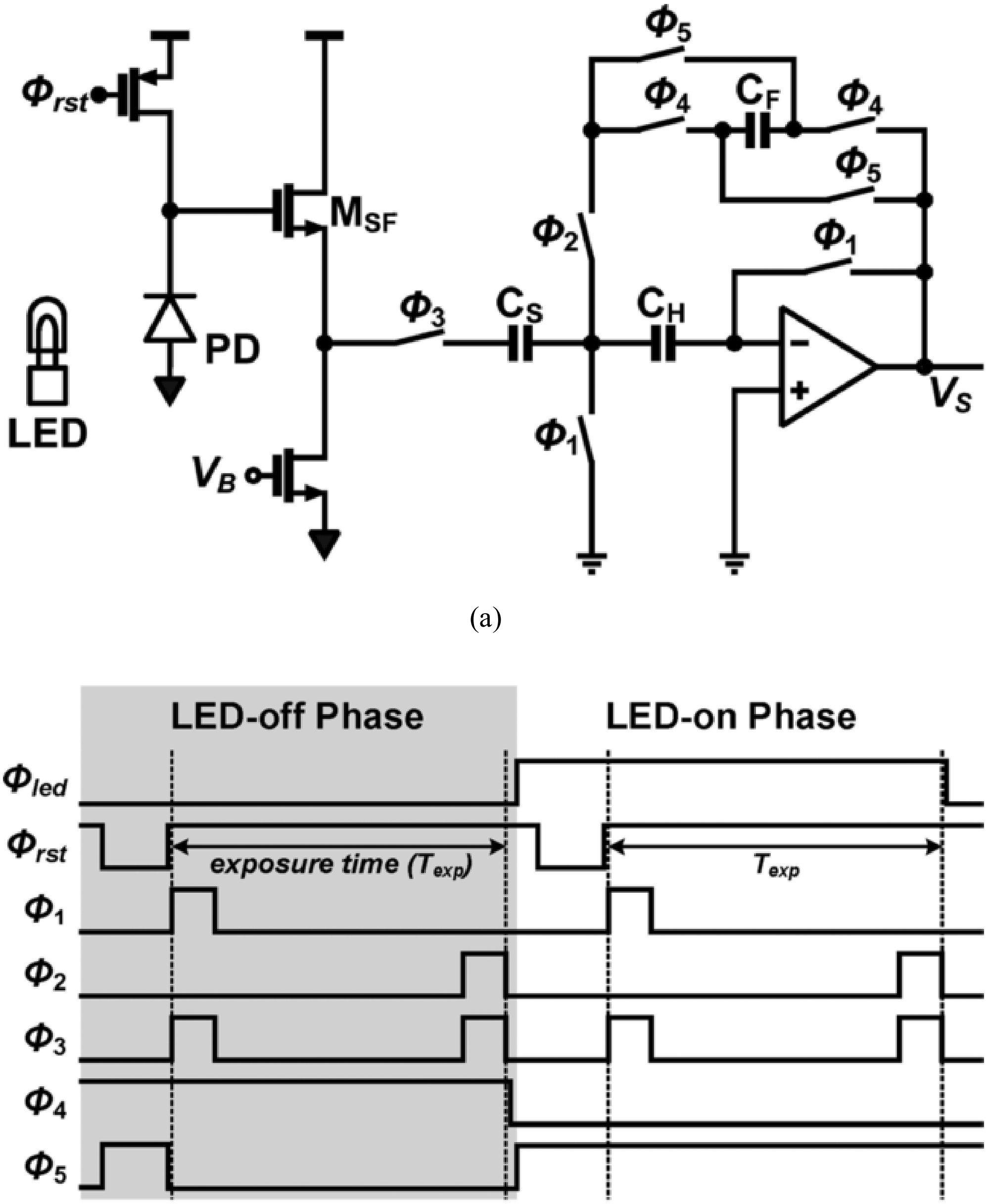
Where B is the effective noise bandwidth, k is the Boltzmann's coefficient which is 1.38×10^{-23} J/K and T is the absolute temperature. Eq. (2.2.4) represents that the noise contribution of R_f is not a function of R_f but a function of C_f. Then, the total output noise voltage is derived as follows:

$$v_{on} = \sqrt{v_{on,v_n}^2 + v_{on,i_n}^2 + v_{on,R_f}^2} \qquad (2.2.5)$$

2.2.2 DC OFFSET CALIBRATION

In the optical PM detector, as shown in Fig. 2.2.3, using the chamber wall material and the structure, even though it does its best to prevent dark current in the PD when there is no particle, offset is one of the major causes of degradation of SNR and dynamic range (DR) performance. Usually, the optical PM detector does not always turn on the light for a long readout time but turns on the light only at the required moment and turns off the light to increase the life of the light source and reduce the power consumption of the ROIC. Fig. 2.4.1 shows the application of a CDS technique to remove DC offsets in a SC ROIC [2.2.1]. This method stores the input value in C_H in the LED-off phase, then reads only the signal excluding the reset value stored in the LED-on phase, and removes the DC offset. With this CDS method, the dark current of the ambient light and the PD itself, DC offset and low-frequency noise of the M_{SF} and ROIC can be removed. However, in the LED-on phase, the offset from the reflected light from the LED to the chamber wall is not removed. This method is also applicable to discrete-time ROIC and is not applicable to the continuous-time ROIC that is generally more power-efficient than the discrete-time ROIC.

To overcome the limitations of the CDS technique and to remove the DC offset in the continuous-time ROIC, there is a current-steering DAC scheme as shown in Fig. 2.2.4. This is often used in bio-application sensors [2.2.2]-[2.2.3]. The output of the current DAC can be connected to the input of the TIA to remove the DC offset in current form, or it can be connected to the TIA output stage or the input stage of the next stage to remove the DC



(a)

(b)

Fig. 2.2.3 Schematic and timing diagrams of SC ROIC using CDS technique. (a) Schematic diagram. (b) Timing diagram [1.2.5].

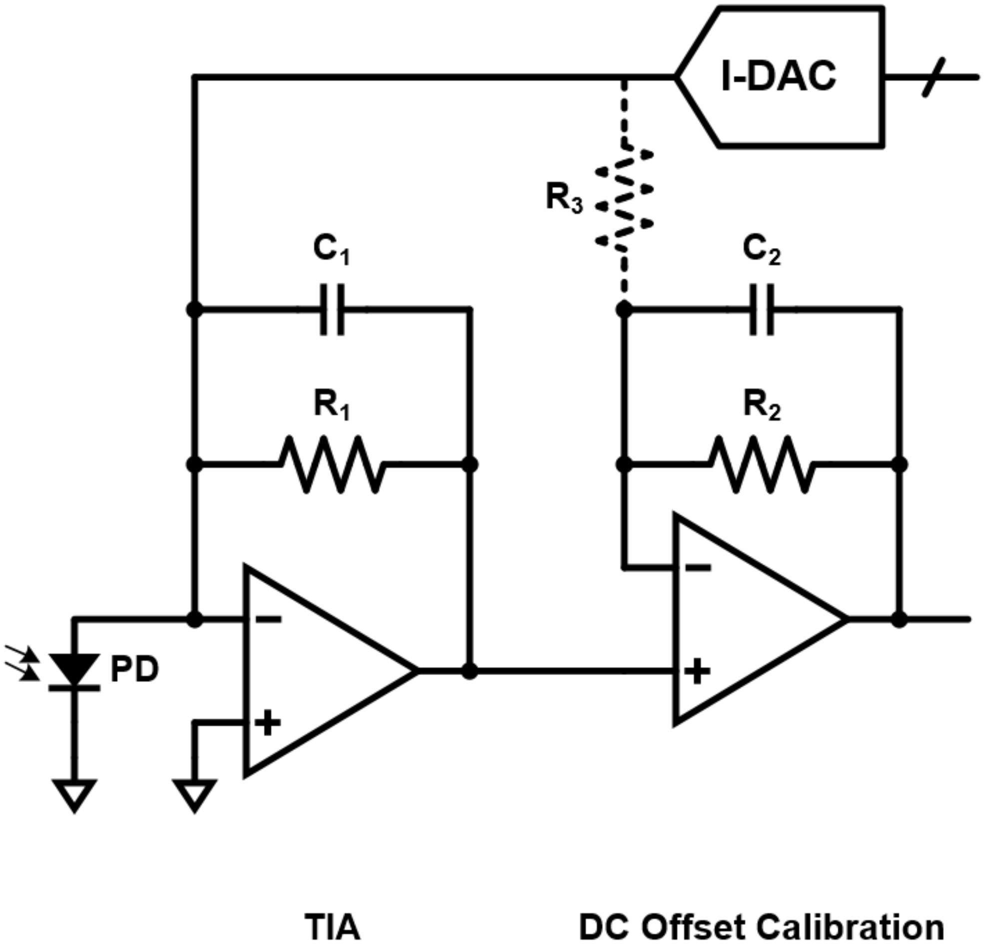


Fig. 2.2.4 Noise model of the single-ended TIA with PD.

offset in voltage form. The Fig. 2.2.5 shows the typical current-steering DAC. This type of current steering DAC is a new noise source. Since the DAC's current sources, bias circuit, switch, feedback resistor, and OPAMP noise are applied to the input without attenuation, the area and the consumption current of the DAC increase by the minimum TIA level in order to reduce it to an appropriate level. Even if the output of the DAC is

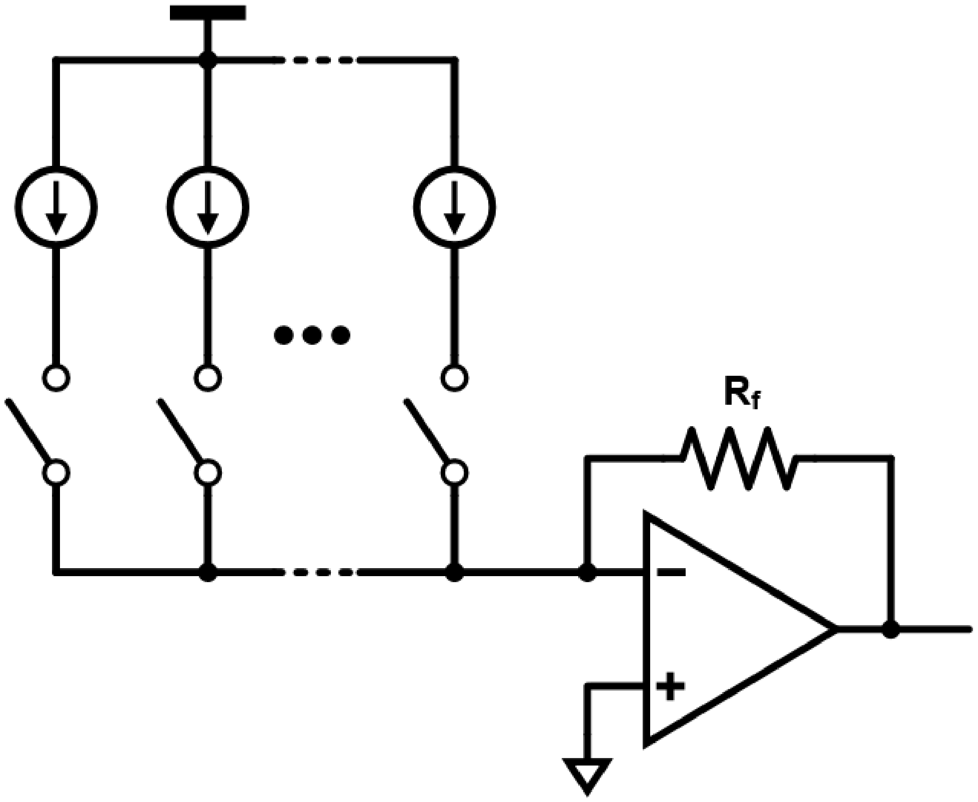


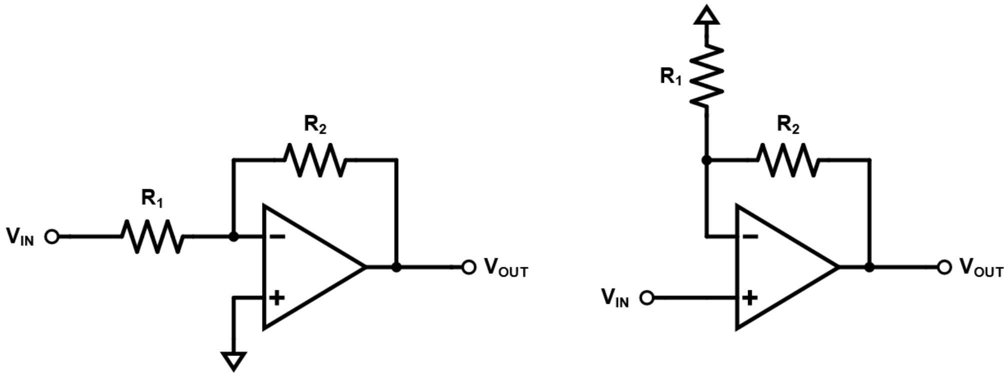
Fig. 2.2.5 Current-steering DAC example.

connected to the output of the DAC at the TIA output stage as shown in the dotted line in Fig. 2.2.4, the input-referred noise is reduced by the transimpedance of the TIA, but the additional thermal noise due to R3 and the intrinsic noise of the DAC are still ignored It is difficult level. In this paper, I propose DAC that can calibrate DC offset and minimize noise degradation even with low power consumption and area instead of conventional current-steering DAC.

2.2.3 GAIN AND FILTER STAGES

Even after the DC offset is removed from the converted signal in the TIA, the signal is still very small and additional gain is required. This reduces the design specification of the ADC because it has the effect of reducing the quantization noise voltage or intrinsic noise voltage of the subsequent ADC by a gain. The amplifiers used in the gain stages can be implemented in two architectures: an inverting amplifier as shown in Fig. 2.2.6 (a) and a non-inverting amplifier as shown in Fig. 2.2.6 (b). When the open-loop DC gain of the OPAMP is sufficiently large, each gain is expressed as:

$$G_{INV} = \frac{V_{OUT}}{V_{IN}} = \frac{R_2}{R_1}, G_{NONINV} = \left(1 + \frac{R_2}{R_1 + R_2}\right) \qquad (2.2.6)$$



(a) (b)

Fig. 2.2.6 (a) Inverting amplifier (b) Non-inverting amplifier.

It is usually possible to implement a LPF function by adding a feedback capacitor when increasing the gain using an active device. Fig. 2.2.6 is a general circuit diagram cascading passive RC HPFs, active non-inverting amplifiers with LPFs. At this time, the total gain, cutoff frequency f_c of HPF and LPF are calculated as follows:

$$G_{tot} = \left(1 + \frac{R_3}{R_2 + R_3}\right)\left(1 + \frac{R_6}{R_5 + R_6}\right) \qquad (2.2.7)$$

$$f_{c,HPF1} = \frac{1}{2\pi R_1 C_1}, f_{c,HPF2} = \frac{1}{2\pi R_4 C_3} \qquad (2.2.8)$$

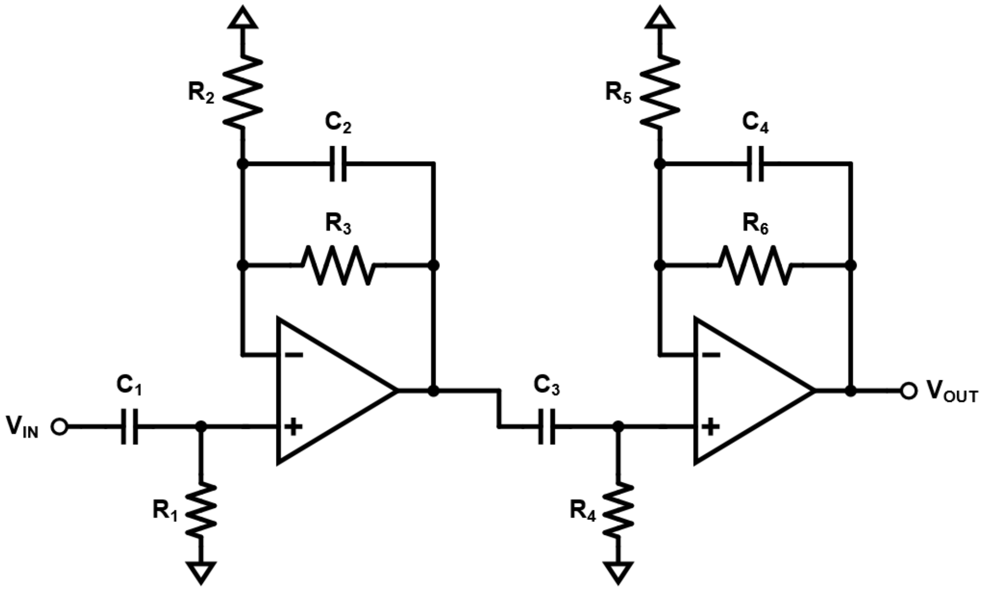


Fig. 2.2.7 Cascaded gain and filter stages.

$$f_{c,LPF1} = \frac{1}{2\pi R_3 C_2}, f_{c,LPF2} = \frac{1}{2\pi R_6 C_4} \qquad (2.2.9)$$

2.2.4 ANALOG-TO-DIGITAL CONVERTER

We use a pipelined architecture to digitize the amplified analog signals. Fig. 2.2.8 shows a block diagram of a typical pipelined ADC. The input signal V_{IN} is sampled first in the sample-and-hold (S/H) circuit inside each stage. Then an n-bit analog-to-digital

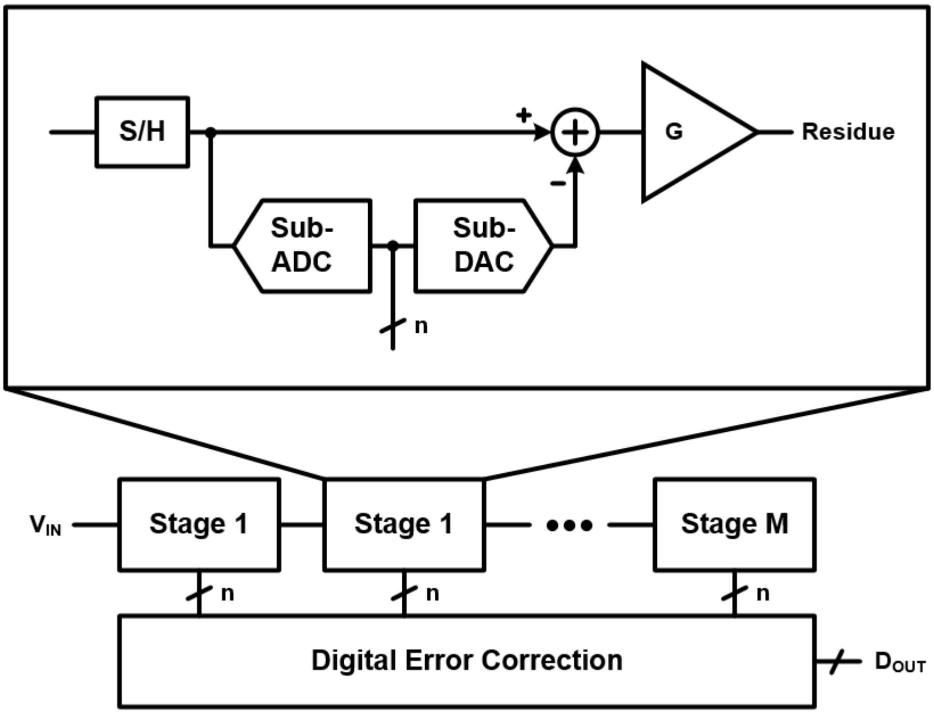
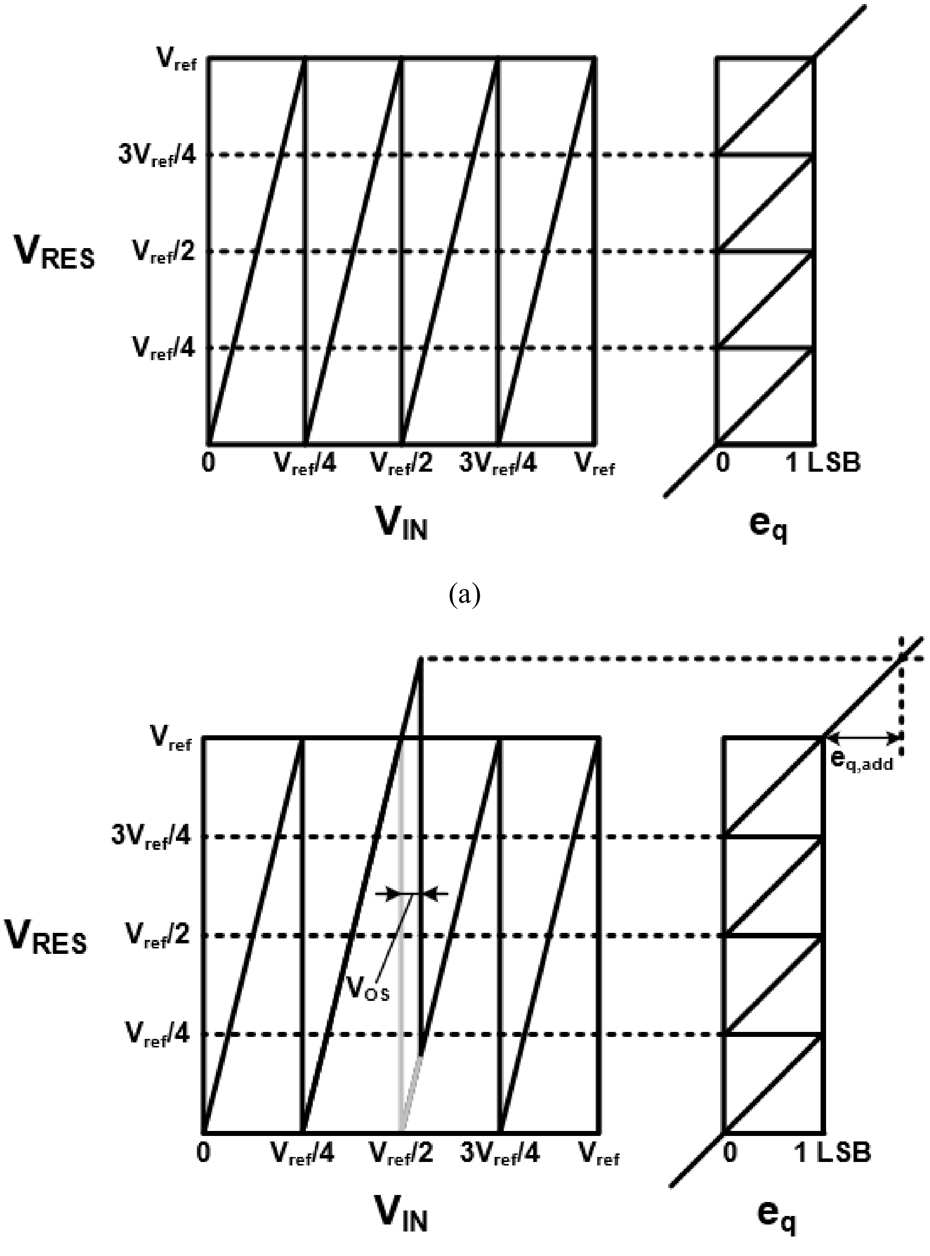


Fig. 2.2.8 Cascaded gain and filter stages.

conversion is performed on a simple form of sub-ADC such as a flash ADC. This n-bit digital output signal is transferred to the digital correction logic, and at the same time, it is converted back to the analog value in the sub-DAC implemented by the normal capacitor DAC. When the analog signal is subtracted from the DAC in the original input signal, a residue signal is generated. When $G = 2^n$, the maximum input range of each stage is set to the maximum input range of the original signal.

Fig. 2.2.9 (a) shows the residue waveform of the stage using the ideal 2-bit sub-ADC and the ideal 2-bit sub DAC. And the quantization error at this time does not exceed maximum 1 LSB. However, if an error such as offset exists in the threshold voltage of the sub-ADC, the residue may deviate from V_{ref} as shown in Fig. 2.2.9 (b). At this time, since the input of the next stage ADC is out of the maximum input range, the quantization error of the next stage A / D conversion result is more than 1 LSB, which is expressed as missing code.

To solve this problem, there is a method of giving redundancy to the sub-ADC. The simplest method is to give a gain less than 2^n when the bit of the sub-ADC is n. This ensures that V_{RES} does not deviate from 0 and V_{ref} even if an offset exists in the sub-ADC. For example, if the gain is 3.5, the effective resolution of the stage is log2 (3.5) = 1.8 bits. Another way is to reduce the effective resolution by lowering the quantization level of the sub-ADCs and sub-DACs while using an integer number of gains. Fig. 2.2.10 shows the 1.5-bit per stage residue waveform [2.2.4].



(a)

(b)

Fig. 2.2.9 Residue waveform of the 2-bit per stage and quantization error (a) without offset in sub-ADC (b) with offset in sub-ADC.

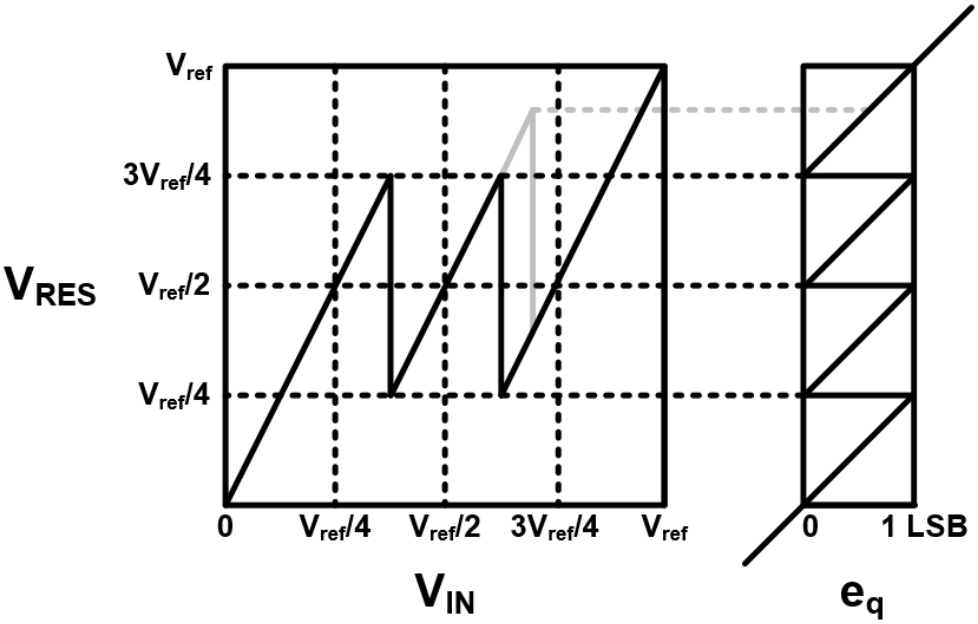


Fig. 2.2.10 Residue waveform of the 1.5-bit per stage.

A pipelined ADC has two phases of operation. One is the sampling phase and the other is the amplification phase. However, OPAMP is actually used only in the amplification phase and not in the sampling phase. Therefore, it is not good for power efficiency to flow current to the OPAMP in the sampling phase. In this study, I used a method to reduce the consumption current of pipelined ADC by sharing OPAMP between stages [2.2.5].

2.2.5 AVERAGE POWER CONTROL

The intensity of the LD varies with the change of temperature, ambient light, and supply power. The output of the ROIC drifts even if the ROIC has a good noise performance when the intensity of the LD varies. To compensate for this, the average power control (APC) circuit is used as shown in Fig. 2.2.11. The basic operation principle as follows. The monitor PD receives the light from the LD, so that it generates a current $I_{MONITOR}$. The monitor PD and the LD are connected with optical fiber or encapsulated in a module, so that particles and moisture cannot affect the current of the monitor PD. This

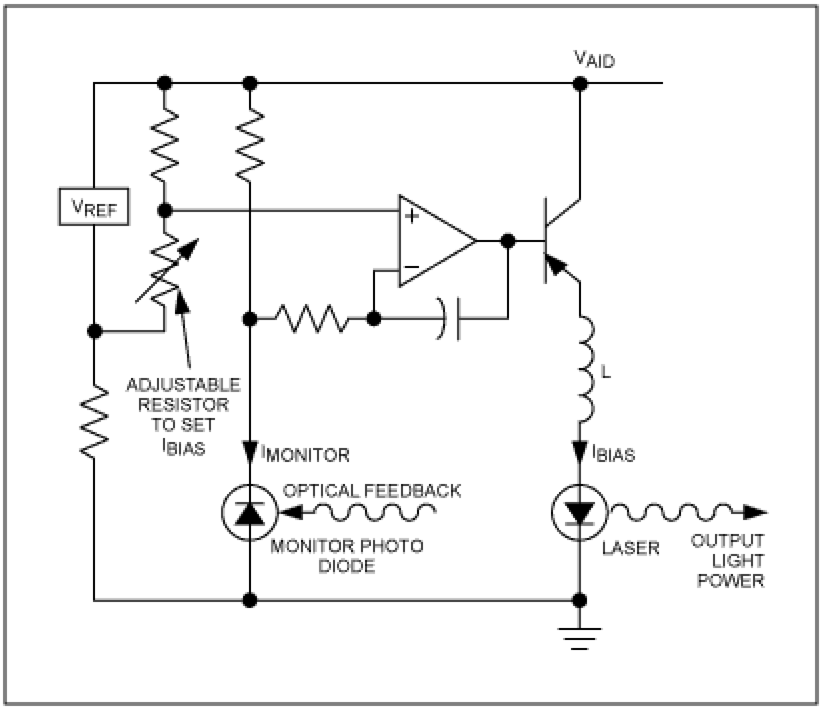


Fig. 2.2.11 APC circuit for LD power control [2.2.6].

current signal is converted into a voltage signal through a resistor and compared with a reference signal insensitive to changes in the external environment. As $I_{MONITOR}$ increases, OPAMP reduces the bias current I_{BIAS} and reduces the light intensity of the LD, and vice versa. The bias current is adaptively controlled in such a way that the light intensity of the LD becomes constant by the negative feedback loop. The average I_{BIAS} is determined by tuning adjustable resistor shown in Fig. 2.2.11, which is usually configured externally.

2.3 DIGITAL BACK-END LOGIC

Digital logic performs analog and digital circuit control functions and post-processing of digitized signals in the ADC. Specifically, I adjust the TIA bandwidth, programmable gain amplifier (PGA) bandwidth, filter cutoff frequency, and so on to obtain the best SNR performance. I also adjust the threshold for classifying the particle size, and the optimal number of average samples. The digital code for DC offset correction performed in the AFE stage is extracted by automatically calculating whether the output code falls within the tolerance range by sweeping the digital code in a particle-free environment. It also performs particle size (PM) size calculations, digital low-pass filtering, PM concentration curve fitting, temperature offset and gain compensation. The output interface supports universal asynchronous receiver/transmitter (UART), serial peripheral interface (SPI) and pulse width modulation (PWM).

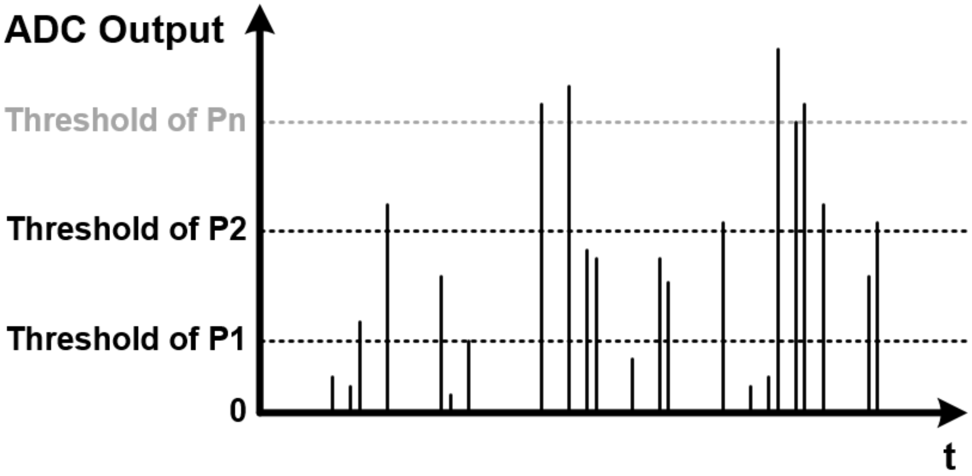
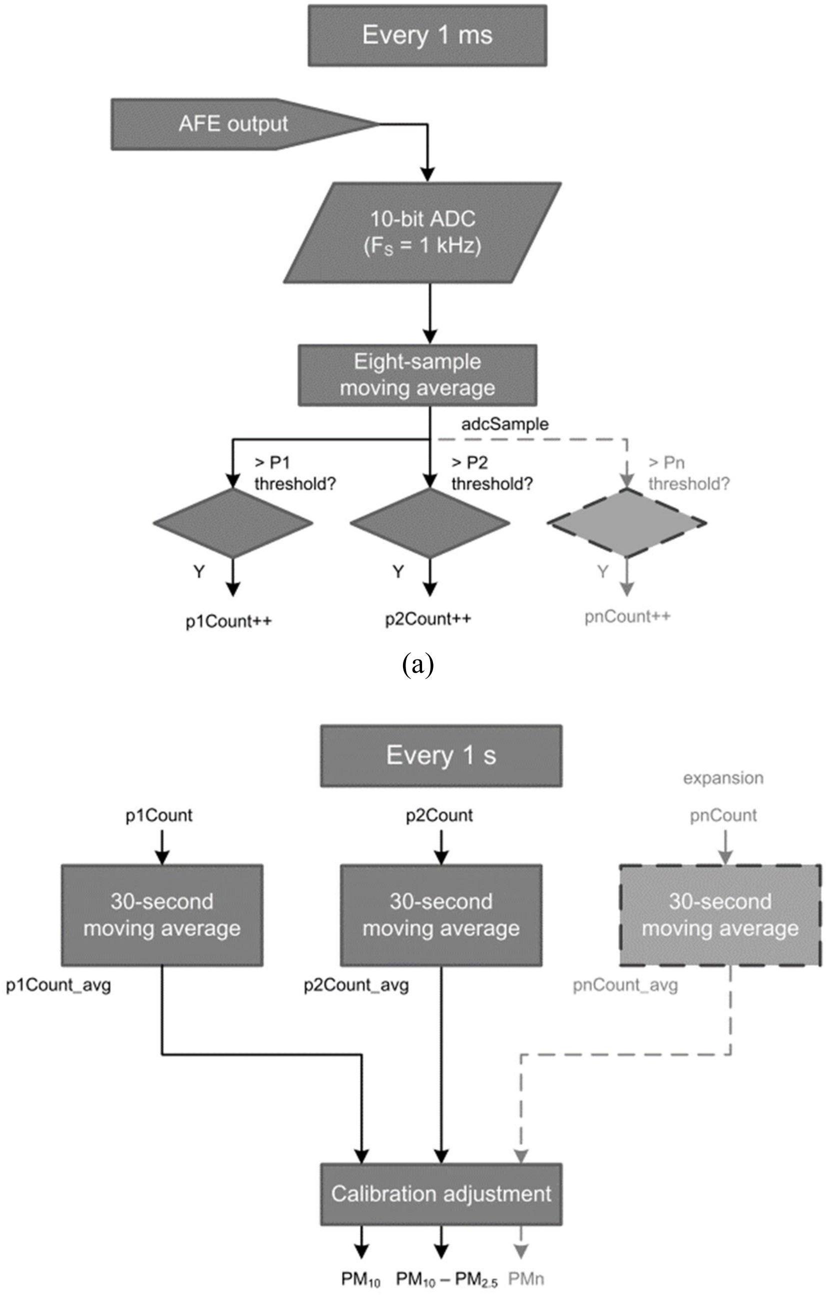


Fig. 2.3.1 ADC output sequence example with thresholds of PM size.

Since the size of a particle is related to the size of a signal, it can be determined by counting a particle exceeding a certain threshold as shown in Fig. 2.3.1. Figure 2.3.2 shows an example of the threshold-based particle size concentration calculation algorithm [2.3.1]. In the example, the moving average is calculated by 8 output values of the ADC outputted every 1 ms, and the high frequency noise is firstly removed. Basically, the larger the particle size, the larger the output voltage. Therefore, it is a principle to set the threshold level that can distinguish the size of the particles and then to calculate the concentration according to the particle size if counting by intervals. Then, every second, the particle size is measured again at intervals of 30 seconds and the moving average is taken again and the final data is output.



(a)

(b)

Fig. 2.3.2 Sample software algorithm for particle concentration estimation [2.3.1].

CHAPTER 3

CIRCUIT IMPLEMENTATION OF THE PROPOSED OPTICAL PARTICULATE MATTER DETECTOR

3.1 SENSOR BLOCK DIAGRAM

Fig. 3.1.1 shows the structure of the proposed PM detector using LD as a light source. This detector is divided into LD, PD, reference PD (PD_{REF}), and ROIC inside chip. The main signal path of the ROIC is through an AFE consisting of TIA, DC offset calibration circuit, DAC, gain and filter stages and on-chip temperature sensor, an ADC. In addition, there is a power management unit (PMU) such as APC, UVLO, BGR, LDO, other circuits such as one-time programmable (OTP) memory and OSC. There is another proposed PM detector using LED as a light source and it does not include several sub-blocks such as APC, on-chip temperature sensor shown in in Fig. 3.1.2. The LED PM detector has external LED driver of which turn-on and turn-off are controlled by digital logic in ROIC. Its AFE uses external 5 V power as a power without regulation unlike the LD PM detector.

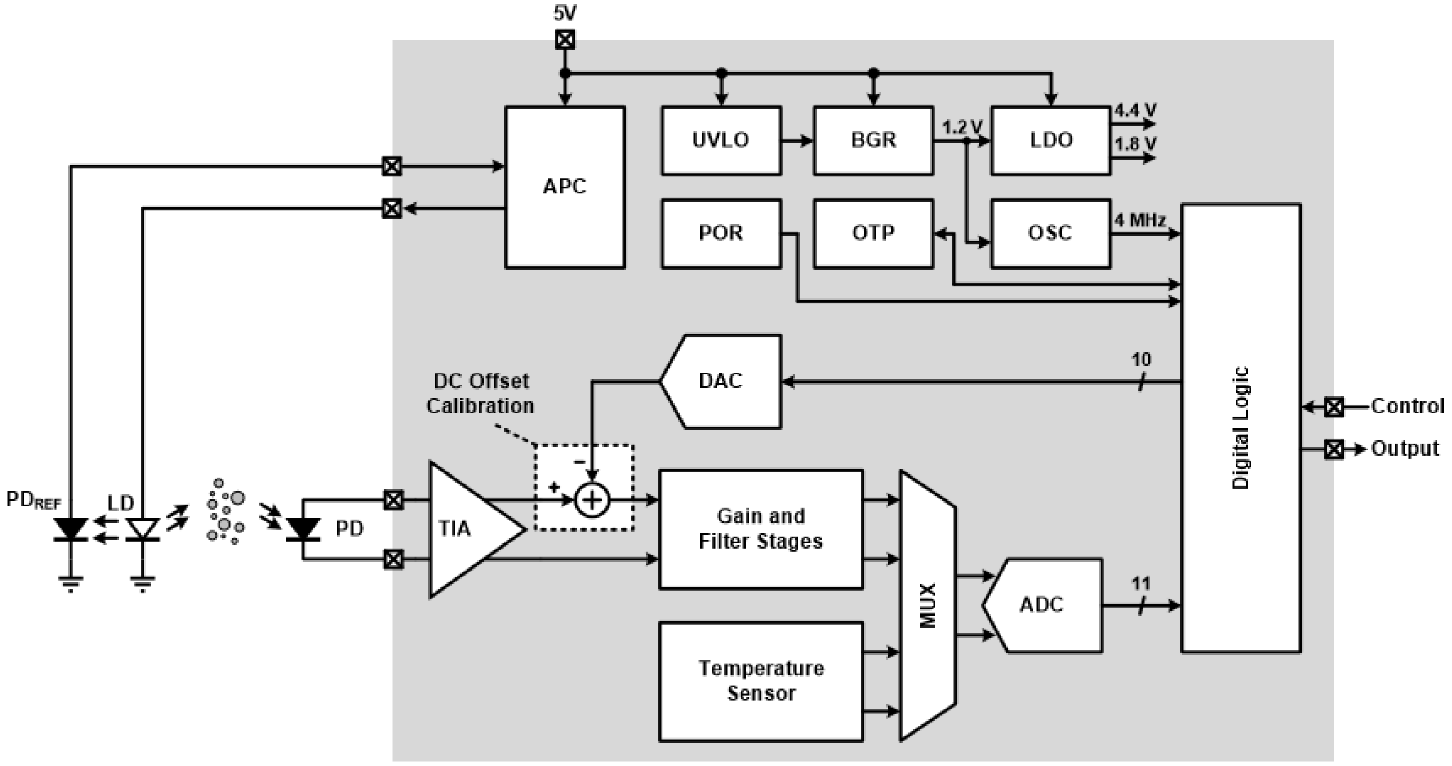


Fig. 3.1.1 Sensor block diagram of the proposed PM detector using LD.

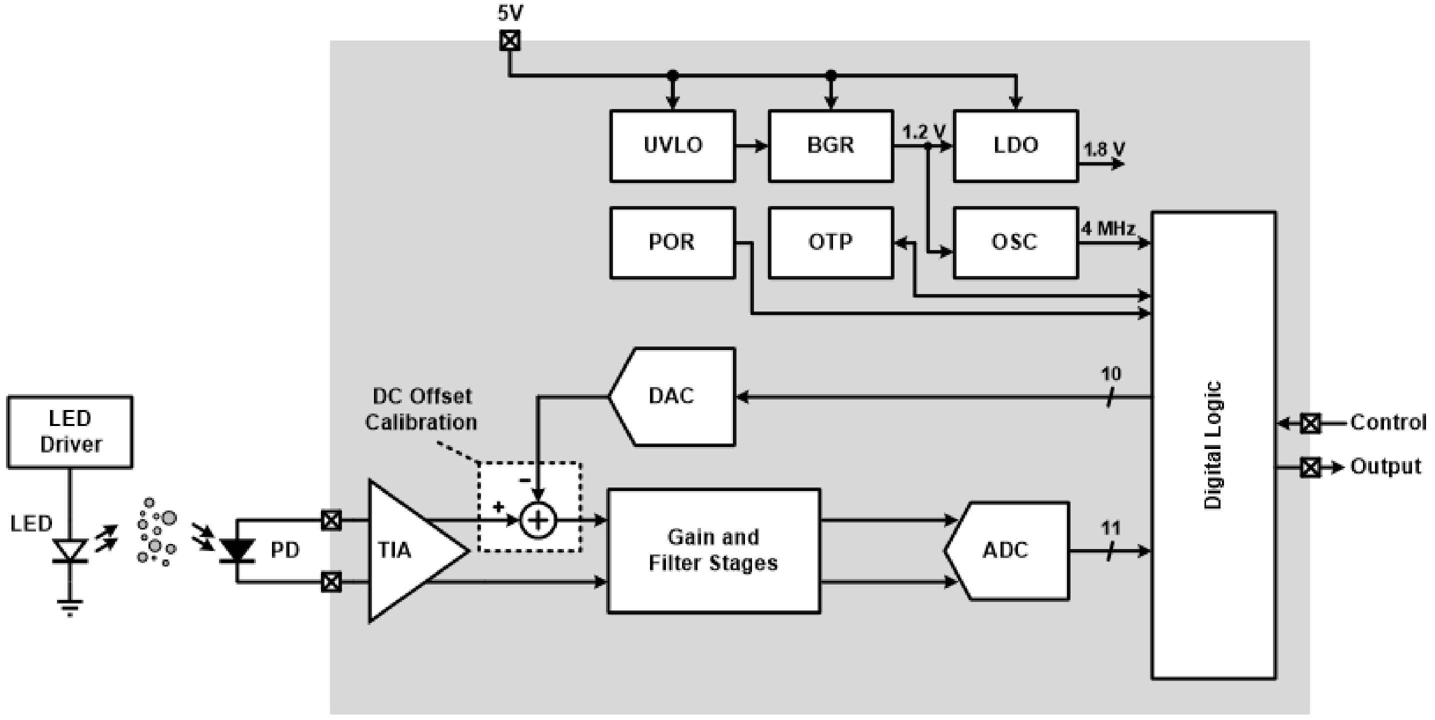


Fig. 3.1.2 Sensor block diagram of the proposed PM detector using LED.

Since the block diagrams of proposed PM detector using LD and LED are similar and all blocks designed for the LD PM detector are included, the rest of this chapter will be described with the LD PM detector if there is a special mention. The light emitted from the LD is gathered at one point through a lens, and the amount of scattering depends on the size and concentration of the particles passing through this point. Meanwhile, the intensity of light irradiated from the LD can be changed depending on external environmental changes such as the noise of the external power supply or the drift of the temperature. To get the accurate results of PM concentration, the sensitivity of the PM detector should be reduced against the external environments. The APC circuit plays this role by controlling the bias current that flows through the LD by monitoring the current generated at the PD_{REF} outside the chip. It maintains the light intensity of the LD constant against external environment changes by decreases the bias current when the intensity of light increases and vice versa.

The timing diagram of the proposed PM detector at a low-power mode is shown as Fig. 3.1.3. The light source can be periodically turned on and off to increase its lifetime and reduce power consumption, which is referred to as the low-power mode. In the low-power mode, the operating time interval is basically 10 ms, but this may be changed depending on the application. The gray-colored waveform represents that the distorted results when the DC offset included in the input signal is not eliminated. It shows that the output signal of PGA2 is clipped to the supply voltage. This problem will be discussed in Chap. 3.2.1.

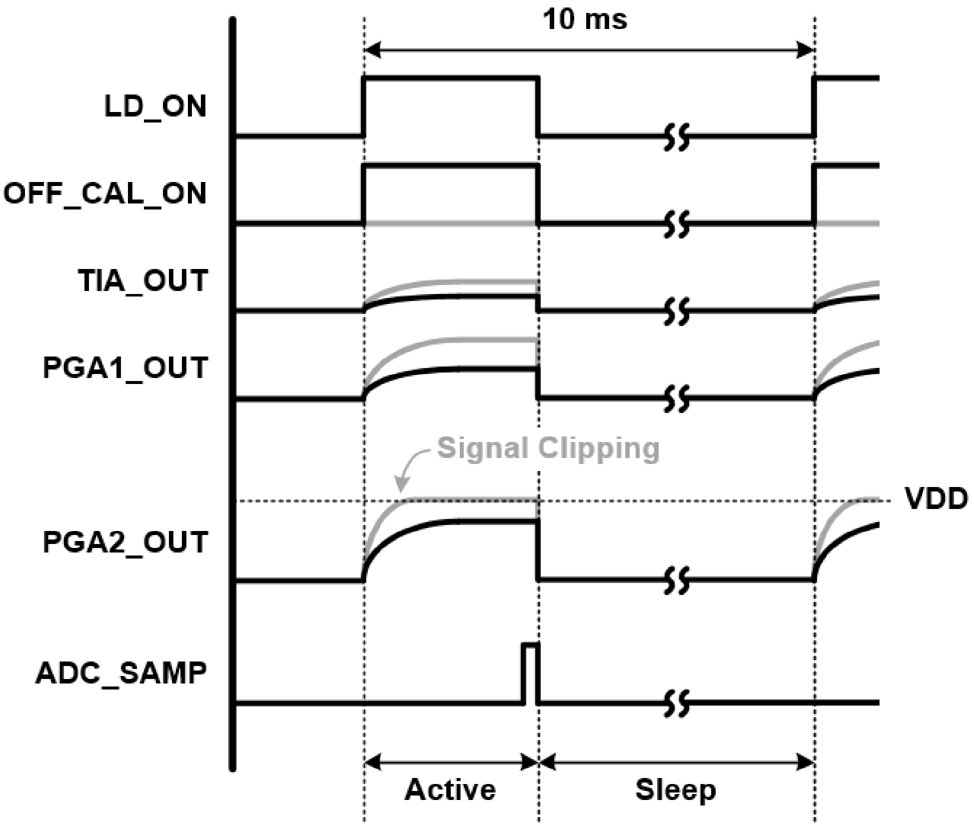


Fig. 3.1.3 Timing diagram of the proposed PM detector at the low-power mode.

The scattered light generates a current in the PD of which output is connected to the ROIC. This current signal is applied to the differential input of the TIA inside the ROIC and converted to a voltage signal. The ROIC is robust to supply noise because the differential input signal is processed by fully-differential AFE and ADC until it is digitized. The intensity of the light is maintained constant by the APC circuit, but the temperature-dependent characteristic of the PD is another factor that degrades the accuracy of the PM detector. To compensate for this, an on-chip temperature sensor is periodically read the temperature using the ADC that is used for PM detection. In the digital post-processing, temperature-dependent offset is applied to the output codes using this temperature information. As a result, the sensitivity to the temperature variation is reduced. The on-chip temperature sensor uses the principle of temperature-dependent characteristics of the bipolar junction transistors (BJTs). ΔV_{BE}, which is the V_{BE} difference between the two BJTs can be obtained if the currents flowing through BJTs of different sizes. It has a proportional to absolute temperature (PTAT) characteristic. By amplifying the ΔV_{BE} and digitizing it, the information of the temperature can be acquired.

The signal transformed by the TIA contains the DC offsets generated by LD, PD, and TIA that are irrelevant to the actual particle information. Since the DC offset is basically very large compared to the input signal the DR of the entire chip is degraded if it is not removed before the signal amplification. In this paper, I propose an OPAMP with the integrated DAC by using an asymmetric digitally-controlled input stage. It relieves the large area and large power consumption problems of typical current-steering DAC. By amplifying the signal of which the DC offset is removed, the full-utilization of the maximum input swing range of the back-end circuit is guaranteed. It is also beneficial that the input-referred noise of the back-end circuit is reduced. A HPF and LPFs at were added to reduce the low-frequency and high-frequency out-of-band noise included in the signal. This signal is digitized in an 11-b pipelined ADC. The ADC consists of a 1.5-b per stage sub-ADCs and uses a shared-opamp technique to reduce power consumption.

There are the other peripheral analog circuits. The UVLO circuit prevents abnormal operation of the ROIC by not providing a BGR start-up signal unless the supply voltage reaches a certain threshold level. The BGR and the LDO receive an external supply voltage of 5 V to generate an analog supply voltage of 4.4 V and a digital supply voltage of 1.8 V to internal circuits. The power-on reset (POR) outputs reset signals for the register to set the initial valuest when the supply voltage is applied. The initial values are stored in the register and OTP memory. The OTP memory helps to maintain the performance against chip mismatches caused by process variations.

Digital logic controls analog and digital circuit and performs the post-processing of digitized signals. Specifically, it adjusts the bandwidth of the TIA and the PGAs, the cutoff frequency of the filters, the bias currents of the AFE sub-blocks, and so on. To obtain the best SNR performance, the threshold for classifying the particle size, and the optimal number of average samples are adjusted in the digital logic. The digital code for the analog DC offset calibration in the AFE is extracted automatically by adjusting the output code within a tolerance range by sweeping the digital code in a particle-free environment. The digital logic also performs particle size calculations, digital low-pass filtering, concentration-based curve fitting, temperature-dependent offset compensation, and gain compensation. The output interface PWM, UART, and SPI.

3.2 ANALOG FRONT-END CIRCUIT

The AFE circuit implementation is shown in Fig. 3.2.1. It consists of TIA, DC offset calibration, two stages of PGAs, and HPF. All of these are implemented with full-differential circuitry to reduce performance degradation due to supply noise. The PD that has a structure of p-type, intrinsic, and n-type (PIN) is capable of receiving wavelengths from 400 nm to 1100 nm. The output current of the PD essentially is changed with the temperature change. The PD used in this research has a temperature coefficient of -0.1 %/K. For example, the input current is changed by 10 % at 100 K temperature change, so it is necessary to compensate the signal depending on the temperature. This is discussed in detail at the Chap. 3.2.2.

The differential light-induced current signal generated in the PD is converted to a voltage signal through the feedback resistors R_{1A} and R_{1B} of the TIA which have the same resistance R_1. The feedback capacitors C_{1A} and C_{1B} which have the same capacitance C_1 form LPF with combination of R_{1A} and R_{1B}, where the 3 dB cutoff frequency is $1/(2\pi R_1 C_1)$. The noise due to the feedback resistance is determined as follows:

$$\mathrm{V}^2_{onoise,RMS,R1,R1} = 4kTR_1 \times \frac{1}{R_1C_1} = \frac{4kT}{C_1} \qquad (2.3.1)$$

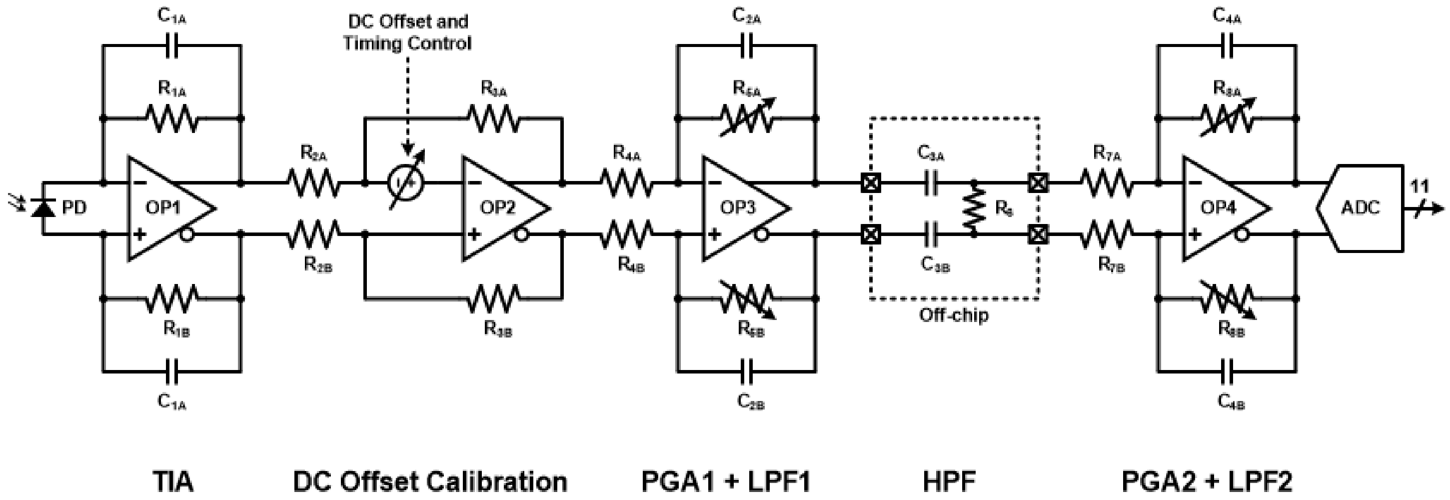


Fig. 3.2.1 Circuit implementation of the AFE.

As shown in Eq. (2.3.1), it is advantageous to increase the output voltage by increasing the resistance to reduce the input-referred noise of the back-end circuit since the thermal noise of the feedback resistor is determined only by the feedback capacitor. However, the optimal 3 dB cutoff frequency f_c of the TIA to filter out the input signal noise should be determined first. With the constant fc, the increase of the feedback resistance makes the feedback capacitance decrease. It means that the change of the feedback resistance does not affect the SNR performance. In this circuit, $f_{c,TIA}$ is 4 kHz using 5 MΩ for R_1 and 8 pF for C_1. It can be tuned from 2.7 kHz to 27 kHz, and the transimpedance can be varied from 30 kV/A to 5 MV/A.

Both PGAs which also are LPFs with a feedback resistor and a feedback capacitor are implemented with a non-inverting amplifier structure. The gain of the PGA is different for the PM detector using LED or LD, 50 for LED and 25 for LD in this design. The tuning range of the PGA gain is from 25 to 86. The f_c of the PGAs is designed to be 4 kHz like the TIA and the tuning range is also the same from 2.7 kHz to 27 kHz. Since the f_c of the target HPF is very low at 0.5 Hz, the RC value must be very large. To reduce the chip area, we used external components that are $R_6 = 300$ kΩ and $C_3 = 1$ μF for the HPF.

The supply voltage of the AFE is 4.4 V that is regulated by LDO regulator for the PM detector using LD, whereas 5.0 V that is applied from external power source for the PM detector using LED.

3.2.1 DC OFFSET CALIBRATION CIRCUIT

In the waveform of Fig. 3.2.2, the black-colored line is the waveform when the DC offset calibration is enabled, whereas the gray-colored line is the waveform when it is disabled. Because of the DC offset, the signal is clipped after amplification. To prevent the signal from being clipped, the gain of the PGA should be small which results in SNR degradation. Or, DR should be smaller to maintain the gain of the PGA. Either ways are not better than DC offset calibration method. As a result, the more accurate the DC offset is removed, the better the PM detector can have higher DR and higher SNR.

Fig. 3.2.3 shows the waveform when the DC offset calibration is always active, not just when the light source is turned on. The both waveforms when the DC offset is not removed and when the DC offset calibration is always active show the same waveforms except for the DC level from the output of the DC offset calibration block to the output of the PGA1. However, since the HPF removes the DC component, the two outputs of the HPF become identical in both cases. Finally, after having the gain of PGA2, the signal clipping occurs again. In other words, if the DC offset calibration is always active, not just when the light source is turned on, the same problem occurs as when the DC offset is not removed. Therefore, as proposed in this paper, the DC offset calibration timing should be synchronoized with the light source turn on and off timing.

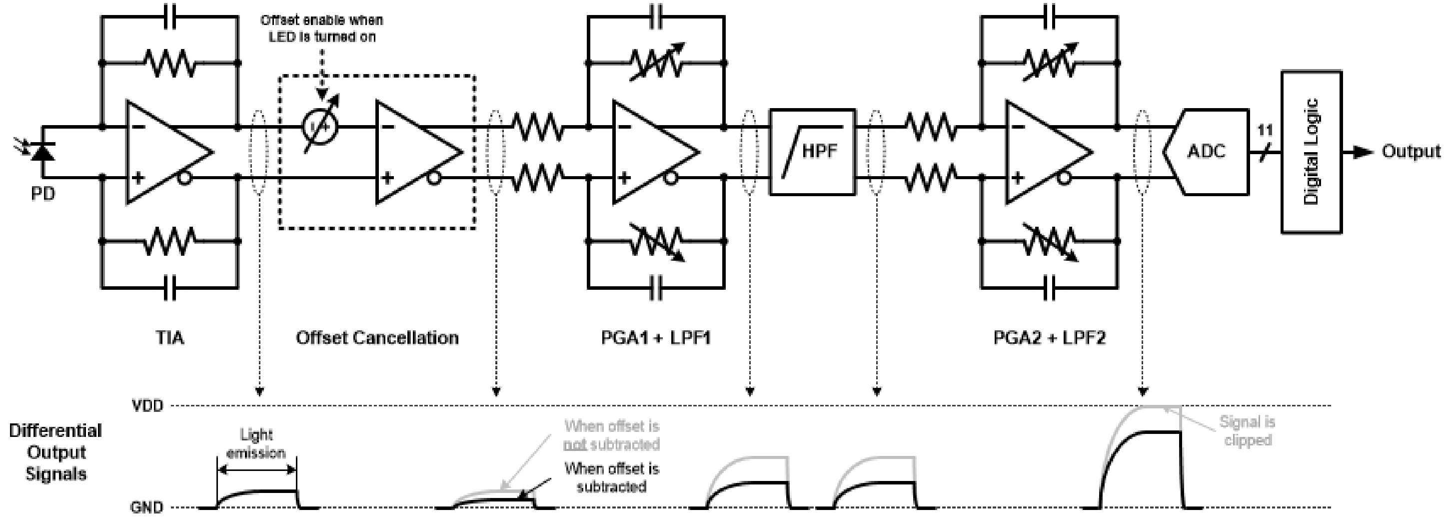


Fig. 3.2.2 Circuit implementation of the AFE.

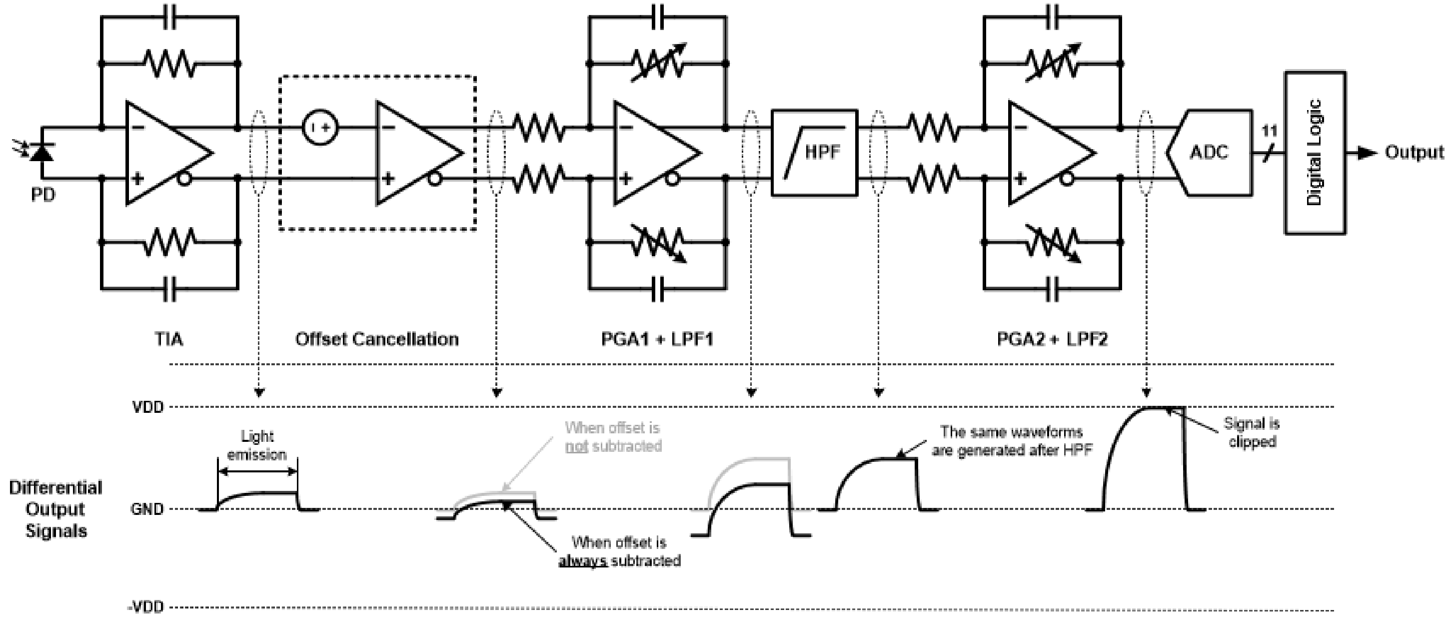


Fig. 3.2.3 Circuit implementation of the AFE.

Fig. 3.2.4 depicts the schematic of the proposed DC offset calibration. Additional input transistors connected in parallel to the positive input transistor produces the DC offset with the opposite sign from the LD offset. The additional transistors are binary-scaled and controlled by a 10-b digital code covering the LD offset of about 70 mV at the input of the DC offset calibration block. Compared to traditional methods that use current-steering DAC, this approach achieves a low-power, low-noise, and small-area. It also does not sacrifice the input DR compared to the digital-only offset calibration.

Voltage step uniformity and monotonicity are not critical in this DC offset calibration circuit. Offset error greater than 68 μV, which is a voltage step, will be compensated in the digital post-processing. Even if monotonicity is not guaranteed, this is not a problem because the digital offset correction algorithm sweeps the digital codes and finds the appropriate digital code that produces an output error below a predetermined tolerance. The location of the input transistors can be either the negative input or the positive input of the OPAMP depending on the DC offset direction, that is the polarity of the PD. Because the polarity of the PD is determined in advance, we can determine where to insert the DAC. The output stage of the OPAMP is class-AB to cover large output swing.

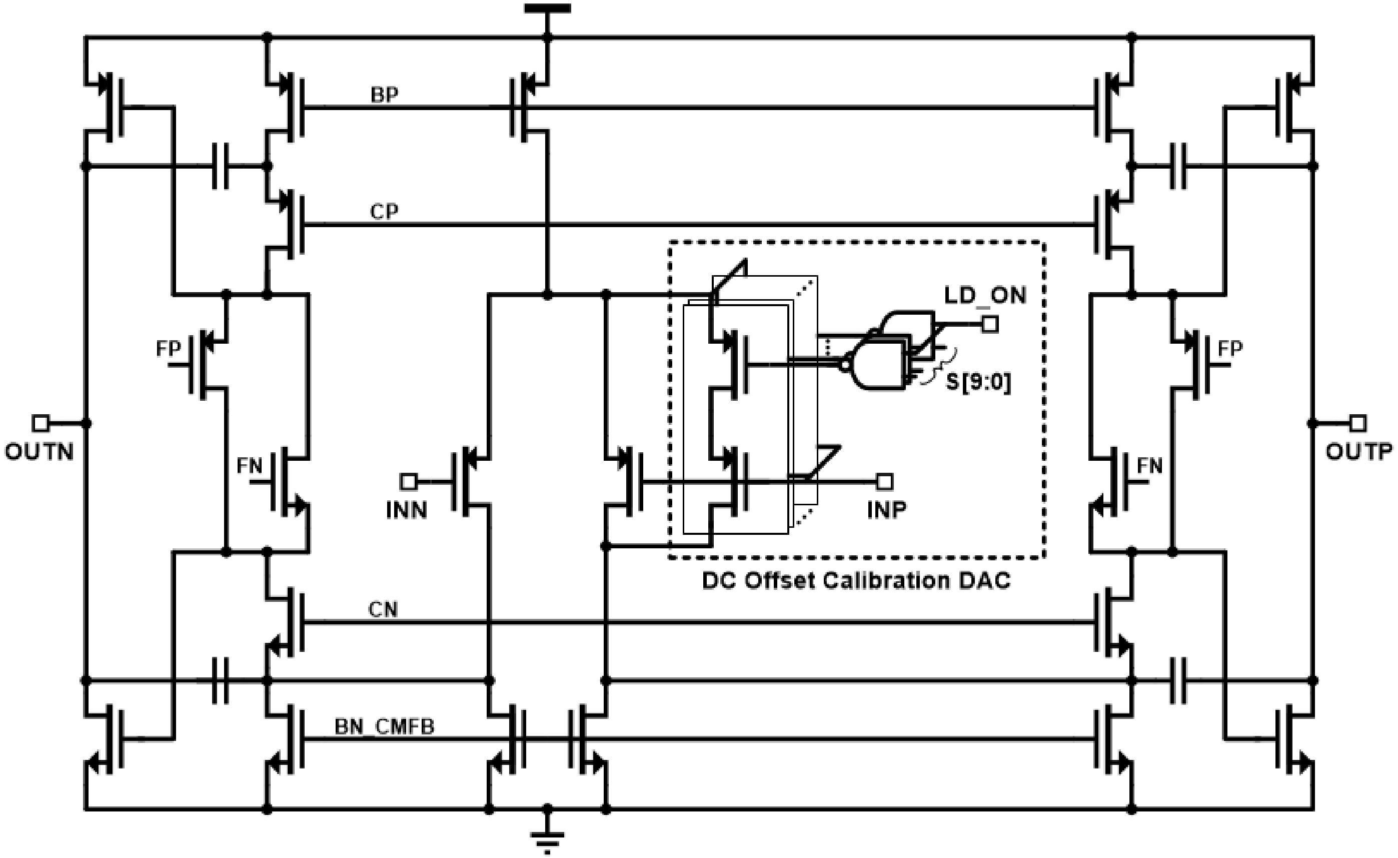


Fig. 3.2.4 Proposed OPAMP with integrated DAC in the DC offset calibration circuit.

3.2.2 ON-CHIP TEMPERATURE SENSOR CIRCUIT

The base-emitter junction current of a BJT according to the temperature change is followed by the next equation [3.2.1]:

$$V_{BE} = V_{G0}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{T}{T_0}\right) + \left(\frac{\gamma kT}{q}\right)\ln\left(\frac{T_0}{T}\right) + \left(\frac{kT}{q}\right)\ln\left(\frac{J_C}{J_{C0}}\right) \quad (3.2.1)$$

Where T is an absolute temperature, T_0 is a reference temperature, V_{G0} is a bandgap voltage of silicon which is normally 1.205 V, V_{BE0} is a junction voltage at temperature T_0 and current I_{C0}, k is a Boltzmann's constant, q is a charge on an electron, γ is a process-dependent temperature coefficient, J_C is a collector current density. If I derive the temperature coefficient of the V_{BE} and that at $T=T_0$,

$$\frac{\partial V_{BE}}{\partial T} = \frac{\partial V_{G0}}{\partial T}\left(1 - \frac{T}{T_0}\right) + V_{BE0}\left(\frac{1}{T_0}\right) + \left(\frac{\gamma kT}{q}\right)\frac{\partial \ln\left(\frac{T_0}{T}\right)}{\partial T} + \left(\frac{kT}{q}\right)\frac{\partial \ln\left(\frac{J_C}{J_{C0}}\right)}{\partial T} + \frac{k}{q}\left(\frac{J_C}{J_{C0}}\right)$$

(3.2.2)

$$\left.\frac{\partial V_{BE}}{\partial T}\right|_{T=T_0} = \frac{V_{BE} - V_{G0}}{T_0} + (\alpha - \gamma)\left(\frac{k}{q}\right) \quad (3.2.3)$$

Where α is another temperature coefficient that has the relationship of $J_C \propto T^{\alpha}$. Eq.

(3.2.3) is normally negative value, which means that the V_{BE} has a complementary to absolute temperature (CTAT) characteristics. However, it's not suitable to use a signal of the temperature sensor since V_{BE} is a non-linear function of temperature. And the temperature coefficient of the V_{BE} is very sensitive to the process variations.

By subtracting two V_{BE} equations of two BJTs, I can derive the following equation:

$$\Delta V_{BE} = V_{BE2} - V_{BE1} = \frac{kT}{q}\ln\left(\frac{J_{C2}}{J_{C1}}\right) = \frac{kT}{q}\ln\left(\frac{I_{C2}}{I_{C1}}\right) \qquad (3.2.4)$$

As you can see from the Eq. (3.2.4), the process-dependent terms are eliminated. And the difference between the two V_{BE}s, ΔV_{BE} shows a PTAT characteristics.

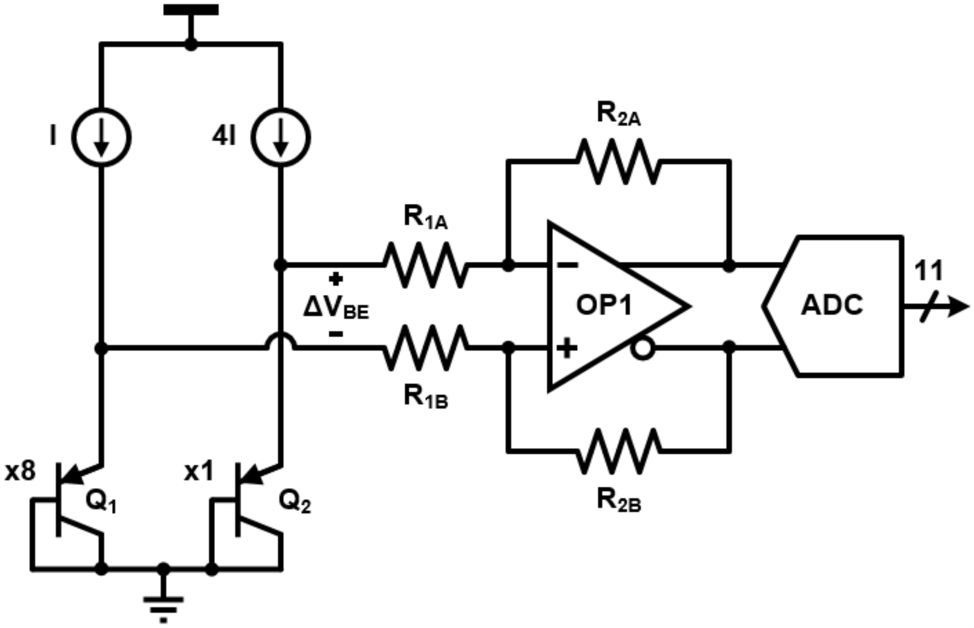


Fig. 3.2.5 On-chip temperature sensor circuit.

Fig. 3.2.6 shows the on-chip temperature sensor schematic. The ΔV_{BE} between Q_1 and Q_2 is used a signal that represents the temperature information. It is amplified by the inverting amplifier that consists of OP1, R_{1A}, R_{1B}, R_{2A}, and R_{2B}, which has a gain of R_2/R_1. The amplified signal is then converted to digital outputs by the 11-b pipelined ADC which is shared in the main signal path that measures PM concentration. The output signal of the inverting amplifier is designed to be less than the maximum input range of the ADC so that the resolution of the temperature sensor is about 0.5 °C, to match the required compensation resolution of the system. By increasing the gain of the inverting amplifier, it is possible to detect the temperature change more precisely, but because of this additional power consumption is required, the gain is optimized for the digital compensation step. The operating range of the temperature sensor is -40 °C to 90 °C.

3.3 DIGITAL BACK-END LOGIC

The basic digital post-processing procedure is shown in Fig. 3.3.1. First, the concentration of PM_1, $PM_{2.5}$, and PM_{10} are obtained using the ADC output data. And alleviates instantaneous changes in dust through the LPF. This output is not linear depending on the particle concentration due to the characteristics of the LD, and the output value is lowered at low concentration. Therefore, curve fitting is performed to linearize this. Then, correction is made by giving different offsets according to the temperature interval with respect to the temperature change, and the maximum output value between the chips is finally adjusted through gain correction. The result is output to the outside of the chip in the form of PWM, UART, SPI, and so on.

The LPF is designed as a primary IIR filter with a fc of 85 mHz. The transfer function of LPF is as follows:

$$H(z) = \frac{0.0234 + 0.0234z^{-1}}{1 - 0.953z^{-1}} \tag{3.3.1}$$

The flow chart for obtaining the PM size and concentration is shown in Fig. 3.3.2. The data output from the ADC is compared with a threshold corresponding to PM_1, $PM_{2.5}$, and PM_{10}. Then, the data is stored in PM_1, $PM_{2.5}$ and PM_{10} registers by counting the input smaller than the threshold. It is LPF once and outputs it to the output. The threshold level is designed to be externally adjustable.

Fig. 3.3.3 (a) shows the curve fitting form of the concentration output. The curve

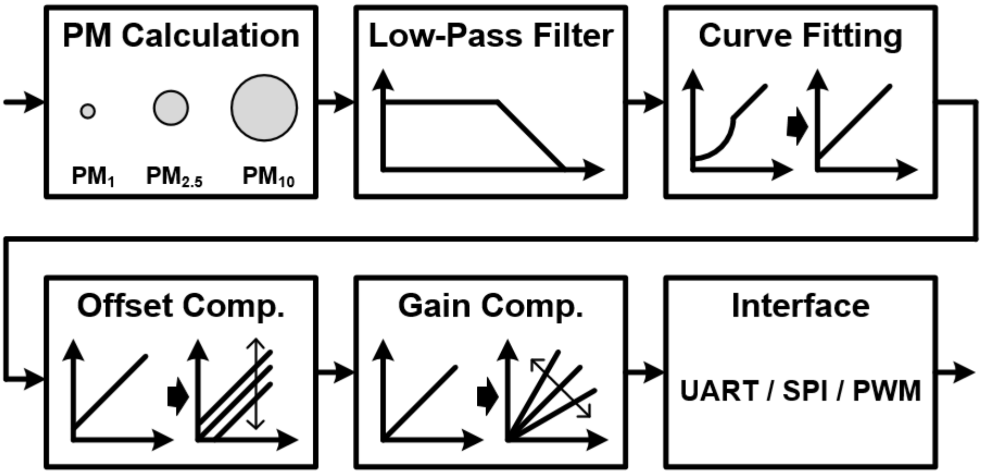


Fig. 3.3.1 Digital post-processing.

fitting is designed to calculate the offset value for one center point by interpolating the remaining offset value within the set interval to minimize the memory usage. In practice, the values set externally are Min., Max. There are four offset values at the center point and the center point, and five bits that determine the interpolation polarity. Fig. 3.3.3 (b) is an offset graph that can give different offset according to the temperature interval. In fact, the external setting values are $T_{TH,\ LOW}$, $T_{TH,\ High}$, slopes of the low and high temperature regions, and polarities of the slopes.

The output method supports PWM, UART and SPI. The PWM output has a 10 ms period and is capable of asynchronous operation with the ADC sampling rate. The periodic UART interface is divided into byte communication and packet communication. Byte

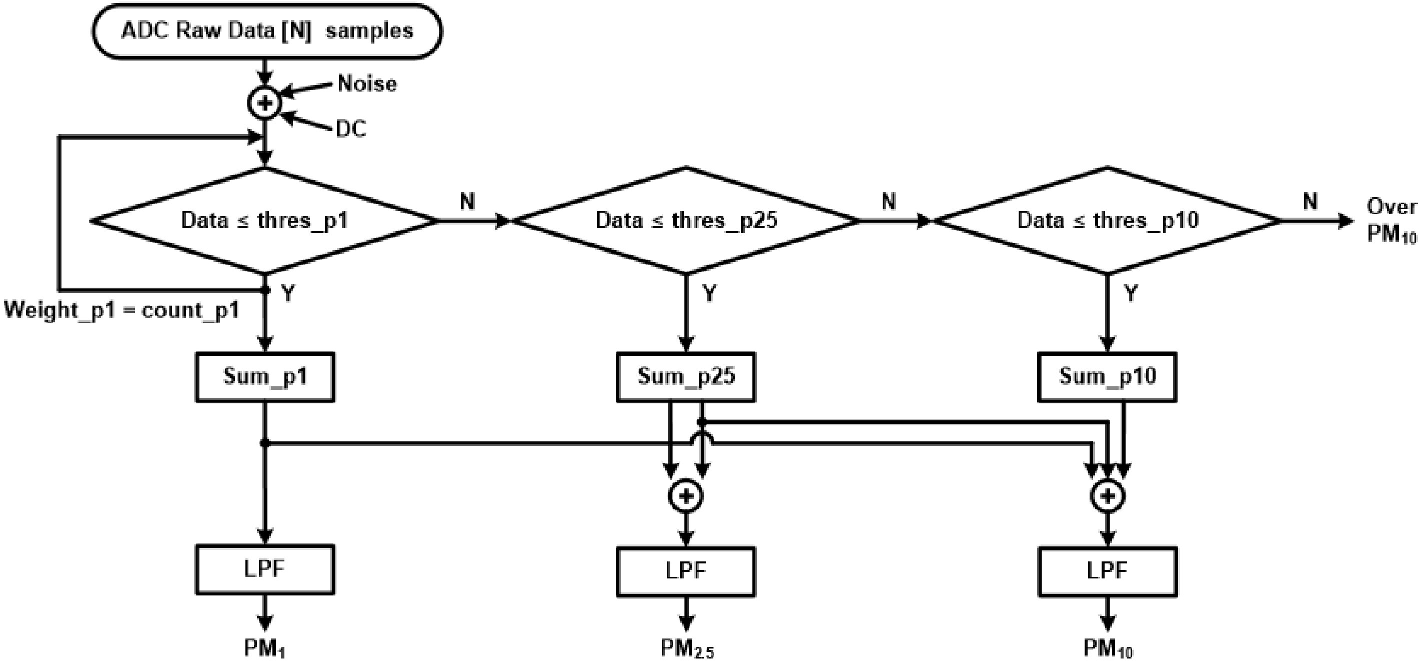
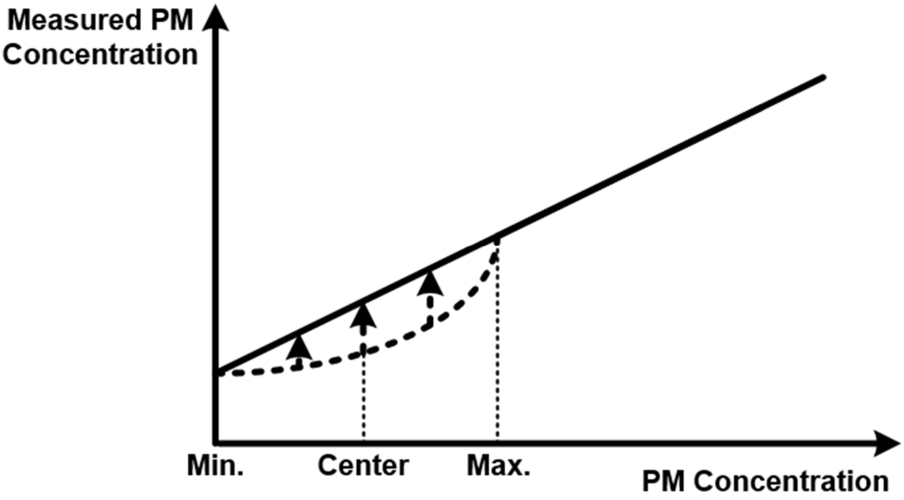
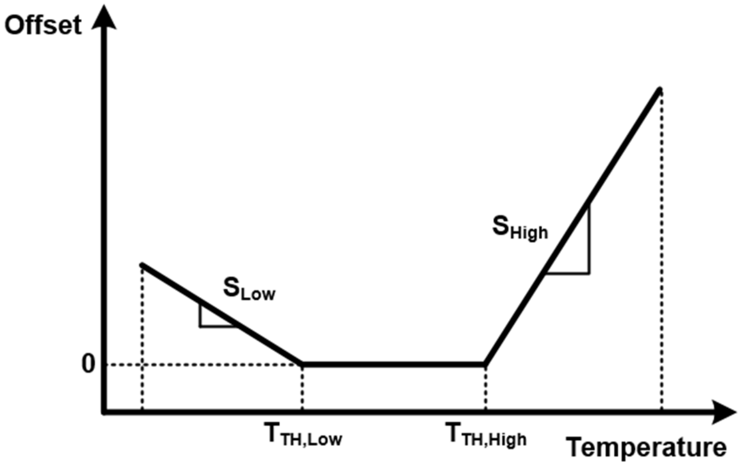


Fig. 3.3.2 PM calculation algorithm.



(a)

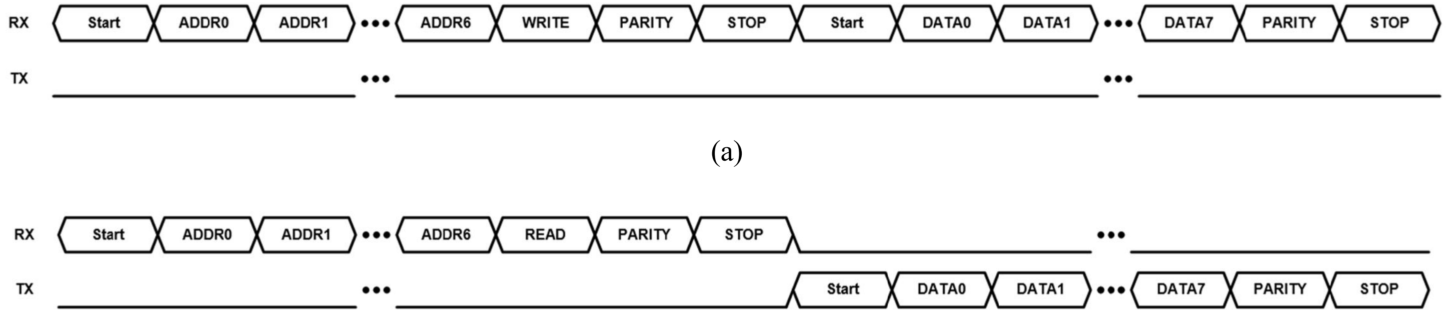


(b)

Fig. 3.3.3 (a) Concentration-based curve fitting and (b) temperature offset compensation offset.

communication performs read and write operations with address 7-bit and data 8-bit. The communication protocol for UART byte communication is depicted in Fig. 3.3.4. The SPI interface operates at 8-bit length, 400 kHz.

The entire digital logic has a scan function using auto test pattern generation (ATPG) and has a test convergence of over 98%. OTP uses 512 bytes and is divided into 6 banks. Each bank has a write flag of 1 bye. It performs a read after a write to verify that the correct data has been written, and writes to this write flag if there is a problem. At the next start-up, the write flag in the OTP loads only the normal bank value.



(a)

(b)

Fig. 3.3.4 UART protocol in the byte communication mode (a) write operation (b) read operation.

3.4 POWER MANAGEMENT CIRCUIT

3.4.1 UNDERVOLTAGE-LOCKOUT CIRCUIT

The typical ROIC operating mode according to the supply voltage is illustrated in Fig. 3.4.1 If the supply voltage does not reach any threshold level, the ROIC must remain in standby by default. When the supply voltage goes well beyond the threshold level, the ROIC enters the functional operating zone and enters the performance guaranteed range once the supply voltage is higher. If the supply voltage does not reach the level of the power supply voltage corresponding to the functional operation period, a problem will occur if the supply voltage is applied to the internal circuit. Leakage problems caused by the internal high impedance nodes, stresses on the devices at this time, and the lifetime of

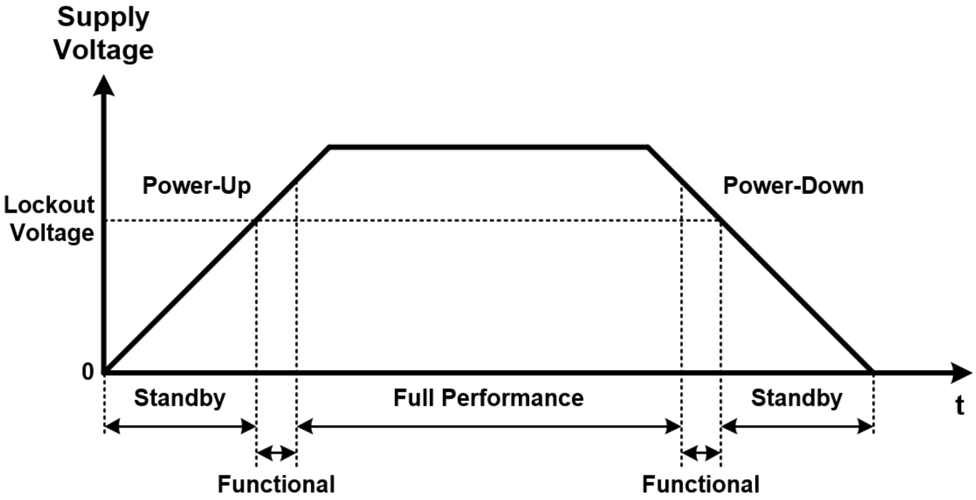
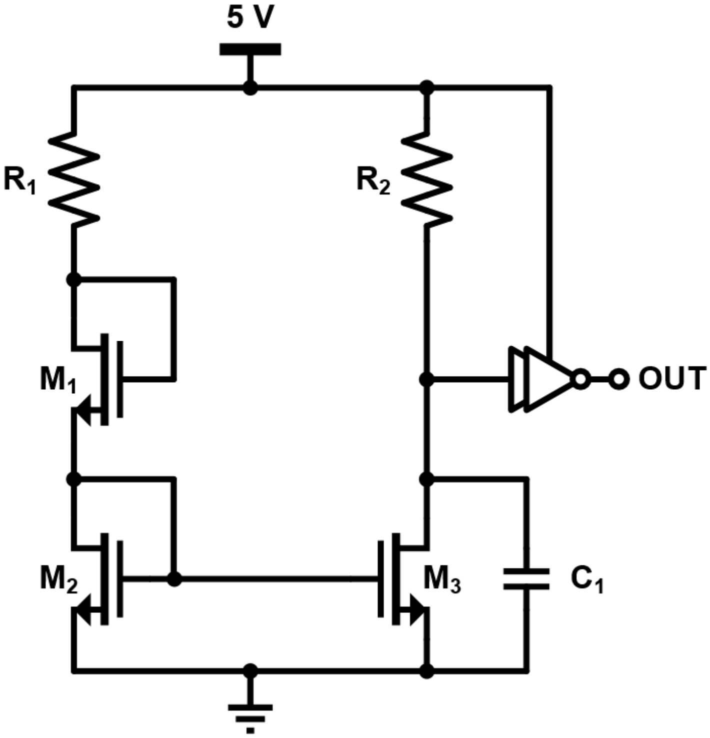


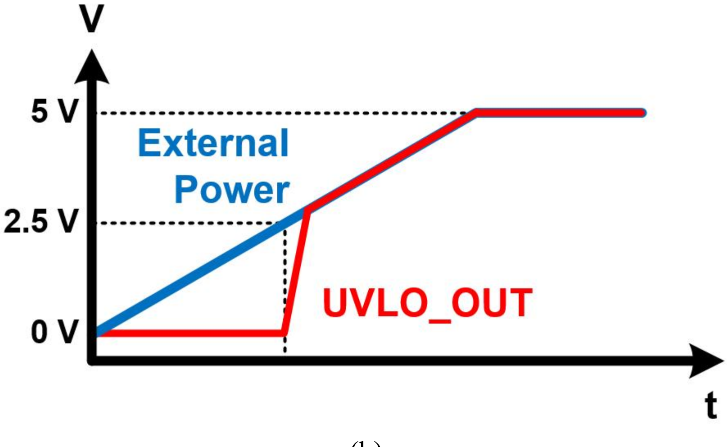
Fig. 3.4.1 ROIC operating mode according to the supply voltage.

the ROIC due to the stress may be caused. Also, the ROIC may become idle due to internal nodes that are not properly reset. Therefore, the internal circuits must not be turned on until the power supply voltage level, which is called the lockout voltage, which ensures the functional operation, is the UVLO circuit.

The detailed circuit diagram and timing diagram of the UVLO circuit can be seen in Fig. 3.4.2 In Fig. 3.4.2 (a), the current flowing through R_1, M_1, and M_2 is mirrored to M_3. M_1 is a diode-connected metal-oxide-semiconductor field-effect transistor (MOSFET) to reduce the area by decreasing the voltage drop on R_1. The bias current flowing through M_3 flows through R_2 and the generated voltage is applied to the input of the inverter. When the supply voltage reaches 2.5 V, the inverter input voltage is designed to be a logic threshold. This signal is applied to the enable signal of the bandgap reference and the bandgap is applied to the LDO which generates the internal supply voltage. Therefore, this UVLO circuit will keep the internal ROIC in standby until the supply voltage reaches 2.5 V.



(a)



(b)

Fig. 3.4.2 (a) UVLO schematic (b) UVLO output waveform when the external supply power is applied

3.4.2 BANDGAP REFERENCE

The BGR circuit supplies the reference voltage to the LDO and supplies the bias current to the internal core circuit. Fig. 3.4.3 shows a BGR circuit with a cascode mirrored load designed in the proposed ROIC. The EN signal is connected to the output

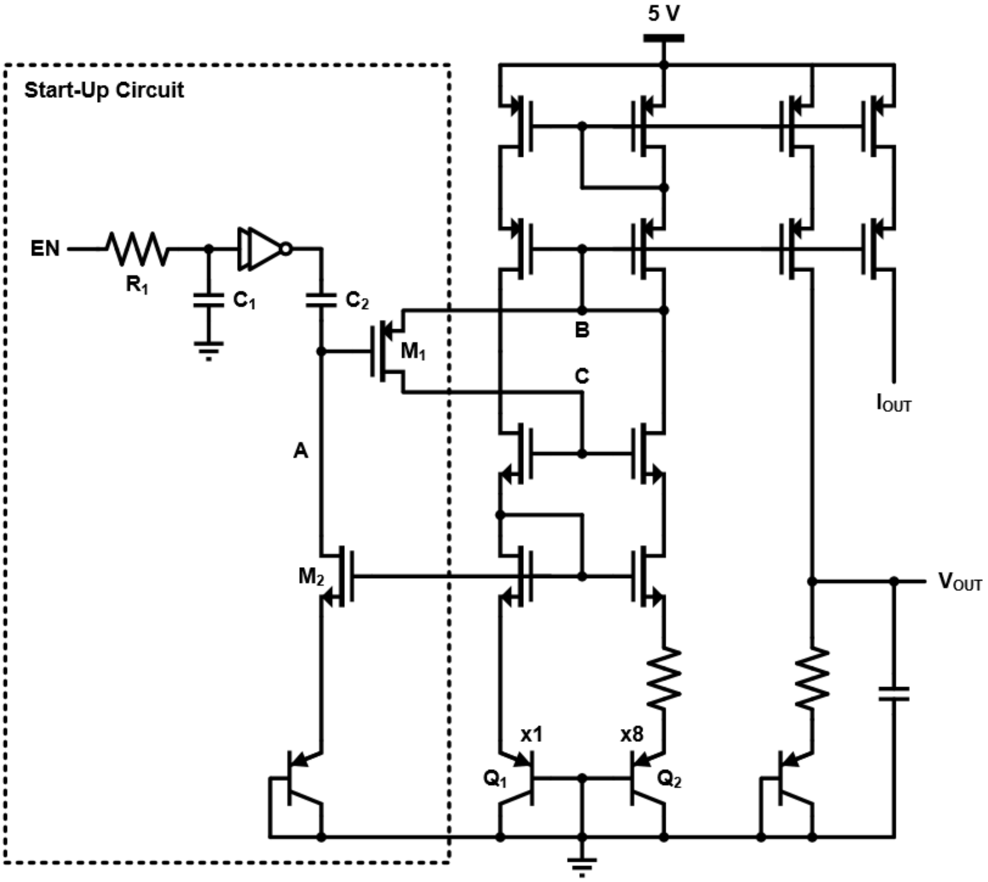


Fig. 3.4.3 BGR schematic.

of UVLO. When EN transitions from low to high, the signal delayed by the LPF consisting of R_1 and C_1 goes through buffering and pulls up the voltage of node A through C_2. M_1 turns on and M1 connects B and C nodes to wake up the BGR core circuit. Then the A node is slowly pulled down by M_2 to turn off the start-up circuit. Q_1 and Q_2 are designed as 1:8 considering layout.

3.4.3 OSCILLATOR

The oscillator is based on a ring oscillator structure as shown in Fig. 3.4.4. The frequency of the output clock is calculated as:

$$f_{CLK} = \frac{1}{2\left(\frac{C_1 V_{REF}}{I_{REF}} + t_d\right)} \tag{3.4.15}$$

Where V_{REF} and I_{REF} is tunable reference voltage and current to get the fine resolution of frequency and C_1 is the capacitance of C_{1A} and C_{1B}. t_d is the propagation delay of the back-end logic gates from the comparator. The center frequency of the clock is 4 MHz with 1 % of frequency resolution and +/-30 % of tunable range.

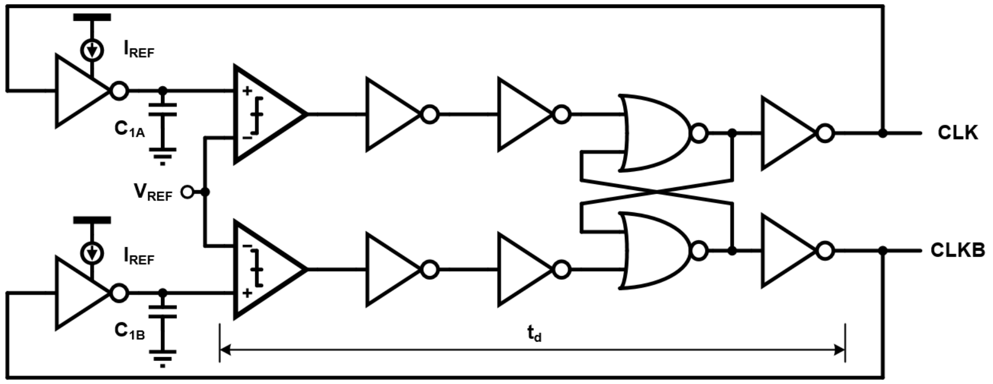


Fig. 3.4.4 On-chip oscillator schematic.

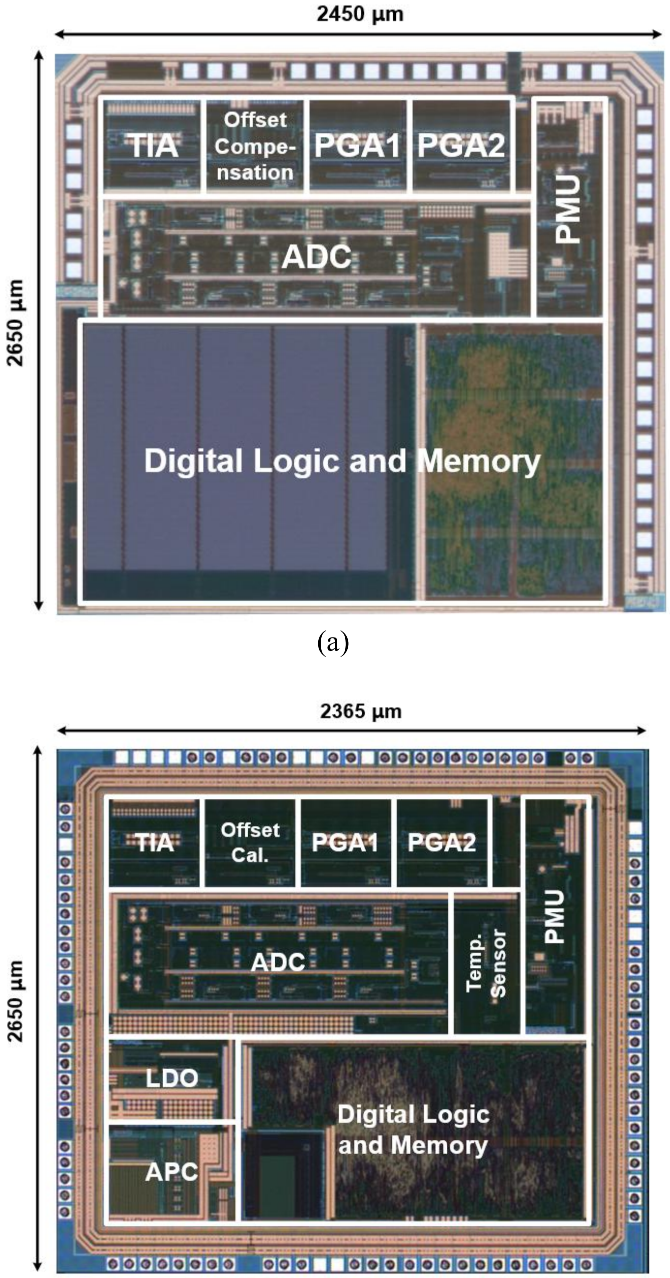
CHAPTER 4

EXPERIMENTAL RESULTS

4.1 DIE MICROGRAPH AND MODULE

The measurements were performed separately for two modules on which the proposed ROICs are mounted. One is to detect $PM_{2.5}$ and PM_{10} using LED as the light source, and the other is to detect PM_1, $PM_{2.5}$ and PM_{10} using LD as the light source. The die micrographs for each chip are shown in Fig. 4.1.1. The on-chip temperature sensor and APC circuit are included only in the LD PM detector. The total die areas of the two chips are almost the same, 6.49 mm^2 for the LED PM detector and is 6.27 mm^2 for the LD PM detector.

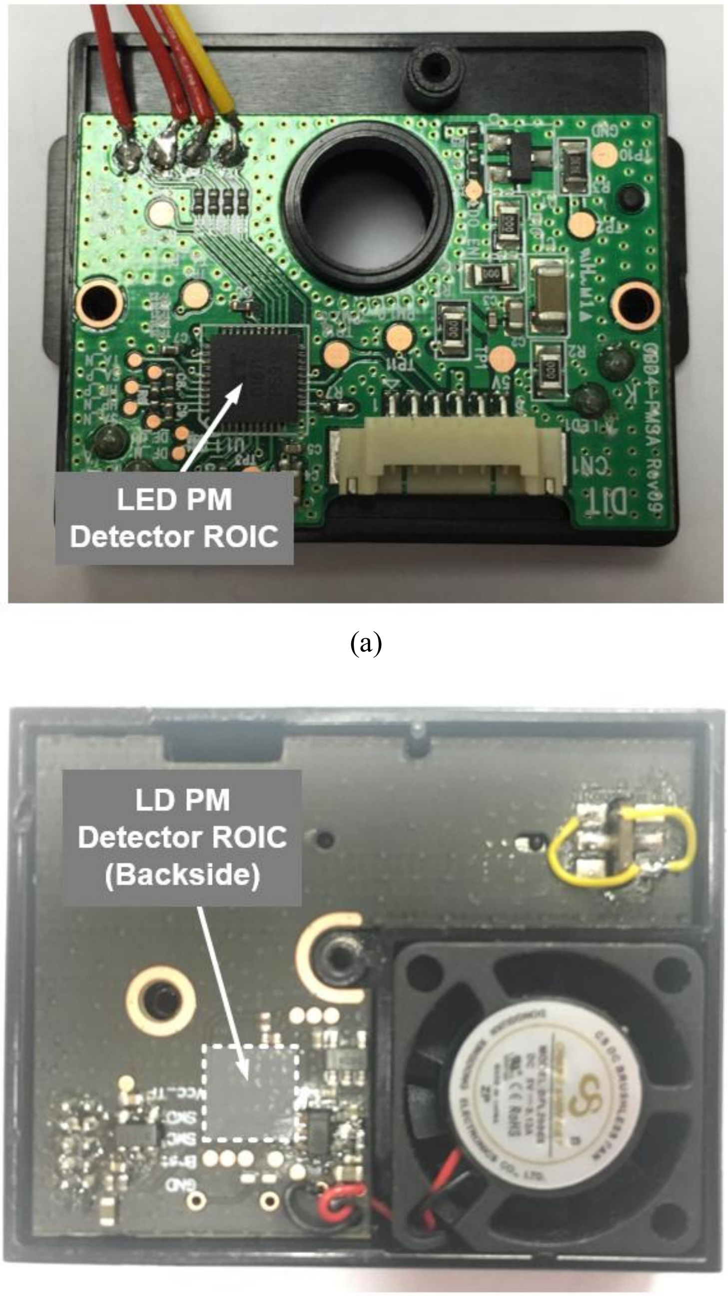
The modules are shown in Fig. 4.1.2. Fig. 4.1.2 (a) shows the LED PM detector module and Fig. 4.1.2 (b) shows the LD PM detector module. Unlike the LED PM detector, the LD PM detector has a fan in the module to create an air flow. The reference PD, which measures the light intensity of the LD, is equipped with a sealed sub-module. The PD that receives the light scattered by the particles and generates the current signal.



(a)

(b)

Fig. 4.1.1 Die micrograph of the proposed (a) LED PM detector (b) LD PM detector.



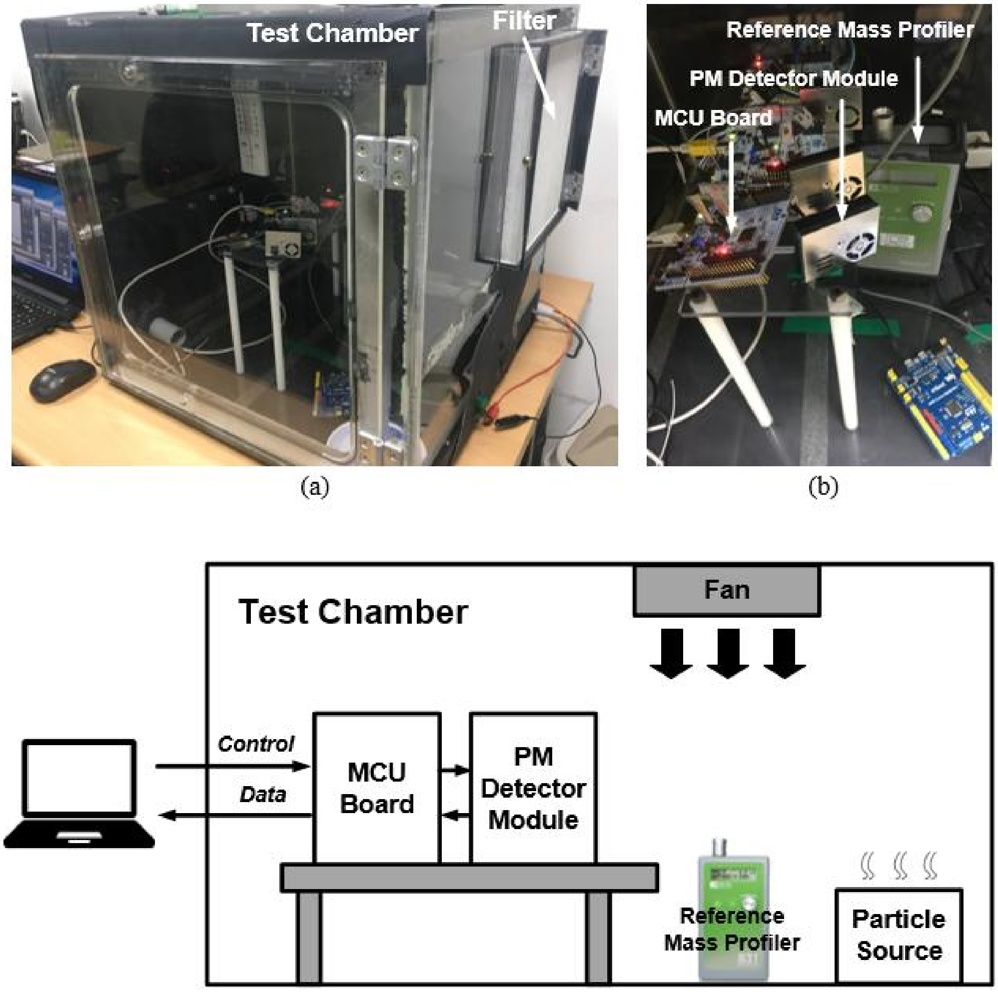
(a)

(b)

Fig. 4.1.2 Module photo of the proposed (a) LED PM detector (b) LD PM detector.

4.2 MEASUREMENT SETUP

The measurements are conducted in a chamber that shields the air inside from the air outside as shown in Fig. 4.2.1. There is a particle source in the chamber and the fan circulating the air inside to generate a uniform air flux. Our PM detector and the reference mass profiler start to measure the particles at the same time inside the chamber. As the particles escape through a filter at the wall of the chamber, the PM concentration decreases over time. A MCU board is utilized between our PM detector and a computer for communication of control signals and data. Cigarette smoke and mosquito coil were used as the particle sources for PM_1, $PM_{2.5}$ and PM_{10} measurement. The *Aerocet 831* and the *Aerosol Spectrometer 11-A*, were used as the reference mass profilers.



(c)

Fig. 4.2.1 Measurement setup.

4.3 MEASUREMENT RESULTS

Fig. 4.3.1 shows the 2nd PGA's output waveform before and after the operation of the proposed DC offset calibration in the LED PM detector. When the DC offset calibration is disabled, the output value is clipped and stuck to the supply voltage as shown in Fig. 4.3.1 (a). If the DC offset calibration is enabled, the analog output is located in the input range of the following ADC as shown in Fig. 4.3.1 (b).

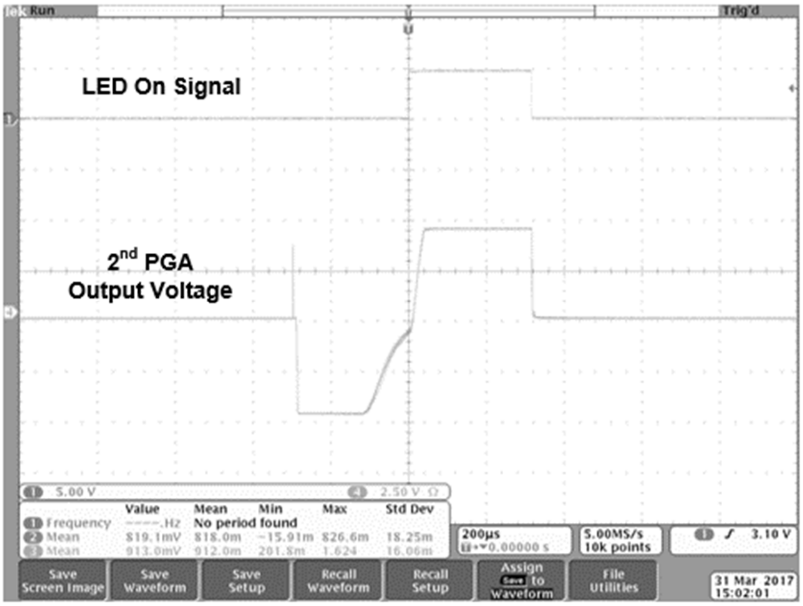
Fig. 4.3.2 shows the measurement results of $PM_{2.5}$ and PM_{10} before and after concentration-based curve fitting with the LED PM detector. I used cigarette smoke as the particle source and the *Aerocet 831* as a reference mass profiler. The non-linear profile is observed in the low concentration region (about 0 ~ 300 $\mu g/m^3$ region) due to the light source characteristics, but the linearity is improved after the concentration-based digital curve fitting. This algorithm is applied to both the LED PM detector and the LD PM detector. To compare the results before and after the curve fitting quantatively, I used the square of the correlation coefficient:

$$R^2 = \frac{(\sum(x-\bar{x})(y-\bar{y}))^2}{\sum(x-\bar{x})^2 \sum(y-\bar{y})^2} \tag{4.3.1}$$

The square of the correlation coefficient, R^2 is improved from 0.9915 to 0.9992 for $PM_{2.5}$ and from 0.9918 to 0.9990 for PM_{10}. It means that the $PM_{2.5}$ and PM_{10} results are very accurate compared with the data measured by the reference mass profiler.

Fig. 4.3.3 and 4.3.4 are the the measurement results of the LD PM detector. I used mosquito coil as the particle source and *Aerosol Spectrometer 11-A* as a reference mass profiler. The analog DC offset calibration is disabled in this measurement since the LD is not turned on and off periodically. The APC is enabled and all the digital post-processing is conducted including concentration-based curve fitting, temperature-dependent offset compensation, and gain compensation. The PM_1, $PM_{2.5}$, and PM_{10} measurement results showed 0.9990, 0.9992, and 0.9992, respectively.

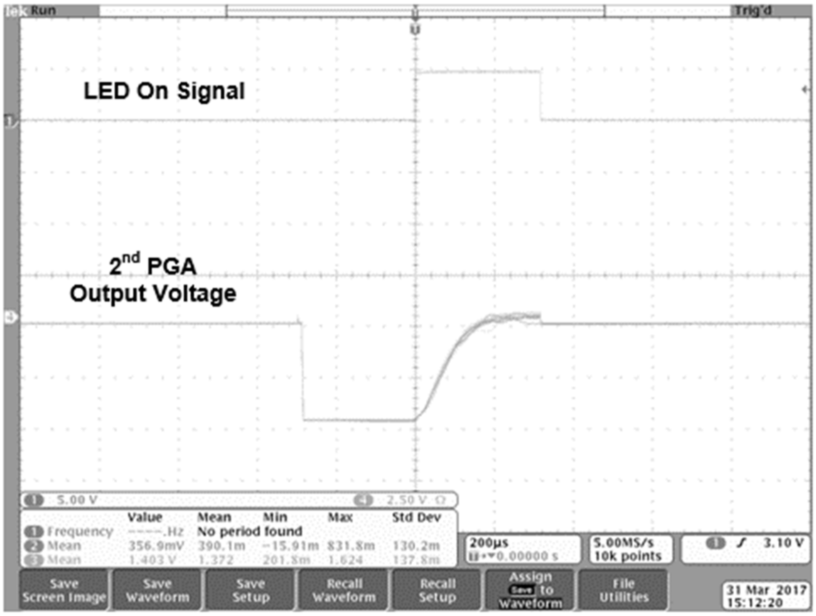
Fig. 4.3.5 is a PM_1 output plot of the LD PM detector with respect to 800 samples according to the temperature. The temperature was swepet with 10 ℃ steps in the range of 0 ~ 50 ℃, when the on-chip temperature sensor and the digital compensation circuit are enabled. Fig. 4.3.6 shows the maximum error modulus results extracted the results of Fig. 4.3.5. The results of the proposed LD PM detector are compared with commercial optical PM detector, PMS1003 made by Plantower. Our chip reveals more than 10 times better performance in the temperature range of 0 ~ 50 ℃.



```
           Value     Mean    Min      Max     Std Dev
1 Frequency ----.Hz  No period found
2 Mean     819.1mV  818.0m  -15.91m  826.6m  18.25m
3 Mean     913.0mV  912.0m  201.8m   1.624   16.06m
```

```
200μs
▼0.00000 s
5.00MS/s
10k points
1 ∫ 3.10 V
31 Mar 2017
15:02:01
```

(a)

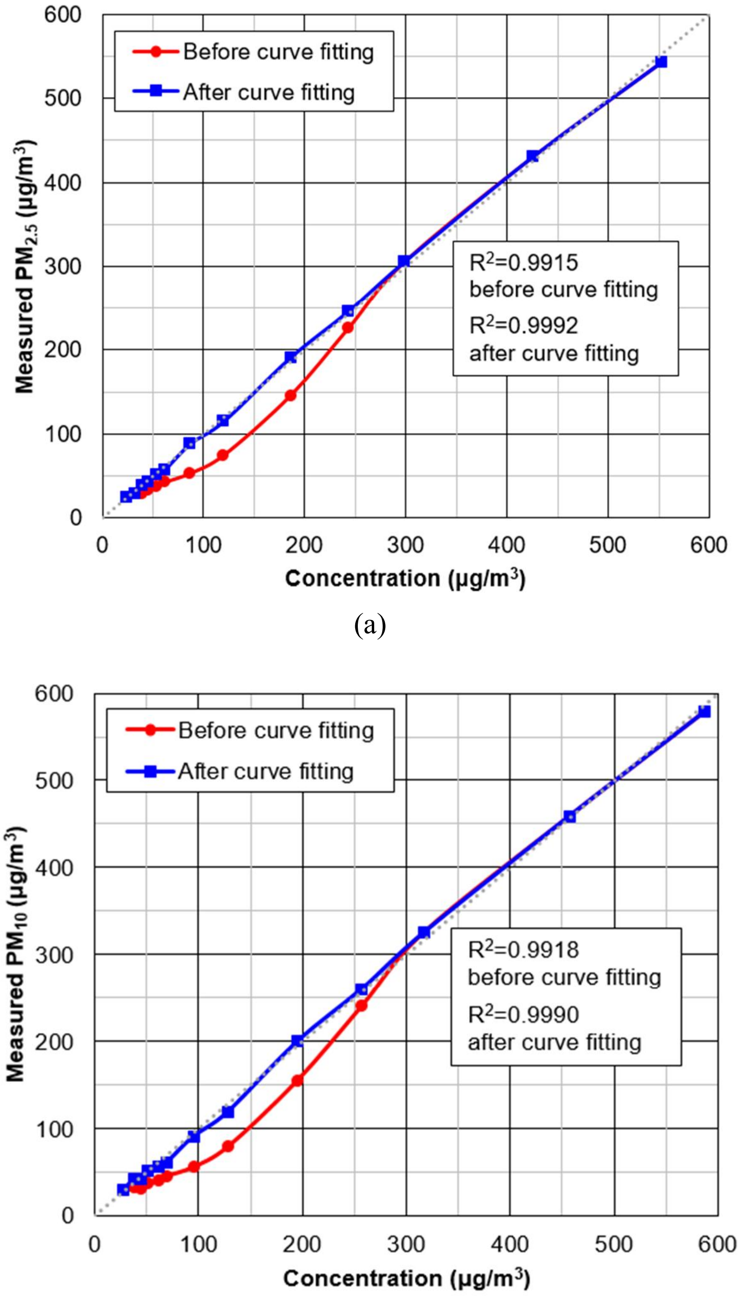


```
           Value     Mean    Min      Max     Std Dev
1 Frequency ----.Hz  No period found
2 Mean     356.9mV  390.1m  -15.91m  831.8m  130.2m
3 Mean     1.403 V  1.372   201.8m   1.624   137.8m
```

```
200μs
▼0.00000 s
5.00MS/s
10k points
1 ∫ 3.10 V
31 Mar 2017
15:12:20
```

(c)

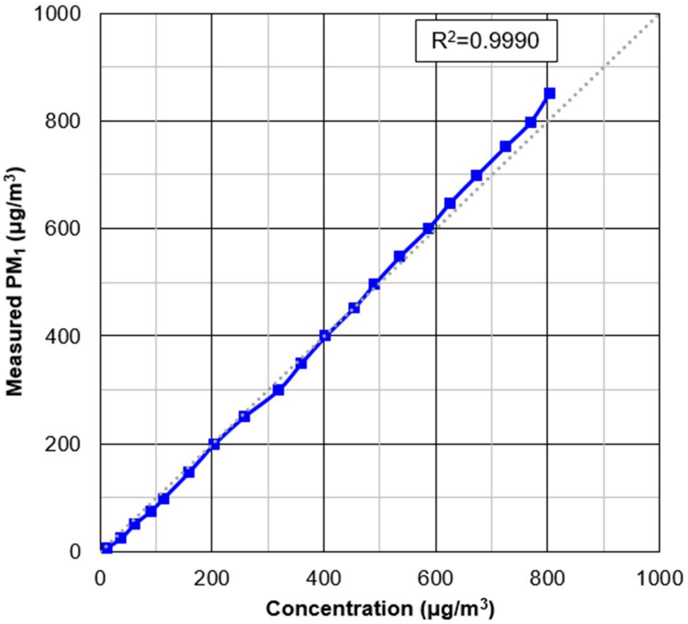
Fig. 4.3.1 Output waveform of 2nd PGA in LED PM detector (a) when DC offset calibration is disabled (b) when DC offset calibration is enabled.



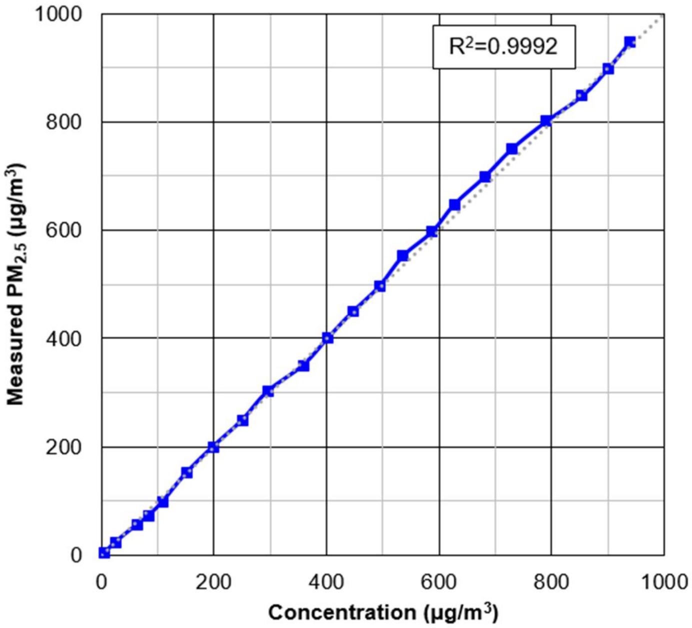
(a)

(b)

Fig. 4.3.2 Measurement results of the LED PM detector for (a) $PM_{2.5}$ (b) PM_{10}.



(a)



(b)

Fig. 4.3.3 Measurement results of the LD PM detector using LD for (a) PM_1 (b) $PM_{2.5}$.

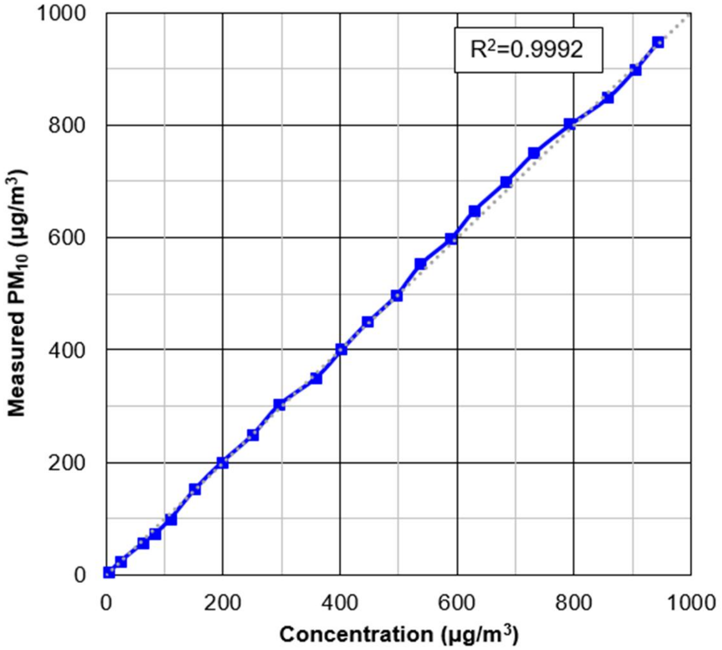


Fig. 4.3.5 Measurement results of the LD PM detector for PM$_{10}$.

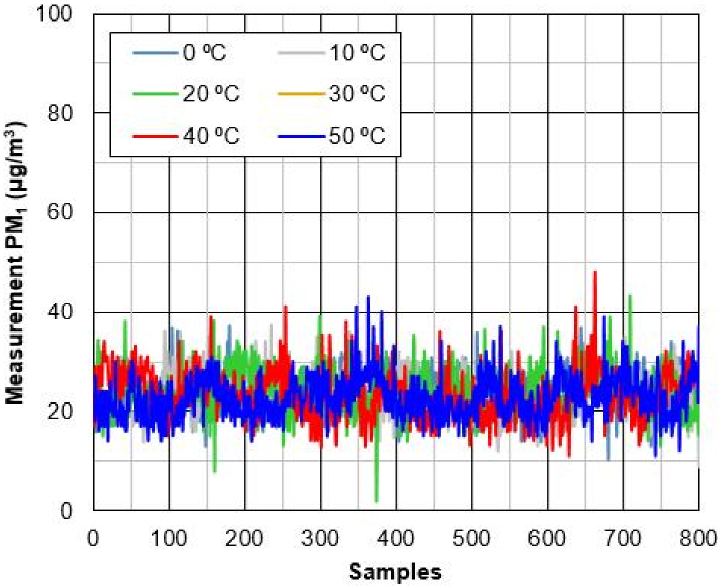


Fig. 4.3.4 Measurement result of the LD PM detector for PM$_1$ with temperature sweep.

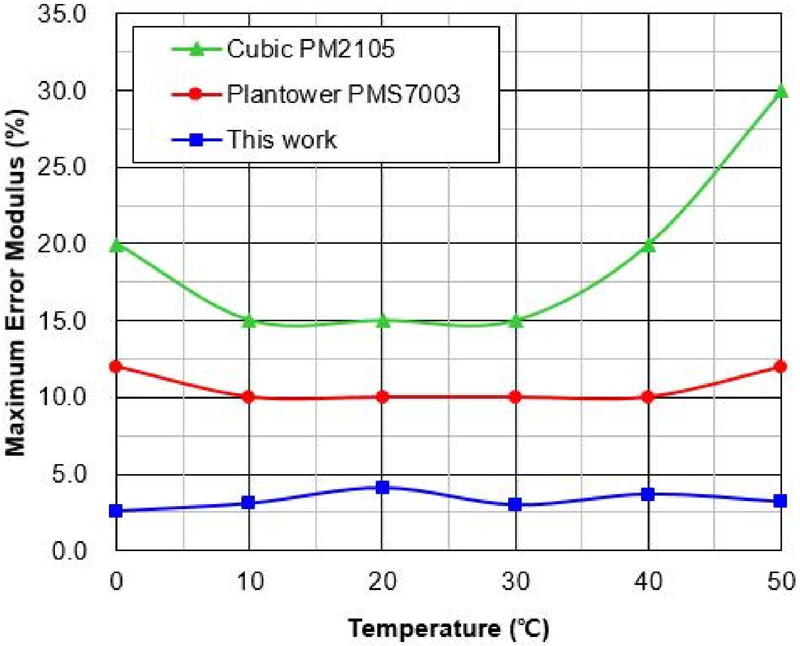


Fig. 4.3.6 Maximum error modulus comparison with Plantower PMS1003 [4.1.2]

Table 4.3.1 shows the comparison of the performance and the prior arts of the proposed LED PM and LD PM detectors. Both proposed PM detectors use a 0.18 μm CMOS process and use a 5 V supply voltage. Both PM detectors support analog output (PWM) and digital output (UART/SPI) and use an 11-b 100 kS/s ADC. The Particle concentration detection range is 0 ~ 600 μg/m^3 for LED PM detector and 0~1100 μg/m^3 for LD PM detector. Input-referred RMS noise current is 2.69 pA for LED type and 2.2 pA for LD type. The total power consumption is 5 mW for the LED type and 10 mW for the LD type, except for the load current of the LED driver and APC in the LD.

Table 4.3.1 Performance summary.

	This work		P. Ciccarella, ISSCC 2016 [1.2.2]	J. Cheon, SJ 2009 [2.2.1]	Honeywell 32322550 2018 [1.2.5]	Plantower PMS1003 2016 [4.1.2]
	LED type	LD type				
Process	0.18 μm CMOS	0.18 μm CMOS	0.35 μm CMOS	0.35 μm CMOS	-	-
Sensing type	Optical (LED)	Optical (LD)	Capacitive	Optical (LED)	Optical (LD)	Optical (LD)
Counting efficiency	-	50% @0.3 μm	-	-	-	50% @0.3 μm
Integrated DSP	O	O	X	X	O	O
Supply voltage	5 V	5 V	3.3 V	3.3 V / 24 V	5 V	5 V
Range of measurement	1 ~ 2.5 μm, 2.5 ~ 10 μm	0.3 ~ 1 μm, 1 ~ 2.5 μm, 2.5 ~ 10 μm	1 ~ 16 μm (sim) 6 μm (meas)	1 ~ 2.5 μm*	1 ~ 2.5 μm, 2.5 ~ 10 μm	0.3 ~ 1 μm, 1 ~ 2.5 μm, 2.5 ~ 10 μm
Resolution	10-b	10-b	-	8-b	-	10-b
Maximum Concentration range	1000 μg/m^3	1000 μg/m^3	-	-	1000 μg/m^3	1000 μg/m^3
Maximum consistency error (PM$_{2.5}$)	± 10 μg/m^3 @0~100 μg/m^3 ± 10 % @100~1000 μg/m^3	± 10 μg/m^3 @0~100 μg/m^3 ± 5 % @100~1000 μg/m^3	-	-	± 15 μg/m^3 @0~100 μg/m^3 ± 15 % @100~1000 μg/m^3	± 10 μg/m^3 @0~100 μg/m^3 ± 10 % @100~500 μg/m^3
Maximum error modulus (0 ~ 50 ℃)	-	3.3 ± 0.75 %	-	-	-	10.7 ± 1 %
Effective area	2.70 mm^2**	4.14 mm^2	6 mm^2	17.64 mm^2	-	-
Power consumption	5 mW (ROIC) 55 mW (Total)	10 mW (ROIC) 400 mW (Total)	84 mW	220 nW (ROIC) 15.35 mW (Total)	400 mW (Total)	500 mW (Total)

* Estimated due to the lack of information.

** Memory size is not included.

CHAPTER 5

CONCLUSION

In this study, I propose a low-noise sensor interface for optical PM detectors. The proposed optical PM detector is implemented in two different types which uses a LED and a LD as a light source. The input current signal is converted to a voltage signal at TIA, amplified and filtered after removing the DC offset of the input. It is then applied to an ADC for digitization. I propose a DC offset calibration method using an OPAMP with embedded DAC only when the light source is turned on. In addition, an APC circuit is used to make the light intensity of the LD less sensitive against the external environmental changes or noise. The APC circuit monitors the light intensity using the reference photodiode and controls the bias current of the LD to get the light intensity be constant when it is changed. This enables small-sized particles to be measured with high resolution. The digital post-processing is performed as the following procedure. First, a PM calculation is performed to calculate the concentration by particle size. Then it is low-pass filtered to remove high-frequency noise. The concentration-based curve fitting algorithm is then carried on to make the concentration profile linear. And next, the offset compensation is performed according to the temperature of which information is generated by on-chip temperature sensor. Finally, the gain-compensated output is sent through a digital interface such as PWM, UART, and SPI. The measurement is conducted in a chamber with two types of optical PM detector that uses LED and LD as a light source, respectively. The result is analyzed by comparing the result of the reference mass profiler located in the same chamber. The experimental results showed high accuracy in PM_1, $PM_{2.5}$ and PM_{10}. The square of the correlation coefficient (R^2) showed more than 0.999 in all measurement, and the maximum consistency errors of the LED module and the LD module are +/- 5 % and +/- 1.6 %, respectively, which is much better than other commercial optical PM detectors. All chips were fabricated with a 0.18 μm standard CMOS process. The chip areas are 6.49 mm^2 and 6.27 mm^2, and power consumptions are 5 mW and 10 mW (excluding bias current of the light sources) for the LED PM detector and the LD PM detector, respectively.

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한글 초록

본 연구에서는 미세 입자 (PM) 검출기를 위한 저잡음 광학 센서 인터페이스를 제안한다. 입자는 직경에 크기에 따라 PM_1 (< 1 μm), $PM_{2.5}$ (< 2.5 μm), PM_{10} (< 10 μm) 로 구분한다. 광학 미세 입자 검출기는 발광 다이오드(LED) 나 레이저 다이오드 (LD) 로부터 조사된 빛이 입자에 부딪혀 산란되는 양을 포토 다이오드(PD)에서 측정하는 방식을 사용한다. 수신된 입력 전류 신호는 트랜스임피던스 증폭기 (TIA) 에서 전압 신호로 변환되고, 입력의 DC 오프셋을 제거한 후 증폭 및 필터링 된다. 그리고 이 신호는 아날로그-디지털 변환기(ADC) 로 인가되어 디지털 신호로 변환된다. 기존의 이중 상관 샘플링 (CDS) 기법은 이산 시간 switched-capacitor (SC) 회로에만 적용이 가능한데, 이 이산 시간 회로는 연속 시간 회로에 비해 일반적으로 전력 소모가 크고 많은 칩 면적을 필요로 한다. 또 다른 기존의 방식인 전류 출력 디지털-아날로그 컨버터 (DAC) 를 이용하게 되면 소자의 잡음이 큰 문제가 있으며, 이를 줄이기 위해서는 다시 많은 소모 전력과 칩 면적이 요구된다. 본 연구에서는 광원이 켜져 있을 때에만 연산증폭기의 한 쪽 입력 트랜지스터의 크기를 디지털 신호로 변화시키는 형태의 연산증폭기 내장 DAC를 이용해 잡음, 소모 전력, 면적을 줄였다. 또한 LD PM 검출기에서 외부 환경 변화와 잡음에 의해 LD의 빛의 세기가 민감하게 변하는 것을 줄이기 위해 평균 전원 제어 (APC) 회로를 사용하였다. APC

회로는 레퍼런스 포토 다이오드를 이용해 빛의 세기를 모니터링하고 의 세기가 변하면 원래의 세기로 돌아가게끔 LD에 흐르는 바이어스 전류를 바꾸어준다. 이로써 작은 크기의 입자도 높은 해상도로 측정할 수 있다. 디지털 후처리 과정은 다음과 같은 프로세스로 수행된다. 먼저 입자 크기별로 농도를 계산하는 PM 계산 과정을 거치고, 고주파 잡음을 제거하기 위한 디지털 로우 패스 필터링 (LPF) 이 수행된다. 이후 비선형적인 형태를 가지는 저농도 구간에 대해 선형화 작업이 수행된다. 그리고 내장된 온도 센서의 출력을 읽어와 구간별로 오프셋을 다르게 주어 온도에 의한 출력값의 변화를 최소화한다. 마지막으로 농도 별 이득 보정을 마친 출력을 디지털 인터페이스를 통해 pulse-width modulation (PWM), universal asynchronous transmitter (UART), serial peripheral interface (SPI) 등의 형태로 내보낸다. 측정은 각각 LED와 LD를 광원으로 사용하는 두 가지의 다른 광학 PM 검출기에 대해 챔버 안에서 수행하였다. 결과는 동일한 챔버 내에서 측정을 진행한 레퍼런스 질량 분석기의 결과와 비교하여 분석하였다. 측정 결과 PM_1, $PM_{2.5}$, 그리고 PM_{10}에서 높은 정확도를 보였다. 상관 계수의 제곱 (R2) 값은 모든 결과에서 0.999 이상을 보였고, 최대 일관성 오류는 LED와 LD 모듈이 각각 +/- 5 %와 +/- 1.6 % 를 보였는데, 이는 상용 광학 PM 검출기를 훨씬 상회하는 성능이다. 모든 칩은 모두 0.18 μm 표준 CMOS 공정으로 제작되었으며, 칩 면적은 LED, LD PM 검출기가 각각 6.49 mm^2, 6.27 mm^2, 전력 소모는 각각 5 mW, 10 mW (광원 바이어스 전류 제외) 로

측정되었다.

주요어 : 광학 미세 입자 검출기, 연기, 먼지, 오프셋 보정, 적응형 전원 제어.

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