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Ph.D. Dissertation

A STUDY ON BLOCKER-TOLERANT WIDEBAND RECEIVERS

대역 외 방해신호에 내성을 가지는 광대역 수신기에 관한 연구

February 2018

GRADUATE SCHOOL OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE
SEOUL NATIONAL UNIVERSITY

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공학박사 학위논문

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2018 년 2 월

서울대학교 대학원

전기 · 컴퓨터공학부

김덕수

Abstract

In this thesis, a study of wideband receivers as one of the practical SDR receiver implementations is presented. The out-of-band interference signal (or blocker), which is the biggest problem of the wideband receiver is investigated, and have studied how to effectively remove it. As a result of reviewing previous studies, we have developed a wideband receiver based on the current-mode receiver structure and attempted to eliminate the blocker. The contents of the step-by-step research are as follows.

First, attention was paid to the linearity of a low-noise transconductance amplifier (LNTA), which is the base block of current-mode receivers. In current-mode receivers, the LNTA should have a high transconductance (G_m) value to achieve a low noise figure, but a high G_m value results in low linearity. To solve this trade-off, we proposed a linearization method of transconductors. The proposed technique eliminates the third-order intermodulation distortion (IMD3) in a feed-forward manner using two paths. A transconductor having a transconductance of $2G_m$ is disposed in the main path, and an amplifier having a gain of $\sqrt[3]{2}$ and a G_m-sized transconductor are located in the auxiliary path. This structure allows for some fundamental signal loss but cancel the IMD3 component at the output. As a result, the entire

transconductor circuit can have high linearity due to the removed IMD3 component. We have designed a reconfigurable high-pass filter using a linearized transconductor and have demonstrated its performance. The fabricated circuit achieved a high input-referred third-order intercept point(IIP3) performance of 19.4 dBm.

Then, a further improved linearized transconductor is designed. Since the linearized transconductors have a high noise figure due to the additional circuitry used for linearization, we have proposed a more suitable form for application to LNTA through noise figure analysis. The improved LNTA is designed to operate in low noise mode when there is no blocker, and can be switched to operate in high linearity mode when the blocker exists. We also applied noise cancelling techniques to the receiver to improve the noise figure performance of the wideband receiver circuit. A feedback path has been added to the current-mode receiver structure consisting of the LNTA, the mixer and the baseband transimpedance amplifier (TIA), and the noise signal can be detected using this path. This feedback path also maintains the input matching of the receiver to 50 Ω in a wide bandwidth. By adding an auxiliary path to the receiver, the in-band signal is amplified and the detected noise is removed from the baseband. The completed circuit exhibited wideband performance from 0.025 GHz to 2 GHz and IIP3 performance of −6.9 dBm in the high linearity mode.

Finally, we designed a double noise-cancelling wideband receiver circuit by improving the performance of a wideband

receiver with high immunity to blocker signals. In previous receivers, the LNTA was operated in two modes depending on the situation. In the improved receiver, the G_m ratio of the linearized LNTA was changed and the RF noise-cancelling technique was applied. The input matching and noise cancelling scheme introduced in the previous circuit was also applied and a wideband receiver circuit was designed to perform double noise-cancelling. As a result, the linearization and noise-cancellation of LNTA could be achieved at the same time, and the completed receiver circuit showed high IIP3 performance of 5 dBm with minimum noise figure of 1.4 dB.

In conclusion, this thesis proposed a linearization technique for transconductor circuit and designed a wideband receiver based on current-mode receiver. The designed receiver circuit experimentally verified that it has low noise figure performance and high IIP3 performance and is tolerant to out-of-band blocker signals.

Keyword : Wideband receiver, blocker, linearity, transconductor linearization, noise cancelling

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Chapter 1. Introduction

In modern society, communication is very important, and wireless communication is done by radio frequency (RF) system. As wireless standards grow year by year and frequency allocation becomes complex, RF systems are demanding high performance and flexibility, small device size and low cost. One of the notable concepts of future wireless systems is software-defined radio (SDR). The concept of SDR has been proposed since the 1990s, but a viable practical SDR has not yet been developed. This thesis describes the structure of a wideband receiver as part of a study to get closer to practical SDR receivers.

Section 1.1 describes the SDR and the wideband receiver as the motivation for the study. Section 1.2 discusses key techniques that must be accomplished in order to implement a wideband receiver, particularly how to eliminate interference. Section 1.3 reviews the various solutions presented so far to eliminate interference signals. Finally, Section 1.4 defines the objectives of this study.

1.1. Motivation of Wideband Receiver Architecture

Communication between people is very important, and communication is one of the basis of modern society. Wireless communications have enabled seamless communication between people who are far away, and their market, size, and importance are increasing day by day. Therefore, many types of wireless communication standards have been developed for various communication purposes. These wireless communication standards are placed in the frequency spectrum through frequency allocation. The frequency spectrum we use today is already complicated by the large number of wireless communication standards, which can be seen in Fig 1.1. Fig 1.1 shows the allocation of wireless communications standards that are closely related to our lives in the frequency range from 30 MHz to 3 GHz. Here, we can find that the communication spectrum for mobile phones such as 3G and LTE, wireless communication standards such as Wi-Fi and Bluetooth, as well as RFID, GPS and TV broadcastings, fill the frequency spectrum .

All wireless communications standards have dedicated transceiver hardware, and the number is growing every year. Suppose that a single transmitter / receiver system can support multiple communication standards. If one system supports multiple wireless communication standards, this system will achieve smaller device size, lower price, and more flexible system than using

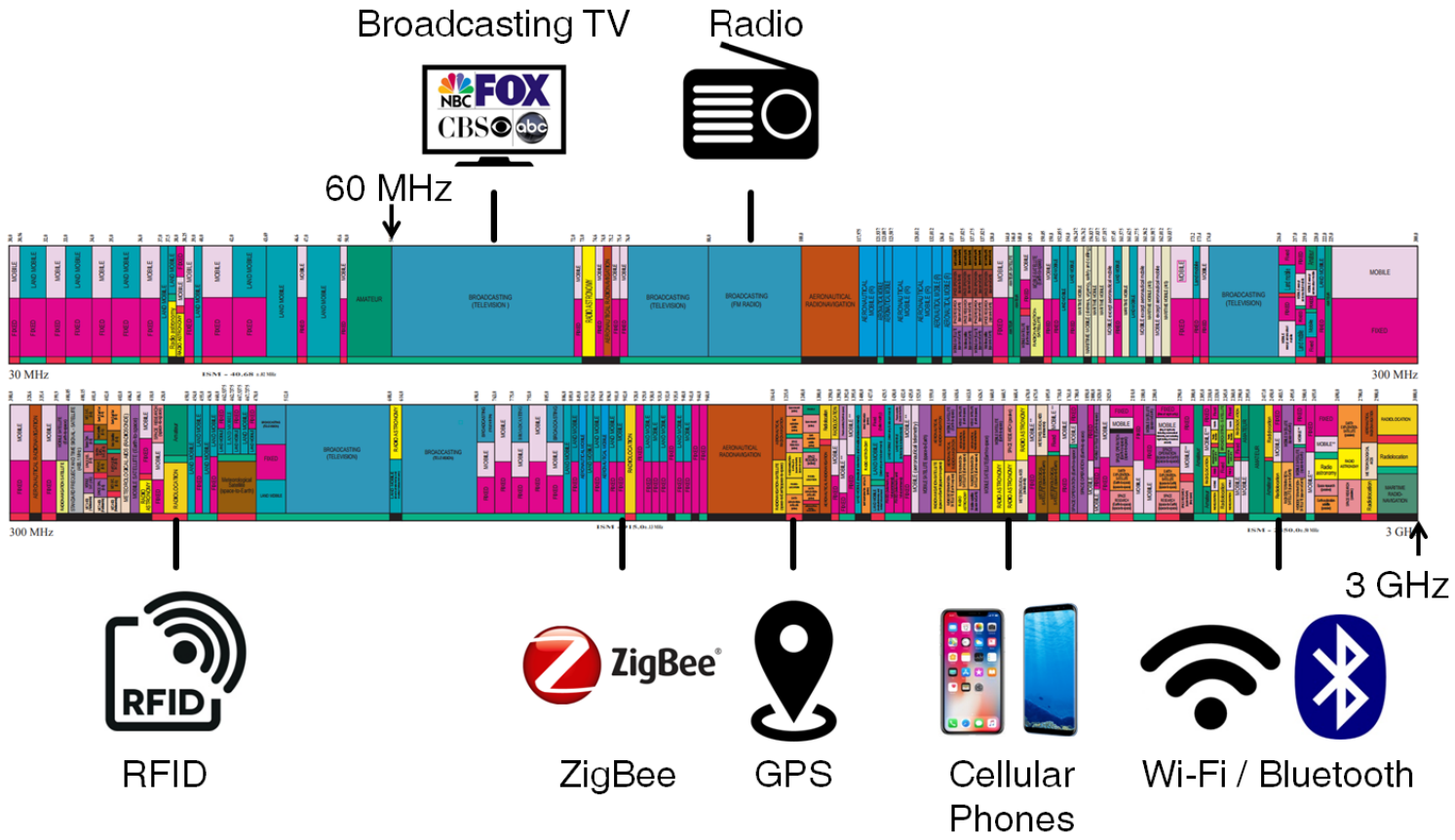


Fig. 1.1 RF frequency spectrum allocation of various standards.

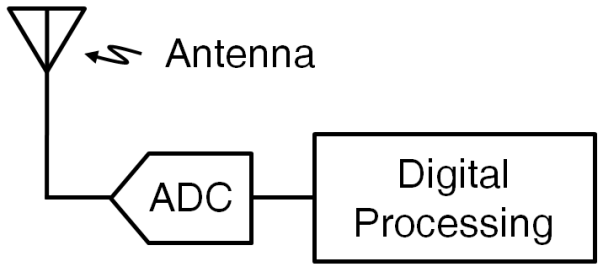


Fig. 1.2 Block diagram of ideal software-defined radio architecture.

dedicated systems per wireless communication standard. This concept can be thought of as controlling flexible hardware using software. This concept is called software-defined radio (SDR) and was first proposed by Mitola in the 1990's [1] [2]. The block diagram of the SDR is shown in Fig. 1.2.

The SDR system consists of an antenna, an analog-to-digital converter (ADC), and a digital processing block. The RF signal received from the antenna is directly converted into a digital signal through the ADC, and the digital processing block carries out signal processing using software. This means minimizing the use of hardware in the system, and the operation of the system is defined by the software.

Although this method can be used to configure the most flexible system, the ideal SDR system has many difficulties in practical implementation. The most problematic part of the SDR system

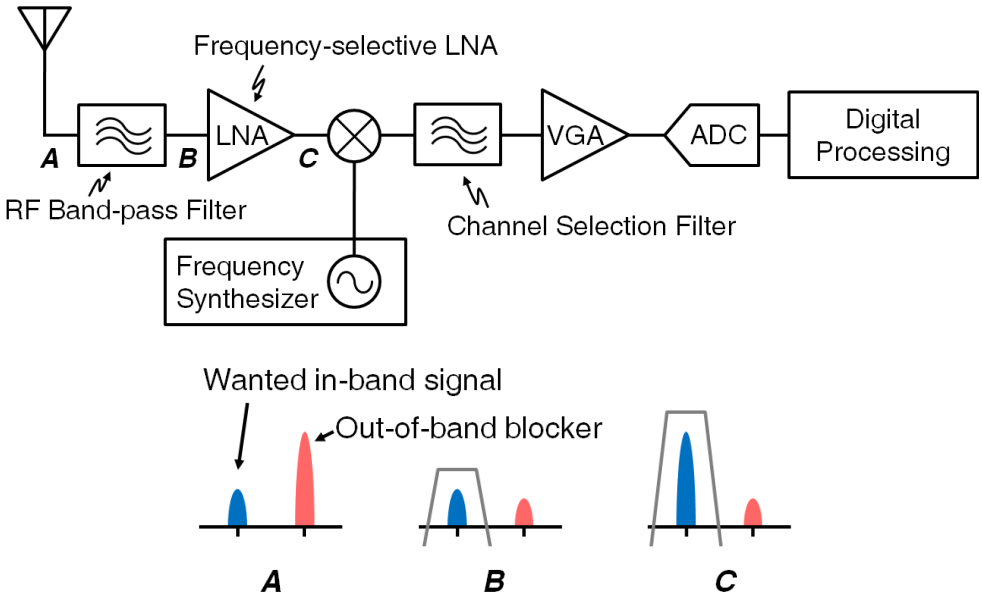
implementation is the ADC. In an ideal SDR system, the ADC directly digitizes the RF signal, but a high-performance ADC capable of this operation is generally not possible. This is because the dynamic range and speed performance required by the ADC are very high. For example, suppose you have an ADC that can handle all the signals from 30 MHz to 3 GHz, as shown in Fig. 1.1. If the signal input to the antenna is between 1 μV and 100 mV, the required resolution of the ADC is approximately 16 bits. To sample a signal at 3 GHz, the ADC speed must be at least $6\,\mathrm{Gsamples/s}$. Assuming optimally that 1 pJ of energy per each conversion is required, this results in a calculation of $6 \times 10^{9}\ \mathrm{samples/s} \times 2^{16}\ \mathrm{levels} \times 10^{-12}\mathrm{J} \approx 400\,\mathrm{W}$ [3] [4]. Therefore, the implementation of ideal SDR is very difficult. Although it is not possible to implement an ideal SDR, it is possible to develop a practical SDR by locating the ADC as close as possible to the antenna and using minimal hardware blocks [5]. Receivers with a structure that uses hardware that supports wideband and places the ADC after mixing, at intermediate frequency (IF) can be a good example of the practical SDR receiver [6] [7].

SDR includes a wide range of research topics, ranging from analog circuits to digital circuits, transmitters to receivers. In this thesis, we will concentrate on the analog-front-end part of a complementary metal oxide semiconductor (CMOS)-based receiver. The analog-front-end is a receiver block that performs amplification, down-conversion, and filtering prior to the ADC. In

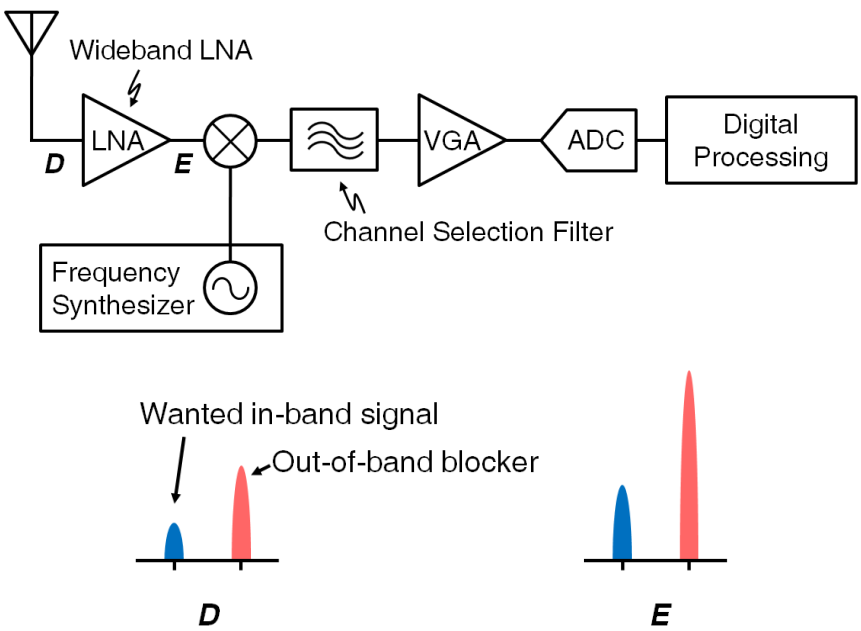
the next chapter, we will look at the challenges to achieving the analog-front-end of a practical SDR receiver.

1.2. Challenges in Designing Wideband Receiver

Conventional wireless receivers are designed to support only one desired communication specification. Fig. 1.3 (a) shows a block diagram of a conventional receiver using direct conversion architecture. The analog-front-end of the receiver consists of RF band-pass filter, low-noise amplifier (LNA), mixer, baseband channel selection filter (CSF), and variable-gain amplifier (VGA). Fig. 1.3 (a) assumes that the signal located in the desired band comes into the receiver along with the out-of-band interference signal. To accept only signals of the desired band among a number of communication standards over a broad frequency spectrum, conventional receivers use the RF band-pass filter without exception. The signal received from the antenna passes through the RF band-pass filter, leaving only the desired band signal and the out-of-band interference signals are removed. The LNA located behind the filter serves to amplify the input signal in the RF band. Since the LNA of the conventional receiver is adapted to the target radio standard, the signal in the desired band is amplified but the interference signal is not amplified. The in-band signals are converted through the mixer with a sufficient signal-to-noise ratio (SNR), and channel selection and amplification are done in the baseband circuit. Since out-of-band signals have already been removed considerably, they are converted to baseband and almost disappear when passing through the filter.



(a)



(b)

Fig. 1.3 Block diagram and effect of out-of-band blocker on (a) conventional direct-conversion receiver, (b) wideband direct-conversion receiver.

Now let's check a wideband receiver that performs functions close to a practical SDR receiver. The wideband receiver described in Fig. 1.3 (b) is a more flexible system than the conventional receiver by removing the band-pass filter of the RF band and designing the LNA as a wideband circuit. After the mixer stage, the block diagram in the baseband is the same as the conventional receiver, but there is a difference in RF circuitry for wideband operation. Unlike conventional receivers, wideband receivers do not depend on any single standard and therefore accept a wide range of signals. If the in-band signal and the interference signal enters together in the conventional receiver, there is a risk that the interference signal becomes much larger than the desired signal in the wideband receiver, thereby saturating the receiver itself.

Of course, designing an RF band-pass filter of a conventional receiver as a CMOS circuit with a very flexible operation would be a good way to implement an SDR receiver. However, it is very difficult to implement this in a CMOS circuit because RF band-pass filters (e.g. surface acoustic wave filters (SAW filters)) dedicated to one standard have very high Q value and low loss characteristics. Also, to be an SDR receiver, it is necessary to design a flexible filter circuit that can be reconfigured over a wide bandwidth, which is a goal that cannot be achieved with small die area and low cost.

In the above case, the most problematic in the wideband receiver architecture is the out-of-band interference signal, or blocker. The problem that the blocker can cause in the receiver is

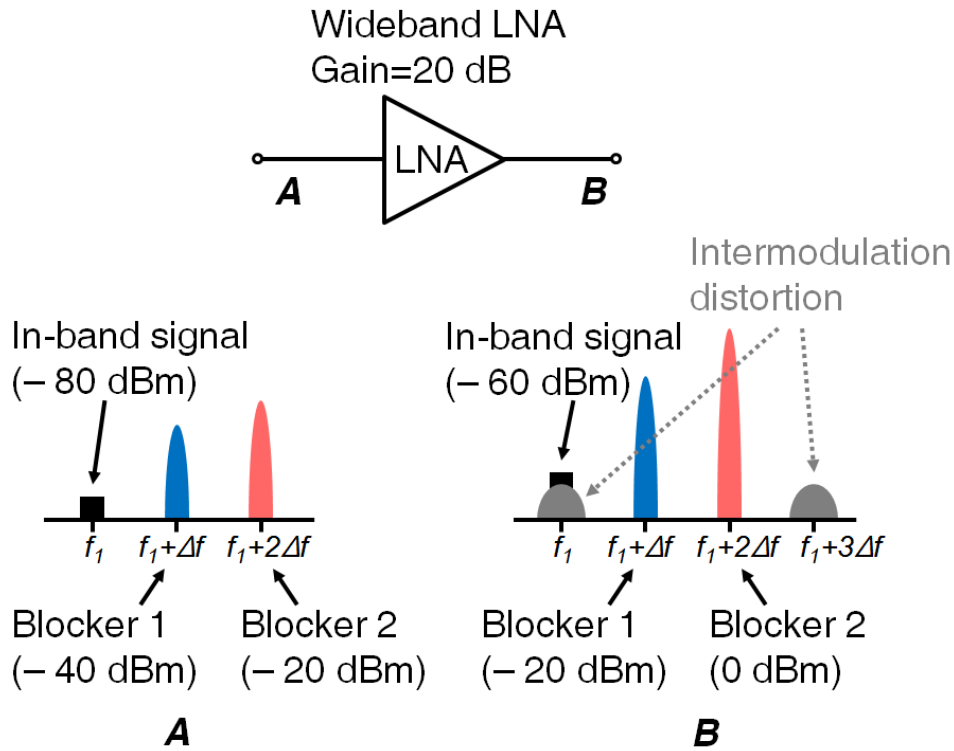


Fig. 1.4 Intermodulation distortion due to the multiple blockers in wideband receiver.

as follows: First, 1) when the blocker of a large power is applied to the LNA, so that the LNA may saturate and the noise performance may deteriorate. If a blocker signal with a magnitude of 0 dBm (0.63 V_{pp}) is applied, the magnitude of the LNA output is about 3.56 V_{pp} when the gain of the LNA is about 15 dB, which exceeds the magnitude of VDD achievable in modern CMOS deep submicron process do. Secondly, 2) if a desired signal of a relatively small magnitude enters, the desired signal may be buried in the blocker,

thereby making it invisible. A large blocker signal can degrade the sensitivity of the receiver itself, thus causing the possibility of disturbing the desired signal slightly over the noise floor. Finally, 3) unwanted spurs may occur in the in-band due to intermodulation components generated by multiple blocker signals [8]. This is about the linearity of the receiver. If the linearity of the receiver is not good enough, intermodulation components due to the large blocker signals may be generated and distort the in-band signal. This situation is shown in Fig. 1.4. Suppose that the desired signal is located at frequency f_1 and the two blocker signals *blocker1* and *blocker2* are Δf and $2\Delta f$ apart, respectively. Since the LNA operates at a wide bandwidth, all three signals are amplified with the same gain. At this time, if the linearity of the LNA is not sufficiently good, the two blocker signals generate modulated signals, and these intermodulation components overlap with the desired signal, causing problems.

In order to solve the problems caused by the blocker, the target to be achieved by the wideband receiver can be summarized as follows.

1) Maintain proper gain and low noise figure over wideband. Since a wideband receiver basically needs to receive and process signals over a wide frequency range, this is the most basic goal to achieve as a wideband receiver.

2) The wideband receiver should be tolerant to out-of-band blocker signals. As described above, the receiver must prevent

saturation of the circuits by the blocker signal and minimize the generation of intermodulation components caused by the blockers. Thus, the receiver should keep the gain and noise figure performance degradation due to the blocker signal small, and maintain high linearity.

In the next section, we will review various methods that have been tried to remove the blocker in the wideband receiver.

1.3. Prior Researches

So far, there have been many attempts to implement an SDR receiver. In this section, we will discuss the structure of the wideband receivers studied and the methods of removing the blockers. Of course, there are examples of achieving a multi-mode multi-band receiver using several RF filters and dedicated LNAs to support a couple of standards [9]. However, the goal of this thesis is to exclude off-chip devices as much as possible and to implement practical SDR using system-on-a-chip (SoC), so this method is outside the scope of this thesis. The ways to design a filter block using a CMOS circuit, or to propose a receiver structure and remove a blocker are summarized into three categories.

The first is to use a circuit called an N-path filter as a reconfigurable band-pass filter. This circuit has a simple structure consisting of metal oxide semiconductor field-effect transistors (MOSFETs) and capacitors, and serves to attenuate the blocker in the RF band. The second method is feed-forward blocker filtering, which proposes the structure that separates the blocker signals in two paths and then combines them in opposite phases. Finally, we will introduce the current-mode receiver architecture. This method improves the vulnerability of the LNA that can be saturated by the blocker, and uses a voltage-current conversion circuit instead of the conventional voltage amplification LNA. A detailed description of each method and previous research findings will be presented.

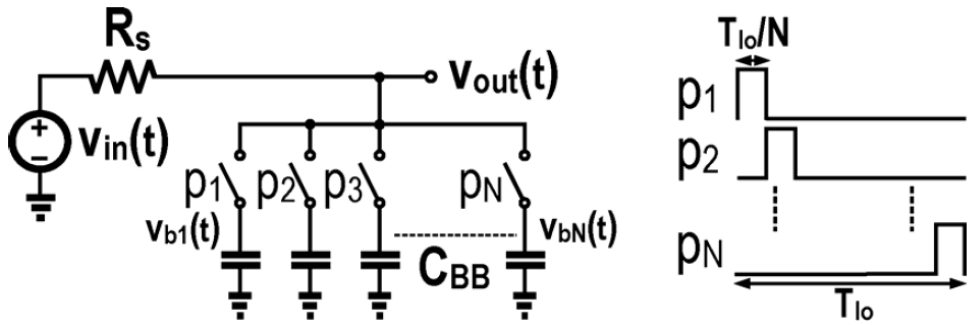


Fig. 1.5 A general N-path filter with its required non-overlapping clocks..

1.3.1. N-Path Filter

N-path filters have been studied as one of the methods for removing blocker signals [10] – [24]. The N-path filter is a research result to replace the existing SAW filter. This is a type of periodic time-varying system, one that can be reconfigured without using inductors. Fig. 1.5 shows an example of an N-path filter [21]. The filter consists of N switches and N capacitors and is operated by clock signals with N non-overlapping phases. If the period of the entire clock signal is T, the signal for operating the individual switches is turned on for T/N. The frequency response of this network appears as the response of a low-pass filter around a signal with a frequency of $1/T$. As a result, it is possible to implement a tunable filter in which the center frequency is changed

by varying the period of the clock signal. The frequency response translates the low-pass response seen by the capacitor near DC to the center frequency *1/T*, allowing a filter with a very high Q value in the RF band.

The first N-path filter was developed in the 1960s [10], but due to process limitations, the operating frequency was only a few kHz. With the recent development of CMOS processes, high-speed operation and low loss circuits have been developed, the N-path filter has begun to attract attention and is being used as a variable filter capable of operating at high frequencies (over 1 GHz).

Although the N-path filter shows possibility as a promising variable filter, there are also disadvantages. One of the major problems with N-path filters is the attenuation characteristics. Since the MOSFET used as a switch in the filter cannot have a resistance value of zero, the attenuation of the filter is limited to about 15 dB [17]. The existence of the resistance value means that there is a loss, so there is a problem that the noise figure is degraded by the N-path filter. This cannot be ignored given the fact that the N-path filter is usually located in front of the LNA to remove the blocker. This is because the circuit located in front of the analog-front-end has a large effect on the noise figure of the entire system.

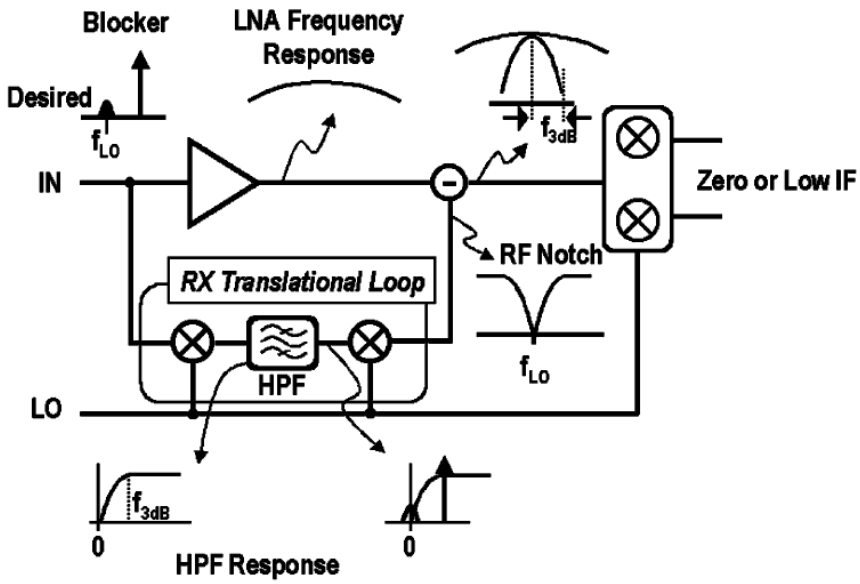


Fig. 1.6 Block diagram of the feed-forward blocker filtering receiver.

1.3.2. Feed-Forward Blocker Filtering

One of the proposed methods to remove the out-of-band blocker signal is to cancel the blocker by using a feed-forward structure [25] - [30]. This method is also called translational filtering. Instead of designing a circuit block like a N-path filter, this method uses a receiver structure to remove the blocker. The feed-forward type receiver provides two signal paths. The main path performs amplification using the LNA as in the conventional method. In the auxiliary path, the in-band signal and the blocker are

downconverted into the baseband together by a mixer, and only the in-band signal is removed using the filter in the baseband, leaving a blocker. This baseband signal, which is left only a blocker, is upconverted to the RF band again by another mixer. When the signals of two paths are added in opposite phase to each other at the output node of the LNA, only the in-band signal is left. These systems have the advantage of avoiding compression even when a large blocker signal of 0 dBm is received. It is possible to avoid filtering in the RF band requiring a high Q value, and the blocker can be removed with a baseband filter that is simpler in design than the RF bandpass filter. However, as shown in the block diagram of Fig. 1.6, this method complicates the circuit configuration. For a large attenuation of the blocker, all circuit building blocks must have high linearity and low noise figure. Therefore, this type of circuit is difficult to achieve a low noise figure, and wideband characteristics are also difficult to achieve.

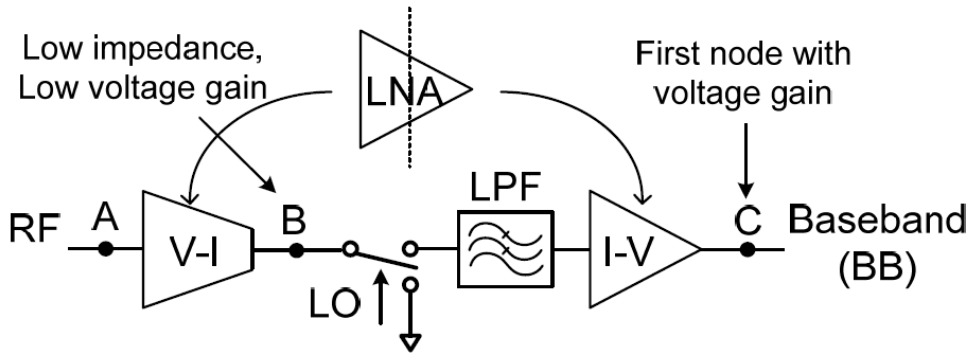


Fig. 1.7 Conceptual diagram of the current-mode receiver.

1.3.3. Current-Mode Receiver

Traditionally, the analog-front-end of a narrowband receiver can provide sufficient linearity (typically, IIP3 < 0 dBm) for an in-band blocker using an LNA and a mixer, and an RF band-pass filter removes the out-of-band blocker. However, because out-of-band blocker is much stronger than in-band blocker in wideband receivers, the required out-band IIP3 is much higher than in-band IIP3 and receiver may be desensitized due to the very large blocker. Therefore, a reconfigurable band-pass filter might be a solution, but it is difficult to provide sufficient noise figure, linearity and good selectivity simultaneously using a CMOS on-chip filter. Let's solve the problem with another receiver structure here.

Amplification is essential at the beginning of the receiver chain

to ensure low noise figure. Consider the voltage amplification in a typical LNA divided into two stages: V−I conversion and I−V conversion. The V−I conversion can be seen as converting the input of the LNA into a current through the transconductance of the transistor. The I−V conversion can also be thought of as the conversion to a voltage through the output impedance or transimpedance of the LNA. Fig. 1.7 shows two functional blocks, V−I and I−V, separated by a passive mixer and a low−pass filter inserted between them. Mixers and filters have no voltage swing internally. Therefore, even if a large blocker signal is applied, the LNA is not saturated. This circuit structure is called the current−mode receiver [31]−[46].

An important part of the current−mode receiver is to provide a low impedance across the output of the RF amplification stage, node *B*, over a wide band. This is to suppress voltage amplification from occurring in the RF band, so the voltage gain first occurs in the baseband. This provides selectivity to mitigate the blocker.

The realization of the general concept (Fig. 1.7) is shown in Fig. 1.8. The current−mode receiver completely removes the voltage gain LNA prior to the mixer and uses the low−noise transconductance amplifier(LNTA) as the first RF stage for V−I conversion. As mentioned above, it is important to maintain a low impedance at the node *B* over a wide band. Passive mixers using transistors as switches can achieve low resistance values. In Fig. 1.8, a transimpedance amplifier(TIA) is used as the baseband I−V

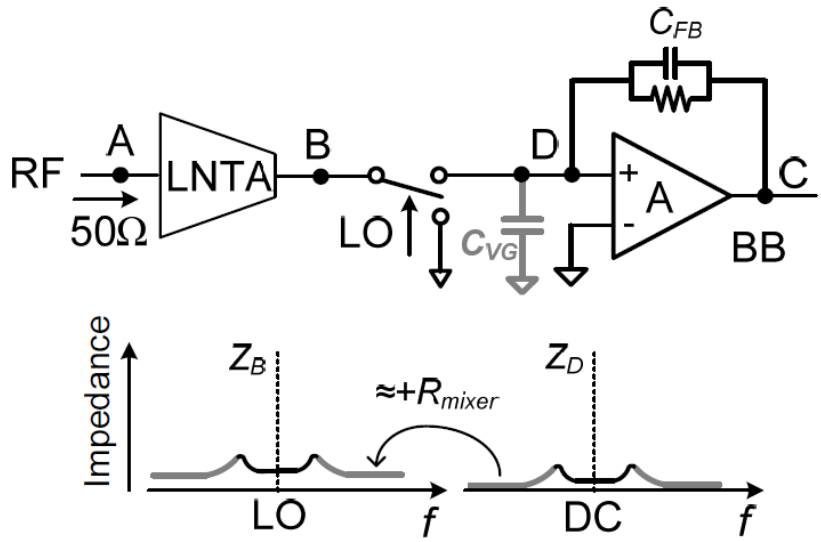


Fig. 1.8 Realization of the low-pass blocker filtering and illustration of the impedance transfer effect (from Z_D to Z_B).

conversion circuit. A feedback circuit consisting of a resistor and a capacitor in parallel in the amplifier acts as a low-pass filter. The blocker is attenuated by a low-pass filter, and the current-mode receiver is a circuit that can withstand the large blocker.

Let's summarize the results of previous studies. The N-path filter is advantageous in that it can reconfigure a high Q-value band-pass filter. However, its application is limited due to the performance limitations of the circuit itself and it degrades the noise figure performance of the entire receiver. In the case of the feed-forward technique, all the circuit blocks constituting the entire system must operate at high performance, and efforts for perfect

cancellation are required. On the other hand, the current-mode receiver can achieve blocker removal using a relatively simple structure. In this thesis, we study LNTA, mixer, and baseband I-V conversion circuit which constitute current-mode receiver and aim to make receiver strong to blocker by increasing noise figure and linearity of whole receiver.

1.4. Research Objectives and Thesis Organization

As can be seen in the previous section, there have been a wide variety of ways to remove blockers from wideband receivers in an attempt to implement a practical SDR system. Each of these methods has shown promising results to speed up the implementation of SDR receivers. However, high-performance, low-cost receivers that can be implemented with SoC still have a long way to go. Based on the results from the previous chapter, we will focus on current-mode receivers in this thesis. The research objectives of the wideband current-mode receiver to be covered in this thesis are as follows.

In this thesis, we will design a current-mode receiver that maintains a reasonable gain (over 40 dB) and a low noise figure (less than 10 dB) over a wide bandwidth (60 MHz – 3 GHz).

A wideband receiver that can achieve an IIP3 value of 0 dBm or better will be designed to have blocker-tolerant characteristic. The high IIP3 value signifies the system is resistant to the blocker signals.

The development process is as follows.

Chapter 2 discusses the fundamental causes of the intermodulation components occurring in transconductance amplifiers. A linearization technique of a general transconductance amplifier will be proposed to suppress the generation of intermodulation components. The effectiveness of linearization

method will be certified by designing and demonstrating the result by a linearized G_m−C filter. Based on the design insensitive to process variations, we will draw a basic sketch of the LNTA of a wideband receiver.

In Chapter 3, the linearization technique developed in Chapter 2 will be applied to the LNTA. The proposed linearization method will be improved to achieve a low noise figure. Then, a wideband receiver system with noise cancellation techniques will be proposed. We will design a receiver that can operate in dual mode in high−linearity mode or low−noise mode, and the measurement results will be shown.

Chapter 4 proposes a high performance wideband receiver by further improving the noise−cancelling wideband receiver proposed in Chapter 3. The LNTA designed in Chapter 3 will be modified to have better noise performance by changing the G_m ratio and applying RF noise cancelling technique. The wideband receiver front−end with double noise cancelling architecture will be introduced. The design procedure and measurement results will be described.

Finally, Section 5 presents conclusions and summarizes the implications and results of this thesis.

Chapter 2. Transconductor Linearization Technique and Design of Tunable High-pass Filter

The demand for highly linear circuits to support various wireless communication standards is increasing. To process in-band signals and prevent such signals from being disturbed by unwanted blockers or interferers, the receiver front-end must consist of circuits with high linearity. In the current-mode wideband receiver, the block closest to the input signal is the LNTA, and the linearity of the LNTA should be very good since this receiver cannot use an external band-pass filter. Therefore, in this chapter, the method of improving the linearity of transconductance amplifiers will be studied.

To enhance linearity, the multiple-gated transistors (MGTR) method is widely used [48], [49]. This technique uses two or more parallel transistors with different gate widths and gate bias voltages to cancel the third-order derivative (g_{m3}) of the transistor. The IIP3 value of the transistor improves, where the g_{m3} value is close to zero. However, the MGTR method has drawbacks in that the linearity improvement is achieved by a precise bias voltage adjustment. To cancel the g_{m3} component, the gate width and gate bias must be controlled to find the optimum operation point, which means the MGTR method is sensitive to bias variations.

Linearity improvements can also be achieved using the feed forward method [50], in which two paths are used to actively cancel the nonlinearity. In addition, it requires accurate scaling between the input signals of the main and auxiliary paths to perform exact cancellation. However, the circuits that generate the scaled inputs for both paths are not shown in [50].

A method of attenuation-predistortion in [51] also uses two paths for the linearization. In this architecture, an attenuated input signal is required for the auxiliary path, and a digitally controlled phase shifter is needed to compensate the mismatches and the process-voltage-temperature (PVT) variations.

In this chapter, we will achieve linearization of the transconductors in a feed-forward fashion using two paths. And the linearity performance of the proposed transconductor circuit will be verified through the design of the filter. If the circuits are cascaded, the nonlinearity components of the latter stages become more critical [47]. Therefore, the input-referred third-order intercept point (IIP3) performance of the latter stages plays an important role in the linearity of the overall system. Since the filters for channel selection or rejection are usually located in the last stage of the receiver front-end, the design of a high-performance intermediate frequency (IF) or baseband filters is necessary. So, a G_m-C filter [53]-[55] will be designed for evaluating the linearization method. Although it has lower linearity than active-RC filter [52], it can be tuned continuously by changing the bias

current.

In this chapter, a linearization technique of the transconductor circuit is proposed. The proposed technique is based on the feed forward method, and it actively cancels the G_{m3} component of the transconductor, which is the main contributor to the nonlinear V−I conversion. This technique is explained in section 2.1. In section 2.2, a tunable G_m−C high−pass filter design adopting linearized transconductor circuits is presented. Section 2.3 deals with the measurement results of the fabricated filter circuit, and section 2.4 concludes the chapter.

2.1. Transconductor Linearization Technique

In MOSFET devices, the drain current I_d can be expressed with Taylor expansions, as follows:

$$I_d = g_{m1}V_{gs} + g_{m2}V_{gs}^2 + g_{m3}V_{gs}^3 + \cdots. \quad (2.1)$$

where V_{gs} is the gate-to-source voltage of the device, and g_{mn} is the n-th order derivatives of the drain current I_d with V_{gs}. Like a MOSFET device, a transconductor circuit can be modeled using the same expression. The output current of the circuit consists of a polynomial of the input voltage V_{in} and the transconductance G_m, which becomes:

$$I_{out} = G_{m1}V_{in} + G_{m2}V_{in}^2 + G_{m3}V_{in}^3 + \cdots. \quad (2.2)$$

To make the voltage to current conversion a linear operation, the I_{out} term must contain the components of G_{m1} and V_{in} only. Assuming that the even order coefficients can be eliminated with a differential architecture, the main contributor to nonlinearity is the G_{m3} component. Higher order components over fourth derivatives are neglected in this method. Then, a transconductor circuit can be modeled as follows:

$$I_{out} \approx G_{m1}V_{in} + G_{m3}V_{in}^3. \quad (2.3)$$

Linearization can be achieved by cancelling the G_{m3} component. The proposed transconductor linearization technique consists of two paths, as shown in Fig. 2.1. Transconductors with different G_m

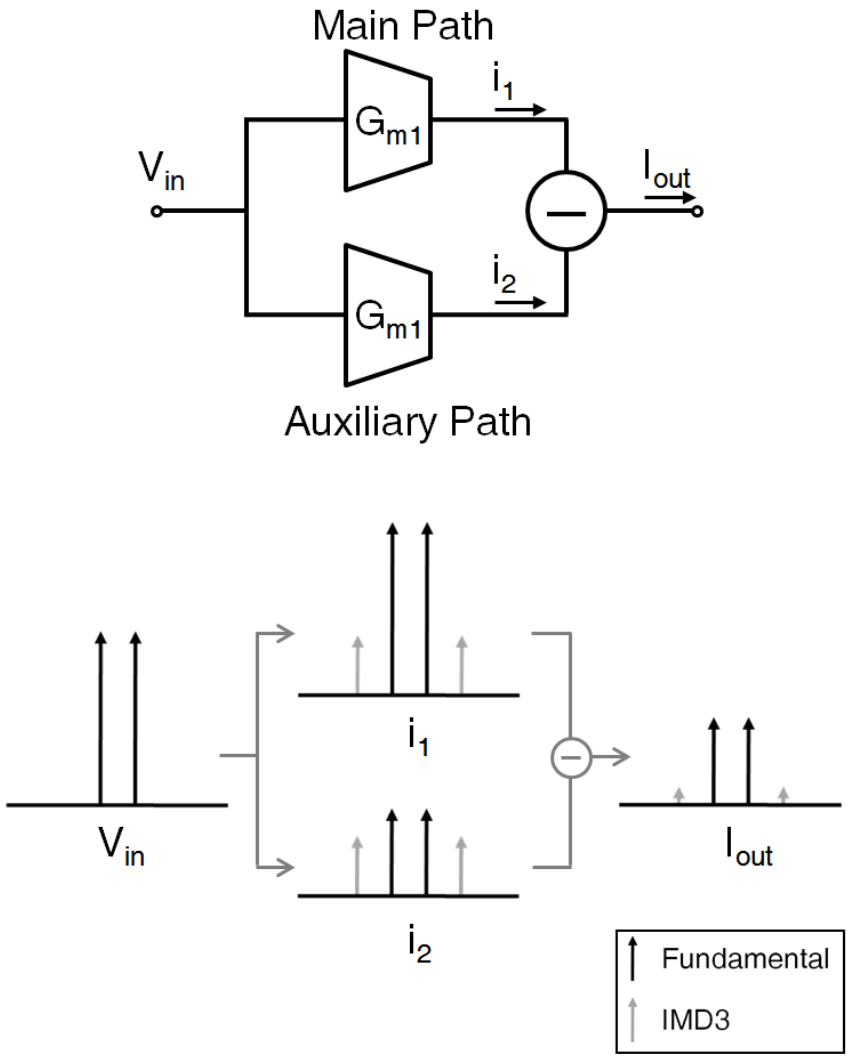


Fig. 2.1 Block diagram of the proposed transconductor linearization technique.

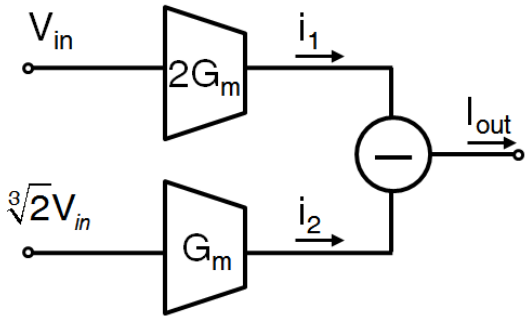
values are located in the main and auxiliary paths. The output currents i_1 and i_2 of each transconductor can be modeled with (2.3). As the third-order intermodulation distortion (IMD3) components of each path are designed to have the same magnitude, they are subtracted and eliminated in the output current I_{out}.

Fig. 2.2 shows the linearization technique with specific values. In the main path, the input voltage is V_{in}, and the transconductance is $2G_m$, which means the two-unit transconductor circuits are connected in parallel. In the auxiliary path, the input voltage to the transconductor is $(-\sqrt[3]{2}V_{in})$, and the transconductance is G_m (unit transconductor). The negative sign at the amplifier output signifies the opposite polarities at the input and the output. Due to this feed forward auxiliary path, I_{out} is given by

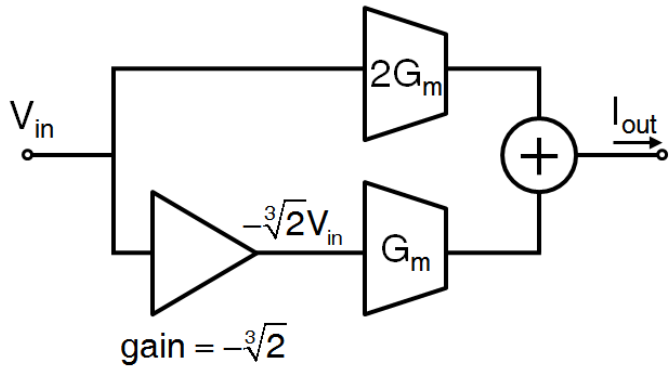
$$\begin{aligned} I_{out} &= i_1 + i_2 \\ &= 2G_{m1}V_{in} + 2G_{m3}V_{in}^3 + \left(-\sqrt[3]{2}G_{m1}V_{in} - 2G_{m3}V_{in}^3\right) \\ &= \left(2 - \sqrt[3]{2}\right)G_{m1}V_{in} \end{aligned} \qquad (2.4)$$

which means a linear V-to-I conversion is possible. The linear conversion is obtained by increasing the power consumption and reduction of transconductance $(2 - \sqrt[3]{2} \approx 0.74)$.

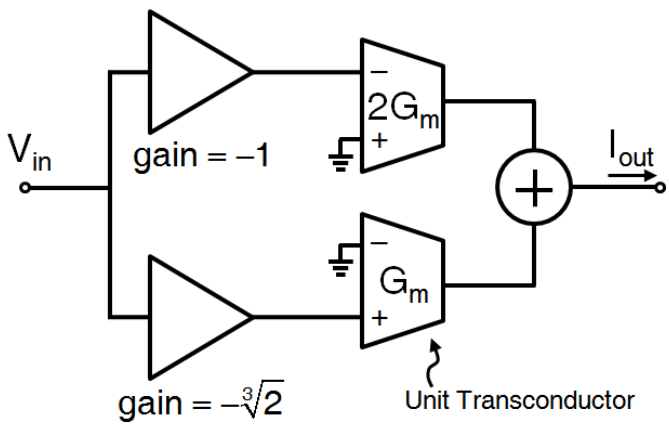
In this linearization method, input voltages of V_{in} and $(-\sqrt[3]{2}V_{in})$ must be applied to each transconductor to perfectly cancel the G_{m3} component. To obtain an input voltage of $(-\sqrt[3]{2}V_{in})$, the linear voltage amplification circuit in Fig. 2.3 (a) is used [56]. In [56], the voltage amplifier consists of a driving inverter and a loading



(a)



(b)



(c)

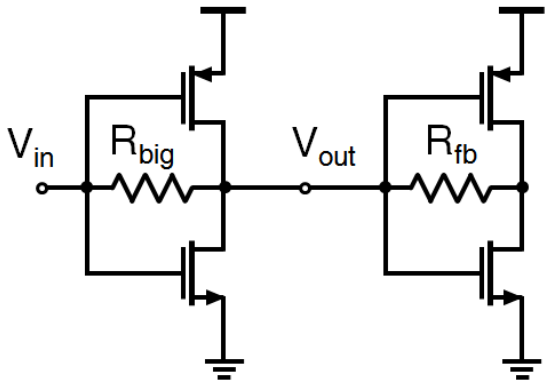
Fig. 2.2 (a) Conceptual block diagram of two−path G_{m3} cancellation. (b) Implementation of G_{m3} cancellation using a voltage amplifier. (c) Final block diagram of linearized transconductor.

inverter. This self-biased inverter-based circuit can amplify the input voltage linearly.

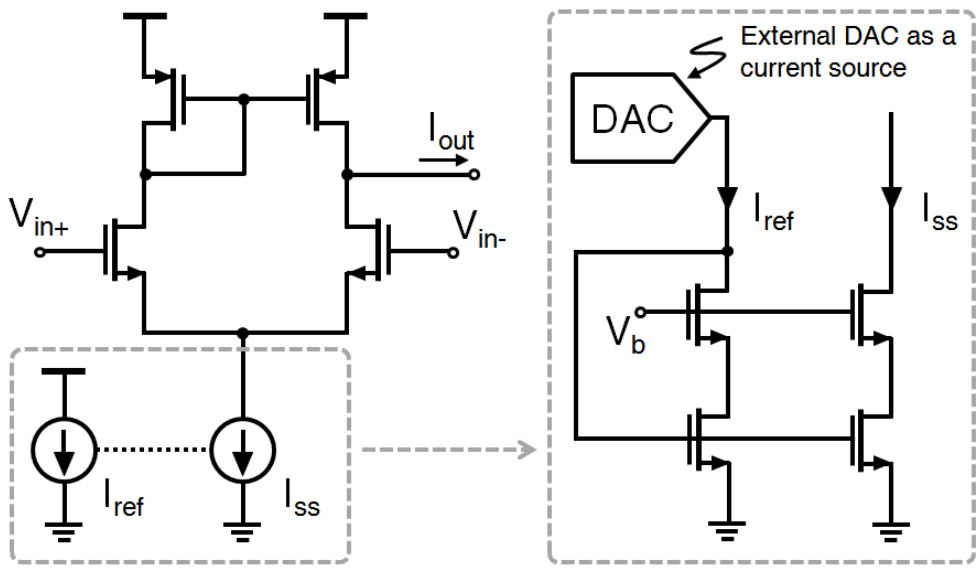
To reduce the phase mismatch of main and auxiliary paths for perfect cancellation, another linear voltage amplifier, which has gain of (-1), is inserted in the main path. The transconductor circuits with differential inputs are used to create opposite polarities in the two paths.

Fig. 2.3 (b) shows the unit transconductor circuit. A basic differential pair is used for the differential input and a current mirror load is implemented to obtain a single-ended output current. The transconductance of the circuit can be adjusted by the tail current, which mirrors the current of an external reference current source.

Since the active G_{m3} cancelling architecture does not alter the original transconductor circuit, this technique can easily be applied to conventional transconductors with differential inputs. In addition, this linearization technique is independent of the bias variations of the transconductor. As reported in [56], the gain of the linear voltage amplifier is defined by the G_m of the inverters and R_{fb}. Therefore, the ratio of the two paths is insensitive to the bias voltages, which means that any value of the G_{m3} component can be eliminated, while the main and auxiliary paths maintain a voltage amplification ratio of $1 : \sqrt[3]{2}$. Fig. 3.4 shows the simulation result of the voltage amplifiers in the two paths. The ratio of the two paths holds up to the input power of -20 dBm, and the gain error reaches



(a)



(b)

Fig. 2.3 (a) Schematic of a linear voltage amplifier. (b) Schematic of a unit transconductor circuit.

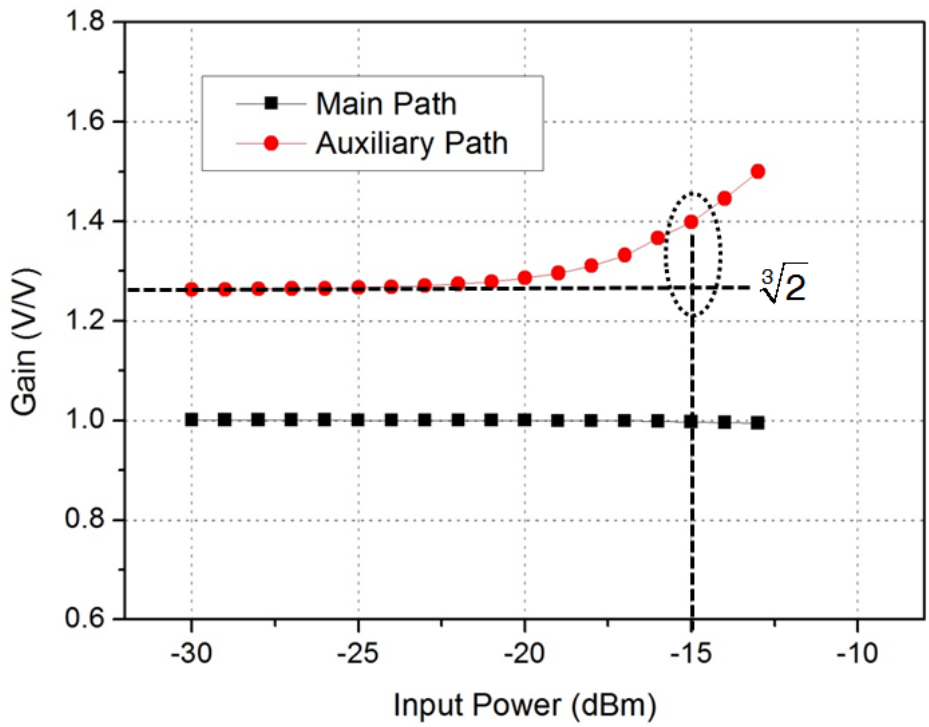


Fig. 2.4 Simulated gain of main and auxiliary paths.

10 % when the input power is −15 dBm. This result demonstrates that G_{m3} cancellation can be performed up to the input power of −15 dBm with small errors.

The linearity of the voltage amplifier is critical for the G_{m3} cancellation. Fig. 2.5 presents the two-tone linearity simulation result of the voltage amplifier. The IIP3 of 20.4 dBm shows highly linear operation of the amplifier.

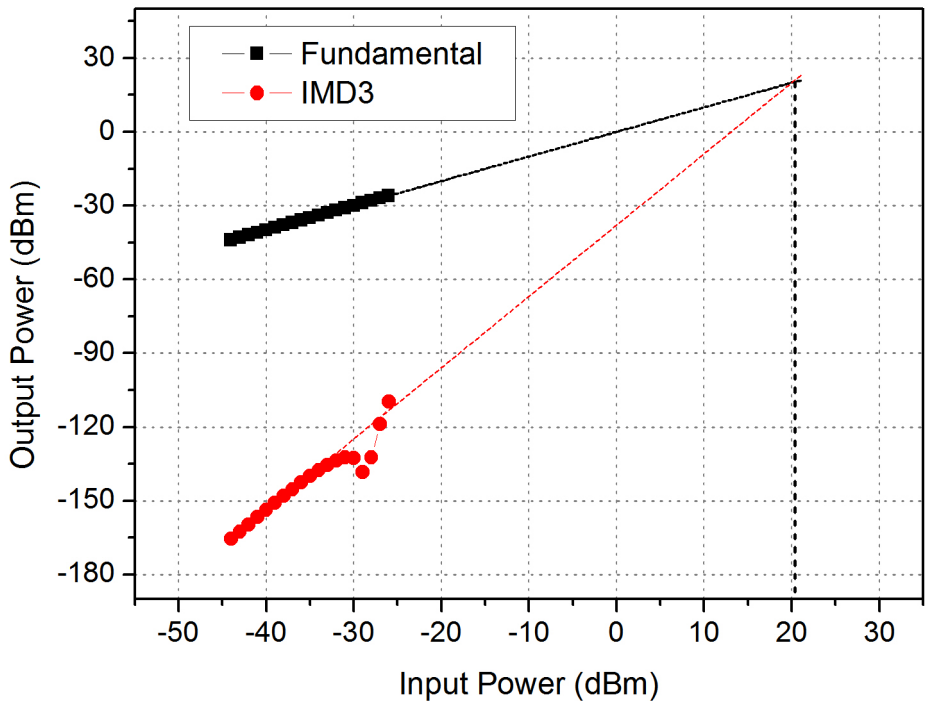


Fig. 2.5 Simulated IIP3 of the voltage amplifier.

The G_{m3} cancellation simulation between unit transconductor and the linearized transconductor is shown in Fig. 2.6. Equal input voltages of 2.5 MHz and 3 MHz are applied to the transconductors, and the output current of each circuit is plotted in dB scale to verify the proposed technique. The result shows IMD3 component of output current at 3.5 MHz is reduced by 38 dB due to the linearization circuit. However, the improvement of IMD3 is achieved by increasing power consumption by the factor of 5 when compared with the unit transconductor, and input referred noise power

increased by the factor of 8.2.

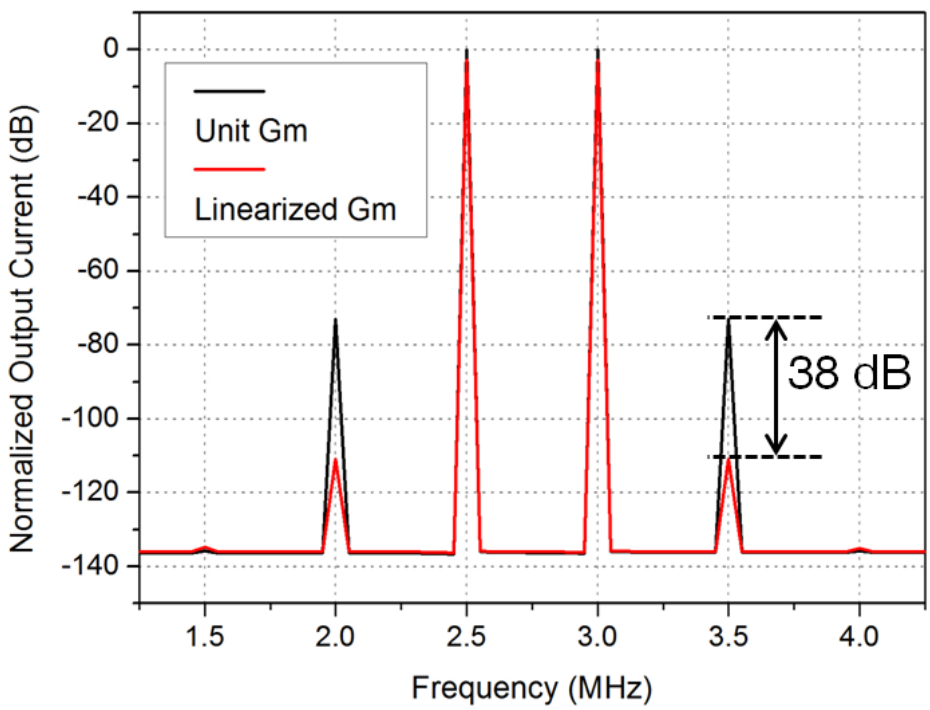


Fig. 2.6 Simulated difference in the IMD3 current between the unit transconductor and the linearized transconductor.

2.2. Design of Tunable High-pass Filter

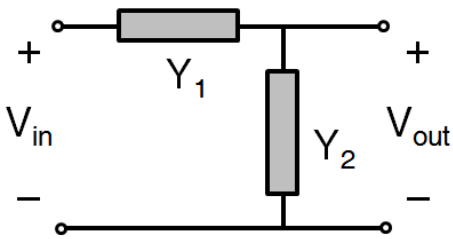
In a frequency modulated continuous wave (FMCW) radar system, the distance from the target is proportional to the baseband frequency of the system [57]. A filter is necessary in the receiver baseband of a through-the-wall FMCW radar system to reject the antenna coupling and wall-reflected waves [58] [59]. In a situation in which the target exists beyond the wall, a high-pass filter can attenuate the unwanted wall-reflected waves. The high-pass filter must have a tunable cutoff frequency, because the distance from the through-the-wall radar to the wall can vary.

A tunable G_m-C high-pass filter in [60] is designed using the linearized transconductors. This filter of order N can be synthesized using N transconductor circuits and N capacitors.

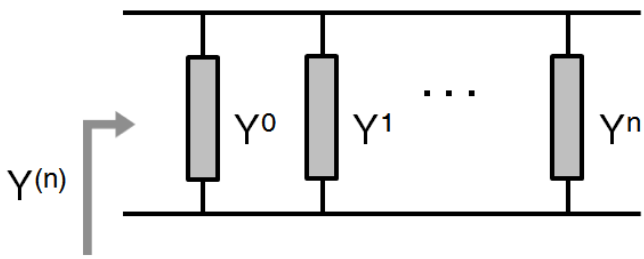
Fig. 2.7 shows the N-th order high-pass filter with high-order admittance element synthesis. The input voltage is divided into C_1 and Y_{in}, making the transfer function from input to output as follows:

$$\begin{aligned} H(s) &= \frac{V_{out}}{V_{in}} = \frac{sC_1}{sC_1 + Y_{in}(s)} \\ &= \left[s^n \Big/ \left(s^n + \frac{G_{mn}}{C_1} s^{n-1} + \frac{G_{m(n-1)}G_{mn}}{C_1 C_n} s^{n-2} \right.\right. \\ &\quad \left.\left. + \frac{G_{m(n-2)}G_{m(n-1)}G_{mn}}{C_1 C_{n-1} C_n} s^{n-3} + \cdots + \frac{G_{m1}G_{m2}\cdots G_{mn}}{C_1 C_2 \cdots C_n} \right) \right]. \end{aligned} \tag{2.5}$$

The designed high-pass filter has a unit filter order of 2 and these unit filters are cascaded to make higher orders to prevent the



(a)



(b)

Fig. 2.7 (a) High−pass filter using admittance elements. (b) High−order admittance element.

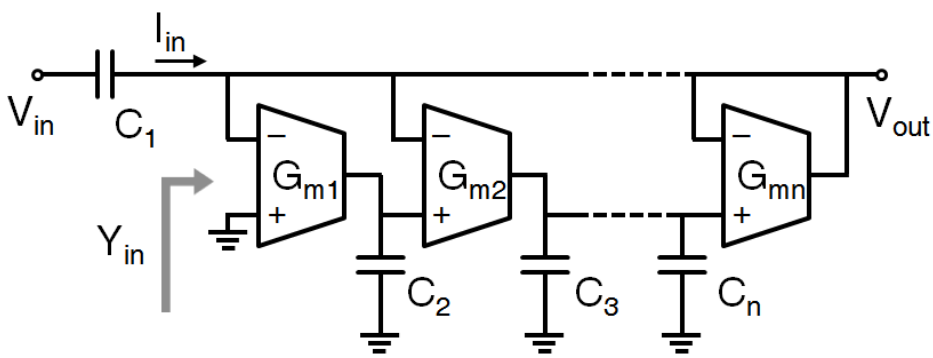


Fig. 2.8 High−pass filter using high−order admittance element synthesis.

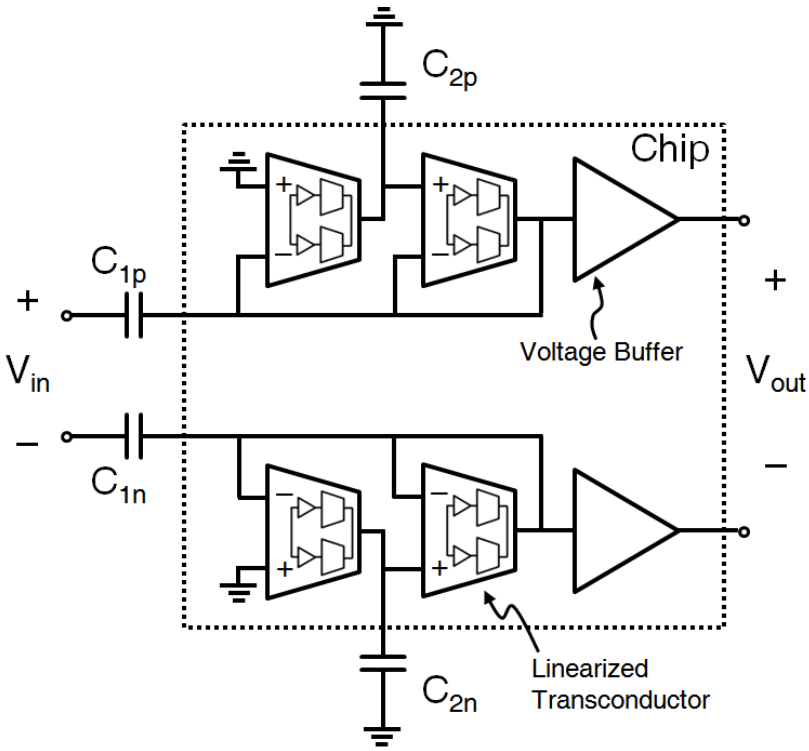
linearity degradation. The normalized transfer function of the second-order filter with the same transconductance values becomes:

$$H(s) = \frac{s^2}{s^2 + c_{21}s + c_{22}}. \quad (2.6)$$

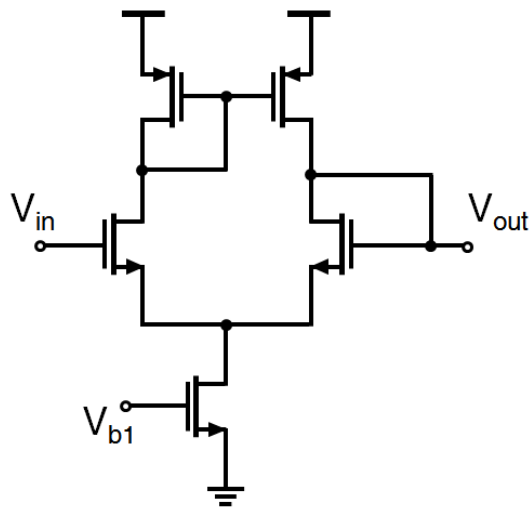
where the normalized transfer function coefficients for the Chebyshev filter response are given by: $c_{21} = G_m/C_1 = 1.1025$ and $c_{22} = G_m^2/(C_1C_2) = 1.0977$. The poles of the transfer function are located at $-0.549 \pm 0.895i$. The capacitor values of the filter are set to a cutoff frequency up to 750 kHz, thus becoming C_1 = 330 pF and C_2 = 82 pF. These capacitors are attached externally so the filter could be adjusted to another cutoff frequency range. By scaling transconductance, the frequency response of the filter is proportionally scaled, which means the filter can maintain the Chebyshev filter response at any given cutoff frequency.

The final design of the filter is implemented with differential inputs and outputs (Fig. 2.9). To avoid the effect of the load on the frequency response of the filter, a voltage buffer is placed after the filter stage.

The frequency response and the phase of high-pass filter in Fig. 2.9 are simulated and the results are plotted in Fig. 2.10. The frequency response presents the filter operation at the cutoff frequency of 250 kHz, and the phase simulation shows the filter is stable.



(a)



(b)

Fig. 2.9 (a) Block diagram of a second−order unit high−pass filter.

(b) Schematic of voltage buffer.

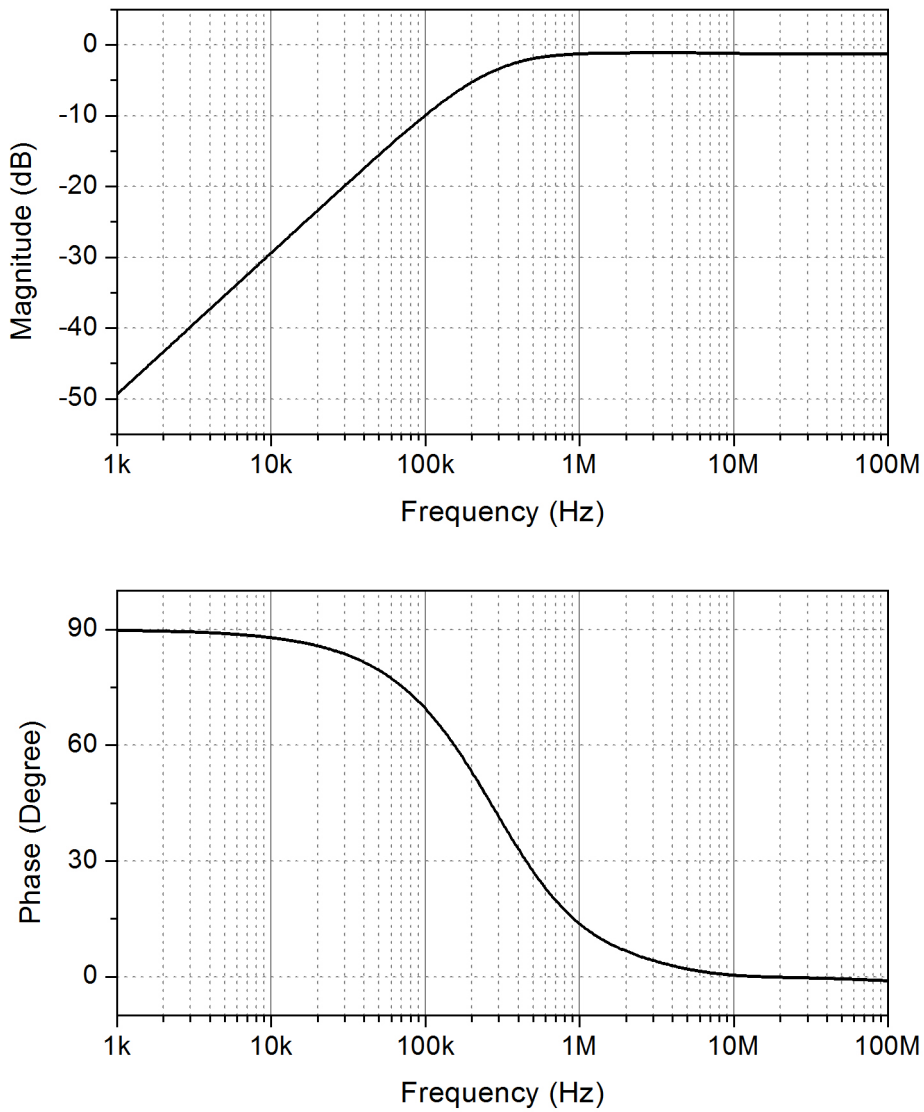


Fig. 2.10 Frequency response and phase simulation of the high-pass filter in Fig. 2.9.

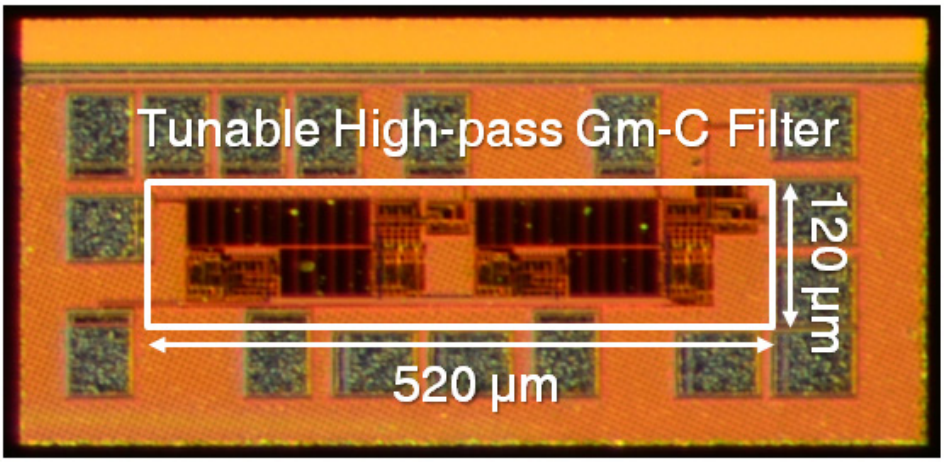


Fig. 2.11 Chip die micrograph.

2.3. Measurement Results

The proposed tunable G_m−C high−pass filter is fabricated using the standard 0.13 μm CMOS process. The whole die size is 700 μm × 270 μm, and the active area of the filter is 520 μm × 120 μm without pads. Fig. 2.11 shows the micrograph of the chip. The power consumption of the fabricated filter is from 13.2 mW to 43.2 mW when the filter bias current changes from 0 mA to 0.5 mA. The large power consumption is mainly due to the inverters in the linearization circuit, because these self−biased inverters draw a DC current when the VDD is applied. Reducing the size of the inverters in the voltage amplifier will decrease the power consumption, but the linearity of the amplifier may degrade. Moreover, the topology

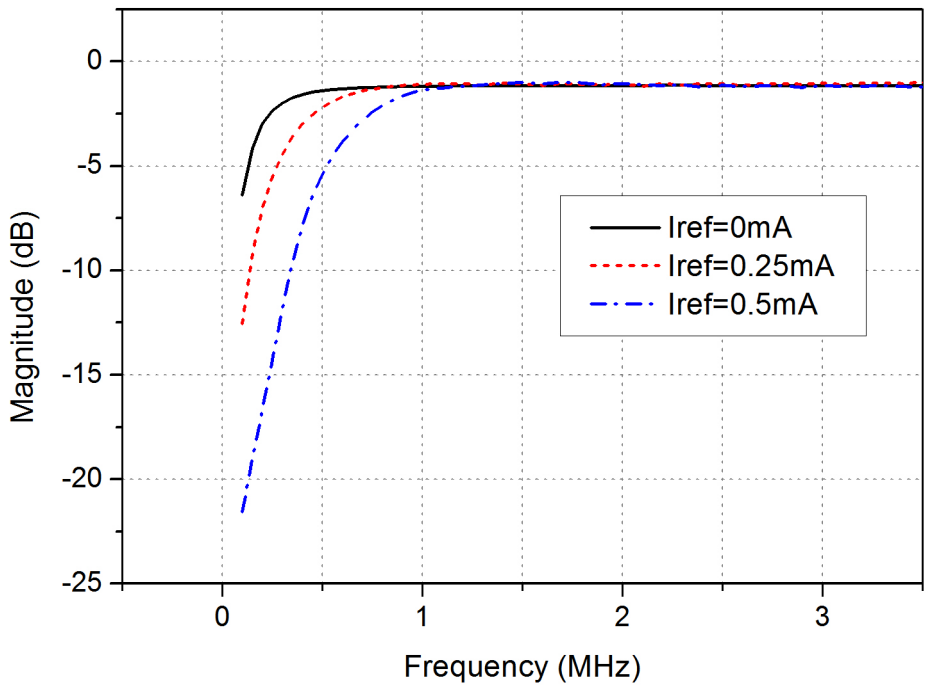


Fig. 2.12 Frequency response tuning of a high-pass filter.

of the linearization technique that uses parallel-connected transconductors also contributes to the large power consumption. If the linearization technique is not applied, the power consumption for the same bias current will be from 2.76 mW to 7.35 mW.

Fig. 2.12 shows the tunable frequency response of the filter. By changing the external reference current source, the frequency response can be adjusted continuously. The cutoff frequency of the filter can be tuned from 150 kHz to 750 kHz by the reference current from 0 mA to 0.5 mA. The filter shows the second-order

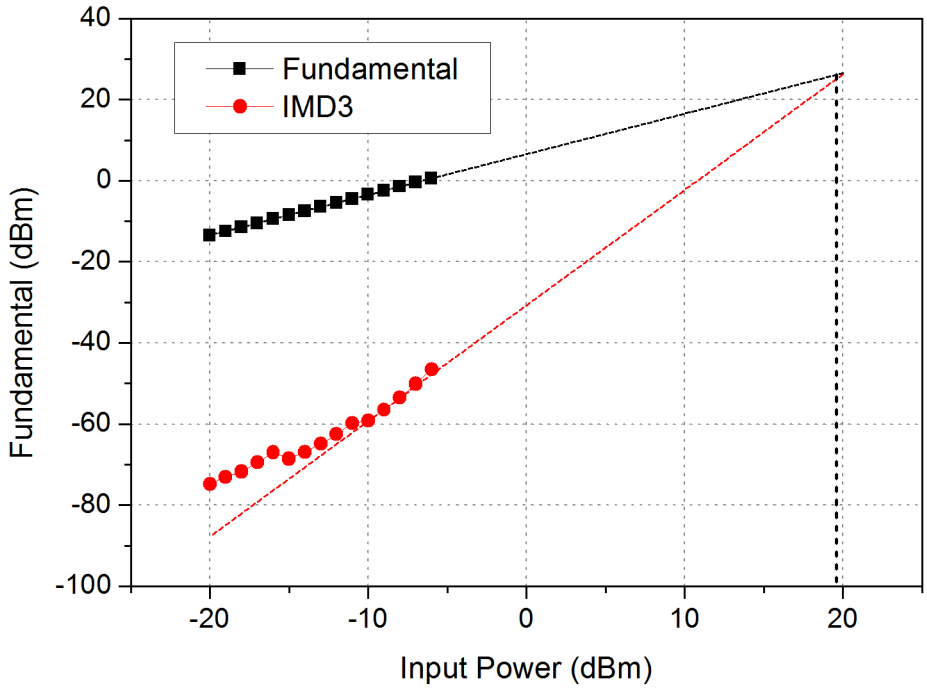


Fig. 2.13 In-band IIP3 measurement of the high-pass filter.

Chebyshev response and insertion loss of the filter is 1.1 dB. The cutoff frequency range can be extended with wide tuning of external reference current, but it requires reduction of voltage headroom of the current mirroring circuit in the unit transconductor.

Fig. 2.13 presents the in-band IIP3 measurement result of a two-tone test. Input signals of 2.5 MHz and 3 MHz tones are applied for the test, and the measured IIP3 of 19.4 dBm shows the highly linear operation of the filter, as well as proving the G_{m3} cancellation circuit works.

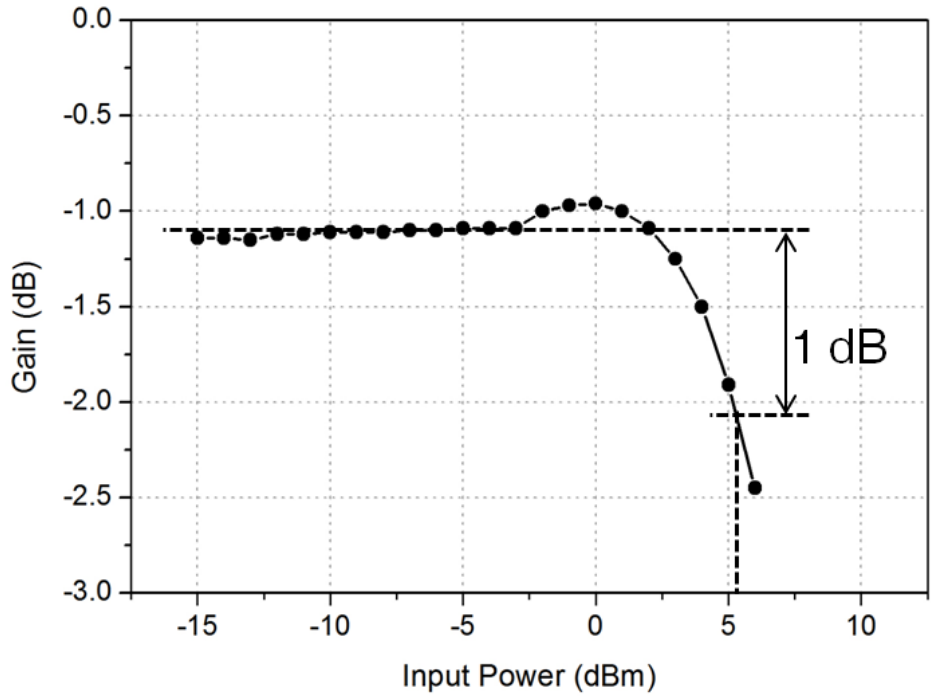


Fig. 2.14 Measurement result of 1−dB gain compression point test.

A single−tone linearity test is performed to measure the 1 dB compression point (P1dB) of the filter and shown in Fig. 2.14. The measured P1dB is at 5.35 dBm, and the gain compression mainly comes from the inverter−based amplifiers in the linearization circuit. The linear operation of the filter leads to achieving the dynamic range of the input power of 77 dB.

The filter performance is summarized and compared with prior research in Table 2.1.

TABLE 2.1
MEASUREMENT RESULTS AND PERFORMANCE COMPARISON

	[49]	[51]	[52]	This Work
Technology (μm)	0.18	0.13	0.13	0.13
Filter Topology	RC− Gm−C low−pass	Gm−C low−pass	Active Gm−RC low−pass	Gm−C high−pass
Linearization Technique	MGTR	Attenuation−Predistortion	−	Feed Forward
Supply Voltage (V)	1.8	1.2	0.55	1.2
Filter Order	3	2	4	2
Cutoff Frequency (MHz)	50−200	200	11.3	0.15−0.75
Tuning Ratio	4	−	−	5
Power Consumption (mW)	23.4	20.8	3.5	13.2−43.2
P1dB (dBm)	−	−	0.5	5.35
IIP3 (dBm)	17.3[a]	14	10	19.4

[a] Extracted value from plot

2.4. Conclusions

A linearization technique of the transconductor circuit that is based on a G_{m3} cancelling method is proposed. Using self-biased inverters and duplicated original transconductors, linearization is easily implemented. It cancels the G_{m3} component of any type of transconductor using the two-path feed forward method. The inverter-based linearization circuits are insensitive to the bias condition, and the ratio of the two input paths is accurately scaled. To demonstrate the linearization technique, a tunable G_m-C high-pass filter is implemented. The filter is synthesized using a high-order admittance element. The measurement results show a highly linear filter operation, as well as proving that the linearization technique is effective. This technique can be adapted to transconductors with differential inputs, and it has an advantage in process scaling.

Chapter 3. Wideband Noise-Cancelling Receiver Front-End Using Linearized Transconductor

As described in Chapter 1, a wideband receiver that is resistant to external blocker signals can be an alternative to a practical SDR. Let's briefly review the problem caused by the blocker. Large blocker signals may saturate the receiver circuits, or they may generate an intermodulation signal with the in-band signal. To prevent performance degradation in the wideband receiver front-end, passive mixers and low-noise transconductance amplifiers are employed, and this receiver architecture is called a current-mode receiver. The passive mixer is suitable for the wideband receiver since it has high linearity, and the LNTA can suppress the voltage gain at RF to prevent the circuits from being saturated.

If a blocker exists, the linearity of the receiver becomes more important. When the blocker and the in-band signal are intermodulated, the intermodulation distortion arises. The amount of third-order intermodulation distortion components can be represented as an IIP3 value. To suppress the IMD3 and achieve high linearity performance, a linearization technique introduced in Chapter 2 is adopted to the LNTA. Linearity can be increased by this technique, but additional circuits for linearization degrade the noise performance of the receiver. Therefore, a noise-cancelling

technique [44], [61] [62] is used to reduce the noise.

In this chapter, the wideband receiver front-end is designed using the linearization technique described in Chapter 2. Firstly, the linearized transconductor developed in Chapter 2 will be modified to have better noise performance in Section 3.1. The noise-cancelling current-mode receiver architecture, including the linearized LNTA, is explained in Section 3.2. In Section 3.3, the measurement results of the fabricated circuit are presented. Section 3.4 concludes the chapter.

3.1. Low-Noise Transconductance Amplifier Based on Linearized Transconductor

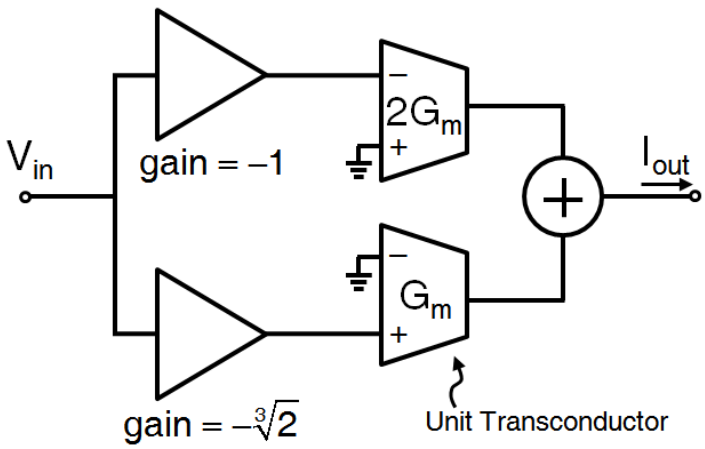
The linearization technique of the transconductors studied in Chapter 2 has confirmed that the elimination of the IMD3 component significantly enhances the IIP3 value of the transconductor circuit. In this chapter, we analyze the noise performance of a linearized transconductor circuit and discuss how to apply an existing circuit as a low-noise transconductance amplifier.

As defined in [47], the noise performance of a circuit can be represented using a noise factor (NF) as an indicator. NF can be calculated by dividing the output noise of the entire circuit by the gain of the circuit, which can be expressed as follows:

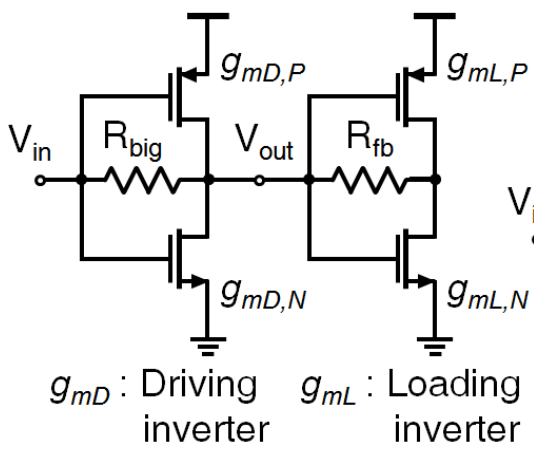
$$NF = \frac{1}{4kTR_s} \cdot \frac{\overline{V_{n,out}^2}}{A_0^2} = 1 + \frac{\overline{V_{n,in}^2}}{4kTR_s}, \tag{3.1}$$

$$NF|_{dB} = 10\log(NF), \tag{3.2}$$

where $\overline{V_{n,out}^2}$ represents the output noise of the entire circuit and includes both circuit noise and source impedance Rs, and $\overline{V_{n,in}^2}$ is the sum of input-referred noise of the circuit and the noise from the source impedance. A_0 is the gain of the circuit, which means the gain from the source to the output node. k denotes the Boltzmann constant and T is the absolute temperature. $NF|_{dB}$ represents the



(a)



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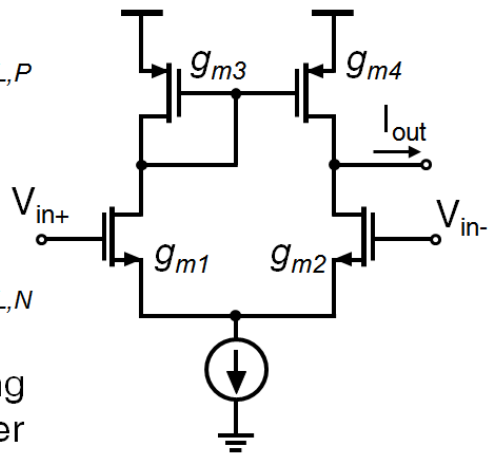


(c)

Fig. 3.1 (a) Block diagram of the linearized transconductor. (b) Schematic of the voltage amplifier and (c) unit transconductor circuit.

noise figure, which expresses the NF in decibels.

Fig. 3.1 (a) shows a block diagram of the linearized transconductor designed in Chapter 2. Fig. 3.1 (b) and 3.1 (c) show the block diagram of the voltage amplifier and the unit transconductor, respectively. The total noise performance of the linearized transconductor circuit is calculated by calculating the noise of each block as follows. First, the input-referred noise of the voltage amplifier of Fig. 3.1 (b) can be derived:

$$\overline{V_{in,amp}^{\ 2}} = \frac{4kT\gamma}{g_{mD}}\left(1+\frac{g_{mL}}{g_{mD}}\right), \tag{3.3}$$

where g_{mD} is the transconductance of the driving inverter, the first stage of the amplifier, and g_{mL} is the transconductance of the second stage, loading amplifier. γ is the excess noise coefficient, which depends on the CMOS process. Since the gain of the voltage amplifier can be expressed by

$$A_{v,amp} = \frac{g_{mD}}{g_{mL}}, \tag{3.4}$$

the equation (3.3) can be expressed as follows :

$$\overline{V_{in,amp}^{\ 2}} = \frac{4kT\gamma}{g_{mD}}\left(1+\frac{1}{A_{v,amp}}\right). \tag{3.5}$$

Next, the input-referred noise equation of the unit transconductor of Fig. 3.1 (c) is derived as follows:

$$\overline{V_{in,unitGm}^{\ 2}} = 8kT\gamma\left(\frac{1}{g_{m1}}+\frac{g_{m3}}{g_{m1}^2}\right). \tag{3.6}$$

The transconductance values of $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$ are

assumed. Using the above results, the input noise of the linearized transconductor of Fig. 3.1 (a) is calculated as

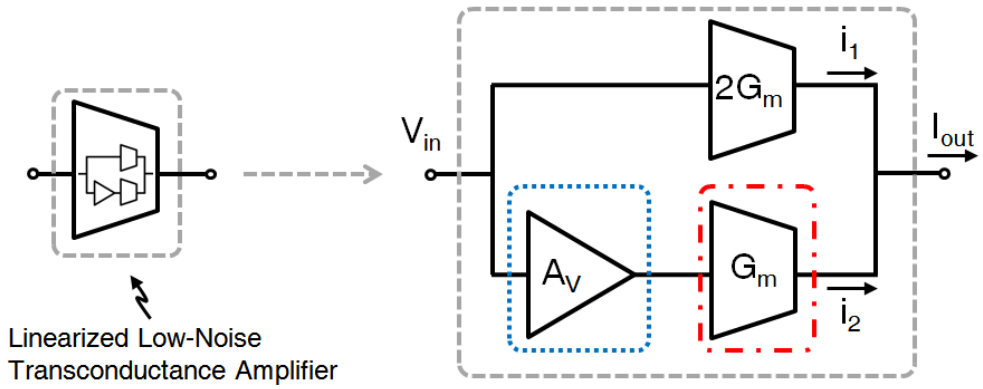
$$\overline{V_{in,Lin.Gm}{}^2} = \frac{4kT\gamma}{(2-\sqrt[3]{2})^2}\left\{\frac{3}{G_m^3}\left(1+\frac{g_{m3}}{G_m}\right)+\frac{1}{g_{mL}}\left(\sqrt[3]{2}+9\right)\right\}, \qquad (3.7)$$

where G_m is the transconductance of the unit transconductor (same as g_{m1}), and g_{m3} is the transconductance of the transistor consisting the active current mirror of the unit transconductor. Thus, the NF of linearized transconductor can be expressed as

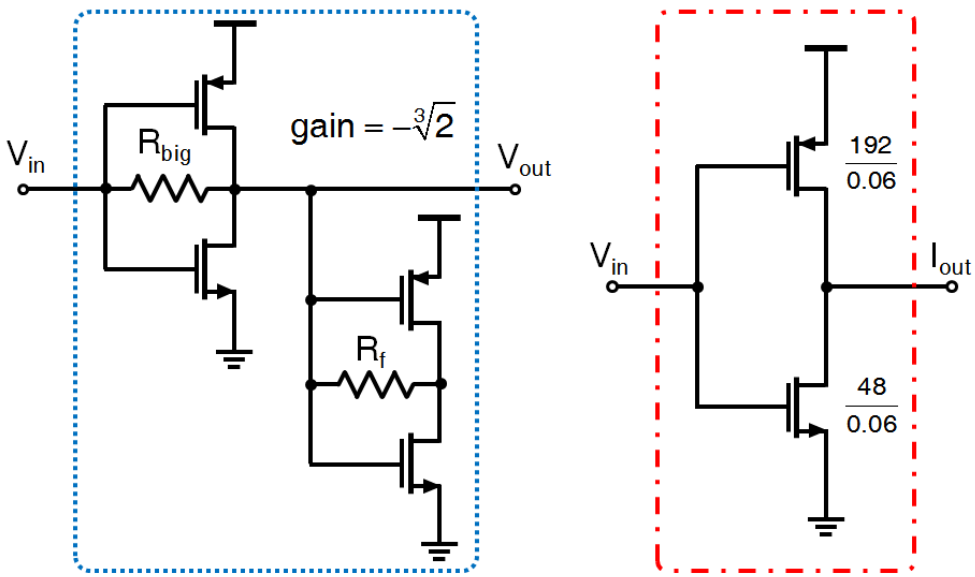
$$NF|_{Lin.Gm} = 1+\frac{\gamma}{(2-\sqrt[3]{2})^2 R_s}\left\{\frac{3}{G_m^3}\left(1+\frac{g_{m3}}{G_m}\right)+\frac{1}{g_{mL}}\left(\sqrt[3]{2}+9\right)\right\}. \qquad (3.8)$$

As can be seen from the above equation, the linearized transconductors of Chapter 2 have a very poor noise figure. In addition, since the unit transconductor is designed based on a differential pair, it is difficult to operate up to a high frequency due to a parasitic capacitors. In order to solve these problems and apply the linearization technique of transconductor to low-noise transconductance amplifier of RF band, the circuit as shown in Fig. 3.2 is proposed.

The modified linearized transconductor circuit consists of a voltage amplifier and a unit transconductor as in the previous circuit. The voltage amplifier uses the same circuit as before, but the unit transconductor circuit is designed as a simple inverter. A simple inverter circuit consists of two MOSFETs of NMOS and PMOS, and this simple structure allows the inverter to operate at high frequency with minimal performance degradation. In addition, the



(a)



(b) (c)

Fig. 3.2 (a) Block diagram of the linearized low-noise transconductance amplifier. (b) Schematic of the voltage amplifier, and (c) the unit transconductor.

inverter circuit has a very low noise figure, making it a suitable circuit for use as a low-noise amplifier in the RF band. The input-referred noise of the modified linearized transconductor circuit of Fig. 3.2 is calculated as follows:

$$\overline{v_{in,LNTA}^{\ 2}} = \frac{4kT\gamma}{(2-\sqrt[3]{2})^2}\left(\frac{3}{G_m}+\frac{\sqrt[3]{2}+1}{g_{mL}}\right), \tag{3.9}$$

which yields the NF value of

$$NF|_{LNTA} = 1+\frac{\gamma}{(2-\sqrt[3]{2})^2 R_s}\left(\frac{3}{G_m}+\frac{\sqrt[3]{2}+1}{g_{mL}}\right). \tag{3.10}$$

Comparing equation (3.8) with (3.10) shows that the modified circuit can achieve much lower noise figure. Assuming, for example, that $G_m = g_{m3} = g_{mL}$, equation (3.10) gives a noise figure value of 40.4 dB lower than equation (3.8).

Next, a simulation was conducted to verify the effectiveness of the improved LNTA linearization technique. Fig. 3.3 shows the simulation results of the linearized transconductor. Two tones, 1003 MHz and 1005 MHz, are applied to the input, and the IMD3 component is generated at 1001 MHz. The magnitude of the output current is normalized by linearization-off output current. When the linearization is turned on, the IMD3 component is reduced up to 30.5 dB, which proves that the linearization is effective. While linearity increases, the transconductnance is reduced to $(2-\sqrt[3]{2})G_m$ as a trade-off.

In addition, the LNTA is designed to operate in two modes. Fig. 3.4 shows the two operating modes of the linearized LNTA. Fig. 3.4

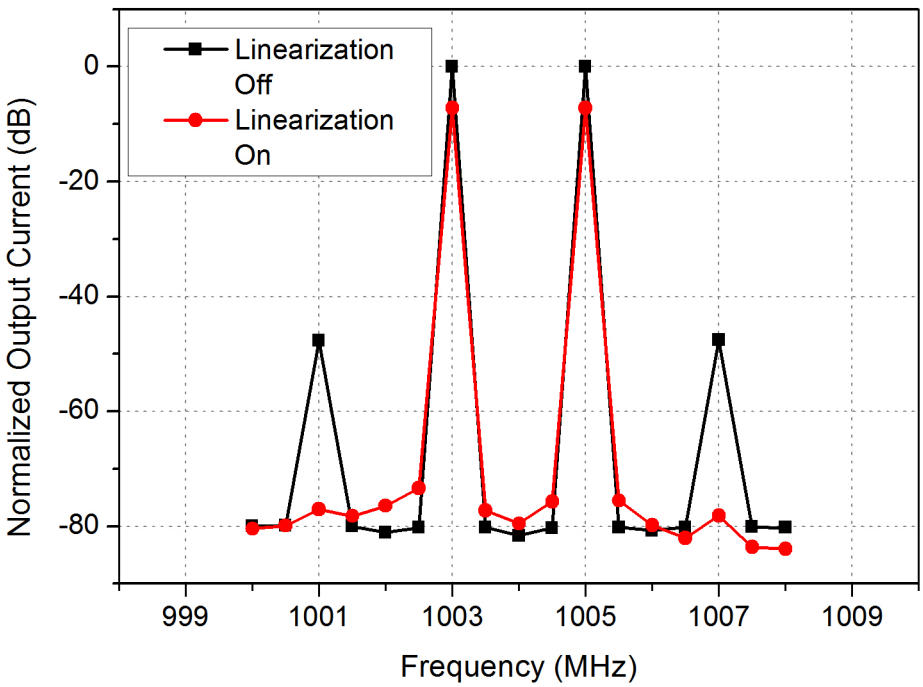


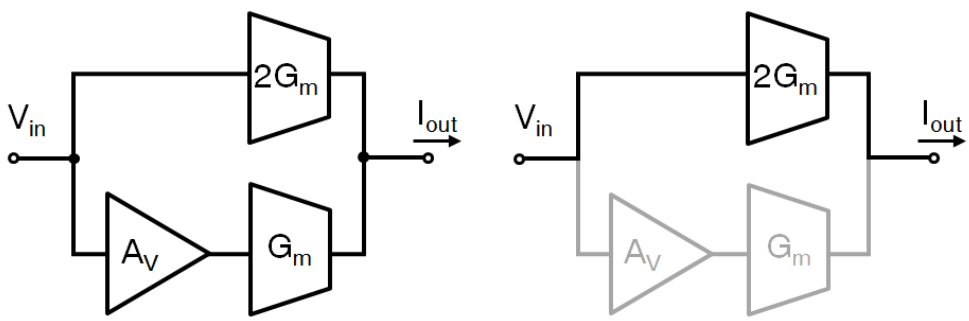
Fig. 3.3 Simulation results of the improved linearized transconductor.

(a) is a high-linearity mode, in which both the main path and the auxiliary path are turned on to operate the linearization circuit. The total G_m value of the circuit is reduced to $0.74G_m$ and has a relatively high noise figure, but high linearity can be achieved due to removal of the IMD3 component. If the auxiliary path is disabled as shown in Fig. 3.4 (b), the circuit operates in low-noise mode. In this case, only an inverter circuit having a transconductance of $2G_m$ is operated, so that it exhibits a low noise figure and an moderate linearity. The noise figure in low-noise mode is given by the

following equation, which is equal to the noise figure of a simple inverter circuit with $2G_m$ of transconductance:

$$NF|_{LNTA} = 1 + \frac{\gamma}{(2-\sqrt[3]{2})^2 R_s}\left(\frac{3}{G_m} + \frac{\sqrt[3]{2}+1}{g_{mL}}\right). \quad (3.11)$$

Table 3.1 shows the simulation results of the circuit operation in the two modes. The comparison shows high IIP3 value in high-linearity mode, but it still shows high noise figure because it operates with LNTA. Therefore, a noise cancelling receiver structure for constructing a low-noise receiver circuit that can operate in a wide band will be described in the next section.



(a) (b)

Fig. 3.4 Linearized low-noise transconductance amplifier in (a) high-linearity mode, (b) low-noise mode.

TABLE 3.1
SIMULATION RESULTS COMPARISON OF DUAL MODE LNTA

Mode	High-Linearity	Low-Noise
Total Gm	0.74	2
NF (dB)	8.24	1.53
IIP3 (dBm)	12.37	5.0

3.2. Wideband Noise-Cancelling Receiver Architecture

The basic architecture of the wideband receiver, shown in Fig. 3.5, consists of an LNTA, a passive mixer, and a baseband transimpedance amplifier (TIA). The LNTA converts the input voltage signal to a current with a transconductance of G_m, and the passive mixer converts the RF current down to the baseband using local oscillator (LO) signals. To generate in-phase (I) and quadrature (Q) signals, a mixer driven by 25 % duty-cycle LO signals is used. The baseband current is then converted into a voltage output in the TIA stage. The TIA consists of a high-gain operational amplifier and feedback resistors. By changing the feedback resistor value, transimpedance can be adjusted. This architecture is promising for the wideband receiver since the RF voltage swing is suppressed by the LNTA, and the risk of receiver saturation by the blocker signal can be reduced.

In the wideband receiver, the LNTA based on an inverter circuit is generally used. Yet, the inverter has high input impedance due to the gates of the MOSFETs. Since 50 Ω wideband input matching is necessary for the wideband receiver, high input impedance becomes a demerit.

To achieve the characteristic of wideband input matching, the global feedback architecture described in [44] is employed. Fig 3.6

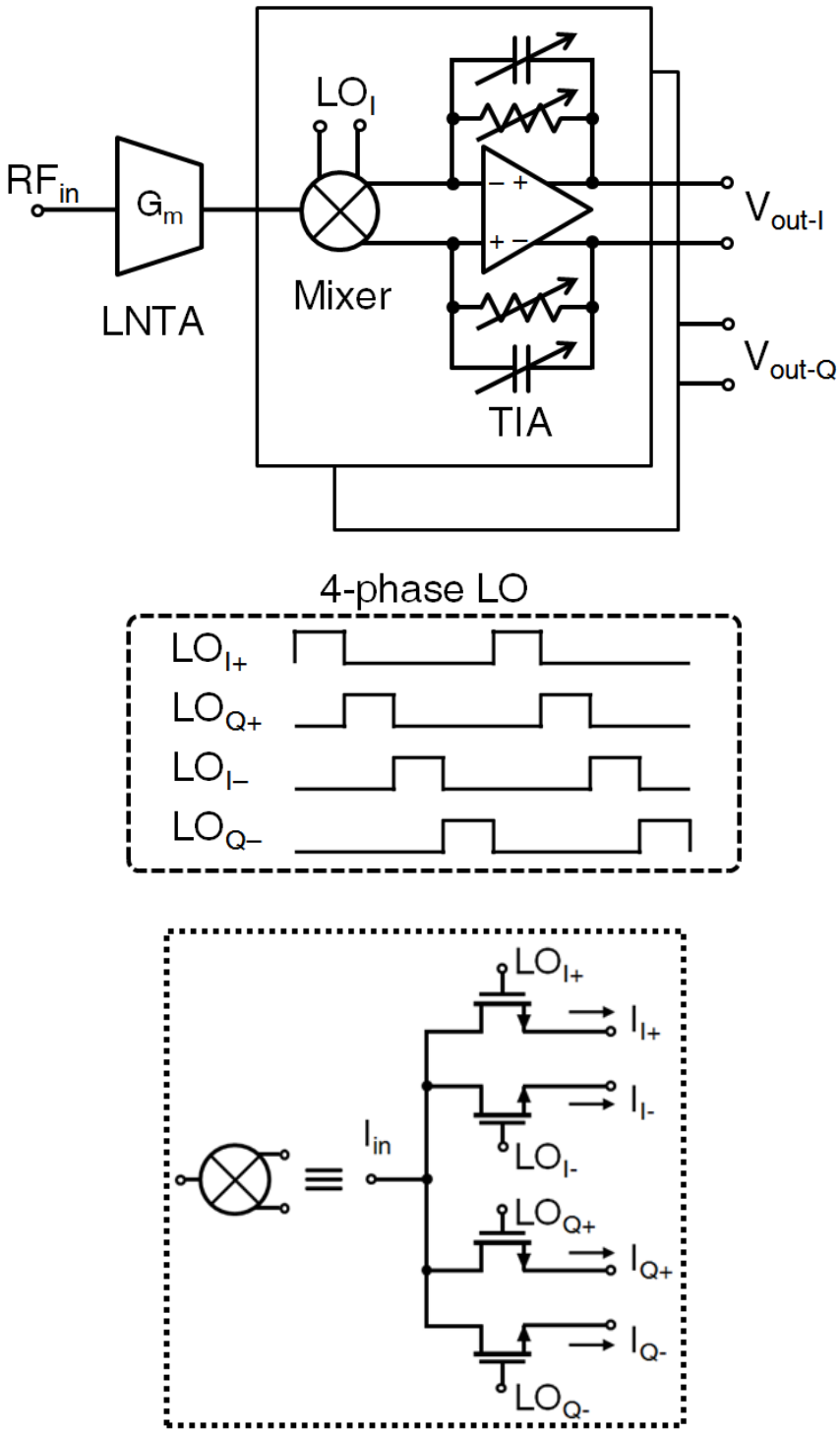


Fig. 3.5 Basic architecture of the current−mode wideband receiver.

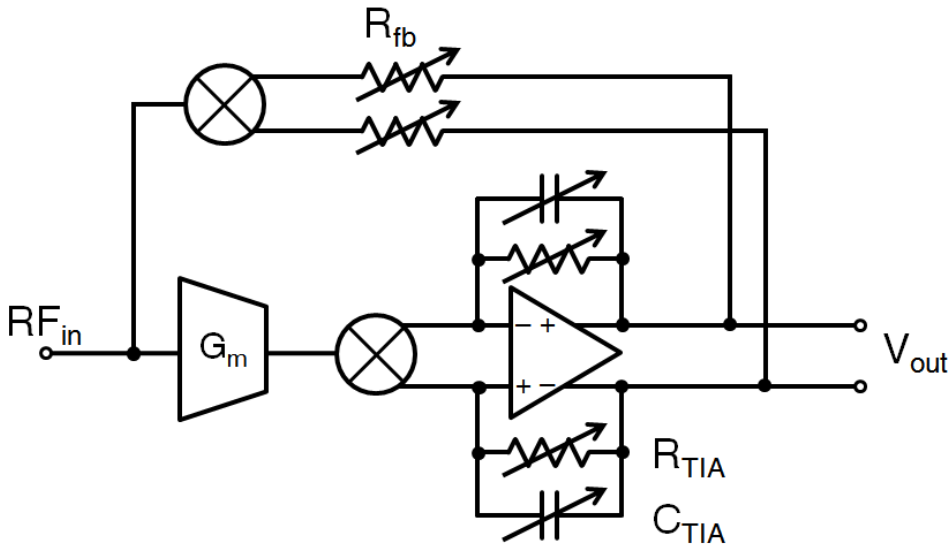


Fig. 3.6 Input matching using global feedback.

shows a wideband receiver with global feedback. The negative feedback of the baseband current to the input node of the LNTA can accomplish 50 Ω input matching. The feedback resistor R_{fb} adjusts the amount of feedback current from the baseband voltage output. With the feedback architecture, the input impedance Z_{in} of the receiver becomes

$$Z_{in}(\omega_{LO}+\Delta\omega) \approx \frac{\pi}{2\sqrt{2}} \frac{R_{fb}}{1+G_m \frac{\sqrt{2}}{\pi} Z_{BB}(\Delta\omega)} \tag{3.11}$$

where Z_{BB} is the transimpedance of the baseband TIA. Therefore, 50 Ω input matching can be achieved by adjusting R_{fb} and R_{TIA}. Equation (3.11) also denotes that Z_{BB} determines the shape of the receiver input impedance, which is close to 50 Ω at the center

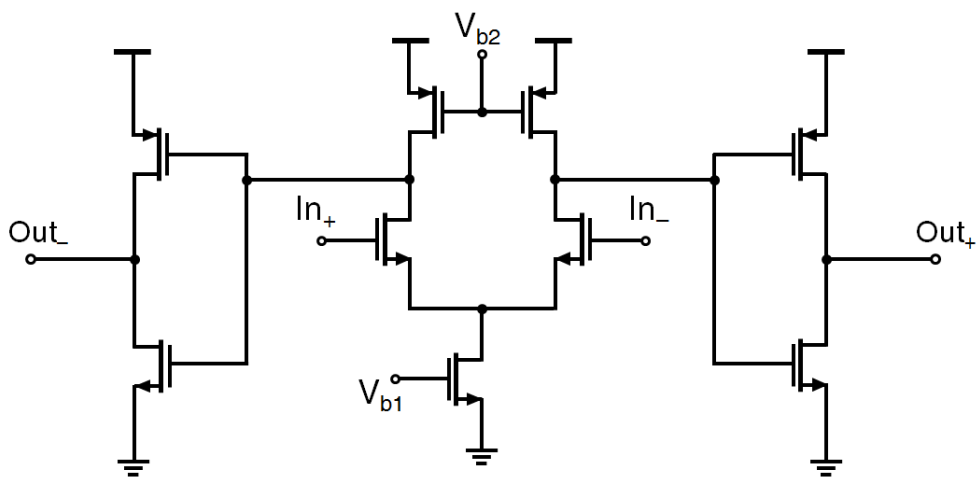


Fig. 3.7 Schematic of operational amplifier in baseband TIA.

frequency, and reaches high impedance as the frequency offset $\Delta\omega$ increases. Fig. 3.7 shows the schematic of operational amplifier in baseband TIA. The amplifier consists of two stages. The first stage is based on a differential amplifier to achieve high gain, and the second stage uses pseudo-differential inverter circuits to produce a high voltage swing output.

The blocker signal is attenuated due to the high input impedance at the blocker frequency, but a large blocker signal can still generate the IMD3 component at the LNTA output. To reduce the IMD3 component, a transconductor linearization method studied in Chapter 2 is adopted to the LNTA.

Although transconductor linearization can be achieved by this method, the additional circuits used in linearization generate

excessive noise. To improve the noise performance of the receiver, a noise-cancelling technique is adopted [61] [62]. Fig. 3.8 shows the complete wideband receiver architecture with this noise-cancelling technique. An auxiliary path is added to the receiver in Fig. 3.6, and the second-stage TIA is added as a summation stage. In-band signals, which are applied to the inputs of LNTAs, are amplified and added in-phase at the summation stage. Noise signals generated in main-path circuits are fed back to the input node, and the polarity of the signal is reversed. This noise signal is sensed by the auxiliary-path circuits, so adjusting the auxiliary-path gain can generate a signal that has the same amplitude and reverse polarity as the original noise signal. Therefore, the noise signals at the TIA outputs of the main and auxiliary paths cancel each other.

A clock generator is designed to create LO signals for a four-phase mixer. To generate 25 % duty-cycle non-overlapping LO signals, a divide-by-four circuit is implemented. The LO signals are generated by combining the outputs of the divider circuits.

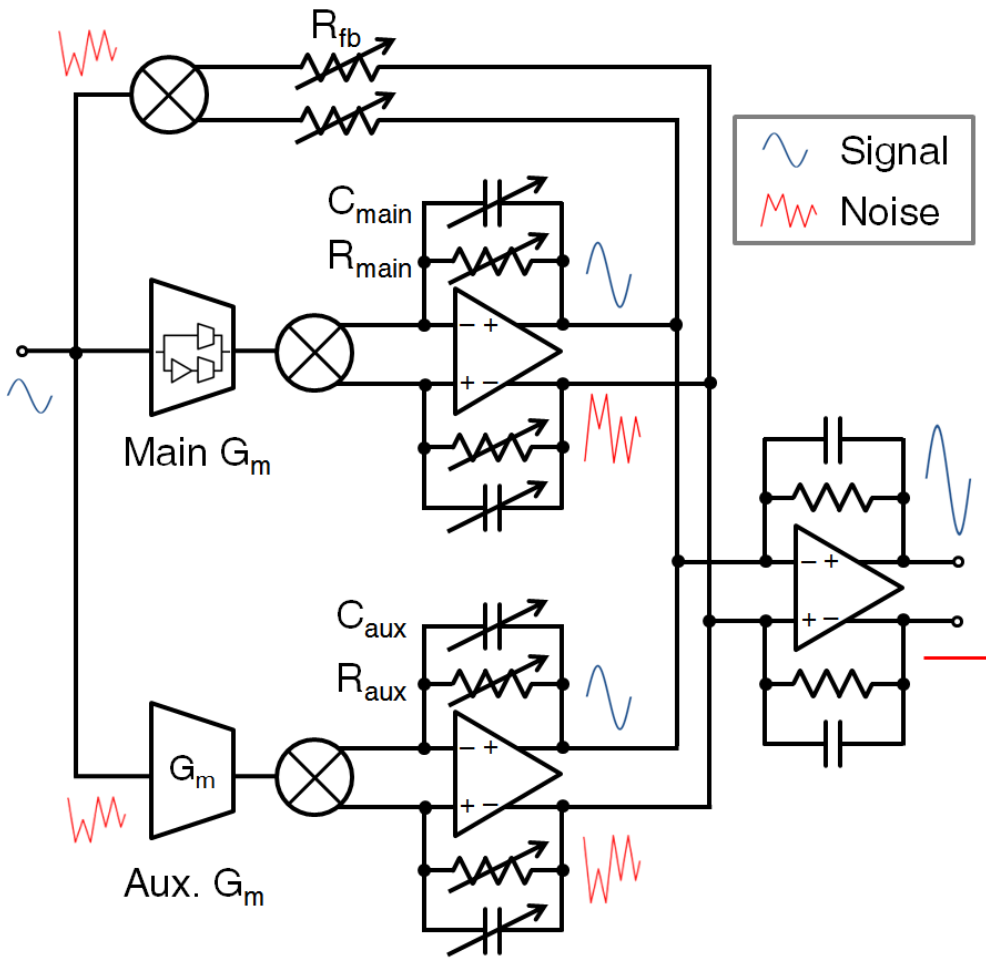


Fig. 3.8 Block diagram of the proposed receiver.

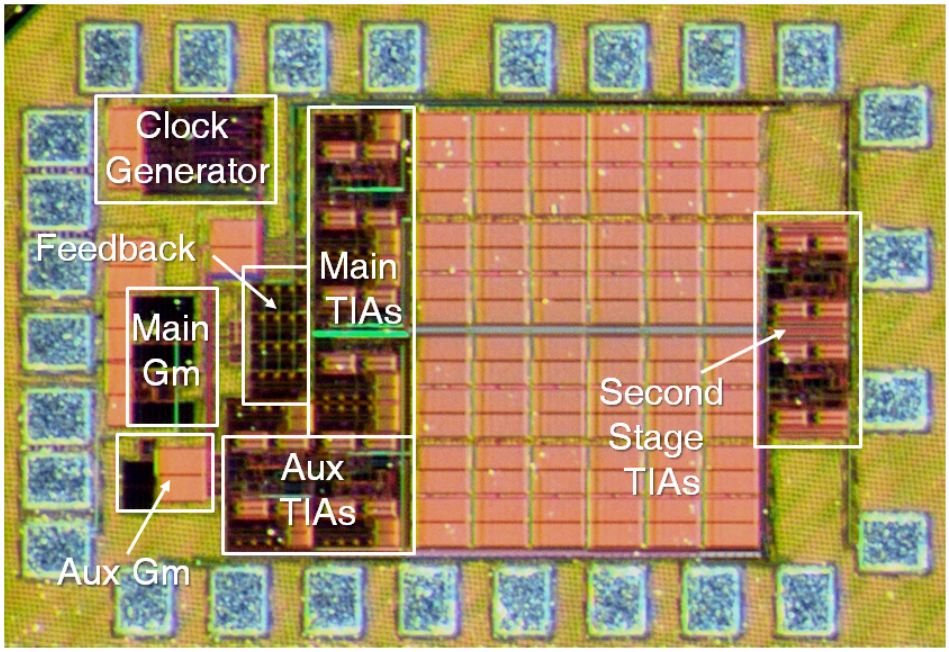


Fig. 3.9 Chip die micrograph.

3.3. Measurement Results

The designed receiver was fabricated using a standard 65 nm CMOS process. The chip die micrograph in Fig. 3.9 shows the chip size (960 μm × 650 μm) with pads.

Fig. 3.10 shows the input matching characteristic of the receiver. As expressed in equation (3.11), optimum input matching of 50 Ω is achieved by adjusting resistor values. By changing the LO frequency, the S_{11} values are maintained below −10 dB from 25 MHz to 2 GHz. Since the clock generator employs true single phase clock (TSPC) logic, it requires a reference clock frequency of 4LO

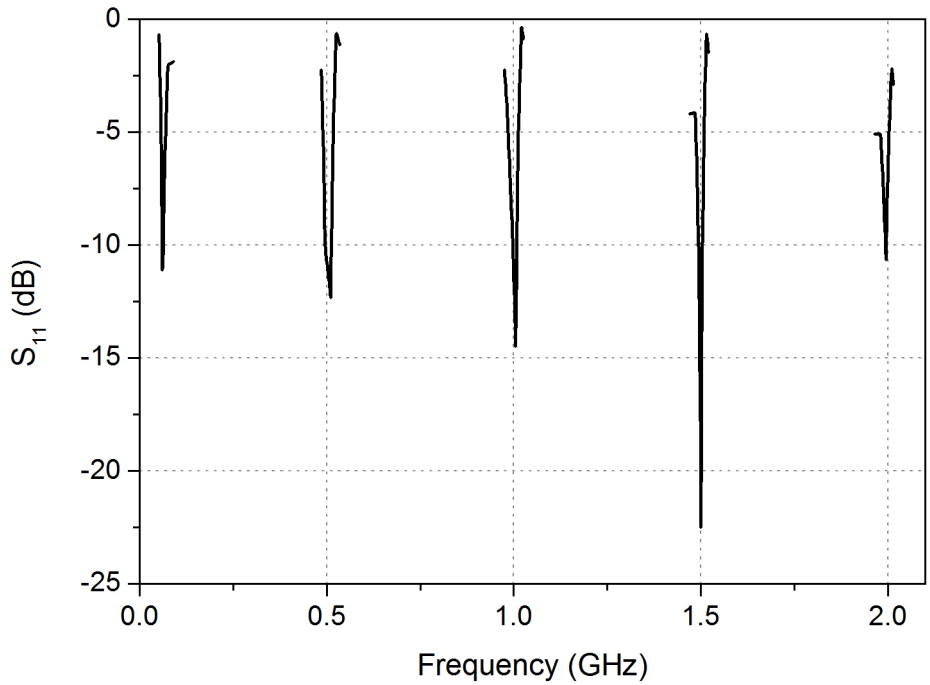


Fig. 3.10 Input matching characteristic of the receiver.

to create an LO signal. The high frequency clock requirement limits the mixer operation range.

The in-band gain and noise figure performance of the receiver is plotted in Fig. 3.11 For the gain measurements, an external amplifier was used to transform a differential baseband signal into a single-ended signal and drive a 50 Ω load. The external amplifier gain was de-embedded after this measurement. The maximum in-band gain is 49.7 dB, and the 3 dB cutoff frequency appears at 25 MHz for the lower bound and 2 GHz for the upper bound. The minimum noise figure achieves 5.1 dB when the linearization

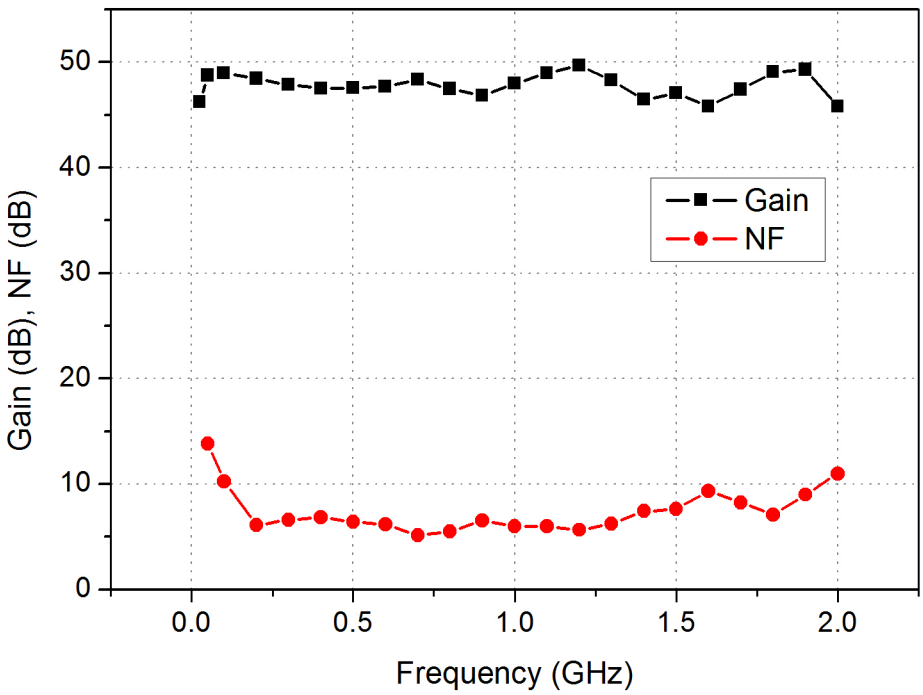


Fig. 3.11 Gain and noise figure performance of the receiver.

circuits are off (low noise mode).

The measurement is performed with an offset frequency sweep at the baseband. Fig. 3.12 shows the gain, the 1 dB compression point (P1dB), and IIP3 measurement results. The single-tone of 1 GHz is applied to measure the gain and the P1dB. The 3 dB bandwidth of the conversion gain is 9 MHz. The P1dB measurement results show a relatively low P1dB at the in-band due to the high level of gain, and the value increases as the offset grows. For the IIP3 measurement, the two-tone test is performed. The first tone at $f_1 = f_{LO} + \Delta f$ and the second tone at $f_2 = f_{LO} + 2\Delta f - 1$ MHz are

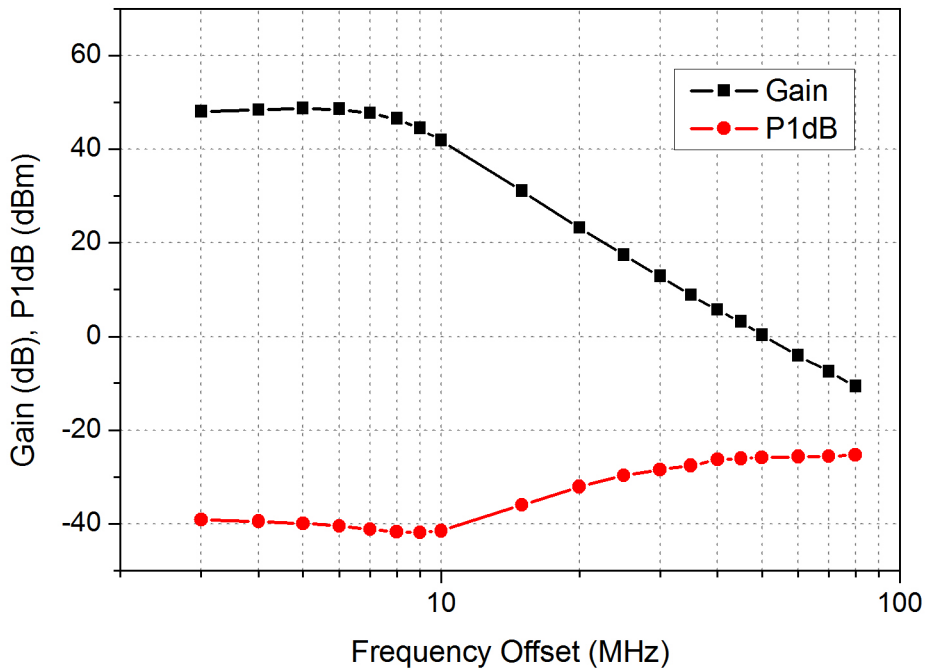


Fig. 3.12 Gain and P1dB measurement results.

applied to the input. This frequency setup always generates IMD3 components at 1001 MHz. Before the linearization circuits are turned on, the maximum IIP3 value is −18.39 dBm. When the linearization is turned on, the maximum IIP3 value is increased to −6.9 dBm; as shown in Fig. 3.13, the linearization method increases the IIP3 values up to 12.3 dBm. The receiver measurement results are summarized in Table 3.2.

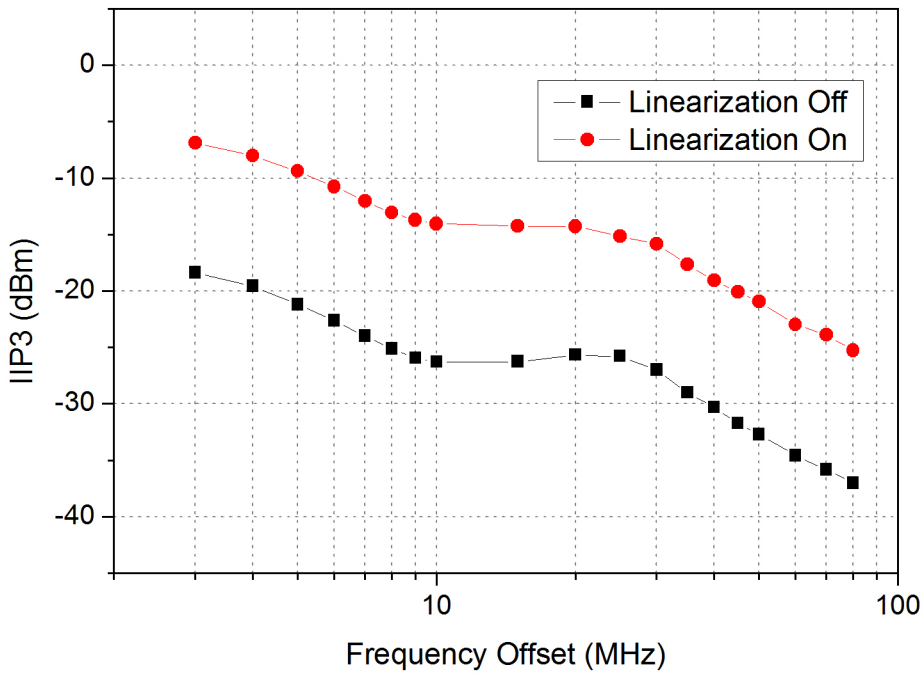


Fig. 3.13 Measured IIP3 with linearization on/off.

TABLE 3.2
MEASUREMENT RESULTS SUMMARY

Topology	Noise Cancelling
Frequency (GHz)	0.025–2
Gain (dB)	49.7 (Linearization off) 45.3 (Linearization on)
NF (dB)	5.1 (Linearization off) 7.6 (Linearization on)
Supply Voltage (V)	1.2
Current (mA)	16–24
IIP3 (dBm)	−18.39 (Linearization off) −6.9 (Linearization on)
Area (mm^2)	0.39
Process (nm)	65

3.4. Conclusions

In this chapter, a wideband receiver using a linearized transconductor is proposed. An LNTA is designed using linearization technique, and noise analysis of LNTA is described. A global feedback structure is applied to accomplish the wideband input matching. To enhance the receiver's linearity performance, a linearization method that cancels the IMD3 components is adopted for the LNTA. Additionally, a noise-cancelling architecture is applied to reduce the excessive noise from additional circuits for linearization. The measurement results show the wideband characteristics of the receiver, and the significant improvement to IIP3 performance proves that the linearization method is effective.

Chapter 4. Blocker-Tolerant Wideband Double Noise-Cancelling Receiver Front-End

This chapter describes how to further improve the performance of the linearized wideband noise cancellation receiver designed in the previous chapter. Although previous studies have shown that linearized LNTA can significantly improve the IIP3 performance of the receiver, additional noise due to added circuits for linearization does not achieve excellent noise figure performance despite the use of noise cancelling techniques. Therefore, in this chapter, we will study the structure of LNTA that can achieve both linearization and noise cancellation simultaneously, and the circuit components that make up the wideband receiver will also be modified to achieve higher performance.

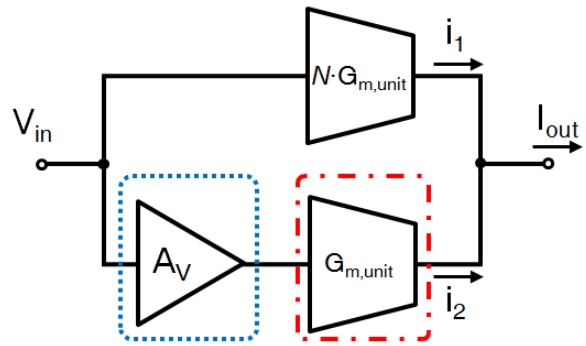
Section 4.1 suggests ways to improve the noise figure performance of the circuit while maintaining the linearity of the linearized LNTA. We will describe a technique for effectively attenuating the IMD component while simultaneously applying the RF noise cancelling technique to the LNTA. Next, Section 4.2 will use the modified LNTA to design a wideband receiver using feedback as in Chapter 3. A wideband input matching and a noise cancellation method through the auxiliary path will be applied, thereby completing a double noise cancelling wideband receiver. The baseband TIA that configures the receiver and the clock

generator for the mixer LO signal generation will also be improved. Section 4.3 will show the measurement results of the designed dual noise cancelling wideband receiver and confirm that the fabricated receiver is resistant to external blocker signals and compare it with previous studies. Finally, we will summarize the conclusions in Section 4.4.

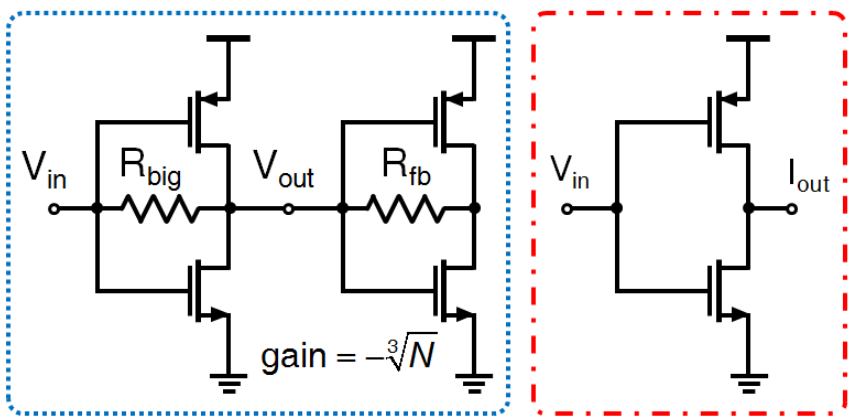
4.1. Linearized Noise-Cancelling Low-Noise Transconductance amplifier

In Chapter 3, the linearization technique has been proposed to suppress IMD3 components generated in LNTA. In the proposed method, the input voltage and output current of the transconductance amplifier are approximated as $I_{out} = G_{m1}V_{in} + G_{m3}V_{in}^{3}$. Here, G_{m1} represents the fundamental transconductance of the transcondcutor, and G_{m3} represents the term for generating the IMD3 component. The linearization circuit consists of two paths, and by adding the output current in each path, the linearization is achieved by cancelling the third-order term.

However, there is a problem that the G_m value of the entire circuit becomes small due to the trade-off for increasing the linearity of the LNTA, and the noise figure rises. Therefore, this section will show how to configure the linearization circuit with minimal performance degradation. Fig. 4.1 is a generalized block diagram of the linearized LNTA circuit proposed in the previous chapters. The Gm ratio of the upper and lower paths is assumed to be N : 1. By adjusting the main G_m value of the upper path and the gain of the voltage amplifier of the lower path, the linearized output current can be obtained by removing IMD3 at any time. The linearized output current can be expressed as



(a)



(b)

Fig. 4.1 (a) Block diagram of linearized transconductor with G_m ratio of N : 1. (b) Schematic of the voltage amplifier and unit transconductor.

$$\begin{aligned} I_{out} &= i_1 + i_2 \\ &= NG_m V_{in} + NG_{m3}^3 V_{in}^3 + (-\sqrt[3]{N} G_m V_{in} - (\sqrt[3]{N})^3 G_{m3}^3 V_{in}^3) \\ &= (N - \sqrt[3]{N}) G_m V_{in}. \end{aligned} \tag{4.1}$$

In this circuit, the noise figure of the whole LNTA can be calculated as follows:

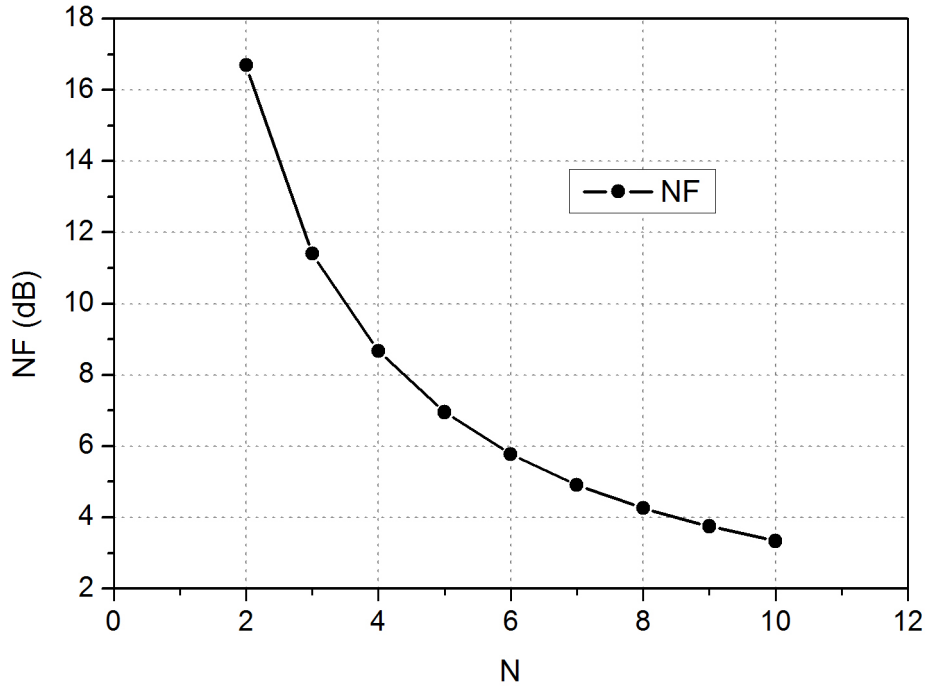


Fig. 4.2 Plotted noise figure as the G_m ratio N increases.

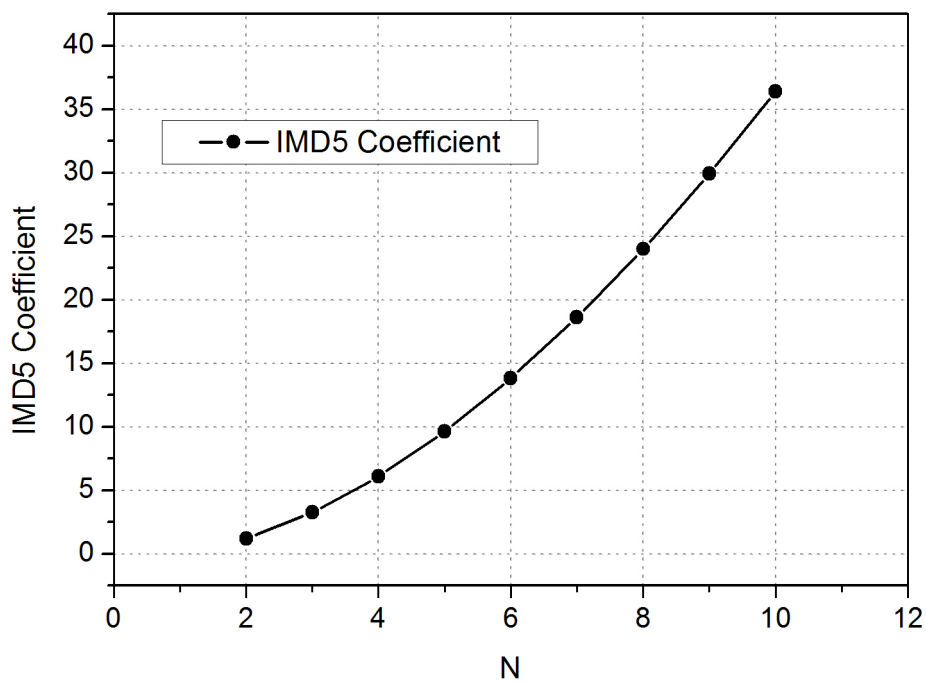


Fig. 4.3 Calculated IMD5 coefficient with G_m ratio of N.

$$NF|_{LNTA,N:1} = 1 + \frac{\gamma}{(N - \sqrt[3]{N})^2 R_s}\left(\frac{N+1}{G_m} + \frac{\sqrt[3]{N}+1}{g_{mL}}\right). \quad (4.2)$$

The above equation can be used to predict how the noise figure of the LNTA changes as N increases. Fig. 4.2 shows the result. It is clear that the graph shows that as N increases, a lower noise figure can be obtained. If so, it would be a good idea to continue increasing N, but there is one more factor to consider. It is about the fifth-order intermodulation distortion component (IMD5). In the linearization method of LNTA, the IMD3 component were mainly considered and cancelled because the coefficients of the IMD5 components were very small and negligible. Also, at low input power, only the third-order term was considered and the fifth-order term can be neglected. However, it should be noted that increasing the N in the linearization scheme of Fig. 4.1 will always cancel out the IMD3 component, but not the fifth-order component. If both the third and fifth order nonlinearities are taken into consideration, the output current can be expressed as follows :

$$\begin{aligned} I_{out} &= i_1 + i_2 \\ &= NG_m V_{in} + NG_{m3}^3 V_{in}^3 + NG_{m5}^5 V_{in}^5 + (-\sqrt[3]{N} G_m V_{in} - (\sqrt[3]{N})^3 G_{m3}^3 V_{in}^3 - (\sqrt[3]{N})^5 G_{m5}^5 V_{in}^5) \\ &= (N - \sqrt[3]{N}) G_m V_{in} + (N - N^{\frac{5}{3}}) G_{m5}^5 V_{in}^5. \end{aligned} \quad (4.3)$$

As can be seen from the equation (4.3), the coefficient of the IMD5 component becomes larger as N increases. The graph of the IMD5 coefficient according to the change of N is shown in Fig. 4.3. Since the IMD5 grows 5 times faster than the fundamental

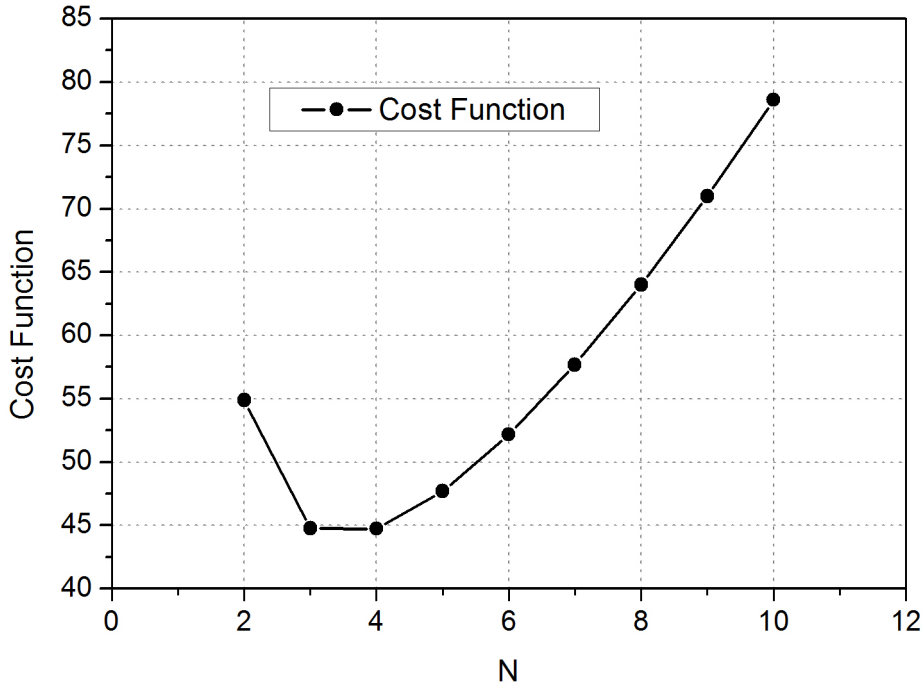


Fig. 4.4 Graph of cost function versus the G_m ratio.

signal, the linearity of the LNTA may be rather reduced if this coefficient is increased. Furthermore, care must be taken in situations where a large blocker signal enters the input at the wideband receiver. Since there is a trade-off between the noise figure and the coefficient of IMD5, let's define a cost function to minimize performance degradation.

$$\text{Cost Function} = \text{Noise factor} \times \text{IMD5 Coefficient} \tag{4.4}$$

The above equation is plotted in Fig. 4.4. As a result, the noise figure and the IMD5 component can be kept low when $N = 4$. Based

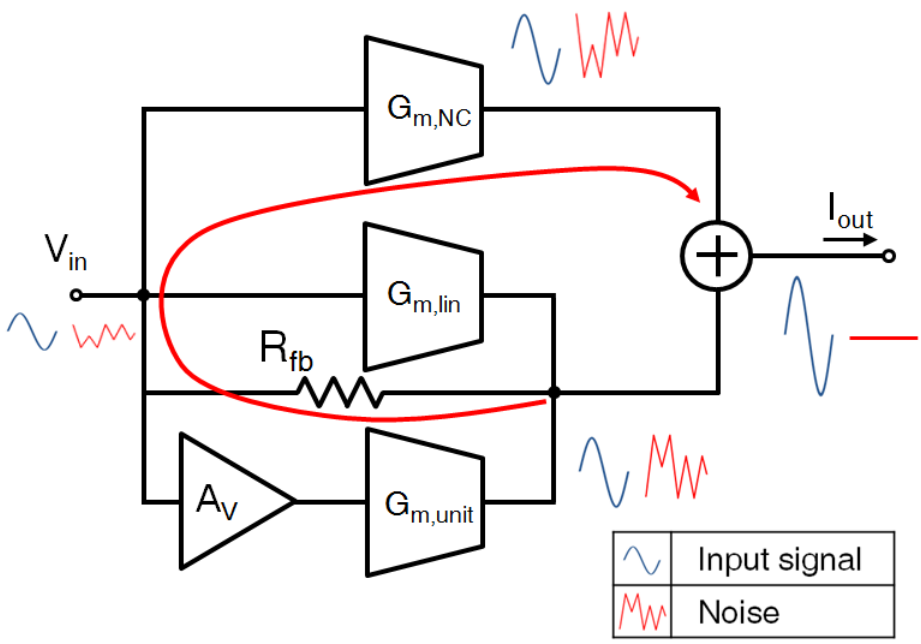
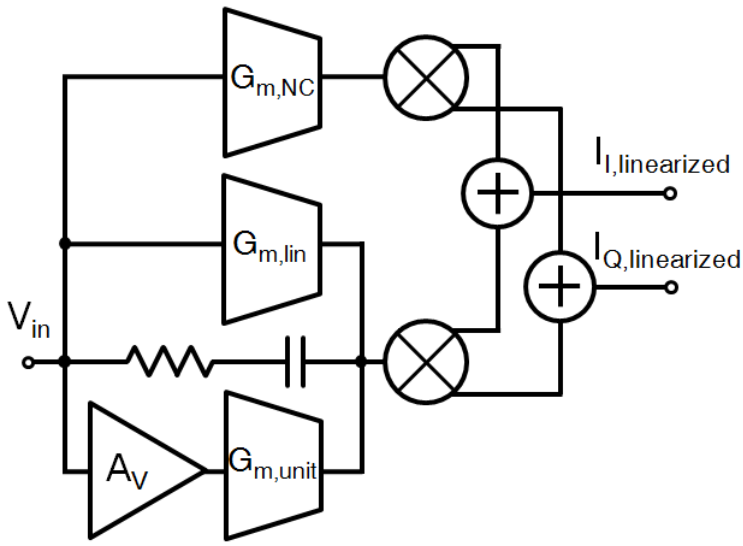


Fig. 4.5 Block diagram of noise-cancelling LNTA.

on these results, the G_m ratio of the linearized LNTA was determined as 4 : 1.

Comparing $N = 2$ and $N = 4$, it can be seen that the noise figure improves by about 8 dB. Assuming that the value of unit G_m is 7.5 mS and the value of g_{mL} is 10 mS, the equation (4.2) gives a noise figure of about 8.67 dB. The modified linearized LNTA still exhibits high noise figure performance compared to a simple inverter circuit, and a way to improve it can be investigated.

To improve the noise performance of modified linearized LNTA, a noise-cancelling method in the RF band is applied [63]. Figure



$$G_{m,total} = G_{m,lin} + G_{m,NC} = 4G_{m,unit}$$

Fig. 4.6 Block diagram of linearized noise-cancelling LNTA.

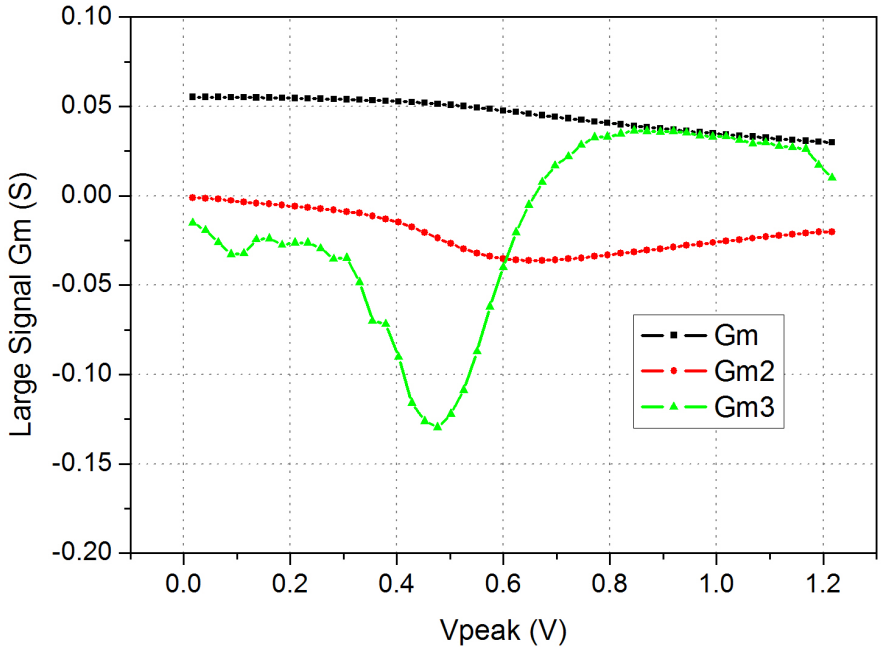
shows the linearized LNTA with RF noise cancelling technique. This method feeds back the noise at the output node and amplifies it with another transconductor to cancel it. The feedback resistor R_{fb} uses a large value (20 kΩ) to minimize the transconductance reduction of the LNTA. A secondary LNTA based on an inverter circuit was used to amplify the feedbacked noise in opposite phase. This is named LNTA for noise cancelling and is denoted as $G_{m,NC}$. It should be noted here that after adjusting the ratio of G_m for linearization and applying the noise cancellation technique, it deviates from the optimum G_m ratio. Thus, the noise is cancelled but the linearization

is not completely performed. Therefore, we propose the following method to remove the noise while maintaining the linearization technique.

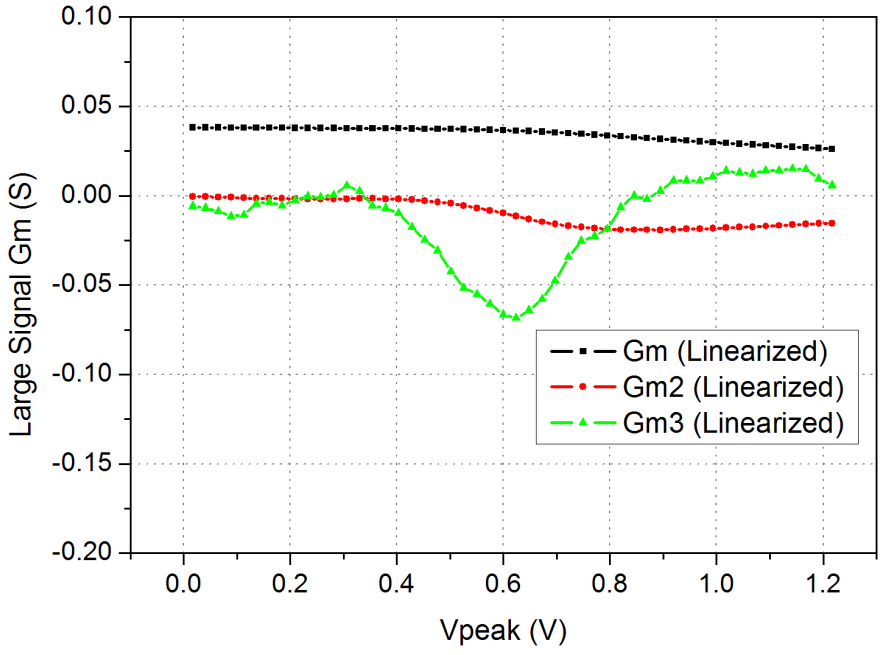
The proposed noise cancelling LNTA is shown in Fig. 4.6. The LNTA of the main path is divided into two LNTAs, and the sum of the total transconductance is designed to be $4G_{m,unit}$. As a result, the G_m ratio of the transconductors in the main path and the auxiliary path is kept at 4 : 1, and the cancellation of the noise occurs in the baseband after downconversion by the passive mixers. This circuit structure can achieve both linearization and noise cancellation of the transconductor, and it can alleviate the performance degradation caused by the blocker. In addition, the configuration in which two mixers are connected in parallel has the same effect as reducing the resistance of the mixer in half, and has the advantage of reducing the voltage swing before the TIA by lowering the input impedance at the following stage of the LNTA. Adjustment of the $G_{m,lin}$ and $G_{m,NC}$ values can cancel the noise from the lower path (voltage amplifier, $G_{m,unit}$, and $G_{m,lin}$), so that $G_{m,NC}$ is the dominant contributor to noise. If all the noise in the lower path is cancelled, the only noise source in the LNTA is $G_{m,NC}$, where the noise figure becomes :

$$NF\,|_{Lin.N.C.\ LNTA} = 1 + \frac{\gamma}{(4-\sqrt[3]{4})^2 G_{m,NC} R_s}. \qquad (4.5)$$

The noise figure performance of the LNTA has been improved much more than the circuit in Chapter 3. In order to eliminate the performance degradation caused by the parasitic of non-ideal



(a)



(b)

Fig. 4.7 Large-signal transconductance and its derivatives of (a) $4G_m$ LNTA and (b) linearized LNTA.

MOSFET switches, the LNTA circuit is designed to operate as one fixed circuit without discriminating the operation mode. By applying noise reduction techniques in addition to linearity and technique, the modified LNTA circuit can achieve the similar level of noise figure as that of the inverter while maintaining the same level of linearity as the LNTA in Chapter 3.

The performance of the modified LNTA was investigated by simulation. The transconductance values and its derivatives of the main amplifier, $4G_m$ ($G_{m,total}$) and the linearized G_m ($(4-\sqrt[3]{4})G_m$) are plotted in Fig. 4.7. A large-signal transconductance can be obtained by using the peak-to-peak value of the input voltage (V_{peak}) of the circuit and the peak-to-peak value of the output current (I_{peak}), and thus the linearization of the LNTA can be analyzed. The value obtained by differentiating G_m (fundamental transconductance) once is denoted by G_{m2}, and that obtained by differentiating G_{m2} once again is G_{m3}. It can be seen that the linearized G_m of Fig. 4.7 (b) is smaller than the G_{m3} from $G_{m,total}$ in Fig. 4.7 (a). In addition, the graph shows that the G_{m3} value of the linearized LNTA is close to 0 when the V_{peak} value is small, and the IMD3 component gradually increases when the V_{peak} reaches 400 mV (when the input power is about −4 dBm). Simulation results show that modified LNTA using 4 : 1 G_m ratio can operate with tolerance to large blocker signal, making the wideband receiver resistant to the blocker. The design process for a wideband receiver using this LNTA and description of other blocks of the receiver will be presented in the next section.

4.2. Wideband Double Noise-Cancelling Receiver Front-End

A wideband receiver was designed using the linearized noise cancelling LNTA. Fig. 4.8 is a block diagram of the wideband receiver with a double noise cancelling scheme. A linearized LNTA is used as the main G_m and a feedback path in the baseband is added using the resistor R_{fb}. This path can be used to feedback the noise in the baseband to the RF input node while achieving wideband input matching [44]. The input impedance of the circuit which the feedback is added becomes:

$$Z_{in}(\omega_{LO}+\Delta\omega) \approx \frac{\pi}{2\sqrt{2}} \frac{R_{fb}}{1+G_m \frac{\sqrt{2}}{\pi} Z_{BB}(\Delta\omega)}, \quad (4.6)$$

where $\Delta\omega$ is the offset from the center frequency and Z_{BB} is the transimpedance value of the baseband TIA. Z_{BB} is adjustable by varying the feedback resistance of the TIA, and additionally controlling R_{fb} can achieve 50 Ω input matching over wideband.

Next, a second noise cancellation operation is enabled by adding an auxiliary path to the receiver circuit. The RF noise that has not been completely removed in the LNTA stage (noise due to $G_{m,NC}$) and noise from the baseband TIA are upconverted back through R_{fb} and removed by combining in the baseband via the auxiliary path.

Fig. 4.9(a) shows the circuit diagram of the baseband TIA. The TIA consists of two stages, a circuit based on the Tow-Thomas

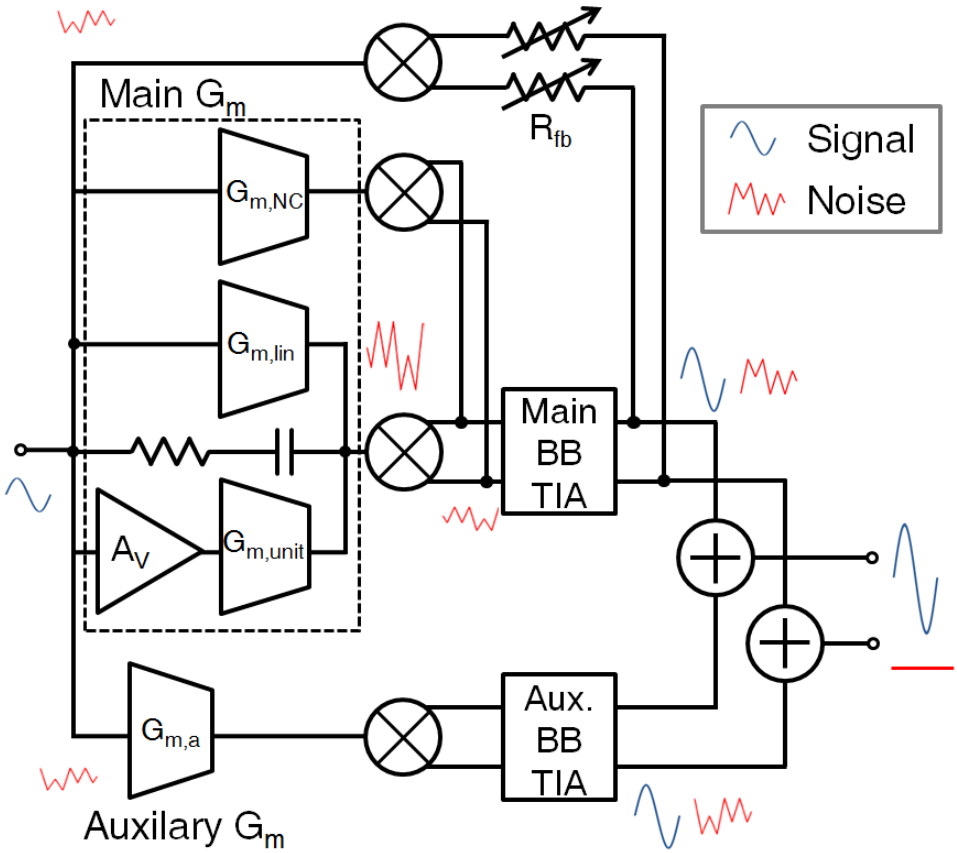
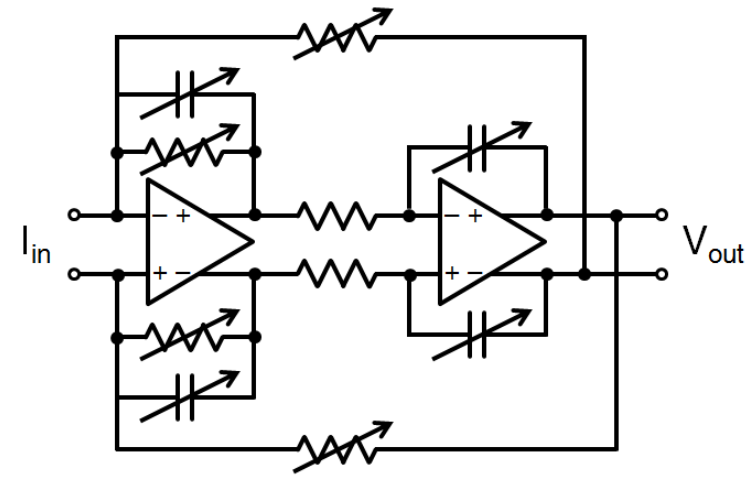
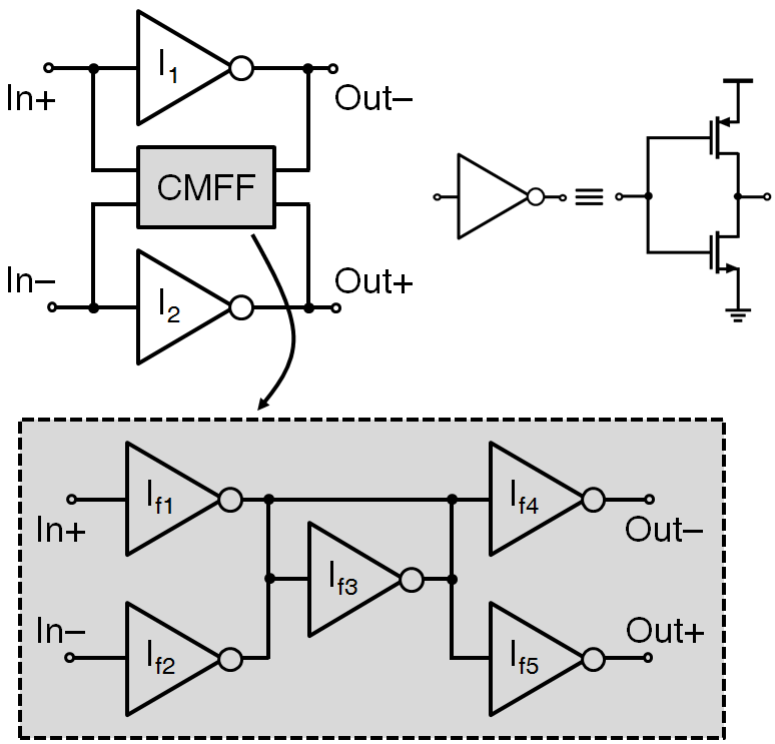


Fig. 4.8 Block diagram of double noise-cancelling receiver front-end using linearized noise-cancelling LNTA.

biquad filter. The attenuation of the blocker signal can be further increased through the second-order filtering operation. It is designed to adjust the gain and bandwidth of the TIA by changing the feedback resistor and capacitor values. A block diagram of the amplifiers in the TIA is shown in Fig. 4.9(b). It is made up of pseudo-differential amplifiers, and all the components are designed



(a)



(b)

Fig. 4.9 (a) Schematic of baseband TIA. (b) Block diagram of operational amplifier in baseband TIA and its common−mode control circuit.

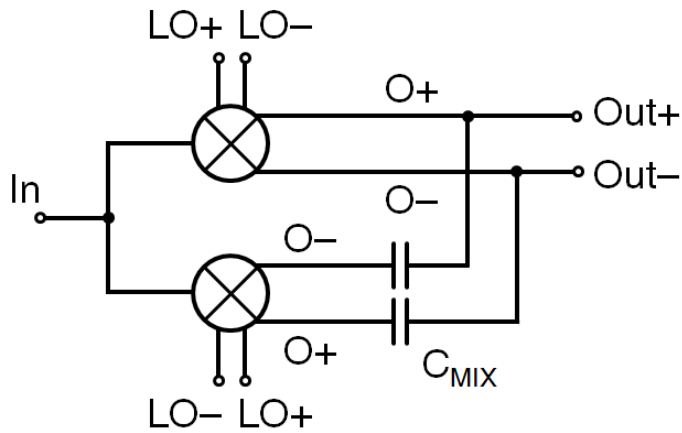


Fig. 4.10 Schematic of dual switch mixer.

using simple inverters. This can maintain high linearity in the baseband, and suppresses the effect of flicker noise by using a long channel transistor in the inverter circuit. In addition, a common mode control circuit consisting of inverters is designed [64].

In order to mitigate the performance degradation of the receiver by the blocker, a dual switch mixer structure has been adopted. The circuit diagram of the dual switch mixer is shown in Fig. 4.10. This circuit adds one more switch set in the passive mixer, and the added switches are driven by the LO signal in phase opposite to the original mixer switch. Here, a capacitor is connected in series to the additional switch path (C_{MIX}), and the output is added again to complete the dual switch mixer. There are two advantages of adding a mixer switch. First, the resistance by the MOSFET switch is equal to half of the original one. In current-mode receivers, it is

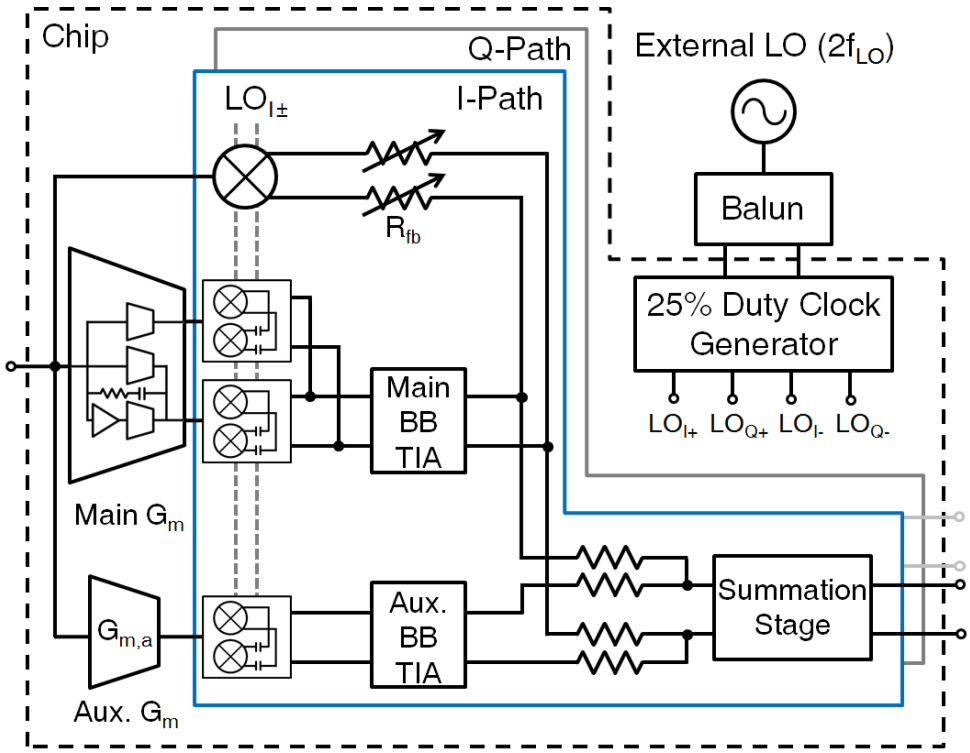
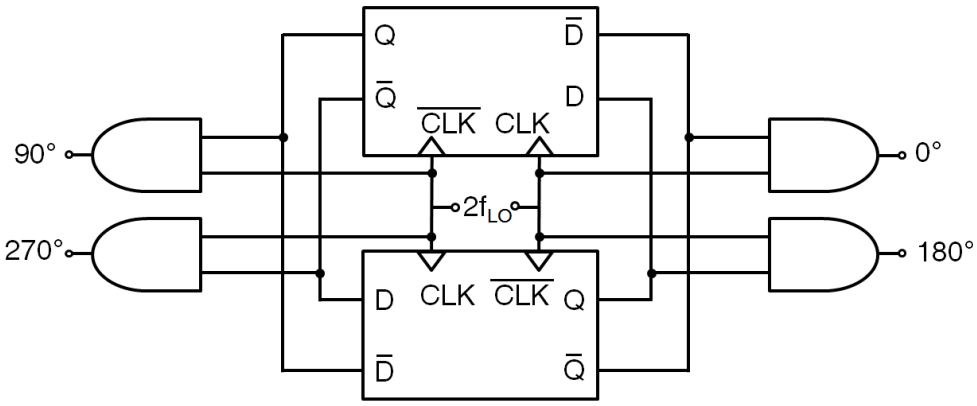


Fig. 4.11 Block diagram of entire receiver front-end.

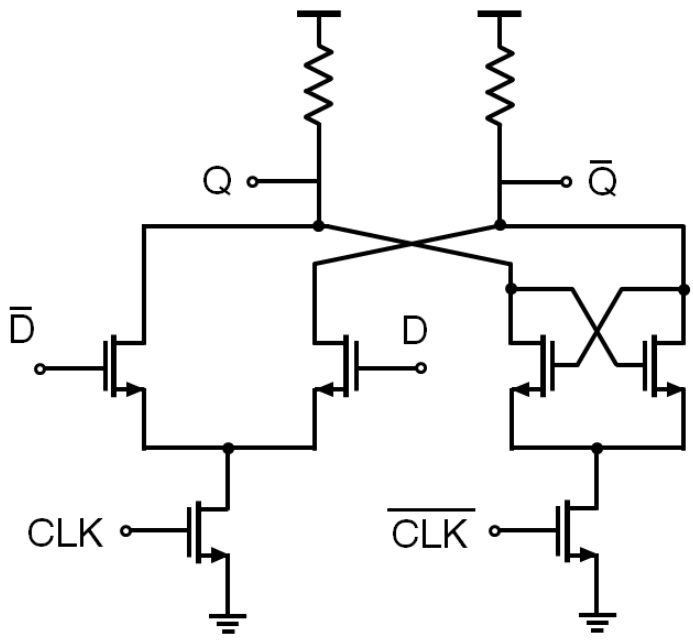
important to maintain a low impedance from the output of the LNTA to the input of the baseband TIA, so a low impedance can be achieved using a dual switch mixer. Second, the upper switch and the lower switch operate with LO signals of opposite phases, so that the blocker current can be attenuated. The series-connected capacitor C_{MIX} appears to have a low impedance for the blocker signal that is distant from the center frequency, so that the blocker signals are combined in opposite phases in the output node. On the other hand, the in-band signal does not pass through the capacitor

because C_{MIX} appears to have a high impedance, and as a result, the attenuation of the in-band signal hardly occurs. In the previously designed double noise cancelling receiver, a dual switch mixer was applied to all mixers except the feedback path.

The structure of the entire receiver is shown in Fig. 4.11. The chip includes a main LNTA, auxiliary LNTA and mixers, and baseband TIAs with a clock generator. The same baseband TIAs are used in main, auxiliary and summation stages. The clock generator is designed using a current-mode-logic (CML) type divider and requires an external signal of $2f_{LO}$. The clock signal is converted into a differential signal through an external balun, which is divided into signals with a phase difference of 90 degrees in the CML divider. Then the signals passed through the AND gate will have a duty cycle of 25 % to drive the mixer. The circuit block diagram of the clock generator is shown in Fig. 4.12.



(a)



(b)

Fig. 4.12 (a) Block diagram of clock generator. (b) Schematic of the CML divider.

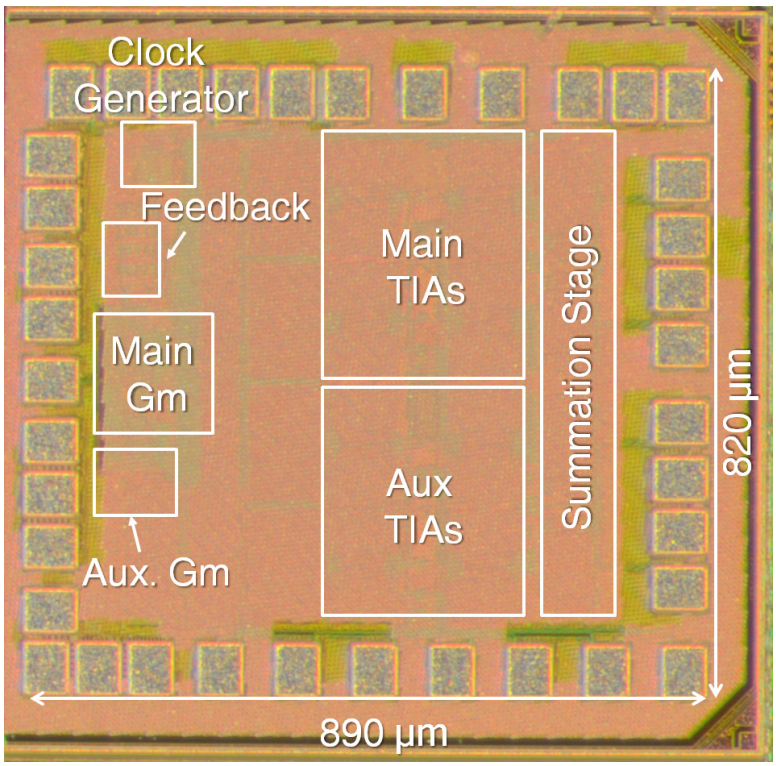


Fig. 4.13 Die micrograph of the fabricated chip.

4.3. Measurement Results

The designed chip was fabricated using 65 nm standard CMOS process. The total chip size is 890 μm × 820 μm and the active area excluding the pad is 650 μm × 640 μm. Fig. 4.13 is a micrograph of the fabricated chip. The supply voltage is 1.2 V and the current consumption is 37−63 mA. In LNTA and baseband TIA,

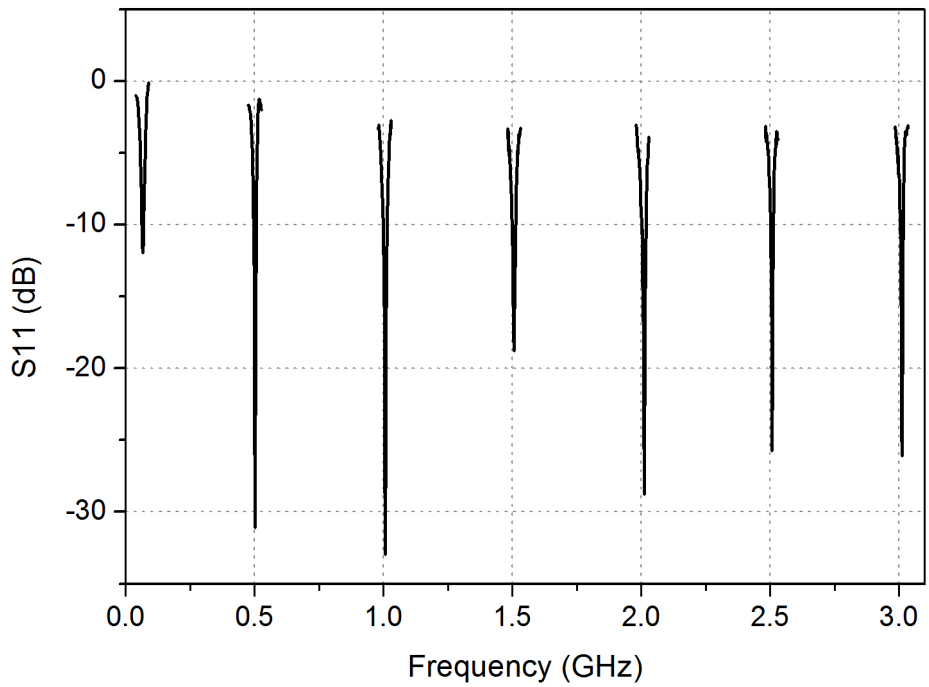


Fig. 4.14 Measurement result of input matching characteristic.

34 mA is constantly consumed and current consumption increases as the operating frequency increases, due to the clock generator circuit.

The operation frequency range of the receiver based on the S_{11} value ($S_{11} < -10$ dB) was measured from 60 MHz to 3 GHz, and the results are shown in Fig. 4.14. This result shows that the input is well-matched to real 50 Ω due to the feedback architecture. The limit of the operating frequency of the receiver is due to the clock generator. Because the passive mixer used in the receiver requires

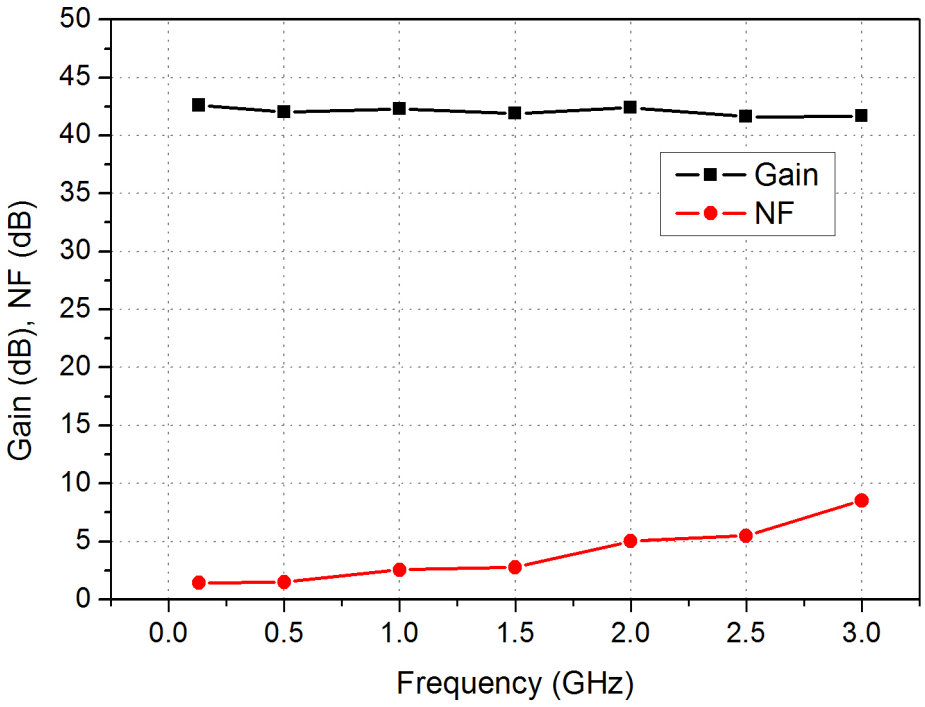


Fig. 4.15 Measured gain and noise figure.

a square wave that swings from 0 V to VDD for operation, its performance is degraded unless the LO signal is in the correct square wave form. Also, because the CML divider circuit used in the clock generator also has an operating frequency range, it cannot operate at very high frequencies.

Fig. 4.15 shows the gain and noise figure for the LO frequency changes. In all bands, the gain is even around 42 dB. The noise figure shows the lowest value of 1.4 dB at the low frequency side,

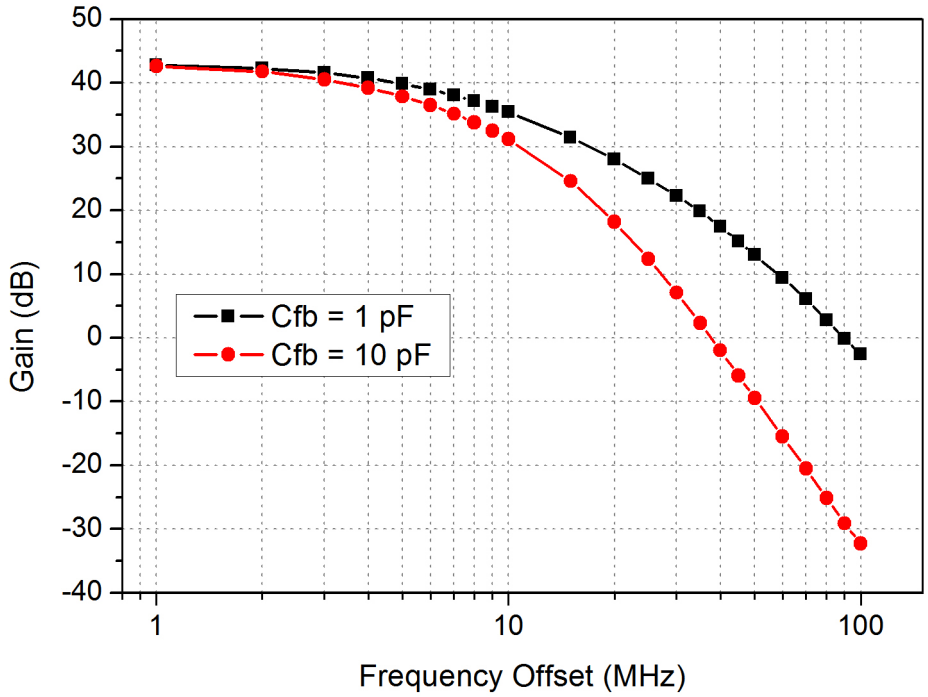


Fig. 4.16 Measurement result of baseband frequency sweep.

but the performance has gradually decreased with increasing frequency.

Fig. 4.16 is a graph of baseband gain over frequency offset. It can be seen that the frequency response of the baseband TIA is in the shape of a low-pass filter. Here, by adjusting the feedback capacitor value of the TIA circuit, it is possible to further attenuate the out-of-band blocker signal. The maximum gain of the receiver was about 42 dB and the in-band signal bandwidth was measured at about 10 MHz.

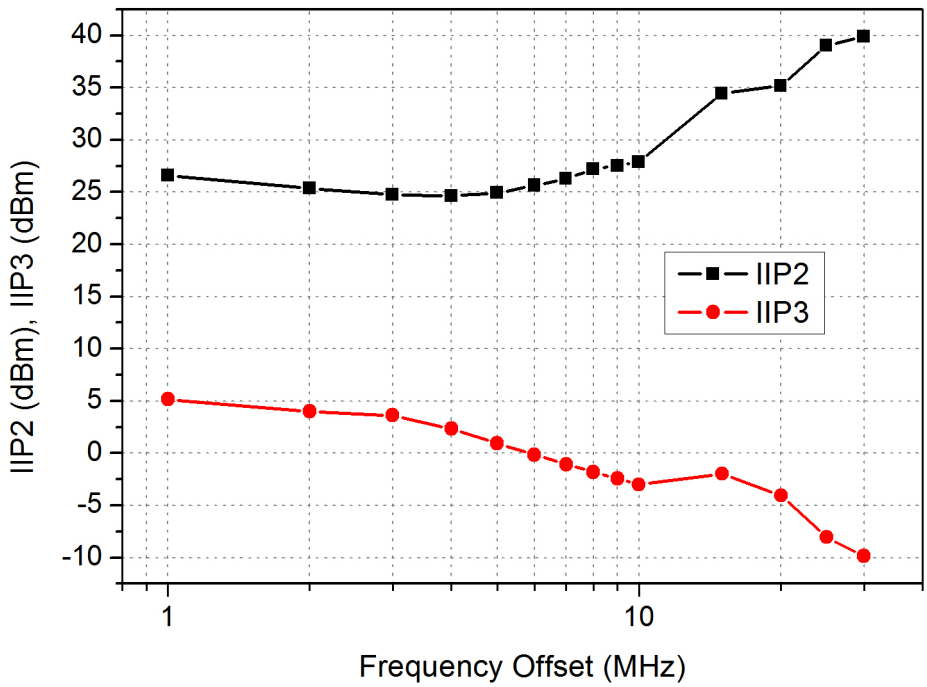


Fig. 4.17 Linearity measurement results of the receiver.

Fig. 4.17 shows the linearity measurement results of the receiver at 500 MHz. The input-referred second-order intercept point (IIP2) and IIP3 values of the receiver were measured using a two-tone signal. For IIP2 measurements, the frequencies used are $f_1=f_{lo}+\Delta f$ and $f_2=f_{lo}+\Delta f+800$ kHz, respectively. For IIP3 measurements, $f_1=f_{lo}+\Delta f$ and $f_2=f_{lo}+2\Delta f+800$ kHz were used. A high IIP3 value of 5.15 dBm was obtained using the linearized LNTA. The IIP2 value was larger than 40 dBm in the out-band.

A figure-of-merit (FOM) is proposed to compare the performance with other wideband receivers studied so far. In the case of a wideband receiver, it is often difficult to set a specific communication standard, so it is unclear to compare the performance by verifying that the specification of the communication standard is satisfied. Therefore, we will quantitatively compare the performance of the receiver using the following equation. The equation for FOM calculation becomes:

$$\mathrm{FOM} = 10 \cdot \log\left(\frac{Gain\ [dB] \cdot IIP3\ [mW] \cdot (f_{high} / f_{low})}{(F-1) \cdot P_{dc}\ [mW]} \right), \qquad (4.7)$$

where $Gain$ is the total gain of the receiver in dB, f_{high} is the highest operating frequency, and f_{low} is the lowest operating frequency. So, the term (f_{high} / f_{low}) represent the fractional bandwidth of the wideband receiver. The IIP3 value was used as an index of linearity and the unit was converted to mW to compare. F denotes the noise factor, and P_{dc} is the power consumption.

The measurement results are summarized in Table 4.1 and compared with the results of previous studies. This design has the widest fractional bandwidth in the operating frequency section. The linearized LNTA and double noise cancellation technique can achieve the lowest minimum noise figure and good IIP3 value.

TABLE 4.1
MEASUREMENT RESULTS SUMMARY AND COMPARISON

	[35]	[44]	[46]	This work
Type	Noise Cancelling	Noise Cancelling	Noise Cancelling	Double N.C.
Frequency (GHz)	0.08−2.7	0.7−3.8	0.1−2.8	0.06−3
Gain (dB)	72	42	50	42.6
NF (dB)	1.9	1.6−3.2	1.5−2.3	1.4−8.5
IIP3 (dBm)	13.5	1	5	5.15
IIP2 (dBm)	54	> 75	50	40
Supply Voltage (V)	1.3	1.2	1.1	1.2
Current (mA)	27−60	22.8−34.9	24.5−36.4	37−63
Active Area (mm^2)	1.2	0.15	0.8	0.42
Process (nm)	40	65	40	65
FOM	34.4	13.7	26	26.1

4.4. Conclusions

By improving the linearization technique of the transconductor, an LNTA that can perform linearization and RF noise cancelling operation simultaneously is designed. The optimal G_m ratio for low NF and IMD5 is set to 4 : 1. Then, a second noise cancellation is performed by adding the feedback and the auxiliary path in the baseband. The dual switch mixer architecture is adopted to further attenuation of the blocker signal. The entire receiver circuit consisted of inverter circuit, resistor, and capacitor, and showed wideband operation characteristics ranging from 0.06 GHz to 3 GHz. The proposed receiver achieves a high IIP3 value by the linearization technique and a low noise figure by the noise cancelling technique, which is suitable for a wideband receiver which must withstand an external blocker.

Chapter 5. Conclusions

This thesis investigates a wideband receiver as one of the methods to implement a practical SDR receiver. We have investigated the out-of-band interference signal or blocker, which is a problem of wide-band receivers, and studied ways to effectively eliminate them. As a result of analyzing previous studies, there are three methods for blocker removal. The first method uses an N-path filter, which has the advantage that a variable band-pass filter can be designed, but the noise figure performance of the receiver is degraded. Next, we reviewed a receiver with a feed-forward structure, which requires a lot of effort to achieve good performance due to the relatively complicated receiver structure. In this thesis, we developed a wideband receiver based on the current-mode structure and tried to remove the blocker. The contents of the step-by-step research are as follows.

First, in Chapter 2, the method of increasing linearity of the transconductance amplifier is studied. In the current-mode receiver, LNTA has a high G_m value to achieve low noise figure, but high G_m value leads to low linearity (low IIP3 value). To solve this trade-off, we proposed a linearization method of transconductor. The proposed technique is to cancel the intermodulation components in a feed-forward manner using two paths. A transconductance of $2G_m$ transconductor was placed in the main path, an amplifier with a gain

of $\sqrt[3]{2}$ and a G_m−sized transconductor were laid in the auxiliary path. This structure allows the fundamental signal to have different magnitude and the IMD3 component to have the same magnitude at the output. As a result, the entire transconductor circuit could have high linearity due to the removed IMD3 component. A high−pass filter that can be reconfigured using a linearized transconductor was designed and proved its performance. The resulting circuit achieved a high IIP3 performance of 19.4 dBm.

Using the linearized transconductor developed in Chapter 2, the wideband receiver was designed in Chapter 3. First, since the linearized transconductor had a very high noise figure due to the additional circuitry used for linearization, we proposed a more suitable form for the linearized LNTA through noise analysis. The LNTA is designed to operate in low−noise mode when there is no blocker and switched to operate in high−linearity mode when blocker is present. We also applied a noise cancelling technique to the receiver to further improve the noise figure performance of the wideband receiver circuit. A feedback path was added to the current−mode receiver structure consisting of LNTA, mixer, and baseband TIA, and the noise signal could be detected using this feedback path. This feedback path also serves to keep the receiver's input match at 50 Ω across the wide bandwidth. By adding an auxiliary path to the receiver, the in−band signal is amplified and the detected noise is canceled at the baseband. The completed circuit exhibited wideband performance from 0.025 GHz

to 2 GHz, and good IIP3 performance of −6.9 dBm in the high-linearity mode. However, the noise figure performance is relatively poor at 5.1 dB, and there is room for improvement.

Finally, in Chapter 4, a double noise-cancelling wideband receiver circuit by improving the performance of a wideband receiver with high immunity to blocker signals is designed. In previous receivers, the LNTA was operated in two modes depending on the situation. In the improved receiver, the G_m ratio of the linearized LNTA was changed to achieve lower NF with high linearity, and the RF noise-cancelling technique was applied. The input matching and noise cancelling scheme introduced in the previous circuit was also applied and a wideband receiver circuit was designed to perform double noise-cancelling. As a result, the linearization and noise-cancellation of LNTA could be achieved at the same time, and the completed receiver circuit showed high IIP3 performance of 5 dBm with minimum noise figure of 1.4 dB. The FOM value shows the performance of the designed wideband receiver is at the state-of-the-art.

In conclusion, a receiver that can operate in wideband and tolerant to the blocker using the current-mode receiver structure was developed. A linearization method of transconductor was proposed to maintain high linearity without generating intermodulation components by blocker in RF band and the result was applied to LNTA to design a wideband receiver. A wideband receiver was fabricated by applying the techniques for input

matching and noise cancellation. The measurement results demonstrate that the proposed method is suitable for practical SDR receivers.

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초록

본 논문에서는 실용적인 SDR 수신기를 구현하는 방법 중 하나로 광대역 수신기를 연구한다. 광대역 수신기의 가장 큰 문제인 대역 외 방해 신호(blocker)를 분석하고, 이를 효과적으로 제거하는 방법을 연구하였다. 이전 연구를 검토한 결과 방해 신호 제거를 위한 방법으로 전류 모드 수신기(current-mode receiver) 구조를 정하였으며, 광대역 수신기를 개발하고 blocker를 제거하려고 시도했다. 단계별 연구의 내용은 다음과 같다.

첫 번째로, 전류 모드 수신기의 기초 블록이 되는 저잡음 트랜스컨덕턴스 증폭기(low-noise transconductance amplifier, LNTA)의 선형성에 주목하였다. 전류 모드 수신기에서 LNTA는 낮은 잡음 지수를 달성하기 위해 높은 트랜스컨덕턴스 (G_m) 값을 가져야 하지만, 높은 G_m 값은 낮은 선형성을 야기한다. 이러한 트레이드-오프를 해결하기 위해 트랜스컨덕터의 선형화 방법을 제안하였다. 제안된 기술은 2 개의 경로를 사용하여 피드-포워드 방식으로 3차 상호 변조 성분(third-order intermodulation distortion, IMD3)을 제거하는 것이다. $2G_m$의 트랜스컨덕턴스를 가지는 트랜스컨덕터가 주 경로에 배치되고, 이득이 $\sqrt[3]{2}$인 증폭기와 G_m 크기의 트랜스컨덕터가 보조 경로에 위치하는 구조이다. 이 구조는 약간의 fundamental 신호 손실이 존재하지만 IMD3 성분을 출력에서 상쇄되도록 한다. 결과적으로, 전체 트랜스 컨덕터 회로는 제거된 IMD3 성분으로 인해 높은 선형성을 가질 수 있다. 선형화된 트랜스컨덕터를 사용하여 재구성이 가능한 고역 통과 필터를 설계하였고, 그 성능을 입증하였다. 제작된 회로는 19.4 dBm의 높은 input-referred third-order intercept point (IIP3) 성능을 달성했다.

다음으로, 선형화된 트랜스컨덕터를 더욱 개선한 설계를 진행하였다. 선형화된 트랜스컨덕터는 선형화를 위해 사용된 추가 회로 때문에 잡음지수가 매우 높기 때문에, 잡음지수 분석을 통해 LNTA에 적용하기 위한 보다 적합한 형태를 제안했다. 개선된 LNTA는 blocker가 없을 때는 저잡음 모드에서 작동하도록 설계 되었으며, blocker가 있을 때는 고선형성 모드에서 작동하도록 전환할 수 있다. 또한 광대역 수신기 회로의 잡음 지수 성능을 향상시키기 위해 수신기에 잡음 제거(noise-cancelling) 기술을 적용했다. LNTA, 믹서 및 기저 대역 트랜스임피던스 증폭기(transimpedance amplifier, TIA)로 구성된 전류 모드 수신기 구조에 피드백 경로가 추가되었으며, 잡음 신호는 이 피드백 경로를 사용하여 감지될 수 있다. 또한 이 피드백 경로는 넓은 대역폭에서 수신기의 입력 정합을 50 옴으로 유지하는 역할도 수행한다. 수신기에 보조 경로를 추가함으로써 대역 내 신호는 증폭시키고 검출된 잡음은 기저대역에서 제거되도록 하였다. 완성된 회로는 0.025 GHz에서 2 GHz까지의 광대역 성능을 보였고, 고선형성 모드에서 −6.9 dBm의 IIP3 성능을 보였다.

마지막으로 방해신호에 강한 내성을 가지는 광대역 수신기의 성능을 개선하여 이중 잡음제거 광대역 수신기 회로를 설계하였다. 이전 수신기에서는 상황에 따라 LNTA를 두 가지 모드로 동작시켰지만, 개선된 수신기에서는 선형화된 LNTA의 G_m 비율을 변경하고 RF 잡음 제거 기법을 적용하였다. 이전 회로에서 도입된 입력 정합과 잡음 제거 기법 또한 적용되었으며, 잡음 제거를 이중으로 수행하는 광대역 수신기 회로를 설계하였다. 그 결과 LNTA의 선형화와 잡음제거를 동시에 달성할 수 있었고, 완성된 수신기 회로는 최소 잡음지수 1.4 dB와 5 dBm의 높은 IIP3 성능을 보였다.

결론적으로, 본 논문에서는 트랜스컨덕터 회로의 선형화 기법을 제안하였고, 전류 모드 수신기를 기반으로 한 광대역 수신기를 설계하였다. 설계된 수신기 회로는 낮은 잡음지수 성능과 높은 IIP3 성능을 보여, 외부 방해신호에 강한 내성을 가짐을 실험적으로 검증하였다.

주요어 : 광대역 수신기, 방해신호, 선형성, 트랜스컨덕터 선형화 기법, 노이즈 제거

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