Ph.D. DISSERTATION

Study on the Zn-Sn-O field effect transistors for the application to transparent and flexible display devices

by

Sungmin Kim

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Department of Materials Science and Engineering

College of Engineering

Seoul National University

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Advisor : Prof. Hyeong Joon Kim

By

Sungmin Kim

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Approved

by

Chairman of Advisory Committee : <u>Cheol Seong Hwang</u>

Vice-chairman of Advisory Committee : <u>Hyeong Joon Kim</u>

Advisory Committee : <u>Ho Won Jang</u>

Advisory Committee : <u>Jae Kyeong Jeong</u>

Advisory Committee : <u>Bong Seop Yang</u>

Abstract

In recent years, the display devices focused on user experience such as curved, flexible and transparent features. Since conventional silicon-based thin film transistors (TFTs) have a limit in flexibility and transparency, it is necessary to develop new materials with these properties. Therefore, amorphous oxide semiconductors (AOSs) such as $InGaZnO_x$ (IGZO) and $ZnSnO_x$ (ZTO) have attracted attention as a new active-layer materials of the TFTs in display devices due to the need for channel materials that have flexibility and productivity. ZTO is especially taking the spotlight as it has none of expensive rare-earth elements as well as high mobility and superior productivity.

ZTO has superior electrical properties, but there are still problems to be solved to apply them to the flexible devices. To fabricate a flexible device, it is necessary to introduce polymer substrates with thermal resistance, such as polyethylene naphthalate (PEN) or poly arylate (PAR), which resist heats up to 200 °C. Whereas conventional process for fabrication of ZTO TFTs need a thermal treatment over 350 °C, which is excessively high than the heat resistance temperature of the polymer substrate. Therefore, it is essential to develop a process which can achieve the transistor properties of oxide semiconductor even at low temperature under the limit of polymer substrate.

Also, there is a lack of understanding of the phenomenon that occurs when a flexible display device using the ZTO exposed to external stress. Generally, the external stresses applied to the flexible display devices are the illumination from the back light unit and the mechanical stress.

In this dissertation, the studies on the ZTO TFTs for the application to transparent and flexible devices were conducted. First, the experiments carried out to lower the maximum process temperature in order to make the ZTO devices applicable to the polymer substrates which have process temperature limit of 200 °C or less. Conventional ZTO should be annealed at 350 °C or higher after the deposition using an RF sputtering system. This annealing process makes atomic bonds tight and enhances to react the oxygen vacancies with oxygen. Instead of post annealing process, the inter-bonding among atoms and relief of oxygen vacancy occurred through heating the substrate and adding oxygen in the process chamber. As a result, it was possible to fabricate devices that show excellent electrical characteristics with field effect electron mobilities of $5.8 - 27.1$ cm^2 V^{-1} s^{-1}, I_{on}/I_{off} of 10^8, and subthreshold swing of $0.15{\sim}1.7$ V dec^{-1}, which are similar to those of the devices fabricated by the conventional process, even though lowering the process temperature by more than 150 °C.

As a result of measuring the thin film density by X-ray reflectometry, the films deposited at room temperature had the density of 5.5 g cm^{-3}, 5.7 g cm^{-3} and 5.9 g cm^{-3} after deposition, post-heat treatment at 200 °C and 350 °C, respectively. The more dense films were formed as the annealing temperature increased. In the case of the in-situ annealing deposition, the density of 5.9 and 6.0 g cm^{-3} was observed at the 150 ° and 200 ° processes, respectively. It was confirmed that a dense thin film can be formed even at a low temperature through the in-situ annealing deposition. In addition, the surface roughness using an atomic force microscope was also improved with in-situ annealing.

The ZTO thin film deposited at room-temperature after post-annealing at 150 °C had a root mean square roughness of 1.81nm, whereas the thin films after in-situ annealing had the roughness of 0.33 ~ 0.43nm, which are improved more than four times better than that of the conventional post annealing method.

Transmission electron microscopy analysis showed the effects of in-situ annealing process indisputably. In the samples deposited at room temperature, a complete amorphous phase was observed even with the post deposition annealing at 350 °C. These results inform that the ZTO clusters deposited on the heated substrate have a sufficient kinetic energy due to high temperature and be movable filling the physical vacancies and forming the crystalline phase which stabilize the electrical properties of ZTO TFTs . Therefore, it has been confirmed that the density increase and the improvement of the roughness occurs together.

These results show that the ZTO clusters deposited on the heated substrate have sufficient kinetic energy due to thermal energy and move to fill the physical pores, and thus the density increases and the roughness decreases.

The ultimate goal of lowering the process temperature was to fabricate the ZTO TFT devices on polymer substrate which have transparency and flexibility. ZTO-TFTs possessing transparency and flexibility were successfully fabricated on the 125 μm thick PEN substrates. They showed electrical properties with a mobility of 9.7 cm^2 V^{-1} s^{-1}, I_{on}/I_{off} of 10^8, and subthreshold swing of 0.28 V dec^{-1}. The devices on the polymer substrates performed good enough to be applied to commercial electronic devices.

Secondly, the effects of external stress on the properties of flexible ZTO TFTs were studied. As mentioned above, ZTO TFTs are widely used in display devices based on the advantages such as transparency and flexibility. When applied to a flexible display device, the ZTO TFTs are exposed to the illumination stress from the back light unit and the mechanical stress caused by the bending. Therefore, it is very important to analyze the reliability of the devices under such stress conditions. The device was fixed in convex and concave jigs with a radius of curvature of 20 mm, and performed reliability analysis by irradiating the light of 450 and 500 nm wavelength under the condition of mechanical stress. As a result, when light was illuminated on the convex jig, the threshold voltage of the TFT moved more toward lower voltage with the tensile stress. Tensile stress tended to deteriorate the reliability of the ZTO TFT devices. On the contrary, when the compressive stress was applied to the devices by fixing on the concave jig, the threshold voltage shift was lowered in the stress state.

To analyze this phenomenon, the way for applying different stress states to the equally deposited ZTO thin films on a transparent PEN substrate was studied, and a method of independently differentiating stress without changing the chemical composition was suggested. The optical band gap measurement using UV-vis spectrometer and elemental analysis using ultra-violet photoelectron spectrometer were performed to analyze the valence band maximum (VBM) and work function. As a result, when the compressive stress was applied up to 0.6 %, the bandgap and VBM increased. It is found that the energy differences between conduction band minimum and fermi level (E_F)

decrease with increasing compression. And the reliability of the devices have correlation with the applied mechanical stress which means that it can be possible to enhance the photo-bias stability by adopting appropriate mechanical stress.

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Chapter 1. Introduction

1.1 Overview

Conventionally, silicon based TFTs has been used in the drive circuits and switching device of the general electronics. In early days, hydrogen passivated amorphous silicon (a-Si:H) was used for the channel material in TFTs. However, silicon has a mobility of 1 $cm^2\ V^{-1}s^{-1}$ or less, which makes it difficult to use it on the electronics with advanced speed or displays with high resolution. Since then, this technical barriers were overcome using low-temperature polycrystalline silicon (LTPS) by crystallizing the amorphous silicon layer which exhibit higher carrier mobility ($\sim$100 $cm^2\ V^{-1}s^{-1}$). However, since the electronics become faster and the screens get bigger with the resolution over high-definition (HD), the grain boundary of the polycrystalline becomes obstacle to the uniformity. Therefore, nanocrystalline silicon with reduced grain size has been used since then, but the uniformity and the carrier mobility are in a trade-off relationship, so there is a clear limit without replacing the material itself.

Moreover, the newest electronics make appeal to customers based on user experiences such as flexibility, curvature, and transparency in the recent trends in electronics. In this situation, amorphous oxide semiconductors (AOSs) such as zinc tin oxide (ZTO), indium gallium zinc oxide (IGZO), etc., are being studied exhaustively owing to the advantages of transparency, high electron mobility, and productivity. Unlike silicon whose conduction band is composed of oxygen 2p orbitals which have directions, the band of oxide

semiconductor is made of metal ns orbitals which have spherical shapes without orientations. Therefore, even when amorphized for uniformity, the conduction path is maintained without breaking and exhibit high carrier mobility. Furthermore, other electrical properties such as the threshold voltage, subthreshold swing and on/off current ratio are superior to Si-based TFTs. The comparison of oxide semiconductor with other materials for channel layer of TFTs was summarized in Table 1.1.1[1-6] and Fig.1.1.1 AOS has merits on the low cost fabrication not only that a higher carrier mobility than Si-based devices. And it also has easier fabrication process and uniformity compared to those based on Si. As a result, AOS are considered much more favorable for high-end display devices than other competitor materials. Among the AOSs, ZTO does not contain rare elements, so it is cheaper than other materials such as IGZO and IZO, but still retains excellent electrical characteristics.

In order to adopt these oxide semiconductors as channel layers of flexible devices, it is necessary to fabricate them on polymer substrates. In general, an oxide semiconductor requires post annealing process to stabilize the interatomic bond after deposition, which may damage the polymer substrate. Although it has been reported that TFT devices are activated without annealing, there is a need to limit the entire process temperature because there are some processes that exceed the maximum process temperature limit such as dielectric fabrication process and encapsulation process. Moreover, there is insufficient research about how to improve the film quality by heating the chamber during deposition to a relatively low temperature compared to the conventional post annealing process.

And there is another problem that arises when AOSs are adopted in flexible devices. As shown in Fig.1.1.2, when the passivation layer which blocks moisture and gas is added with appropriate thickness, the neutral plane which is not mechanically stressed even it is bent in any condition. However, it is impossible to remove the stress applied to all devices by this method because devices are stacked in many layers in the latest advanced devices. For the next generation electronics, it is very essential to study what kind of material and electrical change the thin film has undergone and its mechanism with the stress state applied to the devices. Up to now, Munzenrieder and Shin [7-9] reported the effects of mechanical stress on the AOSs. However there was no analysis on the effects of bending from the point of view focused on the energy band of materials and photo reliability.

In this dissertation, the study was exerted about the TFTs based on zinc tin oxide and fabricated the device by strictly limiting the whole process temperature to 150 °C and 200 °C which means that the ZTO can be sputtered on the polymer substrates. And the fabricated devices exhibited considerable characteristics at a low process temperature. The entire process temperature was strictly limited such that the given temperatures were not exceeded even during dielectric fabrication and encapsulation. And the analysis about the effect of heating during deposition (in-situ annealing) of ZTO TFTs was conducted to confirm that in-situ annealing improves the deposited thin film quality. It is confirmed that the process occurring at 150 and 200 °C is effectively equivalent to the conventional post-deposition annealing at 300 °C or more.

In addition, the improvement in the reliability of ZTO-TFTs was successful with in-situ annealing process. The reliability test with negative biased illumination stress (NBIS) condition proved this, and the devices fabricated at 150 °C exhibited reliability like the devices annealed at 250 °C or higher after deposition.

And the study was also made on the changes occurring in the case where the oxide semiconductor is mechanically strained. 3 jigs were fabricated with convex, concave and flat surface, and the flexible ZTO films were fixed on it to put the mechanical stress. Then, the deterioration and enhancement of the photo-induced reliability with NBIS condition was analyzed as the change of mechanical states. The effect on the energy band was analyzed with compressed ZTO layers on PEN substrate. VBM levels of ZTO layers were measured by UV photoelectron spectroscopy (UPS), and the optical bandgaps were extracted from the transmittance data by UV-Vis spectroscopy.

And a study was conducted on the changes that occur when repetitive stresses are applied on the ZTO TFTs and ZTO itself. The change in electrical properties and chemical composition were analyzed by semiconductor analyzer and X-ray photoelectron spectroscopy (XPS) to identify what occurred on a flat surface after repeated folding and unfolding rather than curved state.

Table 1.1.1 Comparison of oxide, Si and organic TFTs. [10, 11]

Property	Oxide	amorphous-Si	Low-T poly-Si	Organic
Carrier mobility (cm^2/V·s)	~ 100	< 1	50 ~ 100	0.1 ~ 10
$\triangle V_{TH}$	- 0.5 V	< 3 V	< 1×10^{-2} V	< 1 V
S.S (V/decade)	0.1 ~ 0.6	0.4 ~ 0.5	0.2 ~ 0.3	0.1~5
Leakage current (A)	10^{-13}	10^{-12}	10^{-12}	10^{-12}
Process Temp. [ºC]	RT ~ 400	~ 250	~ 500	RT~200
Manufacturing cost	Low	Low	High	Low
Long term TFT reliability	High	Low	High	Low in air
TFT uniformity	Good	Good	Poor	Fair
Yield	High	High	Medium	High
Application	AMLCD, AMOLED	AMLCD	AMOLED	AMOLED
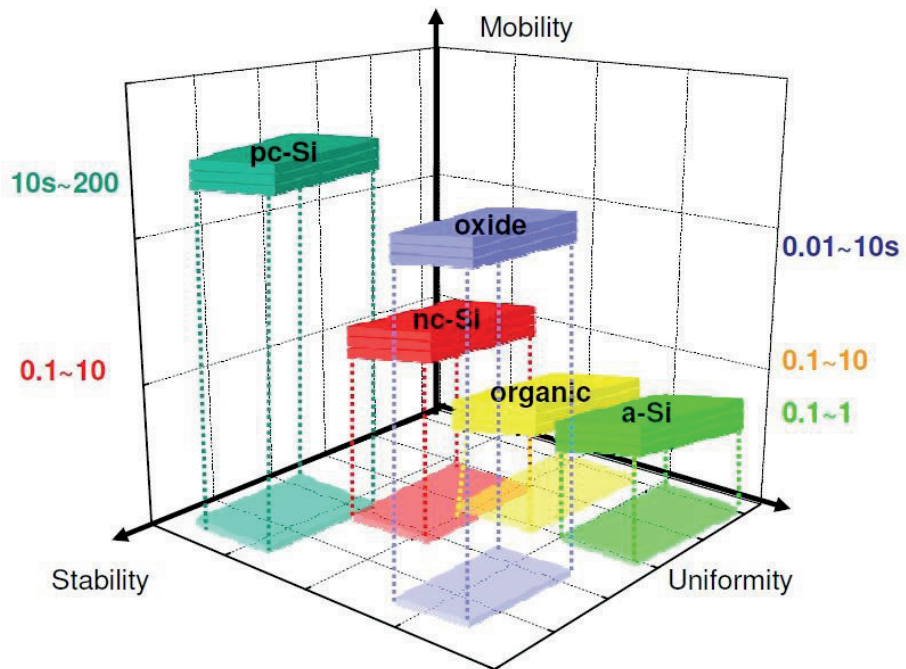
Figure 1.1.1 Comparison of silicon, oxide and organic channel[12]

Table 1.1.1 Summary of physical properties of various metal oxide. [11, 13-15]

Property	In_2O_3	ZnO	SnO_2	β-Ga_2O_3
Mineral name	-	Zincite	Cassiterite	-
Abundance of the metal in the earth's crust (ppm)	0.1	132	40	16.9
Crystal structure	Cubic, bixbyite	Hexagonal, wurtzite	Tetragonal, rutile	monoclinic
Lattice constants [nm]	a = 1.012	a = 0.325 b = 0.521	a = 0.474 b = 0.391	a=1.221 b=0.304 c=0.580
Density [g cm^{-3}]	7.12	5.67	6.99	5.95
Thermal expansion coefficient (300K) [10^{-6}K^{-1}]	6.7	$\parallel$ c: 2.92 $\perp$ c: 4.75	$\parallel$ c: 3.7 $\perp$ c: 4.0	
Melting point [°C]	2190	2240	>1900	1725
Static dielectric constant	~9	$\parallel$ c: 8.75 $\perp$ c: 7.8	$\parallel$ c: 9.6 $\perp$ c: 13.5	9.9~13.9
Refractive index at 500 nm wavelength		2.008		$\parallel$ [010]:1.95 $\perp$ (100):1.92
Bandgap [eV]	3.75	3.4	3.6	4.85
Electron Hall mobility	200 cm^2 V^{-1} s^{-1}	200 cm^2 V^{-1} s^{-1}		< 1
Hole Hall mobility	5-50 cm^2 V^{-1} s^{-1}	5-50 cm^2 V^{-1} s^{-1}		< 1

Tensile strain

TFT

Compressive strain

Neutral plane

Substrate

Tensile strain

TFT

Passivation layer

Compressive strain

Neutral plane
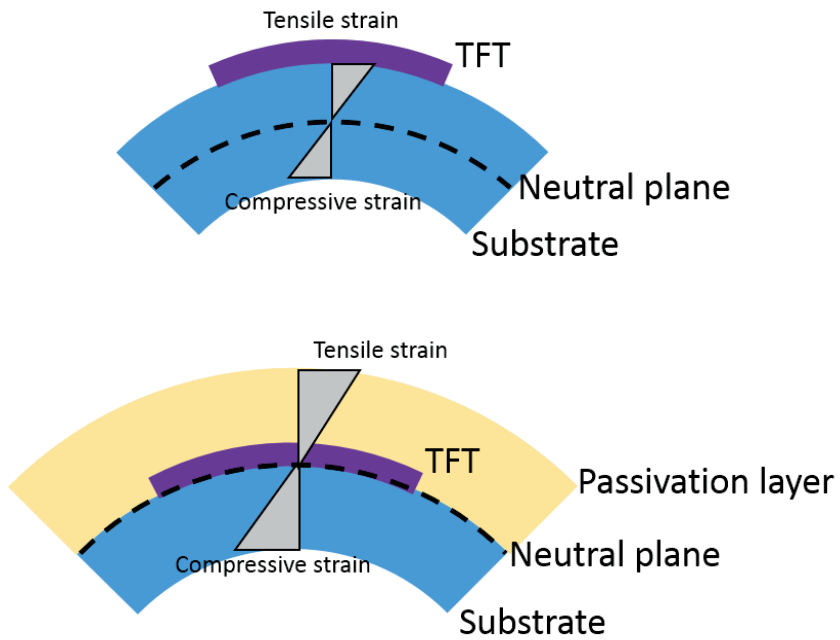
Substrate

Figure 1.1.2 Mechanical stress applied to the inside of the substrate and TFT while bent (up), and a stress state when passivation layer is added (down)

Chapter 2. Literature Review

2.1 Oxide semiconductor thin-film transistors

2.1.1 Device structure

Unlike general silicon-based semiconductors, oxide semiconductors have high degree of freedom in choosing the substrate, electrodes, insulator, and channel layers because they are all deposited by deposition methods such as sputtering, chemical vapor deposition (CVD), and atomic layer deposition (ALD).[16] Fig.2.1.1 shows the typical structure of TFTs.[16, 17] Staggered structure means that source and drain are on opposite side of semiconductor while coplanar structure has them on the same side of TFTs. And these structures can have two types of gate electrode, top and bottom. The staggered bottom gate structure is used in devices with poly-Si and a-Si:H in liquid crystal displays (LCDs). The gate electrode in this structure roles as a screen which prevent the degradation effects of the channel layers by the illumination stress from back light unit (BLU). The coplanar structure is unusual cases for the a-Si:H TFT. These structures are chosen according to the characteristics required by the device such as producibility, electrical properties and process integration.[18, 19] In this study, the bottom gate structure was used, which makes it easier to control the channel layer properties by adjusting the reaction with the environment during annealing or additional treatment. And additional treatments can be easily added for various purposes during and after deposition process. For example, a plasma treatment is added to improve electrical characteristics after deposition. And

the insulating layer can be also added on the top of the devices to improve accuracy of etching depth in the channel layers without damaging the gate dielectric surfaces.[20] And insulating layer on the top of the devices can act as a passivation layer which protect the active layers from moisture, oxygen, and other reactive factors. They are known as electron sources, and causing the change of conductivity of channel material.[21, 22]
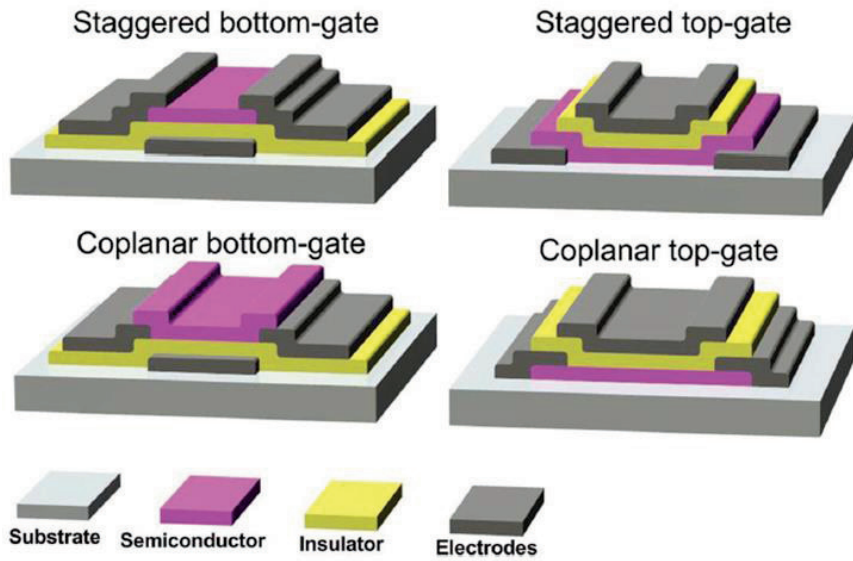
Figure 2.1.1 Schematic diagrams of typical TFT structures. [23]

2.1.2 Operation of thin-film transistors

Operation mechanism of thin film transistor (TFT) is same as the metal oxide semiconductor field effect transistor (MOSFET) in typical electronics such as microprocessors. However, there are some differences between TFTs and MOSFETs. Fig.2.1.2 shows comparison between the typical structures of TFTs and MOSFETs.[17] In MOSFETs, the silicon wafers are substrates and the channel and electrodes are defined by doping elements like phosphor and nitrogen. And the insulating layers are made by oxidation of silicon substrates. In TFTs, various substrates can be used because every layers are fabricated by deposition. Therefore, TFTs have many options to choose electrode, channel and insulator materials. Also, there are difference in the maximum process temperatures between these two devices. Oxidation of Si substrates is essential in forming the insulator layer of MOSFET devices, and it usually occurs over 1000 °C. While TFTs processing temperatures are limited by the thermal resistances of each components of devices, and they typically does not exceed 600 °C.[20] In addition, on/off operation in MOSFETs is based on the depletion mode which is relevant of p-n junctions between the source/drain and channel layer. The gate bias applied makes an inversion region in the channel, then the conduction layers are formed in the interface of channel layer to make electrons movable. However in TFTs, there are no p-n junctions between the components, and they operate in accumulation mode especially in AOS TFTs. This is related with another important difference in device characteristics.
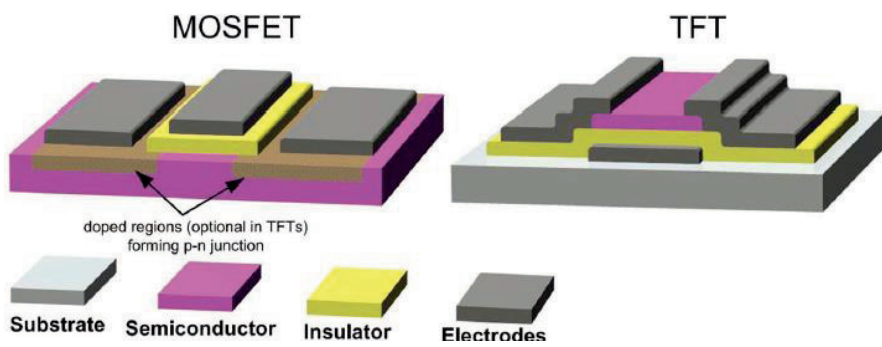
Figure 2.1.2 Comparison between the typical structures of MOSFETs and
TFTs. [23]

2.1.3 Electrical properties of thin film transistors

The electrical properties of TFTs are same with MOSFETs, the well-known characteristics such as drain current on/off ratio, channel mobility (μ), threshold voltage (V_{th}) and subthreshold swing (S.S). Analysis of electrical properties of devices are extracted from the transfer curve of TFTs according to the equations in the following paragraphs.

2.1.3.1. Channel mobility (μ)

Channel mobility is a factor which represent the availability of carrier transport in a channel layer. The degree of mobility is affected by several mechanisms, such as lattice vibrations, ionized impurities, grain boundaries and other structural defects.[23] Because of the movement of carriers is constrained to a narrow channel region close to the interface, additional sources of scattering should be considered, such as Coulomb scattering from dielectric charges and surface roughness scattering. The MOSFET equations for thin film transistor are shown following.

In linear region which means drain voltage are lower than gate voltage minus threshold voltage,

$$I_{D,lin} = \frac{W}{L} \mu_{FE} C_{ox} \left(V_G - V_{th} \right) V_{DS}$$

And conductance g_m is as follows,

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$$

And when V_{DS} is constant,

$$g_m = \frac{W}{L} \mu_{FE} C_{ox} V_{DS}$$

Field effect mobility (μ_{FE}) can be extracted from this equation,

$$\mu_{FE} = \frac{L \, g_m}{W \, C_{ox} V_{DS}}$$

And in saturation region which means the drain voltage exceeds gate voltage minus threshold voltage, saturation mobility (μ_{sat}) is extracted as follows,

$$I_{D,sat} = \frac{W \mu_{sat} C_{ox}}{2L} (V_G - V_{th})^2$$

Therefore,

$$\mu_{sat} = \frac{2L}{W C_{ox}} \left(\frac{I_{D,sat}}{(V_G - V_{th})^2} \right) = \frac{2Lm^2}{W C_{ox}}$$

When m is slope of $\sqrt{I_{D,sat}} - (V_G - V_{th})$ plot, L is the channel length, W is the width, and C_{ox} is the gate capacitance of oxide per unit area.

2.1.3.2. Threshold voltage (V_{th})

Turn-on voltage and threshold voltage (V_{th}) has different physical meaning and which can be defined using several methodologies.[24] In this study, V_{on}/V_{th} were defined as the gate voltage which induces a drain current of L/W x 10 nA at V_{DS} = 10.1 V.[25] The extraction of V_{on}/V_{TH} in this way is frequently used because the analog driver in the actual unit pixel of AMOLED panel is loaded between 1µA and 1nA. Here, the roughly 1 µA and 1 nA are needed to embody the full-on and black gray scale for AMOLED devices, respectively. Although this type of V_{th} definition does not have a unique physical meaning, the gate voltage to induce a drain current of 10 nA can be a very useful guideline for the panel design as well as the process control.

2.1.3.3. Gate controllability

Gate controllability is represented by drain current on/off ratio (I_{on}/I_{off}) and subthreshold swing (S.S). I_{on}/I_{off} is a parameter for switching device and defined by the ratio of the on current to off current. For example, Fig.2.1.3 shows the transfer and output characteristics of ZTO TFTs. In this ZTO TFT device, the on/off ratio is about 10^7. S.S indicates how fast the gate can turn on and off the channel. The value of S.S is estimated using a log plot in the section when the TFT turns on from off states with steep slope near 0 V of gate voltage in the transfer curve of Fig.2.1.3. S.S is the inverse of the maximum slope in this area. S.S can be an useful parameter of how effectively the TFTs turn on by the gate bias.
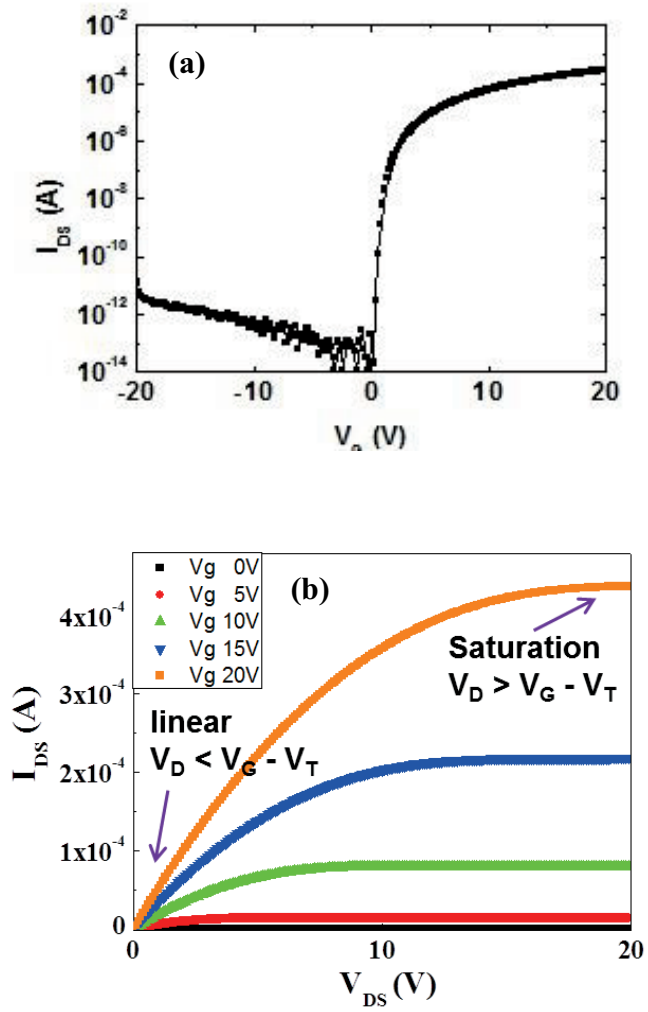
Figure 2.1.3 (a) Transfer curve and (b) output curve of ZTO TFTs

2.2 Electrical instability of the oxide TFTs

2.2.1 Overview

Oxide TFTs are used in driver circuit of unit pixels for flat panel displays and have potential to be adopted in a flexible display based on their superior electrical properties as compared with Si-based devices such as a-Si:H and poly-Si, including a high mobility, excellent uniformity, and good transparency to visible light.[26] The device reliability against a gate bias and illumination stress remains a critical issues remaining to be resolved before their implementation in commercial electronic products.[26, 27] Fig.2.2.1 shows schematic cross section of the oxide TFT and illumination path by the backlight.[28] To simulate this environment, negative biased stress (NBS), positive biased stress (PBS), negative biased illumination stress (NBIS), positive biased illumination stress (PBIS) tests are generally conducted. Fig.2.2.2 shows evolution of the transfer curves as a function of the bias stress time. The V_{th} has a parallel shift to the positive or negative direction by gate bias stress without change in mobility and subthreshold slope value.[29] The TFTs in the displays inevitably suffers light stress from the back light unit and external visible light. And every TFTs are always under negative gate bias stresses except they receive a signal as an active row. In this regard, NBIS condition is the most similar situation with an environment in real display devices. Therefore, intensive efforts have been made to understand the origin of this NBIS instability. NBIS condition induced instability is still one of the crucial obstacles in the practical application. There are some reports about the reason of photo-biased instability. The first one is related to the charge

trapping. The trapping of electron, hole and other charged chemical species such as oxygen vacancy accumulated in the channel/insulator interface[30] screens or enhances the electrical field applied to the channel by the gate bias. Then, there are unwanted on/off operation of channel. The second one is induced by the carrier generation. When the carriers are created due to some reason such as increased hydrogen interstitial sites, the number of carriers existing in the channel is increased or decreased, the threshold voltage may be changed. Here are more specific description below.

2.2.2 Charge trapping model

Two degradation models are related with charge trapping model, which can be considered as plausible origins. First one is the photo-induced hole trapping,[31-34] and the second is photo-transition from V_O to V_O^{2+} [35] and As shown in Fig.2.2.3, the hole trapping model assumes that photo-generated hole carriers drift toward the gate insulator by the negative electric field and are trapped at the gate dielectric/channel interfacial trap sites or gate dielectric bulk film.[32]

Another mechanism is describing that a V_O defect center acts as the source of hole carriers via V_O mediated e-h pair generation during NBIS.[36] In this model assumes that photo irradiation causes the transition of neutral oxygen vacancies $[V_O]$ to the +2 charge states $[V_O^{2+}]$. The $[V_O]$ forms a deep state and the $[V_O^{2+}]$ state donates two electrons into the conduction band as shown in Fig.2.2.4. Therefore, under illumination condition, the photo-transition from $[V_O]$ to $[V_O^{2+}]$ can cause an increase free electron carrier

density, leading to increase of conductivity of channel layer and a negative V_{th} shift.

2.2.3 Carrier generation models

The degradation of photo-reliability can also be considered as a result of photo-desorption in the surface for the negative V_{th} shift under NBIS duration as shown in Fig.2.2.5.[37-39] Because the change in surface coverage with oxygen groups on the back channel surface can affect the number of electron in channel layer during NBIS. By oxygen adsorption from ambient electron depletion layer are formed on the back channel surface in air ambient. Light-illumination can causes desorption of oxygen species on the back channel surface. This photo desorption of adsorbed oxygen releases delocalized electrons into the channel layer. As the result, the free electron density will be increased compared to that of the dark state, leading to increase of conductivity of channel layer and a negative V_{th} shift.

In order to verify these models, the effect of ZrO_2 incorporation in the ZTO film and field effect transistors was investigated and the photo-bias stability of ZTO FETs by performing an ozone treatment was investigated. As similar approaches with ozone treatment, high pressure O_2 annealing and oxygen plasma treatments were demonstrated.[36, 40] However, the present study showed that a simple oxygen vacancy reduction model cannot explain all the experimental observations, and suggested that the surface chemistry of ZTO films related to the chemical adsorption on the back surface of the channel plays a crucial role. And the possible reasons for such highly stable behavior are also discussed in detail.

Recently, the reliability degradation model of oxide semiconductors often excludes the intervention of oxygen vacancy. Oxygen vacancy can exist only when there is a precise crystalline structure, and oxide semiconductors are generally used in an amorphous state. So there are some opinions that it is impossible to define an accurate vacancy state in amorphous structure of oxide semiconductor. Therefore, in recent models, photo-induced instability has been explained using interstitial or deficient sites, which may be more commonly observed in amorphous than oxygen vacancies.

Robertson, et al.[41] reported a model of the NBIS instability in IGZO based on the photo-excitation of electrons from oxygen interstitials. They created four random network models of IGZO with about 84 atoms by molecular dynamics by quenching a crystalline IGZO supercell from 3000K. This sequence was carried out using a full ab-initio density functional theory (DFT) calculation. Fig.2.2.7 shows the calculated formation energy of oxygen interstitial (I_O) as a function of E_F for amorphous IGZO, crystalline IGZO, and crystalline ZnO in the O-rich limit (O chemical potential μ_O of the O_2 molecule). It is shown that neutral I_O in a-IGZO has a lowest formation of I_O among three materials in that Figure In a-IGZO, neutral I_O has an low formation energy of 0.6 eV in its most stable position, and it becomes a negative value when E_F are approaching to E_C. Therefore, a-IGZO can easily forms compensating O interstitial with high E_F. Fig.2.2.6 shows a simplified bonding diagram of the O interstitial. A neutral oxygen atom has six electrons in its valence band which have eight empty sites. In other words, it has two holes in its 2p orbitals. O interstitial is reactive, and can form an O–O bond

with a network O^{2-} site. If it is combined with two hydrogens, their electrons fall down from the donor levels to fill the hole states, as shown in Fig.2.2.6 (b). The O becomes O^{2-} and no longer forms the O–O bond. Fig.2.2.6 (c) shows the effect of illumination to the O + 2H network. Two electrons are excited to the conduction band from O_I^{2-}. These conduction electrons give additional photoconductivity. Through a series of processes aforementioned, additional electrons are generated, which move the transfer curve by increasing the conduction of the channel.

And Y. Kang, et al.[42] reported the effects of interstitial hydrogen atoms in the oxide semiconductors. The bistability of the interstitial hydrogen in AOSs affects the reliability of oxide semiconductors. The simplified diagram of this model is shown in Fig.2.2.8. The details are as follows. H^{i-} and H-DX$^-$ are deep impurity levels, as shown in Fig.2.2.9, whereas all the H_i^+ and H_O^+ are shallow, which generates conduction electrons. Moreover, because a-InZnSnO$_x$ (IZTO) is an amorphous phase the deep levels of H_i^- and H-DX$^-$ are located broadly above the VBM. H-DX$^-$ is active compared to H_i^- on the visible light (low energy) illumination or the thermal excitation. And then, the following series of reactions occur and additional photo-electrons are generated. H-DX$^-$ is same with $(V_O^0 + H_i^-)$

$$H_i^- \left(V_O^0 + H_i^-\right) \rightarrow H_i^+ \left(H_O^+\right) + 2e^-$$
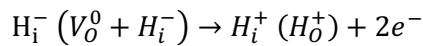
The electrons generated by hydrogen interstitial sites provide additional conductivity and the transfer curve moves.
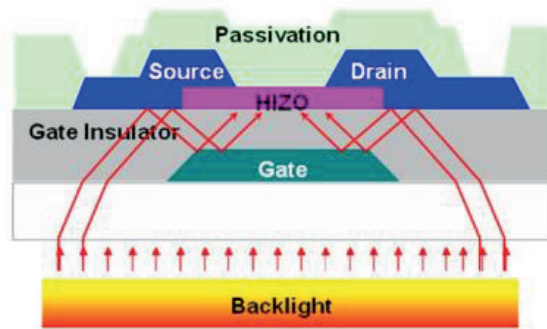
Figure 2.2.1 Schematic cross section of the TFT and illumination path by the backlight. [34]
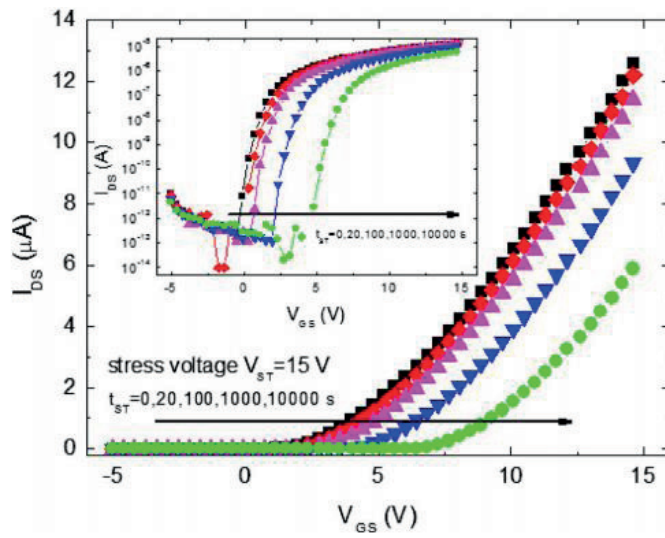
Figure 2.2.2 Evolution of the transfer characteristics of ZnO TFTs under positive or negative gate bias stress with/without light. [35]
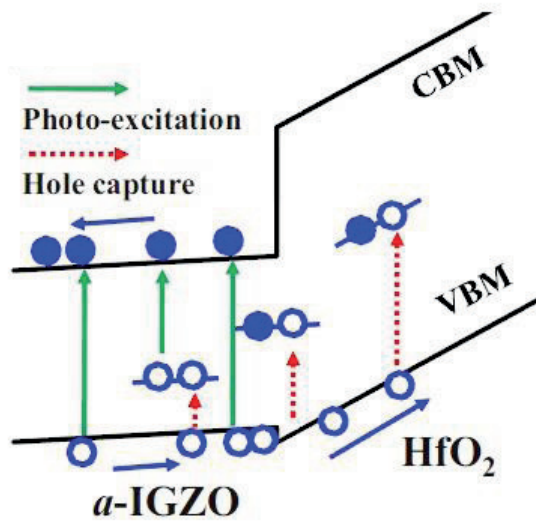
Figure 2.2.3 Schematic band diagram about photo induced hole trapping model. [43]
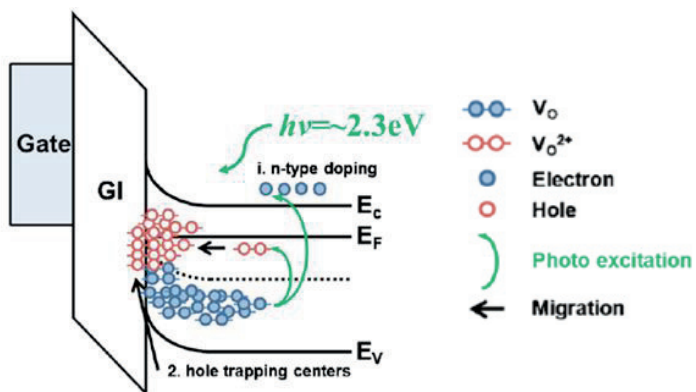
Figure 2.2.4 Schematic band diagram, which is based on transition of neutral oxygen vacancy [V_O] to [V_O^{2+}] charged state by photon irradiation. [44]

Light Surface sensitivity

$V_{DS}>0$

Source H_2O^+ O_2^- H_2O^+ O_2^- Drain

Channel

Back channel
surface conduction

Trapping and/or
defect creation

Dielectric

Gate

Bias Stressing
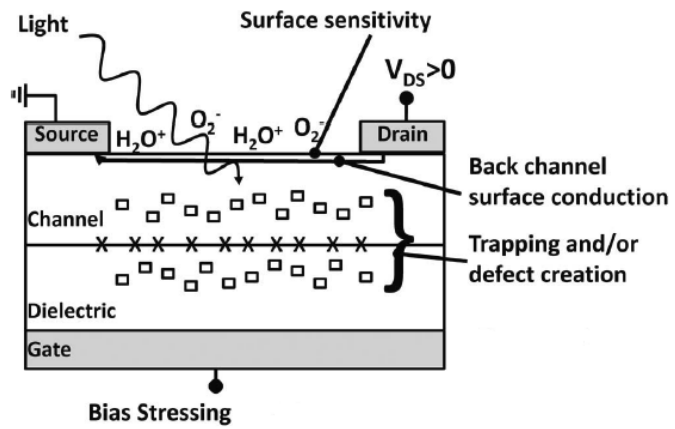
Figure 2.2.5 Schematic summary of the potential instabilities in the AOS TFTs.
[46]
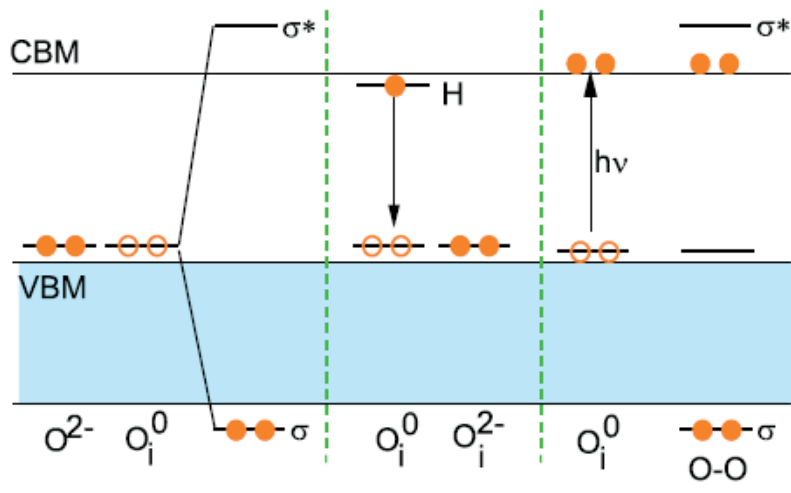
Figure 2.2.6 Schematic diagram of the effect of the oxygen interstitial site to photo instability in the AOS TFTs. [47]
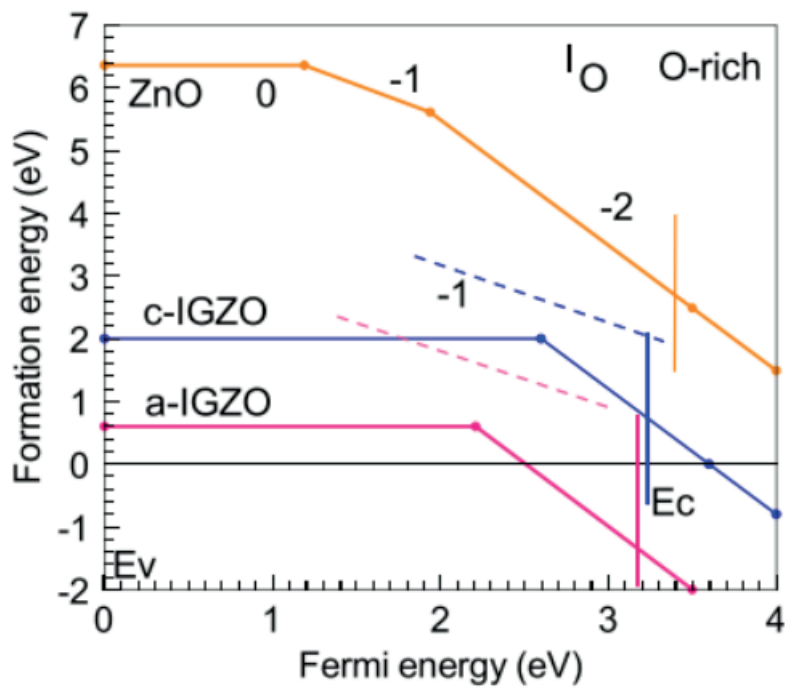
Figure 2.2.7 DFT-calculated defect formation energy for the O interstitial in a-IGZO, c-IGZO, and ZnO in the O-rich limit.[41]
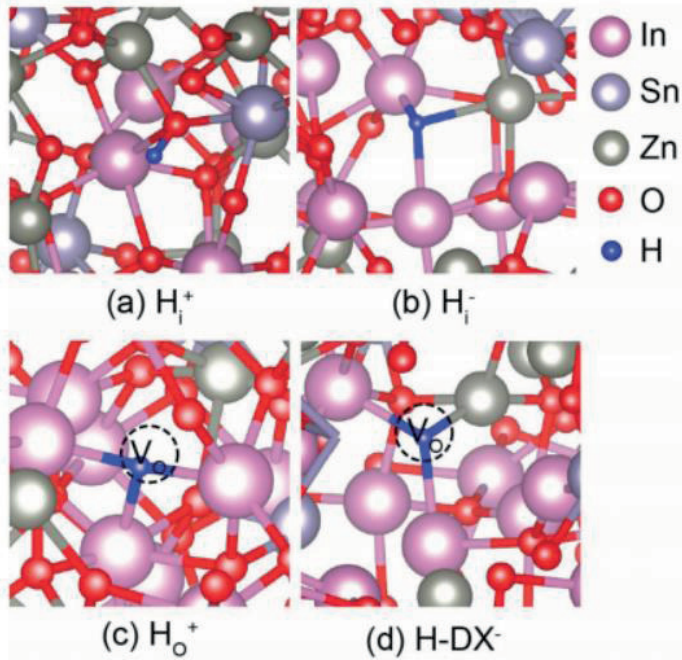
Figure 2.2.8 Atomic structures of (a) H_i^+, (b) H_i^-, (c) H_O^+, and (d) H-DX$^-$ in a InZnSnO$_x$ material [42]

(a) H_i^-

(b) H-DX$^-$

(c)

Conduction band

2.89 eV   2.45 eV   1.58 eV

H-DX$^-$

H_i^-

V_o

Valence band
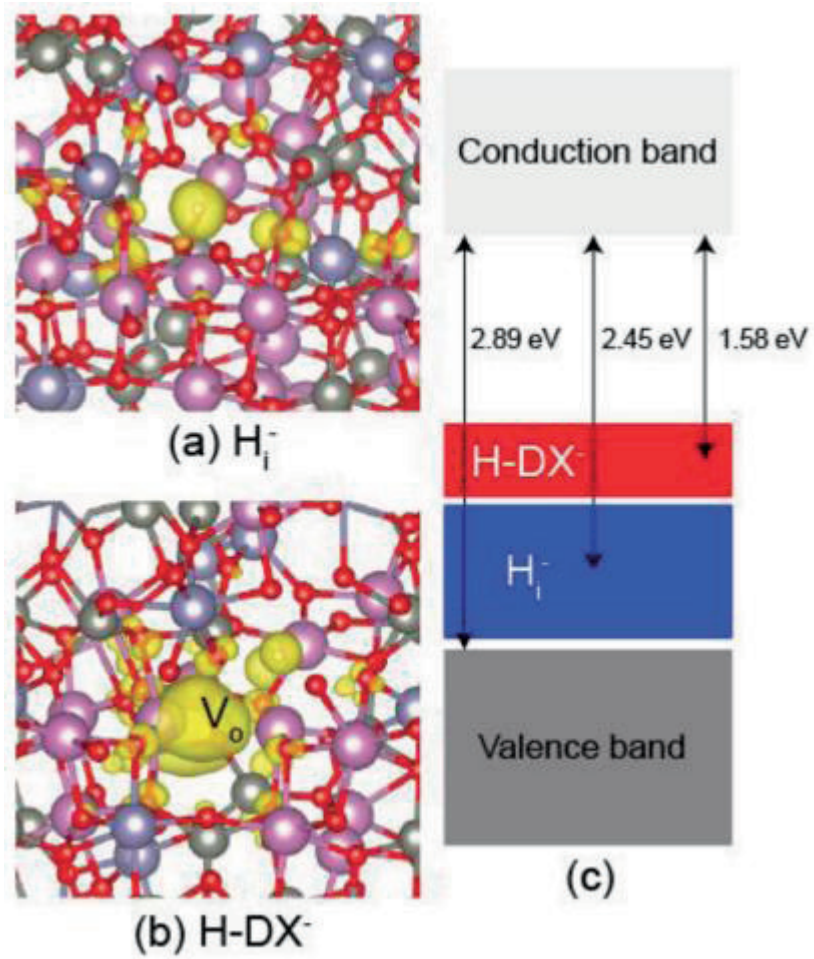
Figure 2.2.9 Schematic diagram of the energy distributions of various H states

Chapter 3. Experiments and Analyses

3.1 Sputter deposition of oxide films

RF magnetron sputtering systems (CS5000, SNTek) was used for the deposition of oxide semiconductor and ITO electrode layers. Fig.3.1.1 (a) and (b) are the sputtering system with cluster-type system and 4 sputter guns. The cathode which attracts the Ar ions to oxide targets were modified to enhance the magnetic field at the target surface.[45] The magnets behind the gun cathode was designed to maximize the magnetic field on the target surface and sputtering effects.

3.2 Deposition of ZTO and ITO films

In the experiments for chapter 4 and 5, 18-nm-thick ZTO and 70-nm-thick ITO film were deposited on p-type Si wafers and poly ethylene naphthalate (PEN) substrates. During deposition, a 3-inch diameter $ZnO:SnO_2$ (1:1 at%, iTasco) ceramic target and $In_2O_3:SnO_2$ (9:1 wt%, iTasco) target with 99.99% purity were utilized as the ZTO and ITO sources. The input power of ZTO and ITO target were fixed at RF 100 W and DC 55W respectively, while the deposition temperature of ZTO target was varied from RT to 200℃. The distance between the substrate and the target was about ~15 cm. The chamber base pressure was below 1.0×10^{-7} Torr. The sputtering was carried out at the chamber pressure of 5 mTorr and the oxygen to $O_2/(Ar+ O_2)$ gas ratio was varied from 0 to 0.2. The specification of detailed deposition condition for

ZTO films was summarized in Table 3.1.1. The ITO layer was used only as an electrode such as source and drain, and gate electrode in special cases.

(a)

(b)
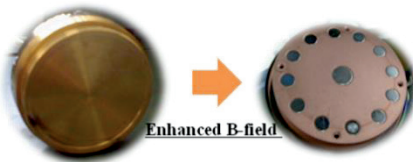
Figure 3.1.1 (a) Overview of RF magnetron sputtering system and (b) enhanced magnetic field structure of cathode (right) compared to the general type (left). Black circles in right figure are neodymium magnets.

Table 3.1.1 Process conditions of ZTO films.

	ZTO
Target	ZnO:SnO$_2$ (1:1 at %)
Sputtering Power (W)	100
Initial Pressure (Torr)	1.0×10^{-7}
Sputtering Pressure (Torr)	5.0×10^{-3}
Target-Substrate Distance (cm)	~ 15
Substrate Rotation Rate (rpm)	8
Substrate Temperature	Room Temperature
Sputtering Gas Flow (sccm)	Ar = 12~9.6
Reactive Gas Flow (sccm)	O$_2$ = 0~2

3.3 Thin film transistor fabrication

ZTO TFTs were fabricated by sputtering method with the system aforementioned. Channel layer consisting of 18-nm-thick ZTO layer was deposited by reactive RF magnetron sputtering on highly doped p-type silicon wafers which act as a gate electrode with a 100-nm SiO_2 gate dielectric layer. Then, a 70-nm-thick source/drain electrode composed of indium tin oxide (ITO) ($In_2O_3 : SnO_2 = 90 : 10$ *wt* %) was formed by the DC sputtering process at room temperature and Ar only atmosphere. The chamber pressure of 5 mTorr and the DC power was fixed 100 W. The channel and source/drain electrodes were patterned using a shadow mask with a channel length of 300 μm and a width of 1000 μm. After the deposition, the samples were annealed in an electrical furnace at a temperature of 150~350 °C for 2 hrs in air ambient, and for post-deposition annealed (PDA) samples, they are annealed at the temperature of 150~200 °C for 2 hrs in same atmosphere for in-situ annealed sample in chapter 4. Thin film transistor Fabrication process flow is summarized in Fig.3.3.1. The schematic diagram of the top-view images of this structure were shown in Fig.3.3.2. And the polymer passivation layer with poly (methyl methacrylate) (PMMA) on ZTO TFTs was formed by the spin coating method.
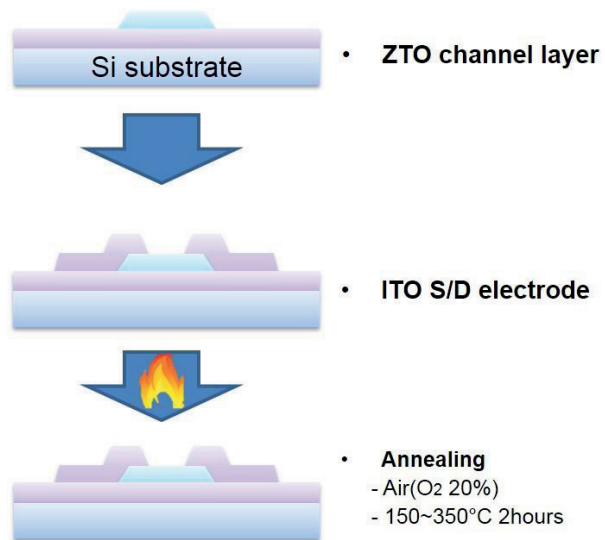
Figure 3.3.1 Thin film transistor fabrication process. Pupple layer on Si substrates is thermal oxide layer.
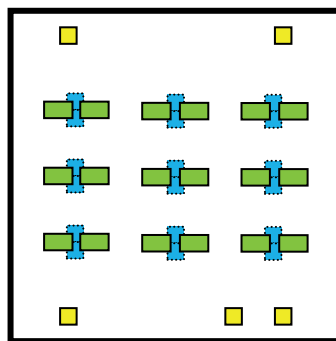
Figure 3.3.2 The schematic diagram of top-view image of TFTs. Yellow squares are align keys, rectangular shape of blue and green color indicates channel and source/drain electrode respectively.

3.4 Analysis Methods

The thickness of the oxide thin films was measured using a spectroscopic ellipsometry (ESM-300, J.A.Woollam). The surface roughness and the surface morphology of the films were investigated by atomic force microscopy (AFM) (JSPM-5200, JEOL) in scan area of 2.0 µm × 2.0 µm. The roughness was extracted from X-ray reflectivity (XRR) measurement data. Standard Θ-2Θ and glancing angle incidence X-ray diffraction (XRD, X'Pert-PRO, PANalytical) measurements were performed using Cu K_α radiation to evaluate the crystallinity of annealed oxide films High-resolution XRR measurements were performed to determine the roughness, density, and thickness of the ZTO thin films. The XRR data so obtained were fitted using the PANalytical X'Pert Reflectivity software. The microstructures of the thin films were analyzed using a transmission electron microscope (TEM) (F20, Tecnai and 2100F, JEOL). Magnification was up to 1 million times.

The electrical and reliability characteristics were measured using semiconductor analyzer (4155A, HP) at room temperature in air ambient. The V_{th} was determined by adjusting the gate voltage, which induces a drain current of L/W x 10 nA at V_{DS} = 10 V. [25] To characterize the effects of NBIS condition on the transfer curves of the ZTO-based FETs, the devices were stressed under the following conditions: a constant gate voltage (V_{th}-20 V) stress was applied as an electrical stress, while the applied drain voltage was 10 V at room temperature which represents the operation voltage in a display devices, and the maximum stress duration was 3,600 s. A white halogen lamp was employed as a light source and the photon wavelength was

approximately 450, 500 nm, which was selected by band-pass filters. The photo-intensity was 0.1 mW/cm^2 calibrated by photometry. The schematics of the illumination system were shown in Fig.3.5.1.
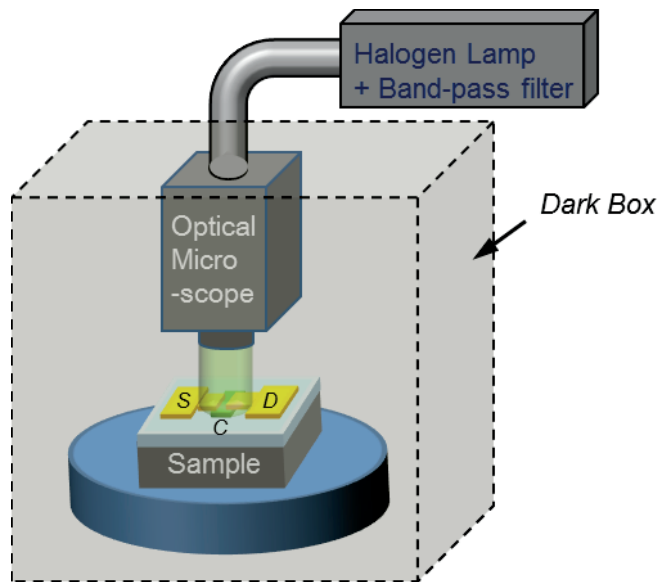
Figure 3.5.1. Schematic diagram of the illumination system for NBIS test.

Chapter 4. Low-temperature fabrication of amorphous zinc-tin-oxide thin film transistors with in-situ annealing process

4.1 Introduction

In the current display market, simply improving the speed or degree of integration no longer appeals to consumers as technology has reached that level where the public cannot notice the difference between the improved and older versions. Therefore, recent products are focused on user experiences such as curved, flexible, and transparent features by abandoning performance-oriented trends. As new channel materials for thin film transistors (TFT) used in high-performance displays, amorphous oxide semiconductors (AOSs) such as InGaZnO$_x$ (IGZO) [27, 46-48] and ZnSnO$_x$ (ZTO) [49-51] have attracted attention. They have outstanding properties such as high electron mobility (>10 cm^2 V^{-1} s^{-1}) as well as transparency and uniformity. Zinc tin oxide (ZTO) is especially attracting attention as it does not contain expensive rare-earth elements yet still has high mobility and low production cost. Therefore, the display industry has named it as the prime candidate for channel material in large-sized and flexible display devices. However, considering that substrates for future flexible displays should be polymer materials such as polyethylene naphthalate (PEN) or polyimide (PI), the current process for AOS has a critical drawback that it requires high temperature post-deposition annealing (PDA), over 350 °C, to activate transistor properties. Considering the maximum temperatures for the processing of PI and PEN are 260 °C and

220 °C, respectively, the temperature for overall AOS process should be lower than 200 °C to prevent the deformation of polymer substrates. In this regard, it is necessary to develop a low-temperature process that yields performance comparable to that of AOS-TFTs. Basic properties of commonly used polymer substrates are shown in Table 4.1.1.

Recently, a process for fabricating AOS-TFTs on polymer substrates at low temperatures has been studied. First, oxide films were deposited by conventional sputtering or spin-coating methods, followed by microwave irradiation [52, 53] or curing by UV annealing [54, 55]. Post-treatments such as microwave or UV annealing are widely used for spin-coated oxide channel layers. However, the sputtering process is still mainstream due to its exceptional productivity, uniformity, and cost of the sputtering process in the display industry. There are other studies that fabricate the oxide TFTs on polymer substrates at room temperature, but these TFTs have been exposed to at least 150 °C of heat treatment during additional processes such as passivation[56-58].

In this study, we focused on the effect of deposition temperature for ZTO channel layers during RF magnetron sputtering. Some researches indicate that the exposure to heat during sputtering improves the bonding in thin films more effectively [59-61]. However, except for transistor characteristics, there are no analyses focused on material. Thus, we conducted material analysis that can show us the effect of heating during deposition in the sputter chamber (hereafter called *in-situ* annealing). We heated the substrate up to 200 °C for similar annealing effect during the sputtering process forming channel layer.

Such *in-situ* annealing process is also advantageous in terms of the process time. To check its feasibility, we further fabricated TFTs on a PEN substrate using the *in-situ* annealing process and demonstrated reliable TFT operation.

Table 4.1.1 Basic properties of commonly used flexible transparent substrates [62]

Property	PI	PEN	PET	PDMS
Name	Polyimide	Polyethylene naphthalate	Polyethylene terephthalate	Poly dimethyl siloxane
T_g [ºC]	300	120	80	-120
Upper temperature for processing [ºC]	250 ~ 320	180~220	115~170	200~260
CTE (ppm)	30 ~ 60	18	20~80	>250
Cut-off wavelength λ_C (nm)	500	380	300	200
Chemical resistance	Good	Good	Good	Good
Surface roughness	Good	Moderate	Moderate	Poor
Manufacturing cost	Low	Low	High	Low

4.2 Experimental

ZTO TFT was fabricated by using radio-frequency (13.56 MHz) magnetron sputtering system. The process pressure was 5 mTorr and the atmosphere was composed of Ar and O_2 gas (Ar:O_2 flow rate = 10:0 – 8:2). The TFT has a staggered bottom gate structure, p^+-Si serves as a gate (G), 100 nm-thick SiO_2 formed through thermal oxidation is the gate dielectric, amorphous ZTO layer forms the channel, and amorphous indium tin oxide (ITO) layer acts as source (S)/drain (D) electrode. The thickness of the ZTO channel layer is 15 nm; target used for this channel was zinc tin oxide (ZnO:SnO_2 = 1:1, iTasco) and was sputtered with 100 W of RF power source. The source and drain were sputtered using ITO (10 wt %-In_2O_3 doped SnO_2, iTasco) under 55 W of DC power source and had thicknesses of 70 nm. All patterns for channel, S, and D were defined by shadow masks with channel length and width of 300 and 1000 μm, respectively. For control group with traditional annealing process, all the samples were deposited at room temperature and were annealed in air atmosphere at 150 – 350 °C under atmospheric pressure for 2 h. For experimental group, annealing process was replaced by heating the stage during deposition to 150 or 200 °C, and some of the samples experienced additional low-temperature PDA for 2 h in air atmosphere. To demonstrate the feasibility of *in-situ* annealed ZTO process, we also fabricated TFTs on 125 μm-thick PEN substrates. The gate electrode was made of 70 nm ITO thin film. The gate insulator was made of 180 nm Si_3N_4 thin film, which was deposited by PECVD at 85 °C. The same above mentioned procedure was used for the formation of S/D electrodes. For

negative bias illumination stress (NBIS) analysis, all TFTs were passivated with spin-coated poly (methyl methacrylate) (950PMMA A resists, MicroChem) to prevent the unwanted effect of adsorbed oxygen from air, which can act as a source of charge.

The transfer curves were measured using a semiconductor parameter analyzer (4155 A, HP). The drain voltage (V_D) was 10 V and gate voltage (V_G) was swept from -20 V to + 20 V. From these curves, the parameters like I_{on}/I_{off} ratio, field-effect mobility (μ_{FE}), and subthreshold swing (SS) were extracted. 10 mW m^{-2} light power at the wavelength of 550 and 500 nm was used for NBIS analysis. Electrical stress was applied with $V_G = V_{th}$ (threshold voltage) – 20 V while V_D was set to 10 V, which is similar to the actual operation environment in commercial devices. The density of the thin film was measured by X-ray reflectivity analysis (X'pert pro MPD, PANalytical). The microstructures of the thin films were analyzed by using TEM (2100F, Tecnai), and the samples deposited at aforementioned process conditions were measured at the magnification of 150,000X and 1,000,000X.

4.3 Results & Discussion

4.3.1 Effects of post annealing temperature in traditional thermal annealing process

In general, the oxide semiconductors need PDA in oxygen atmosphere. In this step, different transistor characteristics are exhibited depending on the annealing conditions such as temperature. As shown in Fig.4.3.1 and summarized in Table 4.3.1, the standard TFT shows I_{on}/I_{off} ratio of 10^8, μ_{FE} of

25.6 cm^2 V^{-1} s^{-1}, and S.S of 0.21 V dec.$^{-1}$. Here, the deposition was performed at room temperature with Ar only (10 sccm) and PDA was at 350 °C with Ar:O$_2$ = 8:2. However, as the PDA temperature drops down to 150 °C, the I$_{on}$/I$_{off}$ ratio decreases below 10^5, the μ_{FE} was undetectable and the S.S deteriorates to 5.0 V dec.$^{-1}$, which means that controllability of the gate becomes weaker and the characteristics as a transistor are lost. Similar trends were also obtained for TFTs deposited with Ar:O$_2$ = 9:1 or 8:2.
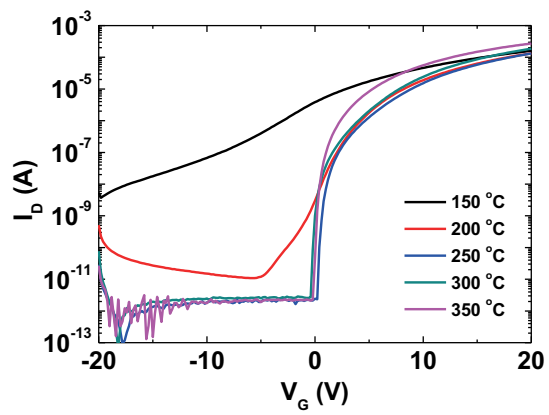
Figure 4.3.1 Transfer curves of TFTs that experienced PDA at different temperatures. Here, Ar:O_2 flow rate during sputtering was 10:0.

Table 4.3.1 Comparison of electrical parameters of TFTs as a function of PDA temperature.

PDA temperature (°C)	V_{th} (V)	I_{on}/I_{off} ratio	μ_{FE} $(cm^2\ V^{-1}\ s^{-1})$	SS $(V\ dec.^{-1})$
150	N/A	10^5	N/A	5.0
200	-3	10^7	16.7	1.6
250	0.2	10^8	18.8	0.4
300	0.2	10^8	22.0	0.3
350	-0.2	10^8	25.6	0.21

4.3.2 Effects of *in*-situ annealing in ZTO-TFTs

In this experiment, channel layers were *in-situ* annealed during sputtering with different Ar:O_2 flow rate at 150 °C (Fig.4.3.2) and 200 °C (Fig.4.3.3). The electrical parameters of the fabricated TFTs are summarized in Table 4.3.2. Fig.4.3.2 (a) shows the transfer curves of the *in-situ* annealed TFTs at 150 °C and Fig.4.3.2 (b) shows the transfer curves for the same TFTs with additional PDA at 150 °C. In both cases, conductive channel layers were formed for TFTs with Ar only and the gate was not able to control the channel. However, as more oxygen is injected during the sputtering process, the TFTs show more stable on/off characteristics. This result clearly indicates that *in-situ* annealing strategy is advantageous for substrates with low thermal stability and that the flow rate is critical for obtaining suitable TFTs properties. The best transistor characteristics were obtained for the *in-situ* annealed TFT with Ar:O_2 = 8:2 and additional PDA (Fig.4.3.2 (b)). The I_{on}/I_{off} ratio, μ_{sat}, and S.S were 10^8, 10.1 cm^2 V^{-1} s^{-1}, and 0.18 V dec.$^{-1}$, respectively. Additional PDA turned out to be favorable to decrease S.S, presumably by improving the interface quality between channel layers and gate dielectrics. Similar behaviors are also observed for the 200 °C case of Fig.4.3.3. Based on the *in-situ* annealing process, we could obtain similar I_{on}/I_{off} ratio with better gate controllability compared to existing high-temperature PDA reference TFTs. Although maximum μ_{FE} of 10.1 cm^2 V^{-1} s^{-1} at 200 °C is about 100 times higher than that of the conventional silicon devices, it requires additional research to improve further through methods such as ultra-low pressure sputtering process.[63]

Surface roughness of the deposited channel layers at 150 °C were investigated by AFM (Table 4.3.3). The root-mean-square roughness (R_q) of the standard 150 °C PDA channel layer was 1.81 nm, whereas smaller R_q of *in-situ* annealed channels was obtained irrespective of the $Ar:O_2$ flow rate: 0.434 and 0.349 nm for $Ar:O_2$ = 10:0 and 8:2, respectively. Additional PDA at 150 °C led to decreased R_q by ~10%. Surface roughness is one of the main reason for surface scattering and therefore affects carrier mobility.

NBIS stability was investigated for 150 °C *in-situ* annealed TFTs with $Ar:O_2$ =8:2. Owing to the NBIS analysis with 550 nm wavelength (Fig.4.3.4 (a)), it was found that the *in-situ* annealed TFT shows V_{th} movement ($\triangle V_{th}$) of -7.2 V. The TFT with additional PDA at the same temperature of 150 °C exhibits better movement of -4.2 V, which is improved by about 40% compared to the one without PDA. The standard TFTs (Ar only) with different PDA temperatures of 200, 250, and 300 °C show the $\triangle V_{th}$ of -5.4 V, -3.8 V, and -2.4 V, respectively. In the case with 500 nm wavelength (Fig.4.3.4 (b)), similar trend is observed. The sample with 150 °C moved -12.8 V and -4.6 V with PDA. The PDA sample moved -6.8 V for 200 °C process, -5.6 V for 250 °C process and -3.8 V for 300 °C process. Based on this observation, comparable NBIS stabilities were obtained for 150 °C *in-situ* annealed TFT with PDA and standard TFT with PDA at 250 °C.

It is widely known that the reliability degeneration of the oxide semiconductors can be explained by three mechanisms: hole-trapping model, oxygen-vacancy model [43], and hydrogen bistability model [42]. In the hole

trapping model, the trap site, which is generated by the broken bond between metal and oxygen, is the main cause of reliability degradation. In oxygen-vacancy model, the instability is caused by insufficient oxygen, which is not compatible with stoichiometry. The hydrogen bistability model has correlation with empty space in the atomic structure of oxide, which is also related to oxygen vacancy and dangling bonds. All three mechanisms are closely related with dangling bonds between atoms. The reason for the improvement in NBIS reliability even when the temperature of the *in-situ* annealed process is lower than that of standard PDA is attributed to the energy that is applied during deposition, which is more effective to form inter-atomic bonds in the thin film than the energy applied at the end of all the deposition processes, as mentioned in the following XRR results.

XRR analysis was conducted to measure the density of the thin film. Theoretical density of ZTO crystal is predicted to be 6.6 g cm^{-3}. In the case of amorphous ZTO thin films, a density reduction of 3 ~ 5% compared to the crystal phase is expected from the simulation results with atomic arrangement without long range ordering [64]. However, this assumes perfect stoichiometry, and the presence of physical defects such as voids during sputtering and presence of chemical defects such as oxygen vacancies must be considered. Therefore, a density loss of 5% or more can be expected. In this study, the density remained similar from 5.5 g cm^{-3} in the as-deposited sample to 5.6 g cm^{-3} in the 200 °C PDA sample (Table 4.3.4). Nonetheless, at 300 and 350 °C, the densities were 5.7 and 5.9 g cm^{-3} respectively, which are increased compared to former three values. This result corresponds with the

aforementioned electrical characteristics results. There was no clear transfer curve up to 200 °C of PDA, and above 300 °C, an exact transfer curve appears. In *in-situ* annealed samples, all the samples had a density similar or higher than 5.7 g cm^{-3}, which is measured for 300 °C PDA sample. The density increased about 2 ~ 6% as the oxygen flow rate increased during deposition.

In PDA results, it is confirmed that the PDA at higher than 300 °C connects the broken interatomic bonds and cures the voids in the thin films. In *in-situ* results, it shows the curing effect occurs from 150 °C. The reason why in-situ annealed ZTO layers have robust structure can be seen from the XRR and TEM results. As the density of the thin film increases, the transistor characteristics are improved. The microstructures in Fig.4.3.5 and 4.3.6 show that in-situ annealing process make nano-ordering in the amorphous ZTO layers which improve the electrical properties by strengthening the interatomic bonds.

Firstly, the effect of PDA after RT deposition shown in Fig.4.3.5 (a) and (b), void size was reduced and denser ZTO layer was formed. Fig.4.3.5 (a) and (c) show that the addition of the oxygen during deposition makes smaller clusters in the thin film and forms a void (white web-shaped area). This void makes an adverse effect on mobility by breaking the conduction path between the clusters. However heat of 150 °C on the substrates reduces the formation of voids induced by oxygen and forms larger ZTO clusters (Fig.4.3.5 (d)). And the amount of void reduced by the PDA at 150 °C after in-situ annealed deposition. (Fig.4.3.5 (e)). This change in microstructure positively affects the formation of denser conduction paths in the thin film.

Fig.4.3.6 shows the microstructures of the clusters. No ordering was observed in (a) and (b) in the samples deposited in Ar-only atmosphere, whereas in (c), (d) which are in-situ annealed in 20% of oxygen atmosphere shows nano-ordering. And PDA makes more nano-ordering in ZTO clusters as shown in Fig.4.3.6 (e)

In-situ annealing also has more positive effect on the film quality, which is shown in Fig.4.3.7. When TEM measurements are conducted, the thin film is damaged by the electron beam. Thus, carbons are deposited on the film making black circular dots. This marks easily occurs in the films with unstable and coarse quality. The ZTO thin films deposited at RT in Ar-only atmosphere with PDA at 300 °C were considerably damage by electron beam and have deposited carbon on its surface as shown in Fig.4.3.7 (a). On the other hand, in-situ annealed samples at 150 °C have only vague circular marks. In sum, in-situ annealing produces more robust film than one deposited in RT and post-annealed at relatively high temperatures, so makes good effects on gate controllability and photo-biased reliability by generating nano crystalline in ZTO clusters. However, mobility decreases as the void increases due to the effect of oxygen during deposition. However, oxygen is known to have a positive effect on reliability as well as on these negative effects aforementioned. The amount of trapped charge which deteriorates the gate controllability decreases as the curing of dangling bonds in the film occurs. However, when oxygen is introduced into the film, the carrier concentration decreases due to the decrease in the oxygen vacancy, such that the conductivity is also lowered. These curing and mobility reductions are in a

trade-off relationship, but it may be improved through further studies to lower the process pressure. Huh et al. reported the advance in electrical and physical properties of oxide TFTs with extremely low process pressure. In that study, more dense film quality was obtained while less oxygen was introduced into the process chamber [63].
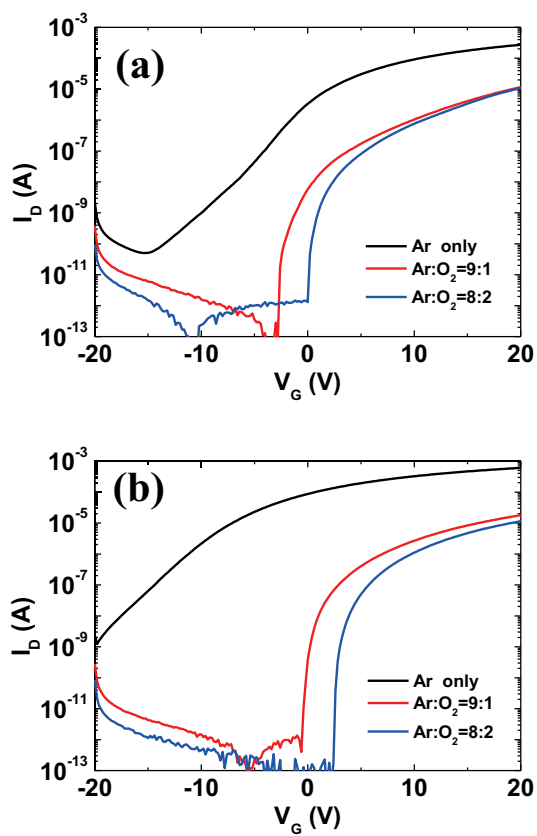
Figure 4.3.2 Transfer curves of (a) 150 °C in-situ annealed ZTO-TFTs with various Ar:O$_2$ ratio and (b) the same TFTs with additional PDA at 150 °C. Here, all PDA was performed at Ar:O$_2$ = 8:2 condition.
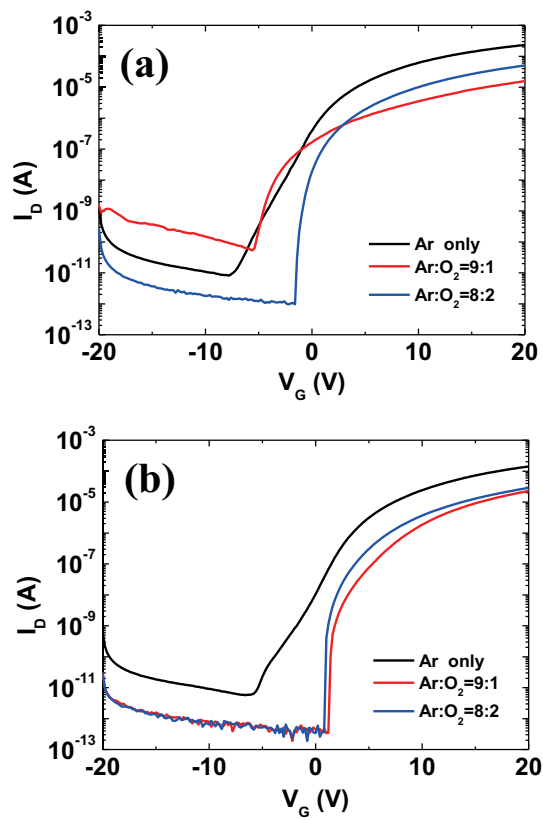
Figure 4.3.3 Transfer curves of (a) 200 °C in-situ annealed ZTO-TFTs and (b) the same sample with additional PDA at 200 °C with Ar:O_2 = 8:2.
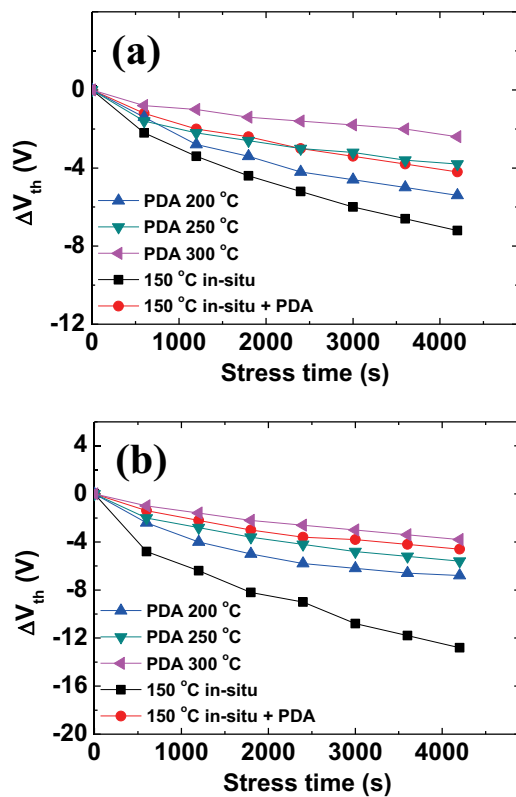
Figure 4.3.4 NBIS results of in-situ annealed TFTs (Ar:O_2 = 8:2) with/without PDA at 150 °C and standard TFTs (Ar:O_2 = 10:0) post-annealed at 200, 250, and 300 °C. Illumination wavelength was (a) 550 nm and (b) 500 nm, respectively.
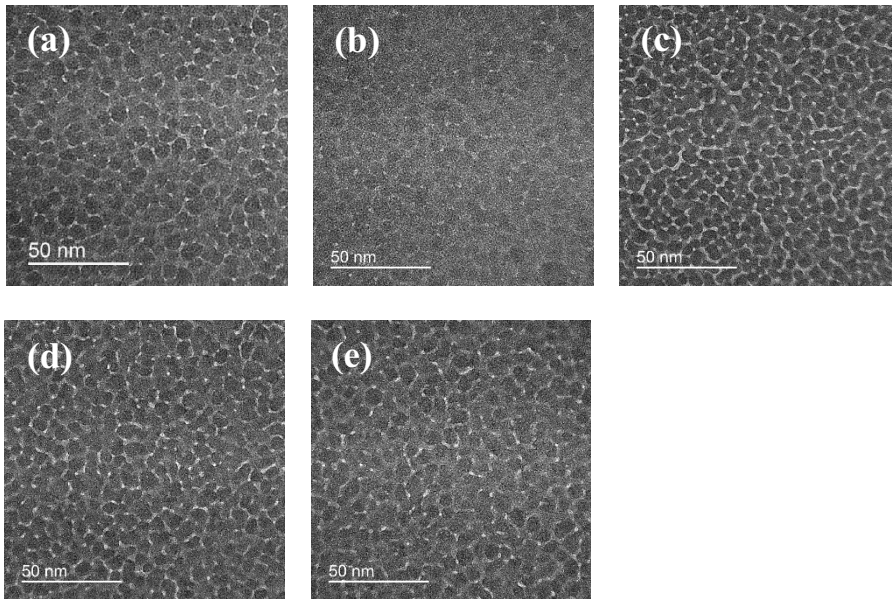
Figure 4.3.5 Microstructure viewed by TEM (magnification X150,000). Sample (a), (b) and (c) were deposited at RT with Ar only atmosphere ((a) and (b)) and Ar:O_2=8:2 (c). PDA was conducted only for (b) at 300 °C for 2 hrs. Sample (d) and (e) were deposited at 150 °C with Ar:O_2=8:2 atmosphere (a) without PDA and (b) with PDA at 150°C for 2hrs.
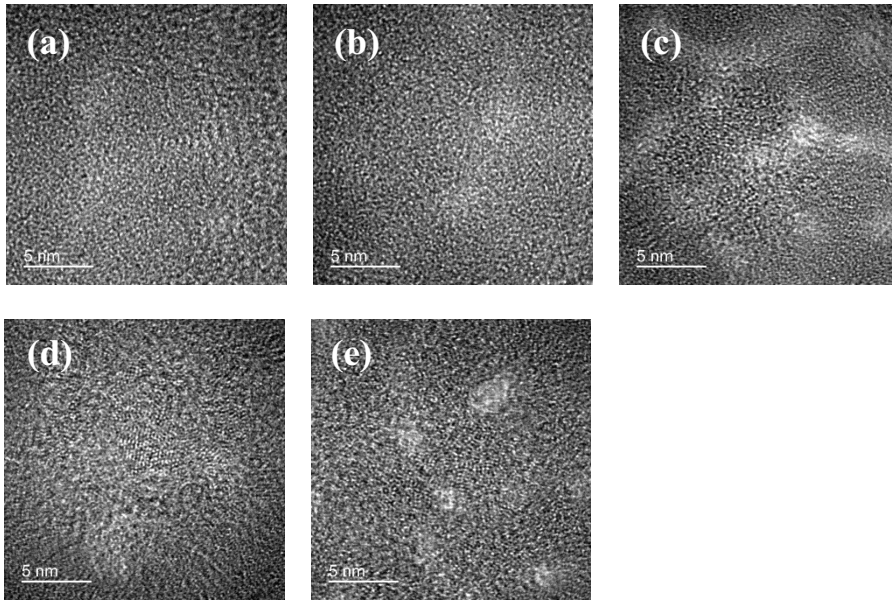
Figure 4.3.6 Microstructure viewed by TEM (magnification X1,000,000). Sample (a), (b) and (c) were deposited at RT with Ar only atmosphere ((a) and (b)) and Ar:O_2=8:2 (c). PDA was conducted only for (b) at 300 °C for 2 hrs. Sample (d) and (e) were deposited at 150 °C with Ar:O_2=8:2 atmosphere (a) without PDA and (b) with PDA at 150°C for 2hrs.
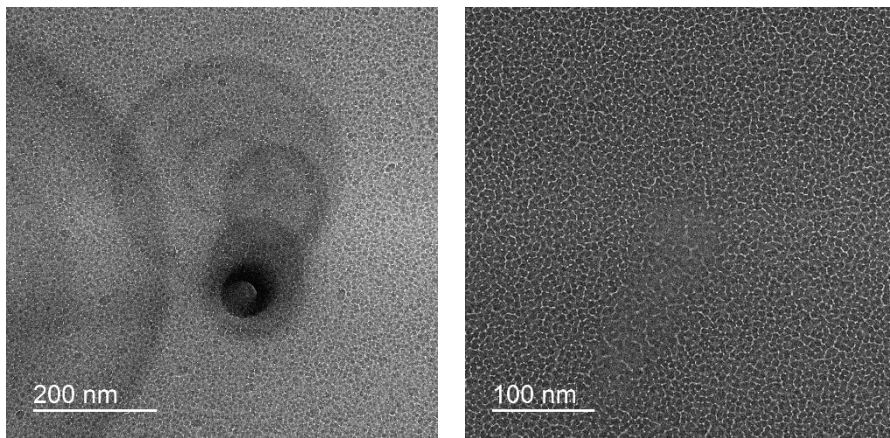
Figure 4.3.7 Marks of damage by the electron beam from TEM. (a) A sample deposited at RT with Ar only atmosphere and post-annealed at 300 °C for 2 hrs.(b) A sample deposited at 150 °C with Ar:O_2=8:2 atmosphere without PDA.

Table 4.3.2 Electrical parameters of TFTs made by in-situ annealing with/without PDA, and conventional PDA process.

Temperature (°C)	condition	Ar:O_2	I_{on}/I_{off} ratio	μ_{FE} (cm^2 V^{-1} s^{-1})	SS (V dec.$^{-1}$)
150	PDA (reference)	10:0	10^5	N/A	5.0
	In-situ	10:0	10^6	27.1	N/A
		8:2	10^8	9.6	0.3
	In-situ + PDA	10:0	10^6	26.8	N/A
		8:2	10^8	9.1	0.18
200	PDA (reference)	10:0	10^7	16.7	1.7
	In-situ	10:0	10^7	21.5	1.61
		8:2	10^8	12.2	0.5
	In-situ + PDA	10:0	10^7	17.5	1.96
		8:2	10^8	10.1	0.15
350	PDA (reference)	10:0	10^8	25.6	0.21

Table 4.3.3 Root mean square roughness values of post annealed, in-situ annealed, and PDA after in-situ annealing samples.
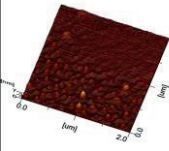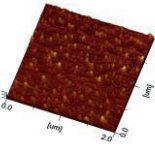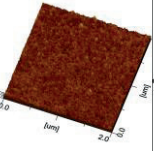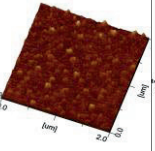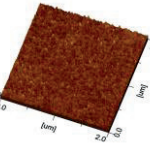
150 °C process				
Condit ion	PDA	*in-situ* annealed		*in-situ* + PDA	
		Ar:O$_2$=10:0	Ar:O$_2$=8:2	Ar:O$_2$=10:0	Ar:O$_2$=8:2
AFM image					
R$_q$ (nm)	1.81	0.434	0.349	0.393	0.329

Table 4.3.4 Density of films of post annealed, in-situ annealed, and PDA after in-situ annealing samples

Process	Process temperature (°C)	Ar:O$_2$	Density (g cm^{-3})
Post annealed (Conventional)	As-dep.	10:0	5.5
	150 °C		5.6
	200 °C		5.6
	350 °C		5.9
in-situ annealed	150 °C	8:2	6.0
in-situ + PDA		8:2	5.9
in-situ annealed	200 °C	8:2	5.9
in-situ + PDA		8:2	5.9

4.3.3 Fabrication of transparent flexible TFTs on PEN substrates

The viability of *in-situ* annealing process was finally demonstrated by fabricating flexible TFTs on PEN substrates using the 150 °C process. Fig.4.3.8 shows the transfer curve of the transparent flexible ZTO-TFTs fabricated on a PEN substrate. Because PEN have a hard coating on one side, the ZTO TFTs on hard coating is named as PEN w/ HC. Transfer curve of PEN w/o HC is the electrical properties of ZTO TFTs on PEN without hard coating

The inset picture shows the actual fabricated device. The deposition temperature was set to 150 °C considering the thermal stability of PEN substrates, and PDA for 2 hrs at the same temperature was also conducted. Here, Ar:O_2 flow rate was set to 8:2. It was confirmed that a TFT having a V_{th} of 0.6 V, an I_{on}/I_{off} ratio of 10^8, μ_{FE} of 1.7 cm^2 V^{-1} s^{-1}, and S.S of 0.39 V dec.$^{-1}$ was fabricated. Compared to standard results based on Si substrates, μ_{FE} reduces from 9.1 to 1.7 cm^2 V^{-1} s^{-1} and S.S also increases from 0.18 to 0.39 V dec.$^{-1}$. The transmittance of the ZTO TFTs on PEN substrates is shown in the Fig.4.3.9. Although the overall performance of the fabricated TFT is somewhat deteriorated compared to that of the standard one on Si substrates, yet proper operation was achieved. One possible origin of the observed deterioration could be the roughness of the substrates. Surface roughness is a main factor in causing surface scattering and has a great influence on electron mobility. The roughness (R_a) of the PEN substrate is 5.0 nm, which is significantly higher than that of silicon below 1.0 nm. Thus, this surface

roughness can also affect the roughness of the thin film being deposited on top. In addition, different mechanical properties of the substrates makes this roughness effect worse. Calculated compressive strain applied to oxide thin films due to the shrinkage of PEN substrates and mismatch of thermal expansion coefficients is roughly estimated to be ~0.3 %, while no or minimal strain (less than 0.01 %) is added in the case of Si substrates. Such compressive strain could induce surface roughening of the channel layer, which worsens the electron mobility.

Tripathy et al. [65] have fabricated IGZO ($InGaZnO_4$) TFT devices with an I_{on}/I_{off} ratio of 10^8, typical mobility of 11 cm^2 V^{-1} s^{-1}, and S.S of 0.33 V dec.$^{-1}$ using IGZO channel layer and silicon nitride insulating film on a PEN substrate with 180 °C process. However, the channel layer was exposed to unwanted heat during fabrication of etch-stop layer and passivation layer. In addition, many other results published in the low-temperature process were obtained by exposure to higher temperatures than the deposition temperature in additional processes such as passivation etc., but in this experiment the mobility is lower than the aforementioned reference. Nevertheless, it is meaningful that the device is manufactured by strictly limiting the exposure of the device to heat throughout the process.
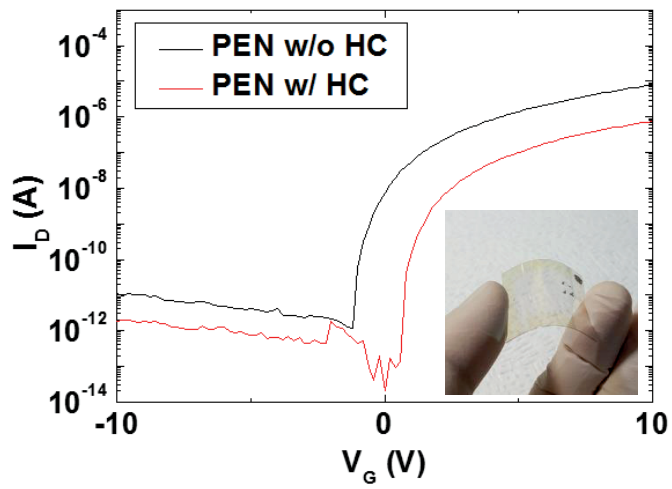
Figure 4.3.8 Transfer curve of the in-situ annealed ZTO-TFTs fabricated on a PEN substrate at 150 °C. Inset picture shows the transparent and flexible ZTO TFT on a PEN substrates.
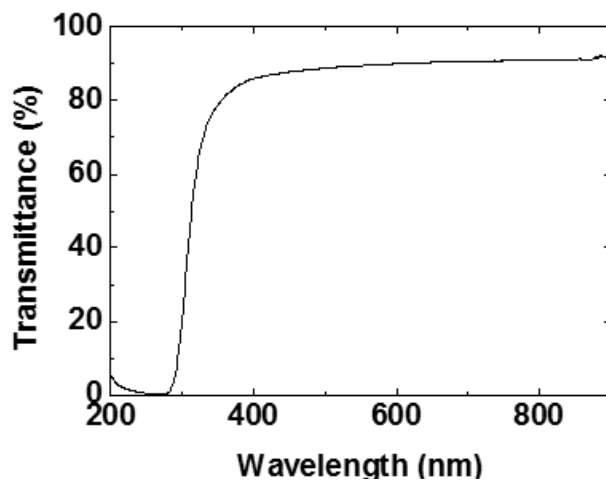
Figure 4.3.9 Transmittance of the ZTO-TFT on a PEN substrates. This result shows the transmittance of the ZTO layer only excluding the bare PEN substrate.

4.4 Conclusions

In this study, the RF magnetron sputtering chamber was heated to fabricate ZTO-TFTs at low temperatures, which enabled the TFTs to be successfully activated even at the lowest 150 °C process, rather than the conventional 350 °C process. The heat applied in the other processes such as the fabrication of dielectric or passivation were strictly controlled to confirm the effect of the *in-situ* annealing on film quality. The main reason for the improvement of the film quality at relatively low temperature can be explained by the densification and ordering effects of thermal energy in the heated sputtering stage. Generally, it is obvious that as-deposited AOS channel needs oxygen curing to connect broken bonds between metal and oxygen atoms. While Ar/O_2 plasma in sputter chamber interacts with relatively low thermal energy (200 °C), curing reaction immediately occurs on as-deposited ZTO clusters on the substrate. The electrical properties are improved by heating the stage which form nano-ordering in the clusters forming the membrane, but the mobility decreases due to the increase of the amount of the void by addition of oxygen during deposition.

Consequently, we fabricated ZTO-TFTs at a temperature below 200 °C, rather than by post annealing over 350 °C. Although the performance should be improved to be applied in the industry, the possibility of building a flexible device using the existing sputtering process is established.

Chapter 5. Reliability analysis of Zinc-tin-oxide thin film transistor under mechanical stress and negative biased illuminated stress condition

5.1 Introduction

Recently, advanced performances of displays cannot appeal no more to customers because the technical level has reached that level where the general person cannot notice the difference between older and new ones. In this situation, many manufacturers are replacing their strategies of developing performances to novel user experiences such as flexibility, foldability and transparency. Many electronics makers are introducing new flexible and transparent products. In this situation, amorphous oxide semiconductors such as amorphous indium-gallium-zinc-oxide (a-IGZO) and zinc-tin-oxide (ZTO) are attracting attention based on their good electrical performances and easy fabrication. They have higher electron mobility (>10cm^2 V^{-1}s^{-1}), lower process temperature (<350 °C) and more superior uniformity than conventional silicon-based devices. Especially, ZTO is attractive material because it does not contain expensive rare-earth elements such as indium or gallium, yet still has high mobility and productivity. Typical oxides are known to have the brittle properties, but they can be suitable for the flexible devices because it can be bent to the strain of several percent as a thin film. Therefore, the display industry has chosen it as the channel material for the TFTs in large-sized and flexible display devices.

Generally, when fabricating a flexible device, the structure is designed to

locate the critical parts in the neutral plane using passivation layer and packaging materials, as shown in Fig.5.1.1. In this structure, the passivation layer blocks the external moisture and gases, and at the same time it translocates the neutral plane of the devices to the TFT layers, thereby reducing the influence of the stress applied to the TFTs. Although the effect of stress on the device is reduced with aforementioned methods, it is essential to study the phenomenon and the mechanisms which occur when the mechanical stress is applied to the devices, since the recent devices have multi-layer stacking structures. Up to now, many groups have reported the studies about oxide semiconductors on flexible substrates, but most of them have focused on the possibility of developing the real flexible devices containing oxide channel layers. Although Munzenrieder and Shin reported the effects of mechanical stress on the amorphous oxide, but there was no analysis on the effects of bending from the fundamental point of view. So this study presents a comprehensive result of the relation between mechanical stress and the electrical properties of the amorphous oxide semiconductors.
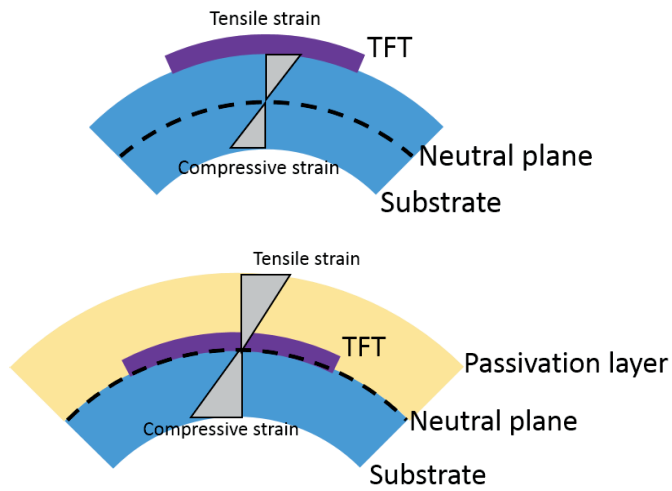
Figure 5.1.1 Mechanical stress applied to the inside of the substrate and TFT while bent (up), and a stress state when passivation layer which put the TFTs on the neutral plane is added (down)

5.2 Experiment

5.2.1 Flexible ZTO TFTs

The flexible TFTs on this study have staggered bottom gate structure on thinned p-Si wafer with thermally oxidized SiO_2 layer as a gate dielectric. 15 nm of ZTO channel layers are deposited on thermally dry oxidized p-Si wafer, and 70 nm of indium tin oxide (ITO) source/drain electrodes are formed on the channel. A RF magnetron sputtering system (SNTEK) was used to deposit 15 nm of ZTO channel and 70nm of ITO source and drain electrode. Targets used for channel was ZTO (SnO_2:ZnO=50:50 mol%, iTasco) and sputtered with 100 W of RF power source. Source and drain was sputtered using ITO (In_2O_3:SnO_2=90:10 wt%, iTasco) with 55 W of DC power source. All patterns for channel, source and drain were defined by shadow masks. Channel has 300 um of channel length and 1mm of width. After fabrication of TFTs, they were annealed at 350 °C for 2 hrs in air atmosphere. And wafer thinning process was conducted after that which provides sufficient flexibility to Si wafers with TFTs. Target thickness was 50 μm and the finished wafer can be bent to a radius of 20 mm.

5.2.2 Negative biased illumination stress (NBIS) conditions for reliability test of ZTO TFTs

Reliability tests were conducted under NBIS (Negative Biased Illumination Stress) condition. NBIS condition is one of the most widely received test condition which simulate the environment of TFTs in display devices. Most of the TFTs used as switching devices in the display are under

negative voltage and are exposed to illumination stress due to back light or emitting layer. So, NBIS simulate the environment that TFTs undergo when they are adopted in real display devices. The experimental conditions are as follows. First, tensile stress was applied parallel to the conduction path by fixing the specimen on a convex/concave jig with a radius of 20 mm as shown in Fig.5.2.1 to simulate bent devices which corresponds to 0.13 % of tensile/compressive strain, and as a control, the samples were placed on a flat surface not to be loaded any external stress. The optical stress conditions applied to the TFTs with three mechanical status are two, wavelengths of 500 and 550 nm. And the intensity of the illumination light is all 0.1 mW m^{-2} which covers entire channel layer. Then, Vth-20 V of gate voltage stress and +10 V of drain voltage stress were applied to the samples which is same as the operating environment of driving TFTs in a display devices. And the changes of transfer curves are measured by sweeping the gate voltage from -20 V to 20 V at every 600 seconds for 3600 s. For the transfer curve measurement, 4155A semiconductor analyzer (HP) and Model-8000 probestation (MSTECH) were used.
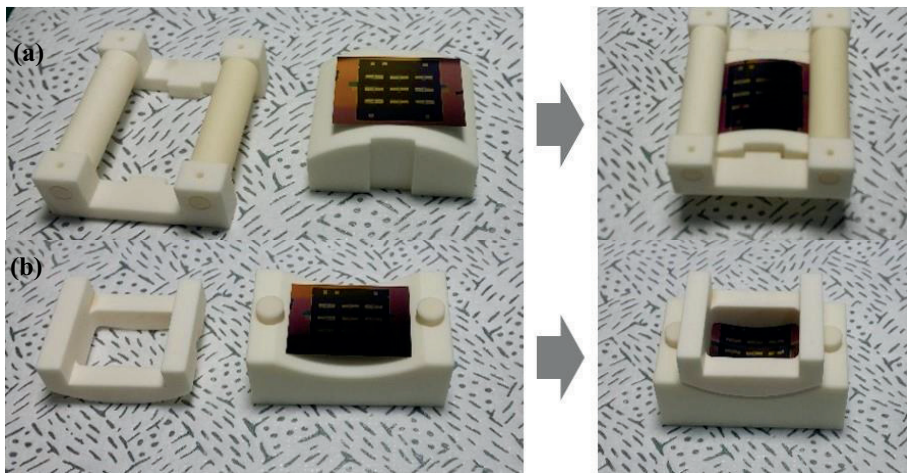
Figure 5.2.1 The jigs used to load mechanical stress to TFTs. (a) Tensile stress and (b) compressive stress parallel to conduction paths are loaded to the channel layer.

5.2.3 Analyzing the band structure of ZTO layer and the effects of the mechanical stress

In this experiment, thermal shrinkage of 125um-thick PEN (Teonex Q65A, DuPont Teijin) polymer substrate was used to apply different stress states to the thin film samples with same chemical compositions. Based on the fact that the maximum heat shrinkage is determined by the heat treatment temperature, Four 20 mm × 20 mm square substrates were thermally shrunk at RT, 150 °C, 175 °C and 200 °C to have 0, 0.2%, 0.4% and 0.6% of shrinkage respectively before deposition of ZTO layer. The ZTO layer was fabricated on these PEN substrates by the process as shown in Fig5.2.2 and annealed after deposition at 200 °C to induce the total thermal shrinkage of 0.6%. Therefore, the ZTO layers on the PEN which have pre-shrunk at RT, 150 °C, 175 °C and 200 °C are compressed equally in plane as 0.6%, 0.4%, 0.2% and 0% respectively . Then, UV-vis spectroscopy (V-770, JASCO) and ultra-violet photoelectron spectroscopy (AXIS-Nova, Kratos) analysis were applied to these samples to obtain bandgap, work function, valence band level and E_F that vary with the amount of compressive stress.
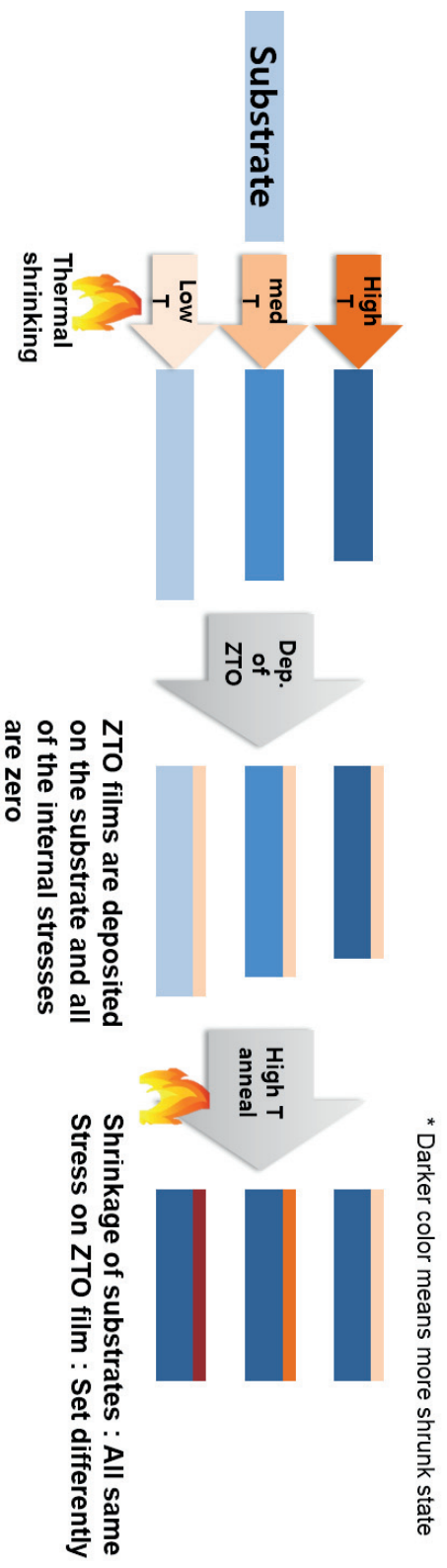
Figure 5.2.2 A method of applying a uniform 2-d biaxial strain to a thin film using heat shrinkage of a polymer substrate. A polymer substrate means that the darker color shrinks further, and a thinner darker color means more compression.

5.3 Results & Discussion

5.3.1 Effects of mechanical stress in electrical properties of ZTO-TFTs

The transfer curve of the ZTO TFT was measured as above-mentioned experimental flow. Fig.5.3.1 shows the threshold voltage shift under NBIS condition of the samples on convexly and concavely bent states with a radius of curvature of 20 mm and flat state. As a result, when light of 450 nm wavelength was illuminated, -4.8 V moved in the flat state while -6.2 V moved in the tensile stressed state which made to deteriorate NBIS reliability, and no change was confirmed when irradiated with a 500 nm wavelength band.

On the contrary, when compressive stress was applied to the sample, the threshold voltage shift of the flat sample was -5.4 V, and the bent sample was -4.0 V when light of 450 nm wavelength was irradiated, representing that the reliability can be enhanced by mechanical stress. The threshold voltage hardly changed with light of 500 nm wavelength too. But it also was found that the reliability was slightly enhanced by -0.68 V for the flat sample and -0.46 V for the bent sample.
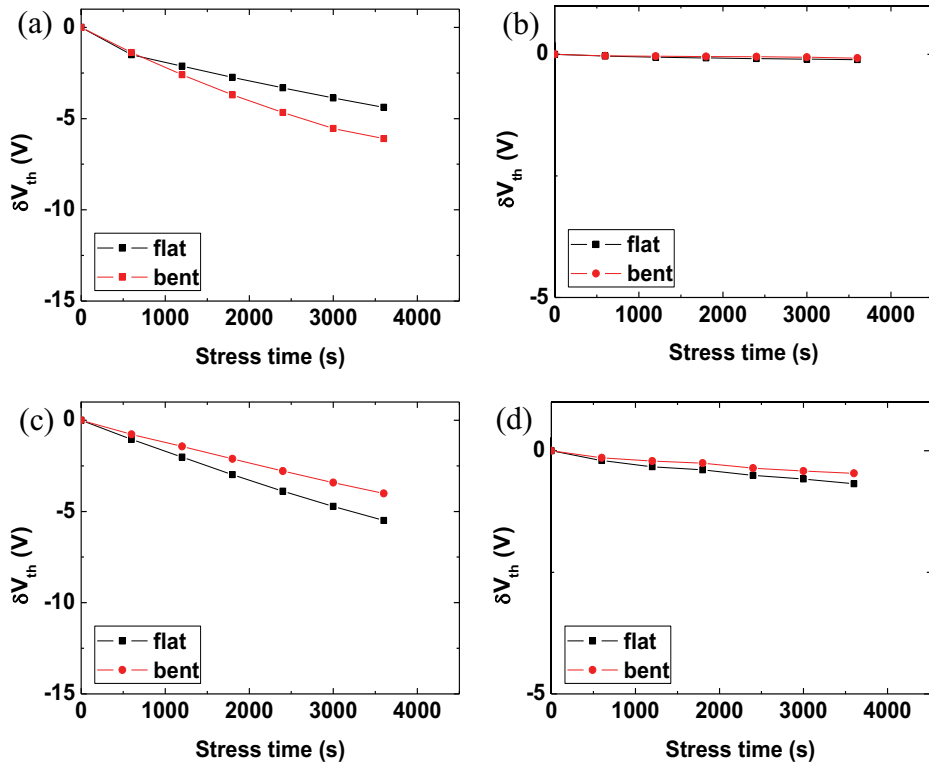
Figure 5.3.1 Threshold voltage shift of ZTO TFTs under tensile stress((a), (b)) and compressive stress((c), (d)) parallel to conduction path with illumination stress of (a), (c) 450 nm, (b), (d) 500 nm of wavelength

5.3.2 Effects of mechanical stress on the ZTO layer

In order to prove the correlation between the mechanical stress and the electrical characteristics of materials, it was necessary to investigate the effect of the stress on the band structure of the material. The relation between the characteristics of the thin film and the stress has been widely reported in the literature. However in these experiments, the method of application of mechanical stress in the thin film was mainly performed by doping an element having a different atomic radius or changing the process condition such as deposition rate, atmosphere and working pressure. However, through this design, the chemical compositions of the thin film are inevitably changed, and it is difficult to accurately analyze the relationship between the mechanical stress and the band structure due to the difference in chemical compositions. The optical bandgap was extracted by extrapolating the linear region near the conduction band using UV-vis spectroscopy. As a result, an optical bandgap of 3.18 eV was measured in the flat state, and the value increases from 3.18 to 3.27 eV with increasing compressive strain from 0 % to 0.6%. This is because the band splits occur differently while the distance between the 4s and 5s orbital of the metal forming the conduction band and the 2p orbital of oxygen forming the valence band are changed. Tauc plots and values are shown in the Fig.5.3.2. And UPS analysis in Fig.5.3.3 show the changes of work function and the energy difference between valence band maximum (VBM) and E_F. Work function of the sample with 0% compression was 3.69 eV and it gradually decreases to 3.42 eV with 0.6% compression. And $(E_F - E_V)$ move from 1.88 eV to 1.57 eV when compression increases from 0 % to

0.6 %. The band structure of the ZTO thin film changed according to the stress state was obtained by combining these results. The results are summarized in Fig.5.3.4 and Table 5.3.1. These changes are thought to be caused by an increase in the split of the energy levels of each atoms due to the increase in orbital overlap by compressive stress. In the previous experimental results, photo-reliability of the ZTO TFT is improved when compression is applied. This phenomenon is related to the oxygen vacancy model and the hole trapping model of the reliability degradation mechanism of the oxide semiconductors in Fig.5.3.5. In this figure, the schematic diagram of the relation between bandgap and mechanical stress is shown. Under compression, as the bandgap increases, gap between the oxygen vacancy at the deep level near the valence band and the conduction band also increases. So, to excite the electrons out of the oxygen vacancies, photons of higher energy are needed. Then, relatively less charged oxygen vacancies (V_O^{2+}, V_O^+) are generated within the forbidden band, resulting in less charge trapping. In recent years, there has been a report that interstitial hydrogen atoms exist at deep level of the forbidden band and causes charge trapping by reacting with the photon from outside, so it can be explained by the same mechanism. And explanation based on the hole trapping model can be suggested since the VBM level moves. As shown in Fig.5.3.6, The ZTO with compression has a higher VBM level. Therefore, the barrier height when the hole moves to the insulator through the gate insulator interface becomes higher. Hole injection from ZTO to the insulator is suppressed by the compression, and the amount of trapped charge is reduced.
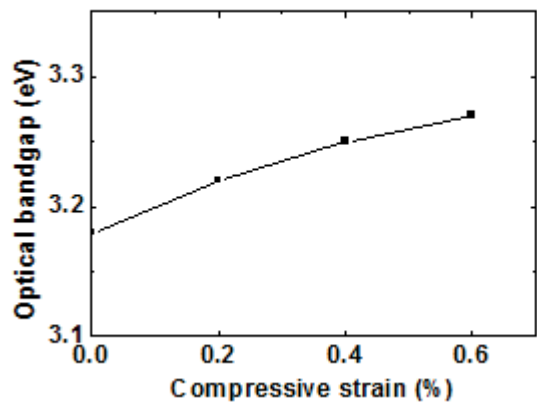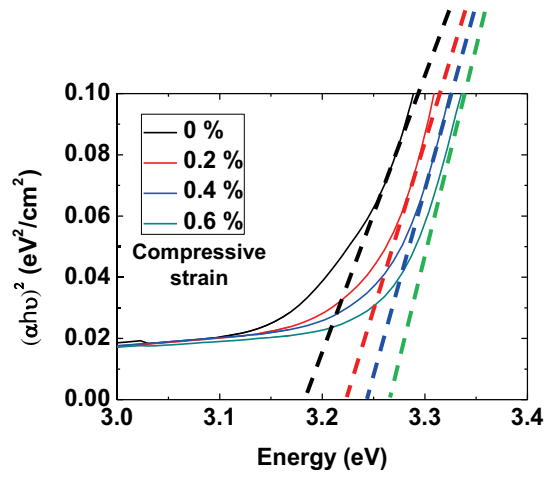
Figure 5.3.2 Optical bandgap measurement by UV-vis spectroscopy. (a) Tauc plot and (b) extracted optical bandgap.
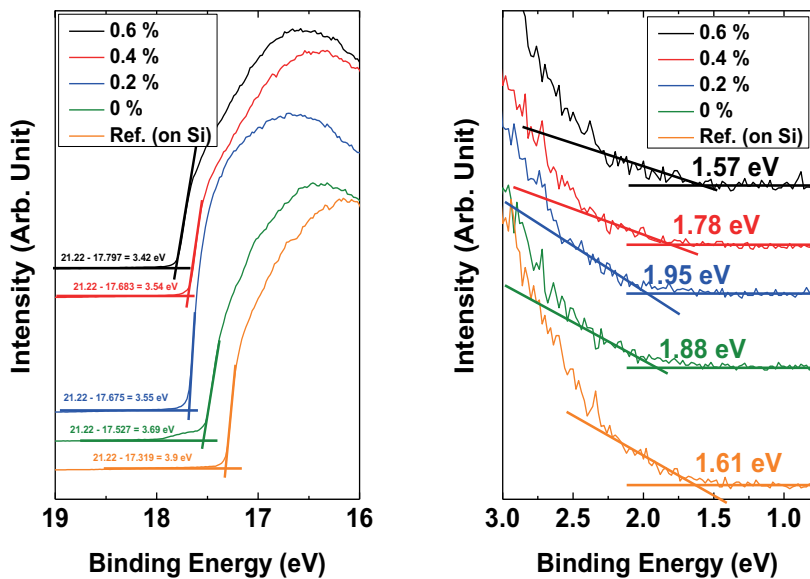
Figure 5.3.3 UPS data of valence band of ZTO film with different compressive states. The values at x-intercept mean VBM energy and cutoff energy which is confirmed by vacuum level.
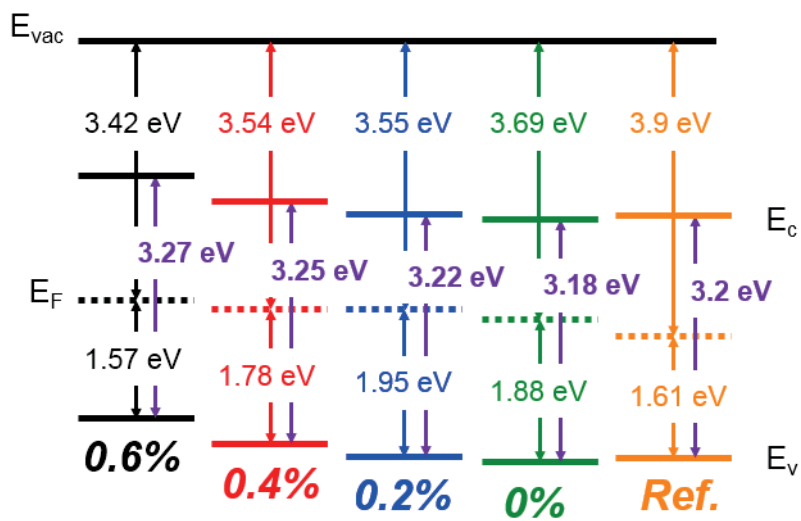
Figure 5.3.4 Relation between compressive strain and band structure.
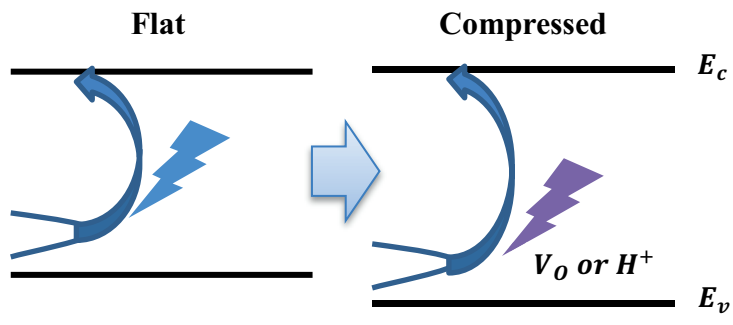
Figure 5.3.5 Schematic diagram of the relation between bandgap and mechanical stress.
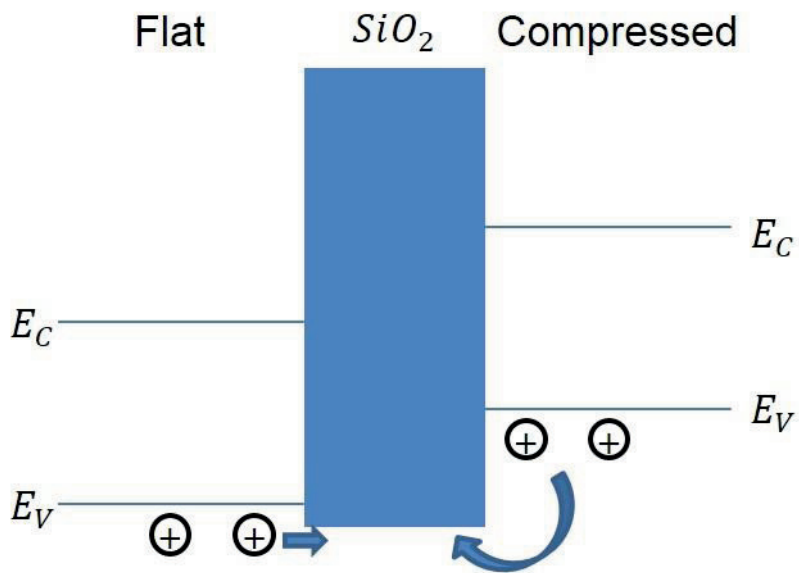
Figure 5.3.6 Schematic diagram of the comparison of hole trapping barrier between flat and compressed state.

Table 5.3.1 Energy values related to the band structure

Compression	Bandgap	Work function	VBM
0.6 %	3.27	3.42	1.57
0.4 %	3.25	3.54	1.78
0.2 %	3.22	3.55	1.95
0 %	3.18	3.69	1.88
Reference (on Si)	N/A	3.9	1.61

5.4. Conclusions

ZTO flexible TFT devices were fabricated by grinding the backside of silicon substrates, and the change in photo-reliability by NBIS condition and bending state was confirmed. The photo-reliability of ZTO TFTs tends to deteriorate under the tension, and enhanced under the compression parallel to conduction path. To analyze the correlation between band structure and mechanical strain, a method to differentiate mechanical stress independently without changing the chemical composition of the thin film or deposition condition was suggested. While the mechanical compressions are applied to the ZTO layer from 0 to 0.6%, bandgap, $(E_{vac} - E_F)$ and $(E_F - E_V)$ tend to move from 3.18 eV to 3.27 eV, from 3.69 eV to 3.42 eV and from 1.88 eV to 1.57 eV, respectively. This trends lead to the enhancement of photo-reliability by suppressing the excitation of electrons from the oxygen vacancies in deep level and inducing elevation of barrier height that the holes in the ZTO encounter when they jump to the valence band of the insulator. In this study, it is confirmed how uniform stress affect to the band structure of ZTO thin film layer, and further suggests a method to design the experiment by isolating only mechanical stress not accompanied by change in chemical composition as conducted in conventional works.

Chapter 6. Conclusions

Two experiments have been carried out for the application of oxide semiconductors as devices for next-generation flexible displays. The first subject was an attempt to lower the process temperature while using the conventional sputtering process, and the second was an experiment about the relation between photo-induced instability and mechanical stress on the ZTO channel layer.

In chapter 4, it was possible to fabricate a ZTO TFT device that performs electrical characteristics with electron mobilities of 9.1 cm^2 V^{-1} s^{-1}, I_{on}/I_{off} of 10^8, and subthreshold swing of 0.15 V dec^{-1}, under the process temperature of 150 °C by heating up the substrates during deposition of ZTO layer. And using this method, it was possible to fabricate the ZTO devices on the PEN substrate which can be processed up to 180 ℃. The electrical properties of ZTO TFTs on PEN substrates were electron mobilities of 9.7 cm^2 V^{-1} s^{-1}, I_{on}/I_{off} of 10^8, and subthreshold swing of 0.28 V dec^{-1}. Therefore, the possibility of fabricating ZTO TFTs on flexible polymer substrates using the existing sputtering system is proposed without additional equipment.

In chapter 5, the mechanisms of degradation and enhancement of the photo-induced reliability of ZTO TFTs were analyzed by correlating the mechanical stress state and band structure of ZTO layer. It is confirmed that tensile stress tended to deteriorate the reliability of the ZTO TFT devices. On the contrary, when the compressive stress was applied to the devices, the threshold voltage shift was suppressed in the NBIS condition. There are two

methods to apply a stress state to a thin film, doping of elements having different atomic radius and adopting different process conditions. But these cannot accurately analyzed due to the change in the chemical composition. And then, in this dissertation, it is suggested a method that differentiate the mechanical stress states on the equally deposited ZTO layers using thermal shrinkage of PEN polymer substrates. As a result, when the compressive stress was applied up to 0.6 %, the bandgap increased from 3.18eV to 3.27eV by 0.09 eV and the VBM level increased from 4.24 eV to 4.81 eV based on the VBM of SiO_2 gate oxide layer. It is found that the energy differences between conduction band minimum and E_F decrease with more compression. This phenomenon is associated with the oxygen vacancy model and the hole trapping model, which are the mechanism of photo instability in oxide semiconductors. An increase in the bandgap induce the reduction of formation of charged oxygen vacancies (V_0^{2+}) when the electrons from the oxygen vacancy excite to the conduction band due to the increased band gap. And the increased VBM level makes the higher energy barrier to jump when the holes in the ZTO jump to the insulator interface, therefore this causes the photo-reliability enhancement.

From these results, it is proposed the possibility of fabricating a transparent flexible substrate by applying a polymer substrate while using the conventional sputtering process. And the effect of mechanical stress on the instability of oxide was confirmed, and a reliability enhancement mechanism using stress was proposed. And it is suggested that this phenomenon may be used as a method to enhance the photo-bias stability by using the mechanical

stress.

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Curriculum Vitae

Sungmin Kim

Department of Materials Science and Engineering

College of Engineering, Seoul National University

Gwanak-ro 1 , Gwanak-gu, Seoul, 08826, Korea

Tel: +82-10-2976-8984

E-mail: ksm0830kr@snu.ac.kr

EDUCATION

M.S. & Ph. D. integrated course, Department of Materials Science and
Engineering
Seoul National University, Seoul, Korea
2013. 3 – 2018. 2

B.S., Department of Materials Science and Engineering
Seoul National University, Seoul, Korea
2009. 3 – 2013. 2

RESEARCH AREAS

- Transparent Thin film Transistor for display application

    - Fabrication and electrical characterization of TFTs based on oxide semiconductor and transparent electrode for large scale and high resolution display.

    - Research for the improvement in reliability of TFTs

TECHNICAL SKILLS

1. Deposition methods

    - **RF and DC magnetron sputtering** for carious oxide and metal films

    deposition.

    - **E-beam evaporation** for metal electrodes

2. Device fabrication methods

    - **TFT structures** by using shadow mask via sputtering method

    - Fabrication of **transparent and flexible oxide TFTs** on glass and

    polymer substrates

3. Analysis methods

    - Transfer characterization and reliability evaluation of TFTs

    - **Ellipsometry** for film thickness and refractive index measurement

    - Hall measurement and 4 point probe for measuring sheet resistance of

    thin films

- **Transmission electron microscopy** (TEM)

- **Atomic Force Microscopy** (AFM)

- **X-ray diffraction** (XRD), X-ray reflectivity (XRR), X-ray fluorescence (XRF)

- X-ray photoelectron spectroscopy (XPS)

4. Furnace for ambient and vacuum annealing

RESEARCH PROJECTS

"Study on the fracture characteristics using the electrical properties of the encapsulation layer for the application to the flexible OLED", from Samsung Display co., Korea, 02/2013 – 01/2014.

"Research on the electrical properties of the flexible oxide semiconductor using TCO TFT technology", from DHK solution corp., Korea, 11/2013 – 04/2014.

"Research for mechanical properties for multilayer and novel materials for passivation layer", from Samsung Display co., Korea, 02/2016 – 01/2018.

List of publication

1. Journals (SCI)

1.1 International

1. Seungha Oh, Bong Seob Yang, Yoon Jang Kim, Yu Jin Choi, Un Ki Kim, Sang Jin Han, Hong Woo Lee, Hyuk Jin Kim, **Sungmin Kim**, Jae Kyeong Jeong and Hyeong Joon Kim, "Dynamics of negative bias thermal stress-induced threshold voltage shifts in indium zinc oxide transistors: impact of the crystalline structure on the activation", Journal of physics D: applied physics., 47, 2014

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3. Eun Kil Park, **Sungmin Kim**, Jaeyeong Heo, Hyeong Joon Kim, "Electrical evaluation of crack generation in SiNx and SiOxNy thin-film encapsulation layers for OLED displays", Applied surface science 370, 126, 2016

4. Sang Jin Han, **Sungmin Kim**, Joongyu Ahn, Jae Kyeong Jeong, Hoichang Yang and Hyeong Joon Kim, "Composition-dependent structural and electrical properties of p-type SnOx thin films prepared by reactive DC magnetron sputtering: effects of oxygen pressure and heat treatment", The Royal Society of Chemistry, 6, 71757, 2016

5. Min Ho Oh, Eun Kil Park, **Sungmin Kim**, Jaeyeong Heo, and Hyeong Joon Kim, "Long-Term Stability of SiNx Thin-Film Barriers Deposited by

Low Temperature PECVD for OLED",ECS Journal of solid state science and technology, 5(5), R55-R58, 2016

6. **Sungmin Kim**, Ji Min Kim, Jaeyeong Heo, and Hyeong Joon Kim, "Low-temperature fabrication of amorphous zinc-tin-oxide thin film transistors with in-situ annealing process", ECS journal of solid state science and technology, 6 (10), P728-P732, 2017

7. **Sungmin Kim**, Ji Min Kim, Jae Kyeong Jeong, and Hyeong Joon Kim, "Effects of the mechanical stress on the electrical properties of zinc-tin-oxide thin film transistors"

2. Conferences
2.1 International
1. **Sungmin Kim** and Hyeong Joon Kim, "Reliability analysis of zinc tin oxide thin film transistor under mechanical stress and NBIS(Negative Biased Illuminated Stress) condition", Poster session, American Vaccum Society 62nd International Symposium & Exhibition, Oct, 2015

2. **Sungmin Kim** and Hyeong Joon Kim, "Low-temperature fabrication of amorphous zinc tin oxide thin film transistor without annealing process", Oral presentation, Pacific Rim symposium on surfaces, coatings & interfaces, Dec, 2016

2.2 Domestic
1. **Sungmin Kim**, Seungha Oh and Hyeong Joon Kim, "Reliability analysis for bent Zinc tin oxide TFT using Si wafer grinding", 한국 반도체 디스플레이 기술학회 2014년 춘계 학술대회, June. 5, 2014

2. **<u>Sungmin Kim</u>** and Hyeong Joon Kim, "Reliability analysis on ZTO TFT under tensile stress and NBIS(negative biased illuminated stress) condition", 한국세라믹학회 2015년 춘계학술대회 및 총회, April. 15, 2015

3. **<u>Sungmin Kim</u>** and Hyeong Joon Kim, "Fabrication and evaluation of transparent flexible thinfilm transistors with amorphous ZTO(Zinc Tin Oxide)", 한국세라믹학회 2015년 추계학술대회 및 총회, Nov. 4, 2015

4. **<u>Sungmin Kim</u>**, Ji Min Kim, Hong-Jeon Kang and Hyeong Joon Kim, "Correlation between Mechanical Stress and Characteristics of Zinc Tin Oxide Semiconductor", 한국세라믹학회 2016년 춘계학술대회 및 총회, April. 20, 2016

5. **<u>Sungmin Kim</u>**, Hong Jeon Kang, Ji Min Kim, and Hyeong Joon Kim, "비정질 ZTO (Zinc Tin Oxide) TFT의 저온제조공정과 전기적 특성 평가", 제34회 한국진공학회 동계정기학술대회, February 7, 2018

Abstract (in Korean)

최근 디스플레이 산업에서는 유연성이나 투명성 같은 유저경험에 기반한 특성을 가진 기기들이 각광받고 있다. 기존의 실리콘 기반 TFT소자는 유연성과 투명성을 구현해내기 어렵기 때문에 이런 특성을 갖는 새로운 물질의 개발이 필요한 시점인데, InGaZnOx (IGZO)나 ZnSnOx (ZTO) 같은 비정질 산화물 반도체가 빠른 동작속도와 생산성을 바탕으로 주목받고 있다. 그 중에서도 ZTO는 구성원소 중에 값비싼 희토류 금속이 없고, 그럼에도 높은 전하 이동도와 우수한 생산성을 가지면서 차세대 소자의 재료물질로 지목되어왔다.

ZTO는 우수한 전기적 특성 또한 가지고 있지만, 유연성 기기에 활용되기 위해서 해결해야 할 문제점이 남아있다. 유연성 기기를 제작하기 위해서는 필연적으로 폴리머 기판을 사용해야 하는데, 일반적으로 내열성 폴리머인 폴리에틸렌 나프탈레이트 (PEN)이나 폴리아릴레이트 (PAR)와 같은 물질의 내열온도는 200도 이하이다. 이에 반해 기존의 ZTO 제작공정에서는 350도 이상의 열처리를 반드시 거쳐야만 했다. 따라서 저온에서도 산화물 반도체의 특성을 구현할 수 있는 공정의 확보가 필요하다.

또한 ZTO가 유연성 디스플레이 기기에 적용되었을 때 노출되는 외부 스트레스 상황에 의해 발생하는 현상에 대한 이해도 부족한 상황이다. 일반적으로 유연성 디스플레이 기기에 가해지는 스트레스는 휨에 의한 기계적 응력과 광원층에 의한 광 스트레스이다.

본 논문에서는 ZTO 박막 트랜지스터 소자가 투명, 유연성 기기에 활용될 수 있도록 하는 관련 연구가 진행되었다. 첫 번째로 ZTO 박막 트랜지스터 소자 제작공정의 최고온도를 200도 이하로 낮추는 연구가 수행되었다. 기존의 ZTO 소자는 상온에서 증착 된 후 350도 이상의 후열처리 공정을 거치며 원자간 결합이 생성되고 산소 공공에 산소가 결합하는 반응이 일어남으로써 소자 특성이 구현된다. 이런 후열처리 공정 대신에 증착 중에 기판을 200도 수준으로 가열하고 산소를 일부 첨가해줌으로써 증착과 동시에 박막 내 원자들이 상호결합을 생성하고 산소 공공의 발생이 억제되도록 하였다. 그 결과 전계효과 전자 이동도가 5.8 – 27.1 $cm^2\,V^{-1}\,s^{-1}$, on/off 전류비가 10^8, subthreshold swing이 0.15~1.7 V dec^{-1} 수준으로 기존의 350도 공정 대비 200도 낮은 온도에서도 충분한 트랜지스터 특성을 구현할 수 있었다.

X-ray 반사율 측정법을 이용하여 박막 밀도를 측정한 결과, 상온에서 증착 된 박막은 5.5 g cm^{-3}였으며, 이를 200도에서 후열처리한 경우 5.7 g cm^{-3}, 350도에서 한 경우 5.9 g cm^{-3} 로 열처리 온도가 증가할수록 더 조밀한 박막이 형성되었다. 고온증착을 진행한 경우, 150도와 200도 공정 모두 5.9~6.0 g cm^{-3}에 해당하는 밀도 값을 보이며, 고온증착을 통해 낮은 온도에서도 조밀한 박막을 형성할 수 있음을 확인하였다. 또한 원자간력 현미경을 이용한 표면조도 측면에서도 이점이 있었는데, 상온증착 뒤 150도에서 후열처리한 ZTO박막은

1.81nm의 평균제곱근 조도를 가진데 반해, 가열증착 공정을 거친 박막은 0.33~0.43nm 수준으로 4배 이상 개선된 특성을 보였다. 투과 전자 현미경 분석 결과, 고온증착의 효과를 직접적으로 확인할 수 있었다. 상온증착 샘플에서는 열처리를 안 한 샘플은 물론, 350도로 후열처리한 샘플에서도 완전한 비정질상이 관찰된 데에 비해, 고온증착 된 샘플에서는 수 nm크기의 나노 클러스터가 다량 형성되어 있었다. 이러한 결과는 가열된 기판 위에 증착 된 ZTO 클러스터가 열에너지로 인해 충분한 운동에너지를 가지며 운동하여 물리적인 공공을 채우고 결정질을 형성하기 때문에 일어나는 현상으로, 따라서 밀도 증가와 조도 개선이 수반된 것으로 확인되었다.

더불어 이 실험의 최종 목표인 '폴리머 기판 위 ZTO 박막트랜지스터 소자 제작' 까지 수행되었다. 그 결과 125um두께의 PEN기판 위에 투명하고 유연성을 갖는 ZTO 박막 트랜지스터 소자가 성공적으로 제작되었으며, 소자의 전자 이동도는 9.1 cm^2 V^{-1} s^{-1}, on/off 전류비는 10^8, subthreshold swing은 0.28 V dec^{-1} 로 충분히 실제 기기에 적용할 만큼 우수한 특성이 나타났다.

그리고 두 번째로, 외부 자극이 유연성을 갖는 ZTO 박막 트랜지스터에 미치는 영향에 대한 연구를 수행하였다. 앞서 언급했듯이 ZTO 박막트랜지스터 소자는 투명성과 유연성을 바탕으로 유연성 디스플레이 소자의 재료물질로 지명되어 왔다. 이 소자가 유연성 디스플레이에 적용되었을 때에는 광원으로부터 발생하는 빛과 휨으로

인해 발생하는 기계적 응력에 노출된다. 따라서 이러한 자극이 주어진 상황에서 소자의 신뢰성을 분석하는 것은 매우 중요하다. 이에 본 논문에서는 소자를 20mm의 곡률반경을 갖는 볼록한 지그와 오목한 지그 위에 고정시킴으로써 기계적 응력은 가해준 후, 450에서 500nm의 파장을 갖는 빛을 조사시켜 소자가 실제 기기에서 받는 환경을 구현하였다. 그 결과, 볼록한 지그 위에서 빛이 조사되었을 때 트랜지스터 소자의 역치 전위가 낮아지는 방향으로 이동하는 현상을 확인하였고, 따라서 인장응력이 ZTO 박막트랜지스터 소자의 신뢰성을 열화시키는 것을 알 수 있었다. 반면에 소자를 오목한 지그 위에 고정시켜 압축 응력을 가해준 상태에서는 응력상태에서 역치 전위 이동이 더 적게 일어나는 현상을 보였다.

이 현상을 해석하기 위해 투명한 PEN 기판 위에 동일하게 증착된 ZTO 박막에 서로 다른 응력을 인가하는 방법에 대해 고찰하였으며, 이를 통해 화학적 조성 변화 없이 응력만을 독립적으로 차등화하는 방법을 제시하였다. UV-vis 분광계를 이용한 광학 밴드갭 측정과 자와선 광전자 분광계를 이용한 가전자대, 일함수 준위 분석이 진행되었다. 그 결과 0.6 %까지 인장응력을 가했을 시 밴드갭과 최대 가전자대 준위가 증가하는 경향을 보였다. 이러한 현상과 산화물 반도체의 신뢰성 열화 메커니즘인 산소 공공 모델, 홀 트래핑(hole trapping) 모델을 연관 지어 기계적 응력이 신뢰성의 강화와 열화에 영향을 미칠 수 있음을 설명하였고, 따라서 외부에서 상황에 맞는

압축 응력을 인가함으로써 소자의 신뢰성 강화 기구로 사용할 수
있는 가능성을 제시하였다.