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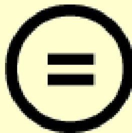
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공학박사학위논문

Noble Methods for Improvement of Electrical Performance of Metal Induced Lateral Crystallized Thin Film Transistor

금속유도 측면결정화 박막 트랜지스터의 전기적 성능 향상을 위한 고귀한 방법

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Noble Methods for Improvement of Electrical Performance of Metal Induced Lateral Crystallized Thin Film Transistor

Hyung Yoon Kim

Under supervision of Prof. Seung Ki Joo

A dissertation submitted to the Faculty of Seoul National University in partial fulfillment of the requirements for the degree of Doctor of Philosophy

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School of Materials Science and Engineering

Graduate School

Seoul National University

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Abstract

Noble Methods for Improvement of Electrical Performance of Metal Induced Lateral Crystallized Thin Film Transistor

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Low-temperature polycrystalline-silicon (poly-Si) thin-film transistors (TFTs) fabricated via metal-induced crystallization (MIC) are attractive candidates for use in active-matrix flat-panel displays. However, these exhibit a large leakage current due to the nickel silicide being trapped at the grain boundaries of the poly-Si. We

reduced the leakage current of the MIC poly-Si TFTs by developing a gettering method to remove the Ni impurities using a Si getter layer and natively-formed SiO_2 as the etch stop interlayer. The Ni trap state density (N_t) in the MIC poly-Si film decreased after the nickel silicide gettering, and as a result, the leakage current of the MIC poly-Si TFTs decreased. Furthermore, the leakage current of MIC poly-Si TFTs gradually decreased with additional gettering. To explain the gettering effect on MIC poly-Si TFTs, we suggest an appropriate model. Gettering method was also applied to nickel silicide seed induced lateral crystallized (SILC) poly-Si TFTs. Although the nickel silicide was already reduced by SILC, the nickel silicide in the SILC poly-Si film could be further reduced through gettering. As a result, the leakage current of the SILC poly-Si TFTs decreased.

Poly-Si TFT fabricated by metal-induced lateral crystallization (MILC) is an attractive candidate for switching and driving elements in large-scaled active-matrix flat-panel displays. However, the MILC poly-Si TFTs have a large leakage current. The leakage current of MILC poly-Si TFTs is induced by charged trap state which is originated from Ni impurities at the interface between gate insulator and poly-Si active layer, and the trap state is activated by high electric field between the gate and the drain. In this study, we developed a double exposure method to form drain offset region. The leakage current of MILC poly-Si TFTs fabricated by double exposure method drastically decreased.

In this study, based on the effect of boron on MILC growth rate, we investigated the effects of boron on the crystallization of amorphous silicon (a-Si).

Low pressure chemical vapor deposition (LPCVD) a-Si and plasma enhanced chemical vapor deposition (PECVD) a-Si showed different tendencies in crystallization by boron. When LPCVD intrinsic a-Si was doped with boron, a-Si was crystallized without Ni at 560 °C within 2 h, whereas boron-doped PECVD a-Si was not crystallized without Ni. However, the MILC growth rate of boron-doped PECVD a-Si significantly increased. The MILC growth was suppressed when annealed in hydrogen ambient, and the sheet resistance of boron-induced crystallized Si annealed in hydrogen ambient was higher than that annealed in vacuum. To elucidate these phenomena, we suggested an appropriate model of boron-induced silicon crystallization.

MILC poly-Si TFTs were fabricated on the compacted glass and the bare glass substrate, and we investigated compressive stress effects on MILC growth rate and electrical properties of MILC poly-Si TFTs. We compacted the glass at 550 °C for 40 h to suppress glass substrate shrinkage. The strain rate of the bare glass substrate was 0.0067% and that of the compacted glass substrate was 0.0012% after crystallization and electrical activation. The MILC growth rate on the bare glass substrate was lower than that on the compacted glass substrate. Compressive strain resulting from glass substrate shrinkage generally increases the size of the micro-cracks and vacancies in Si film, and as a result, field effect mobility, threshold voltage and subthreshold slope of the MILC poly-Si TFTs fabricated on the bare glass substrate deteriorated. The uniformity of electrical properties of MILC poly-Si TFTs was degraded on the bare glass substrate. On the other hand,

the MILC poly-Si TFTs fabricated on the compacted glass substrate showed excellent uniformity of electrical properties.

Keywords: Metal induced crystallization, thin-film transistors, gettering, leakage current, metal induced lateral crystallization, nickel silicide seed induced lateral crystallization, double exposure method, drain offset, boron-induced silicon crystallization, sheet resistance, hydrogen annealing, compressive stress, bare glass substrate, compacted glass substrate.

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Chapter 1

Introduction

1.1 Thin-Film Transistors

In the last two decade, a lot of research has been done on thin-film transistors (TFTs), and TFTs have become a key field of the flat panel display industry. TFT is a type of field effect transistor made by depositing thin films of an active semiconductor layer, the dielectric layer and metallic contacts on supporting substrate. It is basically a three-terminal device and is mainly applied to a liquid crystal display (LCD). In 1949, thin film transistor using CdSe as semiconductor active layer was announced. In 1973, an example of driving a LCD was disclosed. Amorphous silicon (a-Si) and polycrystalline silicon (poly-Si) film are used as active layers of semiconductors. a-Si film was developed in 1979 at the University of Dundee, UK. Since then, a-Si film has been actively researched and developed for LCDs mainly in Japan. a-Si and poly-Si have been widely applied to color TFT-LCD. In addition, studies on transparent TFTs and TFTs using organic or inorganic materials have been actively conducted.

1.2 Flat Panel Displays

1.2.1 Liquid Crystal Display

The LCD is one of the display devices. The LCD is optically passive and consumes little power because it does not emit itself. Therefore, portable calculators that mainly use LCDs without backlight have a long life with only small solar panels or low-capacity batteries. Since the LCD does not emit light by itself, a back light is placed on the back side and a liquid crystal is placed on the front side to emit light in such a way that the liquid crystal blocks or passes the light according to the electric signal [1.1-1.4]. Liquid crystals are substances that have both solid and liquid properties. In normal times, liquid crystals are irregularly arranged to twist the direction of light passing through the polarizing plate to pass through the vertically erected polarizing plate. However, when the current flows, the arrangement of the liquid crystal changes regularly, so that the light is filtered by the secondary polarizing plate. One pixel is made of a liquid crystal in which two transparent electrodes are connected [1.5], and there are polarization filters perpendicular to each other on both sides. Normally, irregular arrangement of the liquid crystal changes the direction of light oscillation so that light that is once filtered through the polarizer can pass through the next polarizer. However, when the voltage is applied, the arrangement of the liquid crystal is fixed in one pattern, and the light that has once passed through the polarizer is blocked by the second polarizer, which is vertically aligned with the first polarizer. An LCD with this

feature uses a backlight and adjusts the brightness of the screen by adjusting the degree of polarization of the liquid crystal. Unlike cathode ray tube, LCD displays have the advantage of being thinner and sharper than previous displays, thanks to the space-saving architecture. As the LCD display using liquid crystal is commercialized, the size of the display becomes smaller and smaller, so that various visual information can be transmitted to a small electronic device such as a mobile phone.

1.2.2 Active Matrix Organic Light Emitting Diode

An active matrix organic light emitting diode (AMOLED) is promising display technology used in smart electronic devices such as mobile phones, laptops and televisions. The AMOLED is a kind of organic light-emitting diode (OLED), and the principle of light emission of OLED is similar to that of light emitting diode. When electrons and holes that are far apart receive electrical energy from the outside, electrons and holes are recombined and light energy is emitted. The amount of the energy is determined by the band gap between electrons and holes. In case of AMOLED, since TFT is built in each light emitting element, it is possible to emit light individually. As a result, power consumption is relatively low and more sophisticated screens can be achieved [1.6]. AMOLED has the following additional advantages: (i) since self-emission is possible, an auxiliary light source such as back light unit is not necessary and the thickness can be reduced. (ii) Transparent display and flexible display are possible. (iii) High contrast ratio, high brightness/luminance, excellent color gamut and wide viewing angle [1.7]. The AMOLED panel consists of a TFT substrate, an organic material layer and a polarizer. The organic layer is composed of a functional organic layer such as a hole injection layer, a hole transfer layer, an emission material layer, an electron transfer layer and an electron injection layer. Unlike an LCD using voltage driving, AMOLED is current drive device [1.8] and it requires about nA of current for light emission. So, high effective mobility of the TFT active layer is essential for AMOLED. Therefore, an amorphous metal oxide such as IGZO or low temperature polycrystalline silicon should be used as an active layer.

Chapter 2

Background and Motivation

2.1 Low Temperature Polycrystalline Silicon Thin-Film Transistors

Low temperature polycrystalline silicon (LTPS) thin-film transistor (TFT) is useful for active matrix liquid crystal display and active matrix organic light emitting diode. Polycrystalline silicon (poly-Si) TFT has high electric field effect mobility (200 cm^2/Vs), which is faster than that of amorphous silicon (a-Si) TFT (0.5 cm^2/Vs) [2.1]. It is possible to implement the system on glass technology in which the peripheral driving circuits are integrated together. It also has the advantage of improvement the various driving properties of the device [2.2]. There are several ways to fabricate poly-Si TFT such as chemical vapor deposition method [2.3], solid phase crystallization (SPC) [2.4, 2.5, 2.6] and excimer laser annealing (ELA) [2.7, 2.8]. However, SPC has the disadvantage that expensive quartz substrate is used and heat treatment time is long. In case of ELA, it needs the expensive laser equipment and uniform poly-Si can't be obtained on a large area substrate. Therefore, the metal

induced lateral crystallization (MILC) method has been developed to improve disadvantages of SPC and ELA [2.9-2.16]. MILC method is capable of large-area crystallization of a-Si at a low temperature (570 ºC), and it also has the advantages of low production cost and excellent electrical characteristics [2.17-2.20].

2.2 Metal Induced Lateral Crystallization

The metal induced crystallization (MIC) method, which is one of the methods for crystallizing silicon at a low temperature, is capable of crystallizing a-Si below the glass substrate strain temperature (600 ºC). When a metal such as Ag, Au, Cu, Ni, Pd or Ti is deposited on a-Si and heat-treated, silicide is generated at a low temperature (< 500 ºC). Then, Si crystallization proceed by silicide.

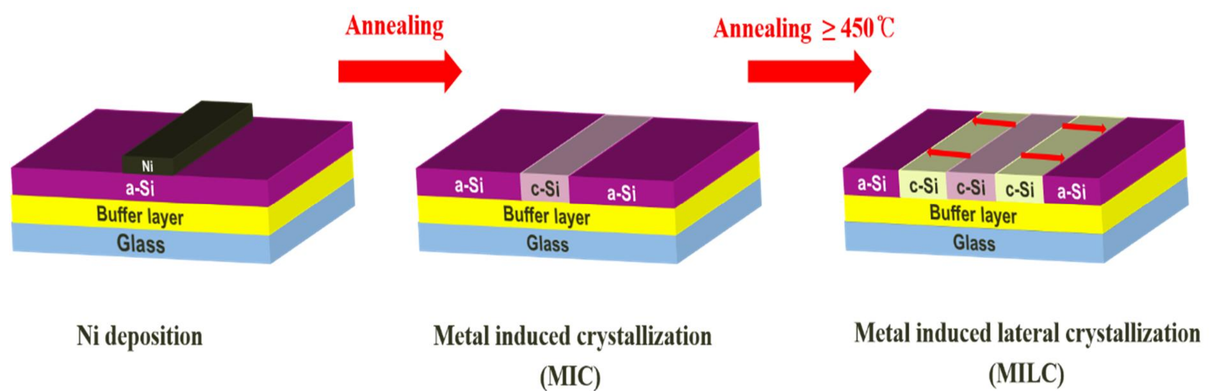


Figure 2.1 Schematic diagram of metal induced crystallization and metal induced lateral crystallization.

As shown in Figure 2.1, MIC is generated in the region of a-Si that is in contact with the metal, and crystallization proceeds on the side of the a-Si that is not in contact with the metal [2.20]. This lateral crystallization phenomenon is called MILC. When the poly-Si TFT is fabricated by MIC, the electrical characteristics are deteriorated due to the metal introduced into the silicon thin film. However, when the

poly-Si TFT is fabricated by MILC, electrical characteristics can be improved due to reduced metal contamination in the channel region of poly-Si. In particular, when a poly-Si TFT is fabricated with MILC by Ni, unlike the poly-Si TFT fabricated by SPC, no twin defects are found at all, and it has excellent electric field effect mobility. However, there is a disadvantage that the leakage current is still high. In order to reduce the leakage current, many researches have been studied such as electrical stress effect to the TFT and asymmetric offset structure to reduce metal contamination in the junction and channel region [2.21].

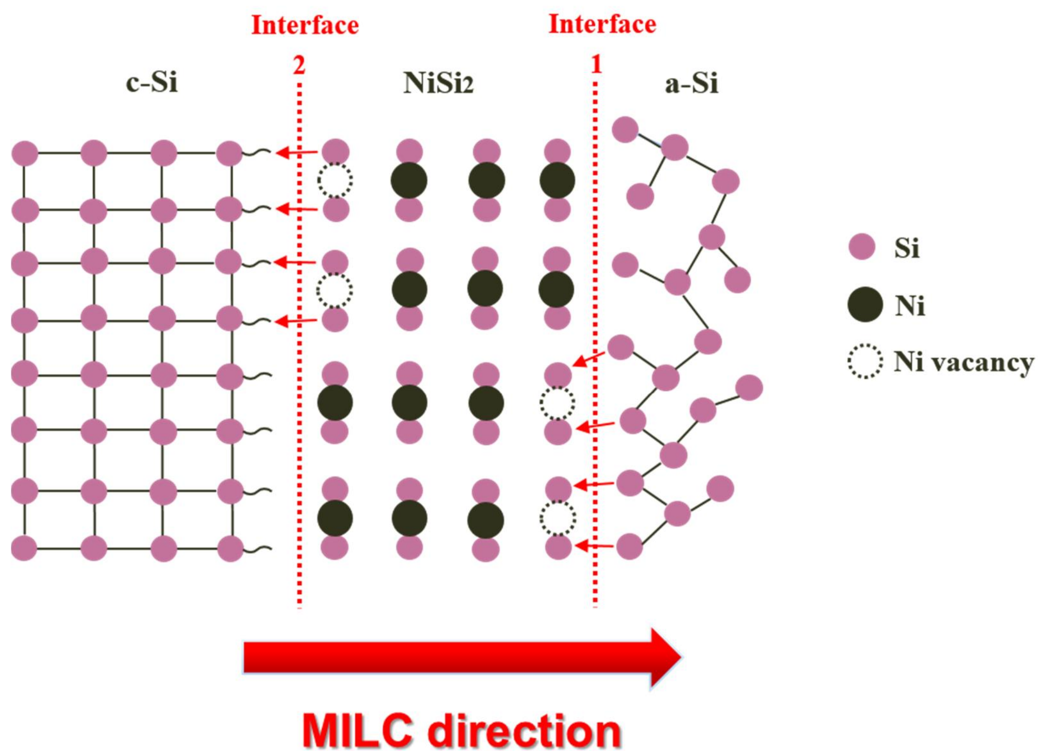


Figure 2.2 Illustration of MILC mechanism.

Figure 2.2 shows the MILC mechanism. There are two interfaces in the MILC reaction. One is the interface between a-Si and $NiSi_2$ (interface 1) and the other is the interface between poly-Si and $NiSi_2$ (interface 2). At interface 1, the Si-Si bond breaks in a-Si and the Si atoms are adsorbed to $NiSi_2$ layer to generate $NiSi_2$ and Ni vacancy. In $NiSi_2$ layer, Ni vacancy migration occurs by hopping mechanism. At interface 2, the bond of $NiSi_2$ breaks and the generated Si atom bonds with the dangling bond of poly-Si, resulting in a new c-Si layer.

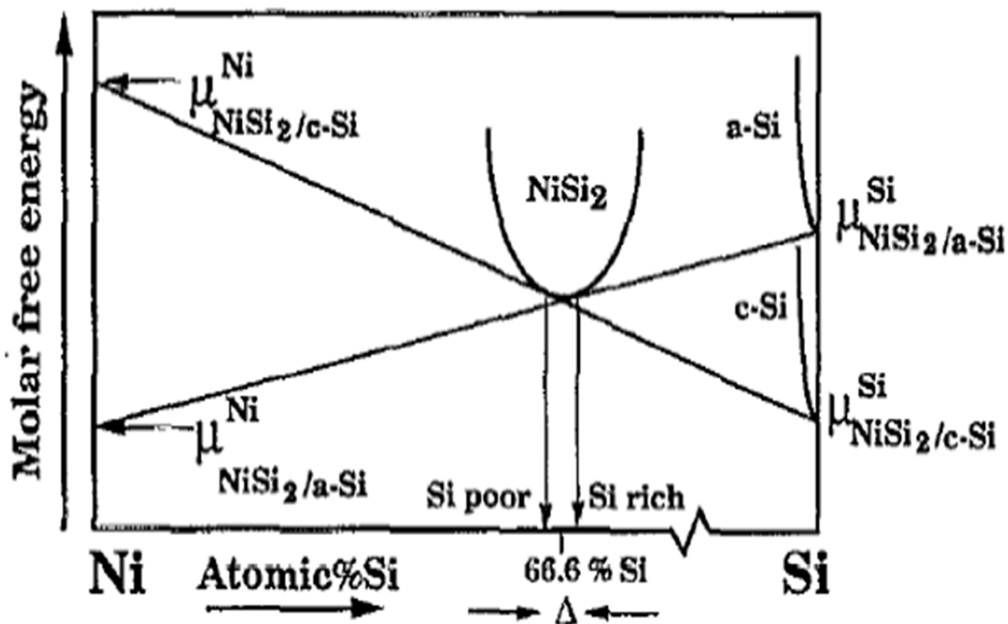


Figure 2.3 Schematic equilibrium molar free energy diagram for $NiSi_2$ in contact with a-Si and c-Si [2.11].

Figure 2.3 shows the schematic equilibrium molar free energy diagram for $NiSi_2$ in contact with a-Si and c-Si [2.11]. The driving force for the MILC is reduction of

free energy. The chemical potential of Ni at c-Si/$NiSi_2$ interface is higher than that at a-Si/$NiSi_2$ interface. And chemical potential of Si at a-Si/$NiSi_2$ interface is higher than that at c-Si/$NiSi_2$. Therefore, MILC proceeds from the c-Si region to the a-Si region by $NiSi_2$. The MILC reaction mechanism occurs in the following order.

1. Adsorption of silicon atoms at interface 1.

   : Bond breaking and migration of a-Si.

2. Migration of Ni vacancy in the nickel silicide.

   : Hopping mechanism.

3. Rearrangement of silicon atoms at interface 2.

   : Atomic rearrangement.

The driving force that silicon vacancy generated at interface 2 diffuses to interface 1 through $NiSi_2$ layer [2.22] is as follows.

1. Flux due to silicon concentration difference (Fick's first law).
2. The difference in Gibbs free energy caused by the higher thermodynamic equilibrium concentration of silicon at interface 2 than at interface 1.
3. Mechanical stress caused by physical density between a-Si and c-Si [2.11].

And MILC rate controlling step is thought to be the reaction at interface 1, which depends on the formation rate of Si atoms.

2.3 Electrical Properties of Polycrystalline Silicon Thin-Film Transistors

2.3.1 Field-Effect Mobility

The field-effect mobility (μ_{FE}) is measured by the transconductance (g_m) at V_D = 0.1 V. By applying this, the drain current (I_D) can be approximated as

$$I_D = \mu_{FE} C_{ox} \frac{W}{L} [(V_G - V_{TH})V_D]$$

The transconductance defined as

$$g_m = \frac{\partial I_D}{\partial V_G} \Big|_{V_D = constant}$$

Therefore, the μ_{FE} can be defined as

$$\mu_{FE} = \frac{L}{C_{ox} W V_D} g_m$$

2.3.2 Threshold Voltage

Threshold voltage (V_{TH}) can be defined as gate voltage that induces a channel inversion layer in semiconductor material. Many studies have been investigated to determine the V_{TH} which is one of the important parameters of poly-Si TFT. In this work, V_{TH} was calculated considering non-zero flat band voltage (V_{FB}), which can be obtained by

$$V_{TH} = V_{FB} + 2\varphi_B + \frac{\sqrt{2\varepsilon_s q N_A (2\varphi_B)}}{C_{ox}} = \left(\varphi_{ms} - \frac{Q_f}{C_{ox}}\right) + 2\varphi_B + \frac{\sqrt{4\varepsilon_s q N_A \varphi_B}}{C_{ox}}$$

2.3.3 Subthreshold Slope

Subthreshold slope is one of the important parameters of poly-Si TFT. Subthreshold slope means how fast the transistor turns on by gate voltage sweep. Subthreshold slope is defined as the amount of the gate voltage required to change a drain current by one order of magnitude, which can be obtained by

$$\text{Slope} = \frac{d(lnI_D)}{dV_G(ln10)}$$

2.3.4 Leakage Current

Leakage current of MILC poly-Si TFT are the flow of carrier generated from defect states such as metal silicide defect center [2.21].

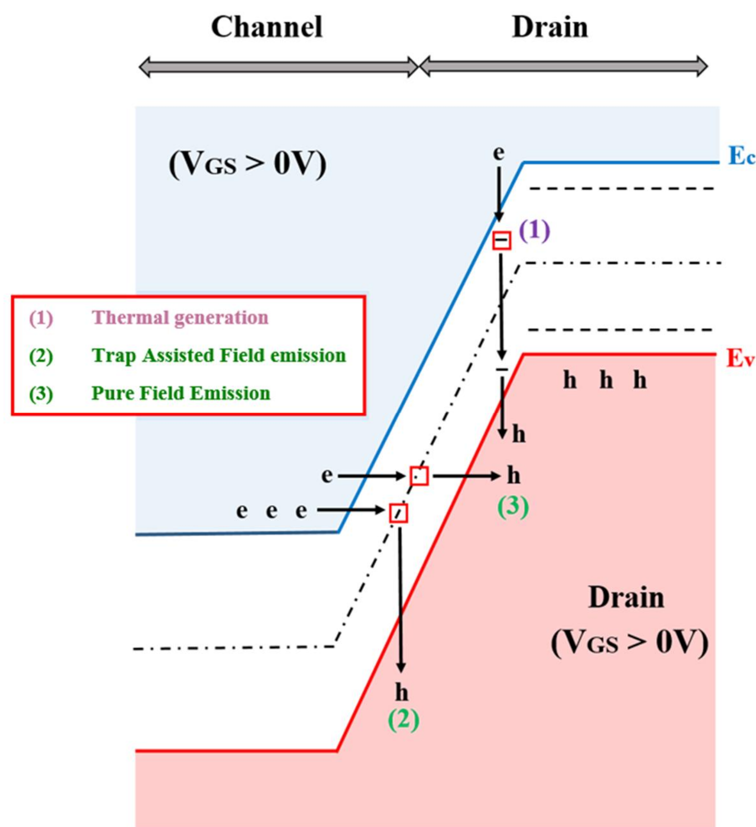


Figure 2.4 The leakage current mechanism of the p-type MILC poly-Si TFT.

Figure 2.4 shows the leakage current mechanism of p-type MILC poly-Si TFT. The leakage current can occur by three types of mechanism: (i) thermal generation at low electric field. (ii) Trap assisted field emission at intermediated electric field. (iii) Field enhanced tunneling at high electric field. Many studies have been conducted to reduce

leakage current of MILC poly-Si TFT. For example, nickel silicide gettering methods has been investigated [2.23]. Nickel silicide trapped at grain boundary can be reduced by applying the gettering method. So leakage current of MILC poly-Si TFT decreases due to reduced trap state. Lightly doped drain (LDD) structure was also investigated to suppress electric field between gate and drain electrode [2.24]. When the LDD structure is applied, potential gradient between channel and drain decreases. As a result, pinning current of MILC poly-Si TFT decreases.

Chapter 3

Gettering

3.1 Introduction

Metal-induced crystallization (MIC) can be used to manufacture polycrystalline silicon (poly-Si) thin-film transistors (TFTs) intended for use in active-matrix flat-panel displays (AMFPDs). Poly-Si TFTs fabricated via MIC offer several advantages, including a low batch cost, simple fabrication process, highly uniform surface, and longitudinal large-grain size [3.1-3.4]. However, most of the AMFPD industries have adopted excimer laser annealing (ELA) because the leakage current of poly-Si TFTs fabricated via MIC is higher than that of poly-Si TFTs fabricated via ELA. Thermal generation, band-to-band (BTB) tunneling, Poole-Frenkel (P-F) emissive current through grain boundary traps, extended defects, and the resistive properties of undoped poly-Si have been suggested to be the possible origins of the leakage current [3.5-3.9]. On the other hand, MIC poly-Si TFTs showed a serious, extensive range of contamination of nickel silicide defects, which assists in thermal generation, BTB

tunneling, and P-F emissive current. Some researchers tried to suppress the leakage current by implementing a lightly-doped drain, drain-off set, field-induced drain, and multi-gate structures to reduce the vertical electric field in the drain junction [3.10-3.13]. However, these techniques are not intrinsic solutions to ultimately achieve a low leakage current.

When metal is used as the crystallization catalyst source, MIC poly-Si TFTs will continue to have issues. Still, many attempts have been made to reduce contamination of nickel silicide to achieve a low leakage current [3.14-3.17]. Although these methods have effectively reduced the nickel silicide contamination of MIC poly-Si, high-performance poly-Si TFTs still cannot be achieved. Gettering method also has been studied to reduce Ni impurities in MIC poly-Si TFTs [3.18, 3.19]. However, mechanism of nickel silicide gettering and its effect on MIC poly-Si TFTs remain unclear. So more studies are needed about effects of nickel silicide gettering on MIC poly-Si TFTs. In this study, we fabricated a MIC poly-Si TFTs by extracting the Ni and residual nickel silicide using a sacrificial amorphous silicon (a-Si) layer to apply a "Gettering" technique. Due to the different chemical potential, Ni and residual nickel silicide migrate to the sacrificial a-Si getter layer that acts as an extraction layer for Ni and nickel silicide. As a result, the leakage current of the MIC poly-Si TFTs decreased after gettering. And we suggest an appropriate model to explain gettering effect on MIC poly-Si TFTs. The gettering was also applied to nickel silicide seed induced lateral crystallized (SILC) poly-Si TFTs. Nickel silicide in SILC poly-Si film was reduced after gettering, as a result, the leakage current of the SILC poly-Si TFTs decreased.

3.2 Experiment

A 100-nm-thick SiO_2 buffer layer was deposited on a compacted glass substrate via plasma enhanced chemical vapor deposition (PECVD). Then, a 80-nm-thick a-Si active layer was deposited via low-pressure chemical vapor deposition. On top of that, a 5-nm-thick Ni was deposited by direct current magnetron sputtering at 0.5 A. To trigger the MIC, the sample was annealed by furnace at 550 °C for 1 h in a H_2 ambient. After the crystallization process, we confirmed that the thin SiO_2 layer, which is etch stop interlayer between active layer and getter layer, was natively formed on the active Si layer surface by the following method: A 80-nm-thick active poly-Si without SiO_2 layer was completely etched after 7 min by KOH (selectivity in KOH; poly-Si:SiO_2 = 88:1), but same thickness active poly-Si with natively formed SiO_2 layer was not etched at all (etch rate of poly-Si without SiO_2 layer was 114.2 Å/min). Then, on the natively formed SiO_2 layer, a 20-nm-thick a-Si getter layer was deposited via PECVD and gettering annealing was performed via rapid thermal annealing (RTA) [3.20]. RTA was carried out with a halogen lamp as a heating source and a thermocouple to measure the temperature. RTA gettering annealing was performed by heating at a speed of 3 °C/sec in air. The partially crystallized Si getter layer was removed by dipping into a KOH solution. The natively formed SiO_2 layer was not etched by KOH during the removal of the Si getter layer. Therefore, the natively formed SiO_2 was removed with 1% HF solution. After finishing the gettering process, a 50-nm-thick silicon nitride was deposited as a gate insulator via PECVD, and a 200-

nm-thick MoW was deposited as a gate metal via direct current magnetron sputtering. The gate metal was etched using a wet etchant (H_3PO_4 + CH_3COOH + HNO_3 + H_2O) and silicon nitride was etched with reactive ion etching using SF_6, Ar, and CHF_3 gases [3.21]. The source and the drain regions were doped with an ion mass doping system using B_2H_6 gas. After the doping process, furnace annealing was carried out to electrically activate the dopant. The gettering method was also applied to SILC poly-Si TFT. A 80-nm-thick a-Si active layer was crystallized by SILC method [3.15]. Then, a-Si getter layer was deposited via PECVD and gettering annealing was performed by furnace at 550 °C. After finishing gettering annealing, the getter layer was removed by KOH. The remaining fabrication processes were the same as the fabrication processes of gettered MIC poly-Si TFT. The drain current-gate voltage (I_D-V_G) transfer curves were then measured using a Keithley 2636 system.

3.3 Result and Discussion

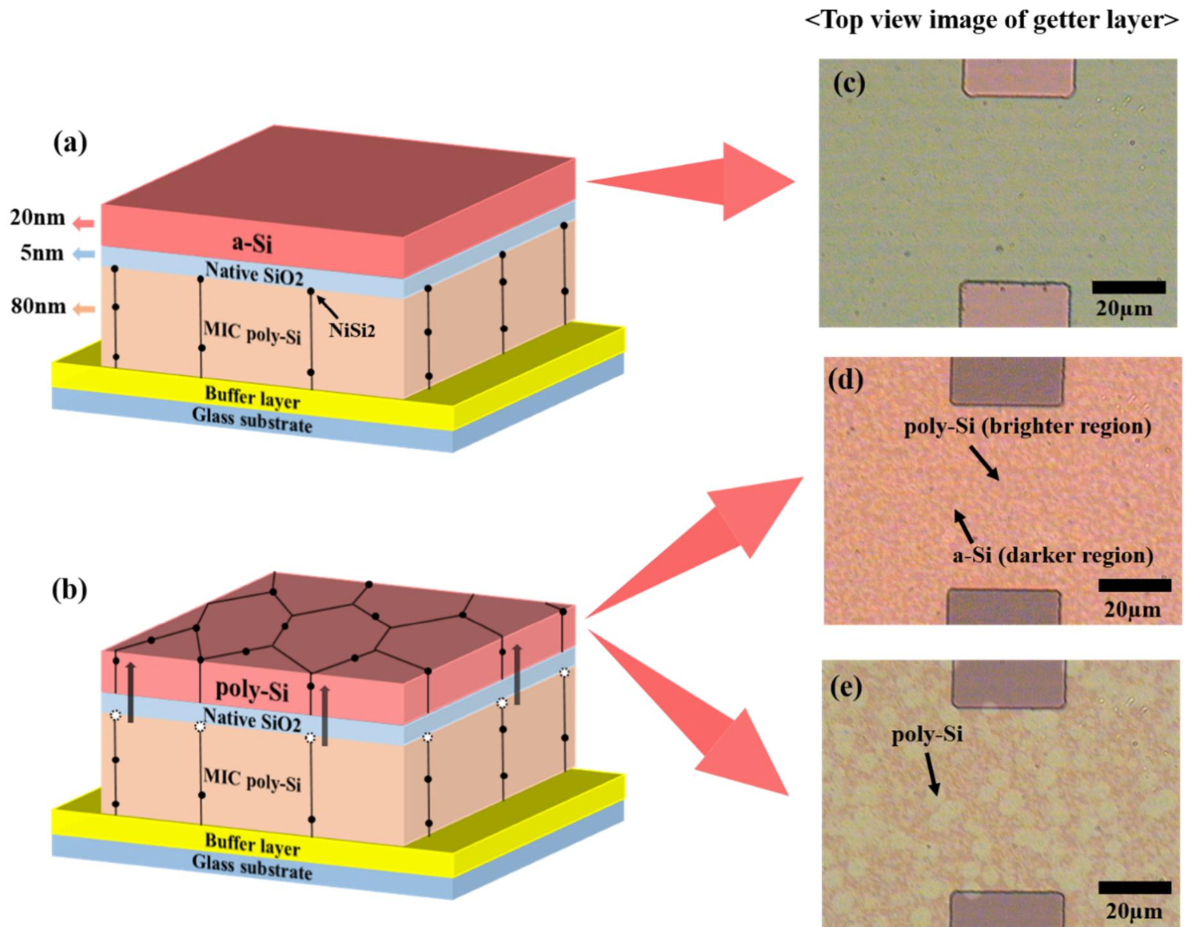


Figure 3.1 Schematics of the key processes for gettered MIC poly-Si TFTs including natively formed SiO_2 and getter layer deposition (a) before gettering annealing and (b) after gettering annealing. Optical microscopy image of the getter layer (c) before gettering annealing, (d) after gettering annealing by RTA for 120 sec, and (e) after gettering annealing by RTA for 140 sec.

Figure 3.1 shows the schematics of the key process to obtain gettered MIC poly-Si TFTs and optical microscopy (OM) image of the getter layer after gettering annealing. A 20-nm-thick a-Si getter layer was deposited on a natively formed SiO_2 layer, as shown in Figure 3.1(a), (c), followed by gettering annealing. As shown in Figure 3.1(b), (d), (e), the Si getter layer was partially crystallized by the nickel silicide diffused from grain boundary in active poly-Si. The nickel silicide at the grain boundary in active poly-Si can migrate to getter a-Si layer through the thin SiO_2 interlayer. This basic principle of nickel silicide gettering has been well studied in previous works [3.19, 3.22, 3.23, 3.24]. Figure 3.1(d), (e) show the top-view OM image of the getter layer after gettering annealing by RTA for 120 sec (final temperature was 400 °C) and 140 sec (final temperature was 450 °C), respectively.

A comparison of typical I_D-V_G characteristics of MIC and gettered-MIC poly-Si TFTs with different gettering annealing time is shown in Figure 3.2(a). When comparing gettering annealing at 120 sec and 140 sec, the getter layer showed more crystallization at 140 sec than at 120 sec. However, the MIC poly-Si TFTs gettering annealed for 120 sec (G120-MIC) exhibited better electrical properties than MIC poly-Si TFTs gettering annealed for 140 sec (G140-MIC). In the case of G120-MIC, the on/off ratio drastically improved, more than quadrupled, by gettering. It successfully lowered the minimum leakage current ($I_{min,off}$) by almost an order of magnitude, and threshold voltage (V_{th}), subthreshold slope (S.S) also improved. The V_{th} and S.S are also related to defects at the active Si channel surface, so nickel silicide, which is major defect at the channel, is considered to have decreased by gettering. The leakage current of G140-MIC also decreased by gettering, but it

decreased less than that of G120-MIC even though the getter layer for G140-MIC was more crystallized by gettering than that of G120-MIC. The gettering mechanism is the same as with metal-induced lateral-crystallization. The Ni can migrate though the $NiSi_2$ layer because the chemical potential of Ni at $NiSi_2$/a-Si interface is lower than that at the $NiSi_2$/c-Si interface, and $NiSi_2$ crystallite also migrates together with Ni [3.25]. However, once Ni migrates from crystalline silicon (c-Si) to a-Si, there is no chemical potential difference between Ni at the $NiSi_2$/a-Si interface and at the $NiSi_2$/c-Si interface. Therefore, nickel silicide does not migrate from the top area of an active Si layer to the bottom area of the getter Si layer anymore. Thus, further gettering annealing is considered not to be effective in reducing the nickel silicide in the active Si layer. And it was reported that thermal damage degrades the electrical properties of poly-Si TFT [3.26, 3.27]. For these reasons, the electrical properties of G140-MIC were worse than those of G120-MIC. Table 3.1 presents the key parameters that were measured and calculated. The channel width and the length were 10 μm respectively, and the drain voltage (V_D) = -1 V and gate voltage (V_G) in the range of $-20 \text{ V} < V_G < 10 \text{ V}$. Gettering annealing without getter layer was also performed by RTA for 120 sec and 140 sec respectively. Electrical properties of MIC poly-Si TFTs gettering annealed without getter layer, especially leakage current and field-effect mobility, were worse than those of conventional MIC poly-Si TFTs. This result means that nickel silicide gettering is effective for improving electrical properties of MIC poly-Si TFTs beyond thermal damage.

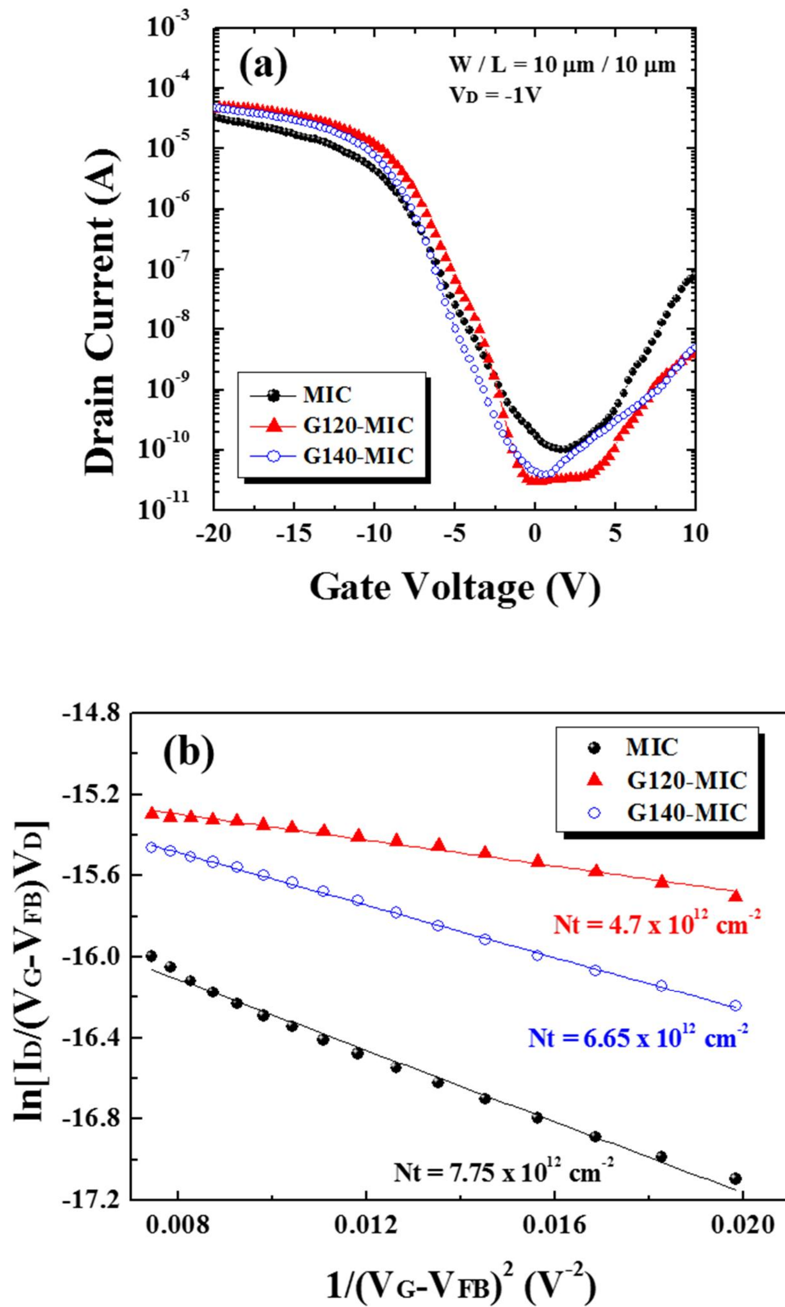


Figure 3.2 (a) Comparison of the electrical properties of MIC and gettered MIC poly-Si TFTs with different gettering annealing time. (b) Levinson and Proano plots of MIC and gettered MIC poly-Si TFTs with different gettering annealing time.

W / L = 10 μm /10 μm (V_D = -1 V)	MIC	G120-MIC	G140-MIC
Field-effect mobility μ_{FE} (cm^2/Vs)	42.6	35.1	32.6
Threshold voltage V_{th} (V)	-6.2	-5.3	-6.3
Subthreshold slope S.S (V/dec)	1.5	0.9	1.1
Minimum leakage current $I_{min,off}$ (x 10^{-11} A)	10.3	3.1	3.9
Leakage current at V_G = 10 V $I_{pin,off}$ (x 10^{-9} A)	79	4.2	5.1
Maximum on current $I_{max,on}$ (x 10^{-5} A)	3.4	5.0	4.8
Maximum on/off ratio (x 10^5)	3.3	16	12

Table 3.1 Device characterization of MIC and gettered MIC poly-Si TFTs with different gettering annealing time.

Figure 3.2(b) shows the trap-state density (N_t), which is the dominant leakage source and is a result of nickel silicide trapped in the channel area. N_t was obtained by Levinson and Proano method, which was well studied to estimate concentration of traps located at grain boundaries in low temperature poly-Si [3.28, 3.29]. N_t was calculated from the slope of a linear region of the curve ln[I_D/(V_G – flat band voltage (V_{FB}))] versus $(V_G\text{-}V_{FB})^{-2}$ at a low V_D and high V_G. The plots were given as

$$I_D = \mu_0 C_{nit} \frac{W}{L}(V_G - V_{FB})V_D \exp\left(-\frac{q^2 N_t^2 \sqrt{\varepsilon_{nit}/\varepsilon_s}}{C_{nit}^2 (V_G - V_{FB})^2}\right) \quad (1)$$

Here, W, L and C_{nit} (1.33 x 10^{-7} F) are the channel width, length and gate insulator capacitance, and ε_{nit} (7.5) and ε_s are the silicon nitride and silicon dielectric constants, respectively. The V_{FB} were extracted from Weisfield and Anderson method [3.30]. As shown in Figure 3.2(b), the N_t for G120-MIC was 4.7 x 10^{12} cm^{-2}, which was almost half that of MIC poly-Si TFTs (7.75 x 10^{12} cm^{-2}). A comparison between G120-MIC and G140-MIC revealed that the N_t for G120-MIC was lower than that of G140-MIC (6.65 x 10^{12} cm^{-2}). From the results of two different gettering annealing time, it can be considered that a longer gettering annealing time cannot effectively reduce the nickel silicide in the active Si layer.

The getter layer according to the gettering cycles is shown in Figure 3.3. To clearly observe the gettering phenomenon in the getter layer, gettering annealing was conducted with RTA for 140 sec instead of 120 sec. The getter layer was removed via

KOH after gettering annealing, and then a 20-nm-thick Si getter layer was deposited via PECVD repeatedly. Figure 3.3(a) shows an OM image of the getter layer after 1-cycle gettering, and Figure 3.3(b), (c), and (d) show the getter layer after 2-cycles, 3-cycles and 4-cycles of gettering, respectively. The nickel silicide in the active Si layer gradually decreased with additional gettering.

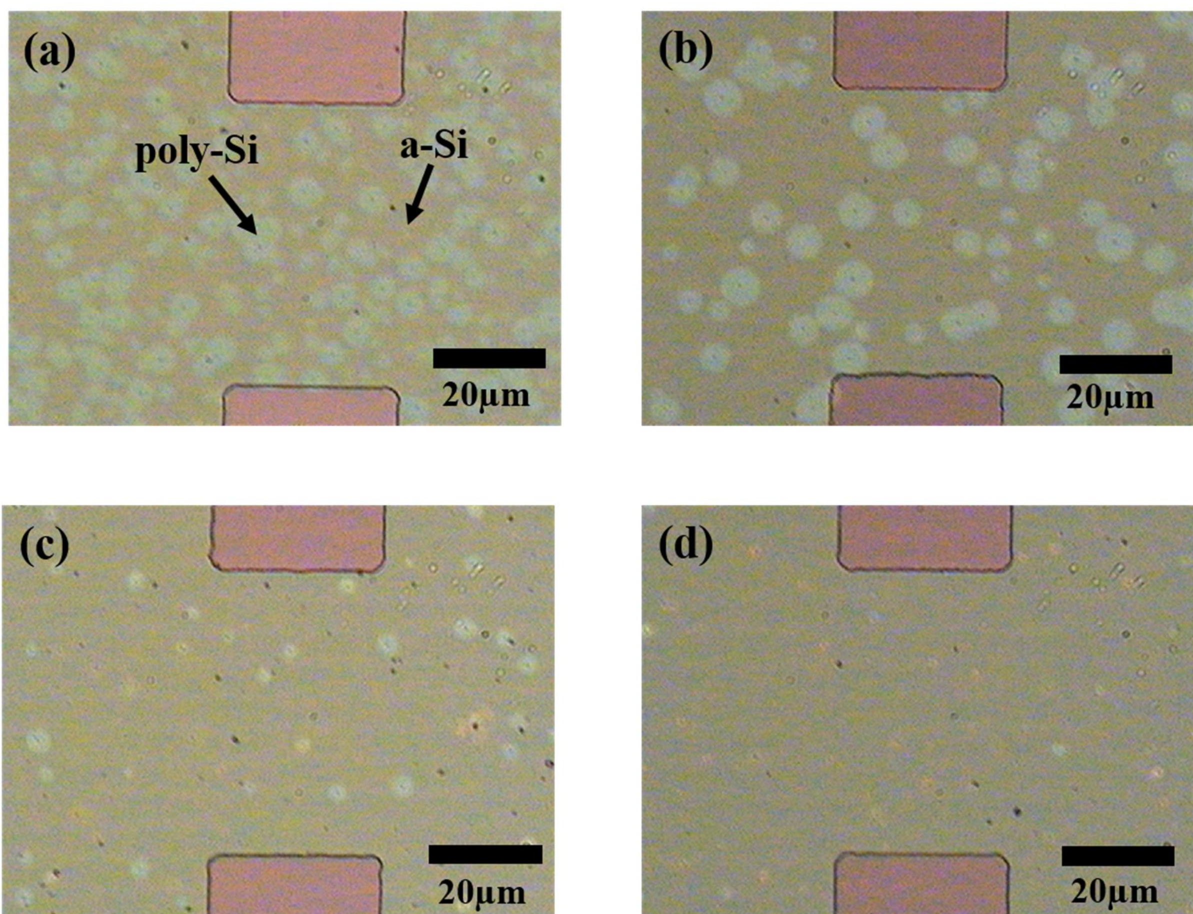


Figure 3.3 Optical microscopy images of the getter layer after gettering annealing with increased number of gettering cycles. The getter layer was removed after gettering annealing and redeposited. (a) 1-cycle, (b) 2-cycles, (c) 3-cycles, (d) 4-cycles gettering annealing.

Figure 3.4(a) shows the N_t of MIC and gettered MIC poly-Si TFTs according to the number of gettering cycles. The N_t of the MIC poly-Si TFTs was successfully lowered by performing additional gettering. The N_t of the MIC poly-Si TFTs was 7.75 x 10^{12} cm^{-2}, the N_t of the 1-cycle gettered MIC poly-Si TFTs (G1MIC) was 6.65 x 10^{12} cm^{-2}, and that of the 4-cycles gettered MIC poly-Si TFTs (G4MIC) was 3.8 x 10^{12} cm^{-2}. A 5-cycles gettering annealing was also performed, but the OM image of getter layer and N_t of MIC poly-Si TFTs were almost same with 4-cycles gettered MIC poly-Si TFTs. So it is considered that 4-cycles of gettering is saturated state in this gettering system. A comparison of the typical I_D-V_G characteristics of the MIC and gettered-MIC poly-Si TFTs according to the gettering cycles is shown in Figure 3.4(b). The pinning current (I_{pin}), which is the leakage current at a high reverse V_G (V_G = 10 V), gradually decreased as the gettering cycles increased. In the case of G4MIC, I_{pin} was reduced to almost one-hundredth despite the thermal damage induced by the gettering annealing process. This means that the nickel silicide in the active Si is the dominant leakage source for MIC poly-Si TFTs. Figure 3.4(c) shows the I_{pin} between MIC and gettered MIC poly-Si TFTs as drain voltage increases. The I_{pin} of MIC poly-Si TFTs was more sensitive to the drain voltage than that of gettered MIC poly-Si TFTs, and sensitivity of I_{pin} to the drain voltage gradually decreased with additional gettering. It was reported that rapid increase of leakage current at high reverse V_G is due to holes trapped at trap site located in the space charged region between the channel and drain [3.31, 3.32]. So it is considered that trap site originated by nickel silicide defect successfully decreased by additional gettering. Table 3.2 presents the measured and

calculated key parameters. The channel width and the length were 10 μm respectively, and V_D = -1 V and V_G in the range of – 20 V < V_G < 10 V.

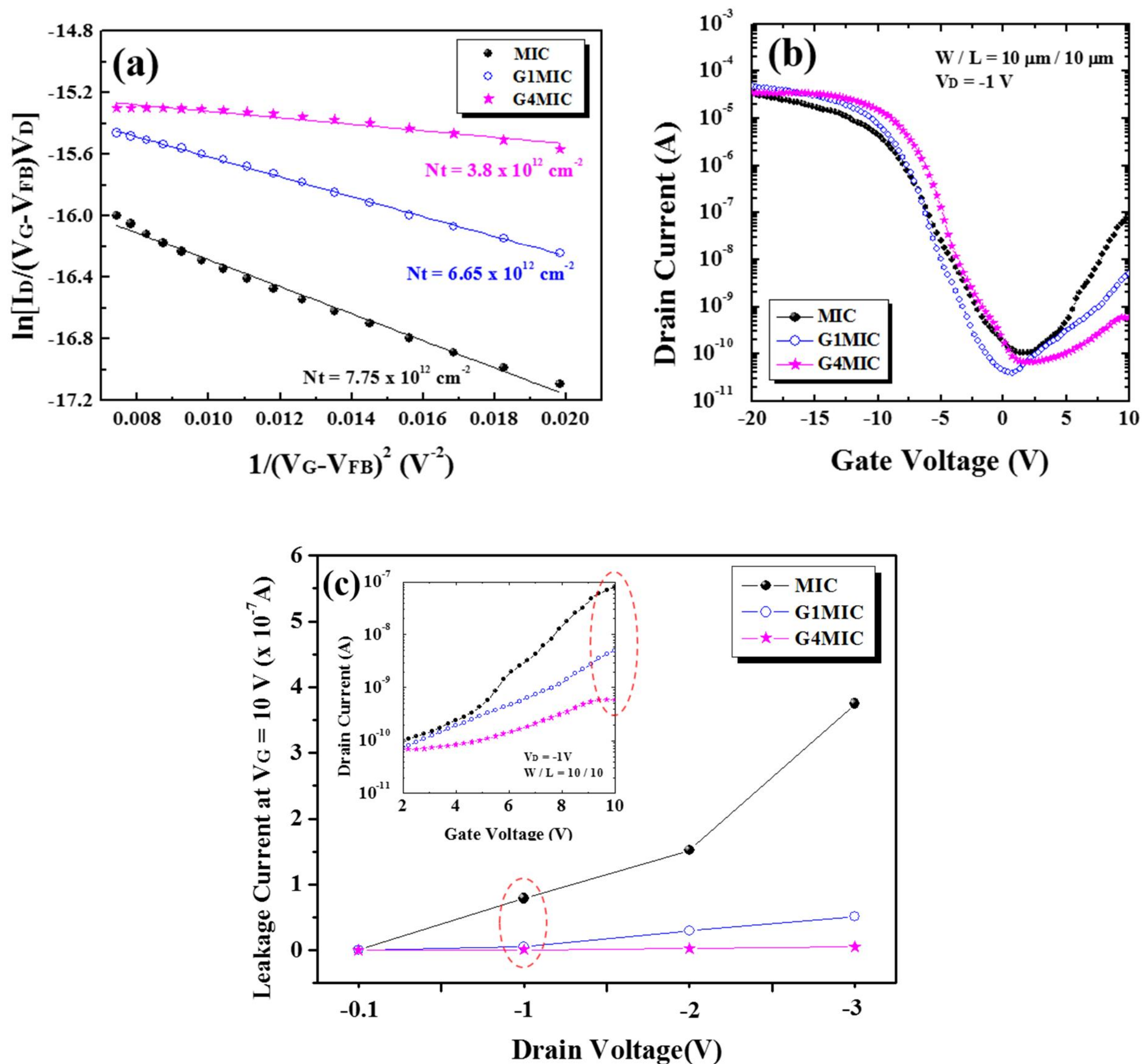


Figure 3.4 (a) Levinson and Proano plots of MIC and gettered MIC poly-Si TFTs with increased number of gettering cycles. (b) Comparison of the electrical properties of the MIC and gettered MIC poly-Si TFTs with increased number of gettering cycles. (c) Dependence of the leakage current at high reverse gate voltage on drain voltage.

To explain gettering effect on MIC poly-Si TFTs, we suggest an appropriate model of the leakage current mechanism in poly-Si TFTs as shown in Figure 3.5(a). The holes can be excited from trap states to the valence band in the following three ways [3.33, 3.34].

1) Thermally generated carrier via shallow level trap states, which is caused by the thermal excitation of trapped holes into the valence band at a low electric field.
2) Trap assisted field emission via shallow level and deep level trap states, which is caused by the field-enhanced thermal excitation of trapped holes into the valence band at intermediate electric fields.
3) Pure field emission via deep level trap states, which is caused by the field enhanced tunneling of trapped holes into valence band in a high electric field.

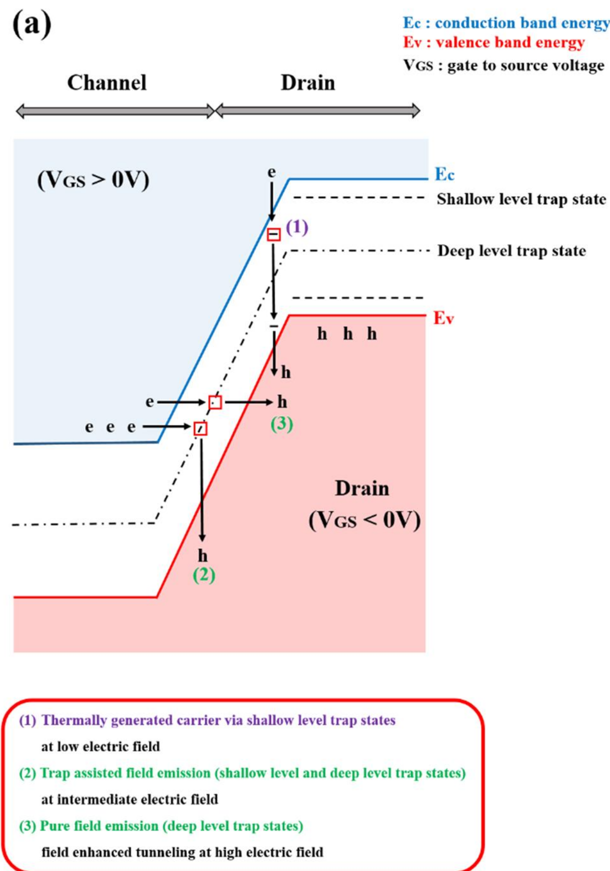
And the shallow level trap state and deep level trap state can be defined as [3.35, 3.36]

4) Shallow level trap state located close to the band edges (either valence band or conduction band).
5) Deep level trap state located close to the middle of the band gap.
6) The energy required to remove a hole from the trap to the valence band or conduction band is higher for the deep level trap state than for the shallow level trap state.

In case of 1-cycle gettered MIC poly-Si TFTs, the leakage current of the gettered MIC poly-Si TFTs was mostly reduced at a low reverse V_G area as shown in Figure 3.2(a), and the leakage current of poly-Si TFTs at a low reverse V_G area is mainly induced by defects located in the shallow level trap state.

W / L = 10 μm /10 μm (V_D = -1 V)	MIC	G1MIC	G4MIC
Field-effect mobility μ_{FE} (cm^2/Vs)	42.6	32.6	35.2
Threshold voltage V_{th} (V)	-6.2	-6.3	-4.8
Subthreshold slope S.S (V/dec)	1.5	1.1	1.1
Minimum leakage current $I_{min,off}$ (x 10^{-11} A)	10.3	3.9	6.7
Leakage current at V_G = 10 V $I_{pin,off}$ (x 10^{-9} A)	79	5.1	0.6
Maximum on current $I_{max,on}$ (x 10^{-5} A)	3.4	4.8	3.5
Maximum on/off ratio (x 10^5)	3.3	12	5.2

Table 3.2 Device characterization of MIC and gettered MIC poly-Si TFTs with different number of gettering cycles.



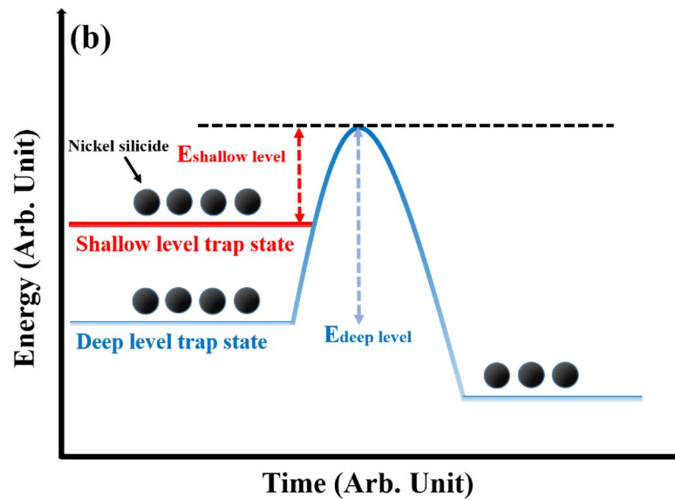


Figure 3.5 (a) The leakage current mechanism of the p-type poly-Si TFTs. (b) Assumed activation energy diagram for nickel silicide located in shallow level and deep level trap state.

Therefore, the nickel silicide located in a shallow level trap state is confirmed to be reduced by 1-cycle gettering. However, there was no significant effect to reduce the leakage current of MIC poly-Si TFTs in the high reverse V_G (V_G > 3 V) area by 1-cycle gettering. The leakage current of poly-Si TFTs at a high reverse V_G area is induced by the defect located in the deep level trap state as well as shallow level trap state (it is known that Ni produces deep-level defects in silicon [3.34]). Figure 3.5(b) shows the assumed activation energy level of nickel silicide in MIC poly-Si film. The energy level in solid crystals is determined by the crystal structure. MIC poly-Si consists of various Si and $NiSi_2$ planes such as Si (110), (220) and $NiSi_2$ (111), (200), (222). So it is considered that deep and shallow level trap states can be formed by the correlation between Si and $NiSi_2$. Many nickel silicides may be located at deep and shallow level trap states in the MIC poly-Si film. And gettering is a competition reaction of nickel silicide at the interface between the active poly-Si layer and getter a-Si layer to diffuse from the active poly-Si layer to getter a-Si layer. In addition, nickel silicide located in the shallow level trap state, which has a low activation energy for $NiSi_2$ to diffuse from poly-Si to a-Si as shown in Figure 3.5(b), may preferentially diffuse from the active poly-Si layer to the getter a-Si layer. For these reasons, the nickel silicide in the active Si layer cannot be completely removed by 1-cycle gettering. As a result, the leakage current of the gettered MIC poly-Si TFTs at a high reverse V_G area was not significantly reduced because the nickel silicide located in the deep level trap state was barely removed by 1-cycle gettering. However, the leakage current of the MIC poly-Si TFTs at a high reverse V_G and the sensitivity of I_{pin} to the drain voltage decreased with additional gettering as shown in Figure 3.4(c). This result

can indicate that nickel silicide located in the deep level trap state was removed by additional gettering.

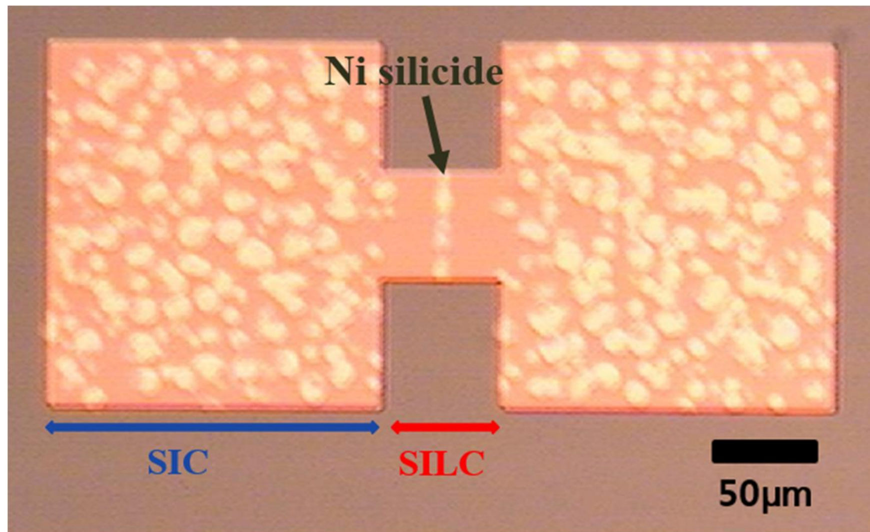
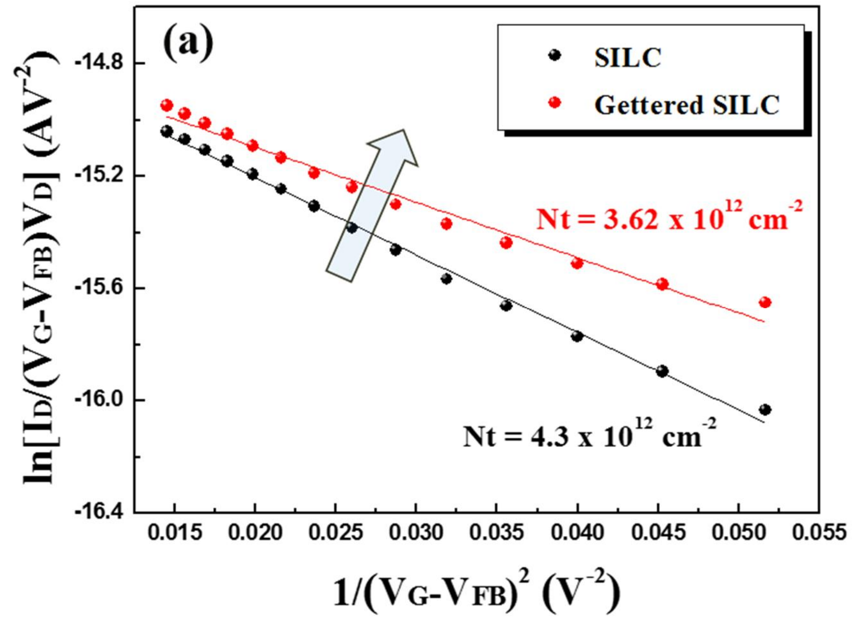


Figure 3.6 Optical microscopy images of the getter layer after gettering (SILC poly-Si).

Figure 3.6 shows the OM image of the getter layer of SILC poly-Si after gettering. Unlike MIC poly-Si film, in the case of SILC poly-Si film, the gettering phenomenon was not observed in the channel region except for the center of the channel. This result indicates that the amount of nickel silicide in the poly-Si channel region was significantly reduced by the SILC method.

Figure 3.7(a) shows the N_t of SILC and gettered SILC poly-Si TFTs. The N_t of the SILC poly-Si TFTs was successfully reduced by gettering. The N_t of the SILC poly-Si TFTs was 4.3 x 10^{12} cm^{-2} and that of the gettered SILC poly-Si TFTs was 3.62 x 10^{12} cm^{-2}. Additional gettering annealing was also performed, but the gettering

phenomenon was not observed in the channel region. So, in the case of SILC poly-Si TFTs, it is



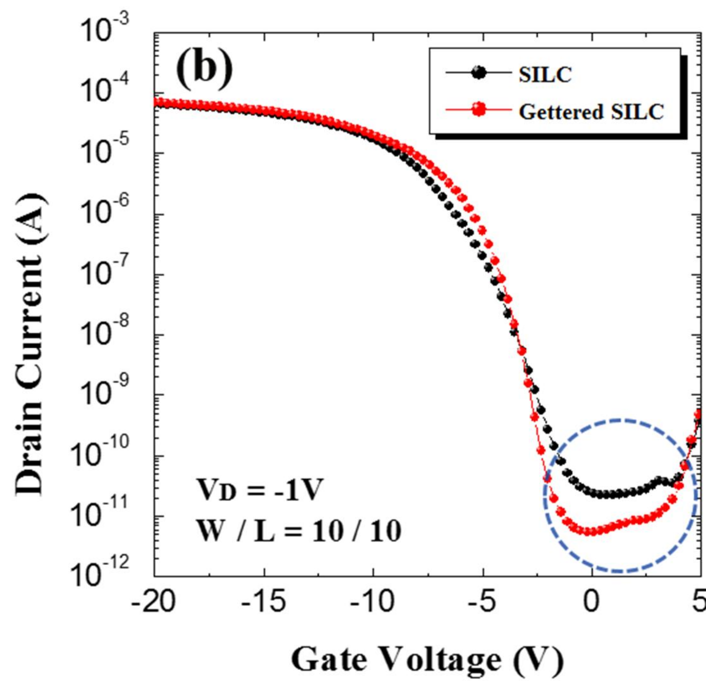


Figure 3.7 (a) Levinson and Proano plots of SILC and gettered SILC poly-Si TFTs. (b) Comparison of the electrical properties of the SILC and gettered SILC poly-Si TFTs.

considered that 1-cycle gettering is sufficient to remove the nickel silicide located at the poly-Si channel region. A comparison of the typical I_D-V_G characteristics of the SILC and gettered SILC poly-Si TFTs is shown in Figure 3.7(b). The $I_{min,off}$ of SILC poly-Si TFTs was 22.5 x 10^{-12} A and that of gettered SILC poly-Si TFTs was 5.4 x 10^{-12} A. This result means that the nickel silicide in the active poly-Si, which is the dominant leakage source for SILC poly-Si TFTs, decreased by gettering.

3.4 Conclusion

In summary, Ni impurities in the MIC poly-Si film were successfully reduced by gettering. As a result, the leakage current of MIC poly-Si TFTs decreased significantly. The results indicate that: (i) gettering is less effective for the MIC poly-Si TFTs when the gettering annealing temperature is high because of thermal damage induced by gettering annealing, and (ii) the nickel silicide in the MIC poly-Si film can be reduced through additional gettering. The N_t of the MIC poly-Si film gradually decreased with additional gettering, and as a result, the I_{pin} of MIC poly-Si TFTs at high reverse V_G gradually decreased. In the case of 4-cycles gettered MIC poly-Si TFTs, the N_t of the MIC poly-Si film decreased from 7.75 to 3.8 x 10^{12} cm^{-2}, and I_{pin} of MIC poly-Si TFTs was reduced to almost one-hundredth. These results can be explained by the behavior of nickel silicides located in the shallow level trap state and deep level trap state. Also, nickel silicide in the SILC poly-Si film can be removed by getteing. As a result, $I_{min,off}$ of SILC poly-Si TFTs decreased.

Chapter 4

Drain Offset Gate

4.1 Introduction

Low-temperature polycrystalline-silicon (poly-Si) thin-film transistor (TFT) fabricated by metal-induced lateral crystallization (MILC) is an attractive candidate for switching and driving elements in large-scaled active-matrix flat-panel displays (AMFPDs) because of its low-batch cost, simple fabrication process, highly uniform surface and longitudinal large-grain size [4.1-4.11]. However, in spite of high-batch cost and non-uniform surface, most of the AMFPD industries adopted the poly-Si TFT fabricated by excimer laser annealing (ELA) [4.12] because the leakage current of MILC poly-Si TFT is relatively higher than that of the ELA poly-Si TFT.

It was reported that the leakage current of MILC poly-Si TFTs is induced by charged trap state at the interface between gate insulator and poly-Si active layer, and trap state originates from impurities such as nickel and nickel silicide [4.13, 4.14]. It

was also reported that trap state is activated by high electric field between the gate and the drain [4.15-4.18]. To solve this problem, lightly doped-drain (LDD) structure MILC poly-Si TFTs fabricated by LDD mask has been investigated [4.19, 4.20]. However, this fabrication method using LDD mask is sensitive to gate insulator thickness. For example, the thinner gate insulator thickness is, the less effective LDD effect is. In this study, we developed a double exposure method. The leakage current of MILC poly-Si TFTs fabricated by double exposure method drastically decreased, and this double exposure method can be compatible with any gate insulator thickness.

4.2 Experiment

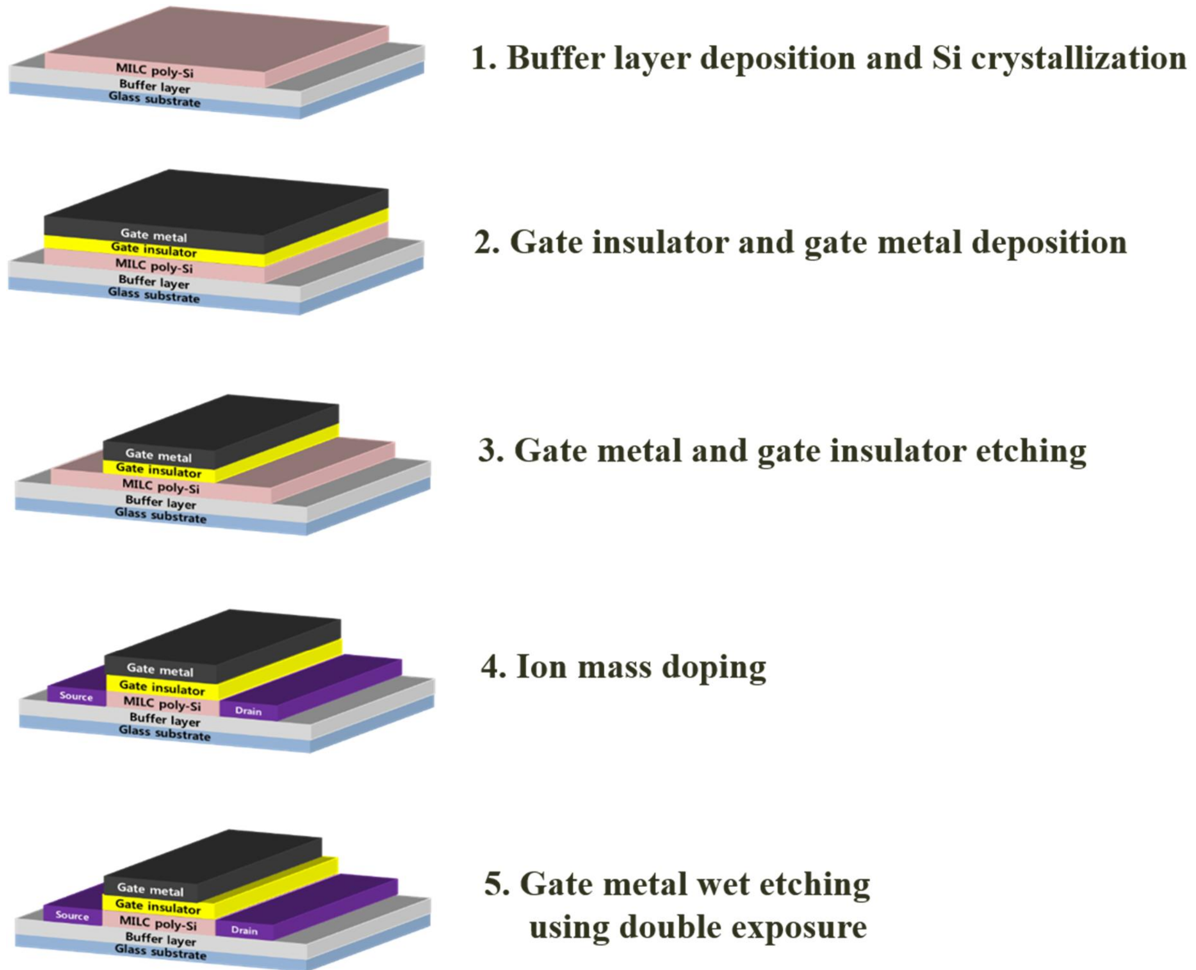


Figure 4.1 The fabrication process of MILC poly-Si TFTs fabricated by double exposure method.

Top-gate p-channel MILC poly-Si TFTs were fabricated on the glass substrate. Figure 4.1 shows an entire process of fabricating MILC poly-Si TFTs. First, a 100 nm-thick SiO_2 for buffer layer was deposited on the glass substrate by plasma enhanced chemical vapor deposition (PECVD) at 350 °C. Then, a 80 nm-thick amorphous

silicon (a-Si) for active layer was deposited by low pressure chemical vapor deposition at 500 °C. Poly-Si for active layer was crystallized by MILC method [4.21]. After crystallization, a 50 nm-thick silicon nitride for gate insulator was deposited by PECVD at 350 °C, and a 200 nm-thick molybdenum-tungsten alloy for gate metal was deposited by direct current magnetron sputtering at 300 °C. Then, the gate metal was wet etched with gate mask using a wet etchant (H_3PO_4 + CH_3COOH + HNO_3 + H_2O) and gate insulator was dry etched by reactive ion etching [4.22]. The source and the drain regions of the p-channel poly-Si TFTs were doped with an ion mass doping (IMD) system using B_2H_6 gas. After the doping process, once again the gate mask was used to define drain offset region. Then, to electrically activate the dopants, furnace annealing was carried out at 550 °C for 2 h in H_2 ambient. The drain current-gate voltage (I_D-V_G) transfer curves were measured with a Keithley 2636 System.

4.3 Result and Discussion

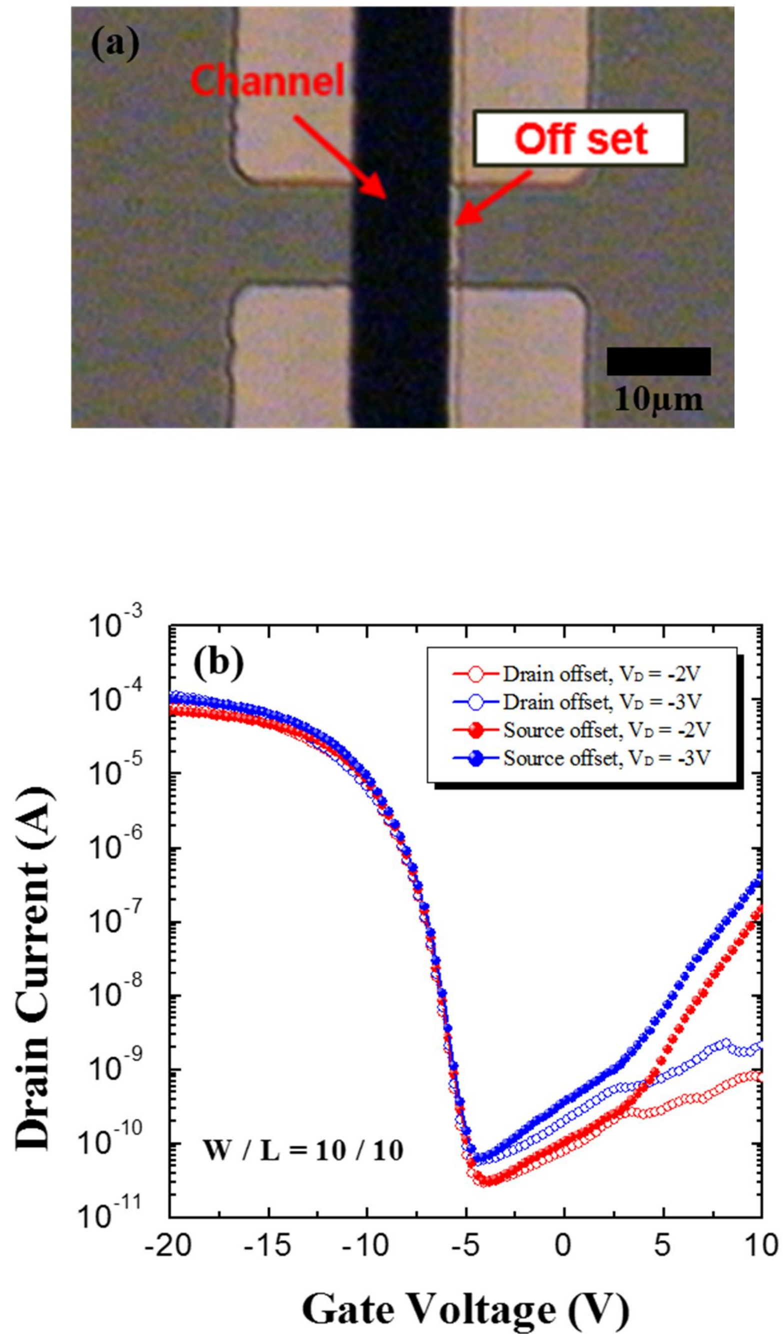


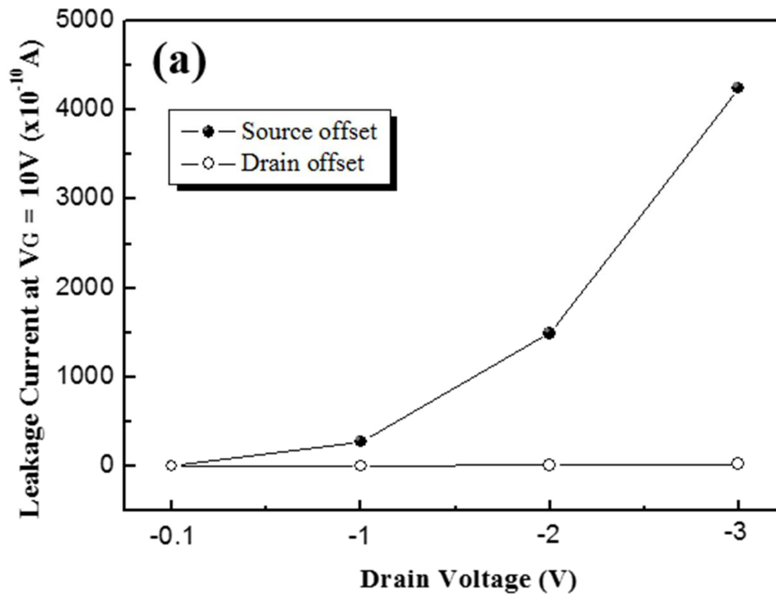
Figure 4.2 (a) Optical microscope top view of drain offset structure and (b) I_D-V_G characteristics of MILC poly-Si TFTs.

The gate mask was used for gate definition and drain offset formation, which is double exposure method. By using double exposure method, we could obtained a 1 μm drain offset length as shown in Figure 4.2(a). Figure 4.2 (b) shows the I_D-V_G characteristics of the p-type MILC poly-Si TFTs. Drain offset means offset region is on the drain side and source offset means offset region is on the source side. I_D-V_G characteristics were measured on the same TFT by just changing the source and the drain. The drain offset poly-Si TFTs exhibit a maximum on current ($I_{max,on}$) of 1.14 x 10^{-4} A, a minimum leakage current ($I_{min,off}$) of 5.76 x 10^{-11} A, a pinning current which is leakage current at V_G = 10 V ($I_{pin,off}$) of 2.13 x 10^{-9} A, a threshold voltage (V_{th}) of -7.2 V at V_D = -3 V and a subthreshold slope (SS) of 0.6 V dec^{-1}. On the other hand, source offset poly-Si TFTs exhibit a $I_{max,on}$ of 1.03 x 10^{-4} A, a $I_{min,off}$ of 6.35 x 10^{-11} A, a $I_{pin,off}$ of 4.25 x 10^{-7} A, a V_{th} of -7.1 V at V_D = -3 V and a SS of 0.6 V dec^{-1}. By comparing the $I_{pin,off}$ between drain offset and source offset poly-Si TFTs, $I_{pin,off}$ of drain offset poly-Si TFTs drastically decreased. The excitation of holes trapped at the space charged region between the channel and the drain causes high leakage current at high reverse V_G [4.13, 4.14]. The LDD region drops the potential between the gate and the drain so that potential across the lightly doped region is not enough to excite holes trapped at the trap sites in the space charged region [4.20]. As a result, the $I_{pin,off}$ of drain offset poly-Si TFTs was lower than that of source offset poly-Si TFTs due to dropped potential between the gate and the drain.

Figure 4.3 (a) shows the $I_{pin,off}$ between drain offset and source offset poly-Si TFTs as drain voltage increases. The $I_{pin,off}$ of source offset poly-Si TFTs was more sensitive to the drain voltage than that of the drain offset poly-Si TFTs. It has been studied that

rapid increase of leakage current at high reverse V_G is due to holes trapped at trap site located in the space charged region between the channel and the drain [4.13, 4.14]. So, it is considered that $I_{pin,off}$ of drain offset poly-Si TFTs is less sensitive than that of source offset poly-Si TFTs due to reduced excitation of holes trapped in space charged region. In the case of $I_{max,on,}$ there is no significant different between drain offset and source offset poly-Si TFTs as shown in Figure 4.3(b). These results mean that drain offset structure is mainly related to the leakage current behavior.

Figure 4.4(a) shows the schematic structure of MILC poly-Si TFTs according to the drain offset length. The drain offset length increased by artificially moving the position of the gate mask when performing a double exposure process. As the drain offset length increases, the length of the channel decreases by an increased drain offset length. Figure 4.4(b) shows the I_D-V_G characteristics of MILC poly-Si TFTs according to the drain offset length. As the drain offset length increased, the $I_{max,on}$ and $I_{pin,off}$ decreased. When the drain offset length was about 1 μm, $I_{pin,off}$ drastically decreased without decreasing $I_{max,on}$. However, when the drain offset length was about 3 μm, $I_{max,on}$ drastically decreased. If the drain offset length is too long, the movement of the carrier from the channel to the drain may be suppressed. So, it is considered that the 3 μm length drain offset is too long and the 1 μm length drain offset is the optimum state.



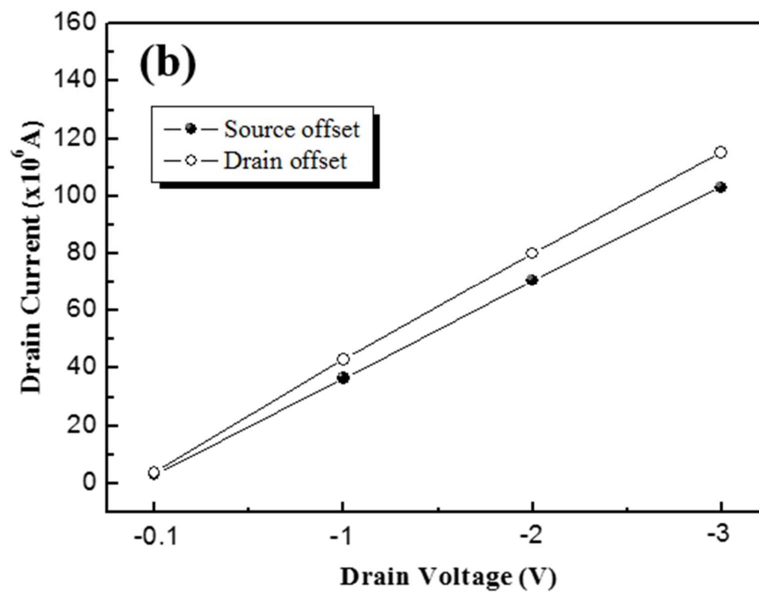


Figure 4.3 (a) Dependence values of the leakage current at high reverse gate voltage as drain voltage increases. (b) Dependence values of the maximum on current as drain voltage increases.

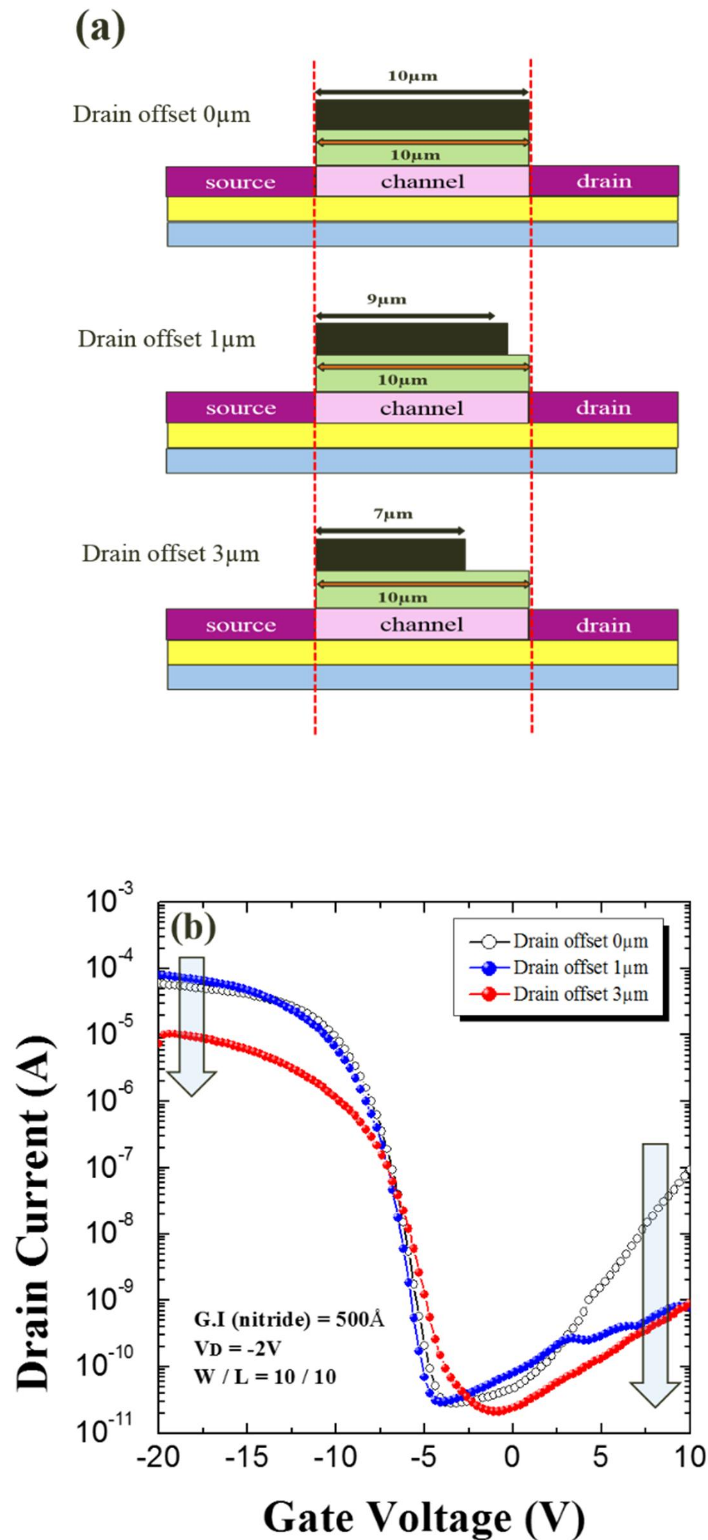


Figure 4.4 (a) Schematic structure of MILC poly-Si TFTs according to the drain offset length. (b) I_D-V_G characteristics of MILC poly-Si TFTs according to the drain offset length.

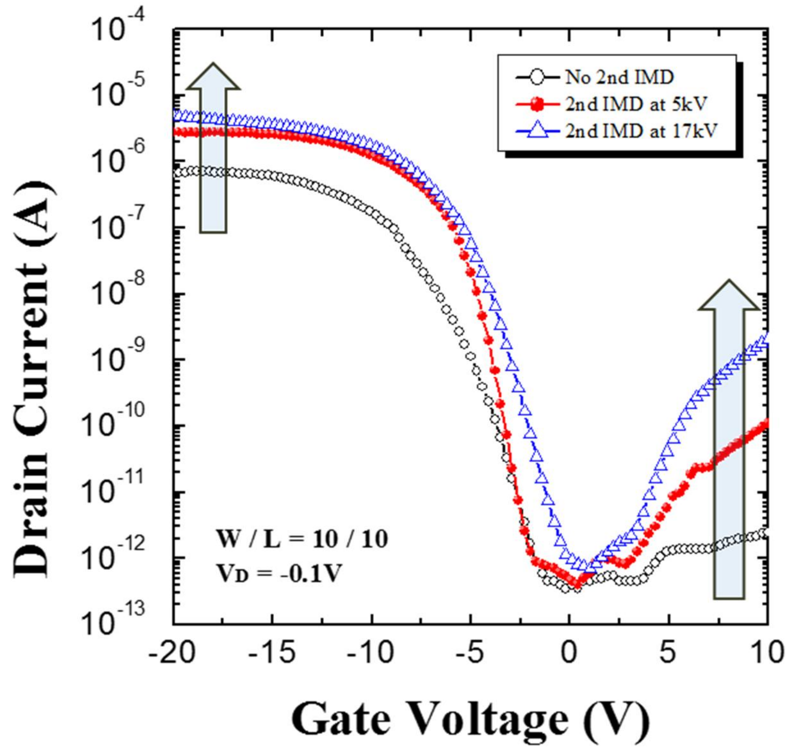


Figure 4.5 I_D-V_G characteristics of drain offset poly-Si TFTs with additional IMD.

Figure 4.5 shows the leakage current behavior of drain offset poly-Si TFTs with additional IMD. After drain offset formation process, additional IMD was performed at 5 kV for 5 min and 17 kV for 10 min respectively. The leakage current increased at high reverse V_G with additional IMD, and the higher additional doping content was, the higher $I_{pin,off}$ was. In the case of drain offset poly-Si TFTs additional IMD doped at 17 kV, $I_{pin,off}$ was very high even at low drain voltage (V_D = -0.1 V). The dropped potential between the gate and the drain may rise with additional doping to drain offset region. So, it can be considered that there is no drain offset effect if additional doping content is so high. $I_{max,on}$ also increased with additional IMD, and it has been studied that on current increases with LDD doping content [4.23]. Sheet resistance at the source and the drain region was almost same among no additional IMD, additional

IMD at 5 kV and additional IMD at 17 kV. However, sheet resistance at the drain offset region significantly decreased with additional IMD, and the higher additional doping content was, the lower sheet resistance was.

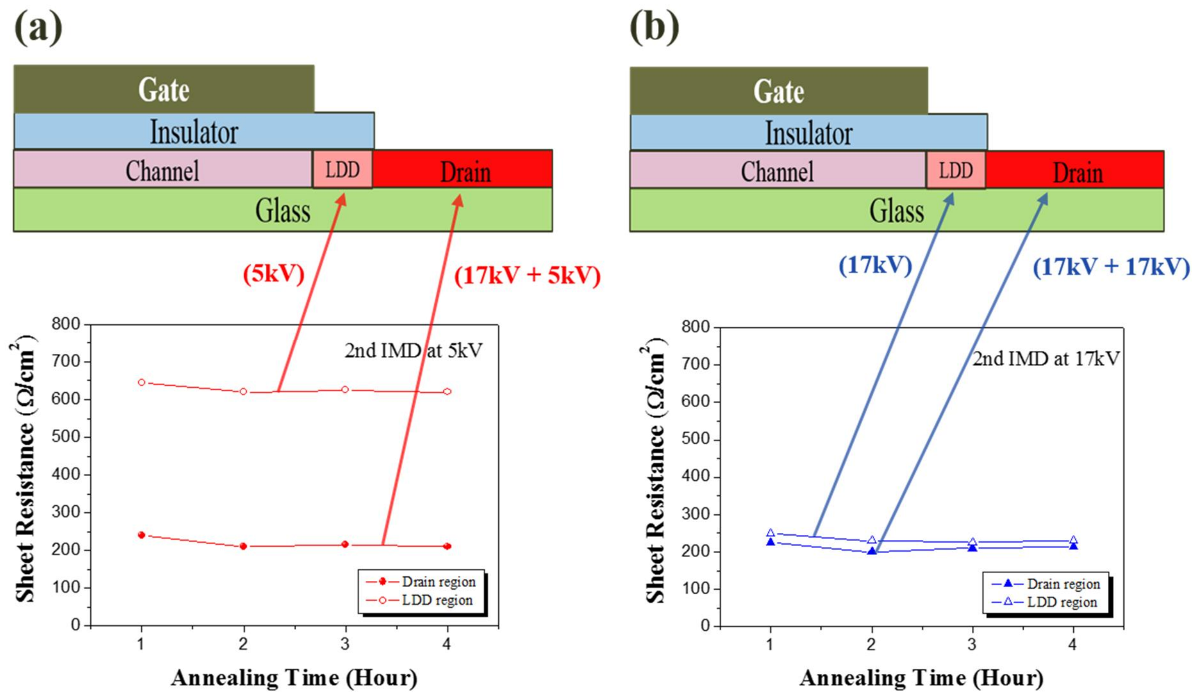


Figure 4.6 Sheet resistance of the LDD and drain region with additional IMD. (a) Additional IMD was performed at (a) 5 kV for 5 min and (b) 17 kV for 10 min.

Figure 4.6 shows the sheet resistance of the LDD and drain region with additional IMD. The difference in sheet resistance between the LDD and drain region was about 400 Ω/cm^2 when additional IMD was performed at 5 kV for 5 min as shown in Figure 4.6(a), and there was still leakage current reduction effect. However, the difference in sheet resistance between the LDD and drain region was only about 30 Ω/cm^2 when

additional IMD was performed at 17 kV for 10 min as shown in Figure 4.6(b), and there was almost no leakage current reduction effect. In the case of $I_{max,on}$, it can be considered that $I_{max,on}$ increased due to the decrease of series resistance resulting from the decrease of sheet resistance at the LDD region with increasing doping content. The measure and calculated key parameters were summarized in Table 4.1.

W/L = 10/10 (V_D = -0.1 V)	No	5 kV	17 kV
Field-effect mobility μ_{FE} (cm^2 /V-s)	16.5	57.2	95.9
Threshold voltage V_{th} (V)	-8.6	-5.9	-5.6
Subthreshold slope S.S (V/dec)	0.85	0.65	0.72
Minimum leakage current $I_{min,off}$ (x 10^{-13} A)	3.5	4.0	7.2
Leakage current at V_G = 10V $I_{pin,off}$ (x 10^{-12} A)	2.45	114	2112
Maximum on current $I_{max,on}$ (x 10^{-7} A)	6.6	26.2	50.2
Sheet resistance at source/drain region (Ω/cm^2)	240	210	200
Sheet resistance at LDD region (Ω/cm^2)	X	620	230

Table 4.1 Device characterization of drain offset poly-Si TFTs with additional IMD.

4.4 Conclusion

In this study, the gate mask was used for gate definition and drain offset formation. By using double exposure method, drain offset length can be obtained below 1 μm. The leakage current of drain offset MILC poly-Si TFTs decreased due to reduced excitation of holes trapped at the space charge region between the channel and the drain. The best electrical properties were obtained when the drain offset length was 1 μm. The leakage current phenomenon and on current were very sensitive to additional IMD to drain offset region.

Chapter 5

Boron Induced Low Temperature Polycrystalline Silicon

5.1 Introduction

In recent years, active matrix organic light emitting diode and active matrix liquid crystal display are promising technology industries. Low temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs) have advantages for use in these two display technologies, because polycrystalline silicon (poly-Si) TFTs have good electrical properties and relatively high field effect mobility [5.1-5.4]. Amorphous silicon (a-Si) can be crystallized in several ways such as solid phase crystallization [5.5, 5.6] and excimer laser annealing [5.7-5.13]. However, these two crystallization techniques have some problems such as high manufacturing cost, and surface uniformity. To solve these problems, metal-induced lateral crystallization (MILC) technique has been investigated [5.14-5.20]. MILC technique enables low-temperature

(under 570 °C) process, large-scale crystallization and good surface uniformity. Moreover, poly-Si TFTs fabricated by MILC technique exhibits high electrical performance. Therefore, MILC technique is promising process for fabricating LTPS poly-Si TFTs.

MILC growth rate, which is one of the key elements of MILC technique, has been studied by many researchers [5.21, 5.22]. As a result, the MILC growth mechanism for intrinsic a-Si seems to be well elucidated. However, the effects of dopant on the MILC growth rate and its mechanism are still unclear [5.23-5.29]. The MILC occurs in three steps as follows: (i) a-Si atomic bond breaking and absorption on the interface between a-Si and nickel silicide, (ii) vacancy hopping in nickel silicide region, (iii) Si atom rearrangement at the interface between c-Si and nickel silicide [5.23]. Moreover, Step 1 determines the growth rate of MILC.

In this study, based on the first step of the MILC mechanism, we examined the effects of boron on crystallization of a-Si. Low pressure chemical vapor deposition (LPCVD) Si and plasma enhanced chemical vapor deposition (PECVD) Si were used, and they showed different tendencies in crystallization by boron. The crystallization of boron-doped a-Si suppressed under hydrogen ambient annealing, and sheet resistance of boron-induced crystallized Si significantly increased when annealed in hydrogen ambient. To explain these phenomena, we suggested an appropriate model of boron-induced silicon crystallization.

5.2 Experiment

First, on glass substrate (Corning Eagle XG), a 200-nm-thick SiO_2 buffer layer was deposited by PECVD at 350 °C at the flow rates of SiH_4:15 sccm, N_2O: 40 sccm, and Ar: 10 sccm. The deposition pressure and radio frequency (RF) power were 300 mtorr and 20 W, respectively. Then, a 50-nm-thick intrinsic a-Si was deposited by LPCVD at 500 °C at 100 sccm flow rate of SiH_4, and the deposition pressure was 350 mtorr. The same thickness of intrinsic and boron-doped a-Si was deposited by PECVD at 350 °C at the flow rates of SiH_4: 50 sccm, and SiH_4: 50 sccm, and B_2H_6: 2 sccm; the deposition pressure and RF power were 300 mtorr and 15 W, respectively. Then, a 5-nm-thick Ni was deposited by direct current (DC) magnetron sputtering at room temperature at a DC power of 0.5 A. Boron was implanted to LPCVD Si by ion mass doping (IMD) at a flow rate of B_2H_6: 35 sccm at 150 W RF power, and secondary ion mass spectrometry (SIMS) was used to analyze the depth profile of boron in the Si film. The samples were annealed in a furnace at 560 °C in vacuum and H_2 ambient, respectively. After the annealing process, the MILC growth rate and crystallization phenomenon were observed by the optical microscopy, recorded using a digital camera attached to an Olympus BX51 microscope. A four-point probe was used to estimate the sheet resistance, and attenuated total reflectance Fourier transform infrared spectroscopy (ATR-FTIR) was used to investigate mechanism of boron effect on crystallization of a-Si.

5.3 Result and Discussion

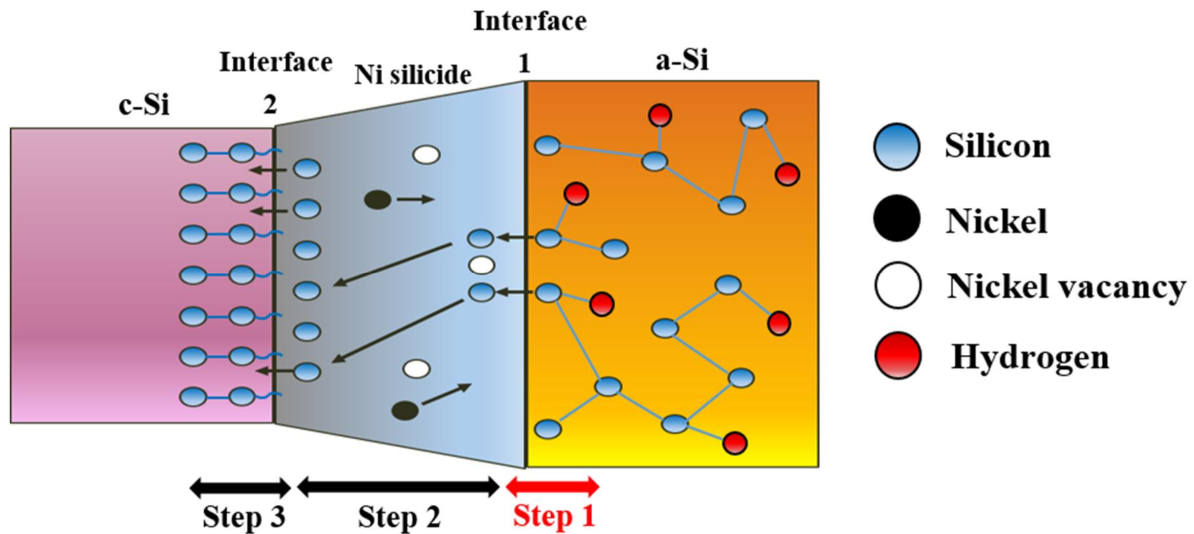


Figure 5.1 Schematic illustration of MILC growth mechanism.

a-Si can be crystallized at < 600 °C in a short time (< 2 h) by the MILC method. The MILC growth occurs by nickel silicide formed by random nucleation and proceeds in three steps as shown in Figure 5.1. First, a-Si bond breaks, and the broken Si bond is absorbed to interface 1 (Step 1). Then, atomic Si migrates to interface 2 by Ni vacancy hopping in the nickel silicide region (Step 2). And finally, atomic Si is combined with the dangling bond of poly-Si at interface 2, resulting in a new c-Si layer (Step 3). Among these MILC growth steps, MILC growth rate is mainly determined by Step 1.

Figure 5.2 shows the MILC growth rate of LPCVD intrinsic Si, PECVD intrinsic Si, and boron-doped PECVD Si. The crystalline fraction of MILC poly-Si film has

been well investigated by Raman spectroscopy in our previous study and found to be 95.24% [5.30].

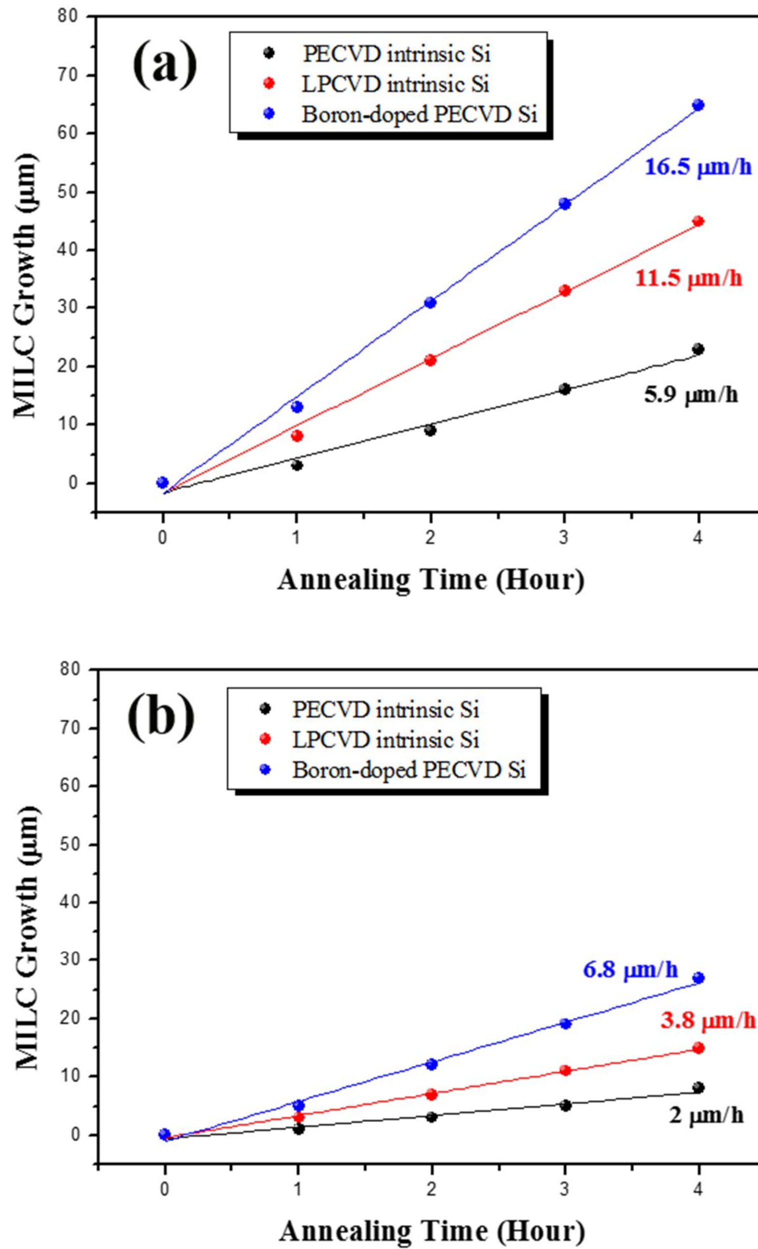


Figure 5.2 Comparison of MILC growth rate of LPCVD intrinsic Si, PECVD intrinsic Si and boron-doped PECVD Si. Annealing at 560 °C in (a) vacuum and (b) H_2 ambient.

As shown in Figure 5.2(a), the MILC growth rate of LPCVD intrinsic Si, PECVD intrinsic Si and boron-doped PECVD Si in vacuum was 11.5, 5.9 and 16.5 μm/h, respectively. The MILC growth rate of PECVD intrinsic Si was about half of that of LPCVD intrinsic Si. PECVD a-Si film typically has more hydrogen content than LPCVD a-Si film; these two types of a-Si film have different SiH bonding states [5.31, 5.32, 5.33]. So, it is considered that the difference in the MILC growth rate between LPCVD intrinsic Si and PECVD intrinsic Si probably arises because of the difference in SiH bonding states in the a-Si film. In the case of boron-doped PECVD Si, the MILC growth rate was significantly higher than those of two types of intrinsic Si. In H_2 ambient, the MILC growth rate significantly decreased, as shown in Figure 5.2(b). This result means that hydrogen suppresses the a-Si bond breaking at interface 1, which is rate controlling step for MILC growth.

Figure 5.3 shows the optical micrographs of boron-doped LPCVD Si after annealing. LPCVD intrinsic a-Si was doped with boron by IMD at 3, 10, and 17 kV for 10 min, respectively. Then, all the boron-doped LPCVD a-Si was annealed at 560 °C in vacuum for 2 h at the same time. Boron-doped LPCVD a-Si was crystallized without Ni, and the crystallization was promoted with increasing boron injection voltage. Si crystallization phenomenon was not observed in boron-doped LPCVD a-Si injected at 3 kV, and the sheet resistance was not measured as shown in Figure 5.3(a). When boron was injected at 10 kV, Si was partially crystallized, and the sheet resistance was about 460 Ω/cm^2 as shown in Figure 5.3(b). When boron was injected at 17 kV, Si was almost fully crystallized and the sheet resistance was about 350 Ω/cm^2 as shown in Figure 5.3(c). Two types of boron-doped PECVD a-Si, which

are doped with boron by IMD and PECVD, were also investigated, but these boron-doped PECVD a-Si were not crystallized without Ni.

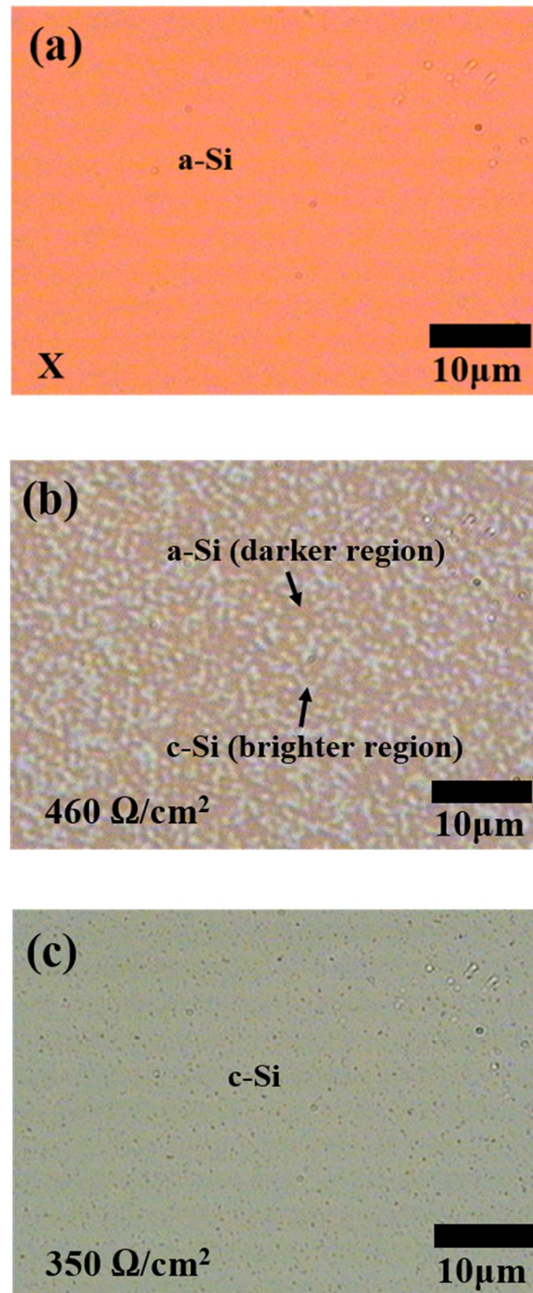


Figure 5.3 Optical micrograph of boron-doped LPCVD Si after annealing at 560 °C in vacuum for 2 h. Boron was doped by IMD at (a) 3 kV, (b) 10 kV and (c) 17 kV for 10 min, respectively.

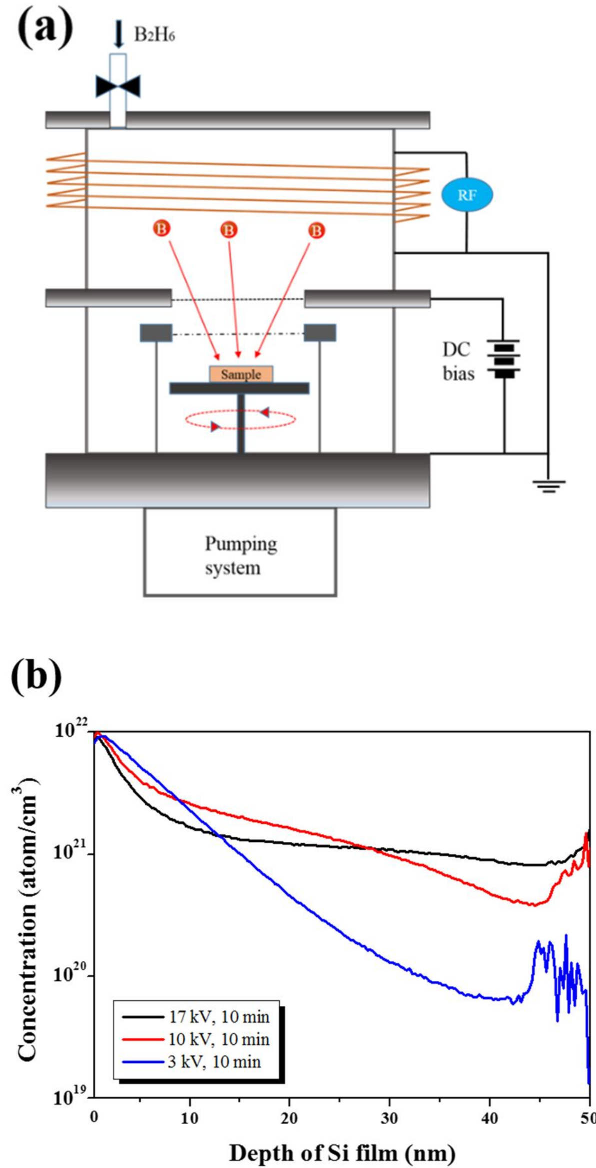


Figure 5.4 (a) Schematic diagram of ion mass doping system and (b) SIMS depth profile of boron in Si film.

Figure 5.4 (a) shows a schematic diagram of the ion mass doping system. First, B_2H_6 gas flows into the vacuum chamber at 5 x 10^{-5} torr at room temperature. Then, working pressure is maintained at 90 mtorr, and the B_2H_6 gas is decomposed by RF power. Finally, boron ions are injected into the sample for 10 min by DC power. The

SIMS depth profile of boron in Si film is shown in Figure 5.4(b). The concentration of boron decreased with increasing depth of the Si film and decreased more rapidly with decreasing injection voltage.

Figure 5.5(a) shows the Si crystallization rate according to boron injection voltage. The boron-doped LPCVD a-Si was annealed by furnace at 560 °C in vacuum. When boron was injected at 17 kV, Si crystallization rate was about 50 %/h and it was almost fully crystallized after 2 h annealing. When boron was injected at 10 kV, Si crystallization rate was about 27.5 %/h and maximum crystallinity was about 71.5%. When boron was injected at 3 kV, Si crystallization did not occur even after 5 h annealing. The sheet resistance of boron-doped LPCVD Si according to annealing time is shown in Figure 5.5(b). Comparing the sheet resistances of boron-doped LPCVD Si injected at 17 and 10 kV, the sheet resistance was slightly higher at 10 kV (460 Ω/cm^2) than at 17 kV (350 Ω/cm^2) for 2 h vacuum annealing. However, the difference in sheet resistance between boron-doped LPCVD Si injected at 17 and 10 kV decreased after additional annealing. When boron was injected at 3 kV, the sheet resistance was not obtained even after 5 h annealing. Also, boron-doped LPCVD a-Si was annealed by furnace at 560 °C in H_2 ambient. The sheet resistance of boron-doped LPCVD Si was much higher when annealed in H_2 ambient than annealed in vacuum. When boron was injected at 17 kV, the sheet resistance of boron-doped LPCVD Si annealed in H_2 ambient for 2 h was about 800 Ω/cm^2. Si crystallization did not occur in H_2 ambient when boron was injected at 10 kV, and the sheet resistance was not measured. These results show that (i) there is a critical value of boron injection voltage for Si to be crystallized by boron, (ii) boron injection voltage affects the Si

crystallization rate and maximum crystallinity and (iii) hydrogen significantly hinders the crystallization of Si by boron.

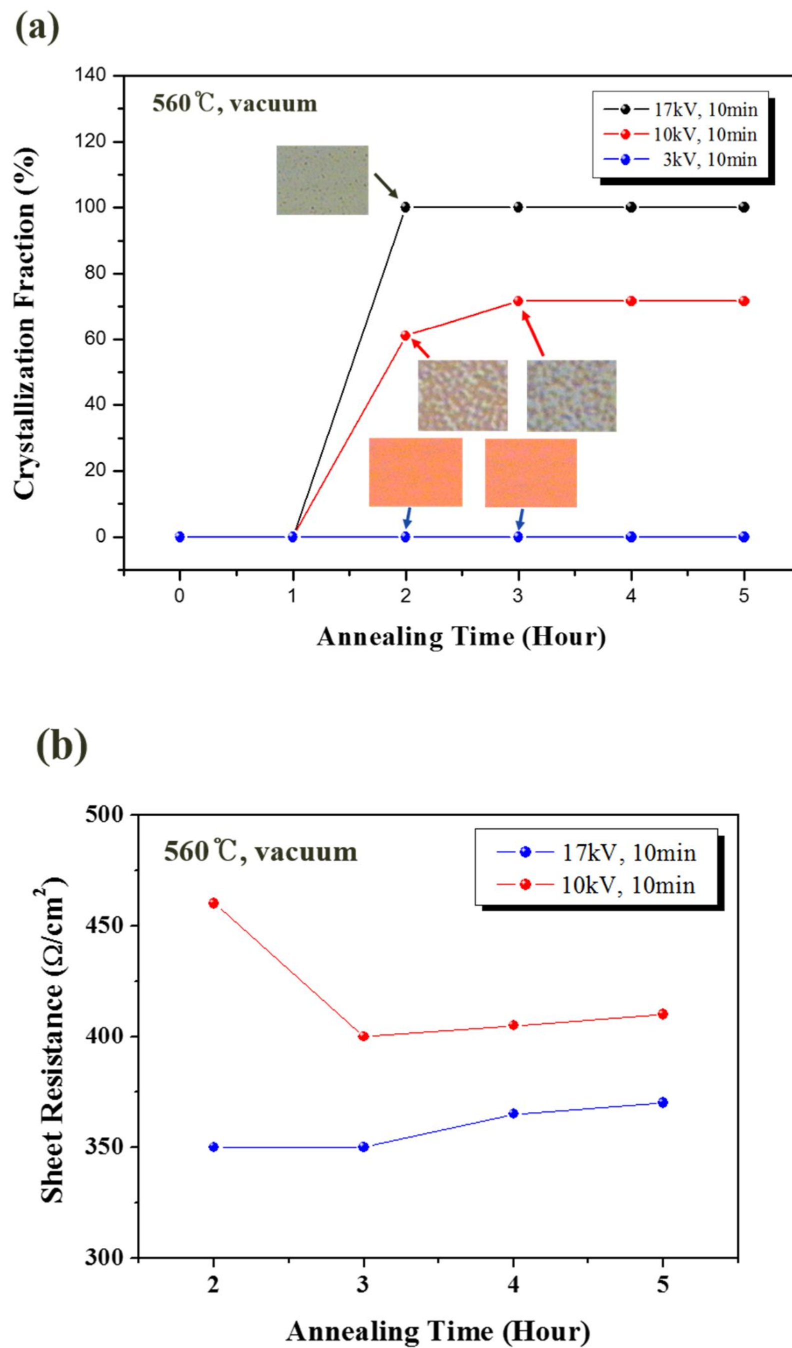


Figure 5.5 (a) Si crystallization rate according to boron injection voltage. (b) Sheet resistance of boron-doped LPCVD Si according to annealing time.

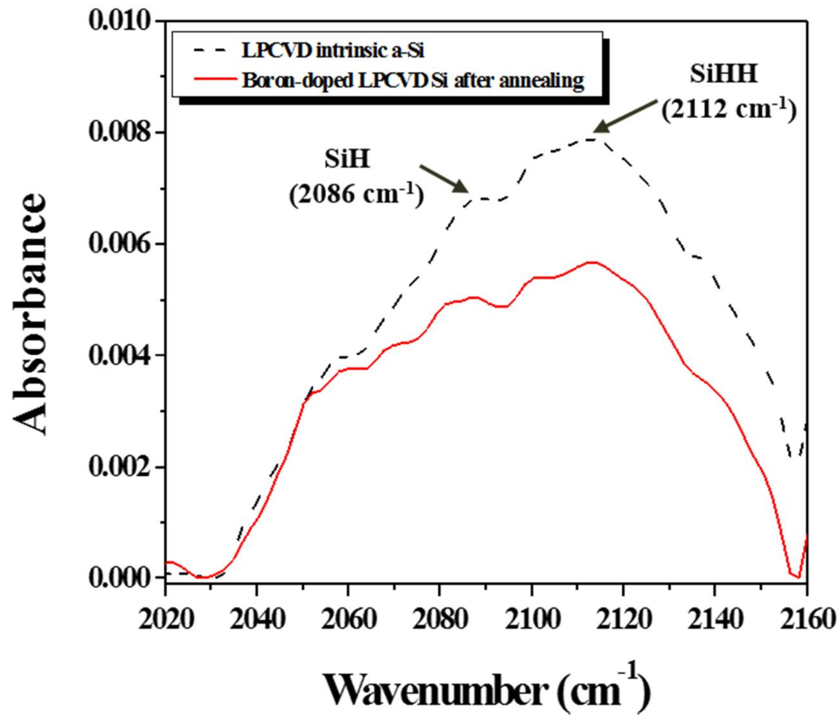


Figure 5.6 The ATR-FTIR change in the boron-doped LPCVD Si after annealing.

The ATR-FTIR change in the boron-doped LPCVD Si is presented in Figure 5.6. LPCVD intrinsic a-Si without annealing and boron-doped LPCVD Si injected at 17 kV, which is annealed at 560 °C in vacuum for 2 h, were analyzed by ATR-FTIR. Peaks of SiH (2086 cm^{-1}) and SiHH (2112 cm^{-1}) bonds [5.34] decreased after boron doping and annealing. The decrease in the intensity of these peaks can be attributed to the decomposition of SiH bond by boron. In previous studies, we reported the reaction model of SiH decomposition by boron, and SiH bond can be decomposed during annealing as follows: [5.35]

$$BH \Rightarrow B^* + H, \quad (1)$$

SiH + B* ⇨ Si* + BH, (E_a of SiH bond breaking ≈ 1.5 eV) [5.36] (2)

Si* + Si* ⇨ c-Si, (3)

Here, Si* and B* mean the activated states for chemical reactions, and E_a means the activation energy of bond breaking. The total reaction is as follows.

Si* + SiH ⇨ H + **c–Si** (Total E_a of SiH bond breaking ≈ 1.5 eV) (4)

Thus, Si crystallization can occur from SiH bond.

SiHH bond can be decomposed by boron during annealing as follows: [5.35]

BH ⇨ B* + H, (1)

SiHH + B* ⇨ SiH* + BH, (E_a of SiH bond breaking ≈ 1.5 eV) (5)

SiH* + B* ⇨ SiB + H, (E_a of SiH bond breaking ≈ 1.5 eV) (6)

and the total reaction is

SiHH + B* ⇨ **SiB** + 2H (Total E_a of SiH bond breaking ≈ 3 eV) (7)

Therefore, SiB bond can be formed from SiHH bond, but Si crystallization cannot occur.

Reaction model of boron-doped PECVD Si during MILC also has been reported [5.35]. In summary, boron triggers SiH* creation such as reaction (5) during annealing, so the reaction SiH* + Ni* ⇨ NiSi + H is promoted. As a result, MILC growth rate increases.

5.4 Conclusion

LPCVD and PECVD Si were used to investigate the effect of boron on crystallization of a-Si. Boron-doped LPCVD a-Si was crystallized without Ni, but boron-doped PECVD a-Si was not crystallized without Ni. However, the MILC growth rate of boron-doped PECVD a-Si significantly increased. Decomposition of SiH bond is one of the factors promoting Si crystallization and MILC reaction. So, it is considered that boron triggers the decomposition of SiH bonds as represented by reactions (2) and (5). The Si crystallization by boron and MILC growth suppressed when hydrogen was supplied from an external source. These results mean that hydrogen hinders the decomposition of SiH bonds. Boron-induced crystallized Si film does not contain any Ni impurities and it can be crystallized in a large area at a low temperature. So, boron-induced crystallized Si film is promising for p-type poly-Si film used in display applications and solar cells.

Chapter 6

Polycrystalline Silicon Thin-Film Transistors on Bare Glass Substrate

6.1 Introduction

Development of nanomaterials and nano processes is one of the most promising technology. There are several nanomaterials such as transition metal dichalcogenide [6.1, 6.2], metal-oxide based semiconductor [6.3], 3-5 group compound semiconductor, graphene [6.4] and silicon for thin-film transistor (TFT) which is essential component for electronic applications. In addition, nano processes such as self-assembly [6.5, 6.6, 6.7], layer-by-layer assembly [6.8], low-temperature polycrystalline silicon (LTPS) are used for fabricating TFTs. Among these nanomaterials and nano processes, LTPS TFT is widely used in electronic application industry due to its reliability and durability [6.9, 6.10].

Polycrystalline silicon (poly-Si) TFTs have a high field effect mobility (μ_{FE}) and a large current density, and as a result, poly-Si TFTs have received a considerable

amount of attention for use in active matrix liquid crystal displays and active matrix organic light emitting diode displays [6.11-6.16]. Poly-Si processing also makes it possible to integrate display circuitry directly on to the glass substrate [6.17, 6.18, 6.19]. Several methods can be used to fabricate the poly-Si TFTs, including the solid phase crystallization (SPC) [6.20, 6.21], excimer laser annealing [6.22] and metal-induced lateral crystallization (MILC). The MILC fabrication has several advantages, including a low-temperature process (under 570 °C), low-batch cost and simple processing methodology, so many studies have been carried out to further develop the MILC technique [6.23-6.33]. However, the compressive stress effect on the electrical properties of the MILC poly-Si TFTs remain unclear.

In this study, compressive stress effect on the MILC poly-Si TFTs was investigated. The strain rate of the bare glass substrate was 0.0067% and that of the compacted glass substrate was 0.0012% after crystallization and electrical activation. The MILC growth rate on the bare glass substrate was lower than that on the compacted glass substrate. The MILC poly-Si TFTs fabricated on the bare glass substrate showed low μ_{FE}, while the MILC poly-Si TFTs fabricated on the compacted glass substrate showed high μ_{FE}. The MILC poly-Si TFTs fabricated on the bare glass substrate have low uniformity of electrical properties. However, the MILC poly-Si TFTs fabricated on the compacted glass substrate have excellent uniformity of electrical properties.

6.2 Experiment

To investigate MILC growth rate on the bare and the compacted glass substrate, first, the bare glass substrate was annealed at 550 °C for 40 h in air for compaction. After glass substrate compaction process, a 200 nm-thick SiO_2 buffer layer was deposited on the bare and compacted glass substrate by plasma enhanced chemical vapor deposition (PECVD) respectively. Then, a 50 nm-thick amorphous silicon (a-Si) was deposited by LPCVD. A 50 nm-thick a-Si film was crystallized by using the MILC method. MILC was performed by furnace at 550 °C in vacuum.

To investigate electrical properties of MILC poly-TFTs fabricated on the bare and the compacted glass substrate, the bare glass substrate was annealed at 550 °C for 40 h in air for compaction. After glass substrate compaction process, a 300 nm-thick SiO_2 buffer layer was deposited on the glass substrate by PECVD. Then, a 50 nm-thick a-Si active layer was deposited by PECVD and then crystallized by using the nickel silicide seed-induced lateral crystallization (SILC) method [6.33]. Si crystallization was performed by furnace at 550 °C for 2 h in H_2 ambient. After crystallization, a 100 nm-thick silicon nitride layer was deposited as a gate insulator by PECVD, and a 200 nm-thick molybdenum-tungsten alloy was deposited as a gate electrode by direct current magnetron sputtering. Then, the gate electrode and the gate insulator were patterned using a wet etchant (H_3PO_4 + CH_3COOH + HNO_3 + H_2O) and reactive ion etching [6.34]. The source and the drain regions of the p-channel TFTs were doped with an ion mass doping system using B_2H_6 gas. After the doping process, furnace

annealing was performed at 550 °C for 2 h in H_2 ambient to electrically activate the dopants. The drain current-gate voltage (I_D-V_G) transfer curves were measured with a Keithley 2636 System.

6.3 Result and Discussion

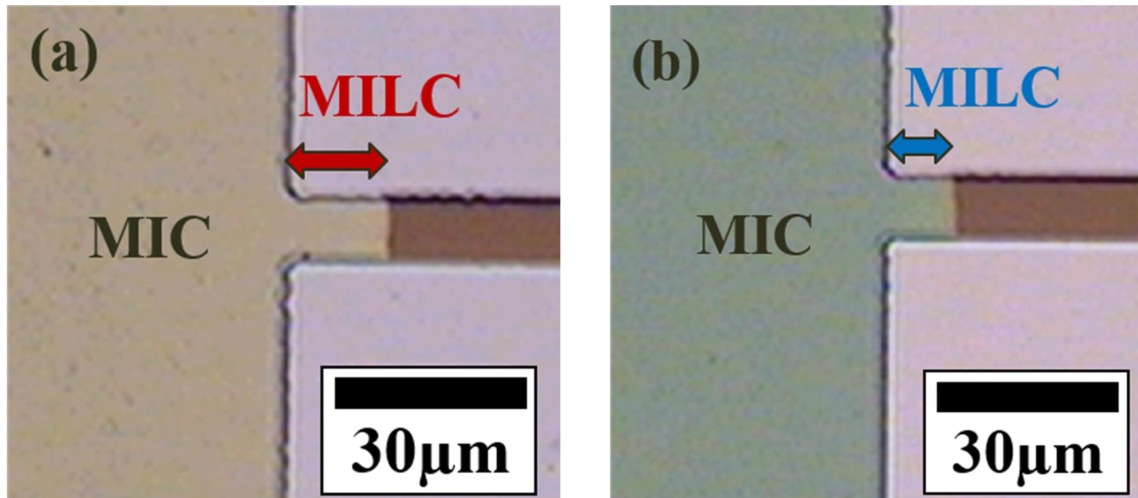


Figure 6.1 Optical micrograph of MILC growth on (a) the compacted glass and (b) the bare glass substrate.

The optical micrograph of MILC growth on the compacted glass and the bare glass substrate is presented in Figure 6.1. LPCVD intrinsic Si on the compacted glass substrate was annealed at 550 °C in vacuum for 2 h and MILC length was 16 μm as shown in Figure 6.1(a). LPCVD intrinsic Si on the bare glass substrate was annealed at 550 °C in vacuum for 2 h and MILC length was 10 μm as shown in Figure 6.1(b).

Figure 6.2(a) shows the MILC growth rate on the compacted glass and the bare glass substrate. The MILC growth rate on the compacted glass and the bare glass substrate were 10.6 μm/h and 6.7 μm/h respectively. Figure 6.2(b) shows the MILC growth rate on the compacted glass and the bare glass substrate depending on the glass

substrate location. In the case of compacted glass substrate, shrinkage of glass substrate hardly occurred and MILC growth rate was almost constant regardless of the location. On the other hand, in the case of bare glass substrate, shrinkage of glass substrate occurred more than compacted glass substrate, and the MILC growth rate decreased as the location moved from the center to the edge.

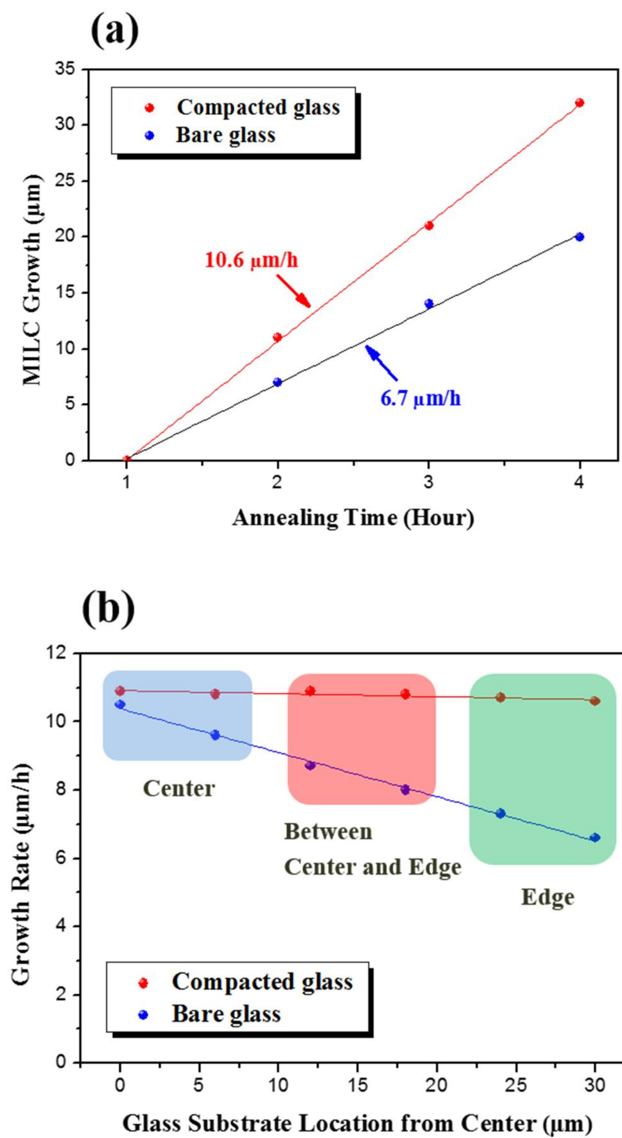


Figure 6.2 (a) MILC growth rate on the compacted and the bare glass. (b) MILC growth rate on the compacted glass and the bare glass depending on the glass substrate location.

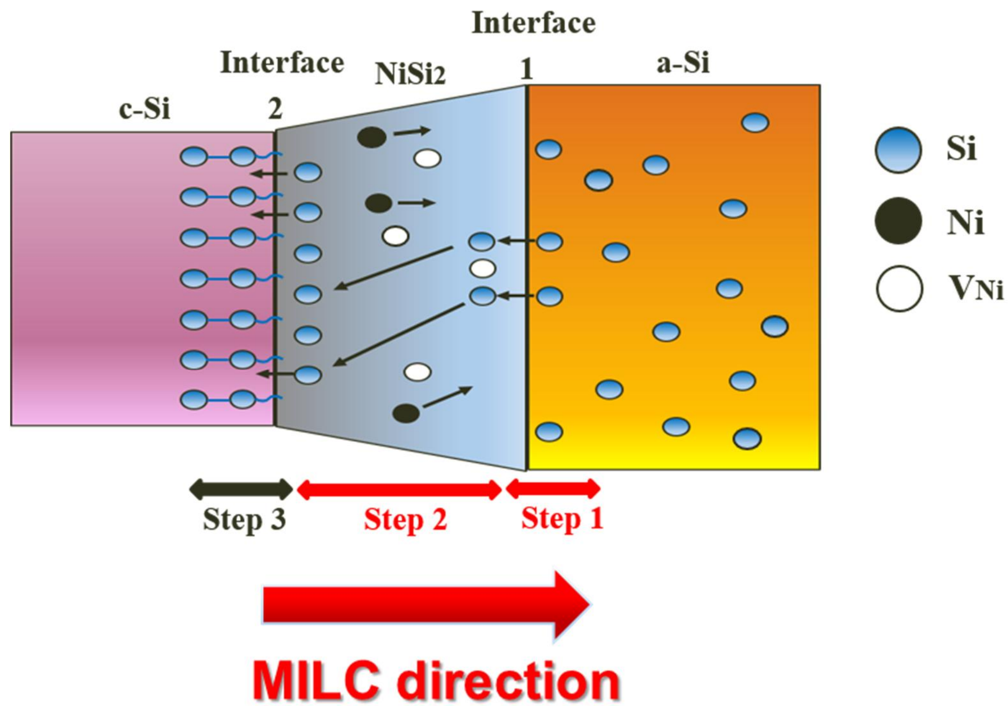


Figure 6.3 MILC reaction mechanism.

MILC reaction mechanism is shown in Figure 6.3 and MILC occurs in three steps as follows:

Step1) a-Si atomic bond breaking and absorption of Si atom at interface 1.

Step2) vacancy hopping in silicide region.

Step3) Si atom rearrangement at interface 2.

Here, the MILC growth rate is determined by step 1 and 2.

Compressive stress on glass substrate affects MILC growth. Figure 6.4 shows the MILC reaction when compressive stress is applied to the glass substrate. The compressive stress on glass substrate hinders a-Si bond breaking at a-Si region [6.35].

So, number of Si atom decreases at interface 1. Decreased Si atom hinders forming vacancy in silicide region and thereby diffusion rate of Ni atom decreased. As a result, the MILC growth rate decrease. Si film on the bare glass substrate has large compressive strain during annealing due to glass substrate shrinkage [6.36]. So, it is considered that MILC growth rate on the bare glass substrate decreased due to suppression of the a-Si bond breaking at a-Si region.

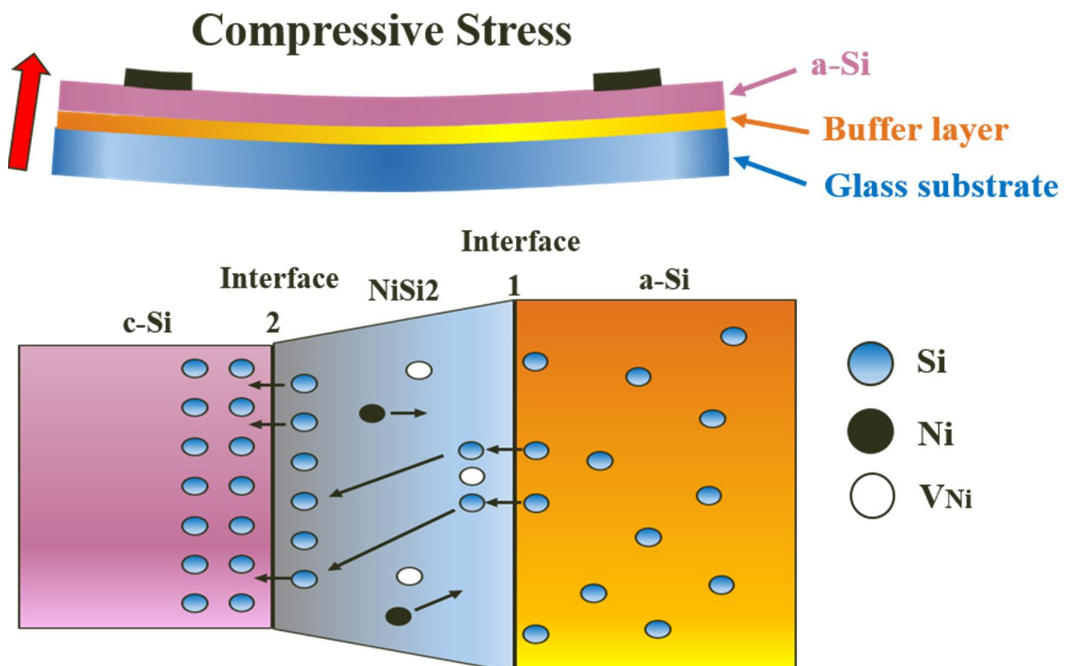


Figure 6.4 MILC reaction under compressive stress.

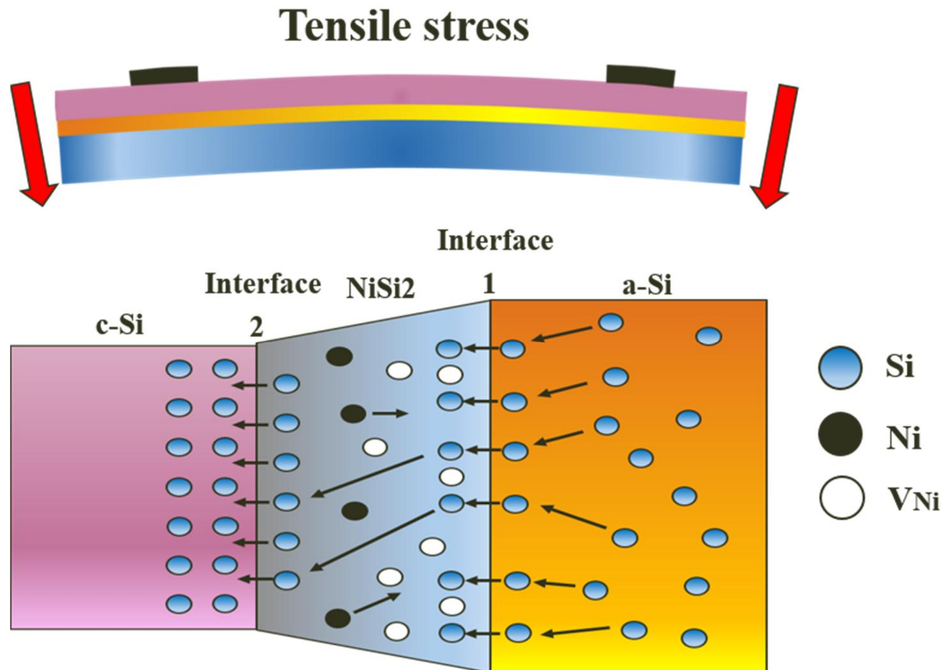


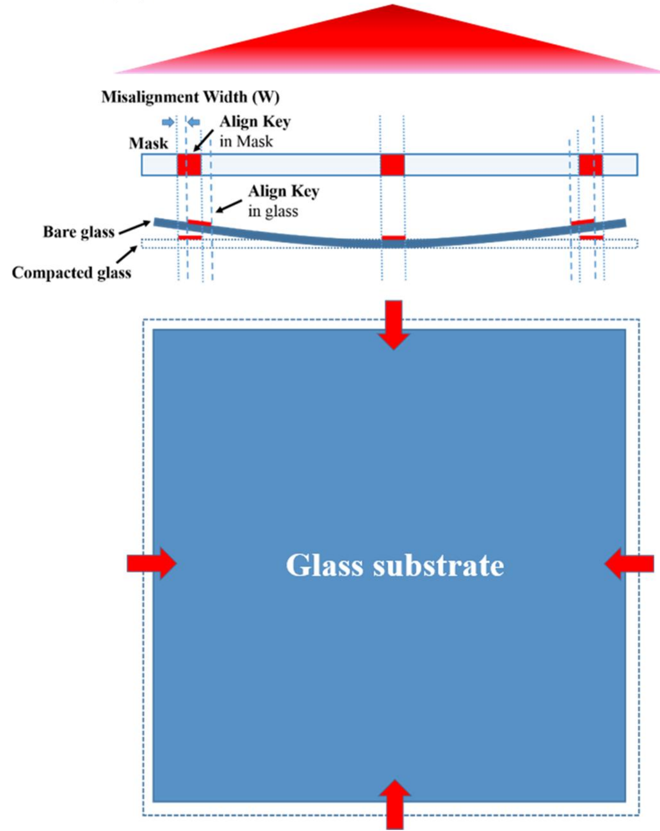
Figure 6.5 MILC reaction under tensile stress.

Figure 6.5 shows the MILC reaction when tensile stress is applied to the glass substrate. The tensile stress on glass substrate help to break a-Si bond at a-Si region [6.35]. So, number of Si atom increases at interface 1. Increased Si atom helps to form vacancy in silicide region and thereby diffusion rate of Ni atom increases. As a result, the MILC growth rate increases.

Figure 6.6(a) shows the schematic illustration of glass substrate shrinkage after annealing process, and Figure 6.6(b) shows the mask misalignment width (W) of the bare and the compacted glass substrate after crystallization and electrical activation. After annealing process, the compacted glass substrate showed 0.35 μm of W at the edges, while the bare glass substrate showed 2 μm of W at the edges. The shrinkage of glass substrate was calculated according to the ratio of Δ L (decreased length from the

center to the edge after annealing) to L_i (initial length from center to the edge before annealing).

Figure 6.7 shows the electrical properties of the p-type MILC poly-Si TFTs fabricated on the bare and compacted glass substrates (Although a-Si was crystallized by SILC method, SILC was expressed as MILC because the experimental variable in this study is not nickel silicide content. And, the SILC can be included in the MILC in that it is also crystallized through nickel silicide). The glass shrinkage of the bare glass substrate was 0.0067%, and that of the compacted glass substrate was 0.0012% after crystallization and electrical activation. The device dimension was width = length = 10 μm and the location of the device was both at the edges of the glass substrate to see the stress effects clearly. The MILC poly-Si TFTs fabricated on the bare glass substrate exhibit a μ_{FE} of 54.2 cm^2 V^{-1} S^{-1}, a minimum leakage current ($I_{min,off}$) of 1.05 x 10^{-12} A, a pinning current which is leakage current at V_G = 5 V ($I_{pin,off}$) of 2.0 x 10^{-12} A at V_D = - 0.1 V, a V_{th} of - 9 V, and a SS of 0.9 V dec^{-1}. On the other hand, the MILC poly-Si TFTs fabricated on the compacted glass substrate exhibit a μ_{FE} of 83.8 cm^2 V^{-1} S^{-1}, a $I_{min,off}$ of 2.1 x 10^{-12} A, a $I_{pin,off}$ of 2.4 x 10^{-12} A at V_D = - 0.1 V, a V_{th} of - 5.8 V, and a SS of 0.6 V dec^{-1}. The μ_{FE}, V_{th} and SS of the MILC poly-Si TFTs fabricated on the compacted glass substrate were superior to that of the MILC poly-Si TFTs fabricated on the bare glass substrate. Compressive strain that originated from the glass substrate shrinkage increases the micro-cracks and the vacancies in Si film, as a result, the μ_{FE} was degraded. Also, the V_{th} and the SS were degraded due to the interface trap density that was generated by the micro-cracks and the vacancies induced by the glass substrate shrinkage.



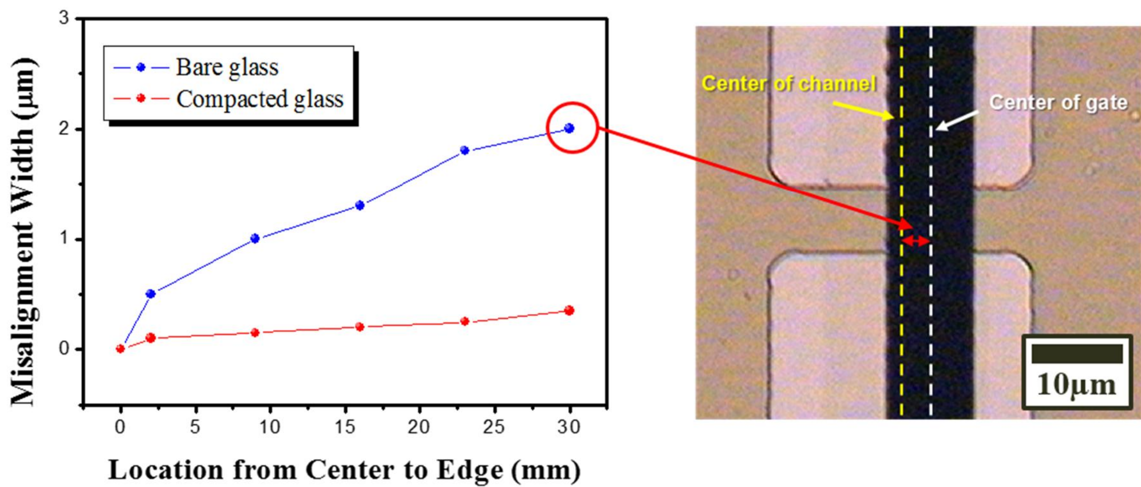


Figure 6.6 (a) Schematic illustration of glass substrate shrinkage after annealing process, (b) mask misalignment width of the bare and the compacted glass substrate after crystallization and electrical activation.

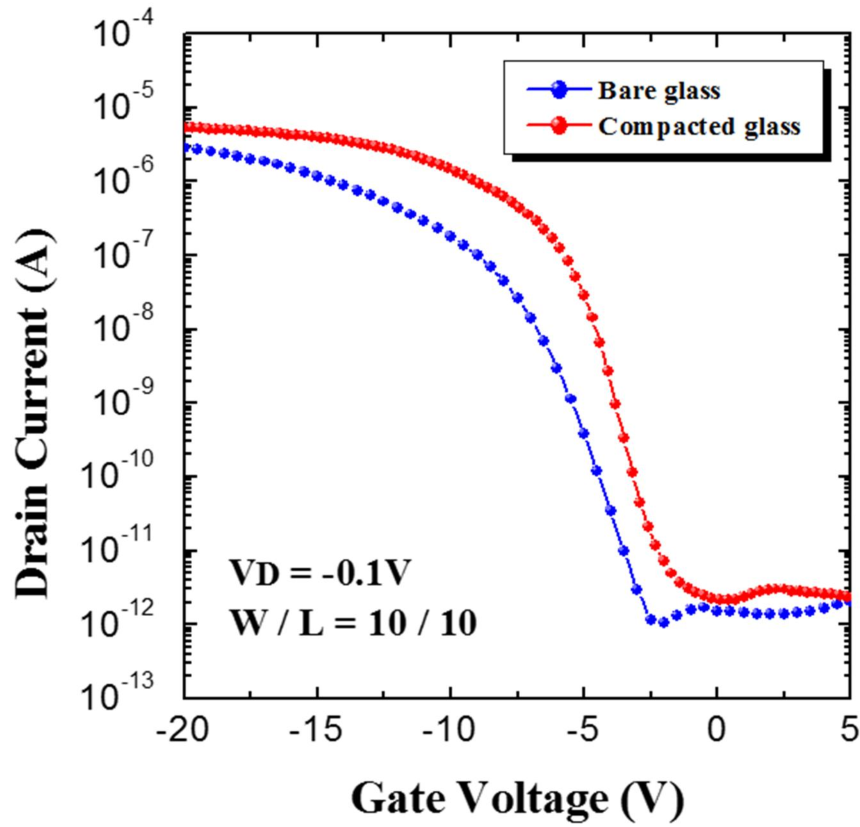


Figure 6.7 Electrical properties of p-type MILC poly-Si TFTs fabricated on the bare and the compacted glass substrate.

Figure 6.8 shows μ_{FE} of the p-type MILC poly-Si TFTs fabricated on the bare and the compacted glass substrate. The μ_{FE} of MILC poly-Si TFTs was significantly degraded on the bare glass substrate. Defects in the grain boundaries of poly-Si form potential barriers after trapping the carriers, and this potential barriers interfere with carrier transport [6.37, 6.38]. So, it is considered that compressive strain originated from the glass substrate shrinkage increased the defects in the grain boundary of poly-Si film.

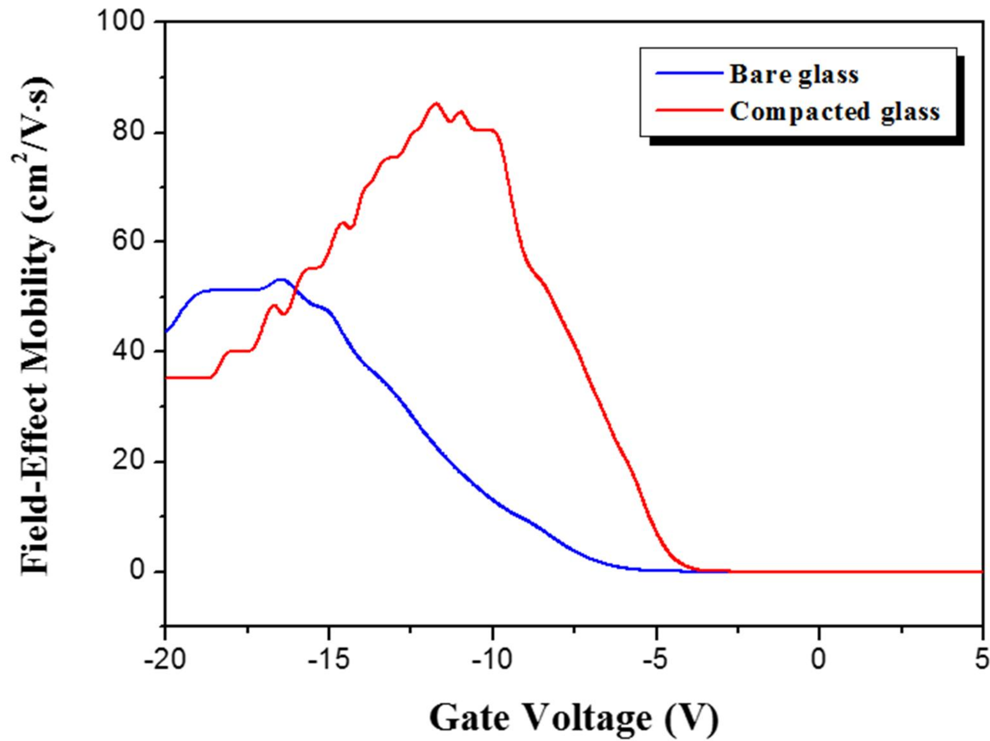


Figure 6.8 Field-effect mobility of p-type MILC poly-Si TFTs fabricated on the bare and the compacted glass substrate.

Figure 6.9 shows the electrical properties of the p-type MILC poly-Si TFTs according to location on the bare glass substrate. In the case of bare glass substrate, the shrinkage of glass substrate gradually increased from the center to the edge and it occurred up to 2.5 μm. As the shrinkage of glass substrate increased, the leakage current gradually increased. Like this, MILC poly-Si TFTs fabricated on the bare glass substrate have low uniformity of electrical properties.

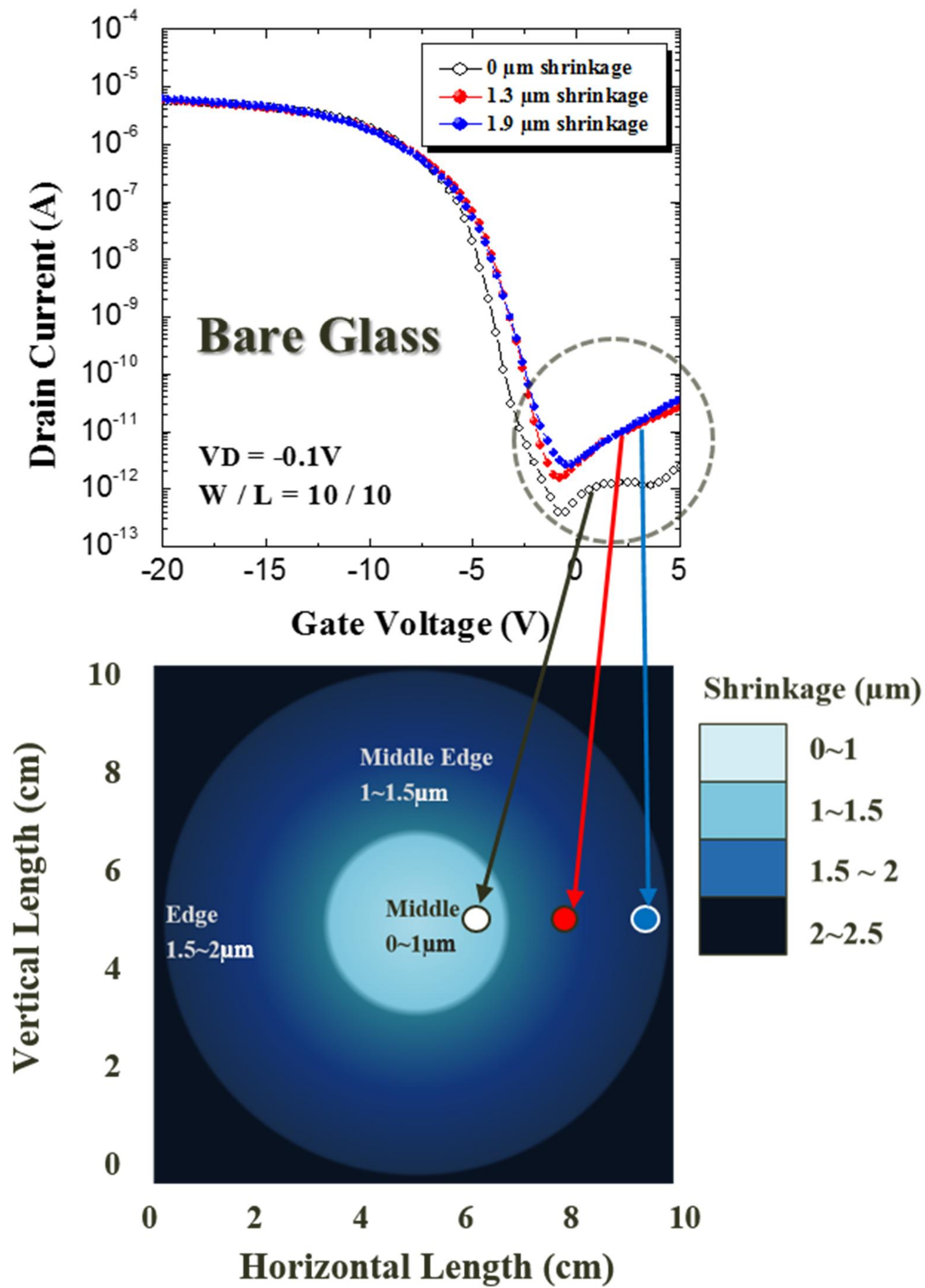


Figure 6.9 Electrical properties of the p-type MILC poly-Si TFTs according to location on the bare glass substrate.

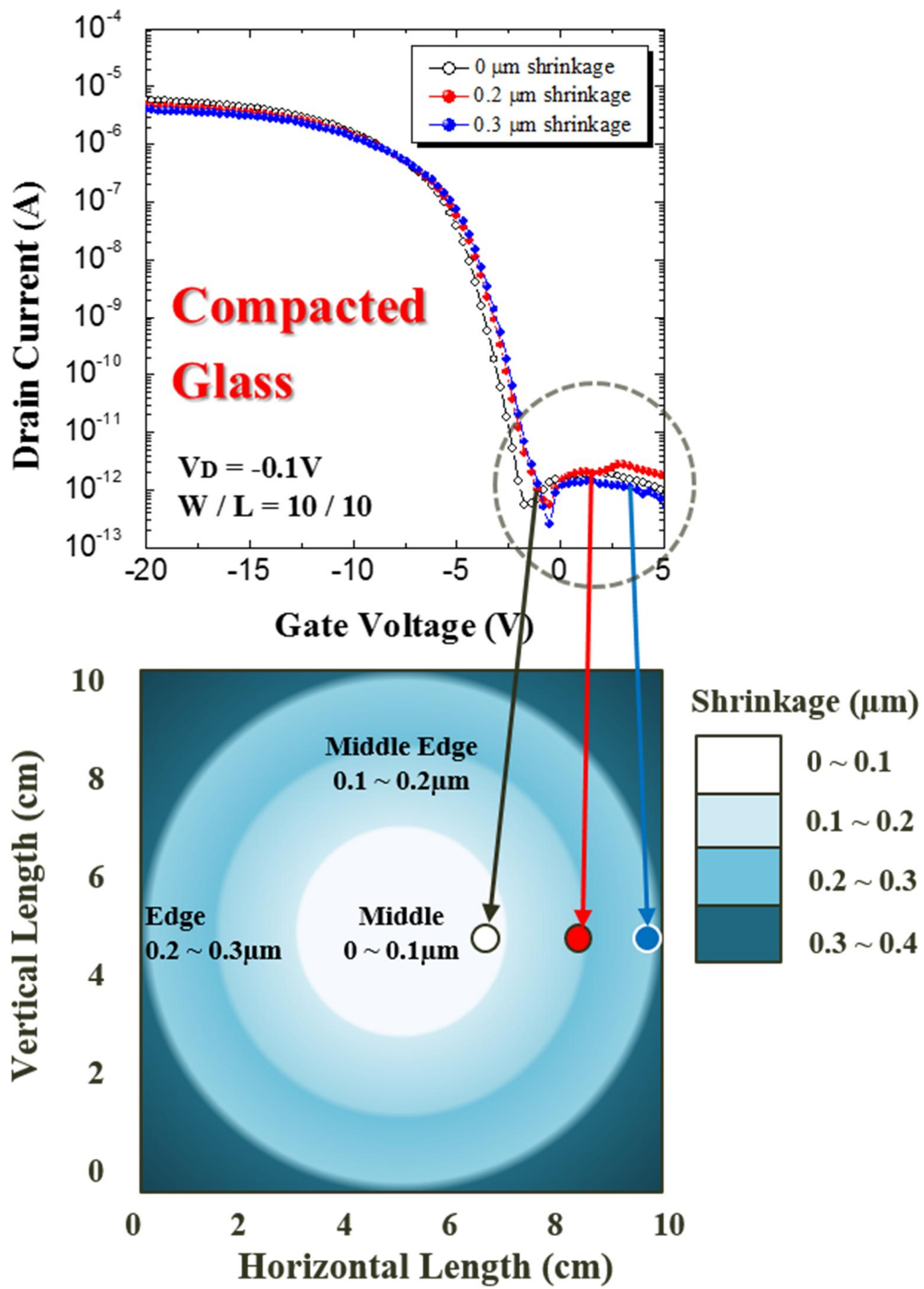


Figure 6.10 Electrical properties of the p-type MILC poly-Si TFTs according to location on the compacted glass substrate.

Figure 6.10 shows the electrical properties of the p-type MILC poly-Si TFTs according to location on the compacted glass substrate. In the case of compacted glass substrate, the shrinkage of glass substrate hardly occurred. The shrinkage of glass substrate occurred only up to 0.4 μm at the edge of the glass substrate, and there was almost no difference in leakage current according to glass substrate location. Like this, MILC poly-Si TFTs fabricated on the compacted glass substrate have excellent uniformity of electrical properties.

6.4 Conclusion

We investigated compressive stress effects on the MILC growth rate and electrical properties of MILC poly-Si TFTs. We compared MILC poly-Si TFTs fabricated on the compacted and the bare glass substrate. The MILC growth rate on the bare glass substrate was lower than that on the compacted glass substrate. The μ_{FE} of MILC poly-Si TFTs was significantly degraded on the bare glass substrate. And MILC poly-Si TFTs fabricated on the bare glass substrate showed bad uniformity of electrical properties. This degradation of electrical properties of MILC poly-Si TFTs fabricated on the bare glass substrate is due to micro-cracks and voids traps that were generated under the compressive strain which is originated from the glass substrate shrinkage. On the other hand, MILC poly-Si TFTs fabricated on the compacted glass substrate showed excellent electrical properties and uniformity of electrical properties. These results can be attributed to the absence of glass substrate shrinkage due to glass substrate compaction. Therefore, the glass substrate compaction process is beneficial for the fabrication of MILC poly-Si devices.

Chapter 7

Conclusion

Nickel silicide trapped in the grain boundary of polycrystalline silicon (poly-Si) increases the leakage current of poly-Si thin-film transistors (TFTs). To reduce the nickel silicide trapped in the grain boundary of poly-Si, the gettering method was investigated by using amorphous silicon (a-Si) layer as getter layer. The nickel silicides in the poly-Si thin film crystallized by metal induced crystallization (MIC) and nickel silicide seed induced lateral crystallization (SILC) were efficiently reduced by gettering. As a result, the leakage current of MIC and SILC poly-Si TFTs drastically decreased. The nickel silicide and leakage current of MIC poly-Si TFTs was continuously reduced as gettering cycles increased. This phenomenon could be explained by the behavior of nickel silicides located in the shallow and the deep level trap state.

The leakage current of metal induced lateral crystallized (MILC) poly-Si TFT occurs due to electric field between gate and drain electrode. The high electrical field between gate and drain electrode causes trap assisted field emission. By applying

drain offset structure, trap assisted field emission can be suppressed. The leakage current of drain offset MILC poly-Si TFTs fabricated by double exposure method decreased. And the best drain current-gate voltage transfer curve was obtained when the drain offset length was 1μm.

Low pressure chemical vapor deposition (LPCVD) Si and plasma enhanced chemical vapor deposition (PECVD) Si were used to investigate the effect of boron on the crystallization of a-Si. Boron-doped LPCVD a-Si was crystallized without Ni but boron-doped PECVD a-Si was not crystallized without Ni. However, the MILC growth rate of boron-doped PECVD a-Si significantly increased. In order for a-Si to be crystallized or MILC reaction to proceed, SiH bonds should first be decomposed. So, it is considered that boron triggers the decomposition of SiH bonds. The crystallization of a-Si and MILC growth suppressed when hydrogen was supplied from an external source. These results mean that hydrogen hinders the decomposition of SiH bonds. By injecting boron into LPCVD a-Si film, it is possible to manufacture a large area p-type poly-Si film without Ni impurities in a short time at a low temperature. So, boron-induced crystallized Si film is promising for p-type poly-Si film used in display applications and solar cells.

We investigated the MILC growth rate and electrical properties of MILC poly-Si TFTs on the bare glass and the compacted glass substrate. During the MILC process, compressive stress caused by glass substrate shrinkage was induced to Si film deposited on the bare glass substrate. Compressive stress suppresses the Si bond breaking at the front of the $NiSi_2$/a-Si interface, which is the rate controlling step for

the MILC growth. As a result, MILC growth rate decreased on the bare glass substrate. Electrical properties of MILC poly-Si TFTs fabricated on the bare glass substrate degraded due to micro-cracks and voids traps that were generated under the compressive strain. To suppress glass substrate shrinkage, the bare glass substrate was annealed at 550 °C for 40 h in air before MILC process. And this process is called glass compaction process. By performing glass compaction process, glass substrate shrinkage drastically decreased. As a result, MILC growth rate increased and electrical properties of MILC poly-Si TFTs were efficiently improved.

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국문 초록

금속유도 측면결정화 박막 트랜지스터의 전기적 성능 향상을 위한 고귀한 방법

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금속유도 결정화에 의해 제작된 저온 다결정 실리콘 박막 트랜지스터는 액티브 매트릭스 평판 디스플레이에 사용하기에 매력적이다. 그러나, 금속유도 결정화에 의해 제작된 실리콘 박막의 결정 입계에는 니켈 실리사이드가 존재하며, 이러한 니켈 실리사이드는 큰 누설 전류를 유발한다. 본 연구에서는 게터층으로 비정질 실리콘, 에치 스톱층으로 실리콘 산화막을 사용하여 니켈 불순물을 제거하는 게터링 방법을

이용하여 금속유도 결정화 다결정 실리콘 박막 트랜지스터의 누설 전류를 감소시켰다. 금속유도 결정화 다결정 실리콘 박막의 니켈 트랩 상태 밀도가 게터링에 의해 감소하였으며, 그 결과 금속유도 결정화 다결정 실리콘 박막 트랜지스터의 누설 전류가 감소하였다. 또한, 게터링 횟수가 증가 할수록 금속유도 결정화 다결정 실리콘 박막 트랜지스터의 누설 전류가 점차적으로 감소 하였다. 이러한 게터링에 의한 누설전류 감소 효과를 설명하기 위해 적절한 모델을 제시하였다. 또한 게터링을 니켈 실리사이드 유도 측면결정화 다결정 실리콘 박막 트랜지스터에 적용하여 누설 전류를 더욱 감소 시켰다.

금속유도 측면결정화에 의해 제작된 다결정 실리콘 박막 트랜지스터는 대규모 액티브 매트릭스 평판 디스플레이의 스위칭 및 구동 소자로서 매력적인 장치 중 하나이다. 하지만 금속유도 측면결정화에 의해 제작된 다결정 실리콘 박막 트랜지스터는 누설전류가 크다는 단점을 가지고 있다. 금속유도 측면결정화 다결정 실리콘 박막 트랜지스터의 누설 전류는 게이트 절연체와 다결정 실리콘 활성층 사이의 계면에서 니켈 불순물에 기인한 하전된 트랩 상태에 의해 유도되고, 트랩 상태는 게이트와 드레인 사이의 높은 전계에 의해 활성화된다. 본 연구에서는 2 중 노광 방법으로 드레인 오프셋 영역을 형성하여 금속유도 측면결정화 다결정 실리콘 박막 트랜지스터의 누설전류를 감소시켰다.

본 연구에서는 boron 이 금속유도 측면결정화 성장 속도에 미치는 영향을 토대로, boron 이 비정질 실리콘의 결정화에 미치는 영향에 대하여 연구하였다. 저압 화학 기상 증착법 및 플라즈마 강화 화학 기상 증착법으로 증착된 비정질 실리콘은 boron 에 의한 결정화에 있어 상이한 결과를 보였다. 저압 화학 기상 증착법으로 증착된 비정질 실리콘에 boron 을 도핑 하였을 경우, 니켈을 증착하지 않아도 560℃에서 2 시간 내에 실리콘이 결정화 되었지만 플라즈마 강화 화학 기상 증착법으로 증착된 비정질 실리콘은 boron 이 도핑 되어도 니켈 없이는 결정화가 되지 않았다. 하지만 플라즈마 강화 화학 기상 증착법으로 증착된 비정질 실리콘에 boron 을 도핑 할 경우 금속유도 측면결정화 성장 속도가 상당히 증가하였다. 수소 분위기에서 열처리 할 경우 금속유도 측면결정화 성장 속도가 감소하였으며, boron 에 의해 결정화된 실리콘의 면저항이 증가 하였다. 본 연구에서는 이러한 원인을 규명하기 위해 boron 에 의한 실리콘 결정화의 적절한 모델을 제시하였다.

일반 유리기판과 열처리된 유리기판 위에 금속유도 측면결정화 다결정 실리콘 박막 트랜지스터를 제작하여 압축응력이 금속유도 측면결정화 성장 속도 및 전기적 특성에 미치는 영향을 연구하였다. 유리기판의 수축을 억제하기 위해 사전에 550℃에서 40 시간동안 유리기판을 열처리하였다. 결정화 및 전기적 활성화 후 일반 유리기판의 변형률은 0.0067% 이었고 열처리된 유리기판의 변형률은 0.0012% 이었다. 일반 유리기판 위에서의

금속유도 측면결정화 성장 속도는 열처리된 유리기판 위에서의 금속유도 측면결정화 성장 속도 보다 느렸다. 유리기판의 수축으로 인한 압축변형은 다결정 실리콘 박막에 마이크로 크랙 및 공극을 증가 시킨 것으로 생각되며, 그 결과 일반 유리기판 위에 제작된 다결정 실리콘 박막 트랜지스터의 field effect mobility, threshold voltage, subthreshold slope 이 악화된 것으로 볼 수 있다. 그리고 일반 유리기판 위에 제작된 다결정 실리콘 박막 트랜지스터는 소자 위치에 따른 불균일한 전기적 특성을 보였다. 반면에, 열처리된 유리기판 위에 제작된 다결정 실리콘 박막 트랜지스터는 뛰어난 전기적 특성과 소자 위치에 따른 균일한 전기적 특성을 보였다.

주요어 : 금속유도 결정화, 박막 트랜지스터, 게터링, 누설전류, 금속유도 측면결정화, 니켈 실리사이드 유도 측면결정화, 2 중 노광 방법, 드레인 오프셋, boron 유도 실리콘 결정화, 면저항, 수소 열처리, 압축응력, 일반 유리기판, 열처리된 유리기판.

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