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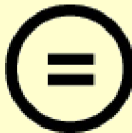

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공학박사 학위논문

Epitaxial Growth of III-Nitride on Nano-Patterned Substrate for Light-Emitting Diode

발광다이오드 응용을 위한 나노패턴된 기판 상의 3족 질화물 에피성장 연구

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이 논문을 공학박사 학위논문으로 제출함

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Abstract

Epitaxial Growth of III-Nitride on Nano-Patterned Substrate for Light-Emitting Diode

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Group III-nitride has been regarded as one of the most promising material for optoelectronic device applications such as light-emitting diode (LED) and laser diode (LD) over past few decades. In order to realize highly efficient and reliable optoelectronic devices, high quality III-nitride epitaxial layers are required. A major problem in the epitaxial growth of III-nitride is that the use of native substrates is still limited due to lack of commercially available substrates. Therefore, III-nitride epitaxial layers are grown on foreign substrates such as sapphire and Si. However, large lattice mismatch and thermal mismatch between the III-nitride epitaxial layers and the substrates lead to several problems such as high-density dislocations, low light extraction efficiency (LEE), and residual film stress, thus hinder the realization of highly efficient III-nitride optoelectronic devices. Therefore, to obtain high quality III-nitride epitaxial layers that are less defective, less

strained, and more effective to enhance the LEE is very important for various III-nitride LED applications. In this study, nano-patterned substrates have been proposed to obtain the high quality III-nitride layers for important epitaxial structures in the III-nitride LED applications such as GaN on Si substrate, AlN on sapphire substrate, and GaN on sapphire substrate. The epitaxial growth of III-nitrides on the nano-patterned substrates was investigated by metal-organic chemical vapor deposition.

Firstly, for the case of GaN on Si substrate, nanoheteroepitaxy (NHE) of GaN on the AlN/Si(111) nanorod structure was investigated. Silica nanosphere lithography was employed to fabricate the periodic hexagonal nanorod array with a narrow gap of 30 nm between the nanorods. Fully coalesced GaN film was obtained over the nanorod structure and its threading dislocation density (TDD) was found to decrease down to half, compared to that of GaN grown on the planar AlN/Si(111) substrate. Transmission electron microscopy (TEM) revealed that threading dislocation (TD) bending and TD termination by stacking faults occurred near the interface between GaN and AlN/Si(111) nanorods, contributing to the TDD reduction. Moreover, the 70% relaxation of the tensile stress of the NHE GaN was confirmed by Raman and PL measurements compared to GaN on the planar AlN/Si(111) substrate. These results suggested that NHE on the AlN/Si(111) nanorods fabricated by nanosphere lithography is a promising technique to obtain continuous GaN layers with the improved crystalline quality and the reduced residual stress.

Secondly, a nano-patterned AlN/sapphire substrate was developed to improve the performance of deep ultraviolet (DUV) LEDs, for the case of AlN on sapphire substrate. We demonstrated AlGaN-based DUV LEDs with

periodic air-voids-incorporated nanoscale patterns enabled by nanosphere lithography and epitaxial lateral overgrowth (ELO). The nanoscale ELO on the nano-patterned substrate improved the crystal quality of overgrown epitaxial layers at relatively low growth temperature of 1050 ºC and at small coalescence thickness. The air voids formed in the AlN epitaxial layer effectively relaxed the tensile stress during growth, so that crack-free DUV LED epitaxial layers were obtained on 4-in. sapphire substrate. In addition, the periodically embedded air-void nanostructure enhanced the LEE of DUV LEDs by breaking the total internal reflection that is particularly severe for the predominant anisotropic emission in AlGaN-based DUV LEDs. The light output power of the DUV LEDs on the nano-patterned substrate was enhanced by 67% at an injection current of 20 mA compared to that of the reference DUV LEDs. We attribute such a remarkable enhancement to the formation of embedded periodic air voids which cause simultaneous improvements in the crystal quality of epitaxial layers by ELO and LEE enabled by breaking the predominant in-plane guided propagation of DUV photons.

Lastly, we proposed the ELO of GaN using the nano-cavity patterned sapphire substrate (NCPSS), which has hexagonally non-close-packed nano-cavity patterns on the sapphire substrates, to grow high quality GaN on sapphire substrate. The fabrication of the NCPSS was enabled by polystyrene coating followed by deposition of alumina and thermal annealing. The coalescence of GaN on the NCPSS was achieved by the formation of relatively large GaN islands and enhanced ELO of the GaN islands over several nano-cavity patterns. The TDD was significantly reduced from 2.4×10^{8} cm^{-2} to 6.9×10^{7} cm^{-2} by using the NCPSS. Dislocation behaviors that

contribute to the reduction of TDD of the GaN layer were observed by TEM. Raman spectroscopy revealed that the compressive stress in the GaN layer was reduced by 21% due to the embedded nano-cavities. In addition, the diffuse reflectance of GaN on the NCPSS was enhanced by 54% ~ 62%, which is attributed to the increased probability of light extraction through effective light scattering by nano-cavities.

Key Words:
Epitxial growth, III-nitride, Nano-patterned substrate, Light-emitting diode, Metal-organic chemical vapor deposition, Stress, Light extraction, Void

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Chapter 1. Introduction

1.1 III-nitride based devices

1.1.1 General properties of III-nitride materials

Group III-nitrides including gallium nitride (GaN), aluminum nitride (AlN), indium nitride (InN), and their alloys have been regarded as one of the most promising materials for optoelectronic device applications such as laser diode (LD) and light-emitting diode (LED) and electronic device applications over past few decades. The III-nitrides and their alloys form continuous and direct bandgaps ranging from 6.2 eV (AlN) to 0.7 eV (InN), so that the III-nitrides enable the fabrication of optoelectronic devices whose emission wavelengths include the whole visible region and extend to the ultraviolet (UV) and infrared (IR) region as shown in Fig. 1.1.[1,2] In addition to the excellent optical properties, III-nitrides also exhibit good thermal stability at high temperature, high mechanical strength, large thermal conductivity, and good chemical stability. III-nitrides commonly have wurtzite crystal structure, with the spacing group of $P6_3mc$.[3] The wurtzite structure is a member of the hexagonal crystal system, thus, has a hexagonal unit cell and two lattice constants a and c, as shown in Fig. 1.2. General properties of III-nitrides are summarized in Table 1.1. Since the III-nitrides have excellent characteristics, III-nitrides have been widely used not only in optoelectronic devices such as LD, LED, solar cell, and photodetector but also in electronic devices, for example, high electron mobility transistor (HEMT).[4]

1.1.2 III-nitride based LEDs

The LED structure consists of a stack of epitaxial layers including p-type and n-type semiconductors, forming a p-n junction. A schematic of GaN-based blue LED structure is shown in Fig. 1.3.[5] The n-type nitride material is doped with impurities which contribute free electrons and the p-type nitride material is doped with impurities which create the deficiency of valence electrons (holes). When a forward voltage is applied to the LED, the free electron and the hole recombine radiatively, thus photon is emitted from the nitride semiconductors. For III-nitrides, Si and Mg are used as dopants of n-type semiconductor and p-type semiconductor, respectively.

The III-nitride based LEDs has attracted much attention and extensively investigated as the next generation light sources. The primary focus of III-nitride based LEDs has been the development of GaN-based visible LEDs for application of solid-state lighting. GaN-based visible LEDs are candidates which replace the conventional light sources including incandescent lamps and fluorescent lamps, taking advantages in high efficiency, compactness, and non-toxicity. Although GaN-based visible LEDs have already been commercialized via significant technology advancement, the efficiency and the cost reduction still need to be improved further. In addition, recently, AlGaN-based deep ultraviolet (DUV) LEDs are of great interest for applications such as sterilization, water purification, and chemi/bio-sensing.[6] However, the efficiency of AlGaN-based DUV LEDs is still much lower than that of GaN-based visible LEDs.[7,8]

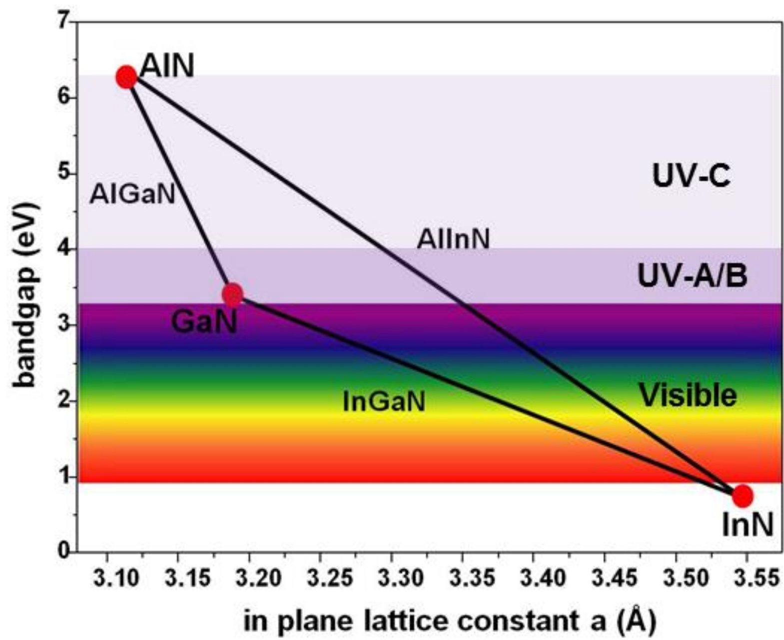

Figure 1.1. Bandgap of III-nitrides and versus lattice constant

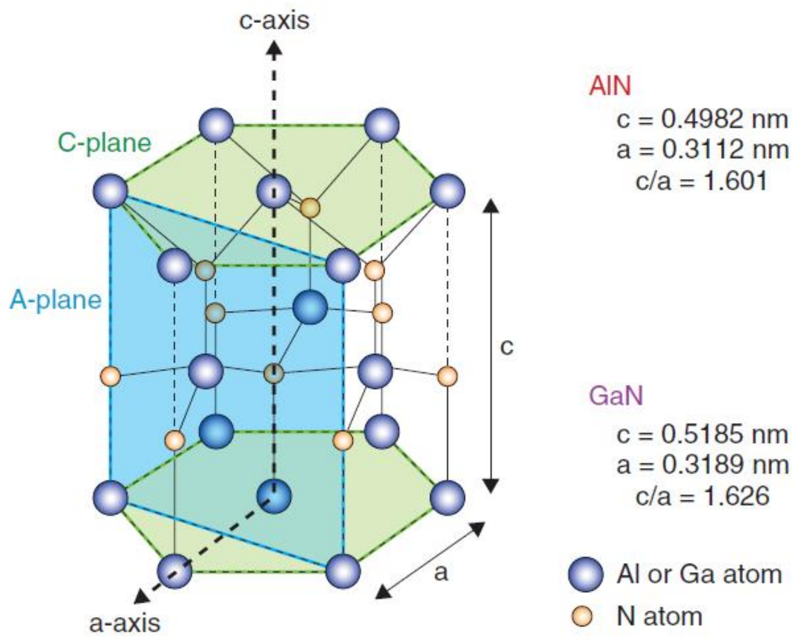

Figure 1.2. Crystal structure of wurtzite AlN and GaN

Table 1.1. General properties of III-nitrides

Properties	**GaN**	**AlN**	**InN**
Bandgap energy (eV at RT)	3.39	6.2	0.7
Lattice constant (Å)	a=3.189 c=5.185	a=3.112 c=4.982	a=3.548 c=5.760
Thermal expansion coefficient (10^{-6}/K)	da/a =5.59 dc/c =3.17	da/a =5.27 dc/c =4.15	
Thermal conductivity (W/mK)	130	200	
Index of refraction	2.4	2.15	2.9
Dielectric constant (ε_0)	9.5	8.5	
Electron effective mass (m_o)	0.20		0.11
Melting point (℃)	>2300	>2800	>1200

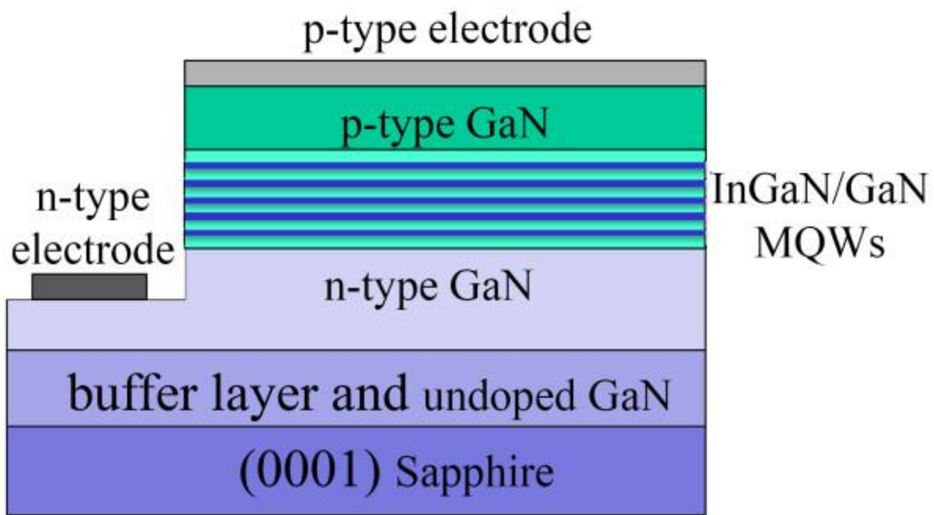

Figure 1.3. Schematic structure of typical GaN-based blue LEDs.[5]

1.2 Epitaxial growth of III-nitrides

The term of epitaxy, epitaxial growth, originates from the two ancient Greek words, επι (epi, placed or resting upon) and ταξιξ (taxis, arrangement). Thus, epitaxy means the growth of a single crystalline film on top of a crystalline substrate.[9] The epitaxial growth has played important rules of the formation of thin films in the thin-film device technology because it has been desired that the deposited thin films are single crystalline for most technology applications. The substrate serves as a seed crystal and the the crystal structure of the deposited film follows the crystal structure of the substrate if the thin film is epitaxially grown. If not, it is not an epitaxial growth. There are several types of epitaxy as follows: homoepitaxy; heteroepitaxy of strained thin film; and heteroepitaxy of strain-relaxed thin film as shown in Fig. 1.4. Homoepitaxy refers to an epitaxy of a single crystalline film on a same substrate or the same material. Homoepitaxy is used to grow a thin film which has an improved crystal quality compared to the substrate and to fabricate thin films with different doping levels. Fig. 1.4(a) shows the lattice arrangement of semiconductors during the homoepitaxy. The lattice contants of the deposited thin film and the substrate are the same, so strain-free and dislocation-free thin film could be obtained. However, homoepitaxy of III-nitrides is not available due to the lack of mature fabrication technology of nitride substrates. III-nitrides are commonly grown by heteropitaxy. Heteroepitaxy refers to an epitaxy of a single crystalline film on a foreign substrate or foreign layers. For heteroepitaxy, the deposited thin film suffers from several problems due to differences in lattice constant and thermal expansion coefficient between the film and the substrate. During the growth,

the film might experience a strain to accommodate the lattice contant mismatch as shown in Fig. 1.4(b). The strain is accummulated as the growth proceeds, and dislocations are inevitably generated at the interface between the film and the substrate when the film thickness exceeds a certain critical thickness, leading to the relaxation of the film strain as shown in Fig. 1.4(c). The structural imperfection of the film affects the physical, optical, and electrical properties. Therefore, it is crucial to consider the lattice constant mismatch for the heteroepitaxy of III-nitrides. In addition, the difference in thermal expansion coefficient between the film and the substrate induces a residual stress in the film.

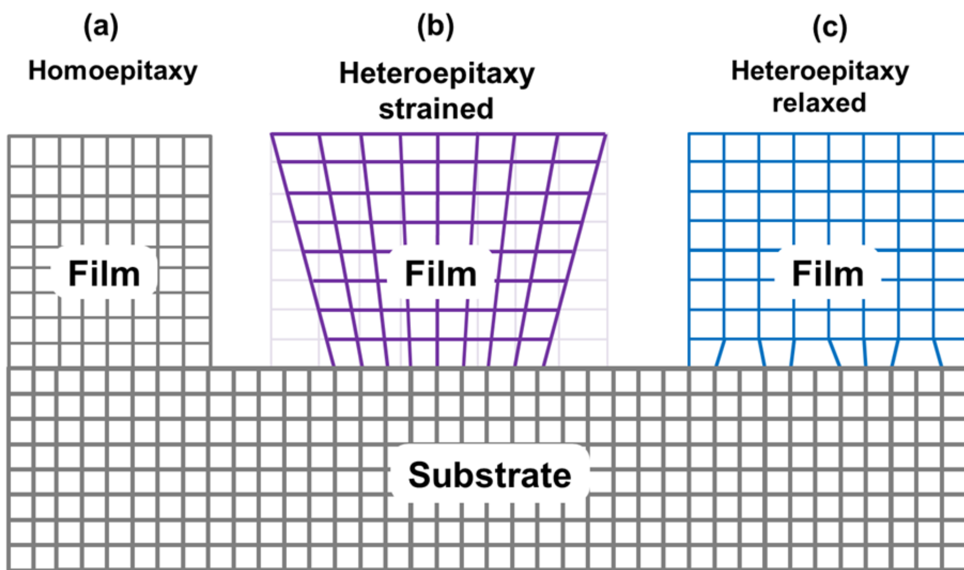

Figure 1.4. Epitaxy; (a) homoepitaxy, (b) heteroepitaxy of strained thin film, and (c) heteroepitaxy of strain-relaxed thin film.

1.3 Substrate for III-nitride

A major problem in the epitaxial growth of III-nitride is the difficulty of using native substrates. The homoepitaxial growth of III-nitrides on native substrates are still limited due to lack of commercially available substrate. Therefore, to obtain III-nitride epitaxial layers, heteroepitaxial growth on foreign substrates is essential. In order to determine suitable substrates for the epitaxial growth of III-nitrides, the crystal structure and the lattice constant mismatch have been considered as the primary criteria.[10] In addition, other properties such as thermal stability at high growth temperatures, thermal, chemical, and electrical properties are also important because the substrates might affect the device performance of III-nitride semiconductors. The crystal structure of III-nitrides is the hexagonal wurtzite as shown in Fig. 1.2, so substrate candidates should have hexagonal crystal structures with a small lattice constant mismatch with III-nitride layers. Also, substrate candidiates should be commercially available. Considering these factors, the most commonly used substrates are sapphire and Si substrates. The properties of sapphire substrate and Si substrate are described as follows.

1.3.1 Sapphire substrate

Sapphire, single crystalline α-phase aluminum oxide, is the most commonly used substrate for the epitaxial growth of III-nitrides due to its commercial availability, thermal stability, transparency, and gradual improvements in wafer size and crystal quality. The crystal structure of sapphire, as shown in

Fig. 1.5(a), is a corundum structure with the space group of sapphire is $R\bar{3}c$. The crystallographic symmetry can be decribed as rhombohedral or hexagonal. The epitaxial growth of III-nitrides on c-plane sapphire results in the c-plane nitrides. In order to reduce the lattice constant mismatch between III-nitrides and sapphire substrates, III-nitrides are grown with the rotation by 30° with respect to the sapphire.[11] Therefore, the epitaxial relationships between the nitrides and sapphire substrates are GaN <0002>|| sapphire<0006> and GaN<01$\bar{1}$0>||sapphire<$\bar{2}$110>. As a result, the lattice constant mismatch is reduced from 33% to 16% for the case of GaN on sapphire, as described in Fig. 1.5(b).

1.3.2 Si substrate

Si substrate is very low cost and commercially available in very large diameters up to 18 in. due to the well-established single crystal growth technique and development. The use of Si substrate as a substrate for the epitaxial growth of GaN has attracted much interests to penetrate the LED market reducing the production cost. Besides, the integration of optoelectronic nitride devices with Si electronics has attracted much attention.[12] The epitaxial growth of GaN on Si substrate was demonstrated by molecular beam epitaxy (MBE) in 1998.[13] During the last decade, the growth of GaN on Si substrate has been extensively studied. The crystal structure of Si is diamond-lattice structure with the space group of $Fd\bar{3}m$. The structure is defined as face-centered cubic (FCC) lattice containing 4 additional atoms in the lattice which is surrounded by four equidistant nearest neighbors that

lie at the corners of a tetrahedron.[10] Fig. 1.6(a) shows the atomic arrangements along the [001], [011], and [111] directions of the Si unit cell. For the growth of wurtzite III-nitrides, Si(111) is the most preffered substrate due to its trigonal symmetry. The crystallographic alignment of GaN on Si(111) substrate is shown in Fig. 1.6(b), which shows a good rotational matching between them. The epitaxial relationships between GaN and Si are $GaN<0002>\|Si<111>$ and $GaN<10\bar{1}0>\|Si<\bar{1}12>$. The lattice constant mismatches of Si with GaN and AlN are 17% and 19%, respectively, as listed in Table 1.2.

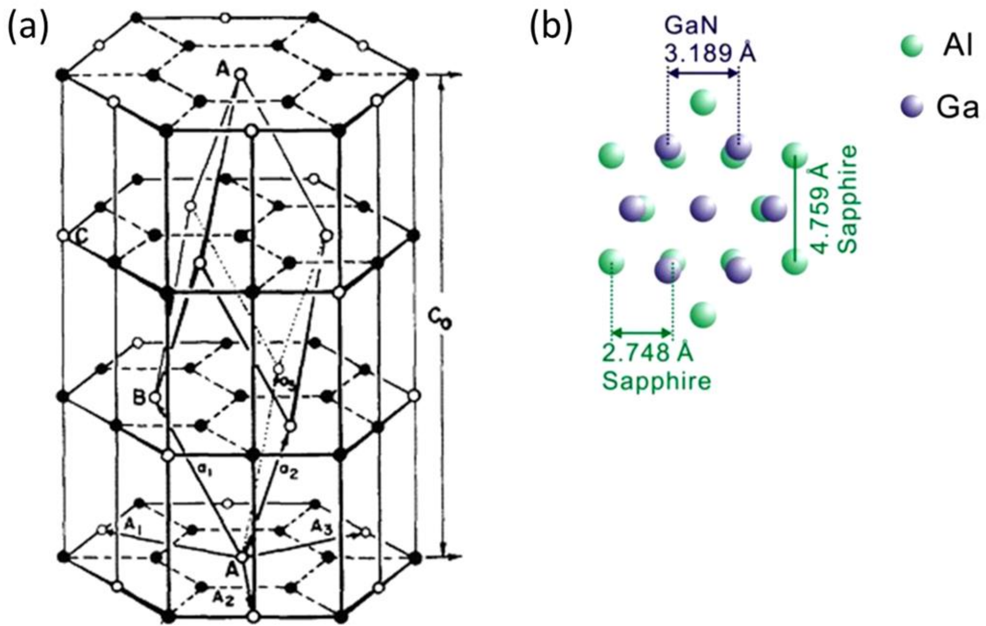

Figure 1.5. (a) Crystal structure of sapphire substrate[14] and (b) atomic arrangement of GaN and sapphire substrate.[12]

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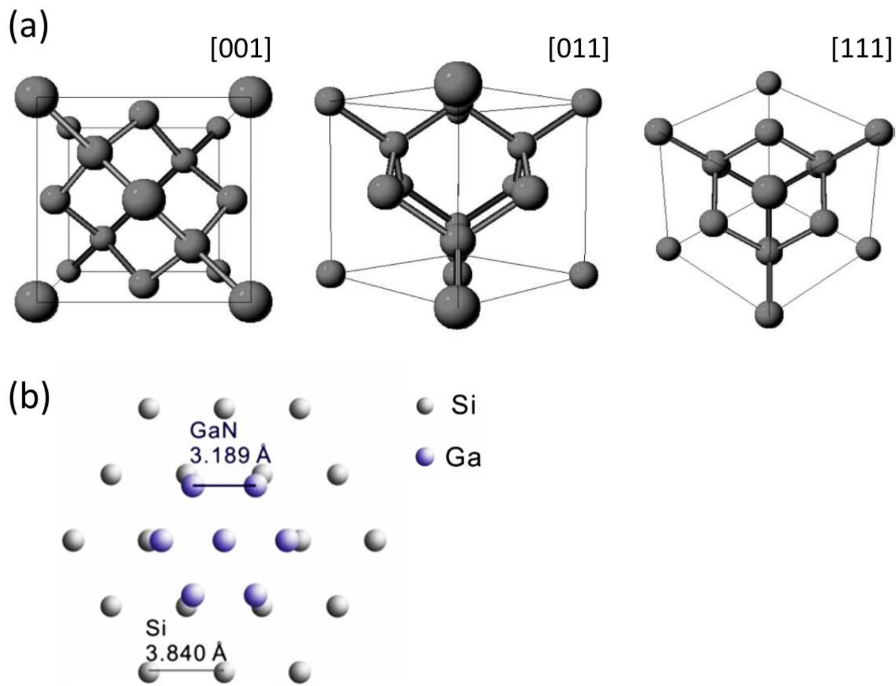

Figure 1.6. (a) Atomic arrangement of Si substrate along [001], [011], and [111] direction.[10] (b) Crystallographic alignment of GaN on Si substrate.[12]

Table 1.2. Properties of sapphire and Si substrates

		Sapphire	Si
Lattice constant (Å)		a= 4.759 c = 12.991	a = 5.431
Lattice mismatch	to GaN	-16%	17%
	to AlN	-13.3%	19%
Thermal expansion coefficient (10^{-6}/K)		a = 7.3 c = 8.5	a = 2.6
Thermal expansion mismatch (a)	to GaN	23.4%	-115%
	to AlN	43.2%	-60%
Thermal conductivity (W/mK)		0.41	1.3
Melting point (K)		2303	1690

1.4 Problems of heteroepitaxial III-nitrides

There are several problems of III-nitride semiconductors, which affect the physical, structural, optical, and electrical properties, thus deteriorate the performance of III-nitride LEDs. The problems mainly originate from the differences in properties of III-nitrides and the substrates which is inevitable for the heteroepitaxial growth of III-nitrides. The problems are dislocation, low light extraction efficiency, and film stress.

1.4.1 Dislocation

Lattice misfit is an important quantity that characterizes the epitaxial growth of the film on the foreign substrate and defined as follow:

$$\text{Lattice misfit} = [a_0(s) - a_0(f)]/a_0(s)$$

where $a_0(s)$ and $a_0(f)$ represent the lattice constant of unstrained substrate and film, respectively. The lattice misfits between nitrides (AlN and GaN) and two representative substrates (sapphire and Si) are listed in Table 1.2: for example, the lattice misfit between GaN and sapphire is 16%. Due to the lattice misfit between the III-nitrides and the substrates, high-density structural defects such as threading dislocations, are generated in the III-nitride epitaxial layers. The threading dislocations are reported to be non-radiative recombination centers which deteriorate the efficiency of devices.[15] In addition, the lifetime of III-nitride devices are affected by the defects in

the epitaxial layers. Although the epitaxial growth of III-nitrides has been extensively studied and significant improvement of crystal quality have been achieved, III-nitrides still suffer from high-density threading dislocations with the density of 10^8–10^{10} cm^{-2}. To improve the efficiency and the reliablility of III-nitride LEDs, it is crucial to grow high quality epitaxial layers with low-density dislocations.

1.4.2 Low light extraction efficiency

Light extraction efficiency (LEE) is defined as the number of photons extracted to free space per unit time to the number of photons emitted from active retion per unit time.[16] Most of the photons generated in the active region cannot escape from the semiconductor, resulting in low LEE. This is attributed to the total internal reflection, which is fundamentally based on Snell's law. When a light ray travels penetrating an interface between two different materials, the light experiences its velocity change depending on the refractive indices of the materials. The larger refractive index the material has, the smaller the velocity of the light in the material is, and the smaller the critical angle is. III-nitride materials have relatively large refractive indices (n_{GaN}=2.5), so that the total internal reflection severly reduces the LEE of III-nitride LEDs. For example, the critical angle at the GaN/sapphire is 23.6^o, calculated by using the refractive indices of GaN and air. This calculation indicates that only 4.2% of total light can be extracted from the structure based on the escape cone as shown in Fig. 1.7.

1.4.3 Film stress

The III-nitrides suffer from the residual film stress due to the differences in the lattice mismatch and the thermal expansion coefficient between the III-nitrides and the substrates as listed in Table 1.2. Because the III-nitride epitaxial layers commonly grown on foreign substrates at the growth temperature of 1000 ^{o}C by vapor phase epitaxy, the III-nitride layers are highly strained dominantly by the thermal mismatch when the III-nitrides are cooled to room temperature after the growth. The residual strain in the layers results in a wafer bow. The status of film stress is mainly determined by the thermal expansion coefficients of the film and the substrate. Considering the case of GaN on sapphire, the thermal expansion coefficient of sapphire is larger than that of GaN. Consequently, GaN layers grown on sapphire are compressively strained after the growth. On the contrary, in the case of GaN on Si, GaN layers grown on Si are under tensile stress. In addition to the thermal stress, intrinsic stresses are generated during the growth. Tensile stress is induced in the III-nitride layers on foreign substrates during the coalescence process of grains at initial growth stage. As shown in Fig. 1.8, when the grains of the deposited material coaslese together at the grain boundaries, the total energy of the system is minimized with the reduction of the surface area, *i.e.,* surface energy, accompanied by the elastic deformation resulting in the tensile stress.[17] For the growth of AlN epitaxial layer on sapphire substrate, large tensile stress is applied in the AlN layer due to the high density of grains compared to GaN, thus lots of cracks are generated on the surface during the growth at high temperature.[18,19]

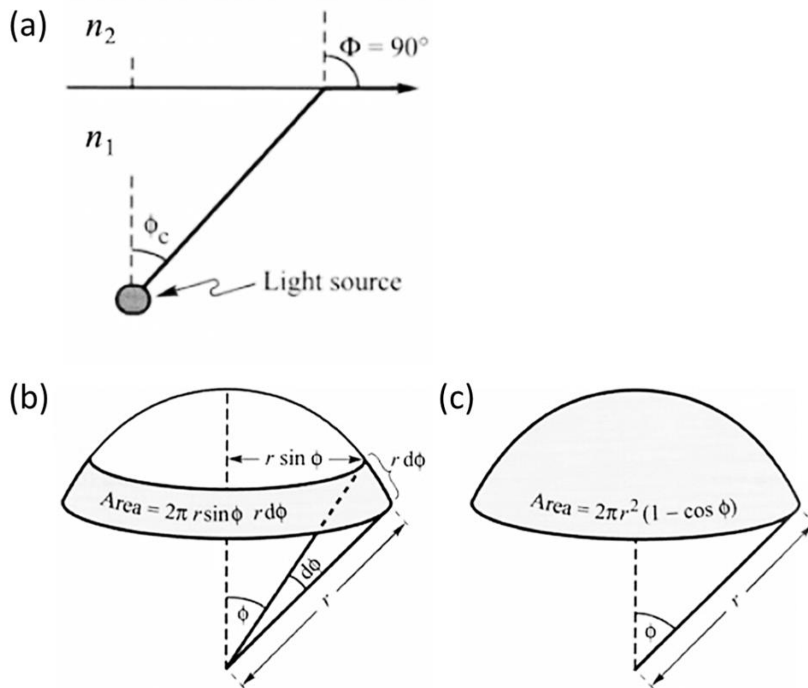

Figure 1.7. (a) Definition of the critical angle (ϕ_c) of the total internal reflection. (b) Area element dA. (c) Area of dome-shaped region.[16]

Figure 1.8. (a) Polycrystalline thin film before and after the coalescence of crystallites and (b) coalescence process showing the elastic displacement and stress associated with forming a continuous film.[17]

1.5 Epitaxial growth of III-nitrides on patterned substrates

To solve the problems in III-nitride LEDs and realize highly efficient III-nitride LEDs, many researches have been carried out until now. Representative technologies to grow high quality III-nitrides and improve the efficiency of III-nitride LEDs are epitaxial lateral overgrowth (ELO) and patterned sapphire substrate (PSS).[20-22]

In order to improve the efficiency of III-nitride LEDs, the growth of high quality III-nitride materials with low-density defects is crucial. ELO is a conventional technique to reduce the dislocation density. The schematic diagram of a typical ELO process is shown in Fig. 1.9. Firstly, a GaN epitaxial layer is grown on the foreign substrates such as sapphire, SiC, and Si. The GaN template has lots of threading dislocations. Secondly, dielectric growth masks such as silicon oxide (SiO_x) and silicon nitride (SiN_x) are patterned on the GaN template by using the deposition of dielectric layer on the GaN template and photolithography as shown in Fig. 1.9(a). In this step, there are window regions where the GaN layer is exposed. Subsequently, GaN is grown on the mask-patterned GaN template. During the growth, selective area growth of GaN is achieved, which indicates that the GaN is grown only in the window region except for the mask region. As the growth progresses, the GaN on the window region grows vertically and laterally as shown in Fig. 1.9(b). The GaN is laterally grown on the growth masks and finally forms a continuous layer through the coalescence of GaN as shown in Fig. 1.9(c). The growth masks block the propagation of threading dislocations beneath the masks, which is called as a dislocation filtering. As a result, the dislocation density of laterally grown GaN is reduced.

The dislocation filtering is also carried out by using the microstructure of GaN and the resultant dislocation bending behavior. The strategy is 2-step growth composed of (i) formation of side facets and (ii) lateral growth.[23] The vertical growth is preferred in the first step and the lateral growth is promoted in the second step. When side facets are developed during the 2-step growth, the threading dislocations bend towards the free surfaces, *i.e.*, side facets as shown in Fig. 1.10(a). It is reported that the threading dislocations minimize their free energy by bending towards to free surfaces when they meet the side facets in the layer.[24] Fig. 1.10(b) shows the schematic diagram of the bending behavior of dislocations (solid lines) clearly. Consequently, the dislocation density could be further reduced using the dislocation bending behavior.

Derived from the ELO, PSS technology is the most widely used technology in GaN-based LED industries to achieve highly efficient LEDs. The PSS is fabricated by using the photolithography and dry etching of the sapphire substrates. The PSS not only reduces the dislocation density of the nitride material thereon but also enhances the LEE.[25] Fig. 1.11 shows the mechanism for the enhancement of LEE. As mentioned in Chap. 1.4.2, only 4.2% of total light could escape from the air/GaN interface, experiencing the total internal reflections. Likewise, 13% of total light could be extracted at the GaN/sapphire interface. Most of light generated in the active layer is trapped in the semiconductor as shown in Fig. 1.11(a). On the contrary, the PSS effectively enhances the LEE by breaking the total internal reflections. The patterns in the PSS play role in scattering the light randomly and give photons more chances to enter the escape cone as shown in Fig. 1.11(b), resulting in the enhancement of LEE.[26]

In addition, the PSS technology is superior to conventional ELO

technology in that it does not use any dielectric mask and does not require a growth interruption. So, the PSS is a contamination-free substrate and it saves manufacturing cost with reduced growth time.

Figure 1.9. Schematic diagrams of a typical ELO process: (a) Patterning of dielectric materials such as SiO_x and SiN_x as the growth mask on the GaN template, (b) regrowth of GaN, and (c) coalescence of GaN forming a continuous film.

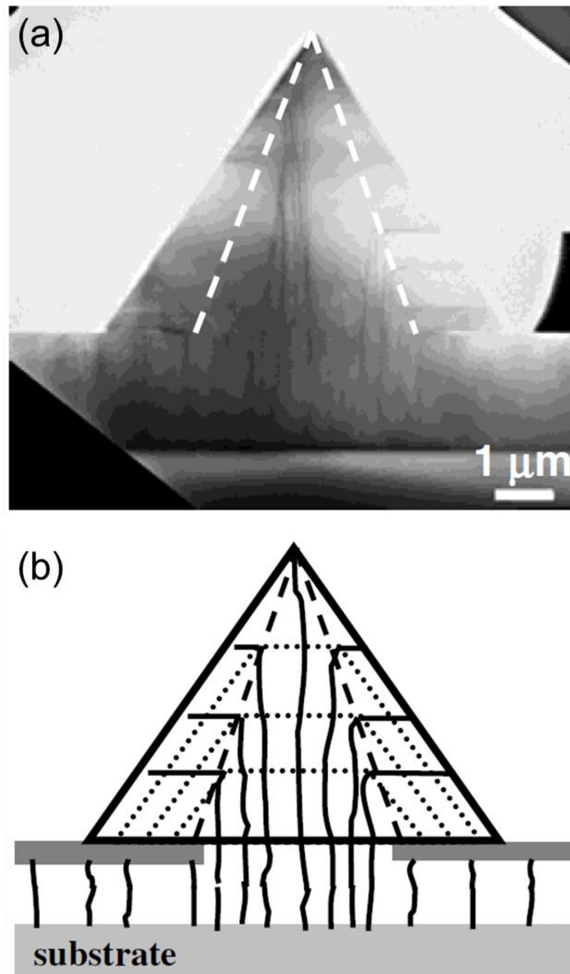

Figure 1.10. (a) Cross-section TEM image showing the bending of threading dislocation. (b) Schematic diagram showing the 2-step ELO. The dashed lines join the dislocation bending points and the solid lines indicate dislocations.[23]

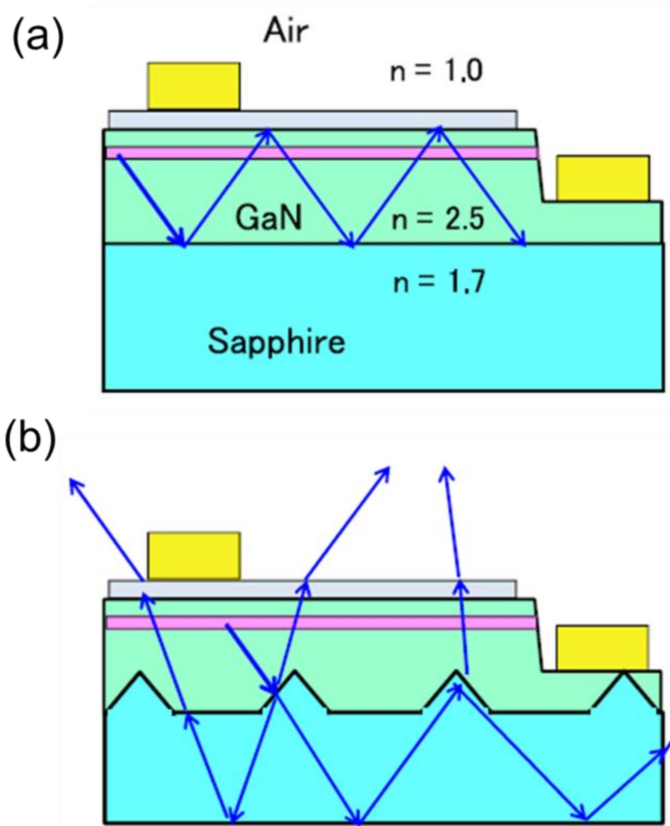

Figure 1.11. Schematic LED structure and photon trajectories: (a) LED on a planar substrate and (b) LED on a PSS.[25]

1.6 Thesis contents and organization

The major goal of this study is to grow high quality III-nitride epitaxial layers on foregin substrates for LED applications. As we discussed above, patterned substrates is crucial to improve the crystal quality of III-nitrides and enhance the LEE of optical devices. When the patterned substrates are fabricated in microscale, however, several problems such as large spacing between the patterns, small diffusion length of adatoms, and production cost still exist. To overcome the problems, nano-patterned substrates for the epitaxial growth of III-nitrides were proposed in this study. It contains three big parts as research subjects about new nano-patterned substrates for important epitaxial structures in the III-nitride LED applications such as GaN on Si, AlN on sapphire, and GaN on sapphire, in parallel.

1. Nano-patterned AlN/Si substrates were proposed for the epitaxial growth of *GaN on Si*. Nanoheteroepitaxy is a useful technique to growth high quality GaN films on Si substrates, however, it is difficult to obtain continuous nitride layers on the nano-patterned due to the limit in narrowing the pitch between the patterns and the small and non-uniform patterns fabricated by former nanopatterning techniques. In addition, an unwanted growth of GaN between the Si nanopatterns, leading to the polycrystal GaN film. To solve the problem, we proposed an AlN/Si(111) nanorod substrate. To fabricate the pattern, we employed a simple and cost-effective nanosphere lithography technique. It provides a uniform pattern of nanoscale hexagonal close-packed array with a narrow gap between

the nanorods. The *in-situ* nitridation of exposed Si surfaces of AlN/Si(111) nanorods was performed to grow GaN film only on the AlN seed and avoid Ga-Si meltback etching reaction. The growth of GaN on AlN/Si(111) nanorods fabricated by nanosphere lithography and properties of GaN layers were studied.

2. Nano-patterned AlN/sapphire substrates were proposed for the epitaxial growth of *AlN on sapphire*. The growth of AlN on sapphire substrates leads to a high density of extended defects such as threading dislocations and cracks due to the large lattice mismatch and thermal mismatch between the epitaxial layer and substrates as well as the low surface mobility of Al adatoms. In addition, the LEE of AlGaN-based deep UV LEDs is severely limited. It has been reported that ELO on microscale patterned substrates is effective to improve the crystal quality of overgrown AlN layers. However, it requires high growth temperature and long growth time, thus high cost. To solve the problems, we proposed nano-patterned AlN/sapphire substrates fabricated by nanosphere lithography. We confirmed that the nano-patterned AlN/sapphire substrate improve the crystal quality, reducing the residual film stress. Also, DUV LEDs were fabricated and characterized.

3. Nano-cavity patterned sapphire substrates were proposed for the epitaxial growth of *GaN on sapphire*. The embedment of void in the GaN layer is considered as a promising technique to solve most of the problems of GaN-based LEDs simultaneously. Besides, the trend in the substrate patterning is to reduce the pattern size from microscale

to nanoscale. In comparison to the micro-patterned substrates, nano-patterned substrates have been reported to enhance the LEE due to the increased density of patterns in the same area. For this purpose, nanoscale cavity patterns patterns which are composed of nanoscale voids surrounded by thin alumina shell were fabricated by a simple and cost-effective spin coating process. The epitaxial growth of GaN on the NCPSS was investigated by varying the growth times. The nanoscale ELO improved the crystal quality further by delaying the coalescence of GaN. The nano-cavities embedded in the GaN layer relaxed the residual compressive stress and enhanced diffuse reflectance, *i.e*. LEE, by breaking the total internal reflections of lights.

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Chapter 2. Experiments and analysis

2.1 Growth process

2.1.1 Metal-organic chemical vapor deposition (MOCVD)

Thomas Swan 6×2 in. close-coupled showehead MOCVD system was used to grow III-nitride epitaxial layers in this work.

Metal-organic precursors including trimethylaluminum (TMAl, $(CH_3)_3Al$), trimethylgallium (TMGa, $(CH_3)_3Ga$) were used as the precursors of the group III sources. Ammonia (NH_3) was used as the precursor of the group V source. Hydrogen gas (H_2) was used as a carrier gas during the growth.

2.1.2 Atomic layer deposition (ALD)

Amorphous aluminum oxide, also called as alumina, was deposited by ALD (Lucida D100). TMAl and de-ionized water (H_2O) were used as the precursors of Al and O, respectively. Nitrogen gas (N_2) was used as a purge gas. Each ALD cycle consists of the alternative supply of TMAl and H_2O. The duration times for the precursor supply and the purge were 0.2 s and 3 s, repectively.

2.2 Analysis tools

2.2.1 Scanning electron microscopy (SEM)

Structural characteristics of the fabricated substrates and nitride epitaxial layers were analyzed by field-emission SEM (Hitachi S-4800). Platinum (Pt) was coated on the samples by sputtering to avoid the surface charging before putting the SEM specimens in the SEM chamber.

2.2.2 High resolution X-ray diffraction (XRD)

Crystal structure and crystal quality were measured by high resolution XRD (Phillips PANalytical X'pert Pro) using theta-2theta scan and ω rocking curve scan. The wavelength of X-ray was 1.5406 Å from Cu-$K\alpha_1$ radiation. The angle resolution is 12 arcsec or less by using 4 bounce Ge 220 monochrometer.

2.2.3 Atomic force microscopy (AFM)

The AFM measurement was carried out using Park Systems XE-100 to analyze the surface morphology of nitride layers. The surface of nitride layers were scanned by non-contact mode. XEI 1.8.0 was used for the analysis of AFM results.

2.2.4 Photoluminescence (PL)

PL measurement, which is a non-destructive analaysis, was performed to investigate the optical spectra of nitride semiconductors. The excitation source was a 325 nm line of He-Cd laser.

2.2.5 Cathodoluminescence (CL)

In order to investigate the crystal quality of nitride layers, the CL measurement (Gatan MonoCL4) was carried out in panchromatic mode at room temperature. The acceleration voltage was 5 kV and the working distance between the samples and the objective lense was 6 mm.

2.2.6 Micro-Raman spectroscopy

Micro-Raman spectroscopy (Horiba JY Labram ARAMIS) was carried out to evaluate the residual stress of nitride layers. The 633 nm line of He-Ne laser was used as the excitation source. The Raman scattered light signal was collected in a backscattering geometry using the x100 microscope objective lens. The frequency of the Raman lines were calibrated using the c-Si wafer at 520.6 cm^{-1}.

2.2.7 Transmission electron microscopy (TEM)

TEM specimens were prepared by using focused ion beam (FIB, NOVA 600 Nanolab). Cross-section TEM micrographs were obtained by JEOL JEM-

2100F with the acceleration voltage of 200 kV. Bright-field mode was used to investigate the threading dislocations in epitaxial layers. Selected area diffraction patterns of alumina were obtained to analyze the crystal structure.

2.2.8 Light-current-voltage (L-I-V) measurement

For I-V measurement, Agilent B2902A Precision Source/Measurement unit was used with voltage sweep from -5 V to 15 V under DC current condition. For L-I measurements, light output (5 ms current pulse sweep, 1% duty cycle) was measured as a photocurrent using a Si photodetector, the same Source/Measurement unit, and bottom-emission measurement setup in a freestanding condition in a dark room environment. The measurement was carried out with the help from Nano Photonics and Optoelectronics Laboratory, Pohang University of Science and Techonology.

Chapter 3. Nanoheteroepitaxy of GaN on AlN/Si(111) nanorods

3.1 Introduction: nanoheteroepitaxy of GaN on Si substrate

The growth of GaN on Si substrates has attracted much attention because Si has several advantages including low cost, availability of large wafer size, and high thermal conductivity.[1,2] In addition, the epitaxial growth of GaN on Si has benefits of compatibility with well-established Si technology and potential for optoelectronic device integration with Si-based circuits. However, the growth of GaN on Si substrates is challenging due to the large mismatches in thermal expansion coefficient (56%) and lattice constant (17%) between GaN and Si, resulting in the high dislocation density (~10^{10} cm^{-2}) and the formation of cracks.[3-5] To overcome the problems and to realize the GaN-based devices on Si substrates, various methods including low-temperature AlN interlayer,[6] Si delta-doping,[7] AlGaN buffer layer,[4] and patterned substrate[8,9] have been investigated.

Nanoheteroepitaxy (NHE), a selective growth of heteroepitaxial film on nanopatterned substrates, has been investigated for the growth of lattice-mismatched materials.[10] Luryi *et al*. provided a background study of NHE that both epitaxial film and substrate experience a three-dimensional deformation so that the strain associated with the lattice mismatch can be relaxed.[11] Fig. 3.1 shows the strain-relief mechanism through NHE. In the case of planar structure, the epitaxial layer can elastically deform only along vertical direction as shown in Fig. 3.1(a). On the contrary, in nanoscale

islands the epitaxial layer and substrate can deform vertically and laterally as shown in Fig. 3.1(b). Therefore, when epitaxial layer is grown on the nanoscale islands, there is strain partitioning between the epitaxial layer and the substrate as shown in Fig. 3.1(c). Moreover, the strain decays exponentially away from the interface. The strain energy and effective range of strain is proportional to the island diameter. The smaller the diameter is, the faster the strain decays.

Besides the theoretical study, experimental results for the growth of GaN on nanopatterned Si have been reported, demonstrating that NHE was a useful technique to obtain high quality GaN films on Si substrates. [12-17] In order to fabricate the nanopatterned Si substrates for NHE, several techniques such as interferometric lithography[12-14] as shown in Fig. 3.2(a) and patterning with anodic aluminum oxide (AAO) mask[15-17] as shown in Fig. 3.2(b) have been adopted. However, most of the results reported the growth of non-continuous GaN islands. This is due to the limit in narrowing the pitch between the patterns by interferometric lithography[12] and due to the small (~60 nm) and non-uniform patterns transferred by AAO mask resulting in the variation in size of the GaN nuclei overgrown on the patterns.[17] In addition to the growth of GaN on top of the Si patterns, Liang *et al*. reported an unwanted growth of GaN between the Si nanopatterns, leading to the polycrystalline GaN film.[15] Considering the above results, we believe that uniform distribution of patterns with a narrow gap and careful selective growth on top of the patterns is essential to obtain a fully coalesced GaN film using NHE. In this chapter, we investigate NHE of GaN film on an AlN/Si(111) nanorod substrate. To fabricate the pattern, we have employed a simple and cost-effective nanosphere lithography technique. It provided a

uniform pattern of nanoscale hexagonal close-packed array with a narrow gap between the nanorods, which is critical for the realization of the continuous GaN film growth.

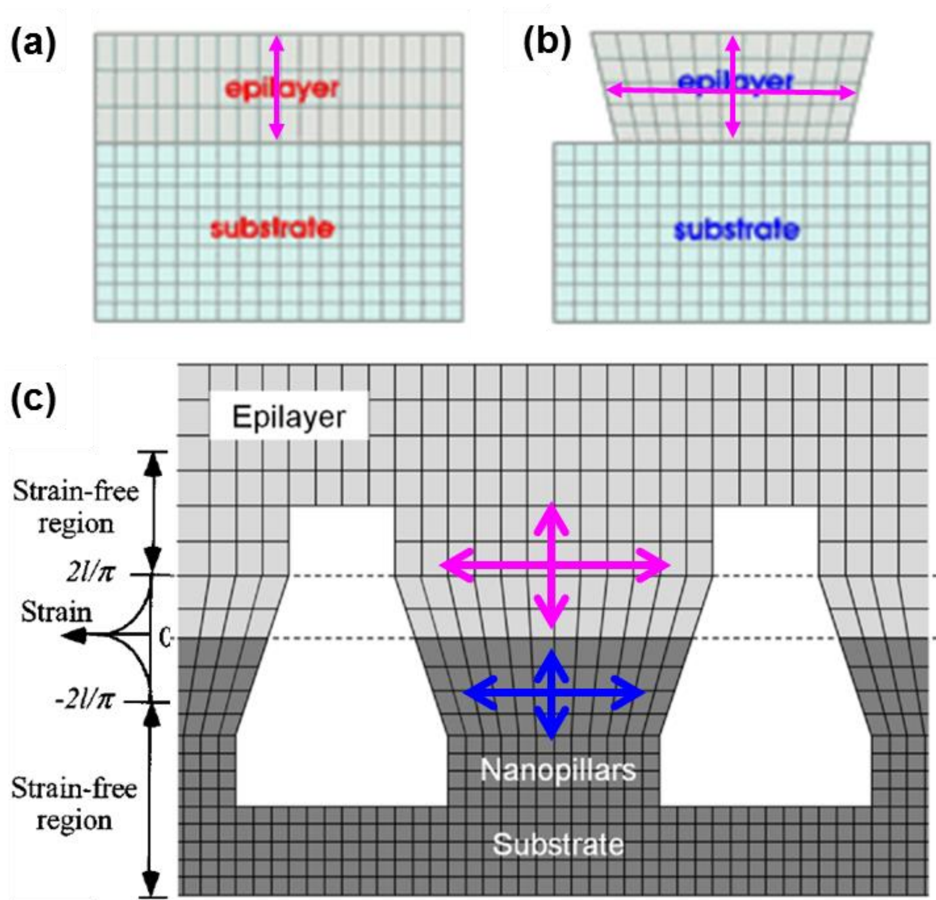


Figure 3.1. Concept of nanoheteroepitaxy: schematic diagrams showing (a) epitaxial layer on the planar substrate, (b) three-dimensional epitaxial island on the planar substrate, and (c) epitaxial layer selectively grown on the nanoscale substrate.

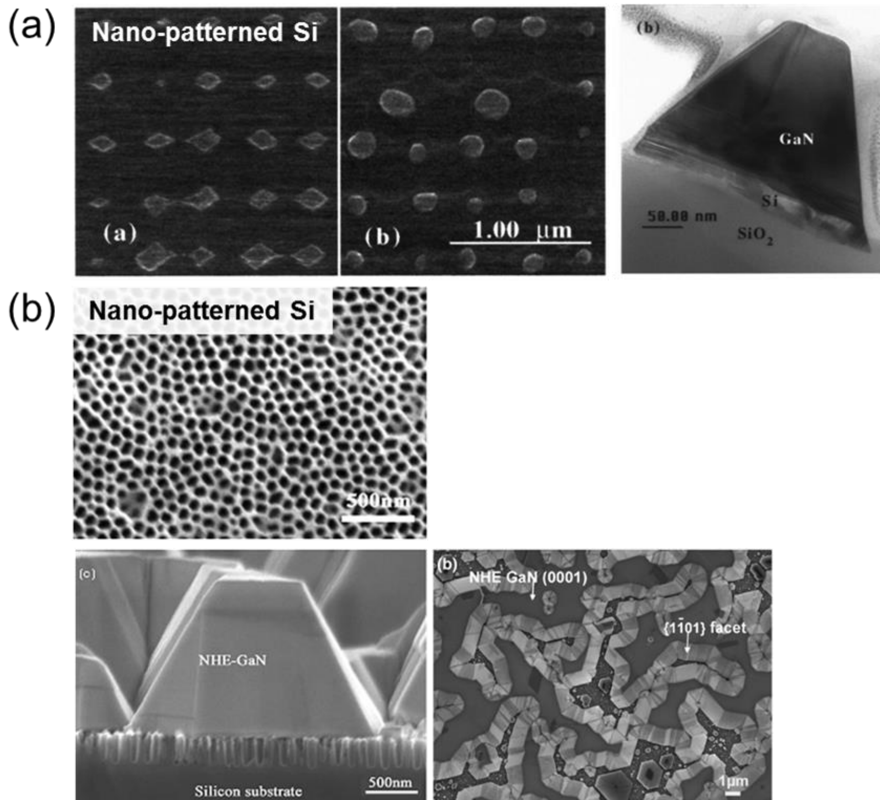


Figure 3.2. Nano-patterned Si substrates and GaN grown on the substrates fabricated by (a) interferometric lithography[12] and (b) lithography using AAO nanoporous mask.[17]

3.2 Experimental procedure

Fig. 3.3 shows the schematic diagram of NHE GaN on AlN/Si(111) nanorods. Si(111) substrates were loaded in a 6×2 in. Thomas Swan close-coupled showerhead MOCVD reactor. A native oxide layer on the surface was thermally removed in H_2 ambient at 1070 °C for 5 min. Subsequently, an 170 nm-thick AlN layer was grown on the Si(111) substrate at 1045 °C, following the 10 s Al pre-deposition to suppress the nitridation of the Si surface.[18] The samples were taken out and a monolayer of silica (SiO_2) nanospheres was coated on the AlN layer by spin coating. The silica nanospheres of a 300 nm diameter were synthesized by the Stöber method.[19] Reactive ion etching (RIE) was carried out to make the AlN/Si(111) nanorod substrate with 10 sccm Cl_2 and 2 sccm Ar flow rates at 6.7 Pa and 200 W RF power. The silica nanospheres behave as the etch mask during the etching process. The etched substrate was cleaned with a buffered oxide etchant to remove the residual silica nanospheres. The AlN/Si(111) nanorod substrate was loaded into the MOCVD reactor for the growth of GaN layer. Prior to the growth, *in-situ* nitridation of the exposed Si surface was performed in NH_3 ambient, resulting in the SiN_x passivation of the Si surface. This scheme enabled us to grow GaN film only on the AlN layer on top of the nanorods avoiding the Ga-Si meltback etching reaction and the growth of GaN between the nanorods. Then, a thin (50 nm) AlGaN buffer layer was deposited and subsequently, a GaN epitaxial layer was grown on the top at 1045 °C and 10.1 kPa. For comparison, a planar AlN/Si(111) substrate was loaded in the same batch of the MOCVD growth of GaN. TMAl, TMGa, and NH_3 were used as the precursors of Al, Ga, and N, respectively.

The structural characteristics of the GaN layers were analyzed by field emission SEM and TEM. The TEM samples were prepared by focused ion beam. The crystalline quality was characterized by XRD and CL. The residual stress in the GaN layers was measured by micro-Raman spectroscopy with a 633 nm line of He-Ne laser. The optical properties were evaluated by PL measurement at 20 K using a 325 nm He-Cd laser.

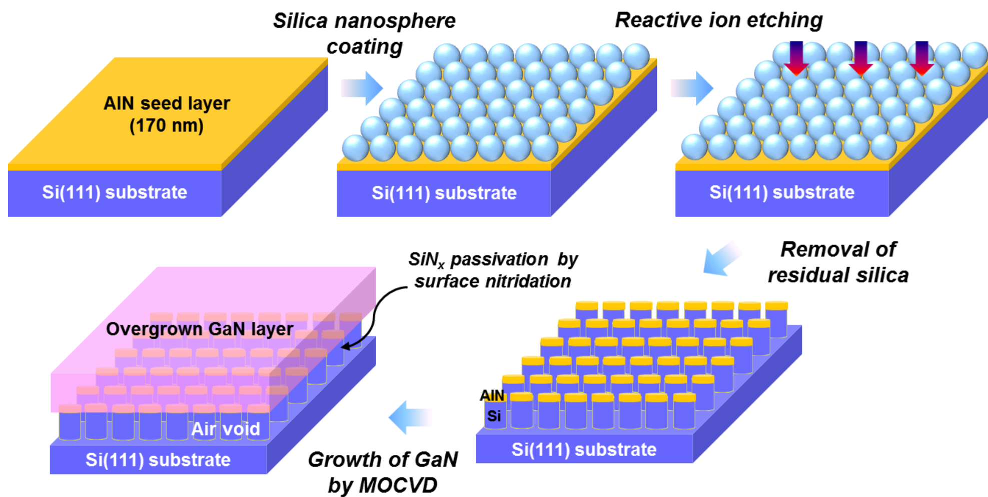


Figure 3.3. Schematics showing nanoheteroepitaxy of GaN on AlN/Si(111) nanorods fabricated by silica nanosphere lithography.

3.3 Results and discussion

3.3.1 Fabrication of AlN/Si(111) nanorods

An AlN layer was grown on Si(111) substrate by MOCVD as a seed layer for the growth of GaN thereon. The AlN layers were grown by two different growth scheme: (i) 1-step growth at 1040 ^{o}C for 10 min and (ii) 2-step growth at 1000 ^{o}C for 5 min and 1040 ^{o}C for 5 min. The total thicknesses of both AlN layers were same as 170 nm. Fig. 3.4(a) represents AFM and SEM images showing the surface morphologies of the 1-step AlN layer. The surface roughness measured by AFM was 2.224 nm and the 1-step AlN showed three-dimensional surfaces. Fig. 3.4(b) shows AFM and SEM images of the surface of the 2-step AlN layer. The surface was flattened and the surface roughness decreased to 1.518 nm compared to that of the 1-step AlN. During the temperature ramping-up process, the recrystallization of the AlN layer grown at 1000 ^{o}C occurred, which resulted in the reduction of surface roughness of the two-step AlN.

Fig. 3.5 shows SEM images of Si nanopillars fabricated by polystyrene nanosphere lithography reported by Cheng and coworkers.[20] The polystyrene nanospheres act as etch masks. As shown in Fig. 3.5, nanosphere lithography provides periodic hexagonal array with narrow spacing between the nanopillars, which enables the overgrowth of continuous GaN films on the patterns. Furthermore, the nanosphere lithography using nanosphere coating is a simple and cost-effective technology compared to other nanopatterning methods.

A schematic diagram showing a typical spin coating process is shown in

Fig. 3.6(a). First step is the deposition of nanosphere solution composed of nanospheres and solvent on a target substrate. Second step is the spinning of the substrate. During the spinning process, the nanospheres are arranged on the substrate by various forces acting on them. As shown in Fig. 3.6(b), there are forces applied to them such as capillary force and van der Waals force between the nanospheres, centrifugal force, and charge/attractive force between the nanospheres and the substrate.[21] By balancing the forces, self-assembly of nanospheres could be achieved.

Fig. 3.7(a) and 3.7(b) show SEM images of a monolayer of hexagonally close-packed silica nanospheres on the AlN layer. As shown in Fig. 3.7(a), well-aligned silica nanospheres were coated on the AlN layer by spin coating. Occassionally, defects of silica nanosphere array such as vacancies and grain boundaries were observed, as shown in Fig. 3.7(b). The periodic silica nanosphere array was used as the etch mask for the fabrication of the nanopatterned AlN/Si(111) substrate by the RIE.

Fig. 3.8 shows the well-defined AlN/Si(111) nanorod substrate. Each AlN/Si(111) nanorod included a cylindrical Si rod and a thin AlN layer on the top of the cylinder which behaved as a seed layer for the subsequent epitaxial growth of GaN. The diameter and the height of the AlN/Si(111) nanorods were about 285 nm and 950 nm, respectively. The gap between the nanorods was measured to be as narrow as 30 nm, which was expected to enable the growth of a fully coalesced GaN film. The structural parameters of the AlN/Si(111) nanorods such as diameter, height, and resultant gap were controlled by the RIE time.

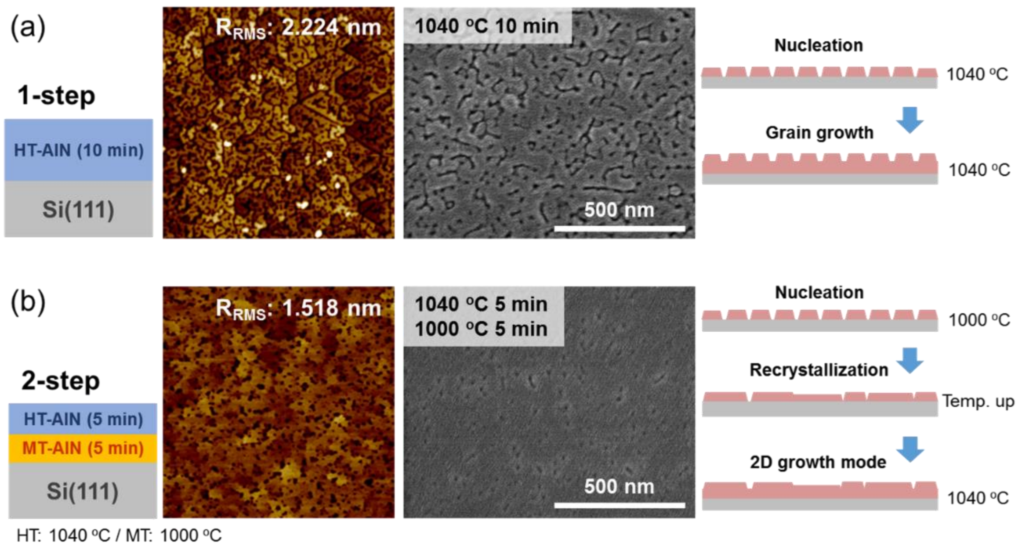


Figure 3.4. Surface morphologies measured by AFM and SEM of 170 nm-thick AlN layer on Si(111) substrate using (a) 1-step growth and (b) 2-step growth.

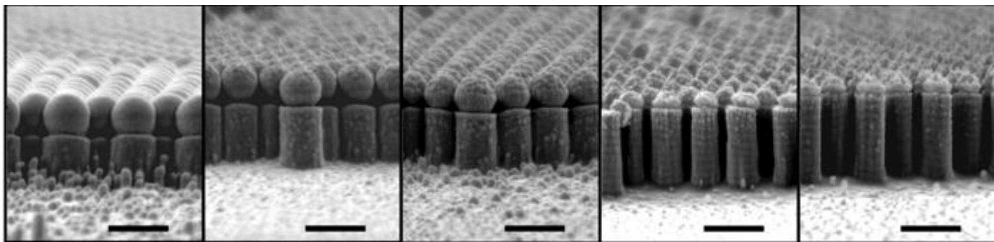


Figure 3.5. Nanosphere lithography combined by patterning of nanospheres and following dry etching of underlying material with nanosphere mask.[20]

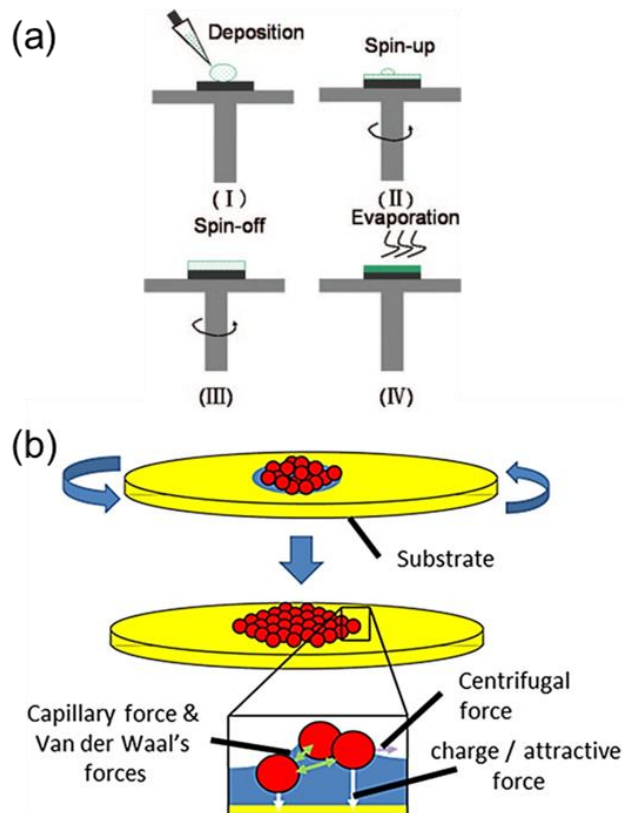


Figure 3.6. (a) Schematics showing the patterning of nanospheres by spin coating and (b) self-assembly of nanospheres resulting from varous forces acting on them.[21]

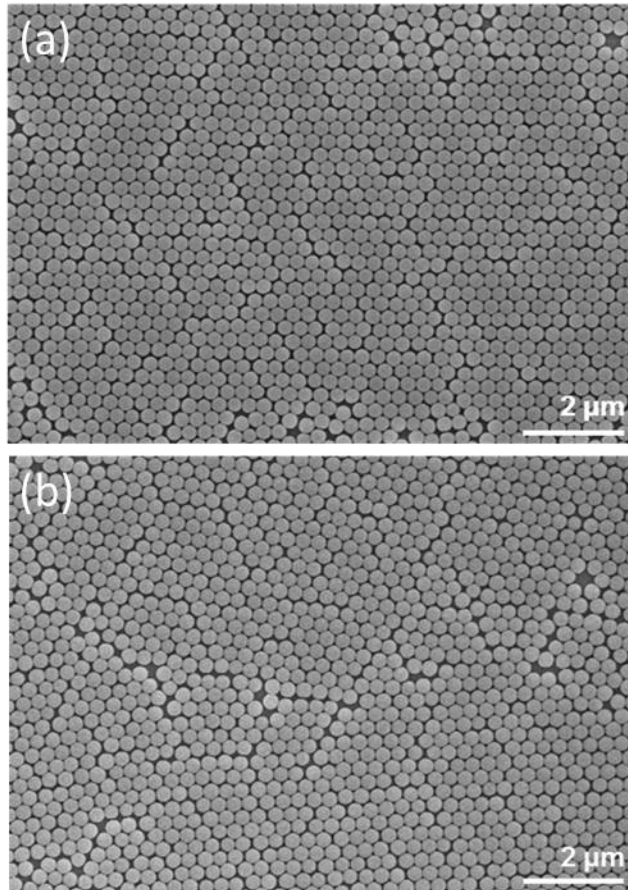
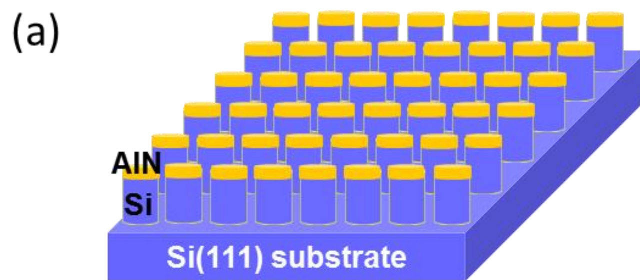


Figure 3.7. (a) SEM image of well-defined silica nanosphere monolayer coated on the AlN/Si(111) and (b) defects of patterns such as vacancy and grain boundary of the nanosphere array.



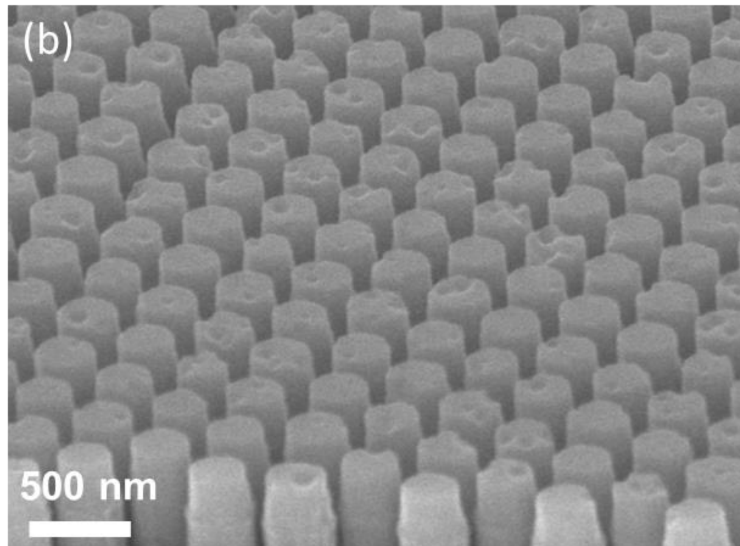


Figure 3.8. (a) Schematic diagram of AlN/Si(111) nanorods and (b) bird's-eye-view SEM image of the fabricated AlN/Si(111) nanorods.

3.3.2 Growth of GaN on AlN/Si(111) nanorods

Fig. 3.9 is a schematic growth process for NHE GaN on the fabricated AlN/Si(111) nanorod template. The growth temperature and the pressure were fixed to 1045 ^{o}C and 76 torr, respectively. While previous NHE reports starts with nanopatterned Si substrate, we used AlN/Si template with nitridation process as starting NHE template. Before the main nitride growth, *in-situ* nitridation of the exposed Si surface was perfomed in NH_3 ambient to grow nitrides only on top of the nanorods selectively and avoid Ga-Si meltback etching. Before the nitridation process, the sidewall of AlN/Si(111) nanorod is Si, which might cause Ga-Si meltback etching when Ga-containing nitrides are grown on it, as illustrated in Fig. 3.10(a). If the Si surface of AlN/Si(111) nanorod is nitridated by *in-situ* nitridation, the surface is passivated by silicon nitride (SiN_x) as shown in Fig. 3.10(b). The resultant SiN_x passivation layers of the AlN/Si(111) nanorods not only suppress the Ga-Si meltback etching but also enhance a growth selectivity by suppressing the growth of nitrides on SiN_x and promote the growth on AlN top seed layer. And 50 nm-thick AlGaN was used as an interlayer between GaN and AlN.

Fig. 3.11(a) and the inset are plan-view and bird's-eye-view SEM images of the GaN islands grown on the AlN/Si(111) nanorods for 3 min. It was shown that, at the initial growth stage, the GaN islands have well-defined hexagonally truncated pyramidal shapes surrounded by the side facets of $\{1\bar{1}01\}$ planes which were determined by the angle of 62° with respect to the basal (0001) planes. When the growth progressed, the GaN islands were expected to grow not only in the vertical direction but also in the lateral one and finally to form a continuous GaN film on the nanorods.

After the 40 min growth, the thickness of the NHE GaN film was measured to be 1.85 μm. Fig. 3.12 shows a cross-section SEM image of the fully coalesced GaN film overgrown on the AlN/Si(111) nanorods. We found that each nanorod consisted of the well-defined Si rod, the AlN thin film, and the AlGaN buffer layer which was deposited in a truncated pyramidal shape on the top. Also, it was clear that the film was grown only on the AlN seeding layer but the growth of GaN on undesirable sites, the area between the Si-rods and the sidewall, was effectively suppressed by the SiN_x passivation layer. The air voids were formed between the nanorods and they were expected to relieve the stress in the epitaxial layer. The surface examination showed that the continuous film was obtained, although some small pits were found on the surface.

To investigate the crystal structure of NHE GaN, XRD measurement was carried out. Fig. 3.13(a) is a 2theta-omega scan and indicates that the epitaxial structure is composed of GaN, AlGaN, and AlN on the Si(111) substrate. The lattice parameter along the c-axis of AlGaN was calculated to be 0.507 nm. Accordingly, the Al composition of the AlGaN layer was calculated to be 54% from and Vegard's law as follow:[22]

$$x_{Al} = (c_{Al_xGa_{1-x}N} - c_{GaN})/(c_{AlN} - c_{GaN}),$$

where c and x represent the lattice parameter along the c-axis and the Al composition, respectively. As shown in Fig. 3.13(b), six peaks with 60° intervals from the phi scan of asymmetric (102) reflection reveals that the NHE GaN layer is a single crystal with hexagonal symmetry.

Cross-section TEM analysis was carried out to investigate the crystalline quality and dislocation behavior in the NHE GaN layers. The comparison of Fig. 3.14(a) and 3.14(b), cross-section TEM images of the interfacial region along $[11\bar{2}0]$ zone axis, showed that the threading dislocation density (TDD) of the NHE GaN grown on the AlN/Si(111) nanorods was somewhat lower than that of GaN on the planar AlN/Si(111). To confirm the reduction of TDD, CL measurement was conducted on both GaN layers as shown in Fig. 3.14(c) and 3.14(d). TDDs determined by dark spots in the CL images were about 2.2×10^9 and 1.2×10^9 cm^{-2} for the GaN grown on the planar AlN/Si(111) and on the AlN/Si(111) nanorods, respectively. TDD was found to decrease down to half. In order to investigate the mechanism for the reduction of TDD, TEM images were taken at the interfacial area for GaN on the AlN/Si(111) nanorod substrate. Fig. 3.15(a) and 3.15(b) are bright-field TEM images taken at the same region under $g = [0002]$ and $g = [1\bar{1}00]$ diffraction conditions, respectively. Screw-type (S, Burgers vector $b =< 0002 >$) and mixed-type (M, $b = 1/3 < 11\bar{2}3 >$) TDs are visible under the $g = [0002]$ diffraction condition, while edge-type (E, $b = 1/3 < 11\bar{2}0 >$) and mixed-type TDs are observable under the $g = [1\bar{1}00]$ diffraction condition. Based on the observation, we believe that all the types of dislocations experienced the bending, which was also observed for the NHE of GaN on a nanoporous Si.[17] It is worth noting that some of the mixed-type dislocations generated at the interface propagated in the [0001] direction, and when they met the $\{1\bar{1}01\}$ sidewalls of growing GaN truncated pyramids shown in Fig. 3.15(a), they changed the propagation direction as indicated by the arrows. Then, the bent TDs continued to propagate parallel to the (0001) basal plane as shown in Fig. 3.15(a) and 3.15(b). Sun *et al*. have suggested that TDs were bent to

minimize their energy when meeting the $\{1\bar{1}01\}$ sidewalls as shown in Fig. 3.16.[23] In addition, stacking faults formed near the interface could block the propagation of TDs, indicated by arrows in Fig. 3.17. It is well known that stacking faults are typical defects in NHE GaN formed near the GaN/Si interface[14-16] when the GaN islands coalesced together[24] as shown in Fig. 3.18. Consequently, we speculate that the TD bending and the termination of TD by stacking faults contributed to the reduction of TDD in the GaN layer on the AlN/Si(111) nanorods.

Fig. 3.19(a) and 3.19(b) are XRD rocking curves of (002) plane and (102) plane of the GaN layers. The peak intensities were normalized. The full width at half maximum (FWHM) values of (002) planes were 557 and 540 arcsec for the GaN layer on AlN/Si(111) nanorods and planar AlN/Si(111), respectively. Unlike the similar FWHM values of (002) plane for both samples, the NHE GaN showed a somewhat lower FWHM value of (102) plane, 728 arcsec, compared to 1005 arcsec for GaN on the planar AlN/Si(111). This result is consistent with the TEM and CL results showing the improved crystalline quality with the lower TDD for the NHE GaN.

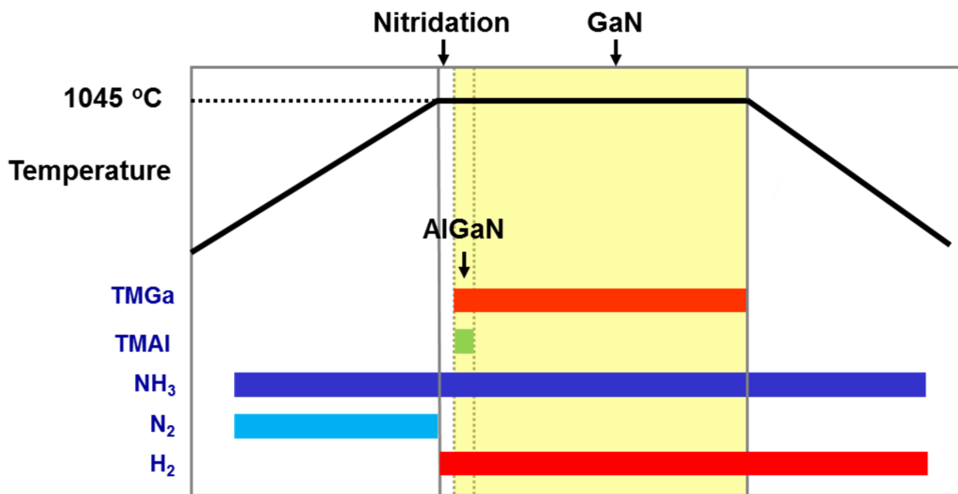


Figure 3.9. MOCVD growth scheme of GaN on AlN/Si(111) nanorods including the *in-situ* nitridation step.

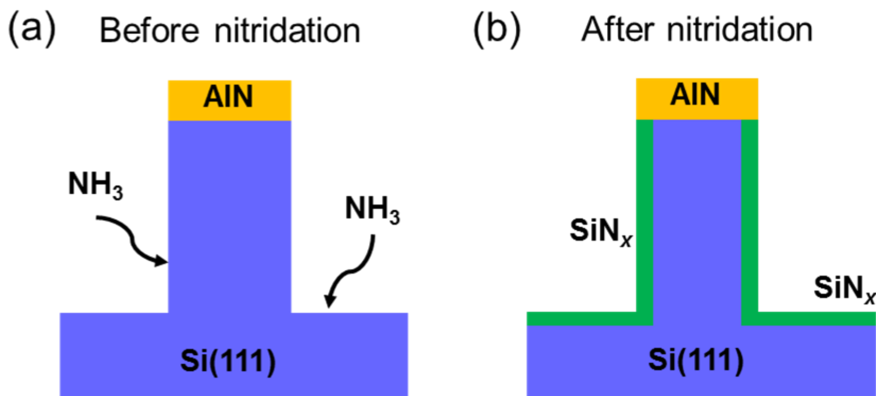


Figure 3.10. AlN/Si(111) nanorods (a) before and (b) after the *in-situ* nitridation step.

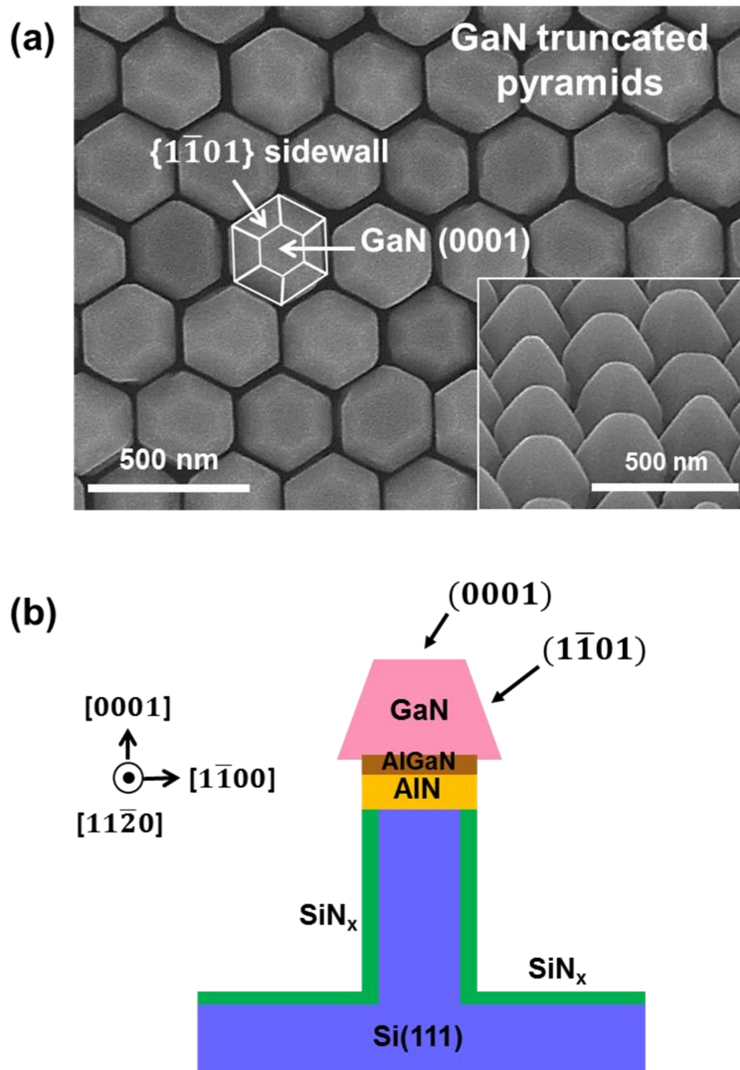


Figure 3.11. (a) Plan-view SEM image of GaN grown on the AlN/Si(111) nanorods after 3 min growth with an inset showing the bird's-eye-view image and (b) structural configuration of GaN island on the AlN/Si(111) nanorod from a cross-section view.

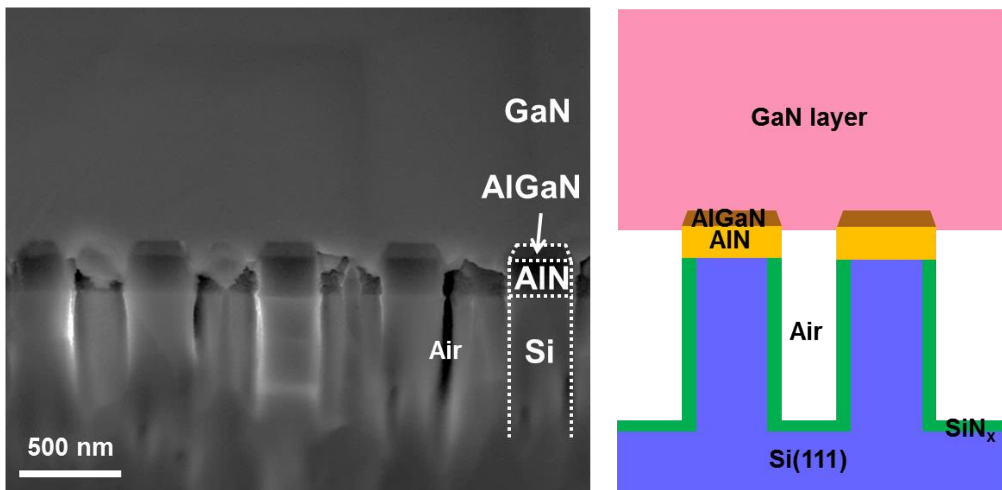


Figure 3.12. Cross-section SEM image of the GaN layer on the AlN/Si(111) nanorods including air voids with the schematics of the corresponding epitaxial structure.

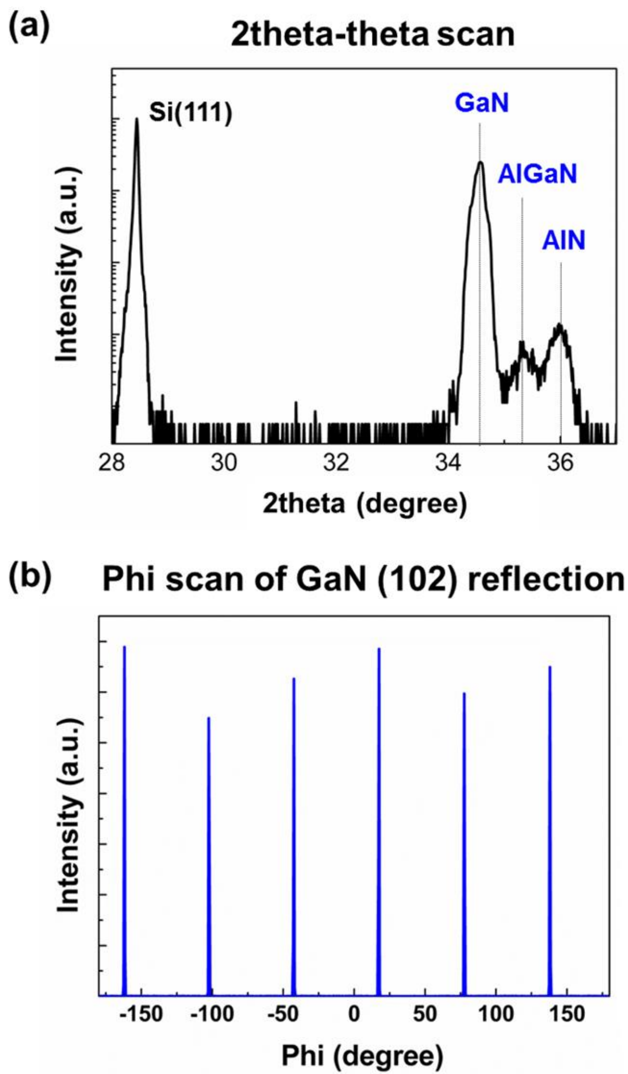


Figure 3.13. (a) 2theta-theta scan and (b) phi scan of the NHE GaN on AlN/Si(111) nanorods using the XRD measurement.

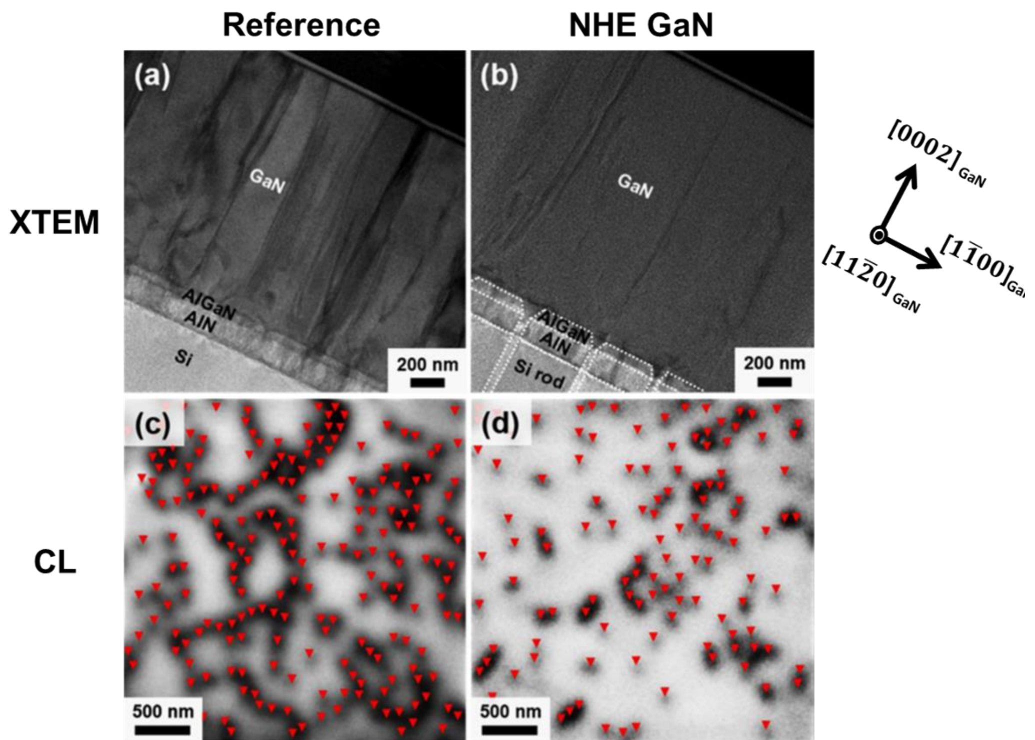


Figure 3.14. Cross-section TEM images of (a) GaN grown on the planar AlN/Si(111) and (b) the NHE GaN grown on the AlN/Si(111) nanorods. Plan-view CL images of (c) GaN grown on the planar AlN/Si(111) and (d) the NHE GaN.

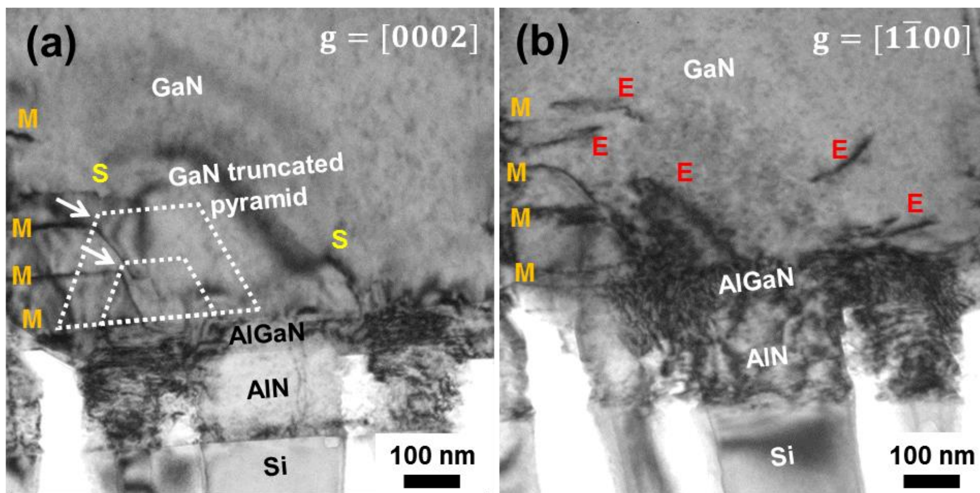


Figure 3.15. High-magnification TEM images taken at the interfacial area between GaN and Si in the NHE GaN showing the bending of threading dislocations with (a) $g = [0002]$ and (b) $g = [1\bar{1}00]$.

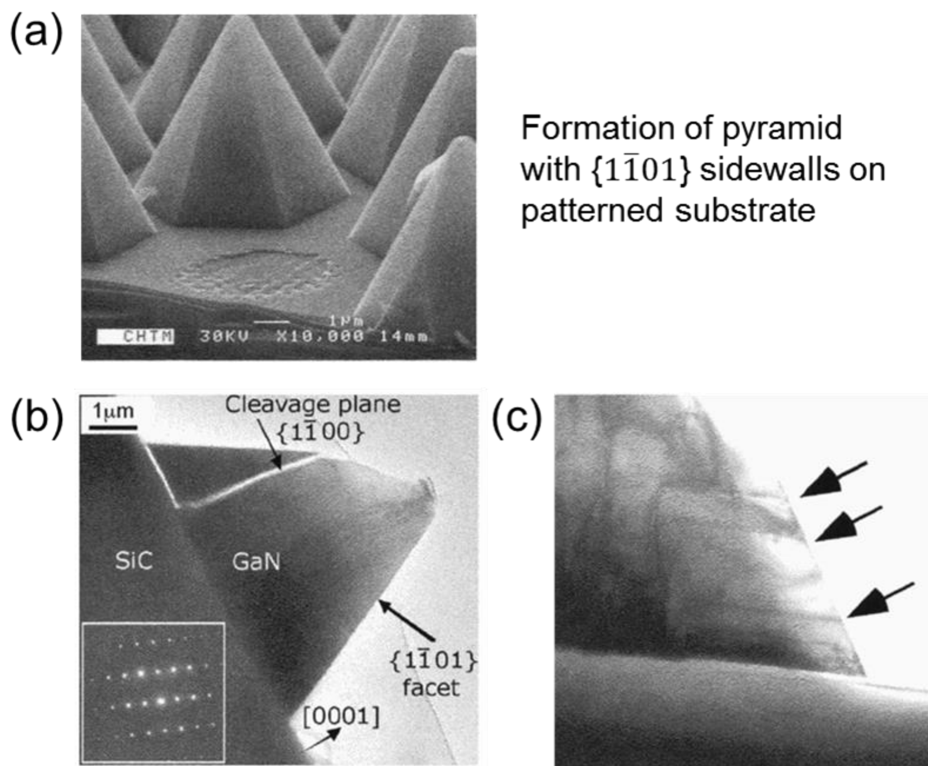


Figure 3.16. Formation of GaN pyramids with $\{1\bar{1}01\}$ side facets observed by (a) SEM and (b) TEM. (c) TEM observation showing the resultant bending of threading dislocations to the side facets.[23]

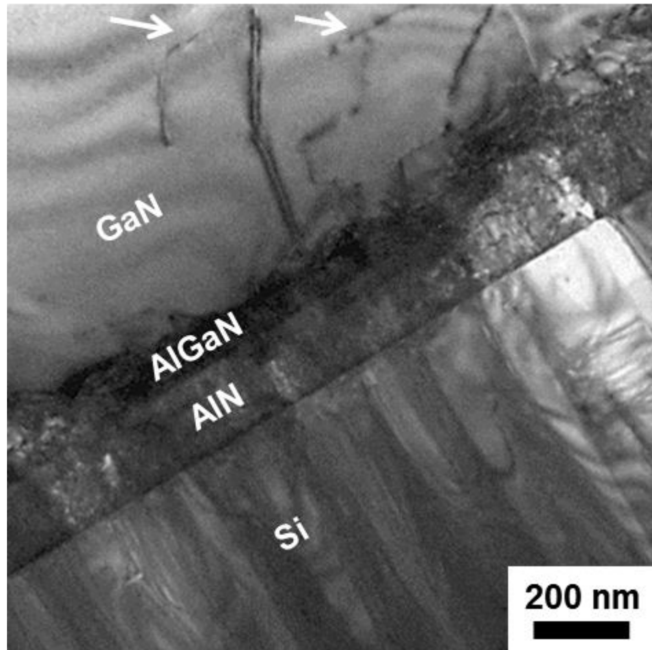


Figure 3.17. TEM image showing the termination of threading dislocation propagation by stacking faults.

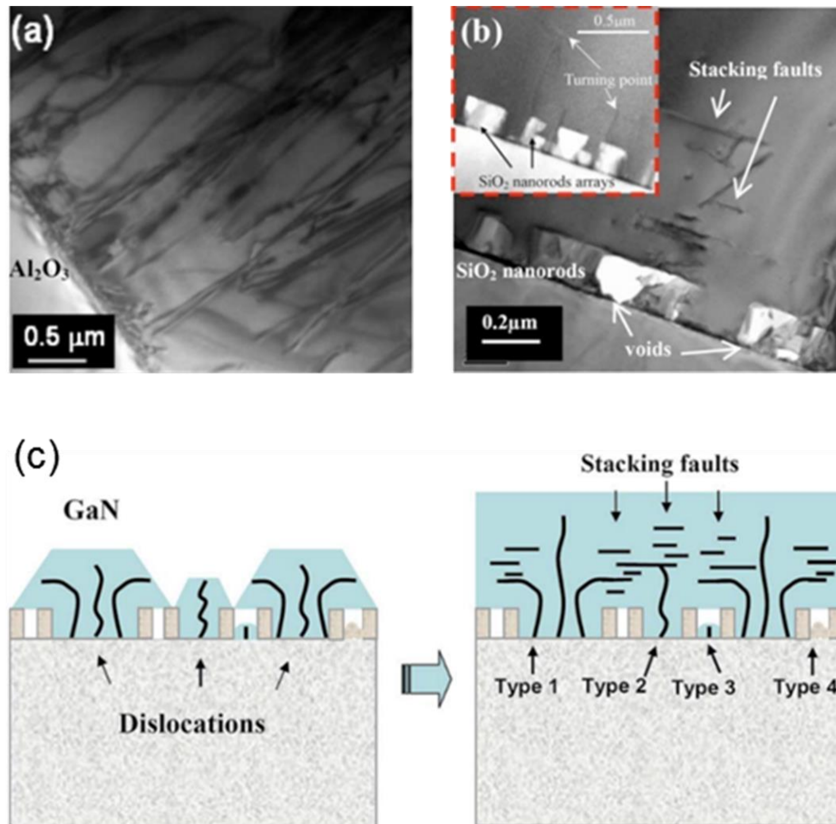


Figure 3.18. Cross-section TEM images of (a) GaN grown on the planar sapphire substrate and (b) GaN grown on the SiO_2 nanorod-patterned sapphire substrate. (c) Schematics describing the formation of stacking faults in GaN grown on the nano-patterned substrate.[24]

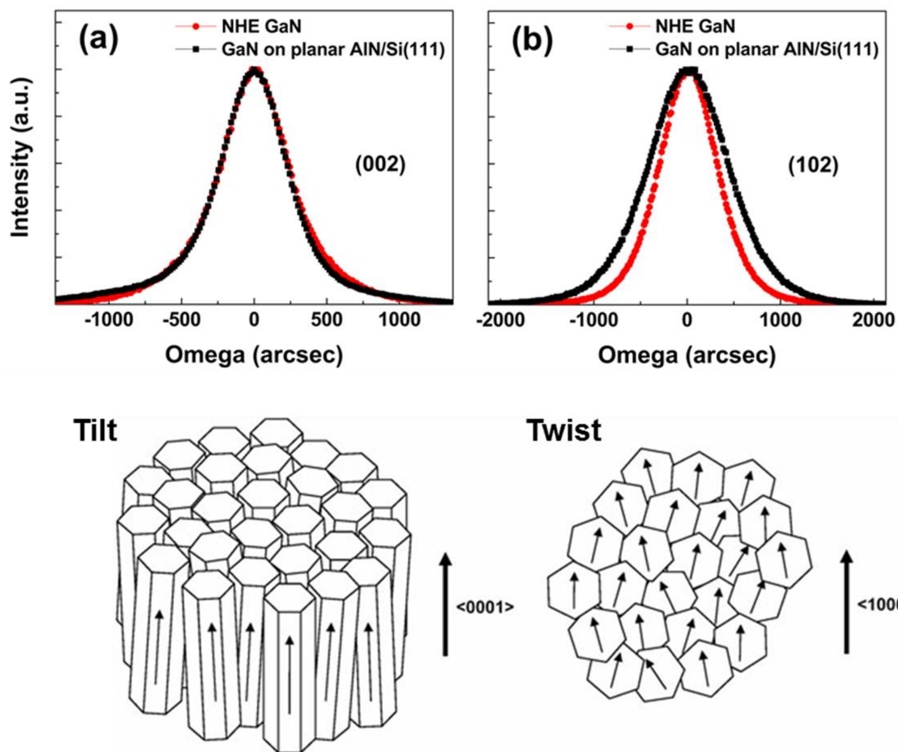


Figure 3.19. XRD omega rocking curves of the NHE GaN and GaN on the planar AlN/Si(111) from (a) (002) plane and (b) (102) plane.

3.3.3 Effect of nano-patterned substrate on GaN-on-Si structure

Micro-Raman spectroscopy was used to evaluate the residual stress in the GaN films. Fig. 3.20 shows the E_2 (high) mode peaks in micro-Raman spectra of the two GaN layers grown on the AlN/Si(111) nanorods and the planar AlN/Si(111), and a thick free-standing GaN crystal of a 200 μm thickness grown by hydride vapor phase epitaxy. The peaks were centered at 566.7, 565.2, and 567.3 cm^{-1}, respectively. The red shift of the peaks for the epitaxial GaN layers from that for the free-standing GaN crystal indicates that tensile stress was built in the GaN films.[25] Based on the shift of the E_2 (high) mode peak, the tensile stress in the GaN films can be obtained by a linear relation as follow:[26]

$$\sigma_{xx} = \frac{\Delta\omega}{4.3} cm \cdot GPa$$

where $\Delta\omega$ and σ_{xx} represent the peak shift and the residual stress, respectively. According to the equation, the residual tensile stresses were calculated to be 0.14 and 0.49 GPa for the NHE GaN and the GaN layer grown on the planar AlN/Si(111), respectively. This indicates the 70% reduction of the tensile stress for the NHE GaN by introducing the AlN/Si(111) nanorod structure forming air voids between them. It was suggested that air voids between nanorods facilitated a three dimensional stress relief mechanism, resulting in the reduction of the tensile stress.[17]

Fig. 3.21 shows low-temperature PL spectra of the samples measured at 20 K. The peaks corresponding to the near band edge emission were located

at 357.1 nm and 358.1 nm for the NHE GaN and the GaN layer on the planar AlN/Si(111), respectively. The blue shift of the emission wavelength indicates that the residual stress in the GaN films grown on the AlN/Si(111) nanorod structure was relaxed[27] which is in good agreement with the micro-Raman result. Besides, it was observed that the integrated PL intensity of the NHE GaN was much higher than that of GaN on the planar AlN/Si(111). We consider that most part of the enhancement is attributed to the strong light scattering by the pattern, but we also expect that the improvement in the crystalline quality of the GaN layer on the AlN/Si(111) nanorod structure such as the reduction of dislocation density could contribute to the PL improvement.

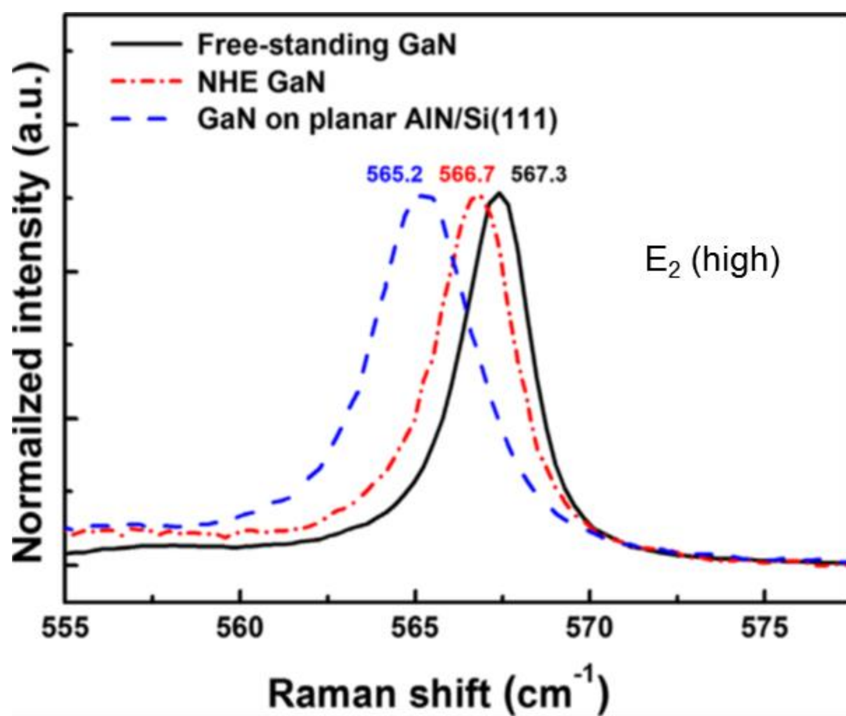


Figure 3.20. Micro-Raman spectra of the NHE GaN, GaN on the planar AlN/Si(111), and the free-standing GaN crystal.

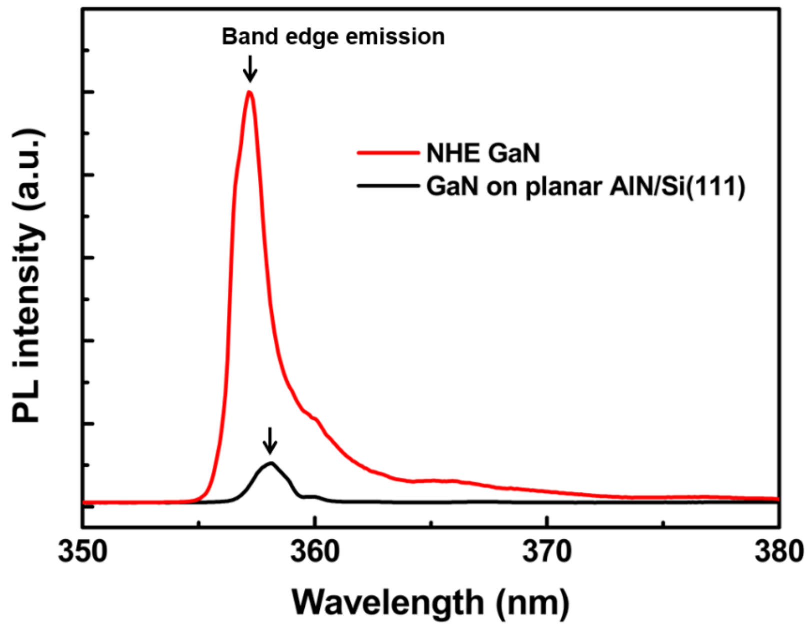


Figure 3.21. Low-temperature (20 K) PL spectra of the NHE GaN and GaN grown on the planar AlN/Si(111).

3.4 Summary

NHE of GaN on the AlN/Si(111) nanorod structure was investigated by using MOCVD. Silica nanosphere lithography was employed to fabricate the periodic hexagonal nanorod array with a narrow gap of 30 nm between the nanorods. Fully coalesced GaN film was obtained over the nanorod structure and its TDD was found to decrease down to half, compared to that of GaN grown on the planar AlN/Si(111) substrate. TEM measurement revealed that TD bending and TD termination by stacking faults occurred near the interface between GaN and AlN/Si(111) nanorods, contributing to the TDD reduction. Moreover, the 70% relaxation of the tensile stress of the NHE GaN was confirmed by micro-Raman and PL measurements compared to GaN on the planar AlN/Si(111) substrate. These results suggested that NHE on AlN/Si(111) nanorods fabricated by nanosphere lithography is a promising technique to obtain continuous GaN films with the improved crystalline quality and the reduced residual stress.

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Chapter 4. AlGaN-based deep ultraviolet light-emitting diode on nano-patterned AlN/sapphire substrate

4.1 Introduction

AlGaN-based deep ultraviolet (DUV) LEDs have attracted much attention due to their various applications such as water purification, sterilization, curing, and bio-agent detection as shown in Fig. 4.1.[1] A spectrum of light is categorized into regions such as visible, UV, and IR with respect to the wavelength of the light as shown in Fig. 4.2. The UV region is further divided into several regions: near UV (300 − 400 nm); DUV (200 − 300 nm); and vacuum UV (10 − 200 nm). Recently, DUV light has attracted much interest for environmental applications due to its high photon energy. DUV light interacts with the deoxyribonucleic acid (DNA) structure of microbiological contaminants such as bacteria and virus, disrupting their DNA. As a result, the replication of microorganisms is prevented by DUV light. The emission wavelength of optical devices is determined by the bandgap of the nitride semiconductors composing the active layer. AlGaN-based LEDs can emit from 200 nm (AlN) to 365 nm (GaN), thus AlGaN with high Al content have been used to fabricate DUV LEDs as showin in Fig. 4.B. In addition, there are advantages of AlGaN-based DUV LEDs in in size, spectral control, and Hg-free operation compared to the conventional Hg-vapor lamp. According to the *Yole development* (2016), DUV LED market

will grow from 7 million dollars in 2015 to 610 million dollars by 2021 with a compound annual growth rate (CAGR) of 210 during the period.[2]

However, the external quantum efficiency (EQE) of AlGaN-based DUV LEDs (typically less than 10% for 280 nm LEDs) is much lower than that of InGaN-based visible LEDs (60% for 450 nm blue LEDs) due to intrinsic material properties of AlGaN which lead to poor internal quantum efficiency (IQE) as well as LEE.[3,4] Fig. 4.3 shows the typical AlGaN-based DUV LED structure. The DUV LED consists of AlN layer, n-AlGaN layer, MQW, p-AlGaN layer, p-GaN contact layer, and electrodes. Increasing the Al composition x in $Al_xGa_{1-x}N$ for the emission of deeper UV photons generally leads to a high density of extended defects such as threading dislocations and cracks due to large lattice mismatch and thermal mismatch between the AlGaN epitaxial layer and foreign substrates as well as the low surface mobility of Al-containing alloys. These extended defects are known to act as non-radiative recombination centers, thus cause low IQE.[5-7] In addition, the LEE of AlGaN-based DUV LEDs is severely limited due to strong absorption of DUV photons by top p-type GaN contact layer and light trapping by total internal reflections particularly for the strong anisotropic transverse-magnetic polarized emission from the AlGaN active region.[8,9] As a result, the EQE of AlGaN-based DUV LED is limited to 20% due to both low IQE and low LEE as shown in Fig. 4.4. The EQE of the LED decreases sharply as the Al content in AlGaN increases as shown in Fig. 4.5.

Since the EQE is determined by both IQE and LEE, in order to overcome such significant limitations in EQE, thus, to realize highly efficient DUV LEDs, it is essential to enhance the IQE by realization of high quality AlGaN epitaxial layers and the LEE simultaneously.

Figure 4.1. DUV LED for healthier living environment.

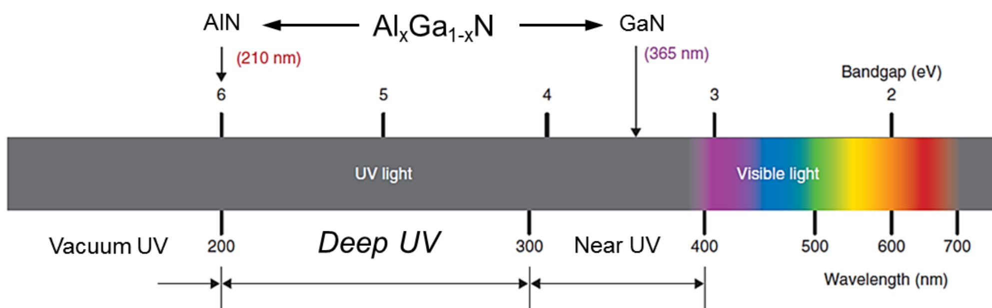


Figure 4.2. AlGaN for UV-emitting devices.

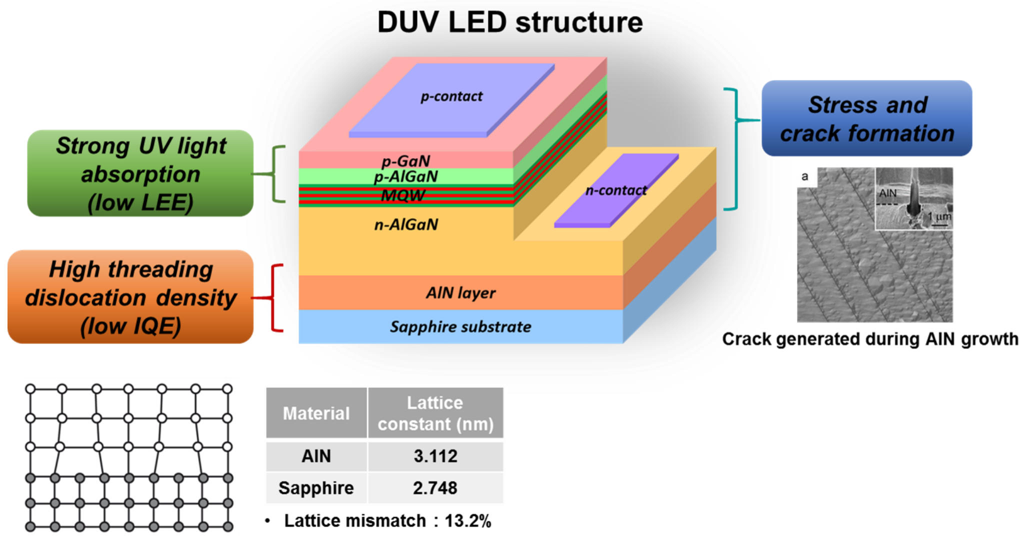
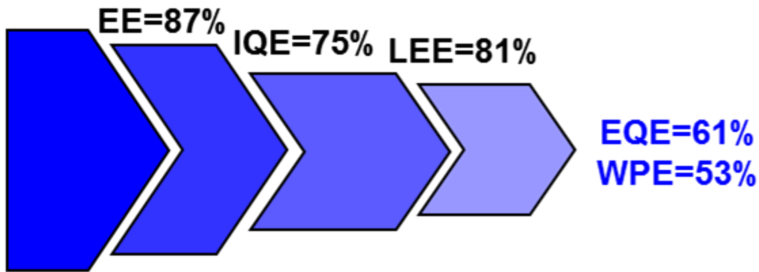


Figure 4.3. Structure of AlGaN-based DUV LED and issues of DUV LEDs.

▪ InGaN-based Blue LED (450 nm)



▪ AlGaN-based DUV LED (250 nm)

Figure 4.4. Flow chart of losses during operation of InGaN-based blue LEDs (450 nm) and AlGaN-based DUV LEDs (250 nm).[3]

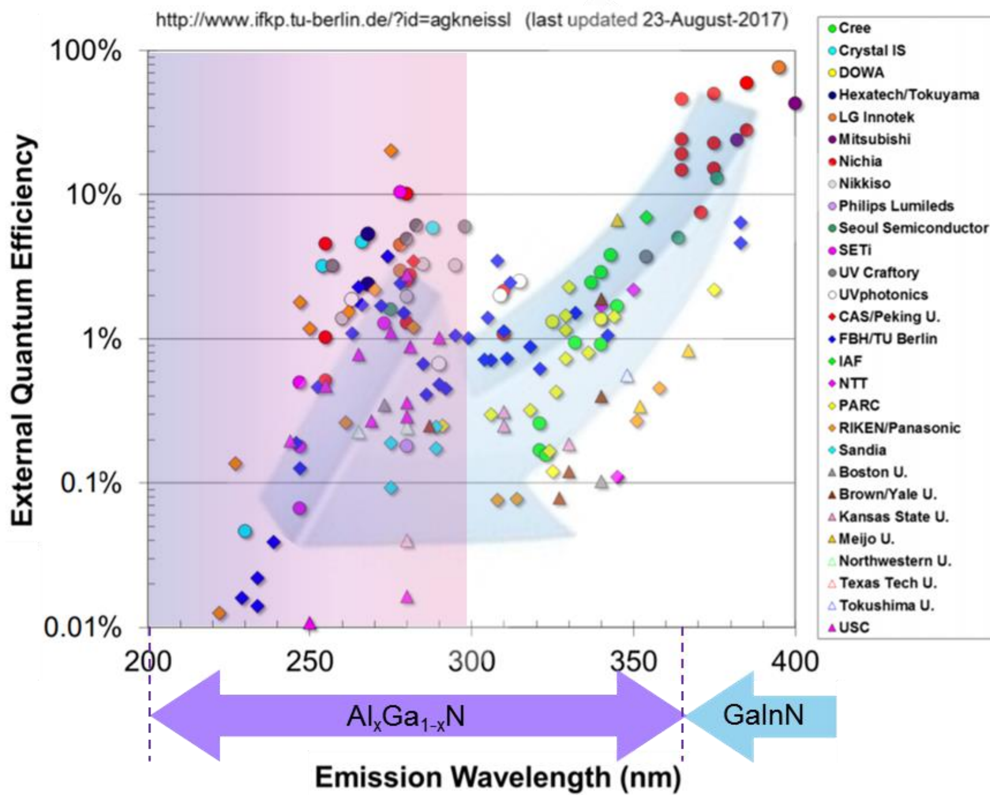


Figure 4.5. EQE of AlGaN-based UV LEDs by different research groups.

4.1.1 Growth of $Al_xGa_{1-x}N$ layer on patterned substrate

PSS is a universal technology used in GaN-based LED structures to improve the crystal quality and increase the LEE at the same time, as described above. However, in the case of AlN growth, the ELO mechanism is not possible. Fig. 4.6 shows our growth result of AlN on PSS with the growth temperature of 1050 ^{o}C using MOCVD. When AlN is grown on the PSS, the AlN is not a single crystal but a polycrystal because there is no growth selectivity between the growth mask (pattern) and the growth window due to the small diffusion length of Al adatoms.

Several growth techniques such as migration-enhanced epitaxy[10] and multilayer-AlN buffer growth by NH_3 pulse-flow method[11] have been reported to reduce the TDD in AlN on sapphire by enhancing the surface migration of Al-species.[10,11] ELO on microscale patterned sapphire substrates and AlN/sapphire substrates has been investigated, demonstrating the reduction of TDD and the enhancement of the light output power (LOP) of UV LEDs.[12-16] ELO of AlN on the patterned substrates, high quality AlN layers with low defect density was obtained as shown in Fig. 4.7.[17] However, ELO on microscale patterned substrates requires high growth temperature above 1300 ^{o}C for enough surface migration of Al adatoms as well as a long growth time for the coalescence of AlN over the wing region as shown in Fig. 4.8, thus high cost.[18] Recently, Dong *et al.* suggested nanoscale ELO of AlN on nano-patterned sapphire substrates at the growth temperature of 1200 ^{o}C to reduce the coalescence gap as well as to increase the light scattering, and have achieved an enhanced EQE.[19] Conroy *et al.* also have reported nanoscale ELO of AlN on uniform array of 1 μm-thick AlN nanorods on

sapphire substrate at the growth temperature of 1100 ^{o}C showing an improved crystal quality of the overgrown AlN films.[20] Although thinner coalescence thicknesses and high quality AlN layers were accomplished by the nanoscale ELO, careful consideration should be given to the effect of nanoscale patterns and resultant formation of a periodic refractive-index contrast between the AlN layer and air on the extraction of DUV photons, thus, on the EQE in order to further improve the efficiency of DUV LEDs.

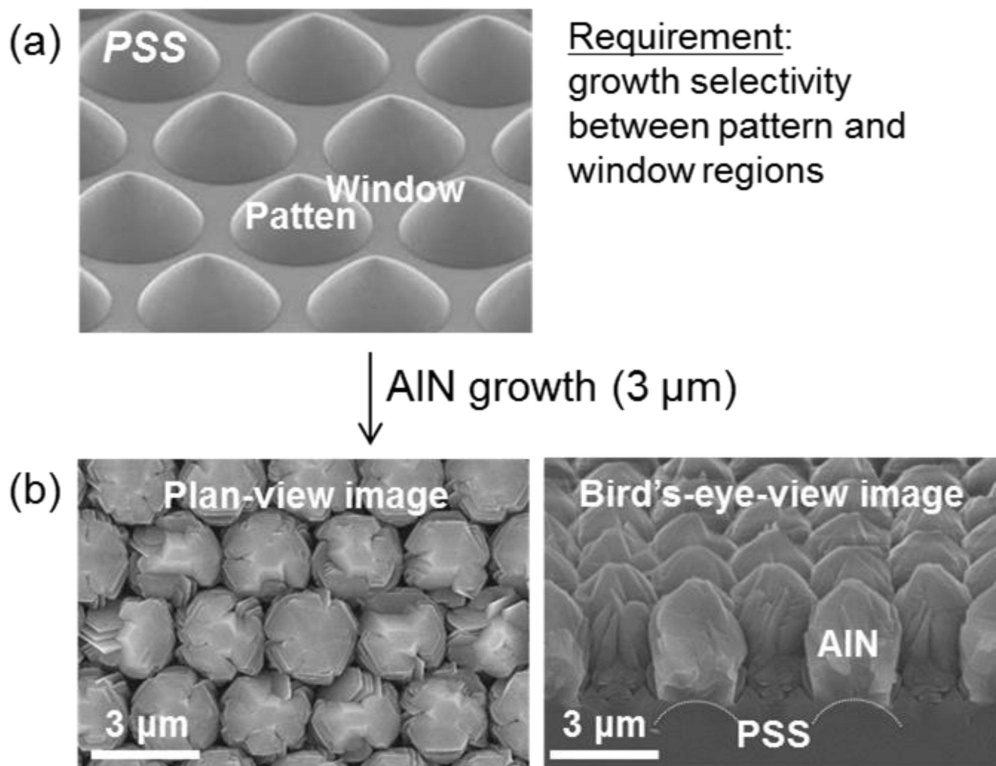


Figure 4.6. (a) PSS and (b) SEM images of poly-crystalline AlN grown on the PSS.

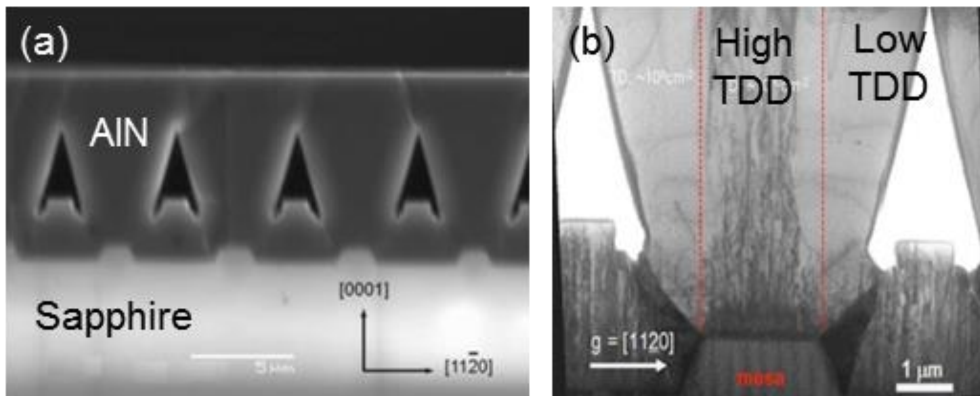


Figure 4.7. (a) AlN grown on the patterned substrate using pulsed growth mode and (b) cross-section TEM image of the overgrown AlN showing reduced density of TDD over wing regions.[17]

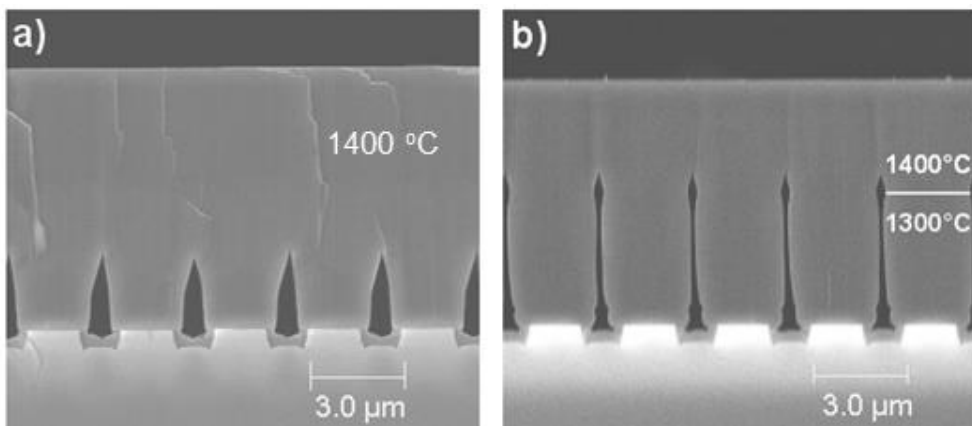


Figure 4.8. High-temperature growth of AlN with (a) 1-step growth at 1400 ºC and (b) 2-step growth at 1300 ºC and 1400 ºC.[18]

4.1.2 Technique for enhancing LEE

Conventional LEE-enhancing techniques such as reflective electrodes,[21] surface roughening,[22,23] and anti-reflection coating[24] are known to be effective for InGaN-based visible LEDs, but less effective for AlGaN-based DUV LEDs due to the strong DUV light absorption in the p-type GaN layer and the difference in intrinsic material properties.[9,25]

The main key to enhance the LEE of DUV LEDs which have typically flip-chip configurations for better light extraction and heat dissipation[26] is to extract the DUV photons through the sapphire substrate effectively before the photons being absorbed in the device structures by reducing the photon path length for extraction. Khizar *et al*. reported an enhancement of LEE of DUV LEDs by introducing microlenses on the sapphire substrates as shown in Fig. 4.9(a).[27] An enhancement of LEE by 55%, which is shown in Fig. 4.9(b), is attributed to the reduced total internal reflection on the light. In addition to the sapphire substrate roughening, patterning of AlN substrates is also effective to improve the LEE of DUV LEDs. Inoue *et al*. have demonstrated the enhancement of LEE by fabricating AlN nanostructures on the transparent AlN substrates as shown in Fig. 4.10.[28]

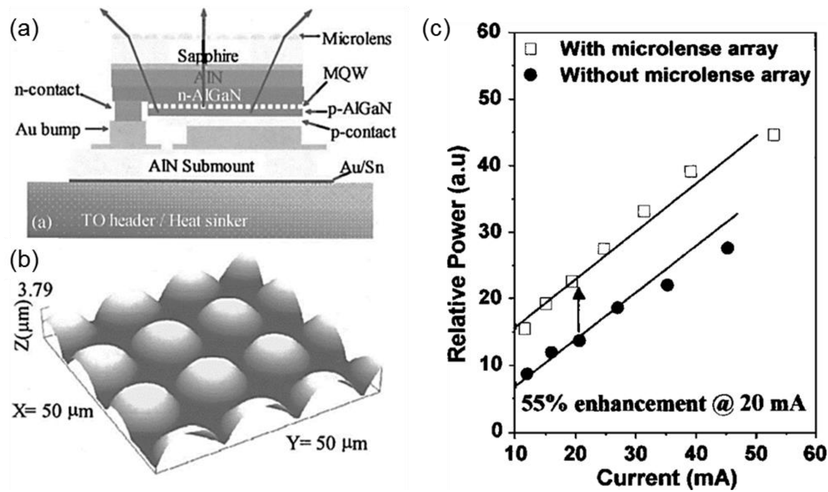


Figure 4.9. Microlense on the sapphire substrate for enhancing the LEE of DUV LED. (a) Schematics of microlense patterned DUV LED, (b) AFM image showing the surface of microlense, and (c) LOPs of DUV LEDs with and without microlense array.[27]

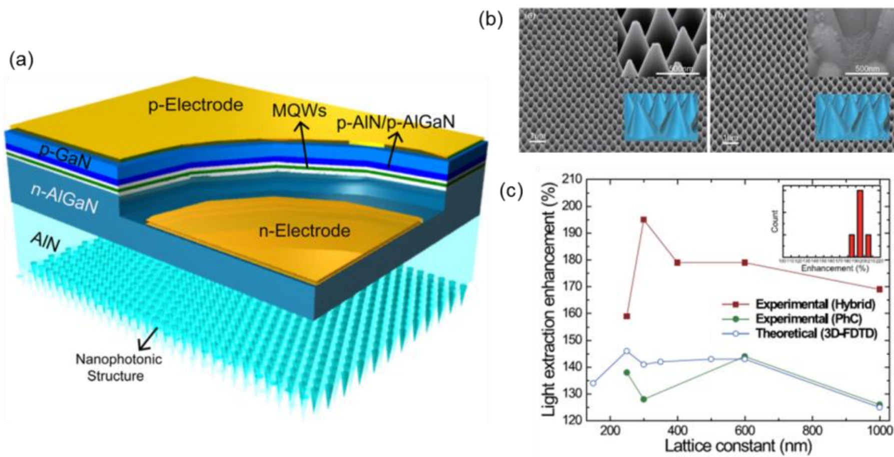


Figure 4.10. (a) Schematics showing photonic crystals on AlN substrate, (b) SEM images of the fabricated photonic crystal, and (c) LEE enhancement from the experimental and theoretical results.[28]

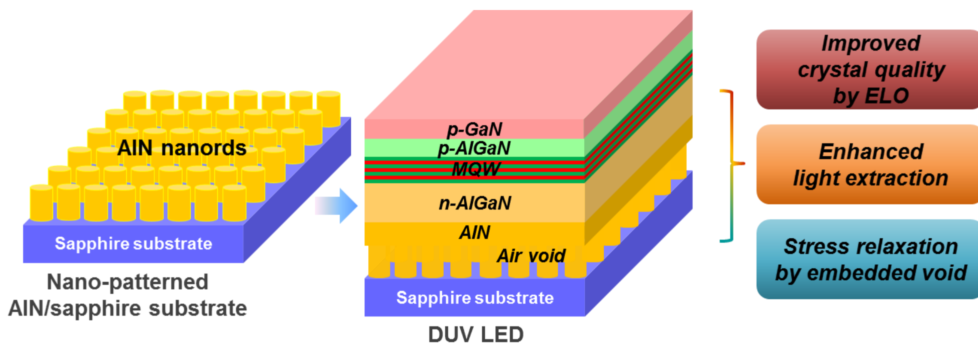
4.2 Experimental procedure

When nano-patterned substrate is applied to the growth of AlN, nanoscale ELO is possible. In this case, improvement of crystal quality can be achieved through ELO, and a rapid coalescence of AlN at relatively low growth temperature is possible even for nitrides containing high Al content. The advantage is that the reduction of both growth thickness and growth temperature for ELO of AlN can directly lead to much reduced manufacturing cost. In addition, air voids are inserted in the final epitaxial structures, which are expected to play a role of relaxing the stress of the film and improving the LEE. This is the motivation for the epitaxial growth of AlN on the nano-patterned substrates, as summarized in Fig. 4.11.

Fig. 4.12 is a schematic fabrication process of AlGaN-based DUV LEDs on nano-patterned AlN/sapphire substrates. A monolayer of self-assembled silica nanospheres was coated on the AlN layer by spin coating. The silica nanospheres were synthesized by the Stöber method[29] and the diameter was 700 nm. To transfer the nanosphere pattern to the underlying AlN layer, Cl_2-based RIE was carried out. The residual silica nanospheres after the etching were cleaned by dipping the substrate in hydrofluoric acid (HF). The fabricated NPS was loaded again into the MOCVD reactor and AlN layer was grown on top of the AlN nano-patterns. ELO of AlN on the NPS was performed at a growth temperature of 1050 ^{o}C.

An $Al_{0.43}Ga_{0.57}N/Al_{0.58}Ga_{0.42}N$ multiple-quantum well (MQW) DUV LED was grown on the NPS with a 3 μm-thick AlN buffer layer. The DUV LED consists of AlN/AlGaN superlattice buffer layers, a 2.4 μm-thick Si-doped n-type $Al_{0.58}Ga_{0.42}N$ layer, five periods of MQWs composed of 2 nm-

thick $Al_{0.43}Ga_{0.57}N$ quantum wells and 10 nm-thick $Al_{0.58}Ga_{0.42}N$ quantum barriers, a 15 nm-thick Mg-doped $Al_{0.8}Ga_{0.2}N$ electron blocking layer, a Mg-doped p-type AlGaN cladding layer with a graded Al composition from 58% to 0%, and a 200 nm-thick Mg-doped p-type GaN contact layer. For a reference, AlN layer and DUV LED were also grown on a planar AlN template without the patterning in the MOCVD reactor. TMAl, TMGa, and NH_3 were used as the sources of Al, Ga, and N, respectively. The structural characteristics were analyzed by field-emission SEM, AFM, and OM. The crystal quality was examined by XRD.



Nanoscale ELO	➢ Improved crystal quality ➢ Fast coalescence: reduced growth temperature and time
Air void embedment	➢ Relaxed film stress ➢ Enhanced light extraction

Figure 4.11. Motivation for the introduction of nano-patterned substrate for highly efficient AlGaN-based DUV LEDs.

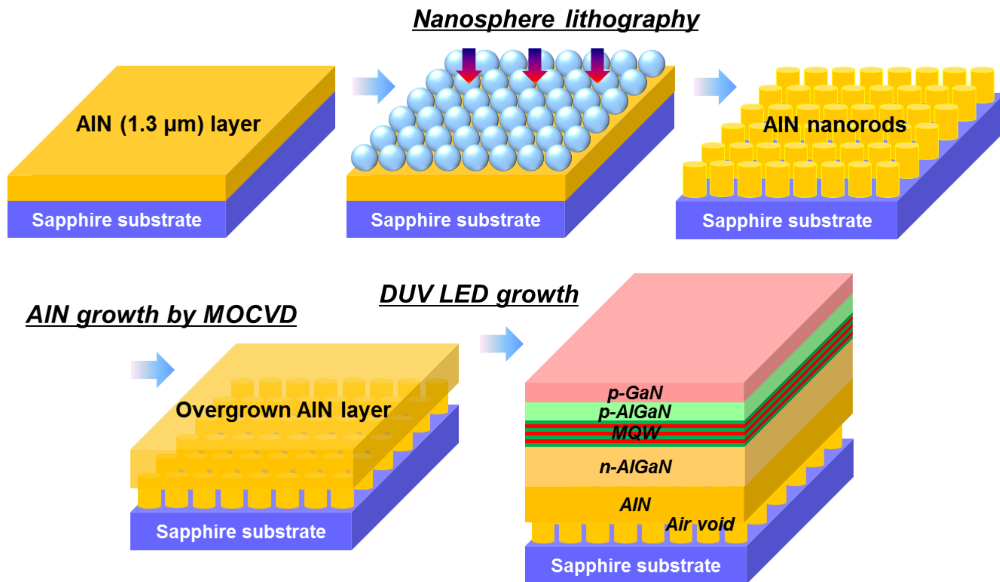


Figure 4.12. Schematics showing the fabrication process flow of AlGaN-based DUV LEDs on nano-patterned AlN/sapphire substrates.

4.3 Results and discussion

4.3.1 Fabrication of nano-patterned AlN/sapphire substrate

A 1.3 μm-thick AlN layer was grown on a 4-in. c-plane sapphire substrate (0.35° miscut toward the m-plane) by an Aixtron G3 MOCVD system. In order to obtain a flat surface of AlN and suppress parasitic reactions between TMAl and NH_3, V/III ratio was lowered to ~160 for AlN growth. Then, silica nanosphere lithography technique was employed to fabricate the NPS. The silica nanospheres with average diameter of 700 nm were synthesized by the Stöber method. Self-assembled silica nanospheres as etch masks were coated on the AlN layer uniformly over the 4-in. wafer by spin coating. Fig. 4.13 shows the coating results measured by SEM images for three locations at different distances from the center of 4-in. substrate. Although there are defects in the silica nanosphere array such as grain boundaries and vacancies, monolayer of hexagonal silica nanosphere array was obtained on the 4-in. sapphire substrate.

Then, Cl_2-based reactive ion etching was carried out to transfer the nanosphere pattern to the underlying AlN layer. RF power, chamber pressure, and Cl_2 flow rate were fixed to 200 W, 50 mTorr, and 16 sccm, respectively. With increasing the etching time, the shapes of the AlN and silica nanospheres were investigated. Fig. 4.14 shows plan-view and cross-section SEM images of AlN nanostructures as a function of the etching time. As expected, the shrinkage of the silica nanospheres was proceeded as the etching time increased. As a result, the diameter of the fabricated AlN nanorods decreased and the height of the AlN nanorods increased with the

increased etching time. During the RIE process, AlN was etched by chemical reaction with reactive ions by forming volatile aluminum chloride gas ($AlCl_3$), while silica nanospheres are etched by physical sputtering. The one step Cl_2-based RIE enabled us to fabricate AlN nanorods on the sapphire substrate.

The residual silica nanospheres after the etching were cleaned by dipping the substrate in HF. Fig. 4.15(a) and 4.15(b) are plan-view and bird's-eye-view SEM images of the fabricated NPS. A well-defined hexagonal array of AlN nanorods with c-plane flat top surfaces on the sapphire substrate was obtained after the nanosphere lithography. The resultant diameter and height of nanorods with the etching time of 30 min were measured to be ~630 nm and 1.3 μm, respectively. The air spacing between the nanorods along the center-to-center direction was about 130 nm, which was small enough to enable the coalescence of overgrown AlN layers on the nanorods overcoming the limited surface migration of Al adatoms.

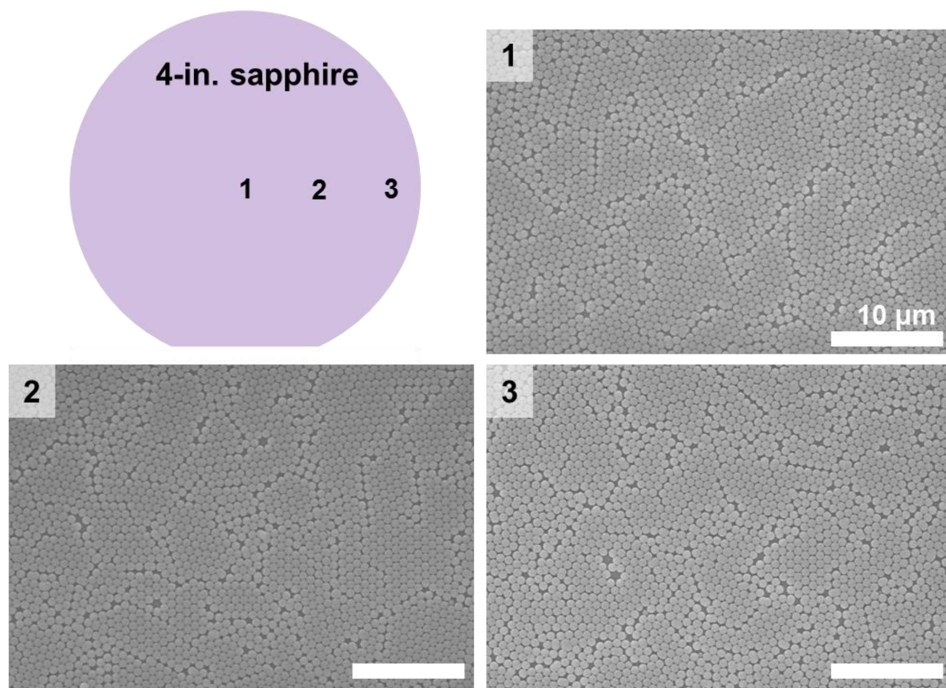


Figure 4.13. Spin coating results showing self-assembled silica nanospheres on AlN/sapphire template at different positions in 4-in. sapphire substrate.

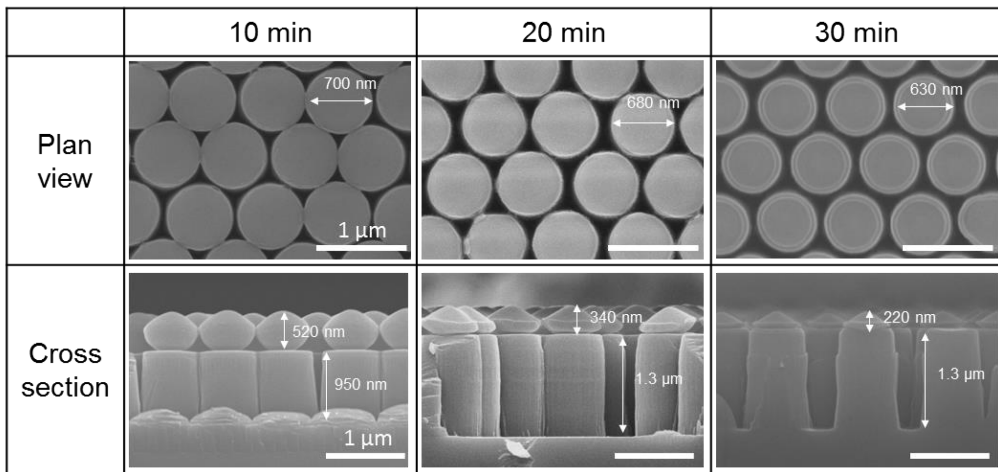


Figure 4.14. Plan-view and cross-section SEM images of AlN nanostructures as a function of Cl_2-based RIE time.

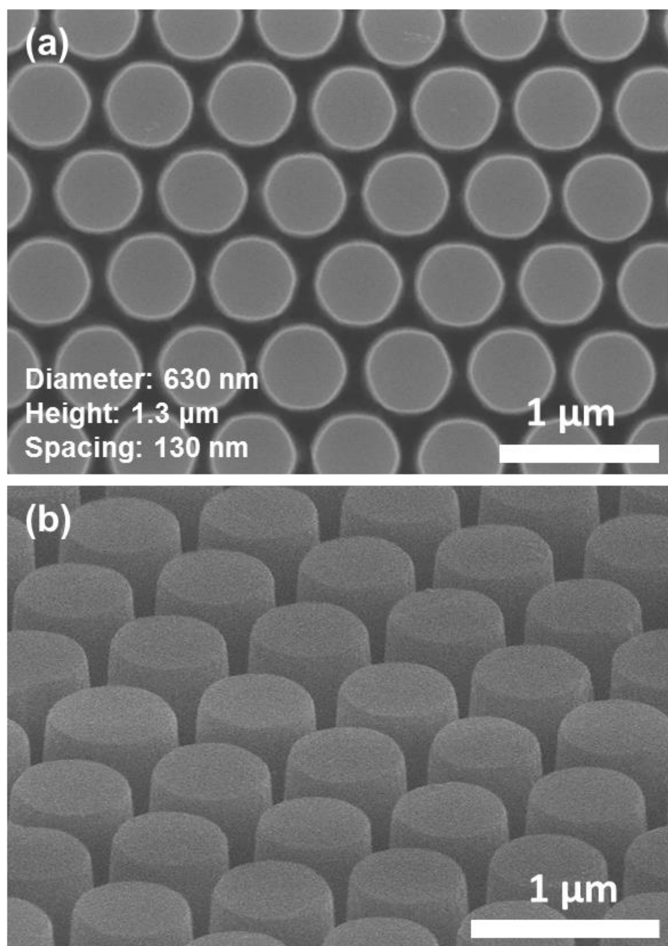


Figure 4.15. (a) Plan-view and (b) bird's-eye-view SEM images of well-defined AlN nanorods fabricated by silica nanosphere lithography.

4.3.2 Growth of $Al_xGa_{1-x}N$ layers on nano-patterned AlN/sapphire substrate

The NPS was loaded again into the MOCVD reactor to grow AlN layer on it. ELO of AlN on the NPS was performed at a growth temperature of 1050 °C, which is much lower than that for microscale ELO (1300-1400 °C)[12-16] and even lower than that for former nanoscale ELO (1100-1200 °C).[19,20] The surface temperature of the MOCVD susceptor, defined as the growth temperature in this study, was measured by a pyrometer. Growth conditions for ELO of AlN were the same as those used for the growth of AlN layer on the planar sapphire substrate. No pulsed growth mode was used for AlN on NPS. For a comparative study, reference AlN was grown on the planar AlN layer at the same time. Fig. 4.16 shows the structure of AlN layer grown on the NPS characterized by SEM and AFM. Fig. 4.16(a) and 4.16(b) are cross-section and plan-view SEM images of the 5.2-μm thick AlN layer overgrown on the NPS. Note that, despite the much lower growth temperature, the AlN completely coalesced within ~200 nm overgrowth, indicating much faster coalescence compared to the previous microscale ELO results, [12-16] thanks to the ELO of AlN on nanoscale patterns as reported in the previous results.[19,20] The coalescence thicknesses with the spacing of the patterned substrates with different researches are summarized in Fig. 4.17. The reduction of both growth temperature and growth thickness for ELO of AlN by introducing the NPS can directly lead to much reduced manufacturing cost. In addition, air voids surrounding the AlN nanorods were formed periodically between the overgrown AlN layer and the sapphire substrate as a result of the ELO of AlN on top of the nanorods. It is expected that the embedded air voids can (i)

relieve the stress of the AlN film by reducing the contact area between the epitaxial layer and the underlying substrate, as well as (ii) make a periodic refractive-index contrast between air and AlN. Fig. 4.16(b) shows a fully coalesced top surface of the AlN layer. Zigzag macro-steps along $[1\bar{1}00]_{AlN}$ observed on the SEM image and also identified by AFM image shown in Fig. 4.16(c) originate from the miscut of the sapphire substrate, as reported previously.[30] Fig. 4.18 shows OM images of reference AlN grown on the planar AlN template without patterning and AlN grown on the NPS, respectively. While there were cracks on the surface of reference AlN, crack-free AlN layers were obtained on NPS over the whole 4-in. wafer. The tensile stress is built up with increasing the thickness of AlN layers during the growth and the accumulated stress leads to the crack formation. The embedded air voids formed in the AlN epitaxial layer effectively released the tensile stress induced in the AlN layer during the growth, so that thick and crack-free AlN layer was grown on the NPS.

To evaluate the crystal qualities of the AlN layers, XRD measurement was carried out. Fig. 4.19(a) and 4.19(b) are X-ray rocking curves of symmetric (002) and asymmetric (102) reflections of AlN layers with normalized peak intensities. The FWHM values of (002) planes were 186 arcsec and 235 arcsec for the AlN on NPS and the reference AlN, respectively. Those of (102) planes were measured to be 432 arcsec and 457 arcsec for the AlN on NPS and the reference AlN, respectively. The reduction of FWHM values of both (002) and (102) reflections indicates that the crystal quality of AlN layers grown on NPS was improved by nanoscale ELO.

An $Al_{0.43}Ga_{0.57}N/Al_{0.58}Ga_{0.42}N$ multiple-quantum well (MQW) DUV

LED was grown on the NPS with a 3 μm-thick AlN buffer layer. Fig. 4.20 is a cross-section SEM image of the LED structure and the total thickness was 7.9 μm. Similarly with the AlN growth result, crack-free DUV LED epitaxial layer was obtained on the NPS while reference showed lots of cracks on the surface.

As shown in Fig. 4.21, the TDD of the DUV LED on NPS is lower than that of the reference DUV LED. TDDs in n-AlGaN layers measured by TEM were 4.4×10^{9} cm^{-2} and 6.0×10^{9} cm^{-2} for the DUV LED and the reference DUV LED, respectively. The reduced TDD indicates the improved crystal quality of AlN and overgrown AlGaN thereon by ELO. In addition to the XRD result for AlN layers, crystal qualities of n-AlGaN layers were analyzed by XRD. FWHM values of (002) planes were 379 arcsec and 490 arcsec for n-AlGaN overgrown on the NPS and reference n-AlGaN, respectively. Those of (102) planes were measured to be 718 arcsec and 759 arcsec for n-AlGaN overgrown on the NPS and reference n-AlGaN, respectively. The reduction of FWHM values of both (002) and (102) reflections indicates the improved crystal quality of n-AlGaN on NPS. Fig. 4.22 is a cross-section TEM image of AlN grown on the NPS with $g = [0002]$. Threading dislocations near the voids were found to bend towards the free surfaces (indicated by arrows). We believe that this dislocation filtering effect contributed to the reduction of TDD in AlN and DUV LED on NPS.

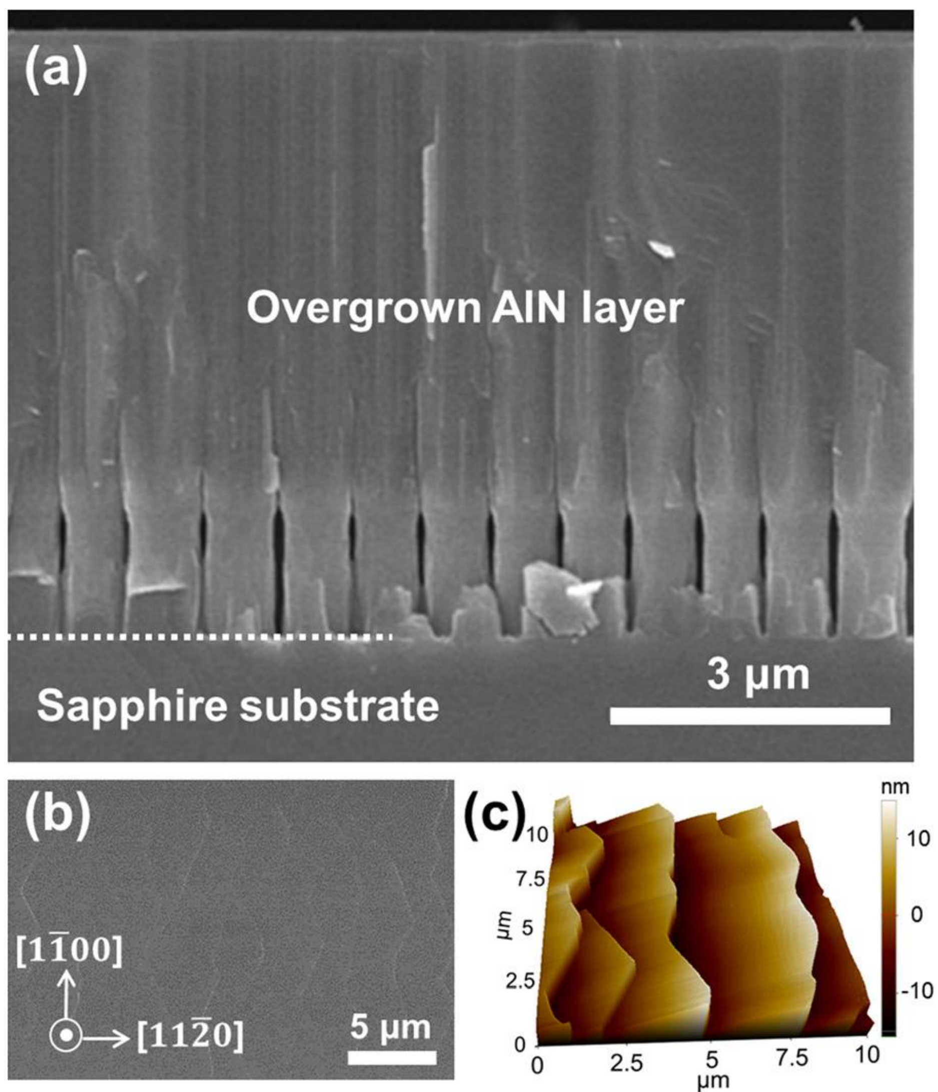


Figure 4.16. Cross-section SEM image of the overgrown AlN layer on the NPS.

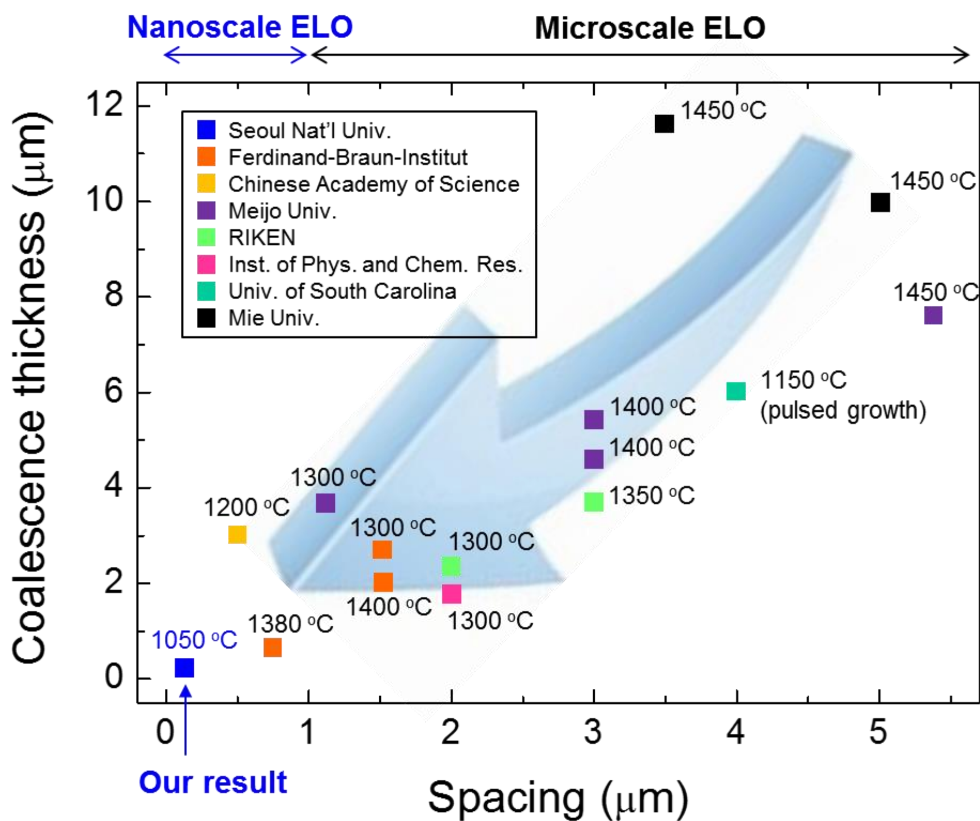


Figure 4.17. Coalescence thickness vs. spacing between the patterned substrates for ELO of AlN. The growth temperature of each result is noted.

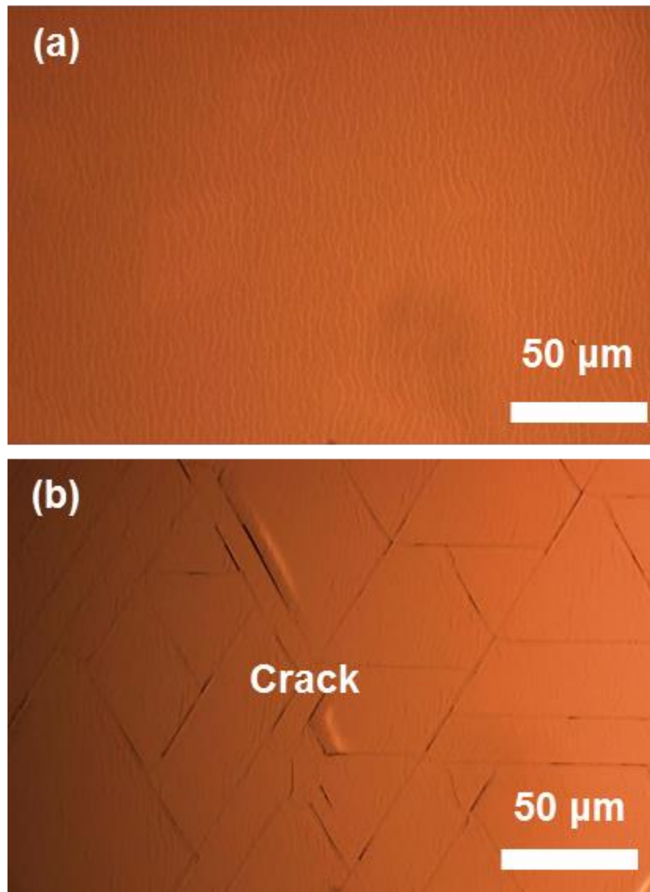


Figure 4.18. OM images of (a) crack-free AlN layer on the NPS and (b) AlN layer on the planar sapphire substrate with lots of cracks on the surface.

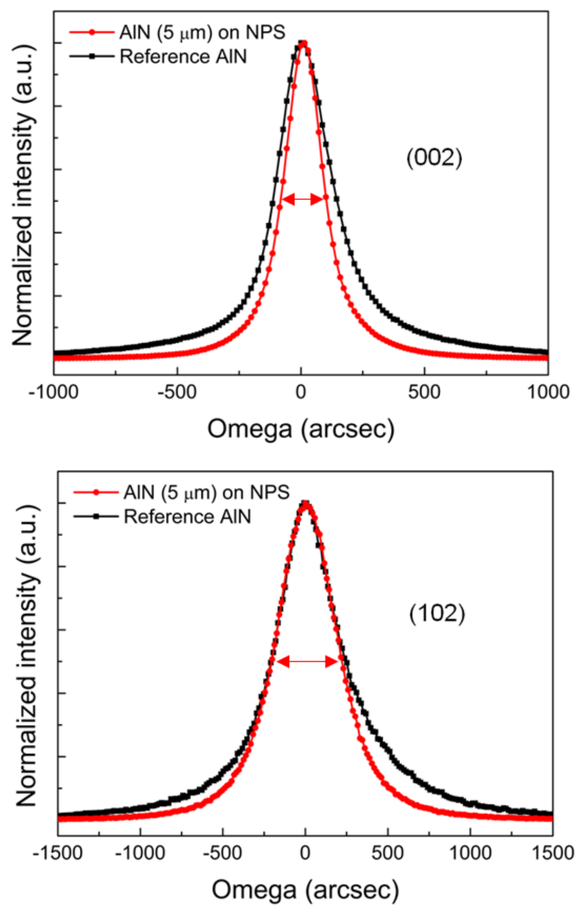


Figure 4.19. XRD omega rocking curves of (a) symmetric (002) and (b) asymmetric (102) reflection of the AlN on the NPS and the reference AlN.

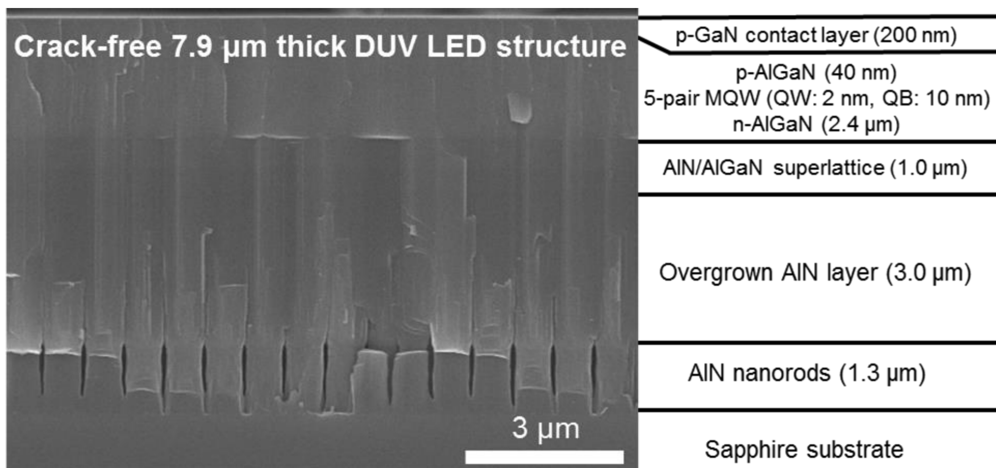


Figure 4.20. Cross-section SEM image of crack-free 7.9 μm-thick DUV LED epitaxial layers grown on the NPS.

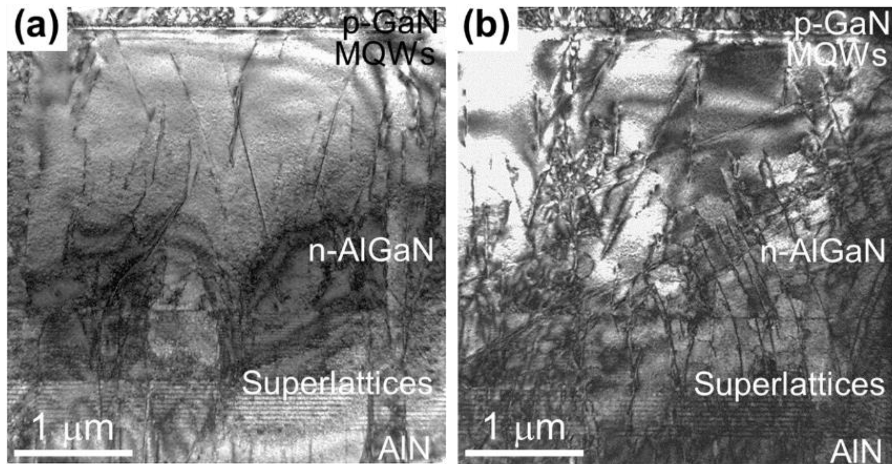


Figure 4.21. Cross-section TEM images of (a) DUV LED on NPS and (b) reference DUV LED taken along $[\mathbf{1}\bar{\mathbf{1}}\mathbf{00}]$ zone axis of AlGaN.

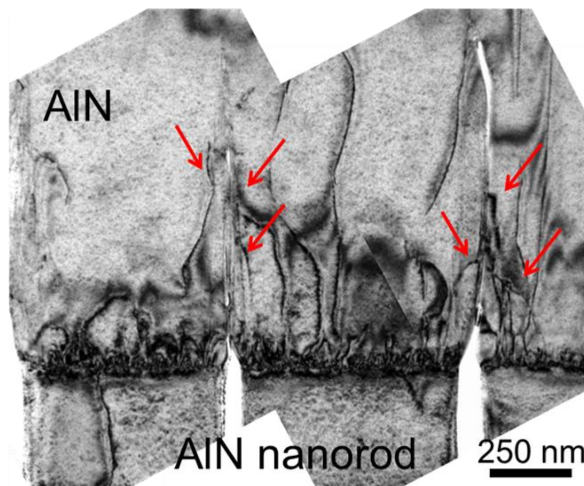


Figure 4.22. Cross-section TEM image of DUV LED on NPS showing the bending of threading dislocations.

4.3.3 Device fabrication and characterization

The DUV LEDs on NPS and the reference DUV LEDs were fabricated with a chip size of 300×300 μm^2 by using conventional GaN-based LED fabrication processes. Fig. 4.23(a) shows the OM images taken after fabrication steps. First, mesa structures were formed by using photolithography and inductively coupled plasma dry etching. The etching depth was ~1 μm to expose the n-type AlGaN. Then, the n-contact Ti/Al/Ni/Au (30/120/40/100 nm) metal layers were deposited on the n-type AlGaN layer by electron-beam evaporation and annealed at 900 ^{o}C for 1 min in N_2 ambient. The p-contact Ni/Au (20/100 nm) metal layers were also deposited on the p-type GaN surface, followed by thermal annealing at 750 ^{o}C for 1 min in air ambient. Lastly, a Ti/Au (20/100 nm) pad metal was deposited on both n- and p-type metal contacts. The target structure is a flip-chip structure which is widely used in DUV LEDs for better heat-dissipation and light extraction as shown in Fig. 4.23(b). So, the photons are mainly extracted to the sapphire substrate, the bottom side.

For current-voltage (I-V) measurements, an Agilent B2902A Precision Source/Measurement unit was used with voltage sweep from -5 V to 15 V under DC current condition. For light-current (L-I) measurements, light output (5 ms current pulse sweep, 1% duty cycle) was measured as a photocurrent using a Si photodetector, the same Source/Measurement unit, and bottom-emission measurement setup in a free-standing condition in a dark room environment. To avoid the possible performance variation over the 4-in. wafers, the center parts of both wafers were used.

Fig. 4.24 shows electroluminescence (EL) spectra as a function of wavelength of DUV LED on the NPS and reference DUV LED, showing the emission with peak wavelength of 280 nm without parasitic emission. Fig. 4.25 shows the representative I-V characteristics for both reference DUV LED and DUV LED on NPS. The inset shows the log plot. The reference DUV LED has much higher forward leakage current than that of the DUV LED on NPS. Reducing forward leakage is very important for improving overall performance of LEDs because it is well correlated with device reliability and determines ideal power consumption. The high forward leakage is commonly believed to be defect-assisted tunneling current resulting from high-density defects in III-nitride films heteroeptaxially grown on foreign substrates.[31,32] The forward leakage of the DUV LED on NPS is significantly reduced compared to the reference DUV LED because nanoscale ELO on the NPS method can efficiently reduce the defects and improve the crystal quality of overgrown AlGaN layers. In addition, the carrier mobility is also increased in the DUV LED on NPS because of reduced grain boundaries and defects, resulting in low sheet resistance.[33] As a result, at the injection current of 20 mA, the operating voltage of the DUV LED on NPS is 9.3 ± 0.16 V, 1.5 V smaller than that of the reference DUV LED (10.8 ± 0.66 V), which is attributed to the reduced sheet resistance in the DUV LED on NPS.

Fig. 4.26 shows the average LOP with error bars as a function of the injection current measured from 50 LEDs at room-temperature. The relative EQE, estimated by dividing the photocurrent by the injection current, is also shown in Fig. 4.27. The LOP of the DUV LEDs on NPS shows much higher LOP by 67% than that of the reference DUV LED at the injection current of

20 mA. Consequently, the DUV LED on NPS shows a remarkably higher relative EQE throughout the whole injection current than that of the reference DUV LED. It is worthwhile to note that efficiency peak point and efficiency droop behavior are different for both DUV LEDs. The DUV LED on NPS has a peak efficiency at 2.6 mA and an efficiency droop of 25.7% when the current is increased up to 20 mA, while the reference DUV LED shows low peak efficiency and little efficiency droop without a pronounced efficiency peak. Based on a model describing the rates of carrier recombination mechanisms, EQE can be expressed by a combination of the carrier concentration in the active region (*n*), defect-related non-radiative Shockley-Read-Hall (SRH) coefficient (*A*), and radiative coefficient (*B*) as follows;

$$\mathrm{EQE} = \mathrm{LEE} \times \mathrm{IQE} = \mathrm{LEE} \times \frac{Bn^2}{An + Bn^2 + f(n)},$$

where *f(n)* represents the carrier loss rate by electron leakage and Auger recombination. For the reference DUV LED with lower crystal quality, *i.e.*, higher point defects and extended defects such as threading dislocations and grain boundaries, the SRH non-radiative lifetime is sufficiently short to suppress the radiative recombination, thus, the radiative recombination is never dominant, resulting in a very low efficiency lack of a pronounced efficiency peak.[34] Consequently, efficiency droop is not observed at measured currents up to 20 mA. In the case of the DUV LED on NPS with smaller A than that of the reference DUV LED, the radiative recombination process becomes dominant at a low current, followed by pronounced efficiency droop phenomenon when other non-radiative mechanisms such as

electron leakage and Auger recombination become dominant as the current increases.

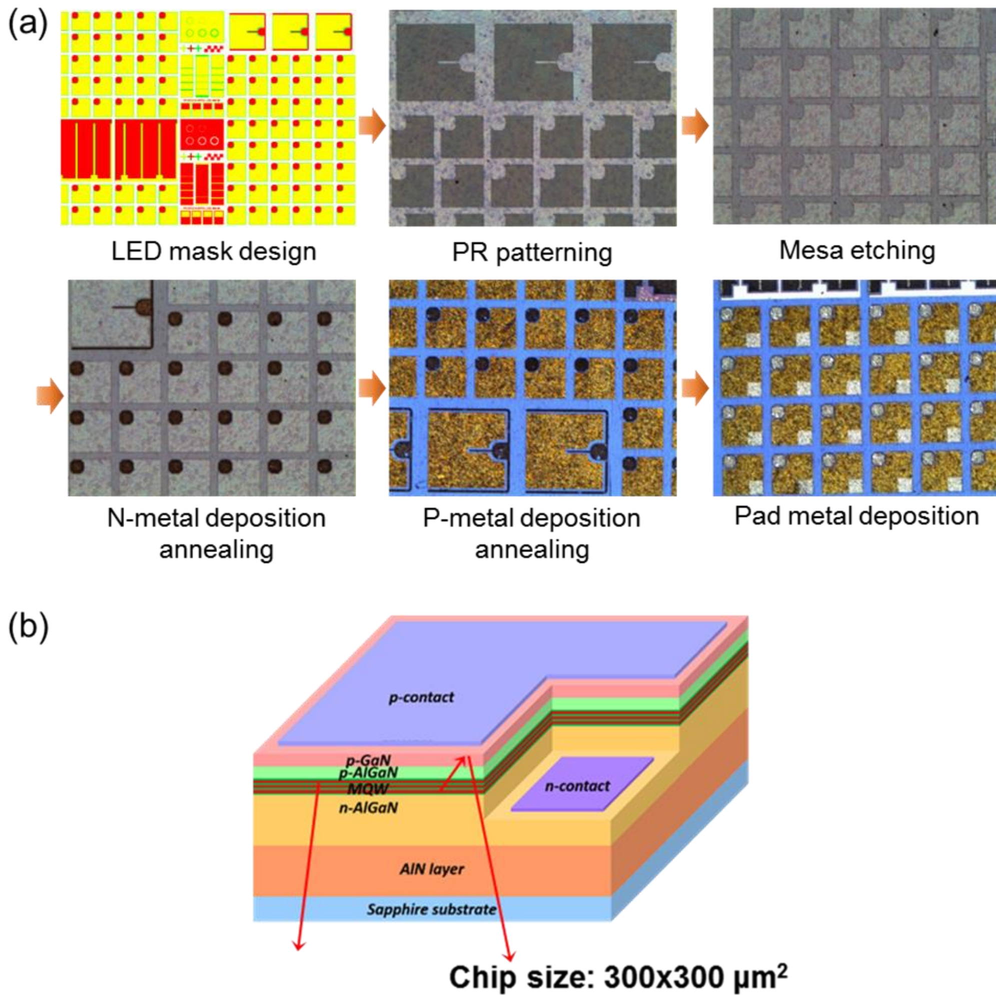


Figure 4.23. (a) Device fabrication process of DUV LEDs and (b) flip-chip configuration extracting the DUV photons through the sapphire substrate with the chip size of 300×300 μm^2.

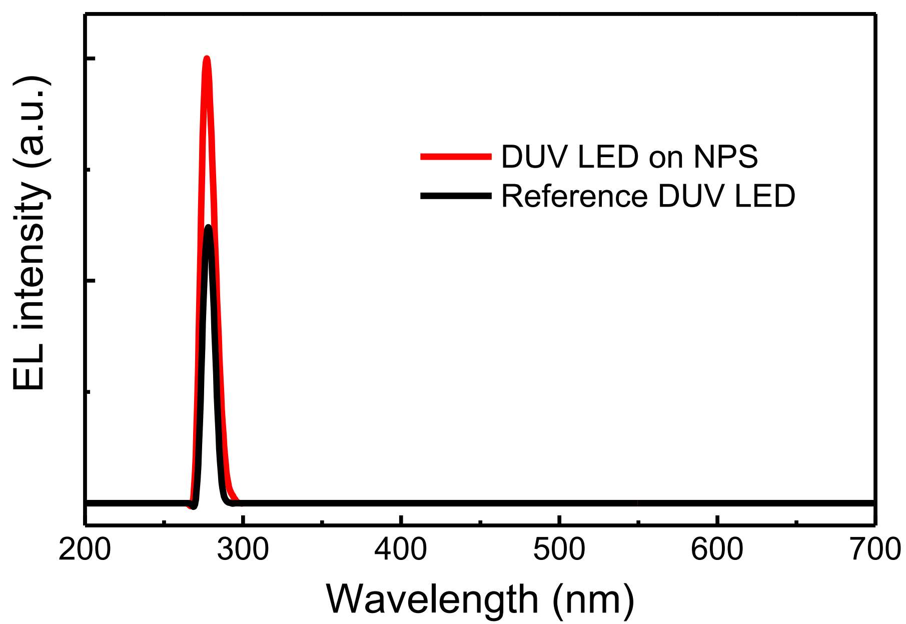


Figure 4.24. EL spectra of DUV LEDs.

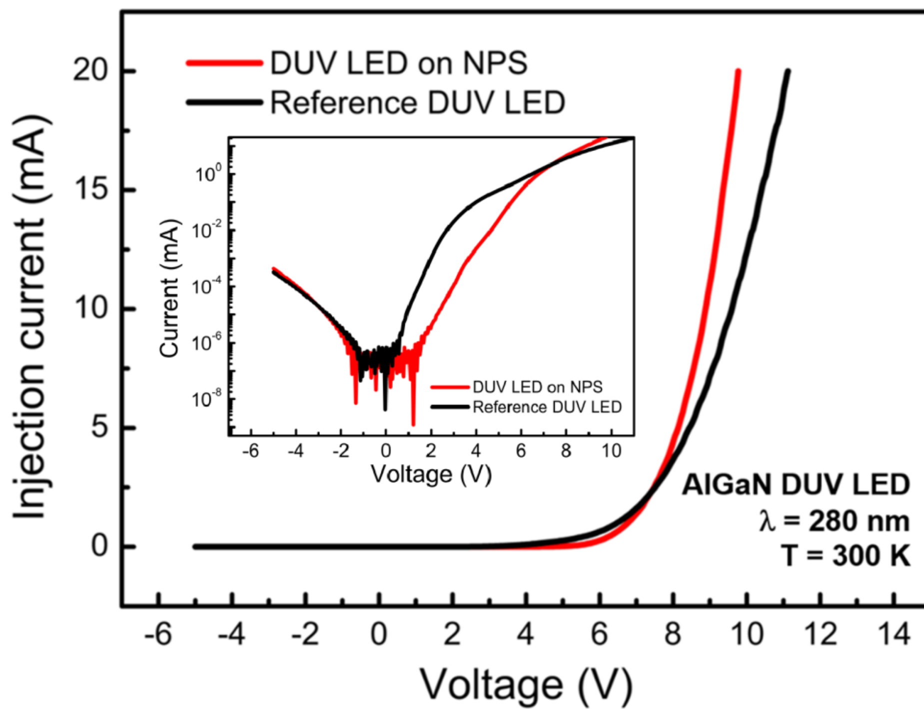


Figure 4.25. I-V characteristics of DUV LEDs. The inset shows the log plot.

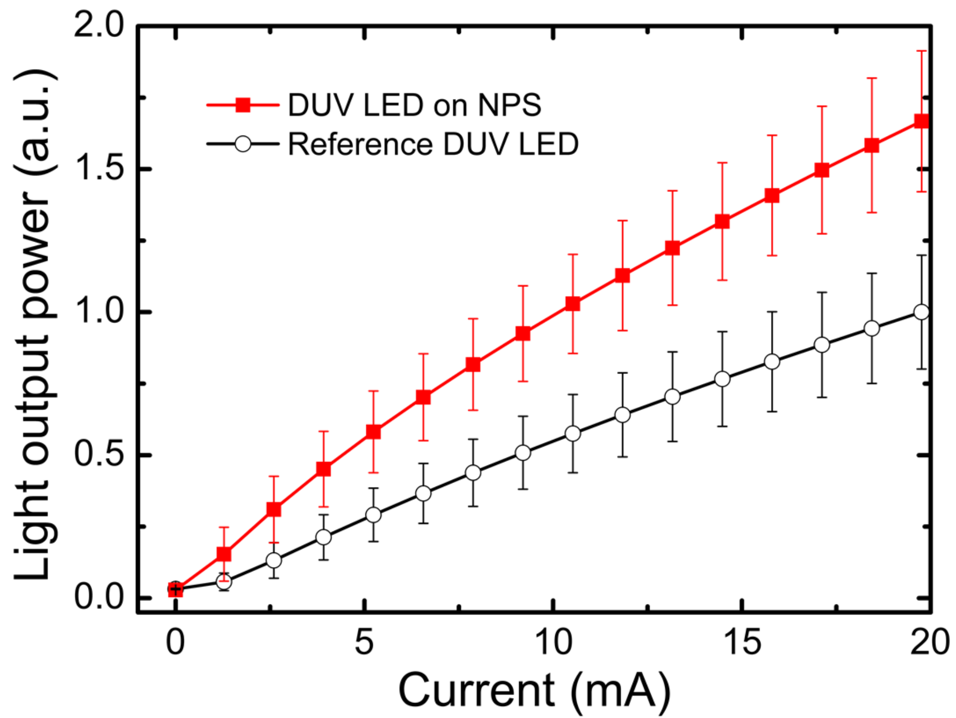


Figure 4.26. Average LOPs with error bars as a function of injection current measured from 50 representative DUV LEDs.

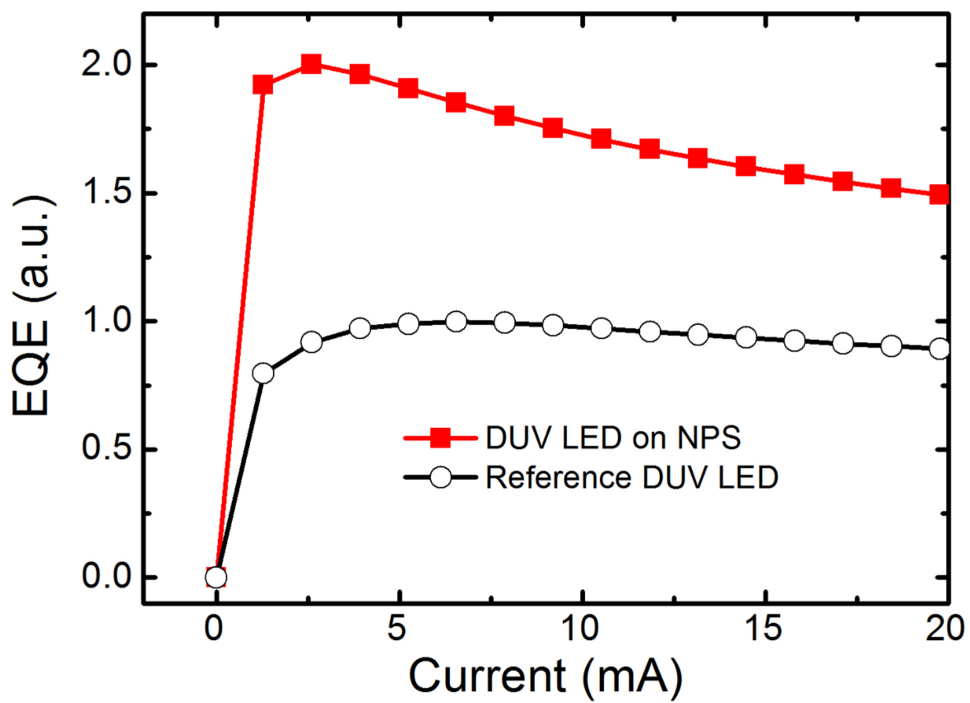


Figure 4.27. Representative EQE of DUV LEDs as a function of injection current.

4.3.4 3-D finite-difference time-domain (FDTD) simulation: effect of embedded air void on light extraction

Three-dimensional (3-D) finite-difference time-domain (FDTD) method (Lumerical FDTD Solutions) was used to analyze the effect of the embedded air-void nanostructure in the AlN layer on the light extraction. Fig. 4.28 shows three-dimensional FDTD simulation models of reference DUV LED and DUV LED on NPS. The simulation models were composed of p-type GaN, MQWs, n-type AlGaN, AlN, and sapphire substrate. The boundary conditions were a periodic boundary condition at lateral surfaces, a mirror at the top of p-type GaN layer, and a perfectly matched layer which absorbs the incident light on it outside of the detector, bottom of the sapphire substrate. For the DUV LED on NPS, the embedded air-void nanostructure which has the periodic hexagonal array of AlN nanorods surrounded by the air void was located in the AlN layer. The light source was a 280 nm monochromatic dipole source and located in the MQW region. The refractive indices at the wavelength of 280 nm were selected as 2.6, 2.6, 2.16, and 1.82 for p-type GaN, AlGaN, AlN, and sapphire, respectively.[35] The absorption coefficient of the p-type GaN layer, a strongly DUV light-absorbing layer, was set to be 170,000 cm^{-1}.[36] Those of MQW layer and n-type AlGaN layer were chosen to be 1,000 and 10 cm^{-1}.[37] Fig. 4.29 shows the light propagation at 2 fs intervals in DUV LEDs without [(a)-(c)-(e)-(g)] and with the embedded air-void nanostructure [(b)-(d)-(f)-(h)]. For the reference DUV LED, the light emitted from the MQW active region radiates in all directions. As a result, most of the light experiences the total internal reflection at the interfaces between AlN/sapphire and sapphire/air, resulting in the huge DUV light loss due to

the absorption in the strongly DUV light-absorbing p-type GaN and MQWs. On the other hand, the light emitted from the MQWs in the DUV LEDs with the embedded air-void nanostructure propagates vertically by passing through the embedded structure. Thus, more DUV photons can be extracted via shorter photon path length before being absorbed by the p-type GaN and MQWs avoiding the total internal reflection. The result indicates that the embedded air-void nanostructure in the DUV LEDs contributed to the enhancement of LEE remarkably.

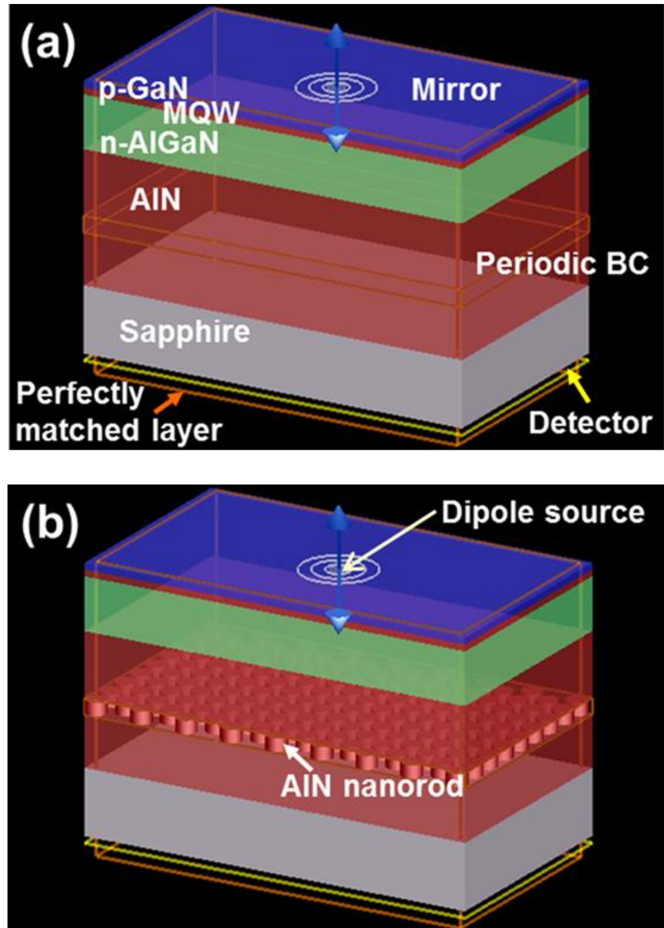


Figure 4.28. FDTD simulation models of (a) reference DUV LED and (b) DUV LED on the NPS.

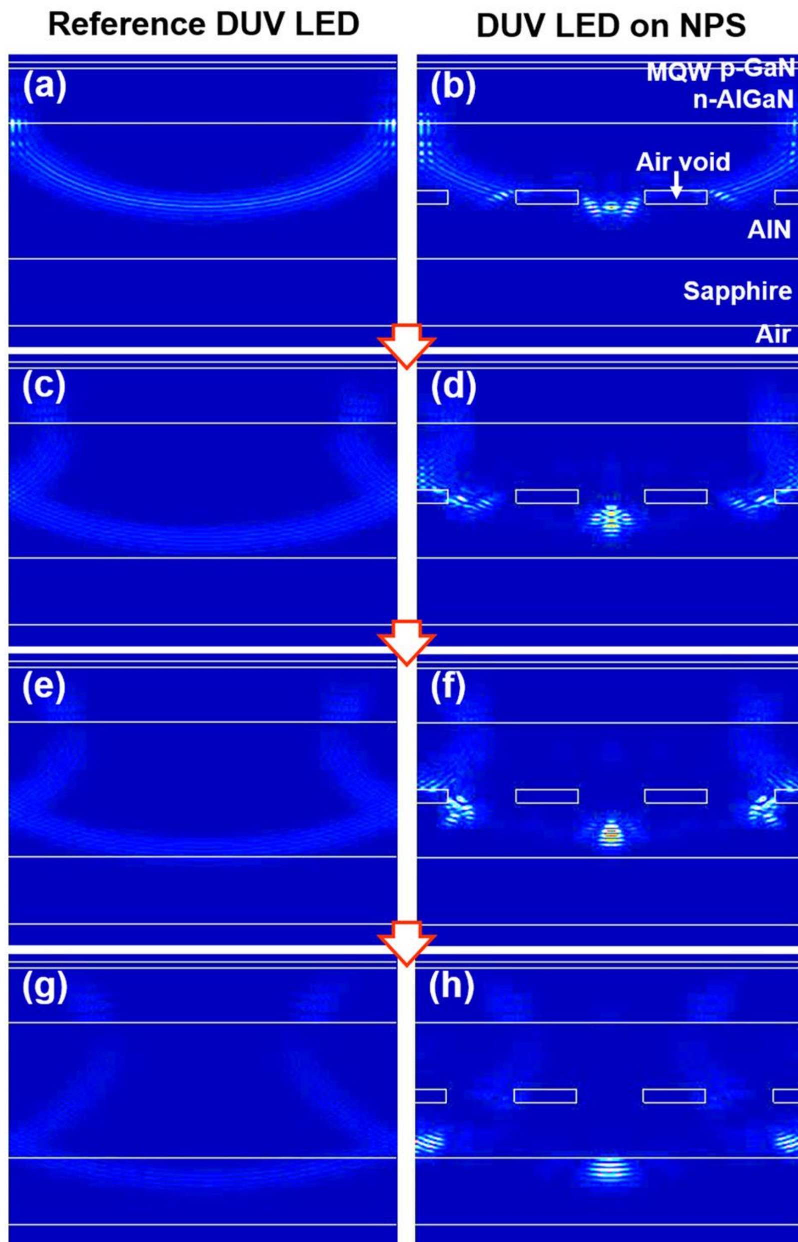


Figure 4.29. FDTD simulation of light propagation at 2 fs intervals in reference DUV LED [(a)–(c)–(e)–(g)] and DUV LED on NPS [(b)–(d)–(f)–(h)].

4.4 Summary

We demonstrated AlGaN-based DUV LEDs with periodic air-voids-incorporated nanoscale patterns enabled by nanosphere lithography and ELO. The nanoscale ELO on the NPS improved the crystal quality of overgrown epitaxial layers at relatively low growth temperature of 1050 °C and at small coalescence thickness. The air voids formed in the AlN epitaxial layer effectively relaxed the tensile stress during growth, so that crack-free DUV LED epitaxial layers were obtained on 4-in. sapphire substrate. In addition, the periodically embedded air-void nanostructure enhanced the LEE of DUV LEDs by breaking the total internal reflection that is particularly severe for the predominant anisotropic emission in AlGaN-based DUV LEDs. The LOP of the DUV LEDs on NPS was enhanced by 67% at the injection current of 20 mA compared to that of the reference DUV LEDs. We believe that the significant enhancement of LOP was attributed to the simultaneous improvements in the crystal quality of AlGaN epitaxial layer, *i.e.*, IQE and LEE.

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Chapter 5. Epitaxial lateral overgrowth of GaN on nano-cavity patterned sapphire substrate (NCPSS)

5.1 Introduction: growth of GaN with embedded voids

Large mismatches in lattice constant and thermal expansion coefficient between GaN and substrate result in high TDD and severe film stress resulting in significant wafer bow, thus decrease IQE and hinder mass production of LEDs using large size wafers. In addition, photons generated in the active region of GaN-based LEDs experience total internal reflections due to the large difference in refractive indices between GaN (n≈2.5) and air (n=1), resulting in low LEE.[1,2]

Many techniques have been investigated to solve the problems in GaN-based LEDs. ELO has been reported to significantly reduce the TDD of heteroepitaxial GaN layers.[3-5] PSS have been developed and widely used to realize highly efficient GaN-based LEDs.[6-8] In addition, it has been reported that the growth of high quality GaN layers was achieved by embedding microscale and nanoscale particles instead of patterns fabricated by photolithography.[9-12] However, the efficiencies including IQE and LEE and cost reduction still need to be improved further.

The embedment of void in the GaN layer has been investigated as a promising technique to obtain high quality GaN epitaxial layers that are less defective, less strained, and more effective to enhance the LEE.[13-15] Recently, the incorporation of well-defined void patterns in the GaN layer has been reported by using cavity-engineered substrates, which not only enhance the

LEE further due to the large refractive-index contrast between GaN and the embedded void but also relax the residual stress of the GaN layer.[16,17] In comparison to the micro-patterned substrates, nano-patterned substrates have been reported to enhance the LEE due to the increased density of patterns in the same area.[18-20] However, there is a debate that the nano-patterned substrates is not beneficial in reducing the TDD because the high density patterns and potential coalescence fronts would generate lots of dislocations in the GaN layer during the coalescence over the patterns.[21] Kim *et al*. have obtained less strained and high quality GaN layers by using cost-effective silica hollow nanosphere coated sapphire substrates, however, there was a limit in obtaining high-coverage and periodic patterns.[22] In this chapter, we propose the growth of GaN using a nano-cavity patterned sapphire substrate (NCPSS), which has high-coverage and periodic nano-cavity patterns on a sapphire substrate, employing polystyrene (PS) sphere patterning. The PS patterning by spin coating, a simple and cost-effective process, enabled us to fabricate periodic nano-cavity patterns which are composed of nanoscale voids surrounded by thin alumina shell. This approach is expected to improve the efficiency and reduce the production cost of GaN-based LEDs. The motivation for the introduction of the NCPSS to GaN-based LEDs is summarized in Fig. 5.1.

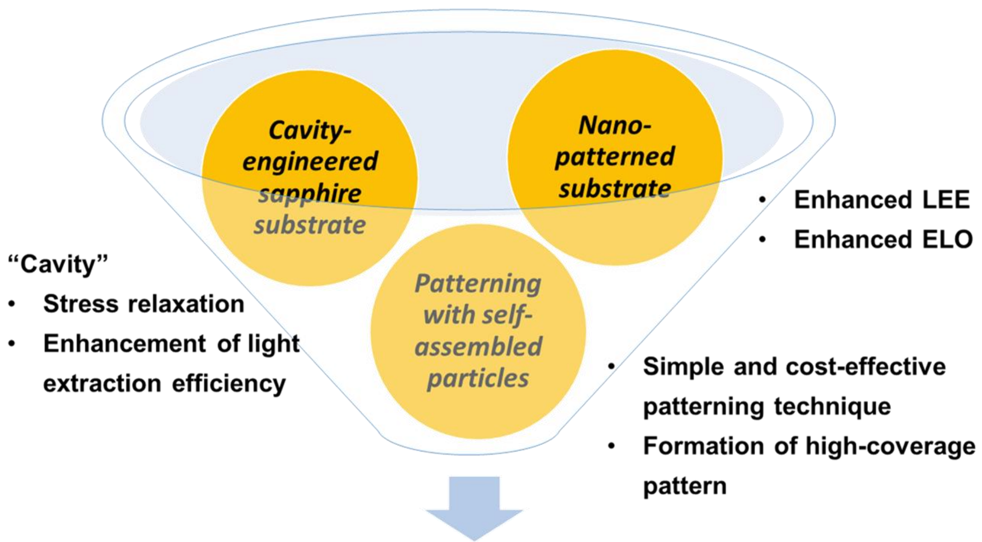

Figure 5.1. NCPSS for highly efficient LEDs.

5.2 Experimental procedure

A schematic fabrication process of NCPSS is shown in Fig. 5.2. The first step to fabricate the nanoscale cavity patterns is coating of PS spheres with a diameter of ~1020 nm on a 2-in. c-plane sapphire substrate. Spin coating, a simple and cost-effective process for the fabrication of large-area and well-ordered nanoscale patterns,[23,24] was employed to fabricate a monolayer of self-assembled PS spheres. After PS patterning, O_2 RIE was carried out with 30 sccm O_2 flow rate at 8.0 Pa and 80 W RF power. The O_2 RIE was performed in terms of two reasons; one is to create a growth window of GaN between the patterns and the other is to remove the surface contaminants on the sapphire substrate which might be present after the PS coating process. Then, a 63 nm-thick amorphous alumina layer was deposited on the PS-patterned sapphire substrate by ALD at the temperature of 110 ^{o}C. The precursors of aluminum and oxygen were TMAl and de-ionized water, respectively. The alumina-deposited substrate was put into the furnace and annealed at 1100 ^{o}C for two hours in air ambient to burn the PS core and crystallize the ALD-deposited amorphous alumina layer to α-phase alumina, *i.e.*, sapphire.

The fabricated NCPSS was loaded in a 6×2 in. Thomas Swan close-coupled showerhead MOCVD reactor for the growth of GaN. TMGa and NH_3 were used as precursors of Ga and N, respectively. The substrate was thermally cleaned in H_2 ambient at 1070 ^{o}C for 5 min. Then, the temperature was lowered to 560 ^{o}C and a 30 nm-thick GaN buffer layer was grown at 13.3 kPa. Subsequently, a GaN epitaxial layer was grown at 1040 ^{o}C and 33.3 kPa. For comparison, a planar c-plane sapphire substrate was loaded in

the same batch of the MOCVD reactor. The structure analysis on nano-cavity patterned sapphire substrates and GaN layers was carried out by field-emission SEM. CL and XRD were used to evaluate the crystal quality of GaN layers. TEM was carried out to investigate the behavior of threading dislocations in the GaN layers. The TEM specimens were prepared by focused ion beam. The residual stress in the GaN layer was evaluated by using micro-Raman spectroscopy with a 633 nm line of He-Ne laser. The diffuse reflectance of GaN layers was measured by spectrophotometer (Varian Cary5000) with an integrating sphere to investigate the effect of nano-cavity patterns on light extraction.

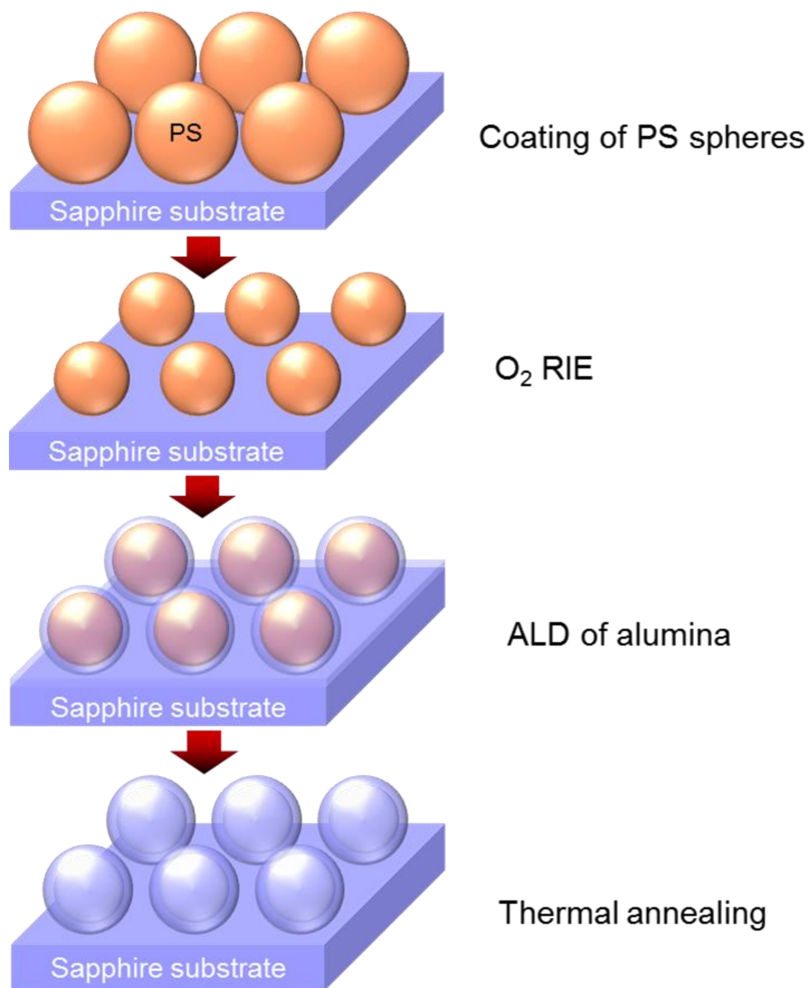

Figure 5.2. Schematic fabrication process of NCPSS.

5.3 Results and discussion

5.3.1 Fabrication of NCPSS

Fig. 5.3 is a plan-view SEM image showing the PS sphere array on the sapphire substrate coated by using the spin coating method. A monolayer of hexagonally close-packed PS spheres was obtained. Fig. 5.4 shows plane-view and cross-section SEM images of PS patterns as a function of O_2 RIE time. As the etching time increases, both the diameter and height of the PS pattern gradually decreases. The size of PS patterns gradually decreased to 550 nm in diameter as the etch time increased up to 4 min. Further etching caused collapse and deformation of PS patterns. Since the position of PS pattern after O_2 RIE remains unchanged, the spacing between the PS patterns, which will be the growth window for GaN, increases with the decrease of the PS pattern size. Consequently, a non-close-packed hexagonal PS array was developed by O_2 RIE from the close-packed PS array as shown in Fig. 5.4. Cross-section SEM images reveal the shape of PS patterns after the etching. During the O_2 RIE process, the reactive ions reach the PS-patterned substrate in a direction perpendicular to the surface of substrate so that the top of the PS patterns was effectively etched while the bottom was not. The top surface of the PS pattern was roughened with increased etching time due to the formation of cross-linked regions on the PS pattern by plasma treatment.[25] Fig. 5.5 reveals that the O_2 RIE process enables the precise adjustment of the PS pattern size and the spacing by manipulating the etching time though the excessive etching induces the surface roughening of the PS patterns.

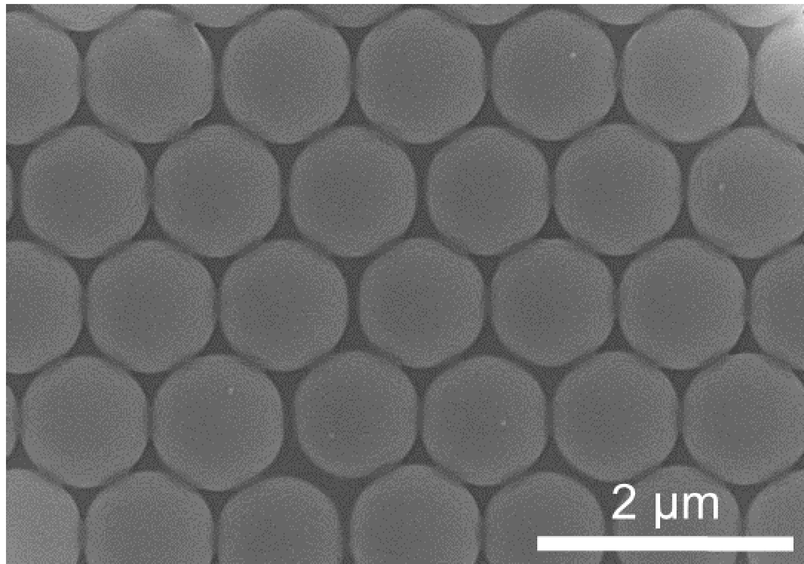

Figure 5.3. PS spheres coated on the sapphire substrate.

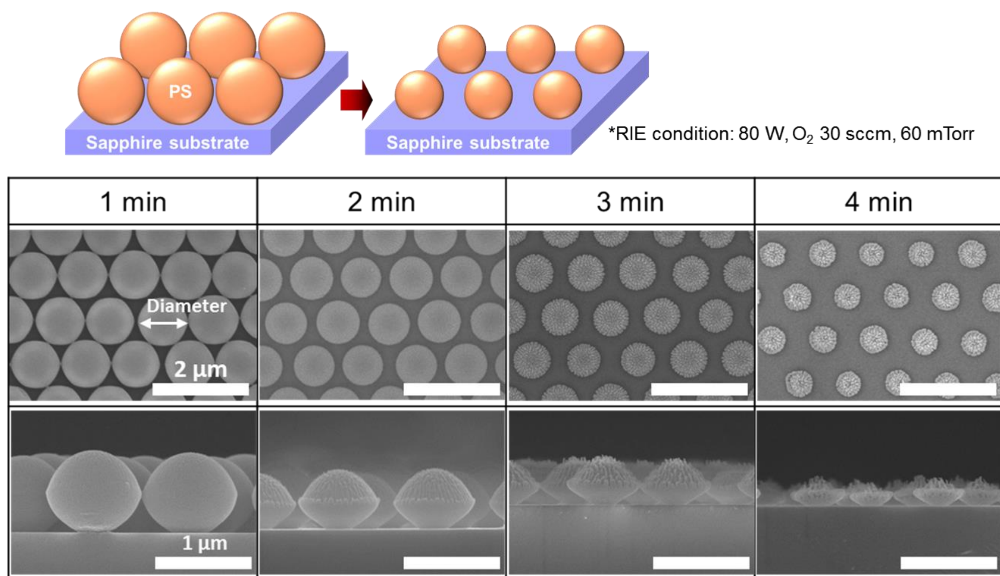

Figure 5.4. Size control of PS by O_2 RIE.

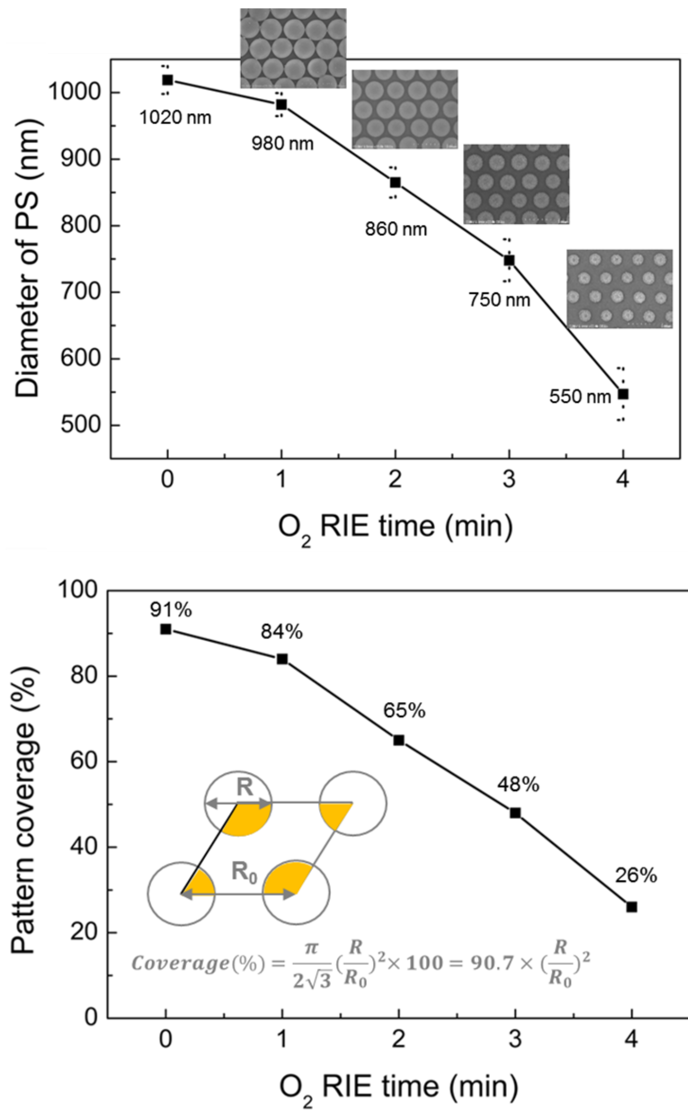

Figure 5.5. O_2 RIE results as a function of etching time.

Fig. 5.6(a) and 5.6(b) show plan-view and cross-section SEM images of the fabricated NCPSS, respectively. As shown in Fig. 5.6(a), periodically distributed nanoscale patterns were formed on the sapphire substrate. The non-close-packed hexagonal array was developed by self-assembly of close-packed PS spheres followed by O_2 RIE, deposition of amorphous alumina, and thermal annealing. The resultant diameter and coverage of patterns were measured to be ~ 930 nm and 75%, respectively. Fig. 5.6(b) reveals that each nanoscale pattern consists of a cavity and an alumina shell surrounding it. The shape of cavity pattern was ellipsoidal, which was determined by the shape of the PS pattern after O_2 RIE. After the O_2 RIE with the etching time of 2 min, amorphous alumina layer with the thickness of 63 nm was deposited conformally along the shape of the PS pattern with the help of high step coverage of atomic layer deposition. During the thermal annealing, the PS inside the alumina shell was removed by oxidation and a cavity was formed as shown in Fig. 5.6(b).

The O_2 RIE time and the thickness of alumina determine the pattern size. By changing the O_2 RIE time and the deposition thickness of alumina, the fabrication window was investigated as shown in Fig. 5.7. The fabrication of stable cavity patterns depends on the PS pattern size and the thickness of alumina shell. If the alumina thin film is too thin compared to the PS pattern size, the cavity structures collapse or disappear during the thermal annealing process. The pattern size is adjustable by varying the deposition thickness of alumina shell even if the same PS pattern was used.

The crystal structure of the alumina shell after thermal annealing was investigated by TEM measurement. Fig. 5.8(a) and 5.8(b) show a cross-section TEM image of the nano-cavity pattern on the sapphire substrate and

selected area diffraction patterns (SADPs) of positions including an original sapphire substrate and alumina that is deposited by ALD and annealed by thermal treatment. It was confirmed that the SADPs of all the positions, 'A', 'B', and 'C' positions in Fig. 5.8, are the same as that of single crystalline α-phase alumina, exactly same with that of sapphire substrate indicated by the position 'S', which reveals that as-deposited amorphous alumina layer was transformed to α-phase during the thermal annealing process through solid-phase epitaxy as shown in the schematic diagram in Fig. 5.8(c).[26,27] Therefore, it was confirmed that the NCPSS is a single crystalline c-plane sapphire substrate which enables the epitaxial growth of nitrides thereon.

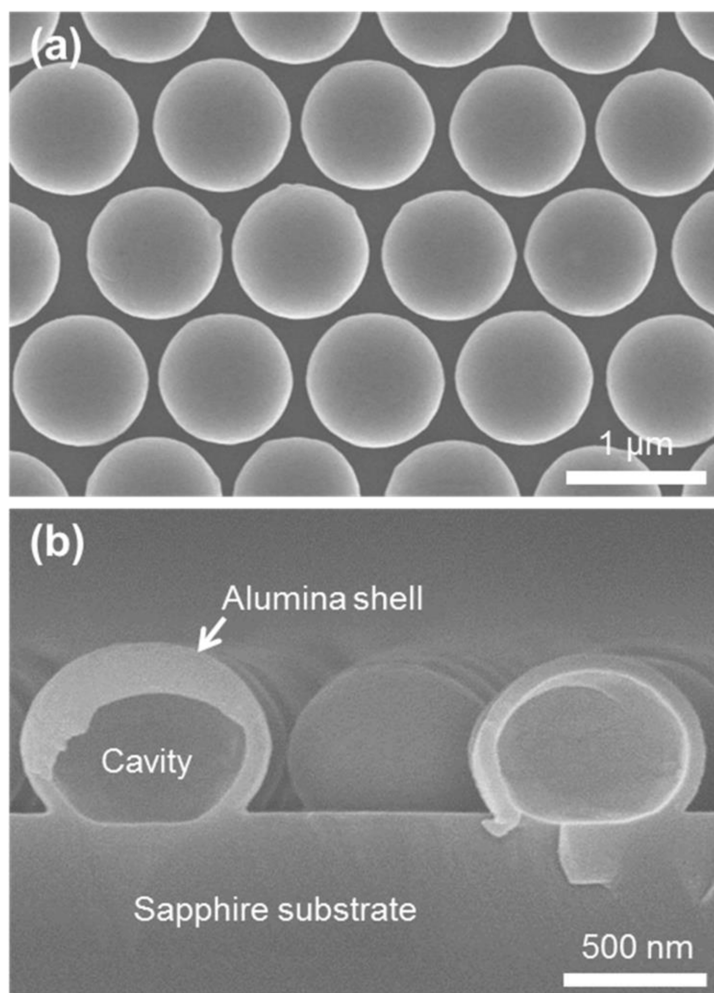

Figure 5.6. (a) Plan-view and (b) cross-section SEM images of the fabricated NCPSS showing the periodic array of nano-cavity patterns.

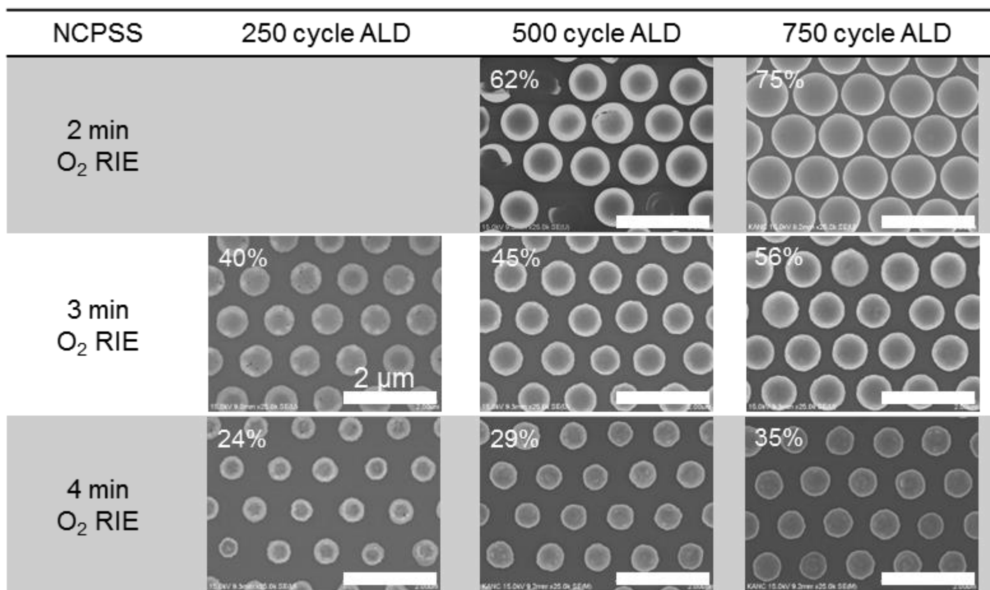

Figure 5.7. NCPSS fabricated by varying O_2 RIE time and ALD cycle.

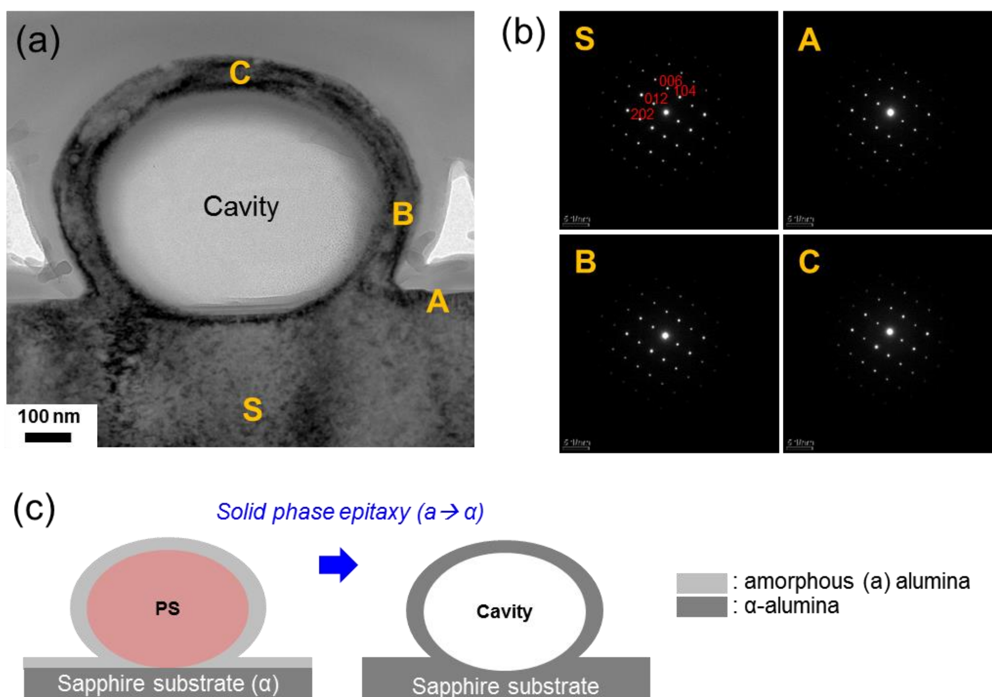

Figure 5.8. (a) Cross-section TEM image of the nano-cavity pattern and (b) the SADP from each position corresponding to the alphabet in (a). Schematic diagram showing the transformation of the alumina during thermal annealing.

5.3.2 Epitaxial lateral overgrowth of GaN on NCPSS

GaN was grown on the NCPSS by using conventional 2-step growth composed of (i) the growth of a buffer layer at low temperature and (ii) the growth of an epitaxial layer at high temperature. The growth temperature and the pressure for the high-temperature (HT) GaN were fixed to 1040 ^{o}C and 33.3 kPa.

A morphological evolution of GaN on the NCPSS during the MOCVD growth was investigated by a series of the growth interruptions as shown in Fig. 5.9. The growth time of high-temperature GaN was varied from 5 min to 40 min. At first, nanoscale GaN islands were grown both on the spacing between the patterns and on top of the patterns as shown in Fig. 5.9(a). It is worth noting that the top surface of the pattern as well as the planar surface between the patterns are c-plane sapphire surfaces, which enable the epitaxial growth of GaN thereon. The inset of Fig. 5.9(a) is a cross-section SEM image, which shows that both the GaN islands grown on the spacing between the patterns and top of the patterns have top (0001) planes and side facets of $\{1\bar{1}01\}$ planes which have a tilt angle of 62° with respect to the (0001) planes. As the growth progressed, GaN islands grown on the spacing between the patterns coalesced together with neighboring islands, forming relatively large islands, while the growth of hexagonal GaN islands on top of the patterns was limited, as shown in Fig. 5.9(b). We believe that the relatively large GaN islands were grown preferentially at wide spaces between the patterns of the as-fabricated NCPSS compared to neighboring growth windows due to higher density of GaN seeds and higher incoming Ga flux. It is noticeable that the relatively large GaN islands coalesced and grew

laterally over several nano-cavity patterns while the growth of GaN on the other regions was suppressed, as shown in Fig. 5.9(c) and 5.9(d). As a result, ELO of GaN over the patterns and small GaN islands was proceeded with further growth. This interesting phenomena causes a delayed coalescence of GaN, which is different from the growth of GaN on microscale patterned substrates where GaN coalesced on each pattern as shown in Fig. 5.10.[16]

The delayed coalescence of GaN was achieved by (i) the selective formation of relatively large GaN islands and (ii) the ELO of GaN over the neighboring GaN. The growth mechanism was investigated in detail step by step.

Some observations lead to a clue to the preferenctial growth site of the relatively large GaN islands at the early growth stage. Fig. 5.11(a) and 5.11(b) are bird's-eye-view SEM images of GaN grown on the NCPSS with the growth time of 5 min. There are pattern defects such as vacancies and grain boundaries as shown in Fig. 5.11(a) and 5.11(b), respectively. These defect structures provide relatively larger spaces compared to regular structures. We believe that the relatively large GaN islands were developed preferentially at wide spaces between the patterns of the as-fabricated NCPSS compared to neighboring growth windows. Fig. 5.12 is a schematic diagram of nucleation and growth of GaN at the initial growth stage. The larger the spacing, the higher the density of the GaN seed immediately after the recrystallization process, the higher incoming Ga flux is supplied, and eventually the relatively large GaN islands are developed.

It is important to understand why the relatively large GaN islands are grown over the neighboring small GaN islands. The growth mechanism can be explained by the two kinetic pathways of incoming Ga flux to the large

GaN islands during the growth: (i) vapor pahse diffusion process and (ii) surface diffusion of Ga adatoms. During the vapor phase diffusion process, the atomic concentration gradient nearby the relatively large GaN islands is large so that more vapor precursors are supplied to the large GaN islands as shown in Fig. 5.13(a). The relatively large GaN islands provide a large surface area, where Ga adatoms can adsorb and contribute to the growth of $\{1\bar{1}01\}$ side facets as well as (0001) plane, while other small GaN islands confined by neighboring patterns do not. As a result, a large amount of excess Ga adatoms which do not participate in the growth migrate to the surrounding large GaN islands to participate in the growth thereon as shown in Fig. 5.13(b). The relatively large GaN islands become bigger and bigger while the neighboring small GaN islands experience a limited growth as shown in Fig. 5.13(c). The growth steps are summarized in Fig. 5.14.

A fully coalesced and continuous GaN layer was obtained on the NCPSS after the 4 hr growth, as shown in Fig. 5.15(a). The thickness of the GaN layer was 5.9 μm and nano-cavity patterns were embedded between the GaN layer and the sapphire substrate, as shown in Fig. 5.15(b). The embedded nano-cavity patterns are expected to relax the film stress and enhance light scattering by introducing a high refractive-index contrast.

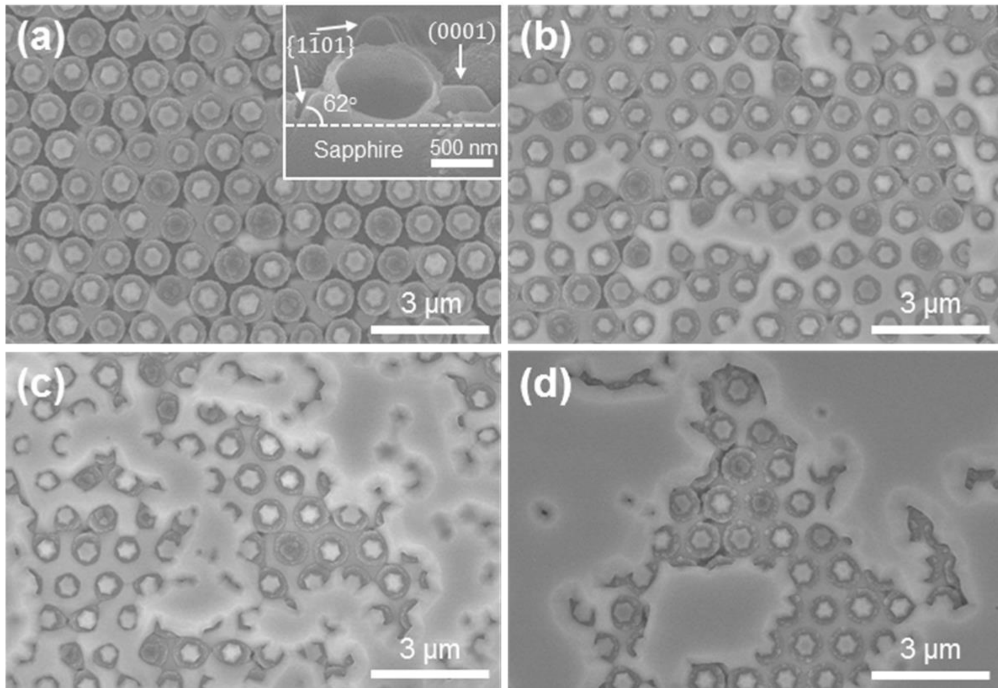

Figure 5.9. Plan-view SEM images showing the growth evolution of GaN on the NCPSS. The inset shows a cross-section SEM image.

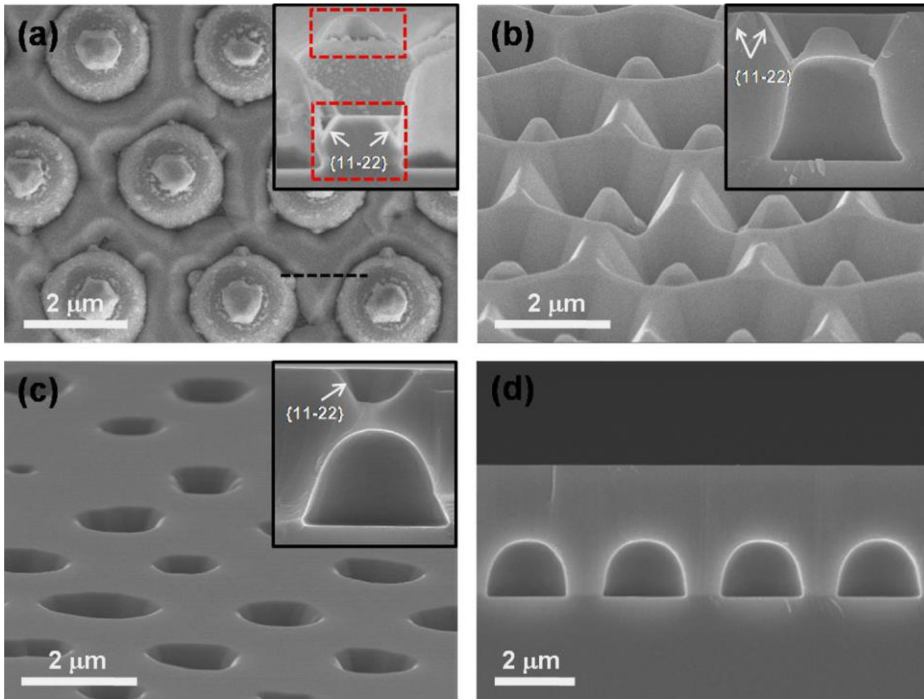

Figure 5.10. Growth of GaN on microscale CES.[16]

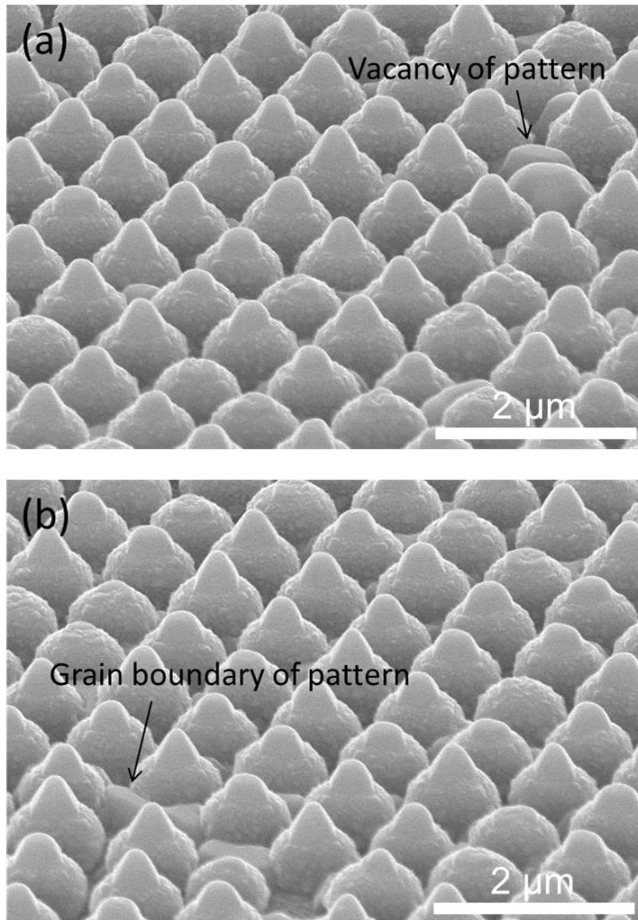

Figure 5.11. GaN islands observed at defect sites of patterns such as (a) vacancy and (b) grain boundary.

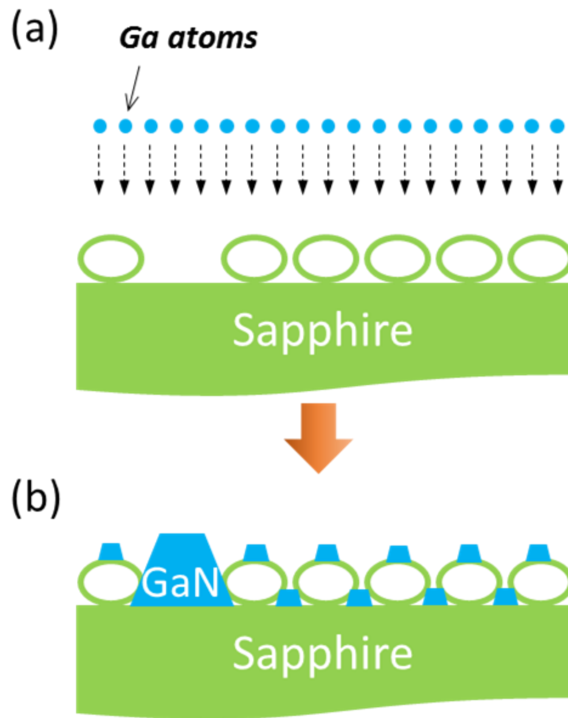

Figure 5.12. Schematic diagram of nucleation and growth of GaN at the initial growth stage including (a) income of Ga atoms and (b) GaN growth after surface reaction.

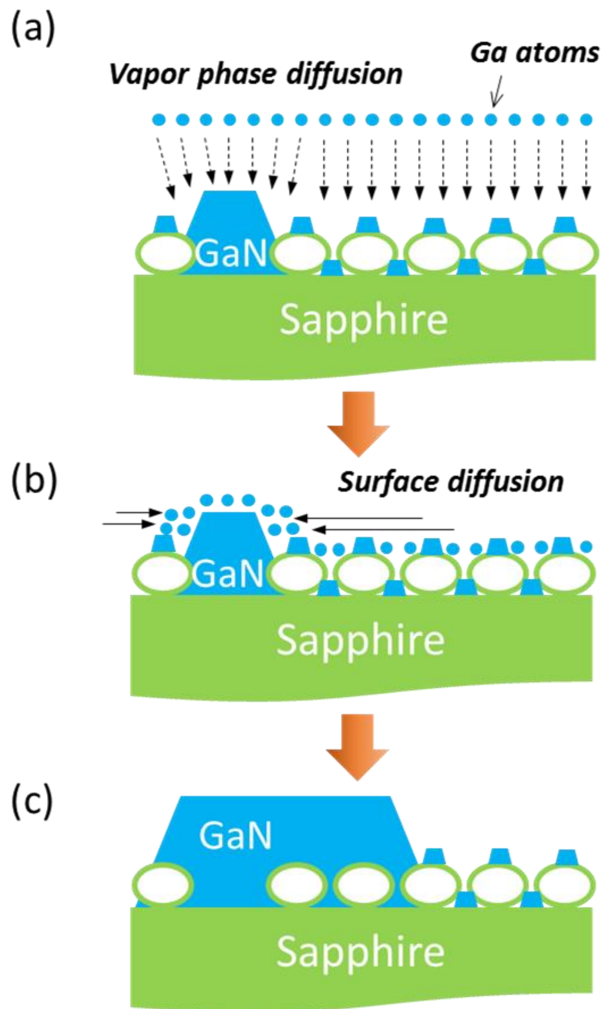

Figure 5.13. Schematic diagram explaining the inhomogeneous growth of GaN on the NCPSS governed by (a) vapor phase diffusion and (b) surface diffusion of Ga atoms, resulting in (c) the grain growth of GaN islands.

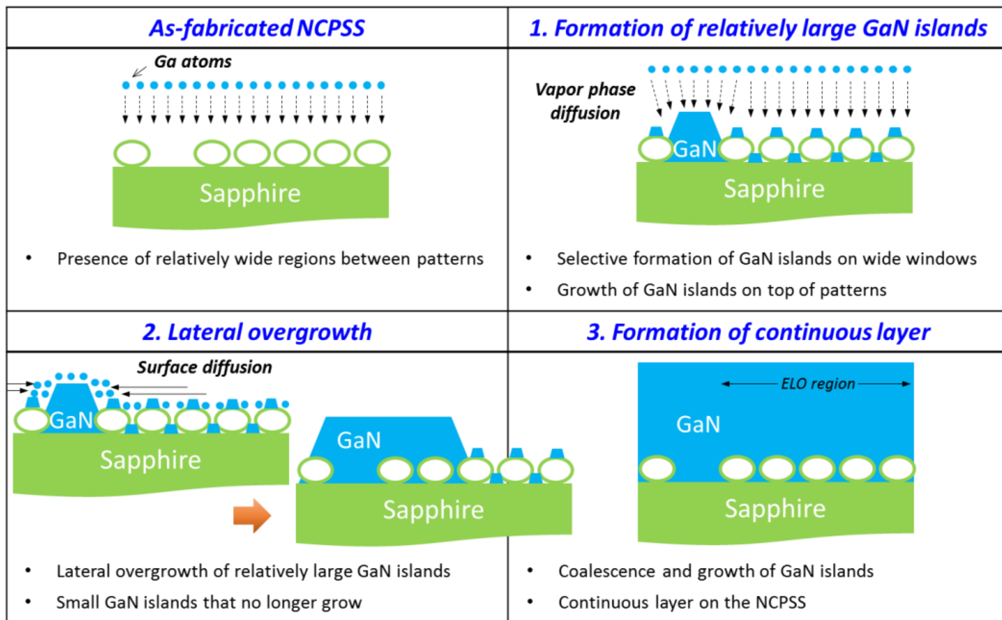

Figure 5.14. Growth steps of GaN on the NCPSS.

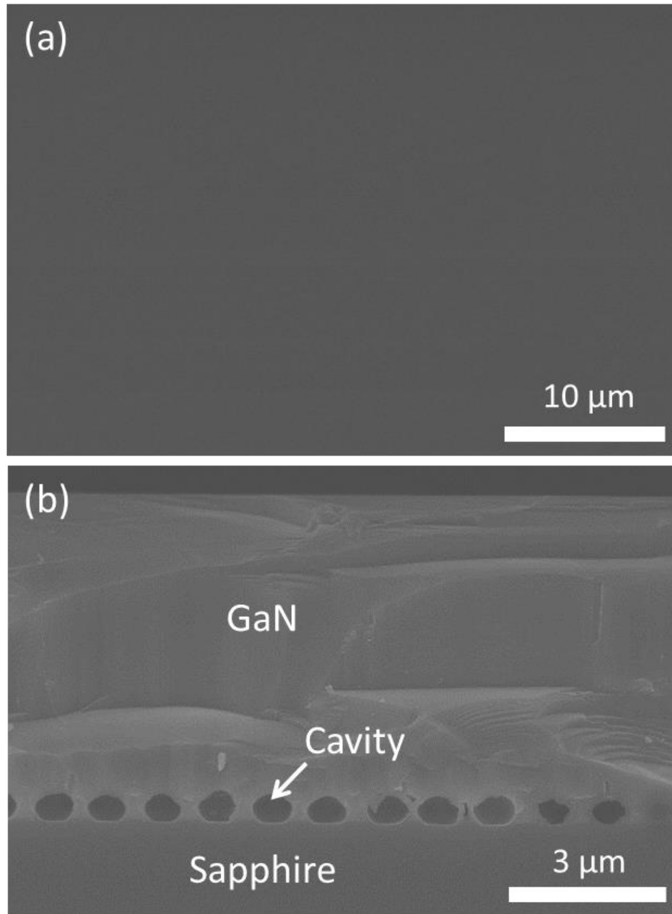

Figure 5.15. (a) Plan-view and (b) cross-section SEM images of GaN grown on the NCPSS with the growth time of 4 hr.

5.3.3 Structural and optical properties of GaN on NCPSS

The surface morphologies of GaN layers were investigated by AFM and are shown in Fig. 5.16. Both GaN layers grown on the NCPSS and the planar substrate showed smooth surfaces with the root-mean-square (RMS) roughness of 0.133 nm and 0.152 nm, repectively.

The crystal qualities of GaN layers were characterized by CL and XRD measurements. Fig. 5.17 shows CL images of both GaN layers grown on the NCPSS and on the planar substrate. TDDs calculated by dark spot densities of CL images were 6.9×10^{7} cm^{-2} and 2.4×10^{8} cm^{-2} for GaN on the NCPSS and GaN on the planar substrate, respectively. The significant decrease of the TDD was attributed to the delayed coalescence of GaN enabled by the selective growth of relatively large GaN islands followed by the ELO of GaN over the patterns.

There is a correlation between the distribution of the defects on the CL image and the growth aspect. Fig. 5.18(a) shows a SEM image of GaN grown on the NCPSS with the growth time of 40 min and Fig. 5.18(b) shows the CL image for the continuous GaN layer with the growth time of 4 hr. The magnification of the two images are the same. It is worth noting that the SEM and CL images were not obtained from the same location. As mentioned in Chap. 5.3.2, GaN islands are surrounded by (0001) plane and $\{1\bar{1}01\}$ side facets. As the growth progressed, coalescence defects are generated along the $<11\bar{2}0>$ direction perpendicular to $<1\bar{1}00>$ direction when the GaN islands coalesce, as shown in Fig. 5.18(c). The coalescence of GaN inevitably causes the generation of coalescence defects, however, it should be noted that the

growth of GaN on the NCPSS siginificantly reduced the dislocation density by delaying the coalescence of GaN islands through the enhanced ELO.

FWHM values of X-ray rocking curves were also measured to study the crystal qualities of GaN layers. The FWHM values for (002) planes of GaN layer on the NCPSS and GaN layer on the planar substrate were 241 arcsec and 220 arcsec, respectively, which are comparable. Those for (102) planes of GaN layer on the NCPSS were 300 arcsec and 366 arcsec, respectively. The reduction of FWHM values for (102) planes also indicates that the crystal quality of GaN layer was improved by the ELO of GaN on the NCPSS.

To analyze the defects of GaN layer grown on the NCPSS, TEM measurement was carried out. Fig. 5.19(a) and 5.19(b) are cross-section bright-field TEM images taken at the interfacial area between GaN and sapphire substrate for GaN on the NCPSS along the zone axis of $[1\bar{1}00]_{GaN}$. From the TEM analysis, two distinctive defect reduction mechanisms were observed. One is the formation of stacking faults near the nano-cavity patterns and blocking the propagation of threading dislocations by them, as indicated by a solid arrow in Fig. 5.19. It has been reported that stacking faults are generated at coalescence fronts when neighboring GaN islands grown on nano-patterned substrates coalesce together.[28,29] The stacking faults suppress the propagation of threading dislocations. The other is the bending of threading dislocations. It was observed that some dislocations generated at the surface of the sapphire substrate and at the top of the patterns bent normal to the c-axis of GaN, as indicated by dashed arrows in Fig. 5.19. The GaN islands grown on the surface of the sapphire and on top of the patterns have $\{1\bar{1}01\}$ side facets. When the threading dislocations meet the side facets, they

bend in a direction perpendicular to the c-axis. This is because threading dislocations tend to minimize their free energy by bending to side facets.[30] As a result, we believe that both the termination of threading dislocations by stacking faults and the bending of threading dislocations contribute to the reduction of TDD.

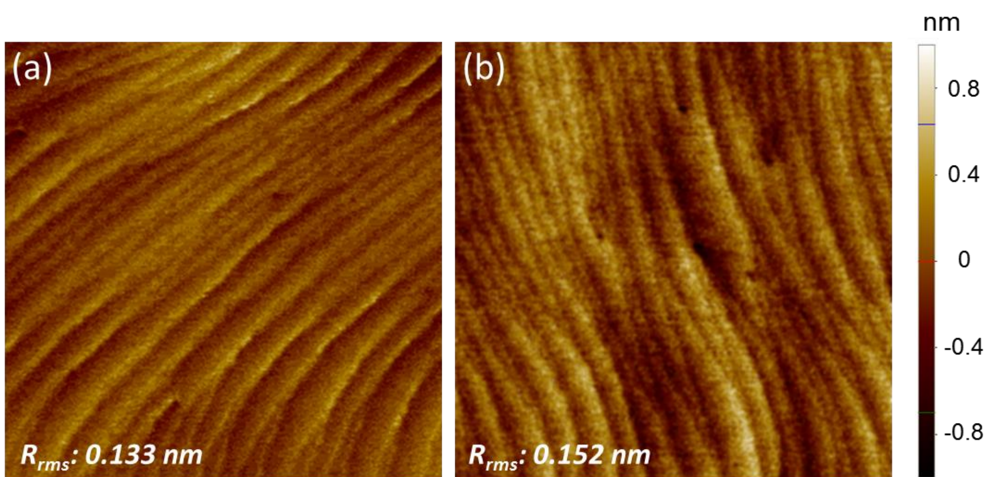

Figure 5.16. AFM images (2×2 μm^2) showing surface morphologies of GaN layers grown (a) on the planar substrate and (b) on the NCPSS, respectively.

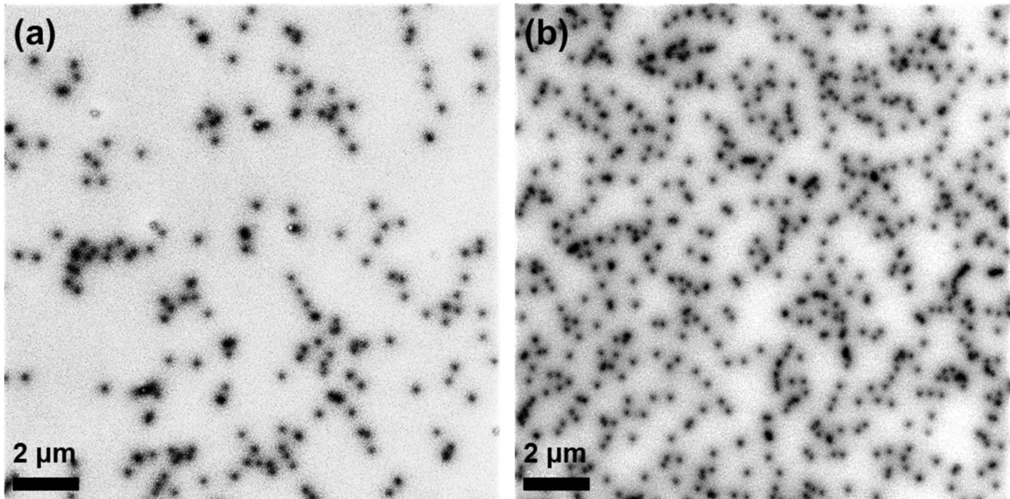

Figure 5.17. CL images of (a) GaN on the NCPSS and (b) GaN on the planar substrate.

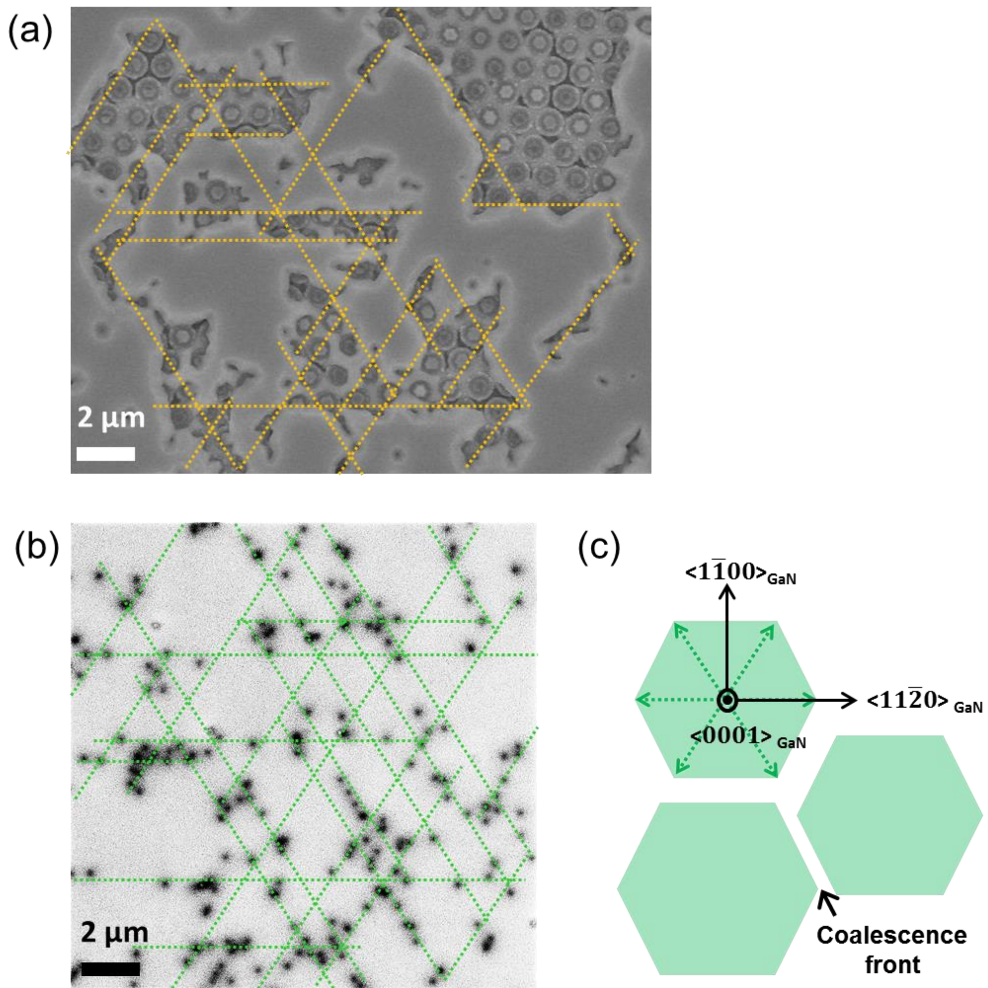

Figure 5.18. (a) Plan-view SEM image of GaN grown on the NCPSS with the growth time of 40 min, (b) CL images of GaN on the NCPSS after 4 hr growth (continuous film), and (c) crystallographic orientation of hexagonal GaN. Dashed lines indicates possible coalescence fronts along $<11\bar{2}0>_{GaN}$.

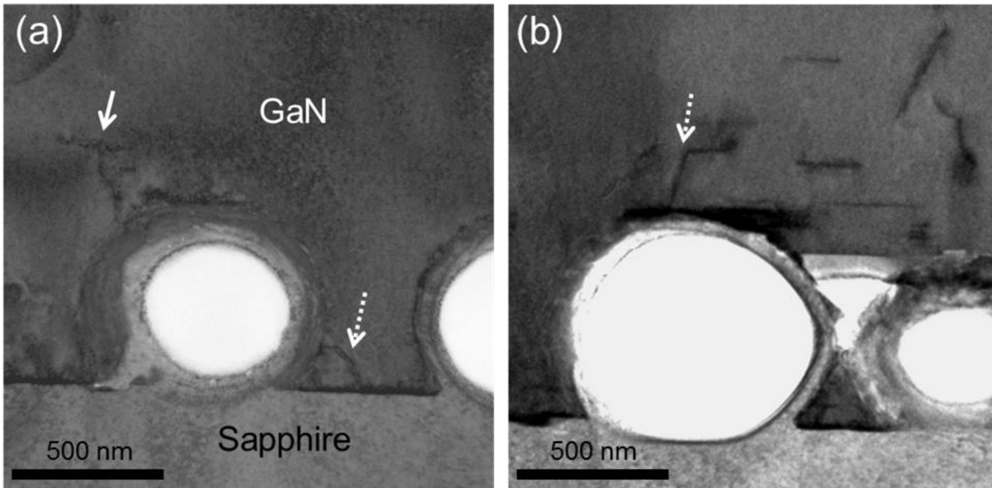

Figure 5.19. (a) and (b) Cross-section TEM images of GaN on the NCPSS taken at the interfacial area between GaN and sapphire substrate showing the termination of threading dislocation by stacking faults (solid arrow) and the bending of threading dislocation (dashed arrows).

Raman spectroscopy was used to investigate the residual stresses of GaN layer grown on NCPSS and the reference GaN grown on the planar substrate. Fig. 5.20 shows E_2 (high) mode peaks in Raman spectra of the two GaN layers grown on the NCPSS and on the planar substrate, and free-standing bulk GaN with a thickness of 200 μm grown by hydride vapor phase epitaxy. The peak positions were 570.2, 569.6, and 567.4 cm^{-1}, respectively. The blue peak shift of GaN layers from that of bulk GaN indicates that GaN layers are under compressive stress. The shift of E_2 (high) peak from the strain-free bulk GaN has a linear relationship with the residual stress of GaN layer as follows:[31]

$$\sigma_{xx} = \frac{\Delta\omega}{4.3} cm \cdot GPa ,$$

where σ_{xx} and $\Delta\omega$ are biaxial residual stress and Raman shift, respectively. Based on the equation, the residual stresses of GaN on NCPSS and reference GaN were calculated to be 0.51 and 0.65 GPa, respectively. This result shows that the embedded nano-cavity in the GaN layer relaxed the residual stress by 21%. The nano-cavity pattern composed of void and surrounding alumina shell deforms elastically and relaxes the compressive stress of GaN layer.

PL measurement was carried out to characterize the optical properties of GaN layers. Fig. 5.21 shows the PL spectra of GaN layers on the NCPSS and GaN on the planar substrate measured at room temperature. The PL intensity of GaN on the NCPSS is higher than that of GaN on the planar substrate, which indicates the improved crystal quality of GaN layers on the NCPSS. In addition, the position of the near-band-edge (NBE) peak from GaN on the NCPSS is red-shifted compared to that from GaN on the planar substrate,

which reveals that the compressive stress is partly relaxed by the introduction of nano-cavities in the GaN layer. This result showing the relaxation of the residual stress in the GaN layer is consistent with the Raman result.

To investigate the effect of nano-cavities on light extraction, diffuse reflectance spectra of both GaN on the NCPSS and GaN on the planar substrate were measured by collecting the reflected light using an integrating sphere, as shown in Fig. 5.22. There is an abrupt decrease of diffuse reflectance at a wavelength of 365 nm for both GaN layers due to the absorption of light by GaN. A strong Fabry-Perot oscillation was observed for GaN on the planar substrate which has optically flat interfaces at air/GaN and GaN/sapphire substrate, which is attributed to a coherent interference of light from the specular reflection. On the contrary, for GaN on the NCPSS, the Fabry-Perot oscillation was weakened due to the deterioration of coherence of light by the nano-cavities at the GaN/sapphire substrate. The diffuse reflectance of GaN on the NCPSS was enhanced by 54%−62% compared to that of GaN on the planar substrate for the wavelength ranging from 400 nm to 800 nm. The significant enhancement is attributed to the increased probability of light extraction through effective light scattering by nano-cavities as a low refractive index material ($n_{\text{void}} = 1$) introduced at the interface between GaN and the sapphire substrate. From the diffuse reflectance result, we believe that the nano-cavities improve the LEE of visible LEDs over a full visible range of blue, green, and red. The effect of nano-cavities on the light extraction can be further improved by optimizing the size and structure of the nano-cavity patterns.

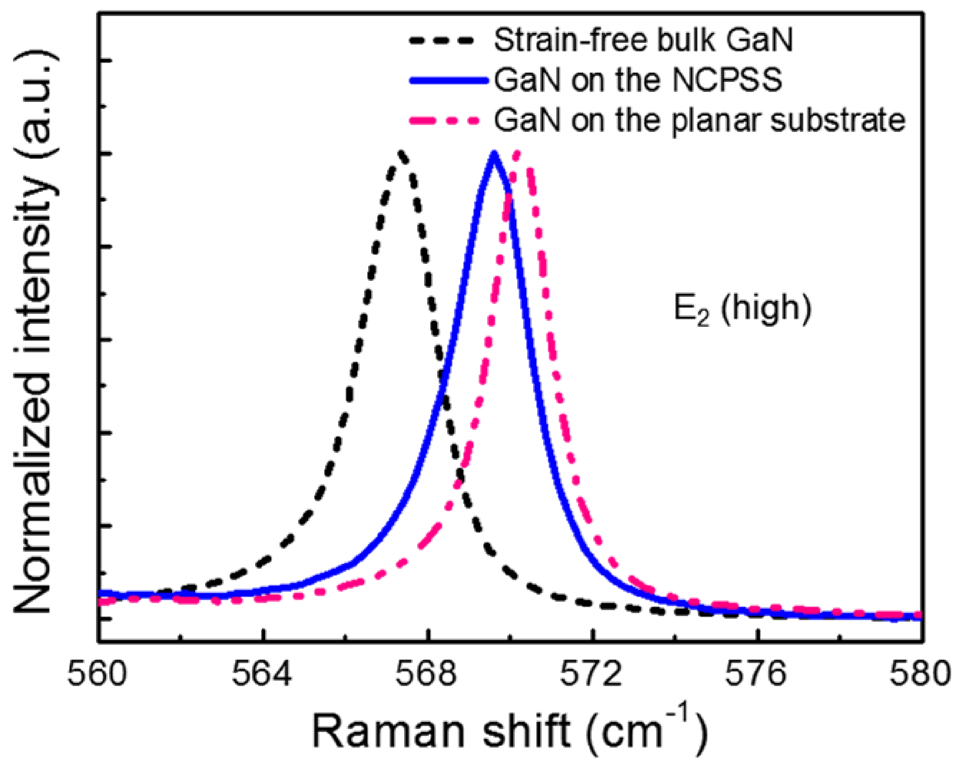

Figure 5.20. E_2 (high) Raman spectra of strain-free bulk GaN, GaN on the NCPSS, and GaN on the planar substrate.

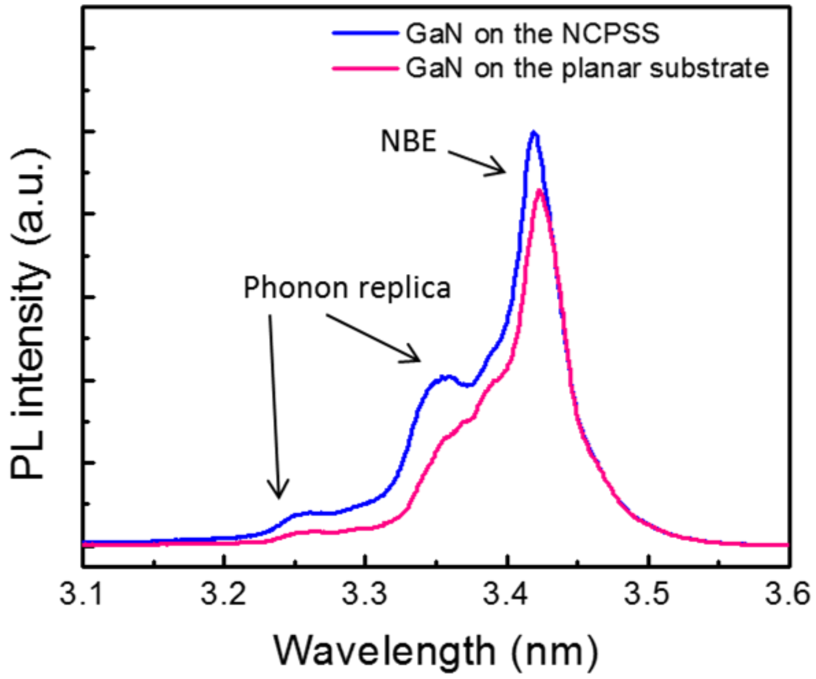

Figure 5.21. PL spectra of GaN on the NCPSS and GaN on the planar substrate measured at room temperature.

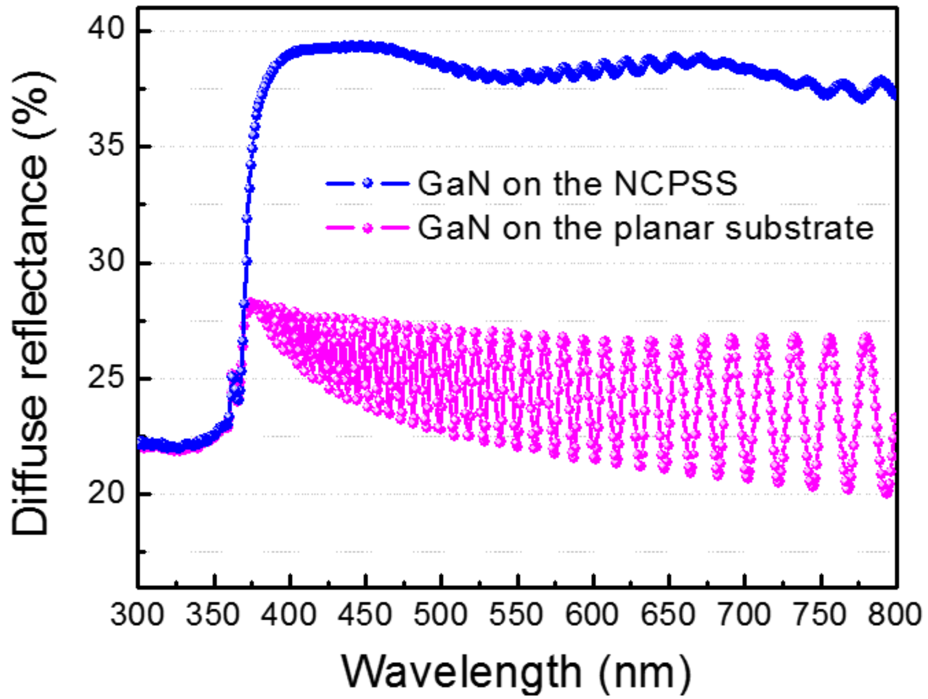

Figure 5.22. Diffuse reflectance spectra of GaN on the NCPSS and GaN on the planar substrate.

5.4 Summary

We report the growth of GaN using the NCPSS which has hexagonally non-close-packed nano-cavity patterns on the sapphire substrate fabricated by the simple and cost-effective PS patterning process. The ELO of GaN on the NCPSS was achieved by the formation of relatively large GaN islands followed by enhanced lateral overgrowth of GaN over several nano-cavity patterns. The TDD of GaN calculated by the CL measurement was significantly reduced from 2.4×10^{8} cm^{-2} to 6.9×10^{7} cm^{-2} by using the NCPSS. The nano-cavities embedded in the GaN layer relaxed the residual compressive stress by 21%. Furthermore, the diffuse reflectance of GaN on the NCPSS was enhanced by 54%−62% compared to that of GaN on the planar substrate. The enhancement is attributed to the increased refractive-index-contrast by introducing the air at the interface between GaN and the sapphire substrate and probability of light extraction through effective light scattering by nano-cavities.

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Chapter 6. Conclusions

The nano-patterned substrates have been proposed to solve the current problems such as high-density dislocations, low LEE, and film stress and to obtain the high quality III-nitride epitaxial layers for important epitaxial structures in the III-nitride LED applications such as GaN on Si substrate, AlN on sapphire substrate, and GaN on sapphire substrate.

Firstly, for the case of *GaN on Si substrate*, NHE of GaN on the AlN/Si(111) nanorod structure was investigated by using MOCVD. Silica nanosphere lithography was employed to fabricate the periodic hexagonal nanorod array with a narrow gap of 30 nm between the nanorods. Fully coalesced GaN film was obtained over the nanorod structure and its TDD was found to decrease down to half, compared to that of GaN grown on the planar AlN/Si(111) substrate. TEM measurement revealed that TD bending and TD termination by stacking faults occurred near the interface between GaN and AlN/Si(111) nanorods, contributing to the TDD reduction. Moreover, the 70% relaxation of the tensile stress of the NHE GaN was confirmed by Raman and PL measurements compared to GaN on the planar AlN/Si(111) substrate. These results suggested that NHE on AlN/Si(111) nanorods fabricated by nanosphere lithography is a promising technique to obtain continuous GaN films with the improved crystalline quality and the reduced residual stress.

Secondly, nano-patterned AlN/sapphire substrate was developed to improve the performance of DUV LEDs, for the case of *AlN on sapphire*

substrate. We demonstrated AlGaN-based DUV LEDs with periodic air-voids-incorporated nanoscale patterns enabled by nanosphere lithography and ELO. The nanoscale ELO on the NPS improved the crystal quality of overgrown epitaxial layers at relatively low growth temperature of 1050 ^{o}C and at small coalescence thickness. The air voids formed in the AlN epitaxial layer effectively relaxed the tensile stress during growth, so that crack-free DUV LED epitaxial layers were obtained on 4-in. sapphire substrate. In addition, the periodically embedded air-void nanostructure enhanced the LEE of DUV LEDs by breaking the total internal reflection that is particularly severe for the predominant anisotropic emission in AlGaN-based DUV LEDs. The LOP of the DUV LEDs on NPS was enhanced by 67% at the injection current of 20 mA compared to that of the reference DUV LEDs. We attribute such a remarkable enhancement to the formation of embedded periodic air voids which cause simultaneous improvements in the crystal quality of epitaxial layers by ELO and LEE enabled by breaking the predominant in-plane guided propagation of DUV photons.

Lastly, the ELO of GaN using the NCPSS, which has hexagonally non-close-packed nano-cavity patterns on the sapphire substrates, was suggested to grow high quality *GaN on sapphire substrate*. The fabrication of the NCPSS was enabled by PS coating followed by deposition of alumina, and thermal annealing. The ELO of GaN using the fabricated NCPSS was investigated. The coalescence of GaN on the NCPSS was achieved by the formation of relatively large GaN islands and ELO of the GaN islands over several nano-cavity patterns. The TDD calculated by CL measurement was

significantly reduced from 2.4×10^8 cm^{-2} to 6.9×10^7 cm^{-2} by using the NCPSS. Dislocation behaviors that contribute to the reduction of TDD of the GaN layer were observed by TEM. Raman spectroscopy revealed that the compressive stress in the GaN layer was reduced by 21% due to the embedded nano-cavities. In addition, the diffuse reflectance of GaN on the NCPSS was enhanced by 54%–62%, which is attributed to the increased probability of light extraction through effective light scattering by nano-cavities.

국 문 초 록

3 족 질화물 반도체는 지난 수십 년 동안 발광다이오드 및 레이져 다이오드와 같은 광전자 소자로의 응용을 위한 가장 유망한 재료 중 하나로 여겨져 왔다. 고효율의 신뢰성 있는 광전자 소자를 구현하기 위해서는 고품질의 3 족 질화물 에피층 성장이 필수적이다. 3 족 질화물의 에피성장에 있어 가장 큰 문제점은 상업적으로 이용 가능한 동종 기판이 없어 여전히 동종 기판 상의 에피성장이 제한된다는 점이다. 이에 따라, 3 족 질화물 에피층은 사파이어 기판 및 실리콘 기판과 같은 이종 기판 상에 성장된다. 그러나, 3 족 질화물 에피층과 기판 사이의 큰 격자 상수 차이 및 열팽창계수 차이로 인해 고밀도의 전위결함이 생성되고, 광추출 효율이 낮으며, 그리고 잔류 응력이 발생하는 문제점이 있으며, 이는 고효율의 3 족 질화물 기반 광전자 소자의 구현을 방해한다. 그러므로, 3 족 질화물 발광다이오드 응용을 위해서는 결함이 적고 응력이 완화된, 그리고 광추출 효율을 향상시키는데 효과적인 고품질의 에피층을 얻는 것이 매우 중요하다. 본 연구에서는 나노패턴된 기판을 제안하여, 3 족 질화물 발광다이오드 응용에 있어 중요한 에피텍셜 구조들인 실리콘 기판 상의 GaN, 사파이어 기판 상의 AlN, 그리고 사파이어 기판 상의 GaN 구조에 대하여 고품질의 3 족 질화물을 얻고자 하였다. 나노패턴된 기판 상 3 족 질화물 에피성장은 유기금속화학기상증착법을 이용하여 연구하였다.

우선, 실리콘 기판 상의 GaN 구조에 대하여, AlN/Si(111) 나노로드 구조 상의 GaN 의 나노이종에피성장에 대한 연구를 진행하였다. 실리카 나노구체 리소그래피를 도입하여 나노로드 사이에 30 nm 의 좁은 간격을 갖는 규칙적인 배열을 갖는 나노로드 구조를 제작하였다. GaN 성장으로 완전히 합쳐진 연속적인 GaN 층을 나노로드 구조 상에 형성하였으며, 관통전위밀도는 평면 구조의 AlN/Si(111) 기판 상에 성장한 GaN 에 비해 절반으로 감소하는 것을 확인하였다. 투과전자현미경 분석으로 GaN 과 AlN/Si(111) 나노로드 사이의 계면 부근에서 관통전위밀도의 감소에 기여하는 관통전위의 휨 현상 및 적층 결함에 의한 관통전위의 종단 현상을 관찰하였다. 또한, 에피층 내부에 형성된 공극으로 인하여 평면 구조의 AlN/Si(111) 기판 상의 GaN 과 비교하여 나노이종에피성장으로 얻은 GaN 의 인장 응력이 70% 감소하였다. 나노구체 리소그래피 방법을 이용하여 제작한 AlN/Si(111) 기판 상의 나노이종에피성장으로 결정성이 향상되고 잔류 응력이 크게 완화된 연속적인 GaN 층을 얻는데 성공하였다.

다음으로, 사파이어 기판 상의 AlN 구조의 경우, 심자외선 발광다이오드의 성능을 향상시키기 위하여 나노패턴된 AlN/sapphire 기판을 제안하였다. 나노구체 리소그래피와 측면에피성장법을 활용하여 주기적인 배열을 갖는 공극이 삽입된 나노크기의 패턴을 적용한 AlGaN 기반 심자외선 발광다이오드를 구현하였다.

나노패턴된 기판 상의 나노 측면에피성장법으로 1050 ºC 의 비교적 낮은 성장 온도와 얇은 두께의 유착 두께로도 AlN 의 측면성장을 가능케 하였으며 에피층의 결정성을 향상시켰다. AlN 에피층 내부에 형성된 공극은 성장 중에 AlN 의 인장 응력을 효과적으로 완화시켰으며, 이를 통해 4 인치 사파이어 기판 상에서 균열이 없는 심자외선 발광다이오드 에피층을 얻을 수 있었다. 또한, 주기적으로 삽입된 나노공극 구조는 빛의 이방성 방출이 우세한 AlGaN 기반 심자외선 발광다이오드의 경우에 있어 특히 심각한 내부전반사 현상을 억제함으로써 광추출 효율을 향상시키는데 효과적임을 확인하였다. 나노패턴된 기판 상에 심자외선 발광다이오드를 제작하였으며, 평면 기판 상의 발광다이오드에 비해 광출력이 67% 증가하였다. 이러한 광출력의 증가는 측면에피성장에 의한 에피층의 결정성 향상과 에피층에 삽입된 공극 구조에 의한 광추출 효율 향상에서 비롯된다.

마지막으로, 우리는 사파이어 기판 상에 고품질의 GaN 를 성장하기 위하여, 사파이어 기판 상에 육각형으로 배열된 나노크기의 공극 패턴을 가진 기판을 제안하였다. 폴리스티렌 구체 코팅과 후속 산화알루미늄 증착 및 열처리에 의해 나노공극이 패턴된 사파이어 기판을 제작할 수 있었다. 나노공극이 패턴된 사파이어 기판 상에서의 GaN 성장연구를 통하여, 상대적으로 큰 GaN 들이 먼저 발달하고, 이러한 GaN 들의 측면에피성장을 통하여 연속적인 GaN 에피층이 형성됨을 확인하였다. 이를 통해

관통전위밀도가 2.4 × 10^8 cm^{-2} 에서 6.9 × 10^7 cm^{-2} 로 크게 감소하였으며, 투과전자현미경 분석으로 관통전위밀도 감소에 기여하는 전위 거동을 관찰하였다. 또한, GaN 에피층과 기판 사이 계면에 삽입된 공극은 잔류 압축 응력을 완화하고, 동시에 효과적인 광 산란으로 광추출 효율을 증가시키는데 효과적이다.

주요어:
에피성장, 3 족 질화물, 나노패턴된 기판, 발광다이오드, 유기금속화학기상증착법, 응력, 광추출, 공극

학번: 2011-22868

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