M.S. DISSERTATION

Electrical Characterization of Si_xTe_{1-x} Chalcogenide Glass for Selector Device Application

Selector Device 를 위한 Si_xTe_{1-x} 칼코제나이드 유리의 전기적 특성

by

Sanggyun Kim

August 2017

DEPARTMENT OF MATERIALS SCIENCE AND ENGINEERING

COLLEGE OF ENGINEERING

SEOUL NATIONAL UNIVERSITY

Abstract

Due to the ongoing advancement in higher density memory technologies, selector devices have become critical components in emerging nonvolatile memories within a passive crossbar array structure. However, the current existing selector devices have been yet to fulfill all the performance requirements necessary for device implementation. The ovonic threshold switching (OTS) device is one of the promising candidates proposed as 3d-stackable selector device composed of chalcogenide material.

In this work, silicon-tellurium binary system is investigated for an OTS selector application. Using triangular pulse measurements, the amorphous Si_xTe_{1-x} ($0.2 \leq x \leq 0.48$) based OTS devices demonstrated high switching speed ($\leq$ 45ns) with low holding voltage ($\leq$ 0.6V). The incorporation of Si in concentrations above 24 at. % decreased the OFF-state resistance owing to the favorable formation of Si_2Te_3 which is known for its hygroscopic nature. The Si-Te binary system was segregated into metallic Te atoms and amorphous SiO_x wherein the formation of Te conductive filament was enhanced by increasing O and Si contents. No siginficant change in V_T, V_H, and t_d was observed with varying Si conc. possibly due to measured portion of the Si_xTe_{1-x} film maintained the same in composition. The OTS behavior exhibited by the Si-Te

system is specuated to be attributed by amorphous Te atoms that migrated between Te nanocrsytalline clusters to create a conductive path.

Keywords: ovonic threshold switching, chalcogenide, selector device
Student Number: 2015-22768
Sanggyun Kim

Table of Contents

List of Tables

List of Figures

Figure 2.3 Structure and energy of simple bonding configurations for amorphous chalcogenides: σ bond orbital (straight line), lone-pair orbital (lobe), and $\sigma*$ antibonding orbital (circle).

Figure 2.4 Charge transfer reaction of chalcogen atoms in amorphous chalcogenide based on VAPs.

Figure 2.5 (a) Electron potential energy profile along the minimum path between localized states S1 and S2: (i) tunneling, (ii) thermal Poole-Frenkel emission, and (iii) thermally-assisted tunneling. (b) Schematic of non-equilibrium energy distribution of electrons in the amorphous chalcogenide.

Figure 3.1 A schematic diagram of lab-made DC sputtering system.

Figure 3.2 A schematic illustration of CBA patterned Si_xTe_{1-x} OTS device

Figure 3.3 The circuit schematic of the electrical circuit used for testing OTS devices. The 81110A pulse generator is used to supply voltage pulses to the OTS device under test (DUT). Current through the DUT is calculated via an internal impedance from the channel 2 of the TDS 684C. The voltage is measured using a Tektronix TDS 684C oscilloscope.

Figure 4.1 The cross-sectional SEM image of Si_XTe_{1-X} films deposited on top of Pt substrate with respect to different compositions.

Figure 4.2 XRD spectrum of 5 different as-deposited Si_XTe_{1-X} films. The broad peak near 27 ^{o} corresponds to tellurium while the high intensity peak near 55^o is from the bare-Si substrate.

Figure 4.3 Time-resolved triangular pulse measurement of $Si_{24}Te_{76}$ OTS device. The following optimized pulse parameters were used to determine V_{TH}, V_H, and t_d: voltage height of 3.5V, pulse width of 800ns, and leading/trailing edge of 800ns.

Figure 4.4 Extracted I-V characteristics from the triangular pulse measurements of (a) $Si_{24}Te_{76}$, (b) $Si_{36}Te_{64}$, and (c) $Si_{48}Te_{52}$ OTS devices. By increasing the Si concentration in Si_XTe_{1-X}, a decrease in OFF-state resistance can be observed.

Figure 4.5 Composition dependence of (a) V_{TH}, V_H, T_d, and (b) ON/OFF ratio.

Figure 4.6 The first DC sweep measurement of 6 different cells (8um x 8um) at each respective Si_XTe_{1-X} composition with compliance current (I_{cc}) of 1.5 mA

for cell-to-cell variation test: (a) $Si_{24}Te_{76}$, (b) $Si_{36}Te_{64}$, and (c) $Si_{48}Te_{52}$. (d) The OFF-state resistance of Si_XTe_{1-X} devices at 1V as function of Si conc.

Figure 4.7 I-V curves of $Si_{24}Te_{76}$, (b) $Si_{36}Te_{64}$, and (c) $Si_{48}Te_{52}$ OTS devices with $(8um)^2$ cell dimension using compliance current I_{CC} of 1.5mA.

Figure 4.8 AES analysis of 100nm thick (a) $Si_{24}Te_{76}$ and (b) $Si_{36}Te_{64}$ thin films on bare-Si substrates.

Figure 4.9 Phase diagram of Si-Te binary system.[22]

Figure 4.10 XPS depth analysis of Si 2p ((a) & (c)) and Te 3d ((b) & (d)) core-level electronic states of $Si_{24}Te_{76}$ and $Si_{36}Te_{64}$, respectively.

Figure 4.11 Schematic illustration of (a) pristine state, (b) electroforming, (c) threshold switching through conductive path, and (d) annealed after forming state in Te-SbO.[26]

1. Introduction

1.1. Background

Owing to the ever-increasing demand for high performance, large capacity, and low cost memory technologies, new non-volatile memories such as resistive RAM (ReRAM), phase-change memory (PCM), and spin-torque transfer magnetic (STT-MRAM) have been investigated as potential alternatives to replace current existing memory technologies.[1] The emergence of new non-volatile memory technologies has been inspired by rising interest in applications which includes storage class memory, embedded non-volatile memory, and neuromorphic computing.[1-3] For these high-density memory applications, crossbar array (CBA) architecture is essential to provide effective cell area of $4F^2$ (F is the minimum feature size) with an excellent scalability.[1] Even higher density memory array can be achieved through 3-dimensional stacking (e.g., 3D Xpoint) or vertical cross-point scheme (e.g., VRRAM).[1,2]

One important challenge pertaining to high-density memory applications is the sneak current that must be accounted for when implementing CBA as it induces undesired memory cell to be biased during a read or write operation. This is enabled due to charges being able to freely flow through the array as no

transistors or diodes exist at each junction. For the read operation, it becomes difficult to accurately sense the state of individual cells. For the write operation, disturbed conditions on unselected cells or incomplete programming of selected cells can be created. Also, without solving the sneak current issue, as the array size increases, large amount of leakage current will cause high power consumption. As a result, suppressing the sneak current in CBA is of utmost importance and this can be achieved by introducing a two-terminal memory selector device with a strong nonlinear current-voltage (I-V) characteristic.

1.2. Selector Device Considerations for 3D Crossbar Memory

1) Two-Terminal Structure

A two-terminal structure is needed to attain minimal single cell area of $4F^2$, reducing the number of space-consuming connections. In addition, it accommodates two-terminal nonvolatile memory elements such as ReRAM and PCM.

2) High ON-State Current Density & Strong Nonlinearity

A selector device connected in series with a memory cell should be able to provide enough current for SET and RESET operations. If this condition is not satisfied, it may lead to undesirable read margin and high-power

dissipation as mentioned previously. In order to sufficiently prevent the leakage current through the unselected cells, the acceptable ON/OFF current ratio is estimated to be ~10^6 which allows maximum tolerable OFF-state leakage for given memory element characteristics and array dimension.[3]

3) Memory Element Compatibility

Resistive memory elements have various working mechanisms that require different read/write conditions. ReRAM consists of metal-insulator-metal (MIM) configuration which depends on redox reactions and the motion of ions. STT-MRAM utilizes magnetization of the storage layer while PCM employs a large contrast between amorphous and crystalline states in chalcogenide material. Accordingly, the performance of an ideal selector device should be comparable or even better than that of the memory element. The parameters to consider for compatibility are SET/RESET voltage, switching speed, cycling endurance, and variability. If the selector device's ON voltage is lower than of the memory element, the selectivity of the device would be degraded.

4) Bidirectional Operation

Some of the emerging new nonvolatile memory technologies are reported to exhibit better performances in bidirectional mode. For instance, in PCM, a bidirectional switching reduces phase/chemical segregation of the

chalcogenide material driven by mechanical stress from incongruent melting and recrystallization, improving its reliability.[4]

5) Back-End-Of-Line (BEOL) Process Compatibility

In order to achieve a high-density memory array, a back-end-of-line (BEOL) fabrication process compatible with 3D multilayer stacking is required. The BEOL process must not exceed thermal budget of ~400C while the selective device itself should endure ~ 400°C at least for 2 hours, which is needed for interconnecting multi-stacked memory elements.[3]

The above discussed selector device requirements make it challenging to realize an ideal selector device compatible with a memory switching element. Among the promising selector device candidates, an ovonic threshold switching (OTS) device based on chalcogenide materials is regarded high due to its excellent scalability, fast operation, and capable in 3D multi-stacking. Nonetheless, high performance OTS device has not been realized as it suffers from low selectivity and poor thermal stability[1]. In spite of these issues, considering high technology maturity behind chalcogenide materials, further optimization of OTS is enabled by combining with wide range of materials.

In this study, co-sputtered Silicon-Tellurium binary system is evaluated for OTS selector application. Tellurium is generally associated with chalcogenides used in phase change memory (e.g., Ge-Sb-Te). Thin films of Si-Te glasses,

100nm thick Si_xTe_{1-x} ($0.2 \leq x \leq 0.48$), were prepared by DC co-sputtering Si- and Te- targets with varying powers and deposition time. The performance of an OTS device based on the effect of Si concentration is assessed by analyzing its transient and I-V characteristics.

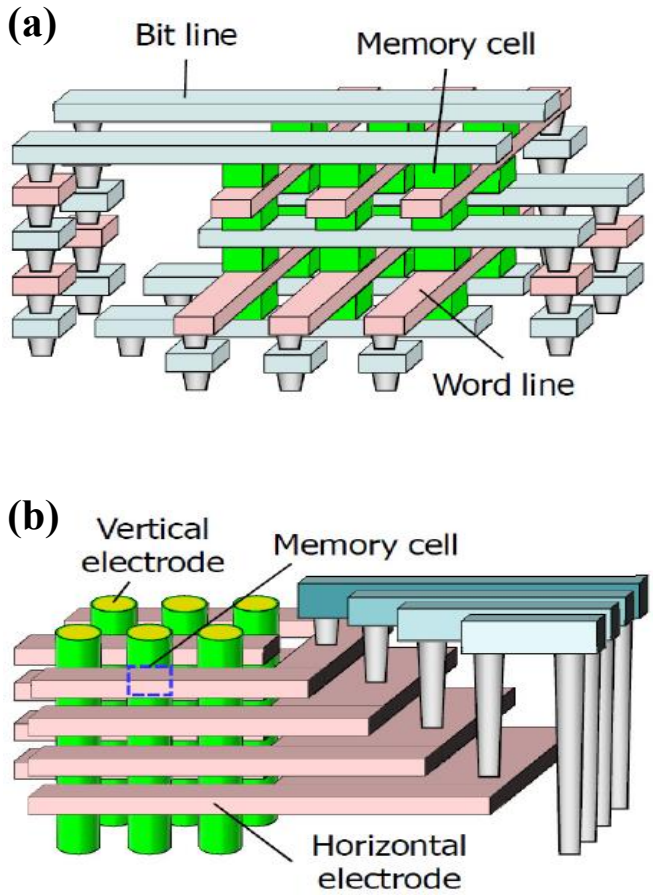


Figure 1.1 Schematic diagrams of (a) 3D crossbar array and (b) vertical cross-point array. The purpose of crossbar array is to attain minimal cell area while maintaining scalability. With 3D integration method, it is a promising approach to enable ultra-high density memory.[5]

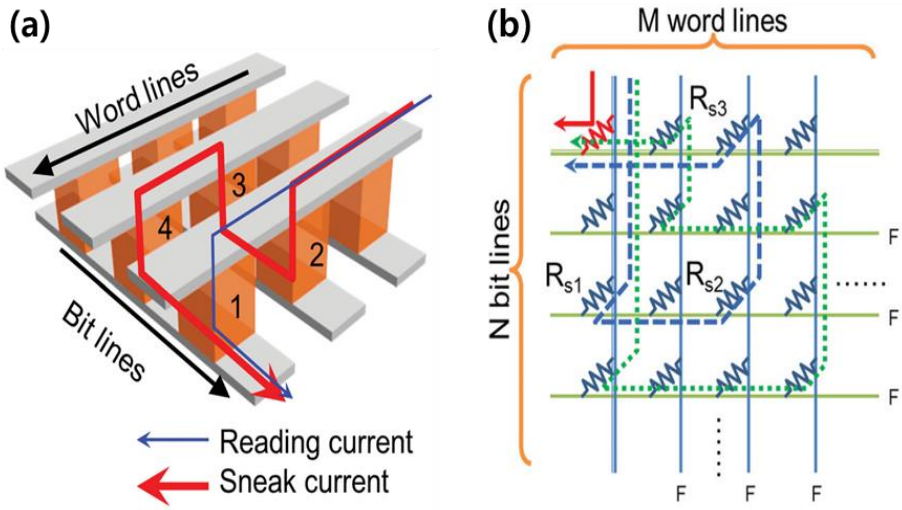


Figure 1.2 (a) Configuration of 2D crossbar array with only resistive switching memory cells illustrating sneak current during read operation. (b) A circuit diagram of crossbar arrays: readout current (red line), possible sneak current path (blue dashed line), and impossible sneak current path (green dashed line). F represents floating.[6]

2. Literature

2.1. Chalcogenide Material

The Group 16 elements in the periodic table are usually defined as chalcogens (e.g., S, Se, and Te), and the term chalcogenide refers to chemical compound comprising of at least one chalcogen element with the addition of electropositive element such as Si, Ge, As, and etc. The oxygen is not classified as a chalcogen element but treated as a distinct class. This can be explained by the difference in band-gap energies in which chalcogenide glasses range between 1 and 3eV while oxygen combined material is more than 5eV.

Chalcogenide materials can be considered unique due to their lone-pair electrons. The amount cross-links and their bonding energies determine the difference between a nonvolatile phase change memory (PCM) and an ovonic threshold switching (OTS) device. For instance, strong and numerous cross-linking atoms such as Si and Ge provide an amorphous material that is structurally not crystallizable. Since lone-pair electrons are nonbonding, when an electrical field beyond a certain threshold value occur, it is electronically switchable through alternating pair of valence electrons which won't disturb its structural stability. The details of the alternating pair of valence electron are discussed in section 2.2.

2.2. Ovonic Threshold Switching

In 1968, Stanford R. Ovshinsky first reported a reversible, rapid switching phenomenon in chalcogenide glass, which bears his name and known as ovonic threshold switching.[7] It was discovered that under critical electric field, fast, reversible electronic transition from high-resistance (OFF) state and low-resistance (ON) state in amorphous chalcogenide with less cross-linking is feasible. The I-V characteristics of an OTS is shown in **Fig. 2.1**. Furthermore, electrically induced reversible amorphous-to-crystalline state in chalcogenide glass is also attainable and is called memory switching. The "SET" process requires an electrical pulse long enough to heat the chalcogenide material above its crystallization temperature while the "RESET" involves an abrupt pulse with a larger electrical current to melt and quench into the amorphous state (**Fig. 2.2**).

In order to explain the unusual switching behavior in chalcogenide glasses, the electronic states of structural defects within the material have been taken into account on the basis of alternating pair of valence electrons from a chemical bonding theory. Simply, of all possible change in ideal bonding configurations, the one that requires the least amount of energy will naturally be present at the highest concentration. It was proposed that least-costly bonding configurations in chalcogenide glasses can be obtained when two defects are created at the same time: a positively charged over-coordinated atom

(C_3^+) and a negatively charged under-coordinated atom (C_1^-).[8] **Fig. 2.3** shows the structure and bonding configuration energy of chalcogenides. Considering the bonding configuration energies of the neutral, disordered chalcogens, the two-fold coordinated (C_2^o) and three-fold coordinated (C_3^o) chalcogen atoms have the lowest energy. However, it can be easily understood that C_3^o is energetically unstable seeing that there is a lower bonding configuration energy when chalcogen atoms are charged which can be seen in the following charge transfer reaction:

$$2C_3^o \rightarrow C_3^+ + C_3^-.$$

Subsequently, C_3^- is also unstable and bring about a spontaneous reaction with the closest-neighboring C_2^o, going through the reaction given by

$$C_3^- + C_2^o \rightarrow C_2^o + C_1^-.$$

The overall reaction is exothermic and it can be expressed as

$$2C_3^o \rightarrow C_3^+ + C_1^-,$$

provided that $2\Delta > U$ where Δ is the bonding repulsive energy and the U is the correlation energy as shown in **Fig. 2.4**. The charged defects produced from the interactions of nonbonding pair electrons in chalcogenide with its local environment or different element are valence alternation pairs (VAPs). It has been suggested that the VAPs and the localized gap state created from the VAPs

are highly responsible for the threshold switching based on the observed trap-limited mobility in amorphous chalcogenide material.[9]

At low applied voltage, the electrons from C_1^- trap sites are removed and converted into C_3^o. Sequentially, the C_3^+ trap sites are neutralized by obtaining the detached electrons from C_1^- trap sites. Chalcogenide glasses have large defect sites roughly between $10^{17} – 10^{19}$ cm^{-3} in which equal concentrations of C_3^+ and C_1^- trap sites are expected to be present.[9,10] As the trap sites are saturated with increasing applied voltage, due to generation of electrons from the conducting material, an abrupt increase in conductivity is observed. The removing of applied bias then will revert the chalcogenide glass back to its equilibrium state. Moreover, the structural stability of the amorphous chalcogenide glass is not weakened given that the lone-pair electrons are nonbonding which makes OTS phenomena repeatable, fast, and nondestructive.

The VAPs theory is based on negative correlation energy which prefers paired electrons in a localized state than single electrons occupying two localized states such as amorphous Si or Ge.[11,12] This is due to strong electron-phonon interaction overcomes the repulsive Coulomb interaction between electrons. The large Stokes shift is a clear indication of lattice relaxation in chalcogenide material.[11] The negative correlation energy gives a plausible explanation to lack of electron spin resonance (ESR) despite large concentration of defects and Fermi-level pinning in the middle of the band gap.[12]

The exact nature of electronic defects in chalcogenide glass is still debated along with its conduction mechanisms. For instance, the structure and reactivities in tellurium compounds cannot be generalized to exhibit similar characteristic of lighter chalcogen elements: S and Se.[13] Nevertheless, it is mutually agreed that the existence of large defect concentrations is crucial to describe the fundamental conduction mechanism of OTS and PCM.

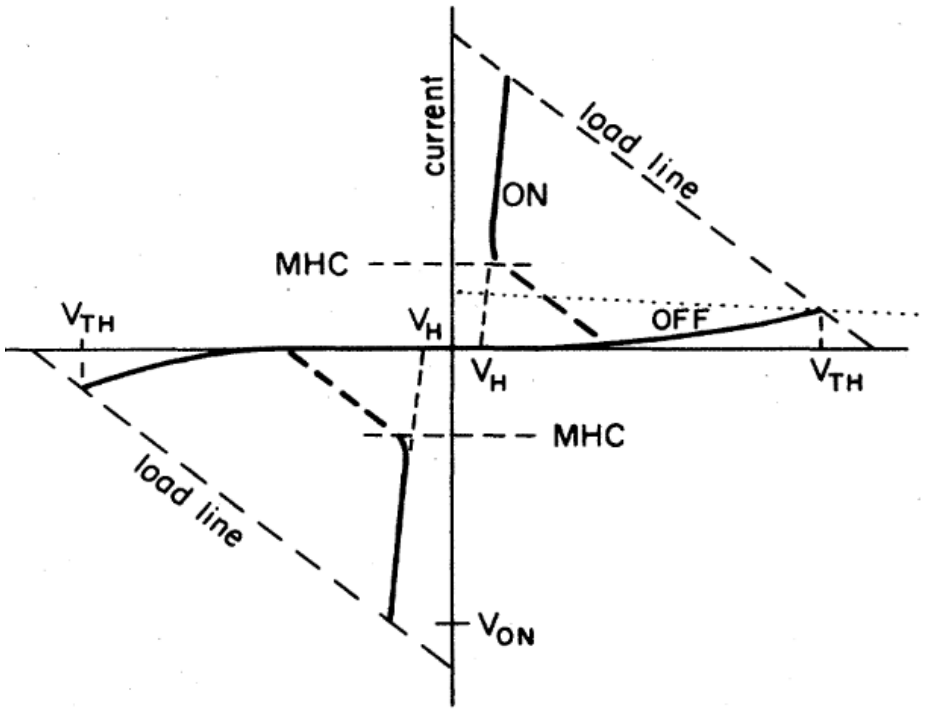


Figure 2.1 I-V characteristic of an OTS device. Above the threshold voltage (V_{TH}), the highly resistive OTS rapidly switches to highly conducting "ON" state. The highly conducting "ON" state can be maintained as long the minimum holding voltage (V_H) is applied.[14]

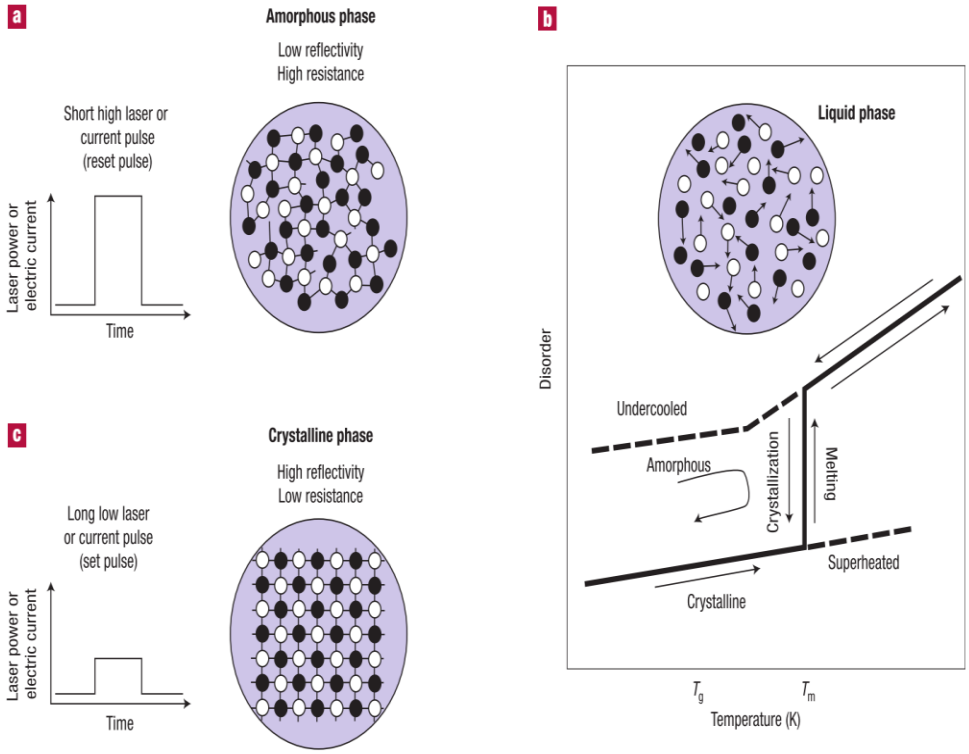


Figure 2.2 The schematic diagram of PCM cell programming. By modulating the electrical pulses of the write operation, intermediate resistance states can be obtained, allowing multilevel-cell (MLC).[15]

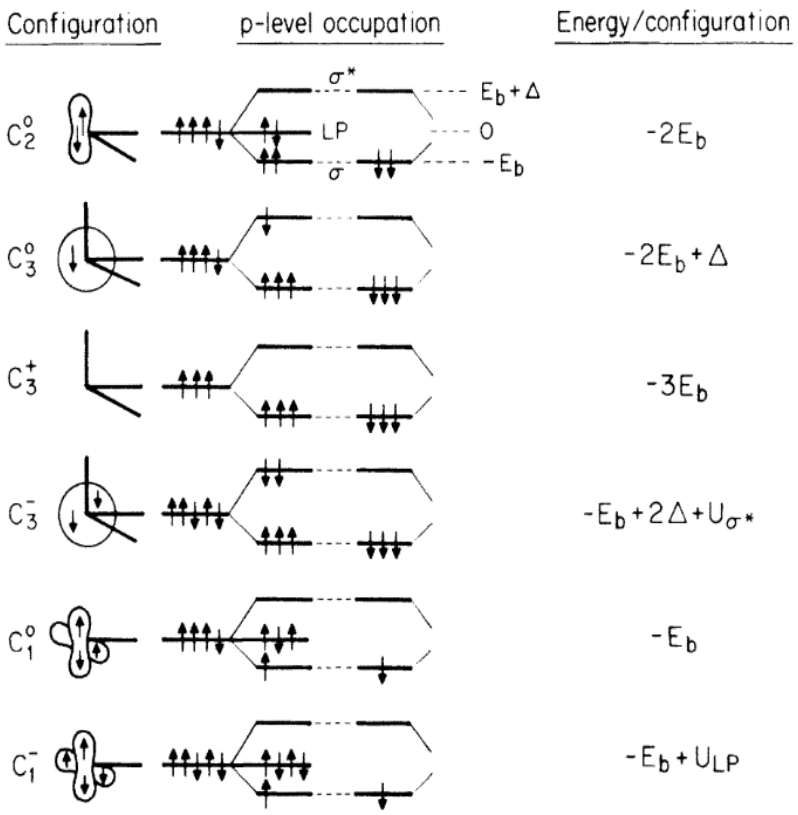


Figure 2.3 Structure and energy of simple bonding configurations for amorphous chalcogenides: σ bond orbital (straight line), lone-pair orbital (lobe), and $\sigma*$ antibonding orbital (circle).[8]

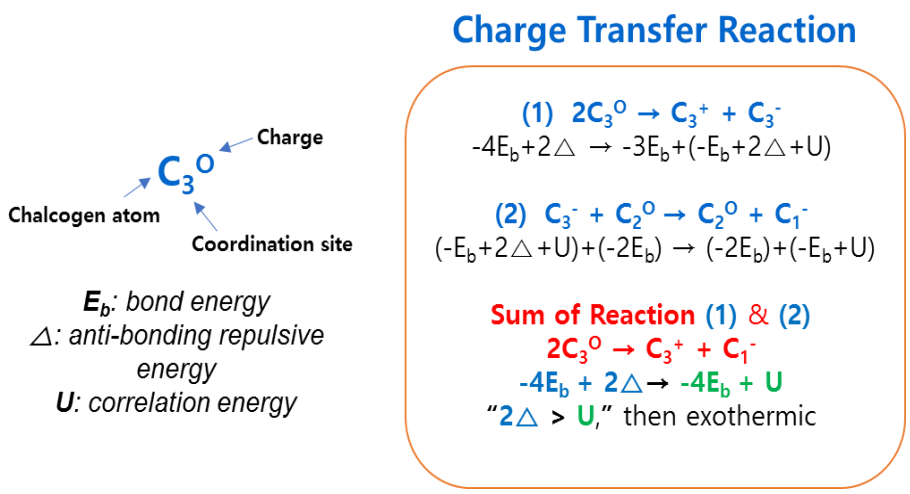


Figure 2.4 Charge transfer reaction of chalcogen atoms in amorphous chalcogenide based on VAPs.

2.3. Conduction Mechanism of Chalcogenide Glass

Various electronic conduction models have been proposed to provide a comprehensive analytical electronic switching model of OTS. In Adler's model, the first agreeable OTS model, the sub-threshold hold region is explained by Poole-Frenkel (PF) effect while the threshold switching is described by Shockley-Hall-Read (SHR) recombination with impact ionization.[9] Nonetheless, there are some issues that have not been addressed within this model: thermal dependence of threshold switching and occurrence of impact ionization. Adler proposed that OTS behavior is an electronic phenomenon and disregarded the thermal process. In addition, Adler did not clarify on how impact ionization could occur within the low carrier mobility system of chalcogenides; the carrier scattering length is much shorter compared to the path length to attain adequate energy for impact ionization.[7] The same model was extended or modified by Redaelli in which formation of current filament is not necessary to explain the switching event unlike Adler's model.[10]

In Ielmini's model, PF effect and thermally assisted hoping transport were utilized to demonstrate the conductivity in subthreshold region.[16] At the same time, non-equilibrium high-energy distribution of trapped electrons was used to describe threshold switching event. The non-equilibrium high-energy distribution means that carriers in the traps that give rise to the sub-threshold conductivity process also can take advantage of field-induced barrier lowering

to tunnel into empty states of higher energies which can be seen in **Fig. 2.5**. This model was put into simulation and displayed a good fitting with measured data, explaining both the temperature and thickness dependencies of the chalcogenide material. However, it has been reported that hopping transport is not possible due to strong polaron effect in chalcogenide material.[12] Polaron effect is defined as trapped carriers that are accompanied with self-induced lattice deformation. Therefore, it will be difficult for trapped carriers to move to the next/higher trap site carrying its lattice deformation.

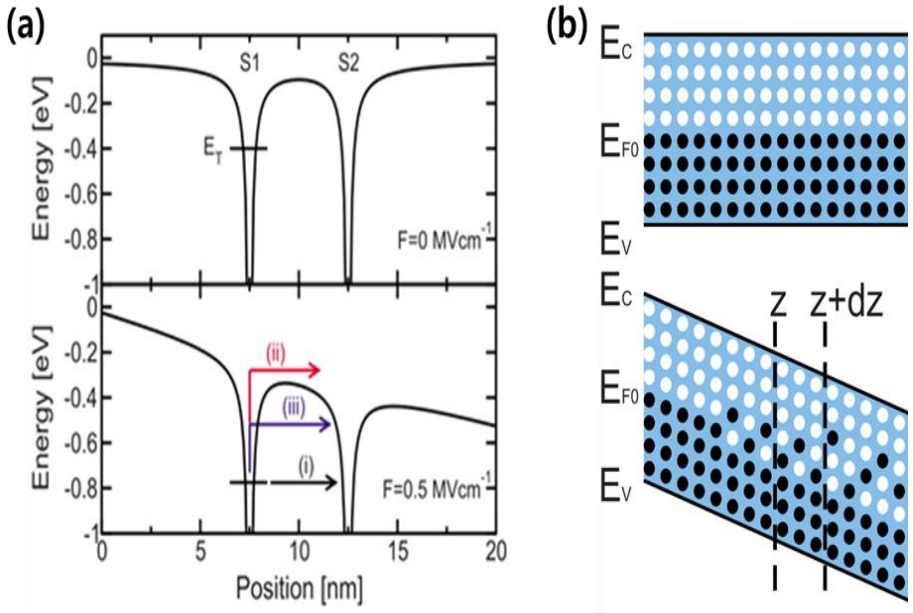


Figure 2.5 (a) Electron potential energy profile along the minimum path between localized states S1 and S2: (i) tunneling, (ii) thermal Poole-Frenkel emission, and (iii) thermally-assisted tunneling. (b) Schematic of non-equilibrium energy distribution of electrons in the amorphous chalcogenide.[16]

3. Experimental Method

3.1. DC Co-sputtering of Si_xTe_{1-x} Thin Film

Si_xTe_{1-x} thin film was deposited at room temperature on 4 different types of substrates by DC co-sputtering Si- and Te- targets: sapphire (Al_2O_3), bare-Si, Pt (80nm of Pt/20nm of Ti adhesion layer), and patterned CBA (50nm of Pt/20nm of Ti adhesion layer). The 100nm thick Si_xTe_{1-x} thin films with compositions ranging between 20 at. % Si to 50 at% Si were obtained through varying plasma power (Si: 20W–50W, Te: 5W) and deposition time. **Fig. 3.1** displays the schematic diagram DC sputtering system utilized in this study. **Table 1** summarizes the details of the deposition conditions used throughout this work.

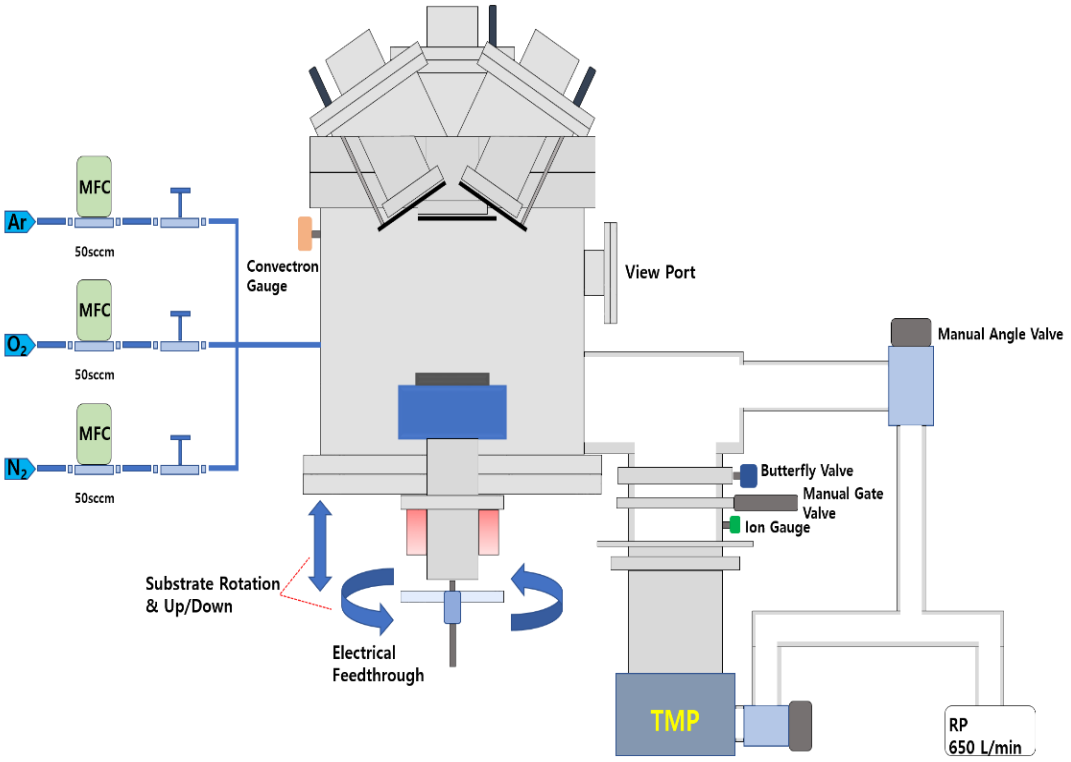


Figure 3.1 A schematic diagram of lab-made DC sputtering system.

Table 3.1 Deposition conditions for DC Sputtering of Si_xTe_{1-x} OTS film.

DC Sputtering Condition of Si_XTe_{1-x}		
Base Pressure (Torr)	$\leq 9.5 \times 10^{-7}$	
Working Pressure (Torr)	6×10^{-3}	
Argon Gas (sccm)	*10*	
Rotation Speed (RPM)	*15*	
Temperature (^{o}C)	*22 - 26*	
Sputtering Power (W)	**Si**	**Te**
	20 – 50	*5*

3.2. CBA Device Fabrication

The crossbar structured OTS device used in this study consists of Si_xTe_{1-x} chalcogenide film enclosed between two metallic contacts, serving as the top and the bottom electrodes. The devices were fabricated on ultra-sonicated SiO_2 substrates of 20mm X 20mm under acetone, isopropanol, and distilled water which was then dried with N_2 gas. The crossbar patterned top (50nm of Pt) and bottom (50nm of Pt/20nm of Ti adhesion layer) electrodes were deposited by e-gun evaporator (Mastech, ZZS550-2/D) and defined through conventional photolithography (Karl-Suss, MA6 II) with a lift-off process. For the bottom electrode, Pt/Ti adhesion layer is an in-situ process and the Pt is used to prevent Ti oxidation. The detailed schematic of CBA structure and device fabrication process are shown in **Fig. 3.2** and **Table 3.2**, respectively. The active cell dimension of 4um X 4um, 6um X 6um, and 8um X 8um was used for DC I-V sweep and triangular pulse measurement.

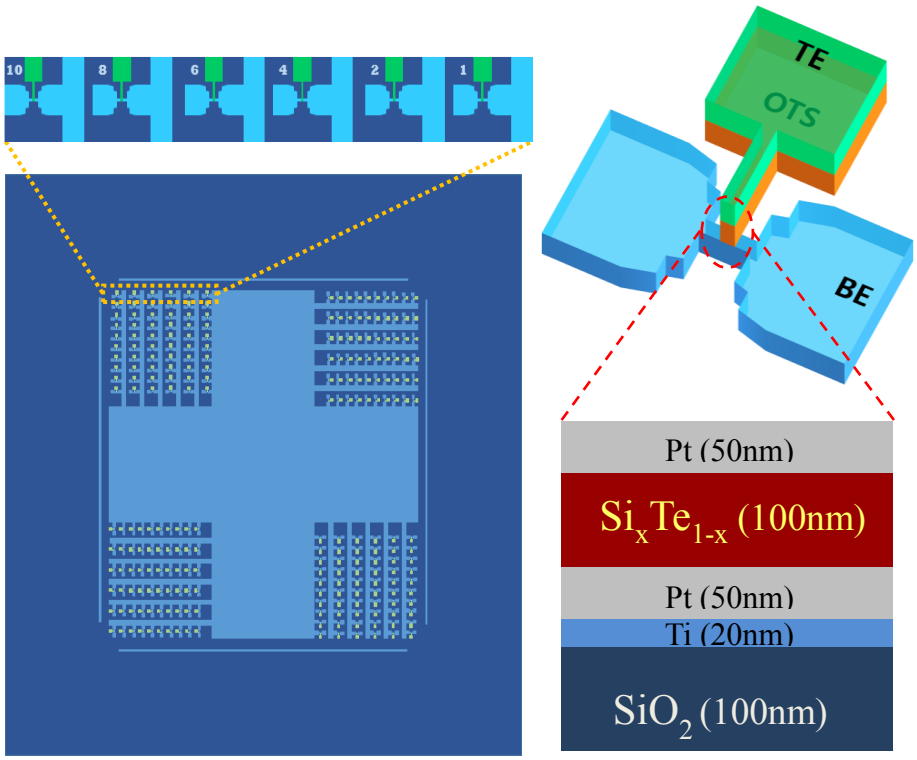


Figure 3.2 A schematic illustration of CBA patterned Si_xTe_{1-x} OTS device.

Table 3.2 Lift-Off Process for CBA patterned Si_xTe_{1-x} OTS device.

No.	Process	Seq.	Recipe	
1	Organic Cleaning of SiO_2 (100nm)/ Bare-Si	1	Acetone	10 min
		2	IPA	2 min
		3	DI Water	2 min
		4	N_2 Gun	-
2	BE (50nm of Pt/20nm of Ti) or TE (50nm of Pt)	1	HMDS + PR (AZ5214)	-
		2	Soft Bake @ 95°C	90 sec
		3	Align + Exposure (HARD)	3.2 sec
		4	Hard Bake @ 110°C	180 sec
		5	Flood Exposure	60 sec
		6	Develop (AZ300)	35 sec
		7	DI Gun/N_2 Gun	
		8	Evaporation of Metal	
		9	Lift-Off with Acetone/DI Gun/N2 Gun	

3.3. Thin Film Analysis

3.3.1. Chemical Analysis

For composition analysis, Si_XTe_{1-x} film was examined by X-ray fluorescence analysis (Thermo Scientific, ARL Quant'X EDXRF). The depth profiles of X-ray photoelectron spectroscopy (VG Scientific, XPS) were performed to determine the chemical bonding states of the deposited film. The impurity level was confirmed via Auger electron spectroscopy (ULVAC-PHI, AES, PHI 700).

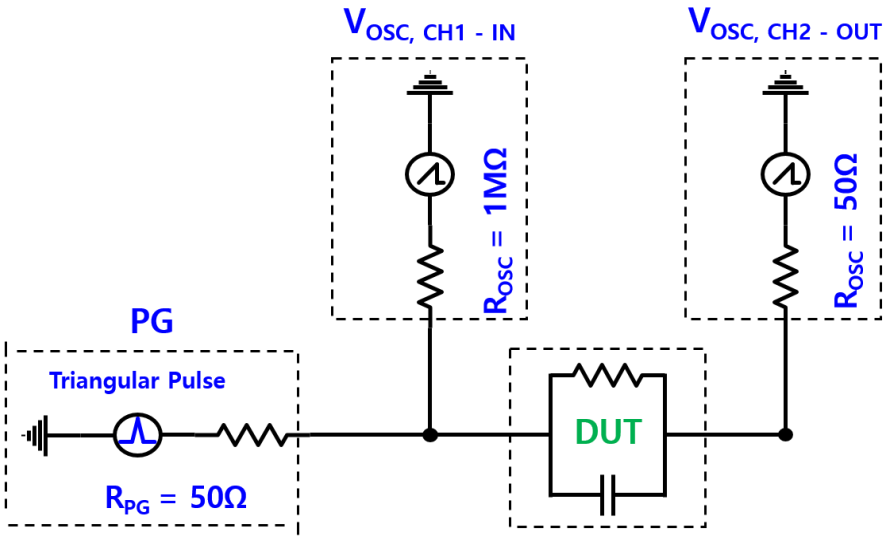
3.3.2. Structure Analysis

The crystallinity and thickness of the film was measured with X-ray diffraction (XRD) and X-ray reflectivity (XRR) using X-ray diffractometer (PANalytical, X'Pert PRO MPD). For 100nm thick Si_xTe_{1-x} film, cross-sectional image was obtained by field-emission scanning electron microscope (Hitachi S-4800, FE-SEM). Spectroscopic ellipsometry (J. A. Woodlam Co. Inc, ESM-300) was used to cross-check the film thickness obtained from XRR.

3.3.3. Electrical Measurement

The DC I-V sweep measurements of CBA patterned Si_xTe_{1-x} cells were performed by using semiconductor parameter analyzer (Hewlett-Packard, SPA 4145B). The switching dynamics of OTS devices were tested with a pulse generator (Agilent, 81110A) to switch to on or off state while an oscilloscope

(Tektronix, TDS 684C) was used to determine the voltage drop across the device. By utilizing the fixed internal impedances of the analyzer in series with the device under test (DUT), one is able to obtain the current through the DUT from channel 2 of the oscilloscope. As a result, the device's resistance can be calculated by taking the difference between the input voltage from the channel 1 and the output voltage from channel 2, and then dividing it with the measured current passing through the DUT which can be seen in **Fig. 3.3**. The internal impedance of channel 1 has been set high in order to ensure the majority of current passes through the DUT, making the measured currents more reliable.



$$V_{DUT} = V_{OSC,CH1} - V_{OSC,CH2}$$

$$I_{DUT} = I_{OSC,CH2}$$

$$R_{DUT} = \frac{V_{DUT}}{I_{OSC,CH2}}$$

Figure 3.3 The circuit schematic of the electrical setup used for testing OTS devices. The 81110A pulse generator is used to supply voltage pulses to the OTS device under test (DUT). Current through the DUT is calculated via an internal impedance from the channel 2 of the TDS 684C. The voltage is measured using a Tektronix TDS 684C oscilloscope.

4. Experimental Results and Discussions

4.1. Characterization of Sputtered Si_XTe_{1-X} Thin Film

The Si_XTe_{1-X} ($0.2 \leq x \leq 0.48$) films were deposited at room temperature through co-sputtering Si- and Te- single targets, simultaneously. In order to obtain 100nm thick Si_XTe_{1-X} film within the desired composition range mentioned above, composition and growth rate of the films with respect to different sputtering power of Si and deposition time were determined by XRF and XRR; the Te sputtering power was fixed at 5W. The thickness of the Si_zTe_{1-x} on 80nm Pt layer was 100nm, as confirmed by SEM shown in **Fig. 4.1**. Furthermore, it was expected that Si_xTe_{1-x} film with increasing Si concentration would be susceptible toward crystallinity as it required higher Si sputtering power. However, in **Fig. 4.2**, the XRD spectra did not reveal any significant peak from the as-deposited Si_XTe_{1-X} film, indicating its amorphous state. A broadened Te peak was observed near 27° given that the crystallization temperature is estimated to be 10 °C.[17]

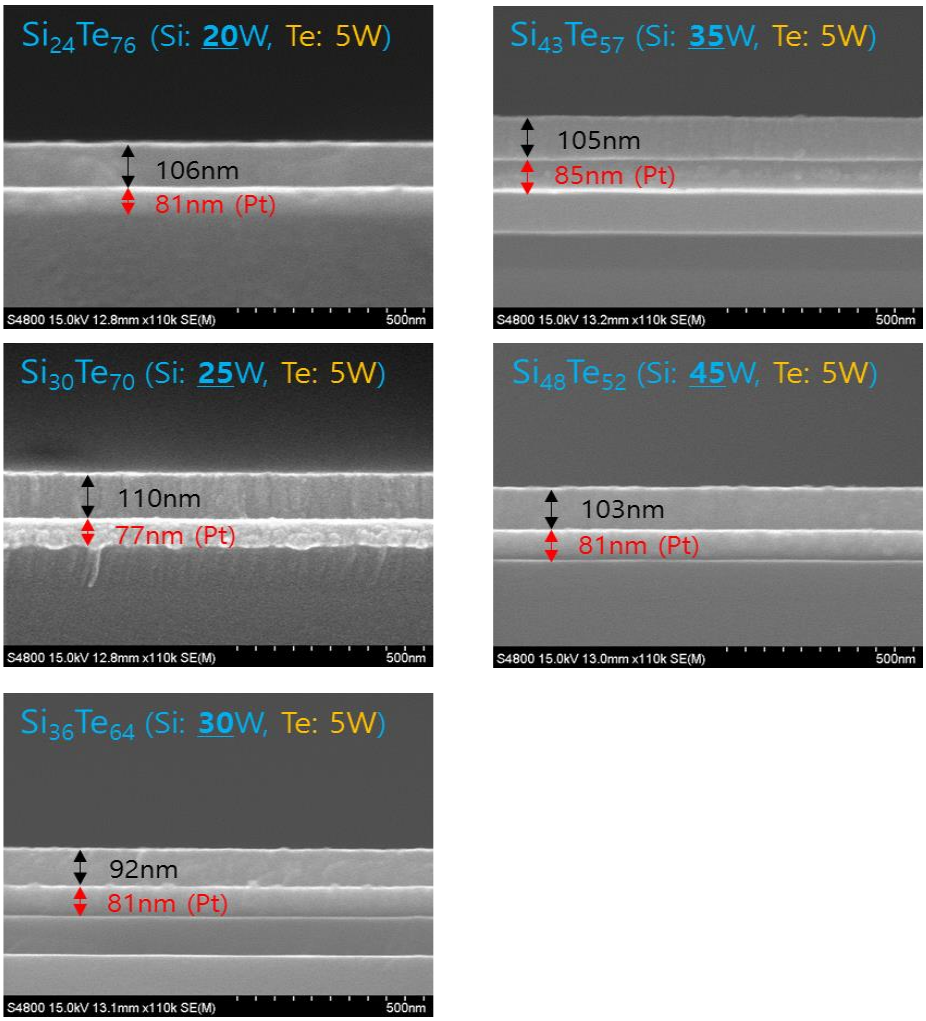


Figure 4.1 The cross-sectional SEM image of Si_XTe_{1-X} films deposited on top of Pt substrate with respect to different compositions.

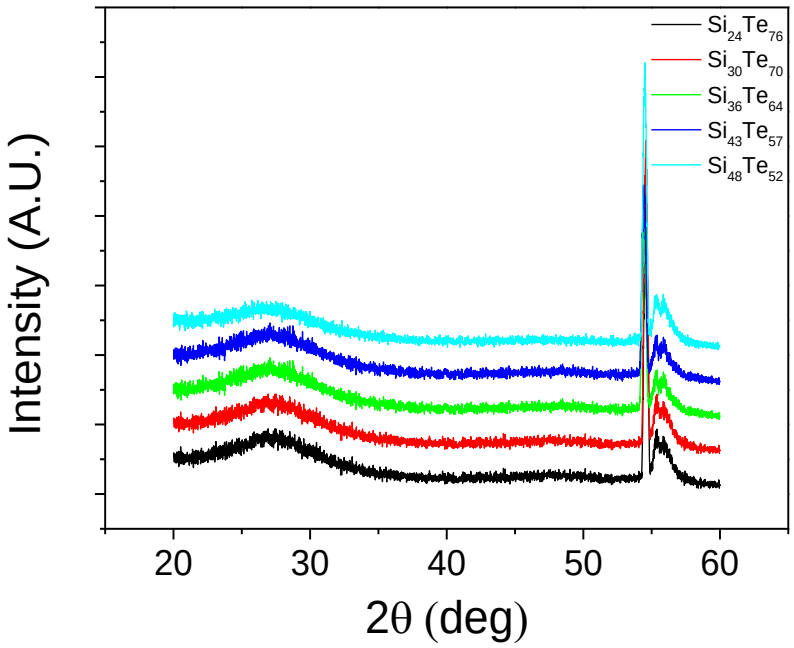


Figure 4.2 XRD spectrum of 5 different as-deposited Si_XTe_{1-X} films. The broad peak near 27 ^{o} corresponds to tellurium while the high intensity peak near 55^o is from the bare-Si substrate.

4.2. Electrical Properties

The threshold switching behavior of amorphous Si_xTe_{1-x} based OTS devices with cell area of $16um^2$ were characterized via triangular pulse measurement. The fabricated OTS cell consist of Si_xTe_{1-x} (100nm) sandwiched between two inert Pt (50nm) electrodes. The fabrication process of CBA patterned Si_xTe_{1-x} OTS device is described in section **3.1** and **3.2**. Unlike conventional DC I-V sweep measurement, pulse measurement reduces both the thermal and electrical stresses from inducing irreversible changes in device characteristics. Moreover, transient parameters of the OTS device such as delay time (t_d) can be assessed; t_d is defined as the time between onset of threshold voltage (V_T) and termination of breakdown in electronic resistivity.[18] A precise measurement of transient parameters can be obtained by optimizing applied voltage pulse parameters: leading edge (rise time), pulse width, and trailing edge (fall time). A steep leading edge is used to determine accurate t_d while long trailing edge enables precise measurement of the holding voltage (V_H). Finally, the pulse width modulates the crystallization of the OTS device. For this study, voltage pulse height of 3.5V and lead/trail edges as well as pulse width of 800ns were utilized.

Fig. 4.3 shows the time-resolved threshold switching behavior of $Si_{24}Te_{76}$ OTS device. The device remains in high resistive OFF-state until it reaches threshold voltage of 2.36V wherein the device's current rapidly increases into low

resistive conducting state (ON). Owing to the triangular-shaped voltage pulse, crystallization of the OTS can be lessened as the duration of the electrical/thermal stress at high voltage is shortened. The device transitions back to high resistive OFF state below V_H of 0.45V.

From the triangular pulse measurement, I-V characteristics can also be extracted to evaluate the on/off ratio and snap-back phenomena by adopting the equations in **Fig. 3.3**. The threshold switching behavior and I-V characteristics for Si_xTe_{1-x} OTS device with 3 different Si concentrations is depicted in **Fig. 4.4**. The given Si_xTe_{1-x} OTS devices demonstrated rapid transition from high-resistance state to low-resistance despite the significant noise at its OFF state. This may be due to the highly intrinsic disordered nature of the Si_xTe_{1-x} or mismatch of internal impedance within the electrical setup.[19,20] During the trailing edge, it was observed that the device switches back into its highly resistive state which indicates its amorphous nature.

Using the aforementioned pulse parameters, the I-V characteristics of the OTS devices with varying Si concentrations are shown in **Fig. 4.5**. At each respective composition of Si_xTe_{1-x}, 10 repeated measurements were taken from each cell out of 5 different. It was expected that increase in Si concentration would result in higher V_T and t_d due to rise in defect concentrations (e.g., dangling bonds) and cross-linking bonds. Nevertheless, no significant trends were observed in

V_T, V_H, and t_d (**Fig. 4.5 (a)**). The switching speed of less than 45ns was obtained with low V_H under 0.6V to sustain its conducting state. On the other hand, it can be noted that the OFF-state resistance decreased with increasing Si concentration as shown in **Fig. 4.4**. Consequently, the on/off ratio was reduced with higher Si concentration **(Fig. 4.5 (b)**).

In order to verify its unusually low OFF-state resistance, DC voltage sweeps were conducted on 6 cells (8um X 8um) for 5 different compositions with compliance current (I_{cc}) of 1.5mA. The resistance of the OTS device was measured at 1V which is below the threshold region as displayed in **Fig. 4.6**. The obtained I-V curves are based on the first DC sweep measurement from each cell. As all the cells from its corresponding compositions showed similar behavior in terms of V_T and OFF-state resistance, cell-to-cell variation due to fabrication process was excluded. Furthermore, volatile threshold switching behavior through positive voltage sweep was demonstrated in **Fig. 4.7**. It is important to mention that above 24 at. % of Si concentration, electroforming process was observed regularly. Electroforming can be described as formation of highly conducting filament that is possibly crystalline.[21]

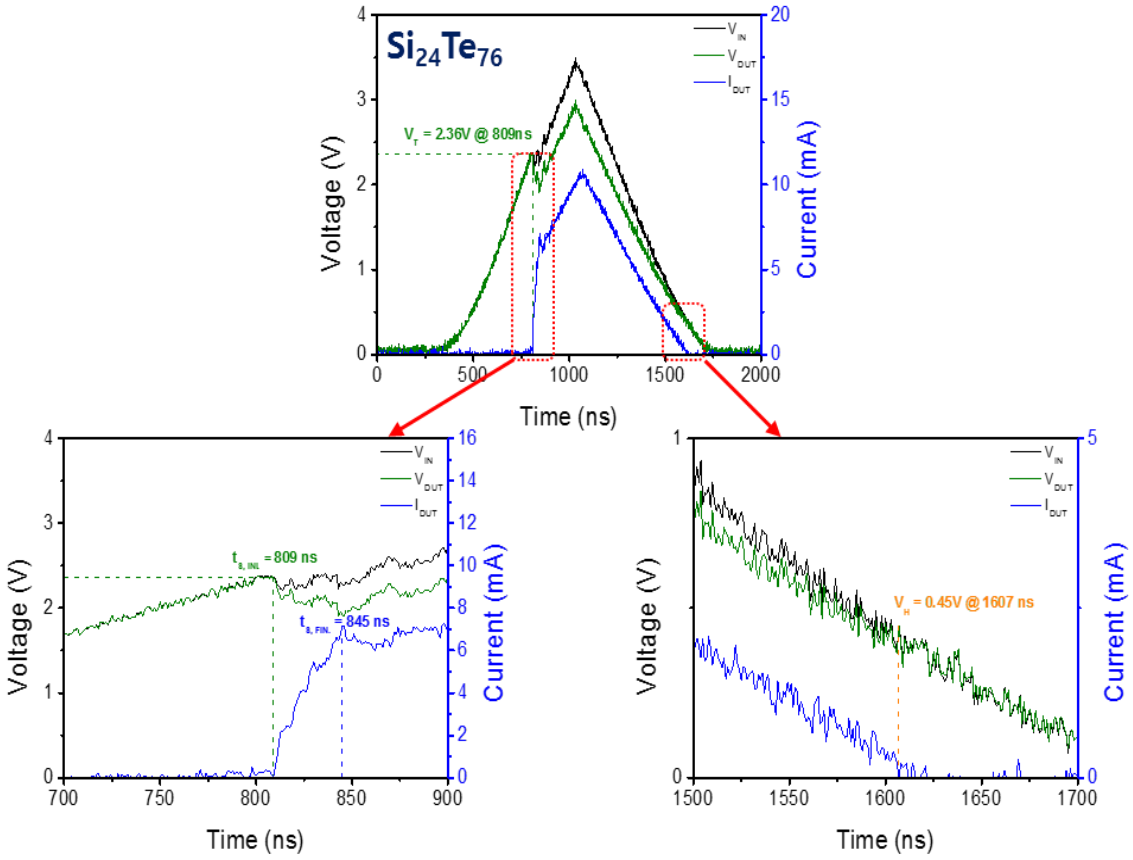


Figure 4.3 Time-resolved triangular pulse measurement of $Si_{24}Te_{76}$ OTS device. The following optimized pulse parameters were used to determine V_{TH}, V_H, and t_d: voltage height of 3.5V, pulse width of 800ns, and leading/trailing edge of 800ns.

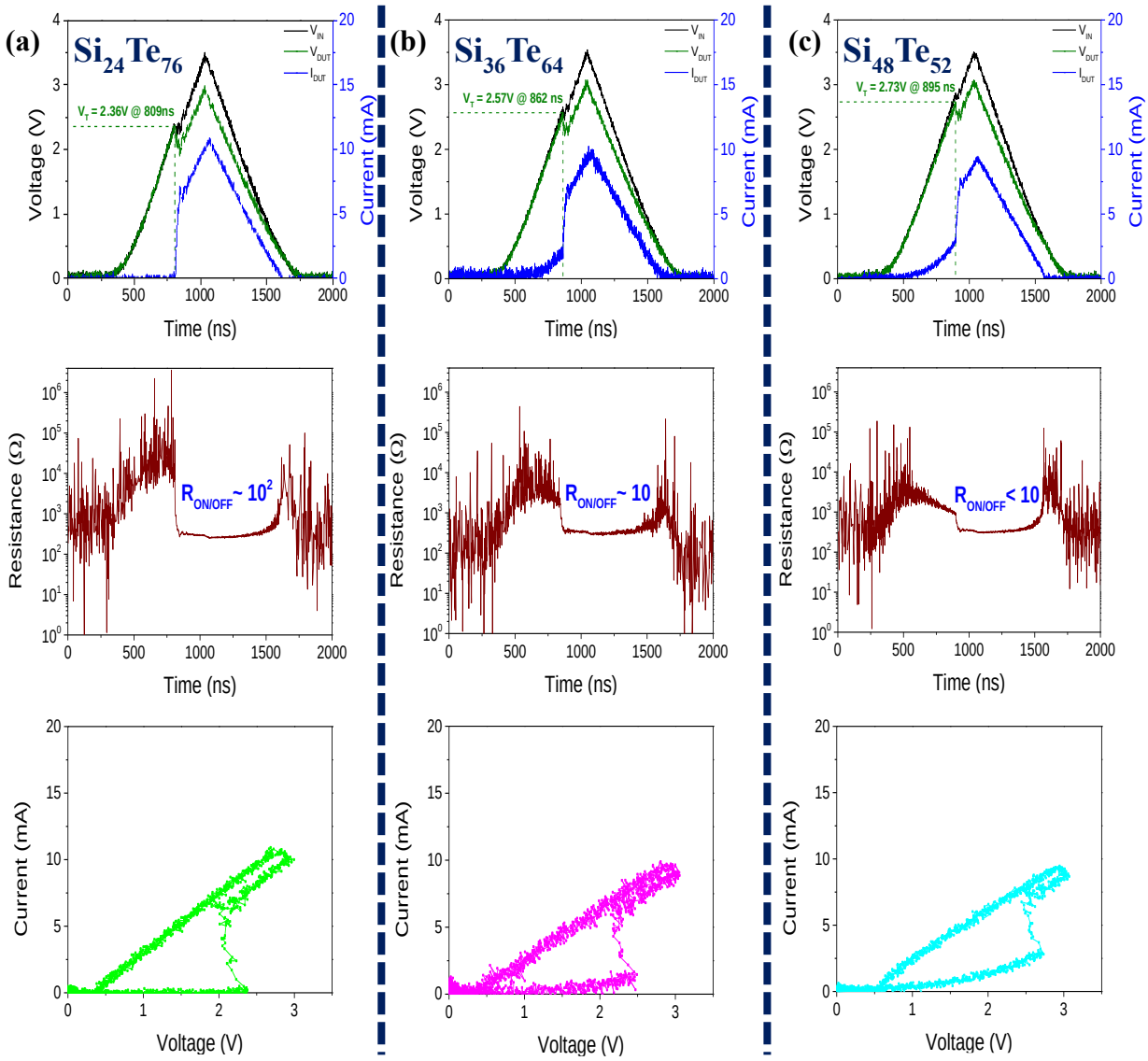


Figure 4.4 Extracted I-V characteristics from the triangular pulse measurements of (a) $Si_{24}Te_{76}$, (b) $Si_{36}Te_{64}$, and (c) $Si_{48}Te_{52}$ OTS devices. By increasing the Si concentration in Si_XTe_{1-X}, a decrease in OFF-state resistance can be observed.

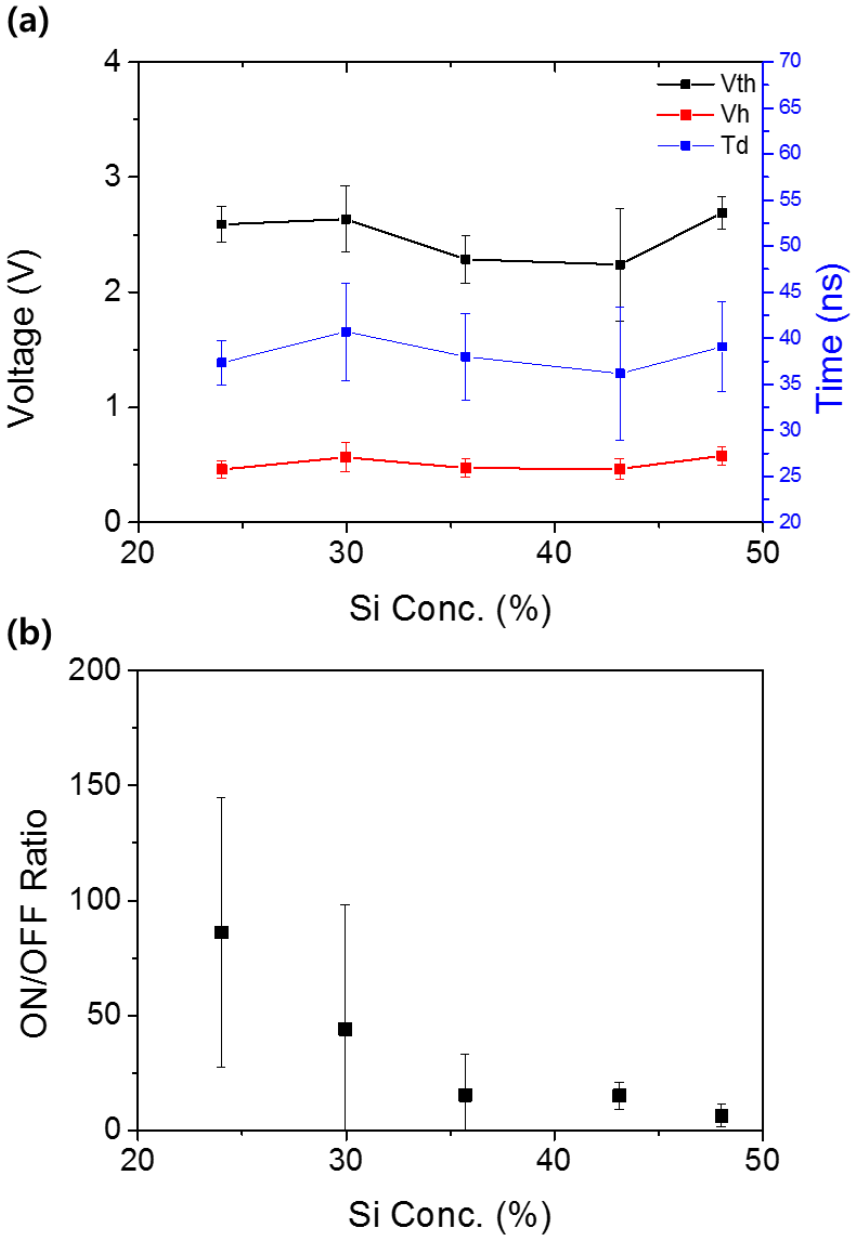


Figure 4.5 Composition dependence of (a) V_{TH}, V_H, T_d, and (b) ON/OFF ratio.

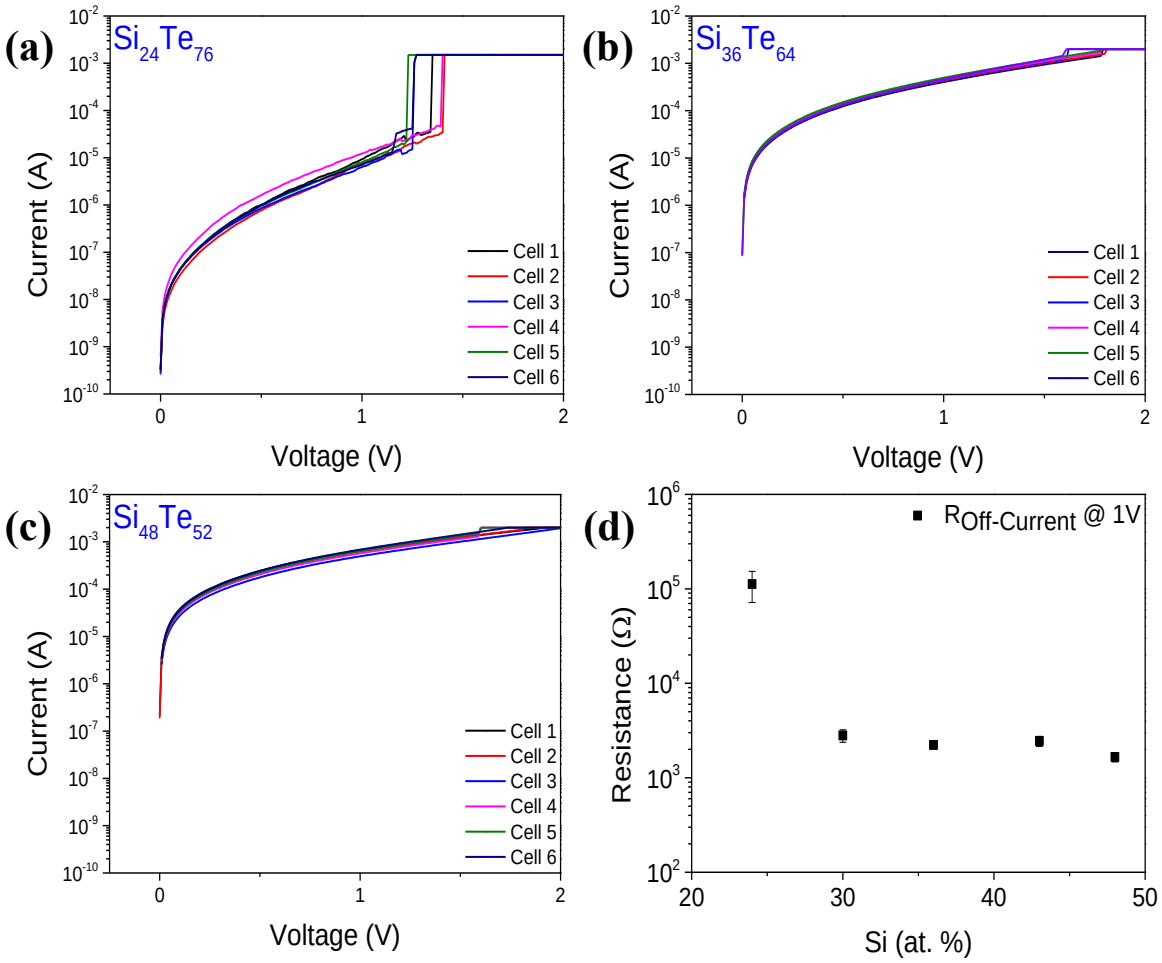


Figure 4.6 The first DC sweep measurement of 6 different cells (8um x 8um) at each respective Si_XTe_{1-X} composition with compliance current (I_{cc}) of 1.5 mA for cell-to-cell variation test: (a) $Si_{24}Te_{76}$, (b) $Si_{36}Te_{64}$, and (c) $Si_{48}Te_{52}$. (d) The OFF-state resistance of Si_XTe_{1-X} devices at 1V as function of Si conc.

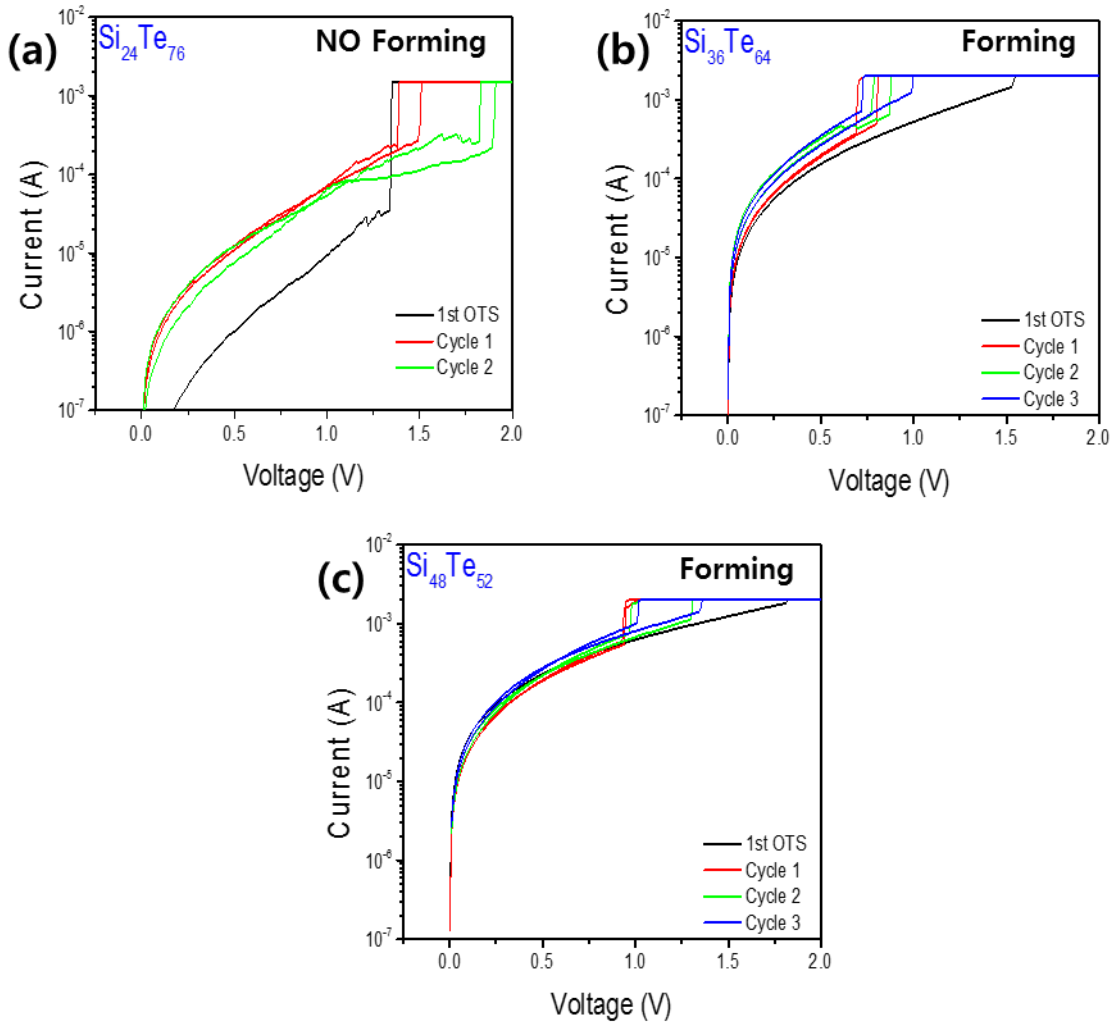


Figure 4.7 I-V curves of $Si_{24}Te_{76}$, (b) $Si_{36}Te_{64}$, and (c) $Si_{48}Te_{52}$ OTS devices with $(8um)^2$ cell dimension using compliance current I_{CC} of 1.5mA.

4.3. AES and XPS Analysis

Fig. 4.8 shows the AES profile of the 100nm thick $Si_{24}Te_{76}$ and $Si_{36}Te_{64}$ films on bare-Si substrates. The initial elemental composition analysis by means of XRF was in good agreement with AES data with respect to Si conc. and Te conc. It was also revealed that not only silicon and tellurium but oxygen was present as well, consistently throughout the film. The O content was observed to rise further with increasing Si conc.

It has been reported that Si_2Te_3 is the only compound in solid state present within silicon-tellurium binary system and it is very hygroscopic.[22,23] The hygroscopic reaction of Si_2Te_3 is shown as

$$Si_2Te_3 + 4H_2O \rightarrow 2SiO_2 + 2H_2Te + Te + 2H_2.$$

Considering the favorable formation of Si_2Te_3 near 60 at. % Te as illustrated in Si-Te phase diagram (**Fig. 4.9**), oxidation of Si_XTe_{1-X} OTS device above 24 at. % Si is one possible explanation for increase in oxygen conc. with Si conc. Furthermore, the oxygen content is likely to be the cause for electroforming and increase in V_T. This is because of many amorphous oxide thin films that exhibit threshold switching or memory switching goes through the electroforming process.[24]

XPS depth analysis was performed to investigate chemical binding states of

Si and Te within the as-deposited $Si_{24}Te_{76}$ and $Si_{36}Te_{64}$ films. The Si 2p core level spectra of XPS (**Fig. 4.10 (a) & (c)**) displays 3 peaks near 97eV, 99eV, and 102eV which reflects Si-Si, Si-Te, and Si-O binding energy, respectively. Even though there has been no report in binding energy of Si-Te, the peak located near 99eV can be recognized as Si-Te binding energy when taking into account of bond dissociation energies of Si, Te, and O at 298K as shown in **Table 4.1**.[25] The Te 3d core level spectra of XPS is presented in **Fig. 4.10 (b)** and **(d)** in which detected peaks are consistent with metallic Te peak. Since oxygen was distributed somewhat uniformly across the Si_XTe_{1-X} film, Te-O binding energy peaks near 576eV and 587eV were expected but they were not found. Therefore, the asymmetric Te peaks are likely due to Si-Te binding energy peak. It was also discovered that with increasing Si conc., the intensity of Si-Te and Te peaks diminished while Si-O peak was enhanced.

From this data, the phenomena behind the low OFF-state resistance can be deduced as segregation between Te in SiO_X amorphous matrix with increasing Si and O contents. This can be realized by Si preferring to bond with O which can be corroborated by increasing Si-O binding energy peak and decreasing Si-Te binding energy peak. As a result, the isolation of Te will be enhanced within SiO_X amorphous matrix as Si conc. increases. The amount of Te conc. is not as important since formation of even one conductive path will allow large amount of current to flow. However, it does not explain how V_T, V_H, and t_d. did not

change much with varying Si conc. This behavior may be understood if the measured portion of the Si_xTe_{1-x} film remained the same in composition while the overall increase in Si conc. is considered to be the background. **Fig. 4.11** illustrates two distinct behaviors that occur in Si_xTe_{1-x} film in order to provide a better understanding of these unusual behaviors.

In the present study, no electroforming was required for threshold switching in $Si_{24}Te_{76}$ OTS device which seems to support VAPs theory. For Si_xTe_{1-x} film above 24 at. % Si, the threshold switching behavior can be understood by a similar conduction mechanism as suggested by Park et al. through Te-SbO OTS device.[26] **Fig. 4.12** shows the conduction mechanism of Te-SbO. It was proposed that the electric field driven amorphous Te atoms drift between nanocrystalline clusters to create a conductive path. Subsequently, as the Te atoms formed between the Te nanocrystalline clusters are amorphous, it can exhibit VAPs based threshold switching.

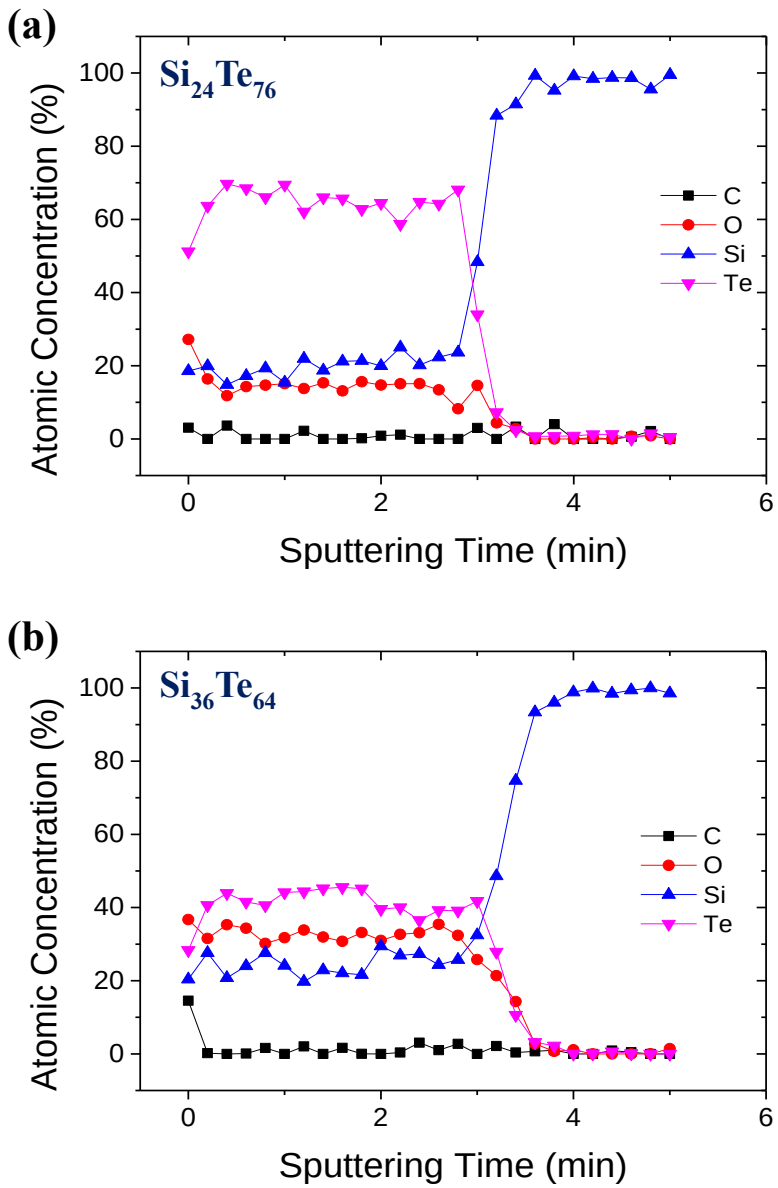


Figure 4.8 AES analysis of 100nm thick (a) $Si_{24}Te_{76}$ and (b) $Si_{36}Te_{64}$ thin films on bare-Si substrates.

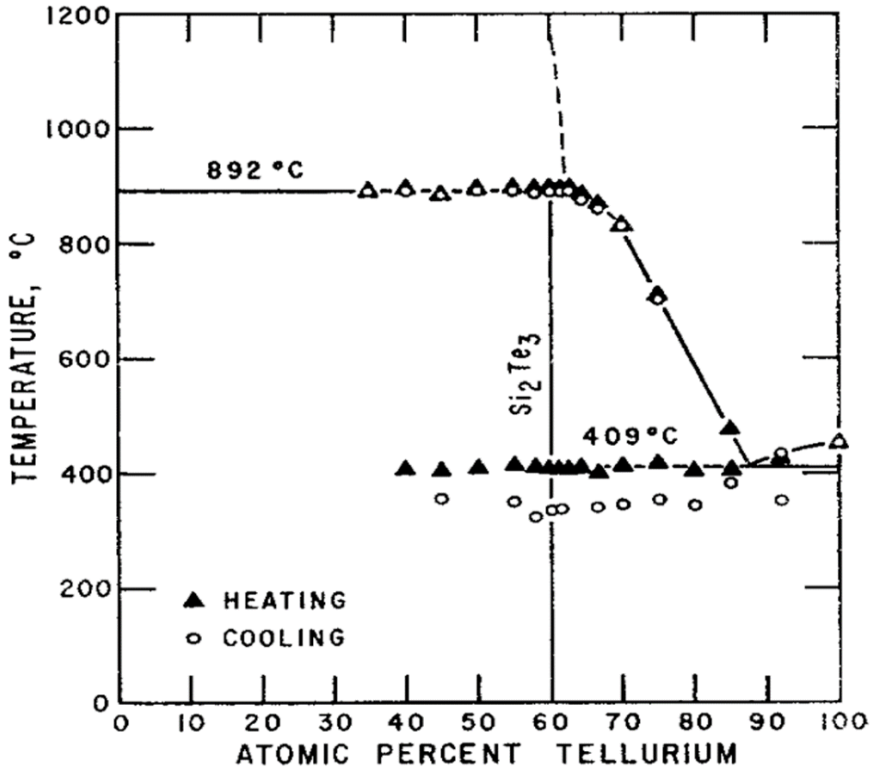


Figure 4.9 Phase diagram of Si-Te binary system.[22]

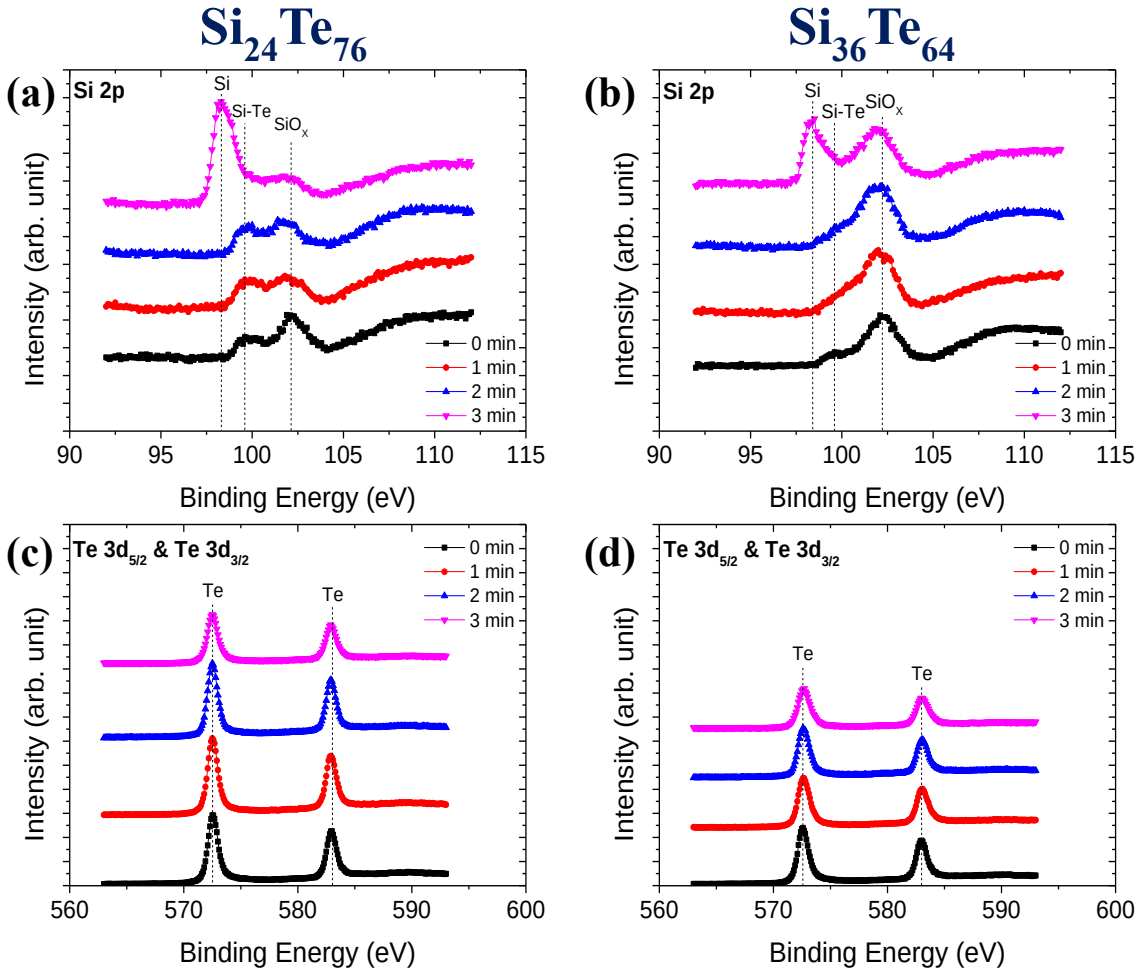


Figure 4.10 XPS depth analysis of Si 2p ((a) & (c)) and Te 3d ((b) & (d)) core-level electronic states of $Si_{24}Te_{76}$ and $Si_{36}Te_{64}$, respectively.

Table 4.1 Bond Dissocation Energies for Si, Te, and O at 298 K.[25]

Bond	ΔHf_{298}, kJ/mol
Si - O	798
Si - Te	506
O - O	498.3
Te - O	391
Si - Si	327
Te - Te	149

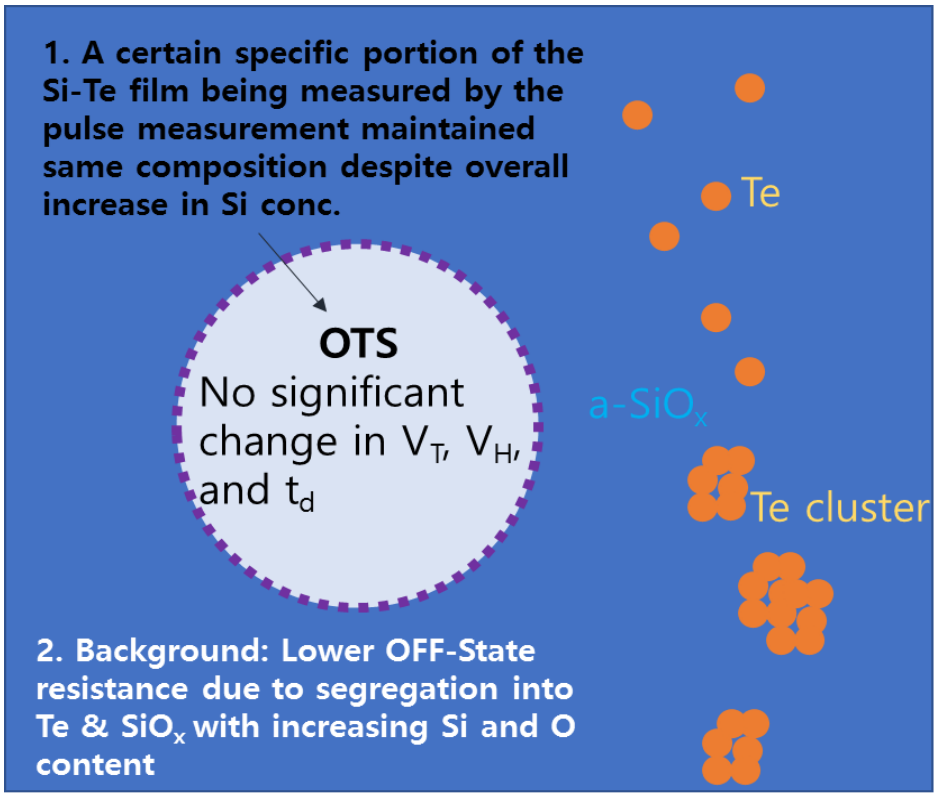


Figure 4.11 A schematic illustration of two different phenomena with increasing Si conc.

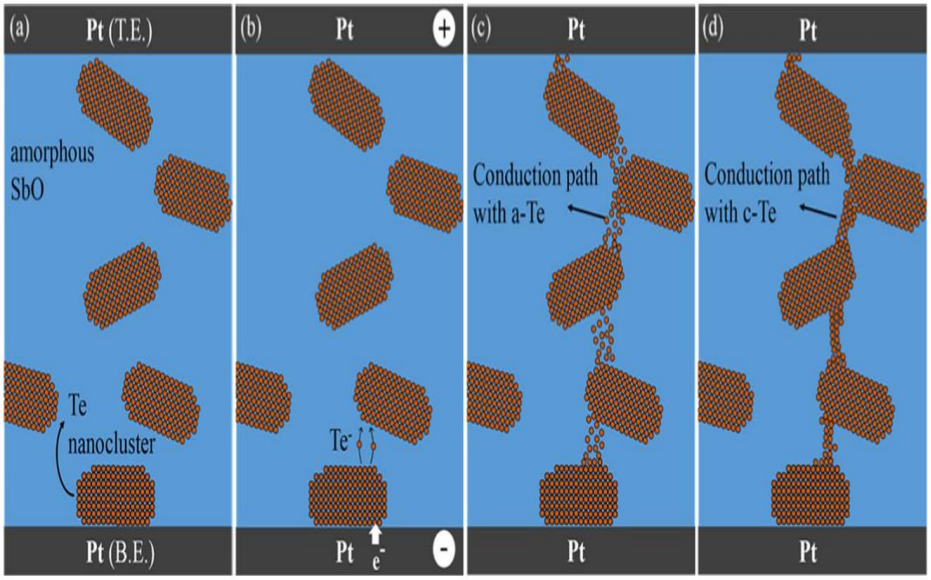


Figure 4.12 A schematic illustration of (a) pristine state, (b) electroforming, (c) threshold switching through conductive path, and (d) annealed after forming state in Te-SbO.[26]

5. Conclusion

The OTS behavior of amorphous Si_xTe_{1-x} ($0.24 \leq x \leq 0.48$) binary system was examined. Threshold switching behavior was demonstrated for all Si_xTe_{1-x} ($0.24 \leq X \leq 0.48$) films with high switching speed less than 45ns and low holding voltage under 0.6V. Due to the favorable formation of hygroscpic Si_2Te_3 above 24 at.% Si, high concentration of oxygen impurities was unavoidable. The introduction of O with increasing Si conc. enhanced the segregation between metallic Te atoms and amorphous SiO_x, allowing creation of condcutive Te filament to lower the OFF-state resistance. Furthermore, the nearly constant V_T, V_H, and t_d despite increasing Si conc. may be attributed to portion of the Si-Te film's composition being unaffected. The electroforming process can be interpreted as migration of amorphous Te ions linking with nanocrystalline Te clusters wherein forms a conductive path under high electric field; the amorphous Te atoms are responsible for trap-limited OTS behavior. Although intnteresting I-V charactersitsics were exhibited by Si-Te system, further study is warranted in which Si-Te system is not exposed to atomsphereic condition.

Reference

1. Hwang, C. S., Prospective of Semiconductor Memory Devices: from Memory System to Materials. *Advanced Electronic Materials* **2015,** *1* (6), 1400056.

2. Burr, G. W., et al., Recent Progress in Phase-ChangeMemory T echnology. *IEEE Journal on Emerging and Selected Topics in Circuits a nd Systems* **2016,** *6* (2), 146-162.

3. Burr, G. W., et al., Access devices for 3D crosspoint memory. *Journal of Vacuum Science & Technology B, Nanotechnology and Micro electronics: Materials, Processing, Measurement, and Phenomena* **2014,** *32* (4), 040802.

4. Ciocchini, N., et al., Bipolar switching in chalcogenide phase c hange memory. *Sci Rep* **2016,** *6*, 29162.

5. Park, S.-G., et al. In *A non-linear ReRAM cell with sub-1μA ul tralow operating current for high density vertical resistive memory (VRR AM)*, Electron Devices Meeting (IEDM), 2012 IEEE International, IEEE: 2012; pp 20.8. 1-20.8. 4.

6. Seok, J. Y., et al., A Review of Three-Dimensional Resistive S witching Cross-Bar Array Memories from the Integration and Materials Property Points of View. *Advanced Functional Materials* **2014,** *24* (34),

5316-5339.

7. Hudgens, S., Progress in understanding the Ovshinsky Effect: T hreshold switching in chalcogenide amorphous semiconductors. *physica s tatus solidi (b)* **2012,** *249* (10), 1951-1955.

8. Kastner, M.; Adler, D.; Fritzsche, H., Valence-alternation model for localized gap states in lone-pair semiconductors. *Physical Review Le tters* **1976,** *37* (22), 1504.

9. Adler, D.; Shur, M.; Silver, M.; Ovshinsky, S., Threshold switc hing in chalcogenide-glass thin films. *Journal of Applied Physics* **1980,** *51* (6), 3289-3309.

10. Redaelli, A.; Pirovano, A.; Benvenuti, A.; Lacaita, A. L., Thres hold switching and phase transition numerical models for phase change memory simulations. *Journal of Applied Physics* **2008,** *103* (11), 111101.

11. Morigaki, K., *Physics of amorphous semiconductors*. World Scie ntific: 1999.

12. Nardone, M.; Simon, M.; Karpov, I. V.; Karpov, V. G., Electric al conduction in chalcogenide glasses of phase change memory. *Journal of Applied Physics* **2012,** *112* (7), 071101.

13. Chivers, T.; Laitinen, R. S., Tellurium: a maverick among the c halcogens. *Chemical Society Reviews* **2015,** *44* (7), 1725-1739.

14. Adler, D.; Henisch, H. K.; Mott, S. N., The mechanism of thre shold switching in amorphous alloys. *Reviews of Modern Physics* **1978,**

50 (2), 209-220.

15. Wuttig, M.; Yamada, N., Phase-change materials for rewriteable data storage. *Nature materials* **2007,** *6* (11), 824-832.

16. Ielmini, D., Threshold switching mechanism by high-field energ y gain in the hopping transport of chalcogenide glasses. *Physical Revie w B* **2008,** *78* (3), 035308.

17. Shufflebotham, P.; Card, H.; Kao, K.; Thanailakis, A., Amorpho us silicon–tellurium alloys. *Journal of applied physics* **1986,** *60* (6), 203 6-2040.

18. Shukla, K. D.; Saxena, N.; Durai, S.; Manivannan, A., Redefini ng the Speed Limit of Phase Change Memory Revealed by Time-resolv ed Steep Threshold-Switching Dynamics of AgInSbTe Devices. *Scientific Reports* **2016,** *6*.

19. Betti Beneventi, G., et al., Analytical model for low-frequency noise in amorphous chalcogenide-based phase-change memory devices. *J ournal of Applied Physics* **2009,** *106* (5), 054506.

20. Wimmer, M.; Salinga, M., The gradual nature of threshold swit ching. *New Journal of Physics* **2014,** *16* (11), 113044.

21. Coward, L., Experimental evidence of filament “forming” in no n-crystalline chalcogenide alloy threshold switches. *Journal of Non-Cryst alline Solids* **1971,** *6* (2), 107-112.

22. Bailey, L., Preparation and properties of silicon telluride. *Journ*

al of Physics and Chemistry of Solids **1966,** *27* (10), 1593-1598.

23. Petersen, K. E.; Birkholz, U.; Adler, D., Properties of Crystallin e and Amorphous Silicon Telluride. *Physical Review B* **1973,** *8* (4), 145 3-1461.

24. Oxley, D., Electroforming, switching and memory effects in oxi de thin films. *Active and Passive Electronic Components* **1977,** *3* (4), 2 17-224.

25. Speight, J. G., *Lange's handbook of chemistry*. McGraw-Hill Ne w York: 2005; Vol. 1.

26. Park, J. W., et al., Threshold Switching in Te–SbO Films for t he Selection Device of Crossbar Resistive Memory Applications. *ECS S olid State Letters* **2015,** *4* (8), N5-N8.

List of publications

1. Refereed Journal Articles (SCI)

1.1 Domestic

1.2. International

1. Sijung Yoo, Taehong Gwon, Taeyong Eom, **Sanggyun Kim**, and Cheol Seong Hwang, “Multicolor Changeable Optical Coating by Adopting Multiple Layers of Ultrathin Phase Change Material Film” *ACS Photonics* **2016,** *3* (7), 1265-1270.

Abstract (in Korean)

고집적 메모리 기술의 발전으로 인해, 선택소자(selector device)는 패시브 크로스바 어레이 구조 내에서 비휘발성 메모리의 중요한 구성 요소가 되었다. 그러나 현재의 선택소자는 아직 장치 구현에 필요한 모든 성능 요구 사항을 충족하지 못했다. ovonic threshold switching (OTS) device 는 칼코제나이드 물질로 구성된 3d-stackable selector 장치로 제안된 유망한 후보 중 하나이다.

본 연구에서는 OTS selector 응용을 위해 Silicon – Tellurium 이성분계 시스템을 조사했다. 삼각 pulse 측정 결과, 비정질 Si_xTe_{1-x} ($0.2 \leq x \leq 0.48$)을 기반으로 하는 OTS 소자는 높은 스위칭 속도 ($\leq$45ns) 그리고 낮은 유지 전압 ($\leq$0.6V)을 나타냈다. OFF 상태의 저항 값은 24 at. % Si 이상에서는 감소하는 것으로 나타났고, 이는 흡습 특성으로 잘 알려진 Si_2Te_3의 형성이 용이하기 때문으로 사료된다. Si-Te 계는 Te 원자와 비정질 SiO_x 로 분리되는데, Si의 농도 증가와 함께 이루어지는 산소의 증가는 Te 전도성 필라멘트의 형성에 기여한다. Si의 농도 변화에 따라 V_T, V_H 및 t_d 의 값은 변화가 없는데, 이는 측정된 부분의 Si_xTe_{1-x} 필름의 조성이 동일하게 유지되었기 때문으로 사료된다. Si-Te 계로부터 나타나는 OTS 거동은 전도성 경로를 만들기 위하여 Te 나노 결정 클러스터 사이로 이동하는 비정질 Te 원자에 기인하는 것으로 추론할 수 있다.

주요어: ovonic threshold switching, chalcogenide, selector device

학번: 2015-22768

김 상 균