Ph.D. DISSERTATION

SiN_x-Based Resistive Memory with Built-in Selectors

자체 선택소자 기능을 가진
질화막 기반의 저항변화메모리

BY

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이 논문을 공학박사 학위논문으로 제출함

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ABSTRACT

The drastic rise of the internet of things (IoT), cloud computing, and big data centers is generating an urgent demand for high-performance/low-power memory. However, conventional charge-based memories, such as flash memory and dynamic random access memory (DRAM), are rapidly approaching their scaling limits. As an alternative, resistive switching in a dielectric film sandwiched between top and bottom electrodes (BEs) has attracted great interest for next-generation non-volatile memory applications, due to its low power consumption, fast switching time, and superb scalability down to the atomic level. Among a variety of resistance materials, silicon-based dielectrics (e.g., Si, SiO_x, and SiN_x) have recently drawn great deal of attention from many researchers, owing to their good compatibility to conventional Si CMOS processes. Especially, SiN_x-based resistive memory shows better switching performance than the SiO_x-based devices, thanks to their abundant defects. In spite of recent advances in resistive memories, some key challenges such as overshoot current and sneak current in crossbar

arrays still need to be overcome.

In introductory part, the advantage of silicon nitride-based RRAM with Si bottom electrode is also described. In addition, the overshoot current and sneak current path issues in cross-point RRAM are discussed and a possible soultion is also presented. In this dissertation, the self-selection SiN_x-based RRAM devices are proposed and their resistive switching characterization and mechanism were discussed. Firstly, the resistive switching characteristics of SiN-based RRAM wi th MIS structure was investigated. The different reset transitions are observed depending on the LRS resistance. The smooth gradual reset switching offers p otential application for a synaptic device in neuromorphic system. Next, the SiN_x-based RRAM with tunnel barrier shows built-in nonlinearity without an additional selector device. The high selectivity in the device with tunnel barrier can be explained by the fact that the electric field depedent nonlinear carrier injection. For another approach, the diode-like resistive switching is achieved by controling dopant concentration in silicon BE. high rectification ratio ($>10^5$)

between forward and reverse currents for unipolar switching mode is demonstrated. Also, the forming polarity and nonlinearity in bipolar switching mode is discussed. The high selectivity and self-rectifying characteristics of SiN_x-based RRAM cell would be one of the most virtuous merits in the high-density crossbar array.

Keywords: RRAM, memory, Silicon nitride, MIS structure, nonlinearity, self-selection.

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CONTENTS

Chapter 1

Introduction

1.1 RRAM technology and its possible applications

The demand for memory has grown explosively with the advent of the Internet of things (IoT). Charge-based NAND flash memory will face limits for applications in non-volatile storage technology because of scaling issues [1]. Several alternative types of memories such as magnetoresistive random-access memory [2], phase-change random-access memory [3], and resistive-switching random-access memory (RRAM) [4] have been researched for next generation nonvolatile memory application. Among these memories based on resistive change, RRAM shows great potential for implementation in future massive storage memory applications because of its outstanding performance such as fast switching operation, low-power consumption, multi-level capability, high endurance, and high scalability in conventional complementary metal–oxide–

semiconductor (CMOS) processing technology [4-23]. Figure 1.1 shows the requirement of RRAM performance to compete with NAND flash. More than 10^7 endurance cycle and less than 100 ns switching speed is required. On/off ratio should be more than 10 times and on-current is about 1 μA at read voltage of ~0.5 V is essential for RRAM commercialization [24].

Figure 1.2 shows the device requirement and demonstrated performance depending on the applications [25]. The RRAM performance is immensely diverse depending on the switching materials. For a storage memory, the density and the nonlinearity should be further improved. Recently, many believe the storage class memory (SCM) is one of the realizable applications [26]. SCM can fill the performance gap between dynamic random-access memory (DRAM) as a main memory and solid-state-drive (SSD) as a storage memory as shown in Fig. 1.3. 3D vertical RRAM structure can be the ultimate solution to further reduce bit-cost and compete with 3D NAND flash according to ITRS roadmap [24]. 3D vertical structure has the advantages over 2D cross-point stack RRAM in the sense that process cost would be significantly cut down by reducing lithography

steps in comparison with 2D cross-point stack RRAM. In 3D vertical RRAM, memory density is directly determined by the total thickness of switching layer, selector device, and top/bottom electrode (TE/BE). However, the deposition of RRAM element as well as thin selector on a vertical sidewall with high accuracy is difficult. Alternatively, X-point using 2 layers of memory cells (Phase change memory) with selector diodes being developed by intel and micron [26].

Classical computing architecture based on the von Neumman model exhibits fundamental limitations, due to the fact that the so-called von Neumman bottleneck cannot process data simultaneously. Brain-inspired computing is believed to be more suitable for real-world environments, such as voice and image recognition, which requires complex and parallel processing, due to its energy-efficient and fault-tolerant computation compared to the von Neumman architecture. The synaptic electronic device is the most important component of a neuromorphic system, as synapses act as connecting bridges between neuron circuits; therefore, the connection strength between neurons can be modulated by synaptic weight.

Among the various synaptic devices, such as phase change [27], ferroelectric [28], and field effect transistor (FET)-based [29] devices that have been proposed, memristor-based synapses have received particular attention, due to their low power consumption, high scalability, and multilevel capability [30–36]. A two-terminal memristor device can mimic biological synaptic functions by modulating the conductance. A great deal of memristor materials, such as NiO_x, HfO_x, TaO_x, AlO_x, MO_x, and InGaZnO, have been reported for synaptic devices until now [30–36].

For neuromorphic application, high number of conductance levels with uniformity and reliability is important. Hence, in this case, the gradual resistance switching is essential.

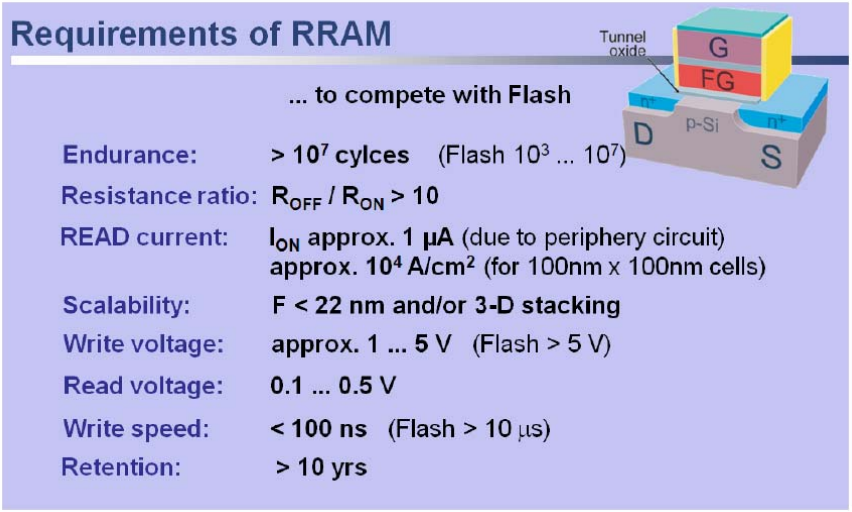


Fig. 1.1 Device performance requirement depending on the applications [24].

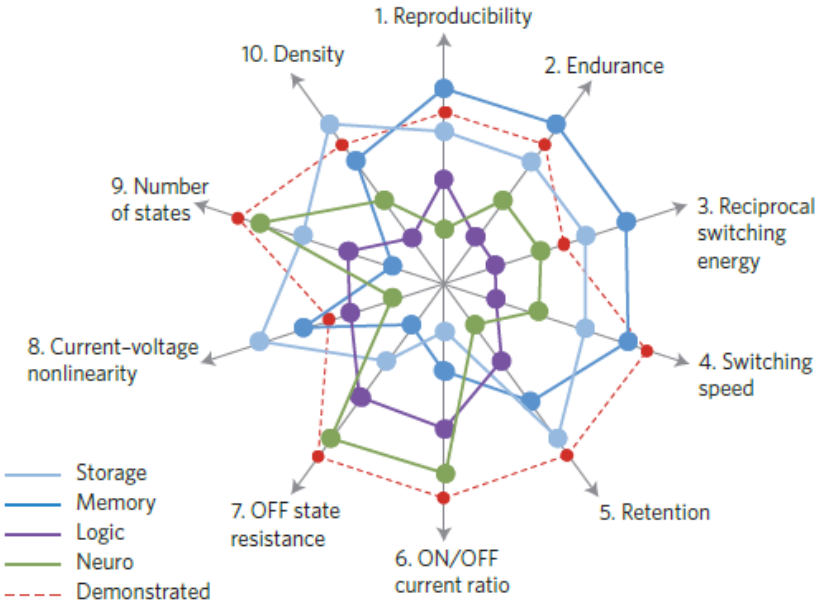


Fig. 1.2 Device performance requirement depending on the applications [25].

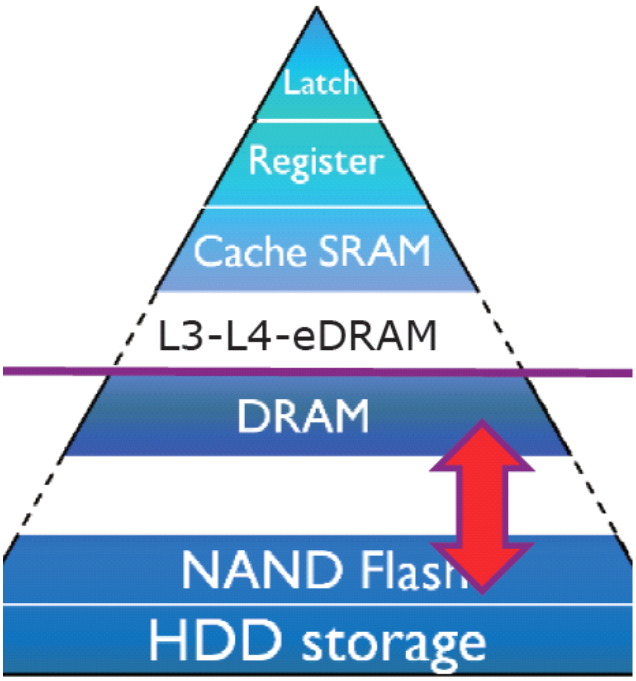


Fig. 1.3 Device performance requirement depending on the applications [26].

1.2 Challenges of RRAM

Several issues such as nonuniformity of resistive switching parameters [37], necessity of electroforming step [38], and high reset current (I_{RESET}) have been an impediment to active commercialization of RRAM technology when using only a single switching layer. Especially, high I_{RESET} has been regarded as an obstacle in realizing high-densith and low-power RRAM array. Current overshoot is a main cause of high I_{RESET}. It is easily confirmed by the fact that the reset current is much higher than the I_{CC} that is applied using external equipment [39, 40]. The I_{CC} independent current overshoot is contributed by parasitic capacitance in a device as well as the testing equipment including a cable and probe station. Integrated 1T-1R can solve the issue, but it is not suitable for high-density memory. Hence, a high reset power consumption, which can be caused by an overshoot current, hinders RRAM commercialization due to its high power consumption. The lack of uniformity in the resistance values is ascribed to the uncontrolled conducting path during the forming, set, and reset processes. The

variation of the LRS can easily be worsened by the uneven current overshoot effect. On the other hand, the HRS can be significantly affected by the size of the conducting path formed during the forming/set processes; it is then difficult to obtain a uniform HRS value under the same reset stop voltage, because a current drop occurs in different ways.

RRAM crossbar array structure having cells with the minimum feature size of $4F^2$ is highly suitable for high-density memory architecture. However, in the crossbar array, sneak current paths through unselected LRS cells can lead to read-out errors when a HRS cell is selected. This issue can considerably reduce the size of crossbar array. Hence, rectifying and nonlinear characteristics are a quite important requirement for two-terminal based emerging memories such as RRAM employing a cross-point array [41-43]. Several architectures have been proposed to solve this issue, such as one diode and one resistive switching element connection (1D-1R), one transistor and one resistive switching element connection (1T-1R) or one selector and one resistive switching element connection (1S-1R) in Fig. 1.4. However, considering the design specifications

and integration availability, a select-less resistive switching element can ease the design and material complexity due to the inherent rectifying and nonlinear properties of the simple unit device.

Selector	J_{ON}	Selectivity	Bidirectional	3D	Other challenges/questions/observations
Vertical Si transistor					Additional process complexity.
Si PN diode					Poly-Si pn diode may be suitable for 3D unipolar NVM.
Si Punchthrough diode					Scalability.
Oxide PN diode					
Oxide/nitride Schottky barriers					Relatively easy to integrate.
Varistor-type Bidirectional Switch (multilayer oxide barrier)					Unknown inter-device yield/variability; voltage margin for higher voltage NVM; Pt electrode processing; write endurance.
Chalcogenide threshold switch					Control of threshold voltage and its variability.
Insulator-metal transition switch					Transition temperature needs to be much higher than chip operating temperature.
Threshold Vacuum Switch					Unknown yield/variability; speed; manufacturability; effect of high-current pulse cycling on off-current.
MIEC selector					Voltage margin for higher voltage NVM.

Fig. 1.4 pros and cons of various selector devices [41].

1.3 SiN-based RRAM with metal-insulator-semiconductor (MIS)

Conventional RRAM devices consist of a metal-insulator-metal (MIM) structure, with insulator resistance switching caused by the diffusion of oxygen vacancies/defects, charge carrier trapping and de-trapping, and Schottky barrier modulation to produce the memory effect. Even though many dielectric materials such as HfO_x [44] and TaO_x, [45] and non-stoichiometric SiO_x [46, 47] and SiN_x [48-55] can be used as resistive switching materials. Among various resistive-switching dielectrics, SiN_x indeed attracts consideration attention due to its compatibility with existent Si-based VLSI platform. In this dissertation, SiN_x-based RRAM devices with MIS structure demonstrating low-power operation and high non-linearity was investigated. Si_3N_4 is a well-known as a trapping layer material in the charge-trap flash (CTF) memory. In addition, it has been used as a resistive switching material for fast switching speed, superb endurance, and retention. The switching mechanism of SiN_x-based may be different from that of oxide-based RRAM utilizing oxygen vacancies and that of conductive

bridge RAM (CBRAM) operated by the arrangement of ions within a solid electrolyte [53]. We believe that the switching mechanism of the intrinsic SiN-based RRAM is basically related to the traps in the SiN film that can be affected by the deposition methods and subsequent switching. The formation and rupture of conducting paths made up of many traps from dangling bonds in the trivalent Si atoms can lead to resistive switching. Much more than initial traps are required for an effective conducting path for the set process and the accelerated electrons with a thermal effect under a high electric field trigger bonding breakage in the SiN film. Then, the electrons injected through the increased trap sites can produce additional traps again. Recently, hydrogen can play an important role in resistive switching, including the reset process [50].

The RRAM device with a silicon bottom electrode (BE) has several advantages over the conventional metal BE. First the structural approaches, such as cone-type BE, can be utilized by using an anisotropic wet-etching process, which can improve resistive-switching performances thanks to the scaling and field-enhancement effects in Fig 1.5 [54]. In addition, the resistive-switching

properties can be tuned by controlling dopant concentration in the surface of Si BE. It is noted that the device with a low dopant concentration on the surface of an Si BE shows low-power switching [55]. Moreover, for embedded memory applications, RRAM cell can directly connected to the source or drain side in a transistor without a metal deposition as BE.

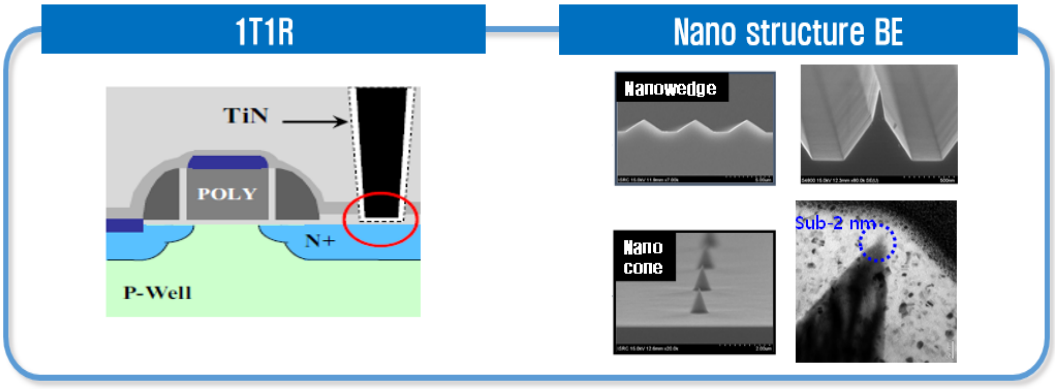


Fig. 1.5 MIS structures for 1T1R and nano structure silicon BEs such as nano-wedge and nano-cone.

Chapter 2

Resistive switching of Ni/SiN_x/highly doped Si devices

2.1 Experimental

The fabricated devices have metal-insulator-semiconductor (MIS) structures. Phosphorus (P) and difluoroboron (BF_2) ions were implanted using a dose of 5 × 10^{15} cm^{-2} at an energy of 40 keV into a single crystalline Si substrate to produce heavily doped n- and p-type Si, respectively, after growth of a 10-nm-thick screen oxide layer. A 4-nm-thick SiN_x layer was deposited by low-pressure chemical vapor deposition (LPCVD) based on the reaction of a mixture of SiH_2Cl_2 (30 sccm) and NH_3 (100 sccm) as the precursor after the annealing process and the removal of the screen oxide. A 100-nm-thick Ni top electrode with a diameter of 100 μm was deposited on the Si_3N_4 layer using a shadow mask. All electrical properties were characterized via the DC voltage sweep mode and the pulse mode using a Keithley 4200-SCS semiconductor parameter

analyzer (SPA) and a 4225-PMU ultra-fast current-voltage (I-V) module at room temperature, respectively. For device operation, the bottom electrodes (BEs) of the n^{++} and p^{++} Si surfaces were grounded and the Ni top electrode bias was controlled.

2.2 Results and Discussion

Figure 2.1(a) and 2.1(b) show the resistive switching I-V curves of the devices with the n- and p-type BEs, respectively. These cells exhibit typical bipolar switching behavior, where the forming and set switching occur under a positive bias and the reset occurs at a negative bias. Both devices were electroformed to switch them from the initial state to the low-resistance state (LRS). The compliance current (I_{CC}) was required to prevent permanent breakdown of the SiN_x layer during the forming process. When a high I_{CC} of 5 mA is applied to the devices, only abrupt reset switching is observed in both devices. In contrast, gradual reset switching can be achieved when using a lower I_{CC}. Figure 2.1(c) to 2.1(e) show the conductance-voltage (G-V) reset curves of the Ni/SiN_x/Si devices for the three reset cases (where (c) is abrupt reset, (d) is multi-step-like gradual reset, and (e) is continuous gradual reset. Interestingly, for the gradual reset process, the device with the p^{++} Si BE shows multi-step-like gradual reset, whereas the device with the n^{++} Si BE shows continuous gradual reset behavior. This difference can be attributed to the different

conducting paths that are caused by current overshoot during the forming and setting processes. To understand these different reset transitions, the explanation based on the resistance in the LRS (R_{LRS}) indicates that the conducting path properties is more effective when compared with that based on the I_{CC}. Figure 2.1(f) shows the distributions of both R_{LRS} and conductance for the three types of reset transition. We believe that the device with the n^{++} Si BE has stronger immunity to current overshoot when compared with the device with the p^{++} Si BE because a higher electric field is initially induced in the SiN_x film of the p^+ Si-type device when the work function difference between the TE and the BE ($\Delta\Phi_{TB}$, where n-type = 0.96 eV, and p-type = −0.14eV) is considered.

Based on the formation and rupture model of the conducting paths that are built from nitride-related traps, we can explain the different reset transitions, as shown in Fig. 2.2(a) to 2.2(c). For abrupt reset switching, the large conducting path (where $R_{LRS} < 1$ kΩ), which is caused by a severe current overshoot, could be ruptured at any time. A singly-linked large conducting path that is composed of nitride-related traps is formed by a hard breakdown. In this process, it is

difficult to use intermediate resistance levels for the multi-level cells because the sharp resistance drop occurs in only one step. For step-like reset switching, multiple conducting paths (10 kΩ < R_{LRS} < 1 MΩ) would be formed and the most vulnerable path with the lowest resistance would initially be ruptured. For continuous reset switching, the effective conducting paths are not initially connected between the TE and the BE, indicating that the resistance level is under the control of the atomic scale configuration. The unit conductance of a single atomic contact $G_0 = 2e^2/h \fallingdotseq 78$ μS, where e is the electron charge and h is Planck's constant [47]. Movement of the aligned conducting defects caused by the electric field would lead to an increase in the number of nonconductive conducting parts. The conductance is continuously reduced until the resistance level reaches the high-resistance state (HRS) in this reset process, indicating that the spatial gap with the nonconductive defects becomes wider.

To validate the proposed conducting path model, which is dependent on the different reset switching behavior types, the conducting path properties are investigated further based on electrical measurements, fitting results, and their

temperature dependence. Figure 2.3(a) shows the activation energies that were extracted from the Arrhenius plot (R_{LRS} as a function of 1/kT) for the three reset switching types. The R_{LRS} that exhibits continuous reset behavior has the highest activation energy, indicating that the conducting path with the higher R_{LRS} shows more semiconducting properties. Figure 2.3(b) shows the nonlinear factor, which can be defined as the ratio of the current at the read voltage V_{READ} to that at half of V_{READ} ($0.5V_{READ}$) in the LRS as a function of V_{READ} for the three reset transitions. Here, V_{READ} is limited before reset switching occurs and a higher V_{READ} is available for continuous reset switching because of the higher reset voltage that is required when compared with that needed for the abrupt and step-like reset transitions. The inset of Fig. 2.3(b) shows the relationship between the nonlinear factor and R_{LRS} at a V_{READ} of −0.2 V for abrupt and step-like reset switching. For the abrupt reset, the nonlinear factor clearly increases with increasing R_{LRS} because the singly-connected conducting path acts as one path, while in the step-like reset case, a broad distribution that is probably due to randomly formed multiple conducting paths is observed. Figure 2.3(c) shows

a log-log plot of the I-V curves in the LRS for the different reset transitions. For abrupt reset switching, the slope of 1 does not change before reset switching occurs, suggesting that the large conducting path in the SiN_x film would lead to insulator barrier modulation between the LRS and the HRS, and the I-V characteristics in the LRS are dominated by ohmic behavior. In contrast, in the gradual switching case, including both the step-like and continuous reset types, the slope gradually increases with increasing voltage, thus causing nonlinear I-V characteristics. These non-ohmic characteristics can be explained using the trap-assisted Fowler-Nordheim (FN) tunneling mechanism [56, 57]. The electrons are initially transported via traps generated in the SiN_x layer, and FN tunneling through the traps becomes dominant with increasing voltage bias when a negative voltage is applied to the TE. Figure 2.3(d) shows the energy band diagram for the Ni/SiN_x/Si system. In the low voltage region, trap-assisted direct tunneling (DT) would be dominant, while in the high voltage region, trap-assisted FN tunneling would be dominant. The I-V curves in the LRS, in the form of a typical trap-assisted DT plot of ln(I) versus 1/V and a FN tunneling

plot of $\ln(I/V^2)$ versus 1/V, are shown in Fig. 2.3(d) [56, 57]. The straight fitting lines indicate that carrier transport in the low voltage region (0.5–1 V) is dominated by trap-assisted direct tunneling. The measured curves also show a straight fitting line with a negative slope in the high voltage regime (>1 V), which indicates that the dominant conduction mechanism in this regime is FN tunneling.

To evaluate the multi-level capabilities of both step-like reset and continuous reset, we first use the DC voltage sweep mode, which can scan a conducting path corresponding to the bias voltage. Figure 2.4(a) and 2.4(b) show the G-V curves for step-like and continuous gradual reset switching, respectively, that were produced by repeated sweeping of identical reset stop voltages. For continuous gradual reset switching, the conducting path responds well to the identical DC voltage sweeping and conductance changes of up to 10 times can be obtained. In contrast, for step-like gradual reset switching, after the effective conductance change, it is difficult to control the conductance under application of the identical DC voltage sweeps. This result indicates that a

higher voltage would be required for annihilation of an additional conducting path after one of the conducting paths is ruptured. Figure 2.4(c) and 2.4(d) show the G-V curves for step-like and continuous gradual reset switching, respectively, produced by sweeping of incremental reset stop voltages. Wider conductance change ranges in the incremental mode are observed for both step-like and continuous gradual reset switching when compared with that produced by identical DC voltage sweeping. The insets show the conductance distribution in each case as a function of the reset stop voltage. In general, when using step-like gradual reset switching, the resistance levels cannot be uniformly controlled using the reset stop voltage because of the conducting paths that are randomly formed during the forming and set processes. In contrast, the multiple resistance states in the continuously smooth gradual reset transition can be obtained more accurately using gap control in only one narrow conducting path.

Next, the pulse responses of the step-like and continuous reset switching types are studied to assess their actual behavior for RRAM implementation. Figure 2.5(a) and 2.5(b) show the conductance changes versus the programming

pulses produced by varying the pulse amplitude from −2 V to −6 V for the step-like reset and continuous reset processes, respectively. For step-like reset switching, a specific threshold pulse amplitude of −2V is required to produce the effective conductance change, and the conductance does not respond to any additional pulses with identical pulse amplitudes. This trend is consistent with the results for the DC voltage sweep mode. The conductance change can be increased further if the absolute pulse amplitude value is increased. In contrast, for the continuous reset process when operating above the threshold voltage, the conductance gradually responds to the pulses with identical amplitudes. Also, when this incremental pulse amplitude is applied to the devices, both step-like and continuous reset transitions are clearly observed, as shown in Fig. 2.5(c) and 2.5(d), respectively.

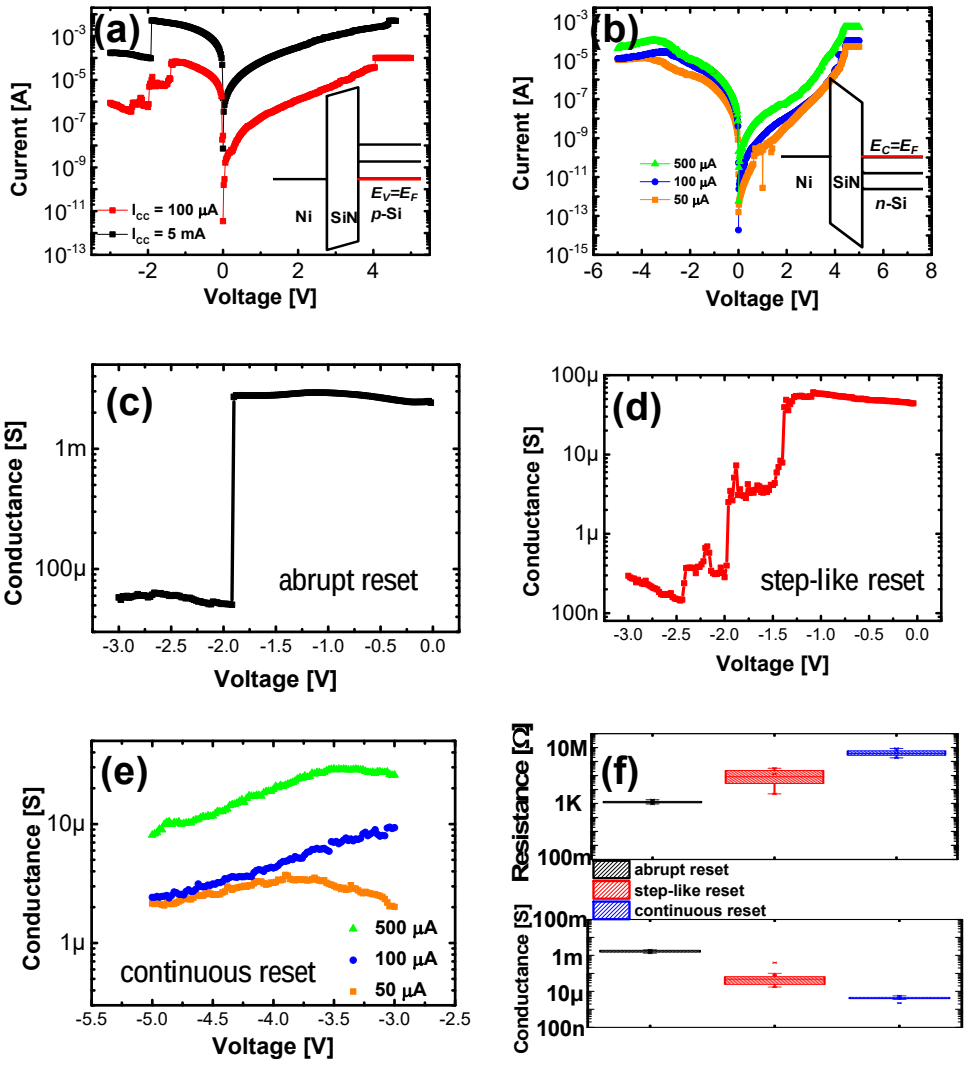


Fig. 2.1 Typical bipolar resistive switching current-voltage (I–V) curves of (a) Ni/SiN_x/p^{++}-Si device and (b) Ni/SiN_x/n^{++}-Si device. Conductance-voltage (G-V) reset curves of (c) abrupt, (d) step-like gradual, and (e) continuous gradual transitions. (f) Statistical distributions of resistance and conductance in LRS for abrupt, step-like gradual, and continuous gradual transitions.

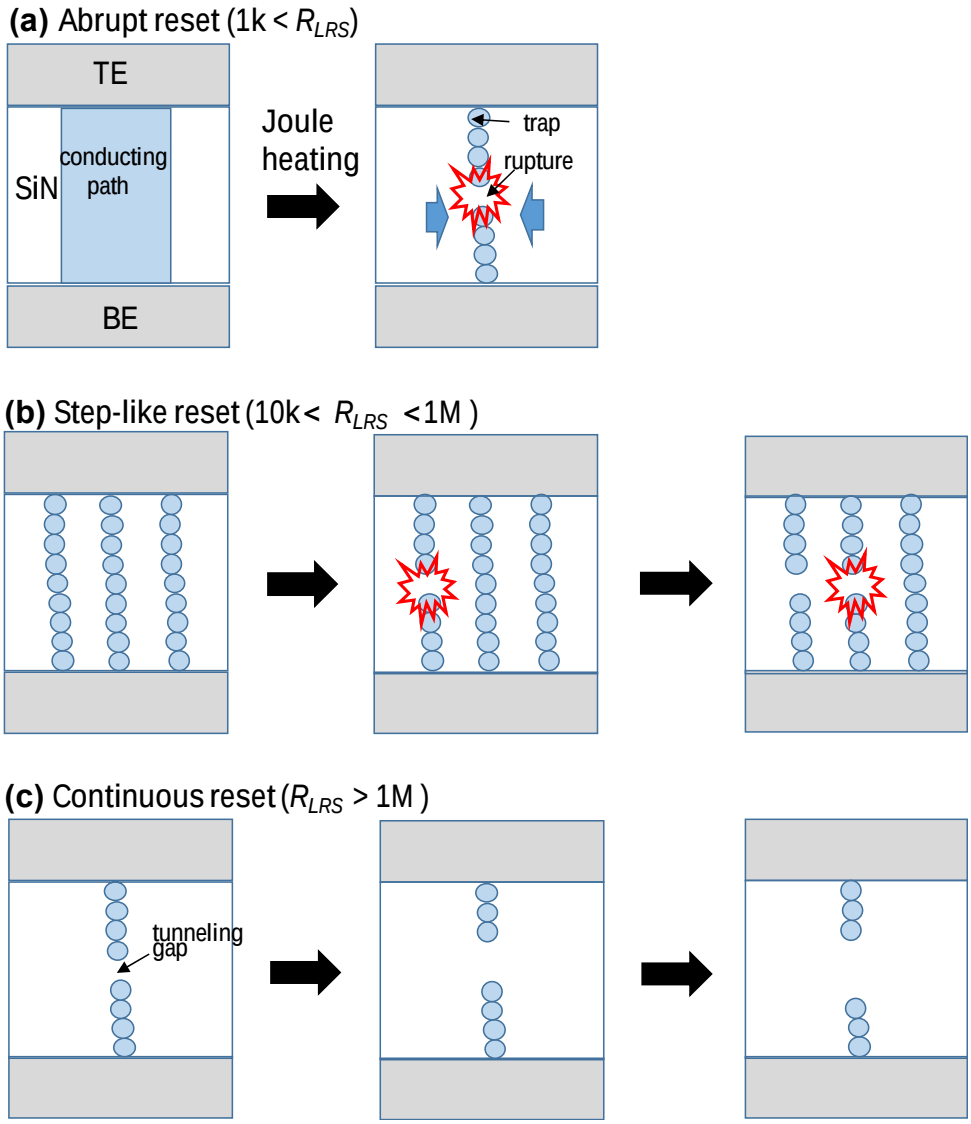


Fig. 2.2 Schematic illustration of reset transitions in Ni/SiN_x/Si device: (a) abrupt, (b) step-like gradual and (c) continuous gradual transitions.

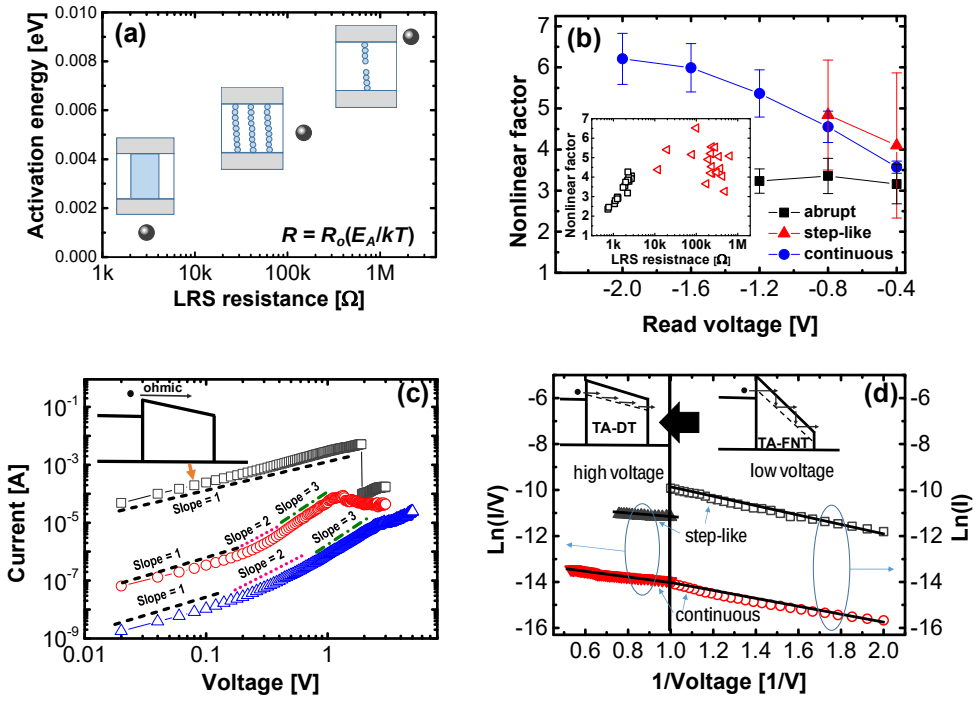


Fig. 2.3 (a) Activation energy (E_A) extracted from Arrhenius plot (R_{LRS} as function of $1/kT$). (b) Nonlinear factor as function of read voltage for the three reset transition types. (c) Log-log plot of *I*-*V* curves in the LRS for the different reset transitions. (d) *I*-*V* curves in the LRS as a typical trap-assisted DT plot of $\ln(I)$ versus $1/V$ and as a FN tunneling plot of $\ln(I/V^2)$ versus $1/V$ for gradual reset transitions.

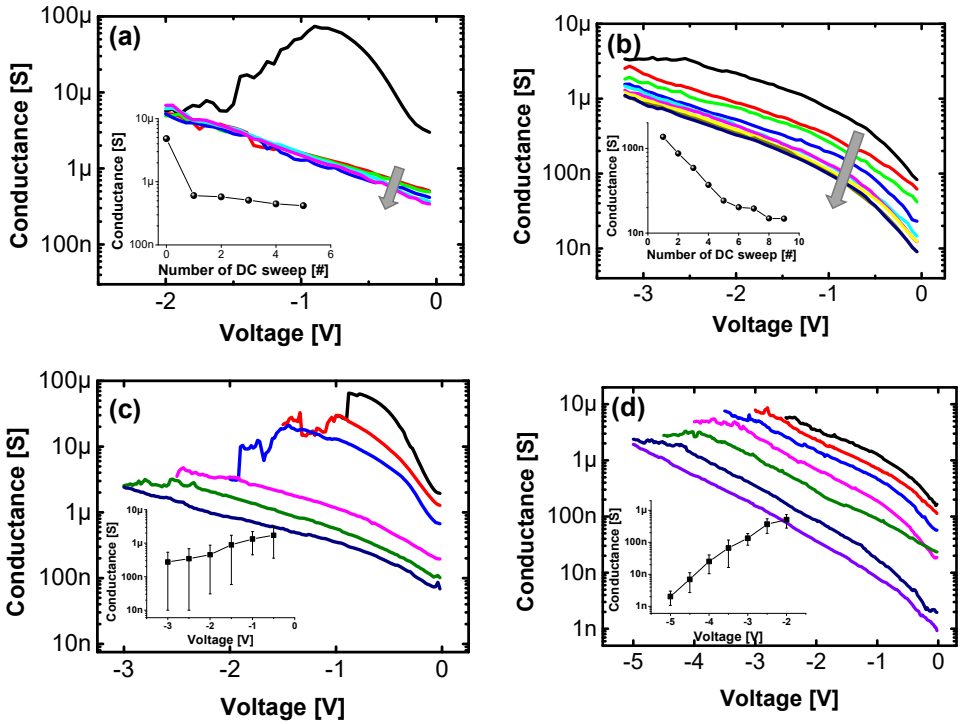


Fig. 2.4 G-V curves for (a) step-like and (b) continuous gradual reset switching produced by repeated sweeping of identical reset stop voltages. G-V curves of (c) step-like and (d) continuous gradual reset switching produced by sweeping of incremental reset stop voltages.

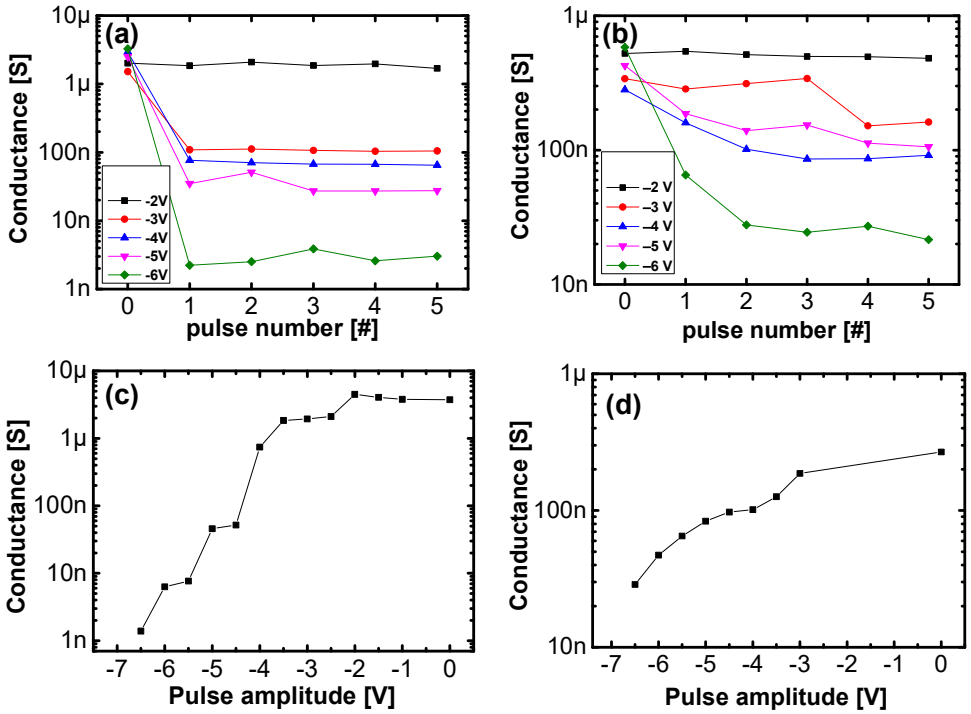


Fig. 2.5 (a) Conductance changes versus programming pulses produced by varying the pulse amplitude from −2 V to −6 V for (a) step-like reset and (b) continuous reset switching. Conductance changes versus programming pulses produced using incremental pulse amplitudes for (c) step-like reset and (d) continuous reset switching.

Chapter 3

Resistive switching of Ni/SiN_x/SiO_2/p^{++}-Si devices

3.1 Experimental

Double-layer RRAM cells with Ni/SiN_x/SiO_2/p^{++}-Si structure were fabricated with a comparison group of single-layer devices with Ni/SiN_x/p^{++}-Si structure as shown in Fig 3.1(a). RRAM cell with Si bottom electrode (BE) in this work have several advantages over the conventional devices with metal-insulator-metal (MIM) structure in the sense that BE can be easily formed without complicating the back-end-of-the-line (BEOL) and higher flexibility in physical design of RRAM devices is available compare with the MIM devices. Fig. 3.2(b) shows the double-layer RRAM cell fabrication process flow. In order to form BE with high conductivity, SiO_2 with a thickness of 60 Å was grown by dry oxidation as the buffer layer. Then, ion implantation of BF_2^+ was carried out at an acceleration

energy of 40 keV and with a dose of 1×10^{15} cm^{-2}. The buffer oxide was removed by diluted HF solution followed by a drive-in process at 1050 °C for 20 min, where lattice damage curing and dopant activation were accompanied. Next, SiO_2 as the tunnel barrier and SiN_x as the switching layer were deposited by medium-temperature oxidation (MTO) at 783 °C and low-pressure chemical vapor deposition (LPCVD) at 785 °C, in sequence.

To analyze the SiN_x material deposited in our laboratory using different methods, X-ray photoelectron spectroscopy (XPS) analysis was performed using a Thermo VG ESCA Sigma Probe spectrometer operating at 15 kV and 100 W with a monochromatic Al-Ka radiation source. The calibration of the binding energy scale was set by fixing the C 1s at 284.5 eV. Figure 3.2(a) and (b) show high-resolution XPS of the Si 2p and N 1s spectra for the SiN_x film, respectively.[47] The atomic concentration was calculated from Si 2p and the N 1s peaks. The N/Si ratio in the SiN_x was 0.87. When compared to the stoichiometric Si_3N_4 sample (x = 1.33), our silicon-rich SiN_x sample ($x < 1.33$) offers favorable resistive switching behavior due to the higher density of traps in the SiN_x film.

The thicknesses of tunnel barrier and switching layer were 2.5 nm and 5 nm, respectively. Two additional RRAM cells with single-layered SiN_x thicknesses of 5 nm and 7.5 nm were fabricated for a comparison study. Finally, Ni top electrode (TE) was deposited by a thermal evaporator, and then, TE was patterned by a shadow mask containing circles with 100-μm diameter. All electrical characterizations were performed by DC voltage sweep mode using Agilent 4156C semiconductor parameter analyzer. For RRAM operations of a cell, BE (p^{++} Si) was grounded and control biases were applied to the TE.

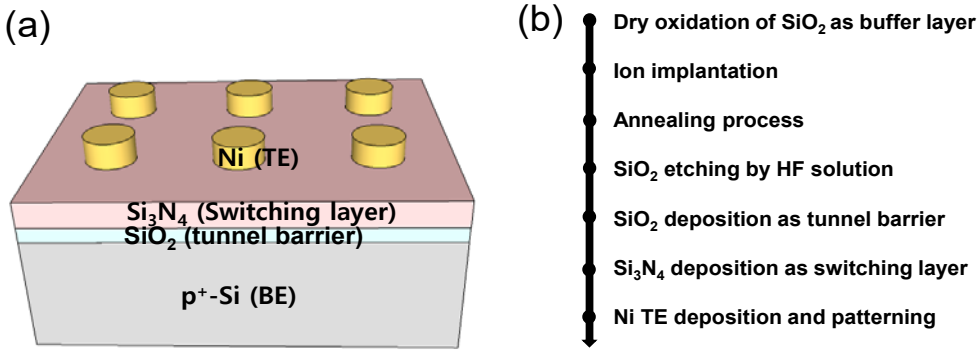


Fig. 3.1 Device configuration. (a) A schematic diagram and (b) Fabrication sequence of Ni/SiN_x/SiO_2/p-Si stacked RRAM cells.

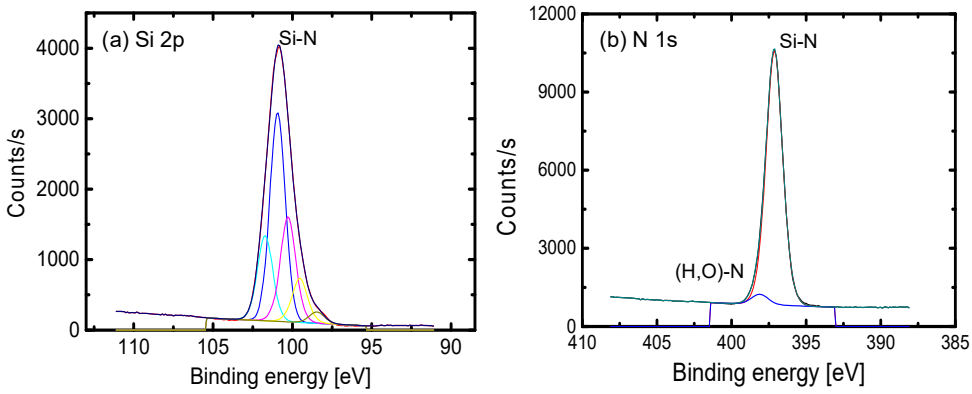


Fig. 3.2 XPS spectra of the SiN_x film deposited via LPCVD: (a) Si 2p and (b) N 1s.

3.2 Results and Discussion

Fig. 3.3 shows I-V curves of 3 devices with a single layer of different SiN_x thicknesses (5 nm and 7.5 nm) and double layers consisting of SiN_x (5 nm)/SiO_2 (2.5 nm). For bipolar resistive switching, the resistance of RRAM cell changes from HRS to LRS while a positive voltage increases from 0 V to the set voltage (V_{SET}) being limited by a compliance current (I_{CC}) which prevents a permanent breakdown of SiN_x film by excessive current. Conducting path may be made up of a lot of traps which originate from dangling bonds in the trivalent Si atoms. Traps much more than initial number of traps are required for an effective conducting path. The accelerated electrons with thermal effect under a high electric field triggers bonding breakages in the SiN_x film. Then, the injected electrons through increased trap site can make additional traps again. Negative voltage is swept down to the reset voltage (V_{RESET}) to change the cell resistance from LRS to HRS by reducing the amount of traps. Due to the thin Si_3N_4 film as the switching layer, both single- and double-layered RRAM cells demonstrate

forming-less process, which means that no difference can be made between the forming voltage ($V_{FORMING}$) and V_{SET}. Fig. 3.4(a) reveals that V_{SET} is mainly determined by the thickness of SiN_x. A higher voltage was needed for single-layered cell with 7.5-nm-thick SiN_x compared with that with 5-nm-thick SiN_x. Although V_{SET} and V_{RESET} are slightly increased in the double-layered RRAM cell, I_{RESET} is drastically decreased to sub-1 μA (I_{CC} = 500 nA). Compared with the single-layer cell, I_{RESET} of double-layer cell decreased more than 3 orders in magnitude. This result is explained by the fact that SiO_2 layer helps to alleviate concentration of excessive electric field in the SiN_x film in the low voltage regime before reaching V_{SET} and the formation of conducting path is effectively controlled by I_{CC}. Fig. 3.4(b) shows I_{RESET} as a function of I_{CC} in the single- and double-layered RRAM cells. I-V curve of the double-layer RRAM cell over the reset process also shows a trajectory similar to that of single-layer device, which indicates that SiO_2 breakdown occurs after the set process in double-layer RRAM cell since an excessively high electric field can be applied to the SiO_2 layer. Therefore, in order to prevent permanent destruction of SiO_2 layer, the control

over I_{COMP} should be highly critical in low-power operation. Fig. 3.4(c) shows the LRS and HRS distributions of single- and double-layer RRAM cells obtained at a read voltage (V_{READ}) of 0.5 V, respectively. It is worth noting that the on/off ratio of double-layer device is maintained as compared to that of single-layer one. On/off ratio is depicted as a function of V_{READ} in Fig. 3.4(d). Here, the on/off ratio was extracted from the ratio between HRS and LRS measured at different read voltages, 0.5 V, 1 V, 1.5 V, 2 V, and 2.5 V. As shown in the figure, on/off ratio is slightly increased at higher V_{READ}. The highest on/off ratio of double-layered cell is over 10^5 in the high voltage region but a relatively large fluctuation is observed. In order to investigate SiO_2 layer as tunnel barrier in the double-layer RRAM cell, selectivity can be defined as the ratio of the current at V_{READ} to that at the half of V_{READ} (1/2 V_{READ}). A single-layered device in LRS demonstrates selectivity of 2–4 with linear I-V characteristics (ohmic behavior near in the low voltage region) as shown in Fig. 3.5(b). The double-layered RRAM cell exhibits improved selectivity as shown in the same figure.

Fig. 3.6 shows that SiO_2 as the tunnel barrier provides non-ohmic

characteristics in the LRS, which permits only a low current by direct tunneling (DT) in the low voltage regime and Fowler-Nordheim tunneling (FNT) more effective in the high voltage regime. The carriers can directly tunnel through the SiO_2 layer as long as it is thin enough, while the carriers would see a triangular barrier modified by a high electric field and have an enhanced tunneling probability even for a thick SiO_2 layer. A serial connection of conducting paths through SiN_x switching layer and SiO_2 tunnel barrier results in nearly Ohmic conduction after a set process, which confirms the dominant conduction mechanism in the LRS of double-layered RRAM cell. Fig. 3.5(c) shows fitted I-V curve showing the relation of $\ln (I/V^2) \sim V^{-1}$. DT regime with negative slope and FNT regime with positive slope are clearly distinguished, meaning that a certain voltage is dominated by FNT rather than DT. Maximum selectivity of 122 has been obtained from the double-layer RRAM cell by the 1/2 bias read scheme (V_{READ} (0.98 V) and 1/2 V_{READ} (0.49 V)) while that of single-layer cell is 2.09 and additional select device is required. This confirms that the excellent non-linearity can be expected by introducing SiO_2 tunneling layer. Further,

higher selectivity would be obtained if 1/3 bias read scheme is employed in the crossbar array architecture based on the proposed double-layer RRAM cells. A large V_{READ} region was secured for double-layer cell owing to high on/off ratio. As V_{READ} is more deviated from V_{SET}, the read disturbance is reduced. Fig. 3.5(d) shows the dependence of selectivity on V_{READ}. Selectivity increases with V_{READ} until V_{READ} reaches 1.5 V and decreases. This result also comes from the role of tunnel barrier. The sharp current transition from DT to FNT occurs at the V_{READ} region between 0.5 V and 1 V. Selectivity is reduced when FNT has predominance and DT is weakened. On/off ratio can be reduced at $V_{READ} < 1$ V. This might put a trade-off since low read voltage should be better to get smaller read disturbance in the ultra-high-density RRAM array. Therefore, for choosing an optimal V_{READ} for operating double-layered RRAM cell, on/off ratio, selectivity, and read disturbance should be collectively considered. In summary, double-layered SiN_x-based RRAM cell with SiO_2 tunnel barrier has been fabricated and its resistive characteristics are closely investigated by a comparison study with single-layered device. Low-current operation is made

possible by controlling I_{COMP} without destructing SiO_2 layer. Also, a large resistance ratio (~10^5) between HRS and LRS has been obtained. The SiO_2 barrier-embedded SiN_x RRAM cell would be highly suitable for the ultra-high-density RRAM array owing to device scalability by its selector-less and superior non-linearity characteristics.

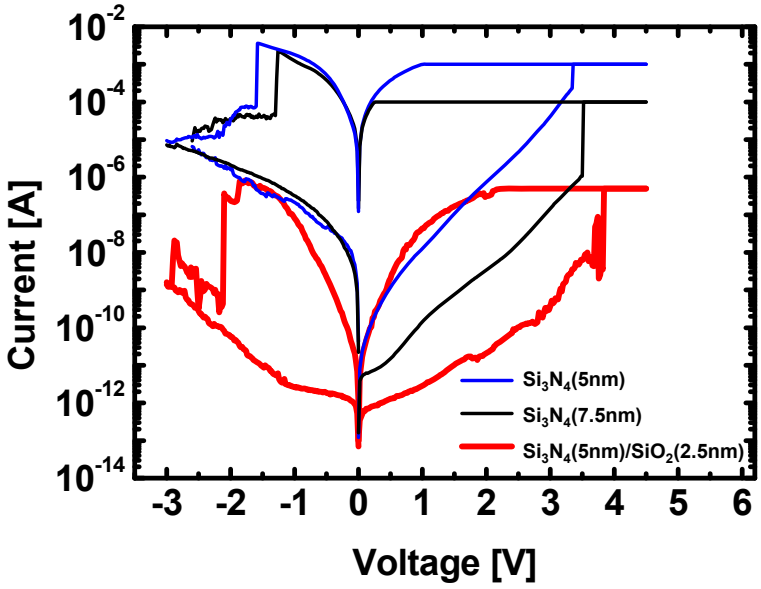


Fig. 3.3 I-V curves of 3 devices with a single layer of different SiN_x thicknesses (5 nm and 7.5 nm) and double layer consisting of SiN_x (5 nm)/SiO_2 (2.5 nm).

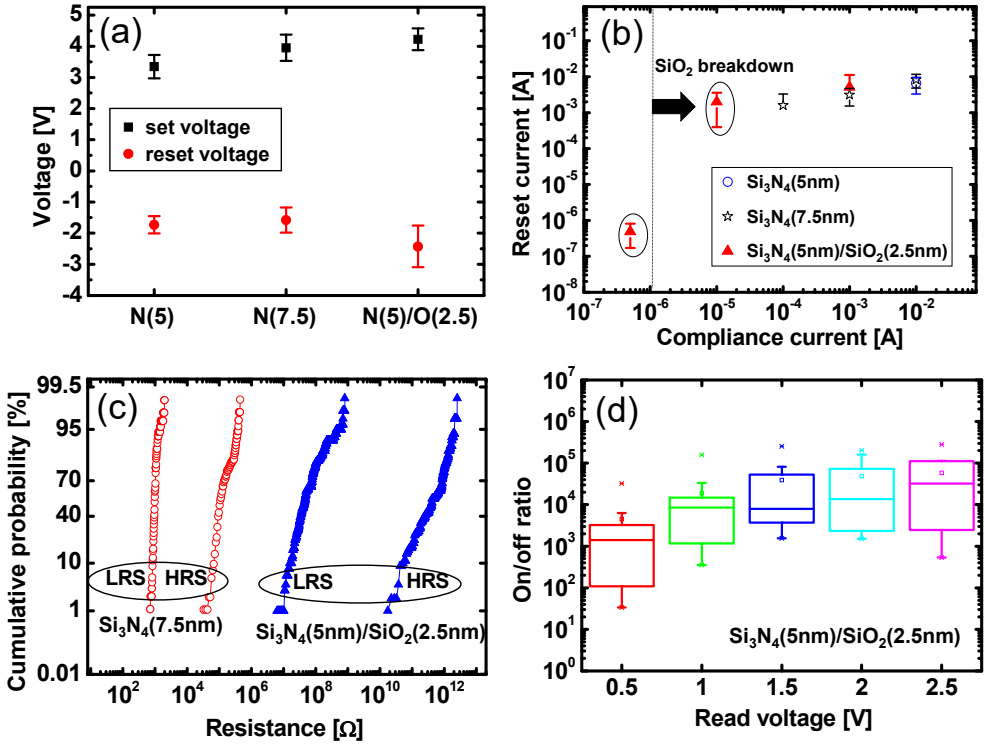


Fig. 3.4 Statistical distribution of the set voltage and reset voltage (a), dependence of the reset current on compliance current (b) in a single-layer cell and double-layer cell. LRS and HRS distribution of single-layer cell (7.5 nm-thick SiN_x) and double-layer cell at read voltage of 0.5 V (c). On/off ratio as function of read voltage for double-layer cell (d).

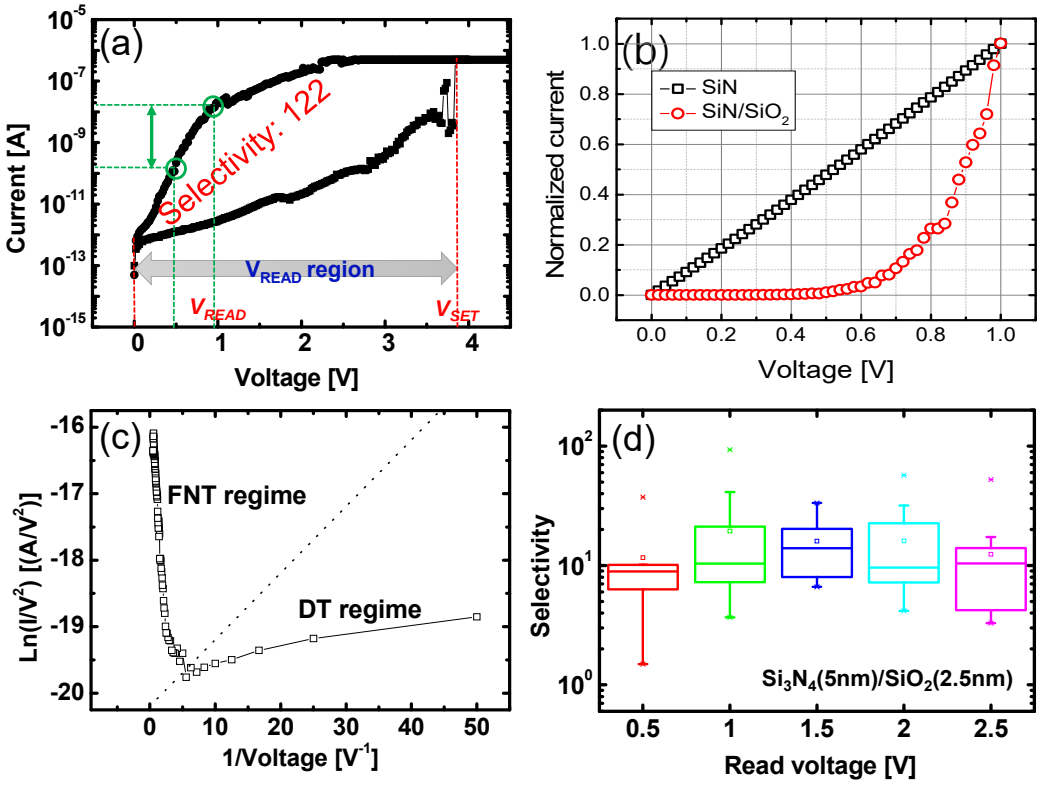


Fig. 3.5 I-V curves (log scale) of double-layer cell (a) and normalized I-V curves (linear scale) showing the selectivity of LRS in single-layer cell with Ohmic conduction, and double-layer cell with non-linearity (b). I-V curves re-plotted in ln (I/V^2) vs 1/V of double-layer cell for tunneling fitting (c). Selectivity as a function of read voltage of double-layer cell (d).

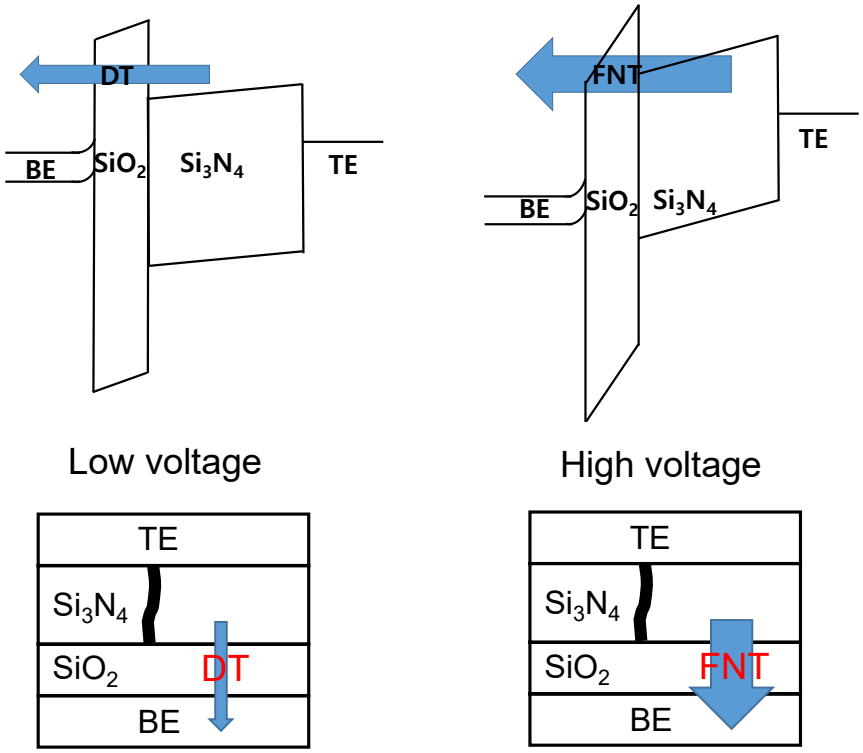


Fig. 3.6 Energy band and schematic diagrams depicting dominant tunneling current transport at low voltage regime and high voltage regime in LRS of double layer cell.

Chapter 4

High rectifying unipolar resistive switching in Ni/SiN_x/p-Si memory devices

4.1 Experimental

Fig. 4.1(a) shows the schematic of fabricated Ni/SiN_x/p-Si RRAM cell. Si BE is constructed in the p-type Si (100) substrate with a resistivity of 5–10 ohm. A 10-nm-thick SiO_2 was thermally grown by dry oxidation after the initial SC1/SC2 etching and HF cleaning processes. Then, BF_2^+ ions with different doses were ion-implanted in the Si at the energy of 40 keV. Doping profiles of the 4 samples were analyzed by secondary ion mass spectrometry (SIMS) as shown in Fig. 4.1(b). Peak concentrations from the samples ion-implanted with dose of 5×10^{12}, 5×10^{13}, 5×10^{14}, and 5×10^{15} cm^{-2} are converted to 10^{17}, 10^{18}, 10^{19}, and 10^{20} cm^{-3}, in sequence. The screen oxide was removed by HF solution and annealing process followed at 1050 °C for 10 min for dopant activation. Subsequently, SiN_x layer was deposited by low-pressure chemical vapor deposition (LPCVD) using

Dichlorosilane (DCS) with a mass flow of 30 sccm and NH_3 (100 sccm) at 785 °C and the deposition thickness of 4 nm was confirmed by a high-resolution transmission electron microscopy (HR-TEM) as shown in Fig. 1(a). Finally, Ni top electrode (TE) with a thickness of 100 nm was deposited by a thermal evaporator and patterned by shadow mask containing circular patterns with 100-μm diameter. All the electrical properties were characterized by the DC voltage sweep mode and the pulse mode using Keithley 4200-SCS semiconductor parameter analyzer (SPA) and 4225-PMU ultra-fast I–V module at room temperature, respectively. p-Si BE was grounded and control biases were applied to the Ni TE over the measurements.

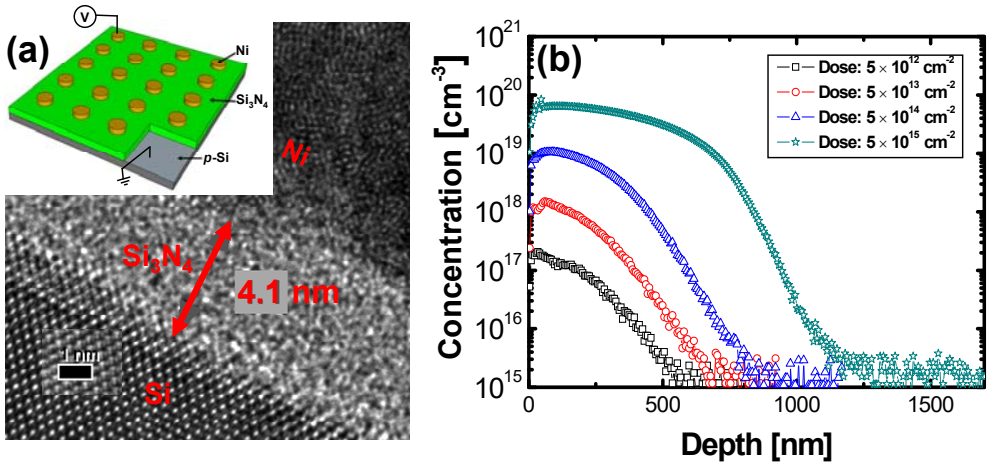


Fig. 4.1 Device configurations. (a) Schematic diagrams and transmission electron microscopy (TEM) image of Ni/SiN_x/p-Si RRAM devices, (b) secondary ion mass spectrometry (SIMS) of Ni/ SiN_x/p-Si RRAM cell with different impurity (BF_2^+) concentration in silicon.

4.2 Results and Discussion

Figs. 4.2(a) through (d) illustrate the typical current–voltage (I–V) characteristics of the 4 devices with the different doping concentrations under the DC sweeping mode. For unipolar resistive switching, the bias is swept keeping the same polarity in the negative region. The electroforming step (the first set process) is required with compliance current (I_{COMP}) to switch the RRAM cell from the initial state to the LRS. The I_{COMP} was set to 100 μA in order to confine the formation of the conducting paths (CP) made of nitride vacancies/defects with prevention of the device under measurement from permanent breakdown. Subsequently, the reset switching from LRS to the HRS is made by backward sweep in the negative voltage region. The rupture of CP is related to de-trapping of carriers, which can be accelerated by the Joule heating during the reset process.

Fig. 4.3(a) shows the distribution of switching voltages for forming/set/reset operations ($V_{FORMING}$, V_{SET}, and V_{RESET}) for those 4 devices with different dopant concentrations. $V_{FORMING}$ is slightly higher than V_{SET} for all the devices due to the

different defect distribution between the initial state and the HRS. Switching voltages, $V_{FORMING}/V_{SET}/V_{RESET}$, become higher when the BE doping concentration decreases. However, higher LRS and lower I_{RESET} can be achieved in the samples with lower dopant concentrations, which is favorable for realizing low-power operation. Higher $V_{FORMING}$ and V_{SET} are required for lightly doped samples, which attributes to reduced carrier concentration and wider depletion layer width in the Si substrate. Also, V_{RESET} increases proportionally to the resistance in the LRS (R_{LRS}), meaning that heat efficiency of CP decreases as R_{LRS} increases, and therefore, higher voltage is needed to disconnect the CP.

To examine the rectifying properties of the fabricated devices in the LRS, the reverse current in the positive voltage region has been read from the devices with different BE doping concentrations. DC sweep was stopped before reaching V_{RESET} in order to avoid reset switching in the positive region since bipolar switching mode of the SiN_x-based RRAM device was made possible. Lightly-doped-BE sample exhibits lower reverse current and higher forward-to-reverse current ratio (F/R ratio) than that with higher doping concentration. Fig. 4.3(c)

shows the F/R ratio at the read voltage (V_{READ}) of 0.5 V as a function of dopant concentration. F/R ratio is nearly 1 under heavy doping concentration (> 10^{19} cm^{-3}). However, the device with BE doping concentration of 10^{17} cm^{-3} exhibits the F/R ratio of higher than 10^4. Furthermore, high F/R ratio (> 10^5) is achieved at V_{READ} of higher than 1 V as demonstrated in Fig 4(d). To discuss the deviations in the self-rectifying characteristics depending on BE doping concentration, energy-band diagrams for the device with lightly and heavily doped BEs in the LRS are illustrated in Figs. 4.4(a) and (b), respectively. In case of the lightly-doped device, the rectification primarily stems from the Schottky barrier between Ni TE and Si BE. SiN_x layer does not serve as a simple insulator anymore when abundant CPs consisting of nitride vacancies are formed. Under the forward bias, holes flow easily from semiconductor to metal because the barrier seen by the holes is lowered. On the other hand, the current is effectively suppressed by the Schottky barrier when reverse bias is applied. Thus, Schottky-diode-like behavior is observed from the devices with lightly-doped BEs. In order to provide empirical evidences for the Schottky current transport mechanism, a Richardson plot [ln

(I/T^2) vs. 1/kT] (here, I: conduction current, T: absolute temperature, and k: Boltzmann constant) is employed to analyze the reverse current in the LRS when the acceptor concentration (N_A) is 10^{17} cm^{-3} as shown in the inset of Fig. 4.4(b). The effective Schottky barrier height (SBH) for holes extracted from the slope of Richardson plot is 0.302 eV. The SBH of metal-semiconductor (MS) or MIS diode is not determined solely by the genuine difference between metal work function and the electron affinity of the semiconductor due to Fermi-level pinning caused by the interfacial states. Also, the reverse current in the voltage region of 0~1 V is checked through Schottky emission equation: ln (I) vs. $V^{1/2}$ plot in Fig. 4.4(b). However, in case of RRAM devices with heavily doped BEs, low-resistance MS contact is attributed to the degenerate Si surface layer. The ohmic contact between metal and semiconductor allows the carriers to readily flow in both directions, and then, the rectifying behavior is no longer observed for heavily doped sample ($N_A > 10^{19}$). Hence, the positive and negative forming/set switching for both unipolar and bipolar operations is realizable. I–V curve in the voltage range of 0~0.8 V from the device with BE doping concentration of 10^{20} cm^{-3} in the LRS can be re-

plotted in the log-log scale, which reveals the ohmic conduction with the slope of 1.

To test reliability of the rectifying devices, endurance and retention characteristics have been measured. The device with $N_A = 10^{17}$ cm^{-3} is proven to be capable of more than 50 DC cycles for unipolar switching in the negative voltage region as shown in Fig. 4.5(a). Also, two resistance states, HRS and LRS, with resistance ratio of 10^5 exhibited no degradation until 10^4 s passed even at the elevated temperature, 100 ºC, as demonstrated in Fig 4.5(b). Next, to confirm the switching time for the set and reset operations, the pulse response of the device having $N_A = 10^{17}$ cm^{-3} were investigated in Figs. 4.5(c) and (d). The pulse amplitudes for the set and reset operations were -10 V and -7 V, respectively.

An increasing tendency in the on/off ratio is observed as both set and reset pulse widths are increased. For operation with lower voltage and faster switching speed, the optimization of Si BE is needed considering the dopant concentration and distribution. We also assess the reliability in the reverse current of the device with $N_A = 10^{17}$ cm^{-3} as shown in Fig. 4.5(e). First, a strong immunity was

confirmed against the pulse disturb (5 V and 500 ns) during the stress time of 10^4 s. Moreover, a thermal stability of reverse current was examined at 100 ºC, where no degradation was observed during the time period of 10^4 s although reverse current was slightly increased.

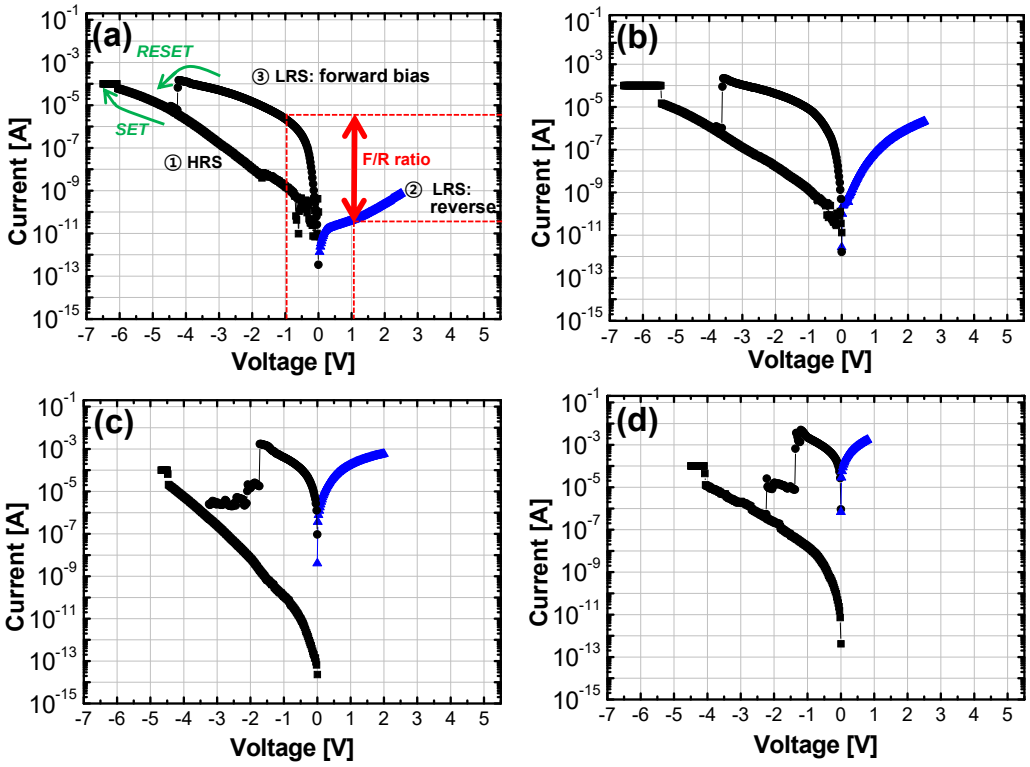


Fig. 4.2 I-V curves of 4 devices with dopant concentration of (a) 10^{17}, (b) 10^{18}, (c) 10^{19}, and (d) 10^{20} cm^{-3}.

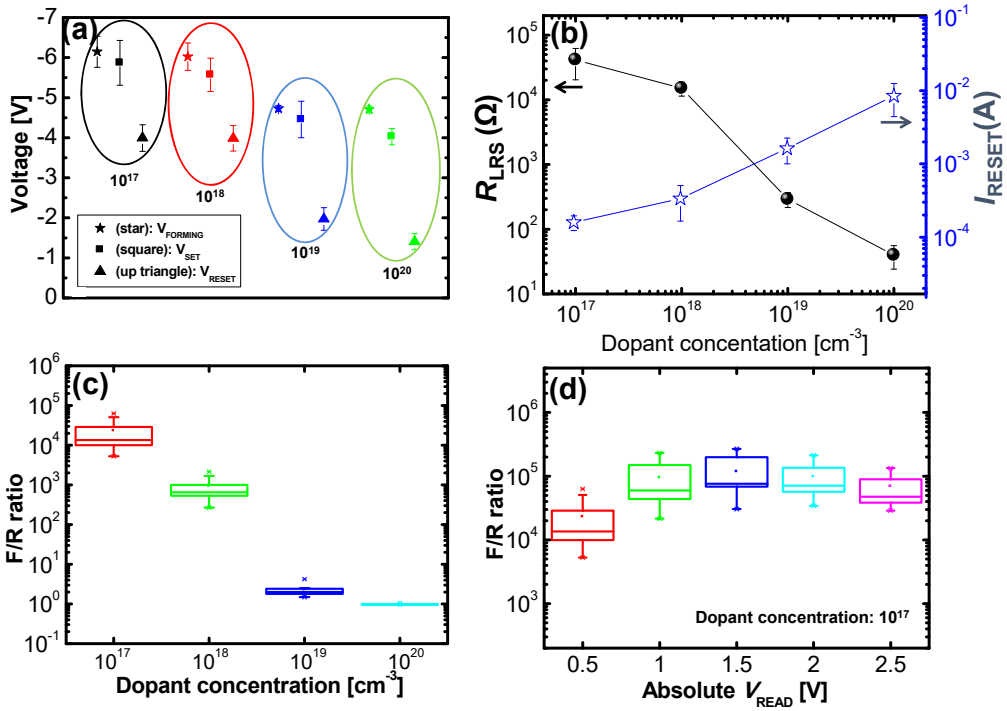


Fig. 4.3 Statistical distribution of (a) switching voltages including $V_{FORMING}$, V_{SET}, and V_{RESET} and (b) R_{LRS} and I_{RESET} for the 4 devices with different dopant concentration. (c) F/R ratio depending on dopant concentrations. (d) F/R ratio as function of read voltage for the device with dopant concentration of 10^{17}.

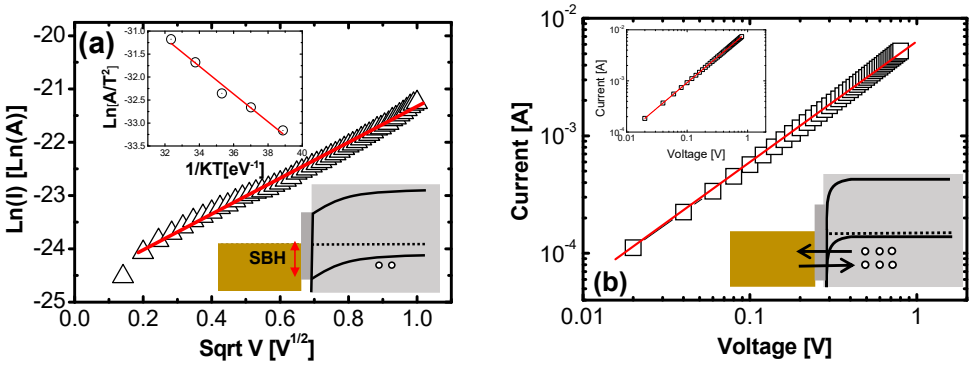


Fig. 4.4 Schottky emission equation: Ln (I) vs. $V^{1/2}$ plot and Richardson plot (inset) of reverse bias in LRS of the device with dopant concentration of 10^{17}. (b) I-V characteristics of in LRS the device with dopant concentration of 10^{20} on a log-log scale (positive region) and inset is fitted in a negative region.

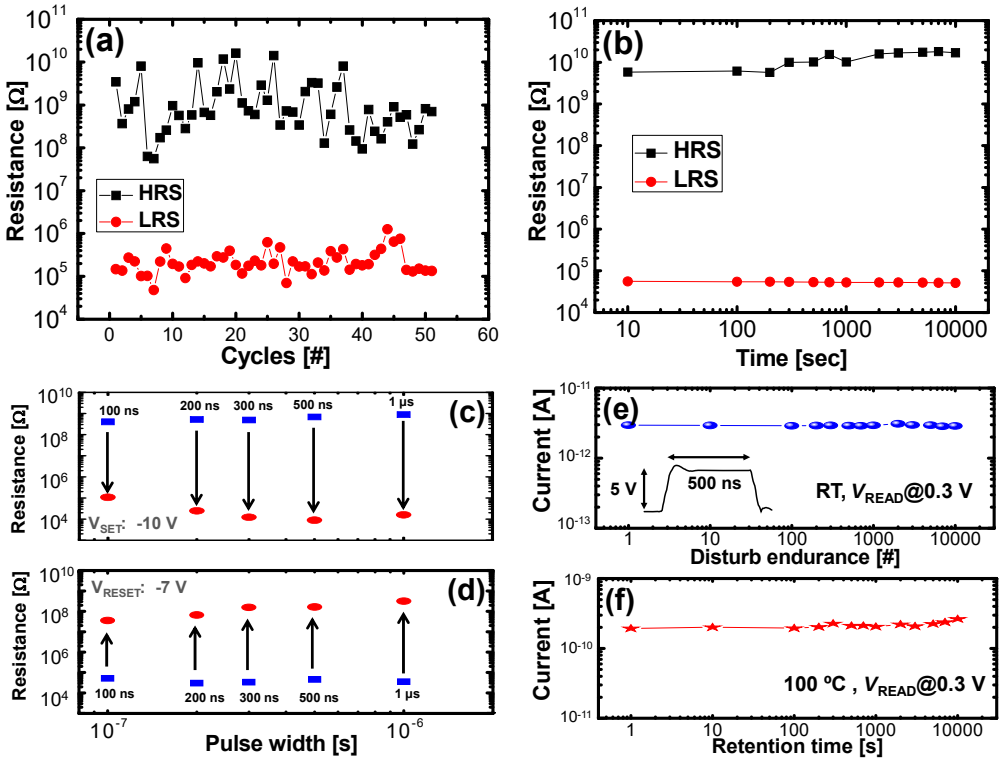


Fig. 4.5 Reliability test for the device with dopant concentration of 10^{17}: (a) Endurance and (b) retention tests in the HRS and LRS. Pulse width dependence of (c) set and (d) reset switching. (e) Pulse disturb endurance and (f) retention time of the reverse current.

Chapter 5

Rectifying and nonlinear bipolar resistive switching in Ni/SiN_x/p-Si memory devices

5.1 Experimental

For the formation of bottom electrode in an MIS system, difluoroboron (BF_2) ions were implanted with energy of 40 keV into a single crystalline Si substrate. The doses of p^+ Si and p^{++} Si bottom electrodes were 5×10^{13} and 5×10^{15} cm^{-2}, respectively. The lattice damage was repaired and dopants were activated by the drive-in process at 1,050 °C for 10 min. A 4 nm thickness SiN_x film, serving as resistive switching layer, was then deposited by a low-pressure chemical vapor deposition (LPCVD) at 785 °C, using a mixture of SiH_2Cl_2 (30 sccm) and NH_3 (100 sccm). Finally, the Ni top electrode was deposited using a thermal evaporator via shadow mask, with a device size of 100 μm. All electrical properties were characterized via the DC voltage sweep mode and the pulse

mode using a Keithley 4200-SCS semiconductor parameter analyzer and a 4225-PMU ultra-fast current-voltage (I-V) module at room temperature, respectively. For device operation, the bottom electrodes of the p^{+} Si and p^{++} Si surfaces were grounded, and the bias voltage was applied on the Ni top electrode.

5.2 Results and Discussion

Figure 5.1(a) shows the typical bipolar I–V curves of the Ni/SiN_x/p^{++} Si device and Ni/SiN_x/p^{+} Si device for electroforming at positive voltage. For unipolar switching, it is difficult to perform uniform and repetitive resistive switching due to the narrow margin between the set voltage and the reset voltage. On the other hand, bipolar switching, in which a different polarity is used for set and reset switching, is more favourable to high performance applications as long as the leakage current elements can be suppressed in a cross-point array. A compliance current (I_{CC}) of 300 μA is applied to the devices to limit the size of conducting path. A higher low-resistance-state (LRS) current is observed for the Ni/SiN_x/p^{++} Si device, compared to the Ni/SiN_x/p^{+} Si device, since the current overshoot can affect the size of the conducting path in SiN_x film.

The subsequent LRS current after the forming and set process is a good barometer of current overshoot. For the reset process, the devices are switched from LRS to high-resistance-state (HRS) when a negative bias is applied to the

devices. An additional current surge is observed for the Ni/SiN_x/p^{++} Si device, before a sharp current drop. The positive bias leads to set switching, in which the devices are switched from HRS to LRS. Here for both devices, the forming-free resistive switching that makes no difference between the forming and set voltage is due to the thin thickness of the SiN_x layer. The formation and rupture conducting path made up of a lot of traps from dangling bonds in the trivalent Si atoms can lead to resistive switching. Much more than the amount of the initial traps are required for an effective conducting path for set process. The accelerated electrons with thermal effect under a high electric field trigger bonding breakages in the SiN film. Then, the injected electrons through increased trap site can make additional traps again. Recently, X. Jiang et.al., reported that hydrogen can play an important role in the resistive switching including reset process [50].

To further identify the current overshoot effect, Figs. 5.2(a)–(d) show that we check the distribution of LRS resistance (R_{LRS}) as a function of the I_{CC} after a positive and a negative forming for the Ni/SiN_x/p^{++} Si device and Ni/SiN_x/p^{+} Si device. After the positive forming, the R_{LRS} value in both devices decreases with

the I_{CC}. Note that low R_{LRS} is randomly observed for the Ni/SiN_x/p^{++} Si device, even though low I_{CC} is imposed to the device for low-power switching, leading to poor controllability of the conducting path. Conversely, the Ni/SiN_x/p^{+} Si device has much higher R_{LRS} with better uniformity. Also, note that Figs. 5.2(a) and (b) show the R_{LRS} at a positive region is higher than that at a negative region. When a negative forming is used for the Ni/SiN_x/p^{++} Si device, more severe current overshoot is observed, leading to very low R_{LRS} with a large conducting path, regardless of the polarity of the read voltage, as shown in Figs. 5.3(c) and (d), indicating that there is very weak rectifying effect.

The insets of Figs. 5.2(b) and (c) show the transient characteristics of a positive forming and negative forming, respectively, for the Ni/SiN_x/p^{+} Si device. A single pulse with a height of 10 and -10 V is applied to the device for a positive forming and negative forming, respectively. The peak current that indicates the overshoot current in a negative forming is higher than that in a positive forming.

Tunneling carriers from metal electrode and the silicon bottom electrode may affect the current overshoot. For a positive forming, the electrons and holes are

injected from silicon electrode and Ni electrode, respectively. For a negative forming, the injections of carriers are in the opposite direction, leading to much higher overshoot, due to the abundant carrier concentrations. Note that, except for reverse current suppressed by the Schottky barrier, which is not appropriate for the rupture of conducting path, the polarity effect induced resistive switching behaviors can potentially be explained by the filament tip contact location in the localized region (close to Ni top electrode or p^+ Si bottom electrode) [58]. Further studies in conducting path growth direction and rupture mechanism during the switching process will be challenging, but important to build a robust device performance prediction in compact model analysis.

Figure 5.3(a) shows the energy band diagrams of the Ni/SiN_x/p^+ Si device under the reverse bias considering the material properties. At low voltage bias region (0.05 – 1 V), the holes from Ni top electrode tunnel into the trap state in SiN_x layer that can be controlled by the I_{CC}, and then the hole injection from SiN_x layer to p^+ Si is strongly affected by the depletion region in p-Si surface. Unlike the Ni/SiN_x/p^{++} Si device, the depletion region from lower dopant concentration in

the silicon surface acting as series resistance helps to alleviate the current overshoot. More importantly, the Schottky barrier that is formed at the surface of silicon bottom electrode is responsible for the asymmetric I-V curves. The forward current and reverse current are driven by a negative bias voltage and a positive bias voltage, respectively. The forward bias voltage lowers the energy barrier in the depletion region, causing the carriers to move fluently. The forward current (I_F) can be expressed as $I_F = I_R\{\exp(eV/nk_BT)-1\}$, where I_R is the reverse current ($I_R = A^*AT^2\exp(-Ø_B/k_BT)$, n is the ideality factor, k_B is the Boltzmann constant, T is the Kelvin temperature, A* is the effective Richardson constant, A is the contact area, and $Ø_B$ is the Schottky barrier height. The Schottky barrier suppresses the reverse current, considering $Ø_B$ is bias voltage-independent [59, 60].

It is also confirmed that all the reverse currents of the Ni/SiN_x/p^+ Si device in the LRS caused by different I_{CC} (0.1, 0.3, 1, and 3 mA) are well fitted with the I-V relationship that is $In(I) \sim V^{1/2}$, as shown in Fig. 5.4(b). Figure 5.3(c) shows a plot of $In(I/T^2)$ versus 1/kT for I_{CC} of 0.3 mA. The slope of Fig. 5.3(c) means the

activation energy (E_a) at bias voltages (0.1 –0.4 V) and then a $Ø_B$ can be extracted from the plot of E_a versus $V^{1/2}$.

The $Ø_B$ is reduced with increasing I_{CC} indicating that the $Ø_B$ can be modulated by the size of conducting path, which is better controllable through I_{CC} for the Ni/SiN_x/p^+ Si device. Figure 5.3(d) shows the log-log plot of reverse current of Ni/SiN_x/p^{++} Si device. Unlike Ni/SiN_x/p^+ Si device, the Ni/SiN_x/p^{++} Si device shows ohmic conduction for the reverse current, suggesting strong and continuous conducting path are formed within SiN_x film. The inset of Fig. 5.4(d) shows the current is slightly increased with temperature, indicating that the conducting path has the semiconducting properties.

To assess the nonlinearity of the LRS current, we define two crucial parameters. The first parameter is the forward-to-reverse current ratio (F/R ratio) that is important for bipolar switching as well as unipolar switching, as shown in Fig. 5.4(a). The forward current can be affected by the thickness of SiN_x film and the size of the conducting path. The reverse current can be mainly determined by the Schottky barrier seen by the holes. Figure 5.4(b) shows the F/R ratio as a

function of the I_{CC} for both devices. The Ni/SiN_x/p^{++} Si device has very low F/R ratio regardless of the I_{CC}, suggesting that the interface resistance and barrier between the SiN_x layer and p^{++} Si are negligible, due to the degenerated Si surface with high dopant concentration. Therefore, the carriers move freely without encumbrance of barrier; and then the size of the conducting path cannot affect the F/R ratio. On the other hand, much higher F/R ratio in the Ni/SiN_x/p^{+} Si device is obtained compared to the Ni/SiN_x/p^{++} Si device. For the I_{CC} of 3 mA, the main cause of reduced F/R ratio would be attributed to a shape increase in the reverse current since the conducting path is too large with loss of Schottky barrier transport, indicating that the size of the conducting path can modulate the Schottky barrier. The second important parameter for nonlinear characteristics is the selection ratio (SR) that can be defined as SR = $I@V_{READ}/I@0.5V_{READ}$, as shown in Fig. 5.4(c). Read voltage that is as low as possible is desirable to minimize read disturbance, and causes less stress in the device cells. Figure 5.4(d) shows the SR at V_{READ} of ±0.5 V as a function of the I_{CC} for both devices. Much higher nonlinear I-V characteristics in the Ni/SiN_x/p^{+} Si device are observed,

compared to the Ni/SiN_x/p^{++} Si device. Figures 5.4(c) and (d) show the SR versus the LRS resistance of the forward and reverse bias, respectively, for both devices. For the Ni/SiN_x/p^{++} Si device, the inherent weak nonlinearity is related to the conducting path with semiconducting behavior. Unlike metal nitride-based RRAM devices showing metallic property of conducting filament in the LRS, the intrinsic SiN_x-based RRAM device shows non-ohmic I-V characteristics when even a large conducting path is formed in SiN_x film. Moreover as the LRS resistance increases, the selection ratio tends to increase, as shown in Figs. 5.4(e) and (f). The experimental results are in accordance with the theoretical backgrounds of conduction transport in the conducting path with quantum-size effects [61].

In particular, the Ni/SiN_x/p^{+} Si device that has a well-controlled conducting path by the I_{CC} shows a clearer relationship between the SR and LRS resistance. The maximum value is higher than 100 for the forward current, when the conducting path with LRS resistance of more than 100 kΩ is formed. The narrow conducting path with high LRS resistance induced by low I_{CC} can boost the SR,

without an additional selection device. Note that the SR in forward current is much higher than that in reverse current. As previously mentioned, the forward current is sensitive to changes in the applied bias voltage. Therefore, for forward current, tunneling transport governed by trap-assisted-tunneling (TAT) and conducting path in SiN_x film plays an important role in the nonlinear characteristics [62, 63]. On the other hand, at low voltage region, the reverse current suppressed by the Schottky barrier height shows weaker nonlinear characteristics.

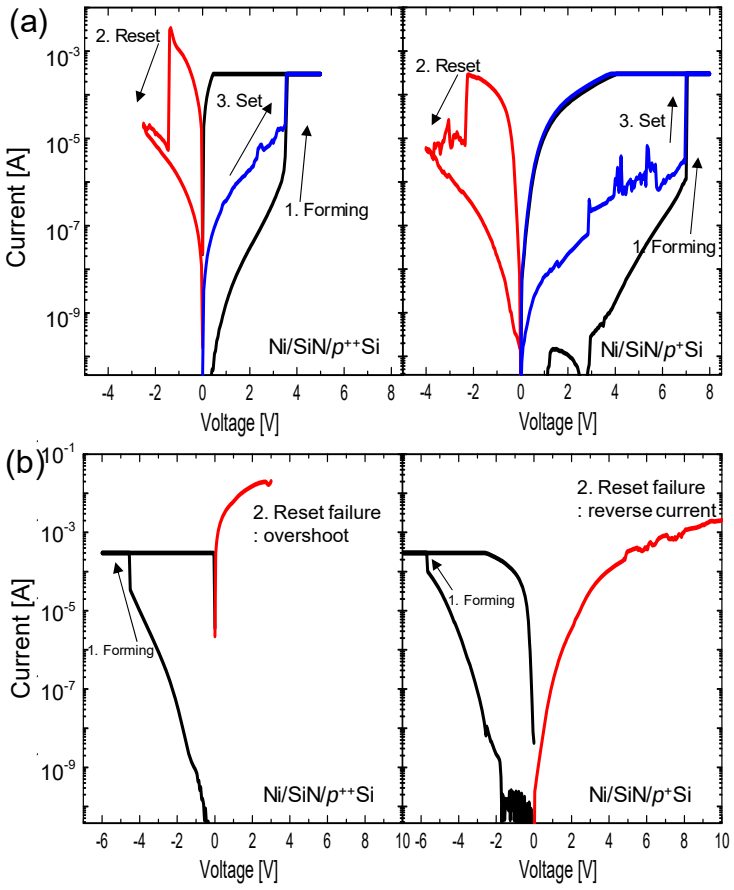
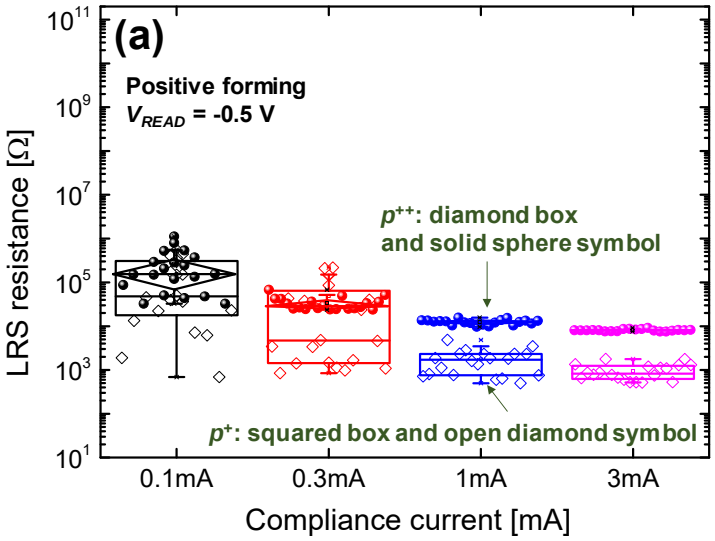
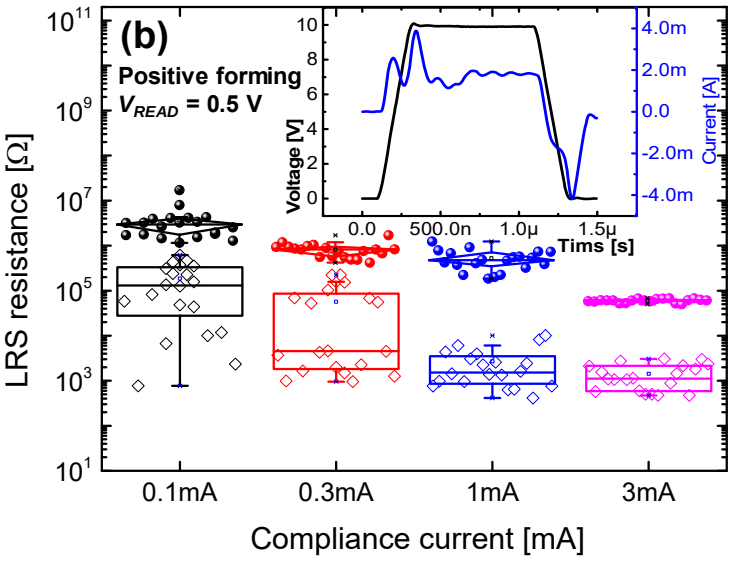
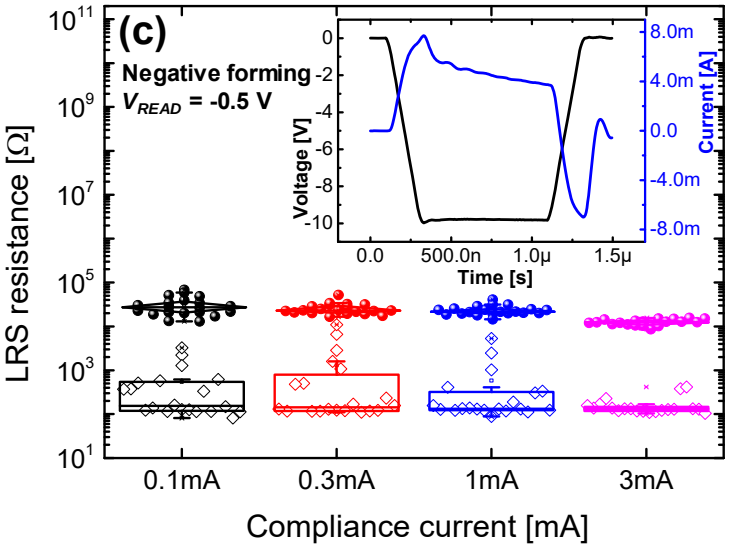


Fig. 5.1 Typical I-V curves of the Ni/SiN$_x$/p^{++} Si device (left), and the Ni/SiN$_x$/p^{+} Si device (right): electroforming at (a) positive voltage, and (b) negative voltage.


(a)
Positive forming
V_{READ} = -0.5 V
p^{++}: diamond box
and solid sphere symbol
p^{+}: squared box and open diamond symbol
LRS resistance [Ω]
Compliance current [mA]
0.1mA
0.3mA
1mA
3mA


(b)
Positive forming
V_{READ} = 0.5 V
Voltage [V]
Current [A]
Tims [s]
LRS resistance [Ω]
Compliance current [mA]
0.1mA
0.3mA
1mA
3mA


(c)
Negative forming
V_{READ} = -0.5 V
LRS resistance [Ω]
10^{11}
10^{9}
10^{7}
10^{5}
10^{3}
10^{1}
0.1mA
0.3mA
1mA
3mA
Compliance current [mA]
Voltage [V]
0
-2
-4
-6
-8
-10
Current [A]
8.0m
4.0m
0.0
-4.0m
-8.0m
0.0
500.0n
1.0µ
1.5µ
Time [s]

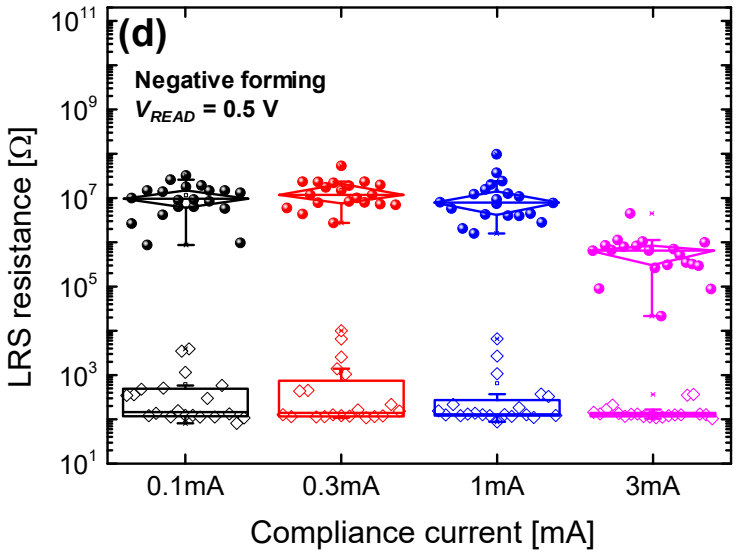
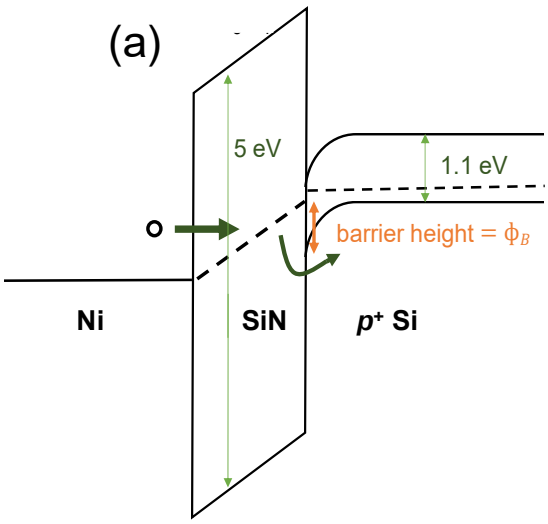

(d)
Negative forming
V_{READ} = 0.5 V
LRS resistance [Ω]
10^{11}
10^{9}
10^{7}
10^{5}
10^{3}
10^{1}
0.1mA
0.3mA
1mA
3mA
Compliance current [mA]

Fig. 5.2 Statistical distribution of LRS resistance for the Ni/SiN_x/p^{++} Si device and Ni/SiN_x/p^{+} Si device: read voltage of -0.5 V (a), and 0.5 V (b) for positive forming; and read voltage of -0.5 V (c), and 0.5 V (d) for negative forming. The insets of Figs. 2 (b) and (c) show the transient characteristics of positive forming and negative forming, respectively, for the Ni/SiN_x/p^{+} Si device.



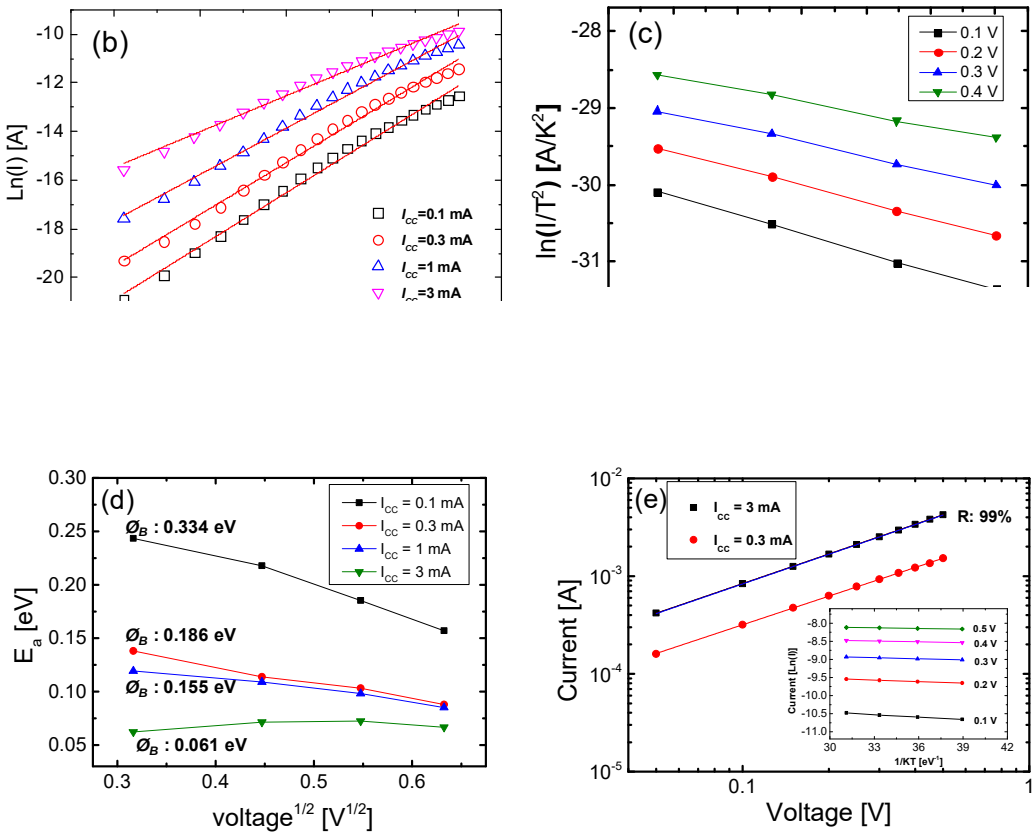


Fig. 5.3 Self-rectification ratio: (a) energy band diagram of the Ni/SiN_x/p^+ Si device under negative bias. (b) ln(I) versus $V^{1/2}$ plots with different compliance current for the Ni/SiN_x/p^+ Si device under negative bias. (c) I-V characteristics at low voltage region for the Ni/SiN_x/p^+ Si device. (d) F/R ratio as a function of compliance current for the Ni/SiN_x/p^+ Si device and the Ni/SiN_x/p^{++} Si device.

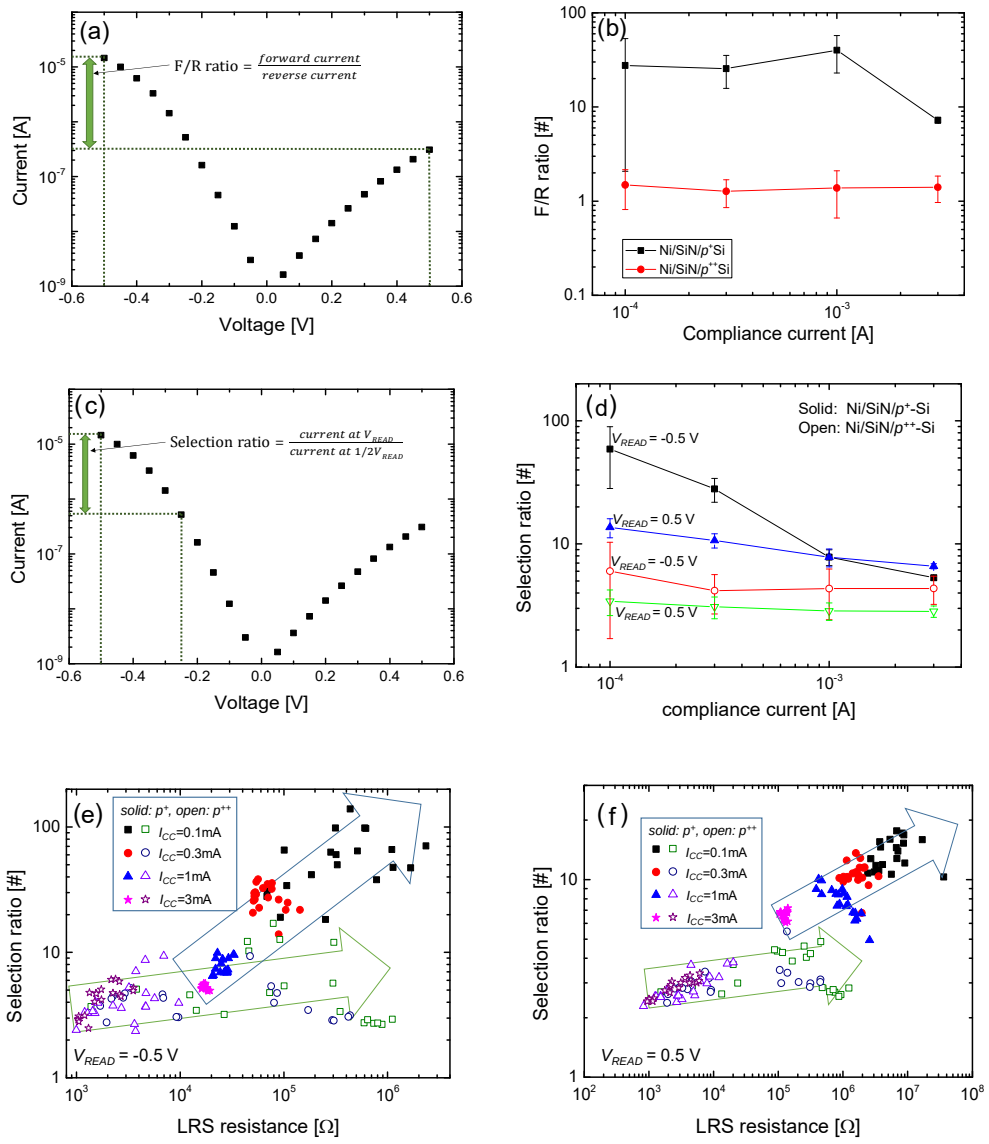


Fig. 5.4 (a) I–V characteristics in the low voltage region in a Ni/SiN$_x$/p$^+$ Si device for F/R ratio. (b) F/R ratio as a function of the compliance current for the Ni/SiN$_x$/p$^+$ Si device and the Ni/SiN$_x$/p^{++} Si device. (c) I–V characteristics in the low voltage region in Ni/SiN$_x$/p$^+$ Si device for selection ratio. (d) Selection ratio as a function of the compliance current. Selection ratio-LRS resistance scatter plots for nonlinearity at a read voltage of -0.5 V (e), and 0.5 V (f).

Chapter 6

Conclusions

In summary, I proposed two self-selection SiN-based RRAM devices. Firstly, double-layered SiN_x-based RRAM device with SiO_2 tunnel barrier has been fabricated and its resistive characteristics are closely investigated by a comparison study with single-layered device. Low-current operation is made possible by controlling I_{CC} without destructing SiO_2 layer. A record resistance ratio between HRS and LRS higher than 105 has been obtained. The SiO_2 barrier-embedded SiN_x RRAM device would be strategic to the ultra-high-density RRAM array owing to device scalability by its selector-less and superior non-linearity characteristics.

In addition, Ni/SiN_x/p-Si structure by controlling the impurity concentration of Si bottom electrode. It is found that we can decrease the reset current drastically by reducing dopant concentration by reducing dopant concentration, which helps

low-power operation in the high density resistive switching memory array. Also, the samples with high impurity concentration exhibited ohmic conduction in the low-resistance state (LRS) while those with low dopant concentration below 10^{18} cm^{-3} showed a remarkable self-rectifying behavior. The nonlinear metal-insulator-semiconductor (MIS) diode characteristics in the samples with low doping concentration (~10^{18} cm^{-3}) are explained by the formation of Schottky barrier at the metal and semiconductor interface. As a result, we demonstrate high rectification ratio (>10^5) between forward and reverse currents along with the robust nonvolatile properties including endurance cycles and retention from the devices with large self-rectification ratio. The high self-rectifying characteristics of SiN_x-based RRAM cell would be one of the most virtuous merits in the high-density crossbar array.

Next behavior when compared to the Ni/SiN_x/p^{++}-Si (~10^{20} cm^{-3}) device. The electroforming process at a positive voltage guarantees better resistive switching performance due to the reduced current overshoot. The rectifying I-V characteristic is attributed to the Schottky barrier in the silicon surface that

suppresses the reverse current. Since the conducting path that can be controlled by the I_{CC} shrinks, the selection ratio generally increases, which shows great potential to produce high-density memory in a cross-point array.

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List of Publications

1. **Sungjun Kim**, Min-Hwi Kim, and Byung-Gook Park, Understanding Reset Transitions in Ni/SiN_x/Si Resistive Random-Access Memory, ***Journal of Nanoscience and Nanotechnology***, Vol. 17, pp. 7231-7235, Oct. 2017
2. Tae-Hyeon Kim, **Sungjun Kim**, Min-Hwi Kim, Seongjae Cho, and Byung-Gook Park, Design and Analysis for 3D Vertical Resistive Random Access Memory Structures with Silicon Bottom Electrodes, ***Journal of Nanoscience and Nanotechnology***, Vol. 17, pp. 7160-7163, Oct. 2017
3. **Sungjun Kim**, Yao-Feng Chang, Min-Hwi Kim, and Byung-Gook Park, Improved resistive switching characteristics in Ni/SiN_x/p^{++}-Si devices by tuning *x*, ***Applied Physics Letters***, Vol. 111, pp. 033509, Jul. 2017.
4. **Sungjun Kim**, Yao-Feng Chang, Min-Hwi Kim, Suhyun Bang, Tae-Hyeon Kim, Ying-Chen Chen, Jong-Ho Lee, and Byung-Gook Park, Ultralow power switching in silicon-rich SiN_y/SiN_x double-layer resistive memory device, ***Physical Chemistry Chemical Physics***, Advance article Jul. 2017, DOI: 10.1039/C7CP03120C
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area dependent gradual resistance switching characteristics of CMOS compatible SiN_x-based resistive memory, ***Solid-State Electronics***, Vol. 132, pp. 109-114, Jun. 2017

6. Min-Woo Kwon, **Sungjun Kim**, Min-Hwi Kim, Jungjin Park, Hyungjin Kim, Sungmin Hwang, and Byung-Gook Park, Integrate-and-Fire (I&F) Neuron Circuit Using Resistive-Switching Random Access Memory (RRAM), ***Journal of Nanoscience and Nanotechnology***, Vol. 17, No. 5, pp. 3038-3041, May. 2017
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초 록

향후 IoT, 클라우드컴퓨팅, 빅데이터의 급격한 수요로 저전력, 고집적 메모리의 수요가 급격하게 증가할 것으로 예상된다. 그러나 현재 상용화 된 전하 기반의 낸드플래시의 경우 스케일링의 한계에 직면할 것이며, 이에 대한 하나의 대안으로 차세대 비휘발성 메모리인 저항변화메모리가 연구되고 있다. 저항변화 메모리는 낮은 전력 소모, 빠른 동작 속도, 우수한 집적도 및 축소화의 가능성을 가지는 장점이 있다. 다양한 저항변화 물질이 개발되고 있지만 실리콘 기반의 실리콘옥사이드, 실리콘나이트라이드는 기존의 CMOS 공정의 우수한 호환성을 가지고 있어서 최근에 주목 받고 있는 저항변화물질이다. 최근에 많은 트랩을 가지고 있는 실리콘나이트라이드는 우수한 메모리 퍼포먼스가 보고 되고 있다. 최근에 저항변화메모리의 연구개발의 많은 발전에도 불과하고 여전히 몇가지 문제점들이 존재한다.

본 논문의 서론에서는 오버슈트커런트와 크로스포인트어레이에서의 기생 커런트의 문제점에 대한 소개를 하였다. 본문에서는 두가지 자체 선택 기능을

가진 실리콘나이트라이드 기반의 저항변화메모리의 공정 과정, 측정 결과에 대한 연구 결과를 보고하였다.

먼저, 터널베리어 삽입을 통하여 추가적인 선택소자의 연결 없이 100 배 이상의 우수한 선택비와 마이크로암페어 이하의 낮은 동작 전류가 관찰되었다. 또한 전계에 의존하는 터널링 메커니즘 분석을 통하여 비선행적인 전류-전압 곡선에 대한 원인을 규명하였다.

두번째로 제안 된 구조에서는 자체 선택기능을 포함하기 위하여 실리콘 하부전극의 도핑 농도를 조절하여 10000 이상의 높은 정류비를 가지는 단극성 저항변화 메모리의 저항변화특성을 분석하였다. 온도 변화 측정을 통하여 금속-부도체-반도체 구조에서 높은 정류비의 원인인 쇼트키 장벽을 규명하였다.

주요어: 저항 변화 메모리, 질화막(실리콘나이트라이드), 실리콘, 자체선택기능, 고집적, 저전력

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