Ph.D. Dissertation

Design of Field-Programmable Mixed-Signal IC with Time-Domain Configurable Analog Block

가변기능형 아날로그 블록 기반의

현장 프로그램이 가능한

혼성 신호 집적회로의 설계

by

Yunju Choi

August, 2017

Department of Electrical Engineering and Computer Science
College of Engineering
Seoul National University

Design of Field-Programmable Mixed-Signal IC with Time-Domain Configurable Analog Block

지도 교수 김 재 하

이 논문을 공학박사 학위논문으로 제출함
2017 년 7 월

서울대학교 대학원
전기·컴퓨터공학부
최 윤 주

최윤주의 박사 학위논문을 인준함
2017 년 7 월

위 원 장 _____ (인)

부위원장 _____ (인)

위 원 _____ (인)

위 원 _____ (인)

위 원 _____ (인)

Design of Field-Programmable Mixed-Signal IC with Time-Domain Configurable Analog Block

by

Yunju Choi

A Dissertation Submitted to the Department of
Electrical Engineering and Computer Science
in Partial Fulfillment of the Requirements for the Degree of
Doctor of Philosophy
at
SEOUL NATIONAL UNIVERSITY

August, 2017

Committee in Charge:

Chairman	Hyuk-Jae Lee
Vice-Chairman	Jaeha Kim
Member	Chulwoo Kim
Member	Yongsam Moon
Member	Jung-Hoon Chun

Abstract

Fast-emerging electronic device applications demand a variety of new mixed-signal ICs to be developed in fast cycle and with low cost. While field-programmable gate arrays (FPGAs) are established solutions for timely and low-cost prototyping of digital systems, their counterpart for mixed-signal circuits is still an active area for research. This thesis presents a design of a field-programmable IC for analog/mixed-signal circuits, which solves many challenges with the previous works by performing analog functions in time domain.

In order to realize the field-programmable analog functionality, time-domain configurable analog block (TCAB) is proposed. A single TCAB can be programmed to various analog circuits, including a time-to-digital converter, digitally-controlled oscillator, digitally-controlled delay cell, digital pulse-width modulator, and phase interpolator. In addition, the TCABs convey and process analog information using the frequency, pulse width, delay, or phase of digital pulses or pulse sequences, rather than using analog voltage or current signals for less susceptibility to attenuation and noise. This analog information expressed in the digital pulses makes it easy to implement scalable programmable interconnects among the TCABs. The architecture of field-programmable IC capable of emulating today's diverse mixed-signal systems is also introduced. In addition to the TCABs, the proposed IC also includes arrays of configurable logic blocks (CLBs) and programmable arithmetic logic units (ALUs) for programmable digital functions. By programming the functionality of the TCAB, CLB, and ALU arrays and configuring the interconnects,

the chip can implement various mixed-signal systems.

A prototype IC fabricated with 65-nm CMOS technology demonstrates the versatile programmability of the proposed TCAB and the IC by being successfully operated as a 1-GHz phase-locked loop with a 12.3-ps_{rms} integrated jitter, as a 50-MS/s analog-to-digital converter with a 32.5-dB SNDR, and as a 1.2-to-0.7V DC–DC converter with 95.5 % efficiency.

Keywords : field-programmable mixed-signal IC, field-programmable analog array, reconfigurable architecture, reconfigurable analog array, mixed-signal IC.

Student Number : 2013-30264

Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Motivations

Today's fast-emerging electronic device applications require a variety of new analog/mixed-signal ICs and the ability to develop them with the least time, cost and effort. However, in general, the whole procedure from system specification to chip-out for application-specific ICs (ASICs) takes lengthy period of time, as shown in Fig. 1.1. Particularly, the procedures of physical design, verification, and fabrication are very time-consuming. The fabrication step not only takes several months but also costs tens of thousands of dollars even if multi-project wafer (MPW) services are available for prototyping purpose. Such design and manufacture processes become more complicated and more expensive with modern deep sub-micron technologies.

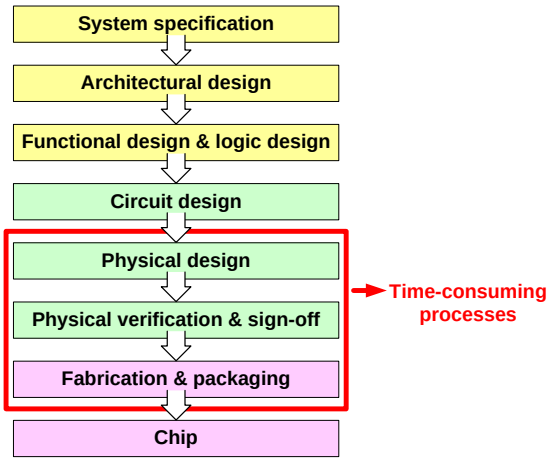


Fig. 1.1 Procedures of IC production.

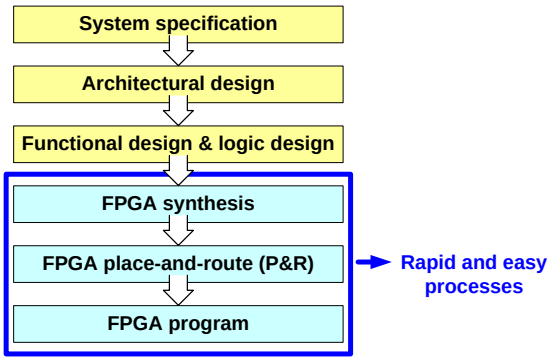


Fig. 1.2 Procedures of prototyping digital systems with FPGAs.

In this circumstance, field-programmable devices can help reduce the cost and time. In case of digital systems, for instance, field-programmable gate arrays (FPGAs) have been well developed and extensively used for those purposes, holding large market since the first commercial FPGA of mid 1980's [1]-[5]. As shown in Fig. 1.2, by synthesizing and programming the designs instead of fabricating them, the time and cost required for prototyping are significantly saved.

On the other hand, the corresponding field-programmable devices for analog/mixed-signal ICs are still under development [6]-[17]. Particularly, a proper design of the configurable analog block (CAB), which is an analog-equivalent to the configurable logic block (CLB) in FPGAs, remains unsettled.

One of the challenges in design of the CAB is to implement various programmable analog functionality. Contrary to the FPGAs including the CLBs whose input-to-output functionalities are reconfigurable by users via field-programming, most previous approaches of field-programmable mixed-signal ICs include fixed function blocks. For example, the works in [6], [7] provide a fixed function block with tunable performance characteristics to program analog filters only. Also, the field programmable ICs in [9], [10] contain several kinds of fixed function blocks and passive components. Then, those ICs are programmed to intended systems by choosing and connecting blocks among the limited blocks. Although there have been field-programmable analog ICs including programmable analog cells for emulation of single transistor behavior [12]-[14], they are too fine-grained to program today's complicated mixed-signal systems consisting of innumerable transistors.

In addition, it is common for the previously reported ICs [6]-[17] to process and propagate analog information with voltage or current amplitude, which limits degree of freedom for interconnection between blocks. Such signal processing with voltage or current form not only faces difficulties in analog circuit design coming along with technology scaling but also has fundamental weak-point in terms of programmable connection between blocks in the field-programmable devices. It is not easy to propagate analog signals through arbitrary direction or arbitrary long path which is

reconfigured each time by users' programming. Therefore, it is required to insert power-hungry analog buffers on the signal path. However, the noise/distortion-sensitive and band-limited nature of the analog buffers eventually limit programmability of signal path and even overall performance.

1.2 Thesis Contribution and Organization

As described in Chapter 1.1, a proper design of the configurable analog block (CAB) both realizing various analog functions and enabling versatile interconnection remains unsettled. This thesis presents a field-programmable mixed-signal IC for the rapid and low-cost prototyping, which solves those challenges with the previous works by performing analog functions in time domain. As an approach to implement the CAB with the various programmable analog functions and ability of versatile interconnection, the time-domain CAB (TCAB) is proposed. It is demonstrated that the proposed TCAB can emulate the functionalities of various mixed-signal circuits used in timing generation, data conversion, and power management ICs. Moreover, since the input and output signals of the proposed TCABs are digital pulses with modulated pulse-width, delay, or frequency, the signals can be easily routed to other TCABs or other part of the IC via digital programmable interconnects. Additionally, this thesis also introduces field-programmable IC architecture to emulate various mixed-signal feedback systems.

This thesis is organized as follows. In Chapter 2, a design of time-domain configurable analog block (TCAB) for the programmable analog functionality is presented. The basic concept and strategy of implementing the TCAB are described. Then, its circuit implementation is presented. In order to show how the input-to-output function of the TCAB can change, diverse examples of the TCABs being programmed to different time-domain analog circuits are presented. An array

composition of multiple TCABs is also described.

In Chapter 3, an IC architecture for the field-programmable mixed-signal IC is introduced. It is explained that how the mixed-signal feedback systems or digitally assisted analog systems can be programmed on the proposed IC.

In Chapter 4, building blocks to implement the proposed field-programmable IC are introduced. In addition to the array of the TCABs for programmable analog functionality, the IC also includes the other two arrays of configurable logic blocks (CLBs) and arithmetic logic units (ALUs) for programmable digital function and interfacing blocks at the boundary of each array of the programmable blocks. Their role and circuit implementation are presented. A method to program the whole chip based on scan chain is also briefly described.

In Chapter 5, measurement results with a prototype IC fabricated in a 65-nm LP CMOS technology are provided. The programmability of the TCAB is first demonstrated by configuring the IC as a digital pulse-width modulator, digitally-controlled oscillator, and gated oscillator and measuring their characteristics. Then, the versatile programmability of the IC is demonstrated by configuring the IC as three representative mixed-signal systems, a PLL, ADC, and DC-to-DC converter, and measuring their characteristics.

Lastly, in Chapter 6, the proposed work is summarized with conclusion.

Chapter 2

Time-Domain Configurable Analog Block

When implementing today's mixed-signal systems including timing generation ICs, data converters, and power management ICs, diverse analog blocks such as a time-to-digital converter (TDC), digitally-controlled oscillator (DCO), digitally-controlled delay cell, digital pulse-width modulator (DPWM), and phase interpolator are required. In common, the listed analog blocks are basically time-domain analog circuits. That is, inputs or outputs of the blocks are binary digital pulses of which time-domain quantity such as pulse-width, frequency, delay or phase encodes analog information. Based on this observation, the key unit block, time-domain analog block (TCAB) that can change its input-to-output functionality to that of the time-domain analog blocks composing the mixed-signal feedback systems like digital PLL, ADC, or DC-DC converter is proposed [18].

That is, as an analogous to the configurable logic blocks (CLBs) used in digital

FPGAs, this work presents the field-programmable analog block of which input-to-output function can be changed via programming. It is contrast to the prior works on field-programmable analog arrays (FPAAs) where the unit blocks have fixed input-to-output functions and only the interconnect blocks among them are programmable. For example, the work in [6] uses an array of transconductance (G_m) cells of which only the parametric characteristics such as gain and bandwidth are programmable. Also, the field programmable ICs in [9], [10] contain more diverse active circuits (e.g., OTAs, current mirrors, and Gilbert multiplier) and passive components, but each block has fixed and unchangeable functionality.

Further, most previously reported ICs [6]-[17] suffer from the loss in signal quality while the signals propagate through the programmable interconnects in voltage or current forms. For instance, the analog voltages propagating via long interconnects and switches are susceptible to attenuation due to the resistance and capacitance of the circuit networks. Also, their signal-to-noise ratio (SNR) can be easily degraded due to noise and interference coupled to the network. Whereas inserting analog buffers (e.g., unity-gain amplifiers) can mitigate these issues to some degrees, analog buffers are typically power-hungry.

In order to achieve both programmable input-to-output functionality of unit analog blocks and solves the scalability of programmable interconnects among them, this work establishes a strategy of conveying and processing analog information in time domain. For instance, the proposed TCABs can be programmed to various time-domain analog circuits including TDC, DCO, DPWM, digitally-controlled delay cell, or phase interpolator. The TCABs receive and produce analog information in the form of digital pulses of which frequency, delay, phase or pulse-

width changes with the signal to be conveyed. Hence, the analog information expressed in digital pulses can reliably propagate through more scalable digital programmable interconnects (e.g., with tri-state buffers and digital buffers) with less susceptibility to attenuation and noise.

The rest of this chapter is organized as follows. The detailed description on features of the TCAB is presented in comparison with the prior works. Then, following subchapters cover the circuit implementation of the TCABs, and explain how their input-to-output functions can be changed via field-programming by listing configuration examples. Lastly, the TCAB array composition including the implementation of programmable interconnects is also described.

2.1 Overview of the TCAB

2.1.1. Reconfigurable functionality

One of the most noteworthy difference of this work compared to the previously-reported works is that programmable analog function is achieved solely by the TCAB. As illustrated in Fig. 2.1, a single TCAB can be programmed to time-domain analog blocks such as DCO, DPWM, gated oscillator, digitally-controlled delay cell or phase interpolator. It is in contrast to the works in [6], [7], [9], [10] that include limited kinds of analog blocks, each of which input-to-output function is fixed and unchangeable. When programming intended mixed-signal systems on those ICs, the only thing allowed to users is to choose the connections among the limitedly

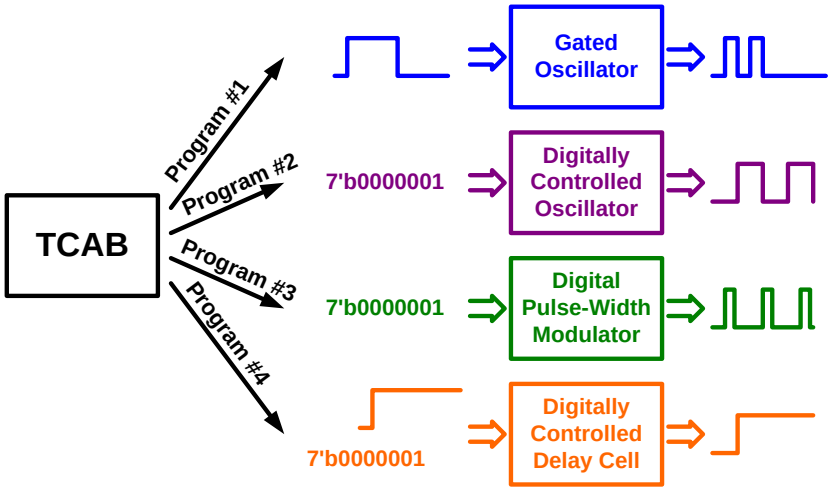
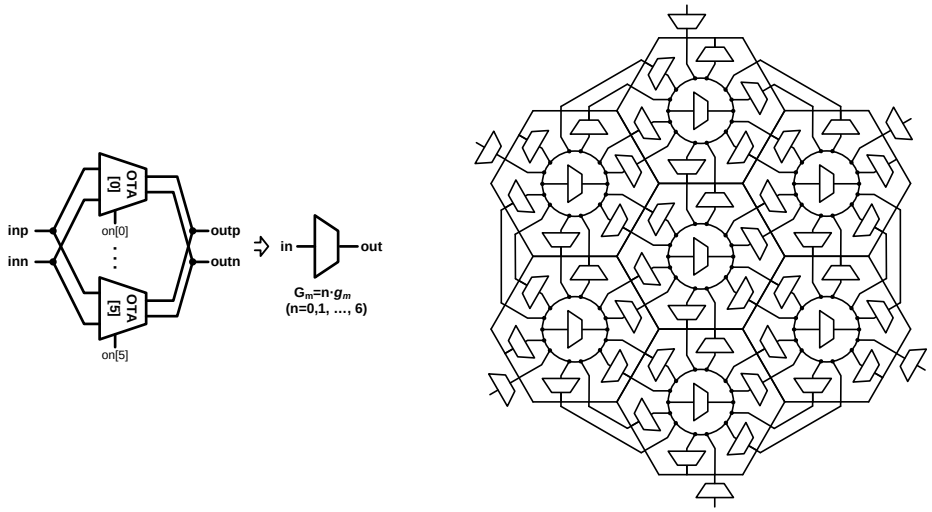


Fig. 2.1 TCAB that can change its functionality via field-programming.

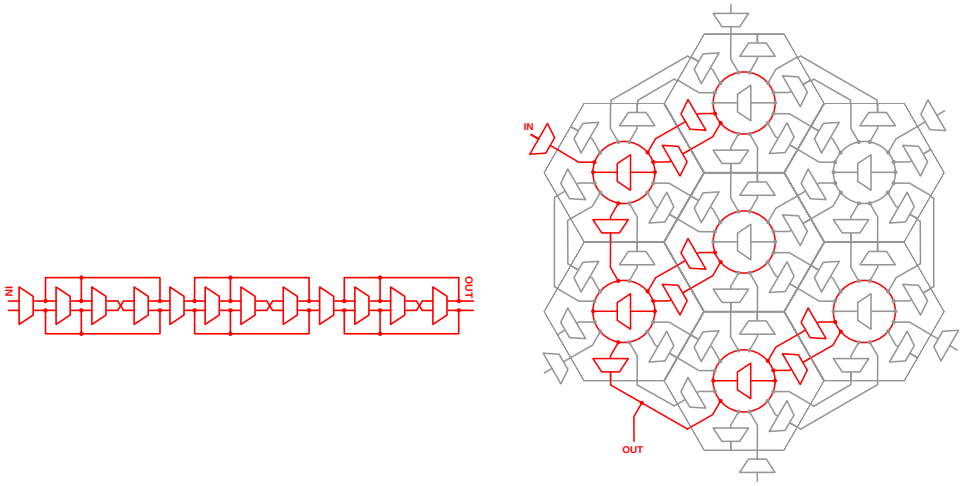
included blocks. Therefore, the availability of the ICs is eventually limited by how many kinds of analog blocks are included in the IC.

For example, Fig. 2.2 shows the field-programmable analog array (FPAA) in [6] which includes 55 tunable G_m cells. As a unit block, the tunable G_m cell includes six OTAs whose on/off is just controlled by digital program code in order to adjust the overall G_m, as shown in Fig. 2.2 (a). That is, the functionality of the unit block is fixed and only the parametric characteristics (i.e., G_m) are programmable. Therefore, when this FPAA is programmed to different analog systems, the things allowed to users are to decide whether to turn on or off each cell and G_m. Fig. 2.3 (a) shows an example analog system of sixth order bandpass filter and its placement-and-routing on the FPAA.



(a) (b)

Fig. 2.2 (a) The unit analog block (tunable G_m cell) and (b) array composition of the unit block in the field-programmable analog array [6].

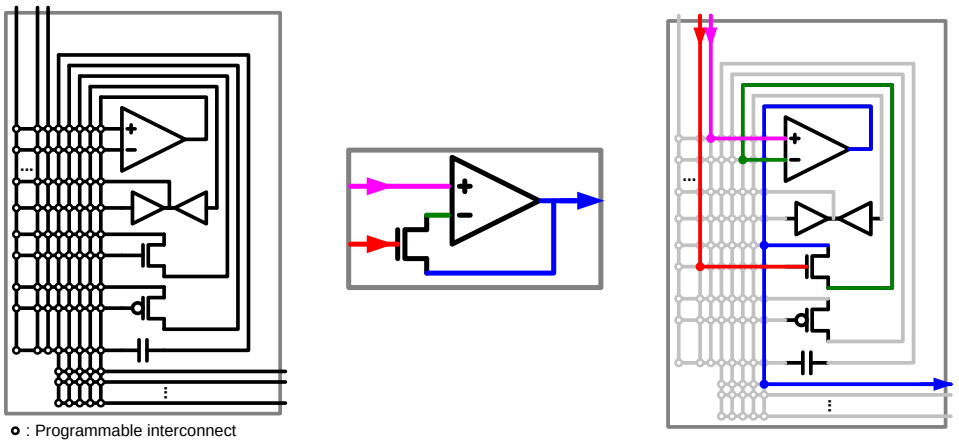


(a) (b)

Fig. 2.3 (a) Schematic of sixth bandpass filter and (b) exemplary placement-and-routing of the filter on FPAA in [6].

Fig. 2.4 (a) shows how the field programmable IC in [10] provides the programmable analog. That is, it contains more diverse analog blocks like OTAs, floating gates to construct trans-linear circuits, a voltage buffer, capacitors, a transmission gate to configure switched-capacitor, nMOSs and pMOSs with two common terminals for easily constructing source-follower or current-mirror, and Gilbert multipliers. Each block still has fixed input-to-output functionality. Then, users choose the connection among the included diverse analog blocks by reconfiguring the programmable interconnects. For example, a logarithmic amplifier in Fig. 2.4 (b) can be programmed as shown in Fig. 2.4 (c) by programing the interconnects to connect the required blocks (i.e. an OTA and an nMOS).

Similarly, [9] contains OTAs, capacitors, switched capacitor, pMOSs or nMOSs, floating gate pMOSs with multiple control gates.



(a) (b) (c)

Fig. 2.4 (a) Implementation of the programmable analog in [10], (b) schematics of logarithmic amplifier, (c) exemplary placement-and-routing of the amplifier on the programmable IC in [10].

The way of programmable analog in this thesis (i.e., each TCAB maps the functionality of the analog circuits rather than their detailed structural topologies.) is also distinguished from the works in [12]-[14] that provide transistor level programmability to emulate behavior and critical analog properties (e.g., I_d, g_m, and r_{out}) of each transistor in an intended system. Fig. 2.5 shows a unit block to emulate single transistor (nMOS case) and its array composition. Every single transistor in a target system are mapped to a unit cell in the array and the digital control code words (b_0, b_1, b_2) in MOSs of the unit cells are programmed in order to match I_d, g_m, and r_{out} to those of corresponding transistor in the system. However, due to the too fine-grained implementation, its availability is limited only to small-scale analog circuits (e.g., OTAs or analog filters) and difficult to be extended to today's mixed-signal systems consisting of innumerable transistor.

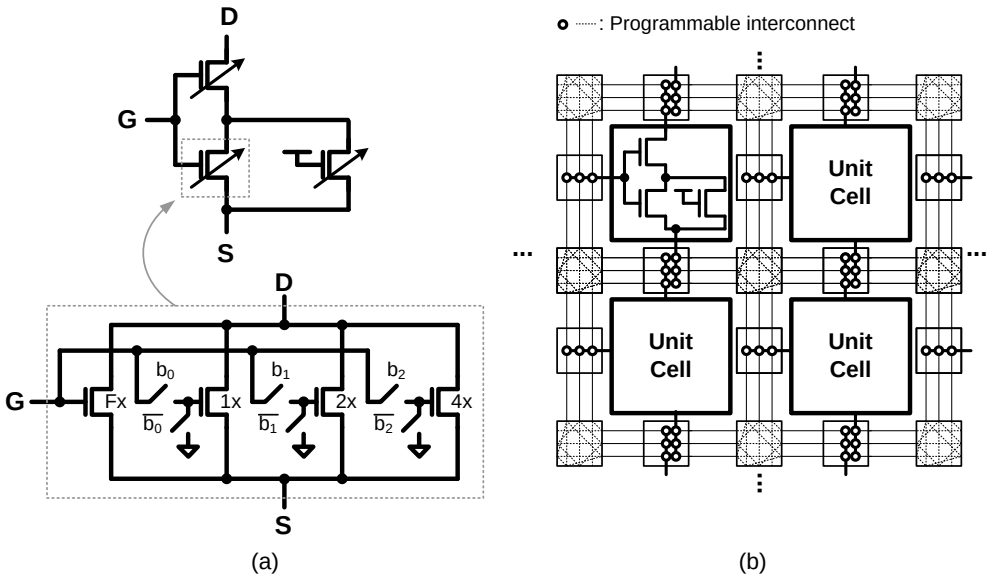


Fig. 2.5 (a) Unit block of programmable nMOSs and (b) its array composition [12].

2.1.2. Time-Domain Signal Processing

Another important point is that the TCAB processes signals in time domain, receiving and producing digital pulses of which frequency, delay, phase or pulse-width presents the analog information. The time-domain signal processing way of the TCAB is illustrated in Fig. 2.6 with the comparison to the voltage-domain signal

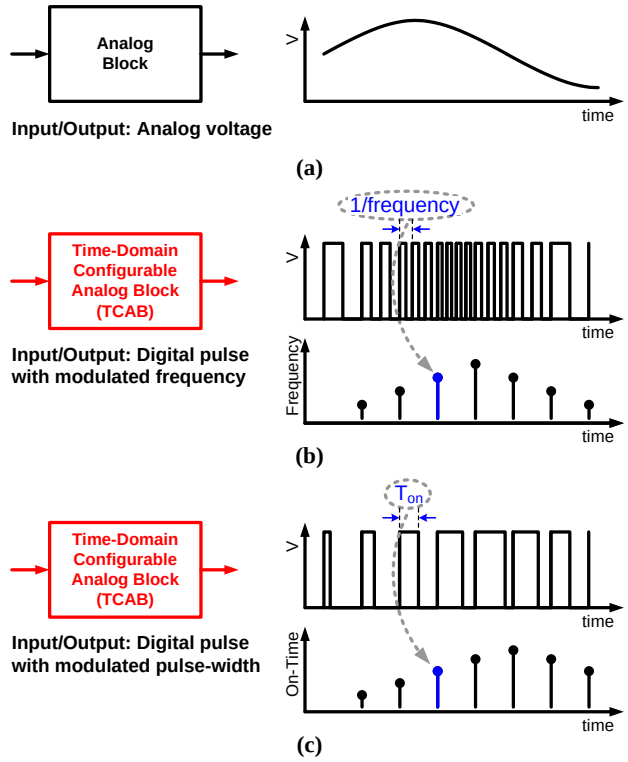


Fig. 2.6 The comparison among the signal representation way of (a) conventional analog blocks with continuous voltage forms, (b) TCAB with modulated pulse frequency, and (c) TCAB with modulated pulse-width.

processing way of the conventional analog blocks. Instead of processing analog information and exposing it with magnitude of voltage or current, the TCAB encodes the information to frequency, pulse-width, delay, or phase of digital pulses and the pulse sequences. Interestingly, this time-domain signal processing is a similar technique which time-based ADCs have adopted in order to overcome the various challenges in design of ADC (e.g., low supply voltage) as technology scales [19]-[22].

Since the inputs and outputs of the TCABs are digital pulses which are less susceptible to noise or distortion than signals in voltage or current forms, this work can achieve high programmability on signal propagation path. Actually, it is another major challenge to provide programmable connectivity for propagation of signals in field-programmable analog/mixed-signal IC because it is difficult to propagate analog signals over arbitrary path or long distance. Due to such difficulties, the work in [6] provides permanent connection between adjacent blocks and effectively disconnects them by programming the gain of the adjacent blocks to zero. Another implementation in [11] employs programmable switches which are placed only between the two adjacent blocks and lets users decide only whether to connect them. The work in [10] limitedly inserts analog buffers (e.g., OTA based unity-gain buffers) to convey analog signals farther, whereas most other interconnects are floating gate based switches that have limited availability due to their finite parasitic capacitance and resistance.

On the other hand, this work facilitates programmable connectivity comparable to that of digital FPGAs since both input and output of the TCAB are digital binary pulses. As can be seen in Chapter 2.4, the switch/connection blocks connecting

among the TCABs are simply implemented with digital tri-state inverters and digital buffers in a similar way of digital FPGAs. As a result, the time-domain representation of analog information makes it easy to implement large-size of TCAB array, propagating signals to everywhere in the array.

The following subchapters present circuit implementation of the TCAB and how the TCAB can change its input-to-output functions in time-domain. Also, the TCAB array composition is described with the implementation of programmable interconnects included in the array in Chapter 2.4.

2.2 Circuit Implementation of the TCAB

Fig. 2.7 shows the circuit implementation of the proposed TCAB. It consists of four sets of switched current source whose output current level is controlled by the preceded DAC, two digitally-controlled capacitors with reset switches, crossing detectors and an SR-latch.

The current sources, I_{1A}/I_{1B} and I_{2A}/I_{2B}, selectively charge the digitally-controlled capacitors, C_1 and C_2, depending on how the switches under each current source are configured by the 8 input signals, *IN*[7:0]. Once non-zero current flows to capacitor C_1 and the voltage across C_1 exceeds a certain threshold voltage, the following crossing detector makes falling transition at its output (XD_1). For this operation, the crossing detector is implemented as shown in Fig. 2.8. The SR-latch then makes the two output pulses, *OUT* and *OUTB*, logic 1 and logic 0, respectively. Simultaneously,

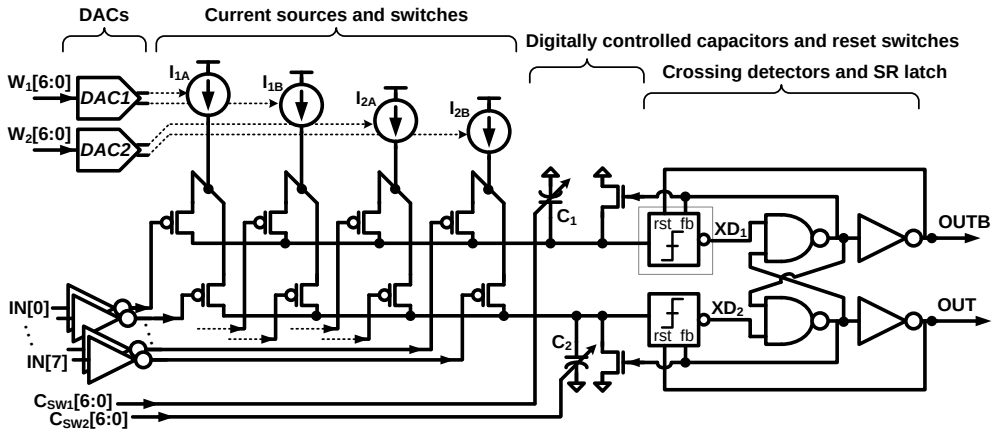


Fig. 2.7 Circuit implementation of TCAB core.

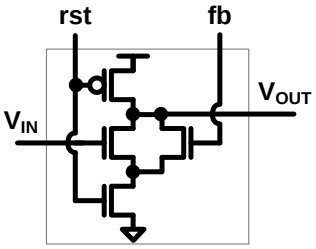


Fig. 2.8 Circuit implementation of the crossing detector in the TCAB.

C_1 is discharged and the voltage across C_1 is reset to zero by the reset switch. Then, the other capacitor C_2 takes turn being charged, whereas C_1 is maintained not to be charged. In this time, if the voltage across C_2 exceeds the threshold, the output pulses, *OUT* and *OUTB*, are toggled to logic 0 and logic 1, respectively. That is, only one of the two capacitors gets charged at a time in an alternating fashion, while generating output pulses. This basic operation is illustrated in Fig. 2.9 with timing diagram.

The time-domain quantity of the TCAB output pulse that represents analog information is decided by how each capacitor is charged. The voltage across each

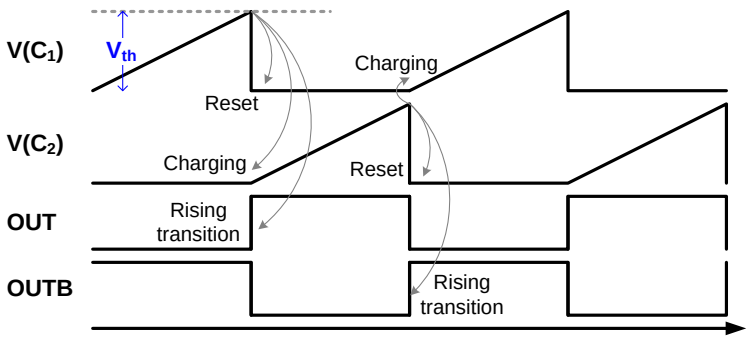


Fig. 2.9 Timing diagram for the basic operation of the TCAB.

capacitor after time t since time 0 when the corresponding capacitor starts being charged is given by

$$V_{C1}(t) = \int_0^t \frac{I_{C1}(\tau)}{C_1} d\tau,\ V_{C2}(t) = \int_0^t \frac{I_{C2}(\tau)}{C_2} d\tau, \quad (2.2.1)$$

where $I_{C1}(\tau)$ or $I_{C2}(\tau)$ denotes net current flowing to C_1 or C_2 at time τ. By adjusting the current, $I_{C1}(\tau)$ or $I_{C2}(\tau)$, or the capacitance of C_1 or C_2, the time required for each capacitor to reach the threshold voltage changes and the time when output pulse is asserted changes.

There are three ways to control the charging behavior, and therefore, the pulse modulation of the TCAB output, which carries analog information. Those are to adjust *IN*[7:0] for the switch configuration, W_1[6:0] and W_2[6:0] for the DACs, and C_{SW1}[6:0] and C_{SW2}[6:0] for the digitally-controlled capacitors.

First, the charging behavior can change depending on the configuration of the 8 switches which are turned on/off by input pulses, *IN*[7:0]. When the switches are configured so that constant currents, I_{C1} and I_{C2}, always flow to C_1 and C_2, the time which it takes for each output pulse to be asserted since the corresponding capacitor starts being charged is given by

$$t_{OUT} = \frac{V_{th} C_1}{I_{C1}} + t_{xing} + t_{logic},\ t_{OUTB} = \frac{V_{th} C_2}{I_{C2}} + t_{xing} + t_{logic}, \quad (2.2.2)$$

where V_{th} is the threshold voltage of crossing detector, t_{xing} denotes delay of crossing detector, and t_{logic} is logic gates delay from the SR-latch inputs to *OUT*/*OUTB*. In this case, output pulses oscillate and the oscillation period of the TCAB is given by

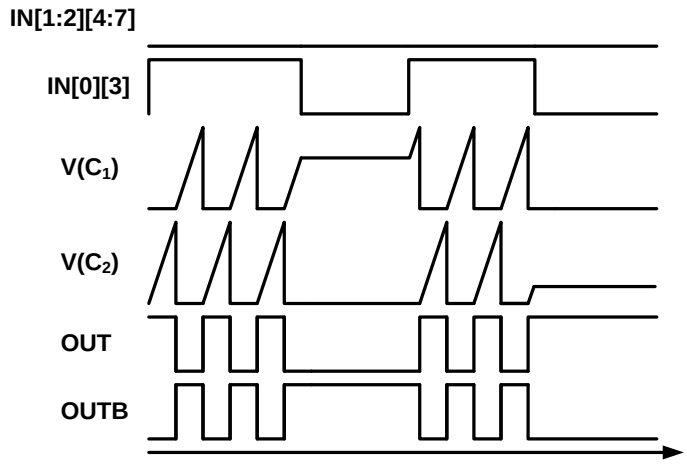


Fig. 2.10 Timing diagram for TCAB operation when the switch configuration changes.

$$T_{period} = \frac{V_{th}C_1}{I_{C1}} + \frac{V_{th}C_2}{I_{C2}} + 2\left(t_{xing} + t_{logic} + t_{reset}\right), \tag{2.2.3}$$

where t_{reset} denotes the time that it takes for one of capacitor reset switches to be released since the other reaches the threshold voltage of the crossing detector.

If the switch configuration changes in the middle of charging and no current flows to C_1 or C_2 for a second, the voltage across each capacitor remains fixed during that time. Then, the switch configuration changes again and I_{C1} and I_{C2} flow to C_1 and C_2, respectively, the output pulse is eventually asserted. When all the switches are open so that both I_{C1} and I_{C2} are always zero, then output pulses are not asserted at all. The described behaviors are illustrated in Fig. 2.10 with timing diagram when two switches are controlled by external signals and the others are maintained off.

Another way to control the charging behavior of the two capacitors is to change the current levels through the DACs. Each pair of current sources in the TCAB,

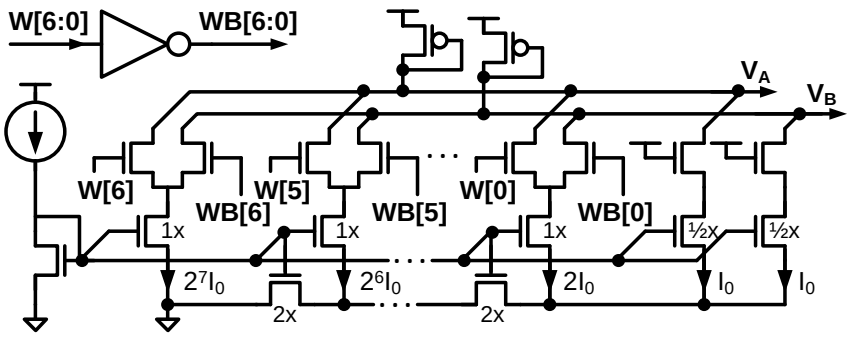


Fig. 2.11 Circuit implementation of nMOS ladder based current steering DAC in the TCAB.

I_{1A}/I_{1B} or I_{2A}/I_{2B}, is adjusted by the preceded DAC so that their output currents in a pair are biased to be complementary each other. That is, I_{1A}+I_{1B} (or I_{2A}+I_{2B}) remains constant regardless of W_1 (or W_2), while I_{1A} (or I_{2A}) increases and I_{1B} (or I_{2B}) decreases if W_1 (or W_2) increases and vice versa. To bias the paired current sources in this way, the preceded nMOS ladder based current steering DAC generates two voltages, V_A and V_B, as in Fig. 2.11. The ladder has similar architecture of R-2R ladder, therefore, the current through each pMOS is given by Eq. (2.2.4).

$$\begin{aligned} I_A &= I_0 + 2^1 W[0]\times I_0 + 2^2 W[1]\times I_0 + \cdots + 2^7 W[6]\times I_0, \\ I_B &= I_0 + 2^1 WB[0]\times I_0 + 2^2 WB[1]\times I_0 + \cdots + 2^7 WB[6]\times I_0, \end{aligned} \tag{2.2.4}$$

where I_0 is unit current step. Since WB[6:0] is inverse of W[6:0], the sum of I_A and I_B maintains same. Owing to its low-power consumption and compact size [23], the adopted DAC is suitable to compose the TCAB, considering that multiple TCABs are included in the proposed IC.

Lastly, it is also possible to adjust the charging rate by changing capacitances of C_1 and C_2. Each of C_1 and C_2 is basically an array of binary weighted capacitors with switches which are turned on/off by input digital codes C_{SW1}[6:0] and C_{SW2}[6:0], as shown in Fig. 2.12. Its equivalent output capacitance is given by

$$\begin{aligned} C_1 &= C_0 + 2^0 C_{sw1}[0]\times C_{step} + 2^1 C_{sw1}[1]\times C_{step} + \cdots + 2^6 C_{sw1}[6]\times C_{step}, \\ C_2 &= C_0 + 2^0 C_{sw2}[0]\times C_{step} + 2^1 C_{sw2}[1]\times C_{step} + \cdots + 2^6 C_{sw2}[6]\times C_{step}, \end{aligned} \quad (2.2.5)$$

where C_{step} is the unit capacitance and C_0 includes all the parasitic capacitance on that node and input capacitance of the following crossing detector. By changing the input digital codes C_{SW1}[6:0] and C_{SW2}[6:0], the capacitances of C_1 and C_2 are adjusted.

In addition to the described TCAB core in Fig. 2.7, the overall TCAB implement includes multiplexers for input signals (W_1[6:0], W_2[6:0], IN[7:0], C_{SW1}[6:0], and C_{SW2}[6:0]) and configuration blocks for selection signals of the multiplexers and storing of constants, as illustrated in Fig. 2.13. That is, instead of connecting input signals directly to the received signals, it is implemented for the signals to select among the received ones or programmed constants. For example, W_1[6:0] ,W_2[6:0], C_{SW1}[6:0], and C_{SW2}[6:0] of the core can be connected to one of the signals among

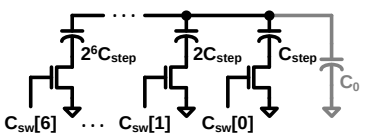


Fig. 2.12 Circuit implementation of digitally-controlled capacitor included in the TCAB.

received digital codes, their inverted codes, or programmed constants. Also, *IN*[7:0] can be connected to one of the signals among received digital pulse or zero. If they connected to zero, the corresponding switches after inverters are turned off. Configuration storages in Fig. 2.13 is where binary program codes are stored, which will be described in Chapter 4.4, Program Method. For the sake of simplicity, the rest figures to illustrate TCAB in this thesis can be presented, excluding the TCAB_CONFIG part in Fig. 2.13.

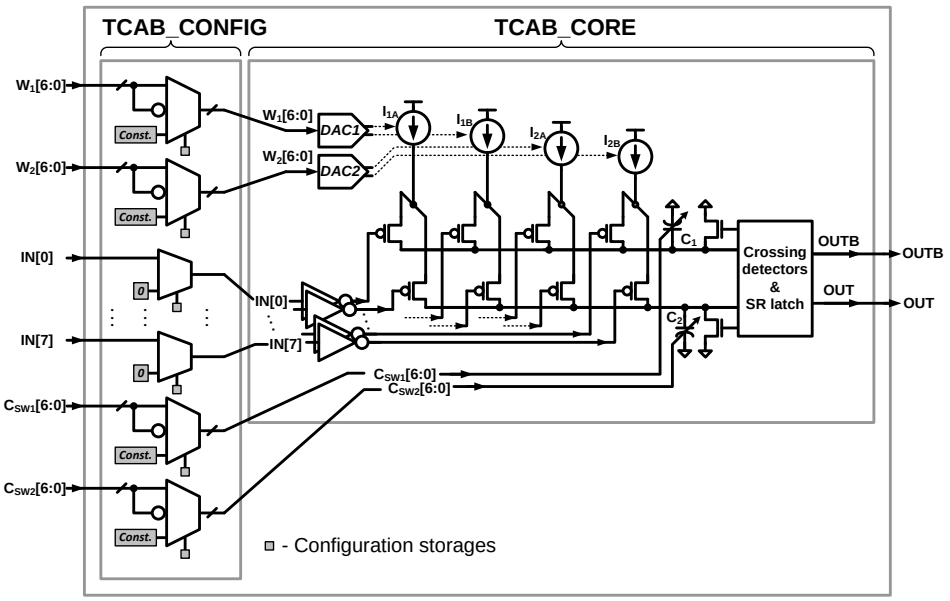


Fig. 2.13 TCAB implementation including the input multiplexers and configuration blocks.

2.3 Versatile Programmability of TCAB

In order to explain how the input-to-output function of the TCAB changes, this subchapter presents configuration examples of the TCAB when it operates as six different time-domain analog blocks which are required when composing timing generation (e.g., PLLs), data conversion (e.g., ADCs), or power management ICs (e.g, DC-DC converters). Note that its input-to-output function totally changes depending on how the three kinds of inputs (i.e., IN[7:0] for the switch configuration, W_1[6:0] and W_2[6:0] for DACs, and , C_{SW1}[6:0] and C_{SW2}[6:0] for digitally-controlled capacitors) are controlled.

Further, additional two examples, multiphase DCO and non-overlapping pulse generator, are also presented to show that multiple TCABs are combined together and operate as a time-domain analog block.

2.3.1. Relaxation Oscillator

First, a TCAB can operate as a relaxation oscillator [24] with a fixed frequency as shown in Fig. 2.14. The TCAB is configured so that the two output pulses, *OUT* and *OUTB*, are connected back to two inputs, IN[1] and IN[0], respectively. Due to the complementarity of the output pulses which consequently turn on/off the two switches below a current source, the output current I_{1A} is always fully steered to one of the two capacitors. Then, C_1 and C_2 are charged alternately and output pulses are toggled. The timing diagram of this operation is presented in Fig. 2.15. If C_{SW1}[6:0]

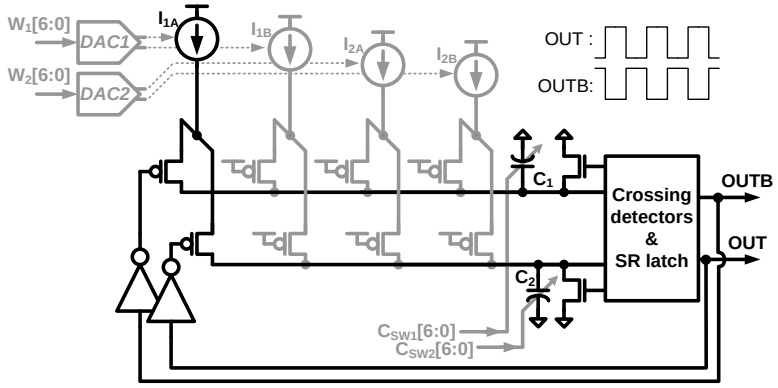


Fig. 2.14 The TCAB configuration as a fixed-frequency relaxation oscillator.

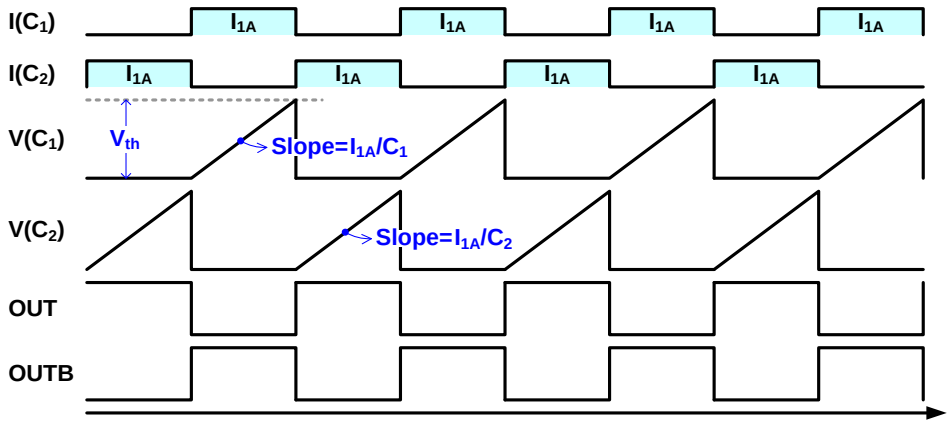


Fig. 2.15 Timing diagram of the TCAB when configured as a fixed-frequency relaxation oscillator.

and C_{SW2}[6:0] are programmed same so that C_1 and C_2 have same capacitances, the configured TCAB operates as relaxation oscillator of which output pulse period, T_{period}, follows (2.3.1).

$$T_{period} = \frac{V_{th}C_1}{I_{1A}} + \frac{V_{th}C_2}{I_{1A}} + 2t_{xing} + 2t_{logic} + 2t_{reset}$$
$$= 2\left(\frac{V_{th}C_1}{I_{1A}} + t_{xing} + t_{logic} + t_{reset}\right). \quad (2.3.1)$$

By changing the current level of I_{1A} via W_1[6:0] or two capacitances via C_{SW1}[6:0] and C_{SW2}[6:0] via programming, the TCAB is reconfigured to different relaxation oscillator with different period.

Fig. 2.16 also shows other four ways to configure relaxation oscillator with the TCAB. The relaxation oscillators in Fig. 2.16 (a)-(d) have the same behavior of that in Fig. 2.14, but with different expressions for T_{period}. Assuming C_1 and C_2 have same capacitances for Fig. 2.16 (a)-(d) and W_1[6:0] and W_2[6:0] are same so that I_{1A} and I_{2A} have same output currents for Fig. 2.16 (c)-(d), T_{period} for each is given by Eq.

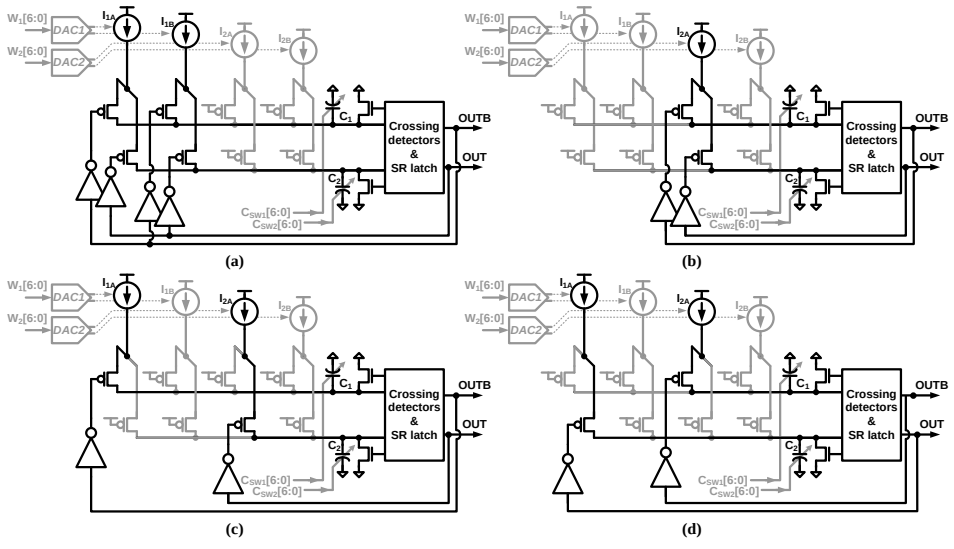


Fig. 2.16 The TCAB configurations as different relaxation oscillators.

(2.3.2) - Eq. (2.3.5), respectively.

$$\begin{aligned} T_{period} &= \frac{V_{th}C_1}{I_{1A}+I_{1B}} + \frac{V_{th}C_2}{I_{1A}+I_{1B}} + 2t_{xing} + 2t_{logic} + 2t_{reset} \\ &= 2\left(\frac{V_{th}C_1}{I_{1A}+I_{1B}} + t_{xing} + t_{logic} + t_{reset} \right). \end{aligned} \tag{2.3.2}$$

$$\begin{aligned} T_{period} &= \frac{V_{th}C_1}{I_{2A}} + \frac{V_{th}C_2}{I_{2A}} + 2t_{xing} + 2t_{logic} + 2t_{reset} \\ &= 2\left(\frac{V_{th}C_1}{I_{2A}} + t_{xing} + t_{logic} + t_{reset} \right). \end{aligned} \tag{2.3.3}$$

$$\begin{aligned} T_{period} &= \frac{V_{th}C_1}{I_{1A}} + \frac{V_{th}C_2}{I_{2A}} + 2t_{xing} + 2t_{logic} + 2t_{reset} \\ &= 2\left(\frac{V_{th}C_1}{I_{1A}} + t_{xing} + t_{logic} + t_{reset} \right). \end{aligned} \tag{2.3.4}$$

$$\begin{aligned} T_{period} &= \frac{V_{th}C_1}{I_{2A}} + \frac{V_{th}C_2}{I_{1A}} + 2t_{xing} + 2t_{logic} + 2t_{reset} \\ &= 2\left(\frac{V_{th}C_1}{I_{1A}} + t_{xing} + t_{logic} + t_{reset} \right). \end{aligned} \tag{2.3.5}$$

In addition to relaxation oscillators in Fig. 2.14 and Fig. 2.16, there are 64 different ways to configure oscillators with the TCAB.

2.3.2. Digitally-Controlled Oscillator

Second, a TCAB can operate as a DCO when it is configured as shown in Fig. 2.17. The TCAB is configured so that the one of two output pulses, *OUT*, is fed to two inputs, *IN*[1] and *IN*[5], and the other, *OUTB*, is connected to other two inputs

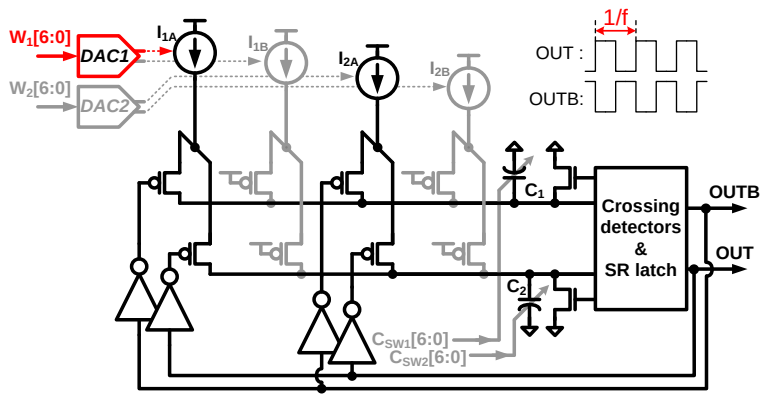


Fig. 2.17 The TCAB configuration as a DCO.

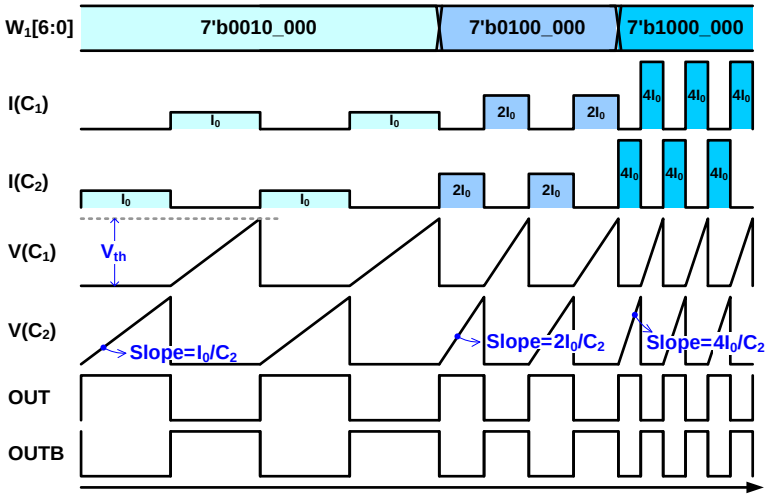


Fig. 2.18 Timing diagram of the TCAB when configured as a DCO.

IN[0] and *IN*[4], in order to conduct both I_{1A} and I_{2A}. Similar to the configuration of the TCAB as a relaxation oscillator, the current I_{1A} and I_{2A} are always fully steered to one of the two capacitors and alternately charge C_1 and C_2. The timing diagram of this operation is presented in Fig. 2.18, where the relative magnitude of current and oscillation frequency difference are shown. When W_1[6:0] increases, I_{1A} increases via the DAC1. Then, each capacitor gets charged faster, increasing output pulse frequency. Assuming t_{xing}, t_{logic}, and t_{reset} are relatively small amount compared with charging time of the capacitors and the capacitances of C_1 and C_2 have same value, then output frequency of the TCAB, f_{osc}, is given by Eq. (2.3.6), as a linear function of input digital code W_1[6:0].

$$\begin{aligned} f_{osc} &= \frac{1}{\dfrac{V_{th}C_1}{I_{1A}+I_{2A}} + \dfrac{V_{th}C_2}{I_{1A}+I_{2A}} + 2\left(t_{xing}+t_{logic}+t_{reset}\right)} \\ &\cong \frac{I_{1A}+I_{2A}}{2V_{th}C_1} = \frac{k\times W_1 + I_{2A}}{2V_{th}C_1}, \end{aligned} \tag{2.3.6}$$

where k is gain from DAC input to I_{1A} (i.e., current change per unit change in the input code, $\Delta I_{1A}/\Delta W_1$). The minimum frequency of this DCO is mainly determined as $I_{2A}/2V_{th}C_1$ and its gain (i.e., frequency change per unit change in the input code, $\Delta f_{osc}/\Delta W_1$) is $k/2V_{th}C_1$.

It is also possible to program different DCOs with different configurations of the TCAB. Fig. 2.19 shows additional six examples that the TCAB operates as DCO. The described basic operation is maintained same, the only difference is the equations that present f_{osc}. For example, the configured DCO in Fig. 2.19 (a) has the same connection when output pulses are fed back to switch control signals. However,

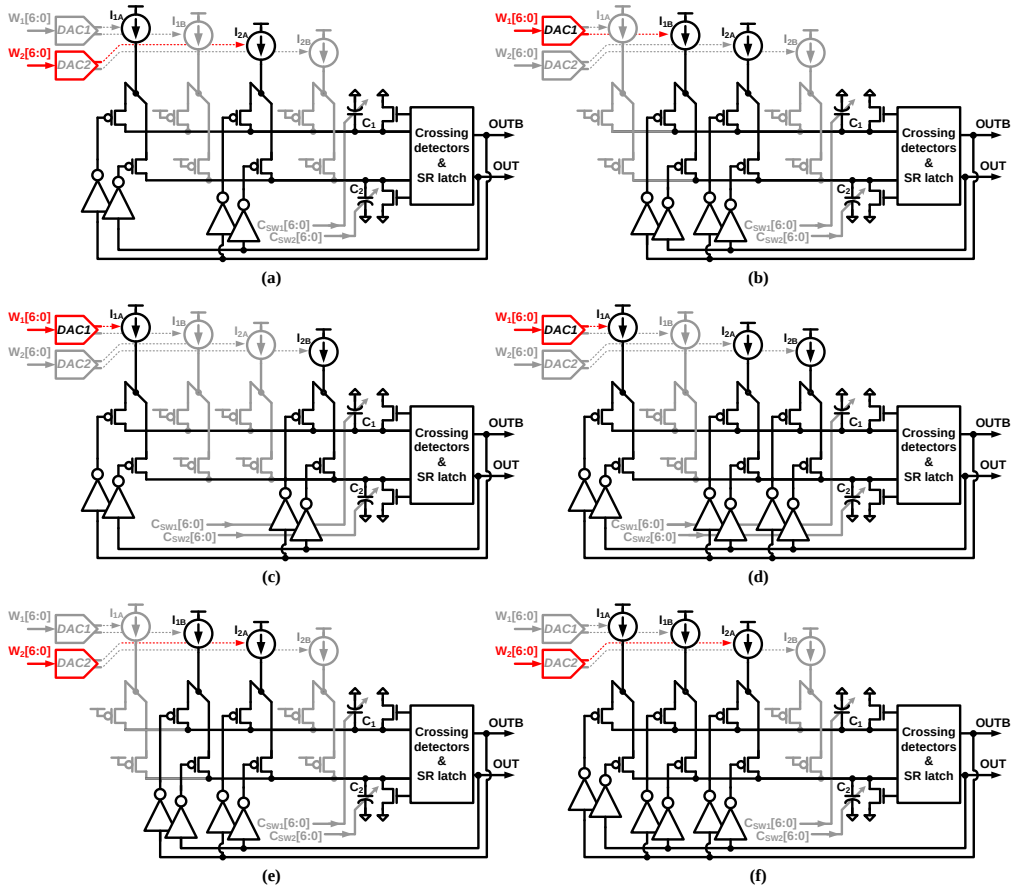


Fig. 2.19 The TCAB configurations as different DCOs.

its frequency is controlled via W_2[6:0], not W_1[6:0]. Therefore, f_{osc} of the DCO in Fig. 2.19 (a) is determined as Eq. (2.3.7), a function of W_2[6:0].

$$f_{osc} \cong \frac{I_{1A} + I_{2A}}{2V_{th}C_1} = \frac{k \times W_2 + I_{1A}}{2V_{th}C_1}. \tag{2.3.7}$$

In Fig. 2.19 (b), *OUT* and *OUTB* are connected back to *IN*[3],[5] and *IN*[2],[4], respectively. Then, f_{osc} is determined by Eq. (2.3.8).

$$f_{osc} \cong \frac{I_{1B} + I_{2A}}{2V_{th}C_1} = \frac{k \times (127 - W_1) + I_{2A}}{2V_{th}C_1}. \quad (2.3.8)$$

That is, f_{osc} increases when W_1[6:0] decreases and the opposite happens when W_1[6:0] increases. The DCOs in Fig. 2.19 (c) and (d) have the very similar that of Fig. 2.17 with the only difference in the minimum frequency. f_{osc} of the DCOs in Fig. 2.19 (c) and (d) is given by Eq. (2.3.9) and Eq. (2.3.10), respectively.

$$f_{osc} \cong \frac{I_{1A} + I_{2B}}{2V_{th}C_1} = \frac{k \times W_1 + I_{2B}}{2V_{th}C_1}, \quad (2.3.9)$$

$$f_{osc} \cong \frac{I_{1A} + I_{2A} + I_{2B}}{2V_{th}C_1} = \frac{k \times W_1 + I_{2A} + I_{2B}}{2V_{th}C_1}. \quad (2.3.10)$$

Also, f_{osc} of the DCOs in Fig. 2.19 (e) and (f) is given by Eq. (2.3.11) and Eq. (2.3.12), respectively, each as a function of W_2[6:0].

$$f_{osc} \cong \frac{I_{1B} + I_{2A}}{2V_{th}C_1} = \frac{k \times W_2 + I_{1B}}{2V_{th}C_1}, \quad (2.3.11)$$

$$f_{osc} \cong \frac{I_{1A} + I_{1B} + I_{2A}}{2V_{th}C_1} = \frac{k \times W_2 + I_{1A} + I_{1B}}{2V_{th}C_1}. \quad (2.3.12)$$

2.3.3. Digital Pulse-Width Modulator

Third, a TCAB configured similar to relaxation oscillator in Fig. 2.14 can also operate as a DPWM [24] as shown in Fig. 2.20. The only difference is that the

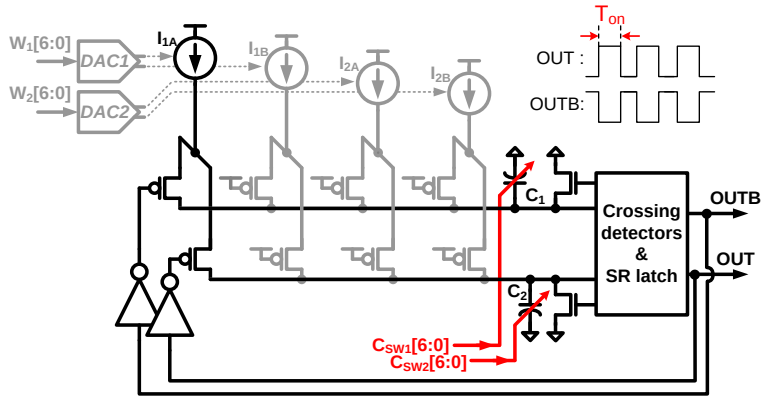


Fig. 2.20 The TCAB configuration as a DPWM.

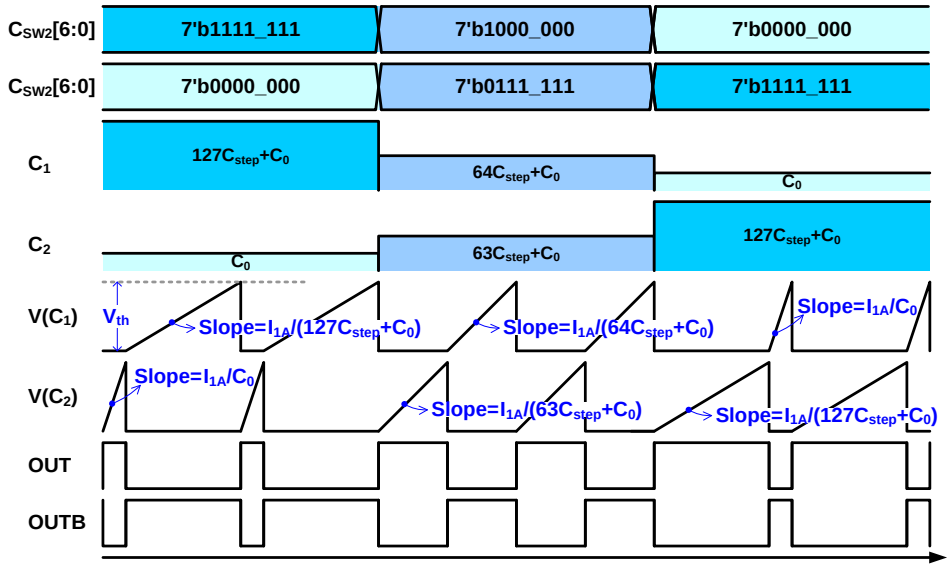


Fig. 2.21 Timing diagram of the TCAB when configured as a DPWM.

capacitances of C_1 and C_2 are adjusted in a complementary fashion through C_{SW1}[6:0] and C_{SW2}[6:0] instead of adjusting charging current, respectively, maintaining the sum of those two digital input code as 127. Then, the TCAB exhibits same behavior as that of relaxation oscillator, as shown in timing diagram of Fig. 2.21, where the relative capacitance and time difference are shown. Its oscillation period given by Eq. (2.2.3) and duty-cycle of output pulse, *OUT*, follows Eq. (2.3.13).

$$\begin{aligned} D &= \frac{T_{on}}{T_{period}} \\ &= \frac{\dfrac{V_{th}C_2}{I_{1A}} + t_{xing} + t_{logic} + t_{reset}}{\dfrac{V_{th}C_1}{I_{1A}} + \dfrac{V_{th}C_2}{I_{1A}} + 2\left(t_{xing} + t_{logic} + t_{reset}\right)} \\ &= \frac{\dfrac{V_{th}\left(C_0 + C_{sw2} \times C_{step}\right)}{I_{1A}} + t_{xing} + t_{logic} + t_{reset}}{\dfrac{V_{th}\left(2 \times C_0 + 127 \times C_{step}\right)}{I_{1A}} + 2\left(t_{xing} + t_{logic} + t_{reset}\right)} \\ &\cong \frac{C_0 + C_{sw2} \times C_{step}}{2 \times C_0 + 127 \times C_{step}}. \end{aligned} \tag{2.3.13}$$

That is, its duty-cycle is adjusted as a linear function of C_{SW2}[6:0]. If it is carefully designed so that C_0 and the three kinds of delay, t_{xing}, t_{logic}, and t_{reset}, are relatively small compared to $127C_{step}$ and charging time of the capacitors, respectively, the configured DPWM covers wide range of duty-cycle.

2.3.4. Gated Oscillator

Fourth, the TCAB is a gated oscillator as in Fig. 2.22. In this case, an external input is connected to the input switches so that the circuit oscillates only when the input is high. This operation is illustrated with timing diagram in Fig. 2.23. The number of edge transitions in the output pulses is proportional to the pulse width of

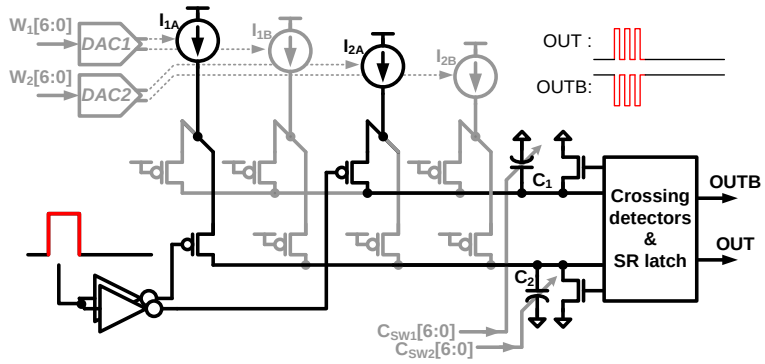


Fig. 2.22 The TCAB configuration as a gated oscillator.

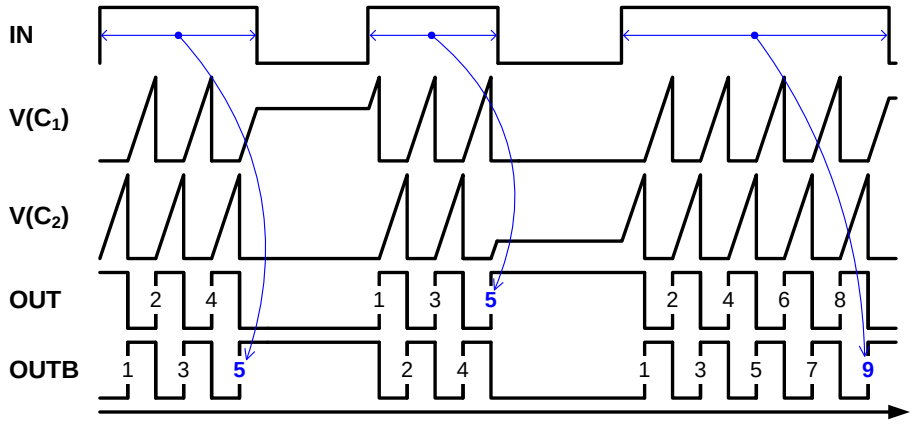


Fig. 2.23 Timing diagram of the TCAB when configured as a gated-oscillator.

the input. Therefore, one can comprise a TDC [25], [26] with this TCAB followed by a counter. The counter records the number of edge transitions in the output pulse of gated oscillator, which directly relates to the on-time of the input pulse. That is, the output of counter, which is digital in nature, provides a quantized estimate of input pulse-width. The gated oscillator configured with the proposed TCAB can also hold its intermediate state similar to the case of [25]. As a result, the TDC achieves first order noise shaping.

2.3.5. Digitally-Controlled Delay Cell

Next, the TCAB can serve as a digitally-controlled delay cell as in Fig. 2.24. A pair of complementary input signals are connected to *IN*[1:0] and steers the current I_{1A} between C_1 and C_2. In this configuration, only C_1 gets charged if *IN*[0] is high and the other, C_2, gets charged if *IN*[1] is high, as shown in Fig. 2.25. Therefore, the outputs do not oscillate but toggle only once whenever the two inputs toggle with

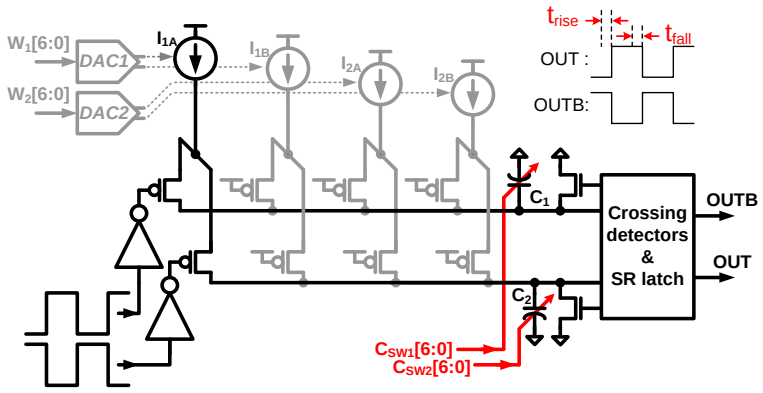


Fig. 2.24 The TCAB configuration as a digitally-controlled delay cell.

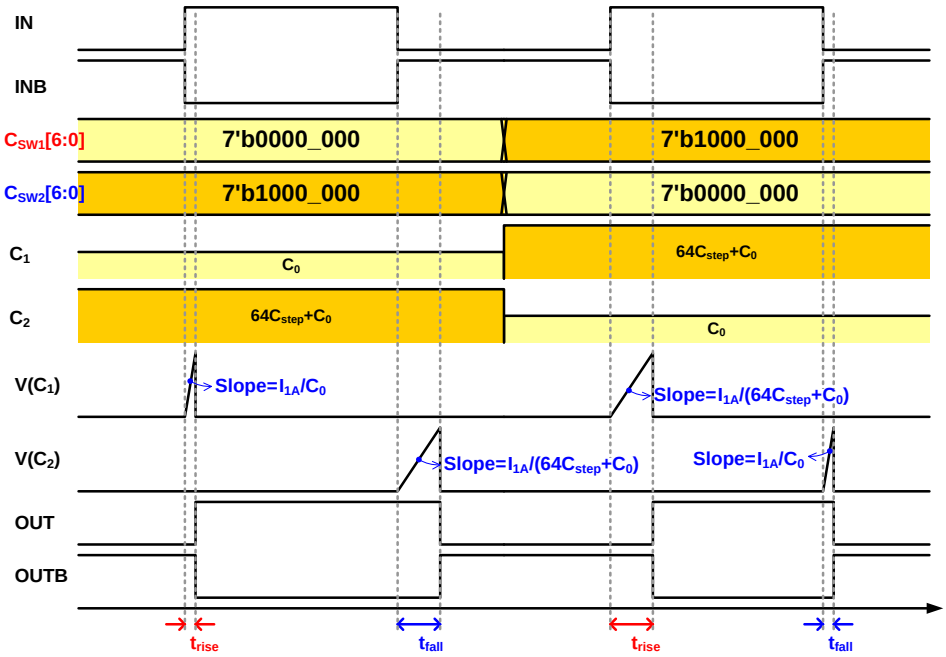


Fig. 2.25 Timing diagram of the TCAB when configured as a digitally-controlled delay cell.

rising or falling delay given by

$$t_{rise} = \frac{V_{th}C_1}{I_{1A}} + t_{xing} + t_{logic},\ t_{fall} = \frac{V_{th}C_2}{I_{1A}} + t_{xing} + t_{logic}. \tag{2.3.14}$$

By adjusting C_{SW1}[6:0] and C_{SW2}[6:0], delay can be controlled linearly as a function of the two digital input codes.

2.3.6. Phase Interpolator

Lastly, the TCAB operates as a phase interpolator (PI) when two pairs of complementary input signals steer the current I_{1A} and I_{1B}, respectively, as shown in Fig. 2.26.

Its operating timing diagram is given in Fig. 2.27. If the rising edge of *CLK*1 arrives earlier than that of *CLK*2, the capacitor C_1 is charged by the current source I_{1A} for the time period when only *CLK*1 is high. Then, voltage across C_1 at t_2 when the rising edge of *CLK*2 arrives is given by

$$V_{C1}(t_2) = \frac{I_{1A}}{C_1}(t_2 - t_1) = \frac{I_{1A}}{C_1}(\phi_{CLK2} - \phi_{CLK1}) \times \frac{1}{2\pi f}, \tag{2.3.15}$$

where ϕ_{CLK1} and ϕ_{CLK2} denotes phase of *CLK*1 and *CLK*2, respectively, and f is frequency of *CLK*1 and *CLK*2. Once *CLK*2 rises, C_1 is charged with the current amount of I_{1A}+I_{1B}. Then, the time it takes for C_1 to reach the threshold voltage of the ensuing crossing detector, V_{th}, since t_2 is given by

$$t_{out} - t_2 = \left(V_{th} - \frac{I_{1A}}{C_1}(\phi_{CLK2} - \phi_{CLK1}) \times \frac{1}{2\pi f} \right) \times \frac{C_1}{I_{1A} + I_{1B}}. \tag{2.3.16}$$

That is, if the phase of *CLK*1 is earlier than that of *CLK*2 so that ϕ_{CLK1} is smaller than ϕ_{CLK2}, the output phase, ϕ_{OUT}, is given by

$$\begin{aligned} \phi_{OUT} &= \phi_{CLK2} + (t_{out} - t_2) \times 2\pi f \\ &= \phi_{CLK2} + 2\pi f \frac{CV_{th}}{I_{1A} + I_{2B}} - (\phi_{CLK2} - \phi_{CLK1}) \frac{I_{1A}}{I_{1A} + I_{1B}}. \end{aligned} \tag{2.3.17}$$

As W_1[6:0] increases, ϕ_{OUT} gets earlier since I_{1A} increases, whereas I_{1A}+I_{1B} maintains

same. For the falling transition out *OUT*, the same behavior occurs when rising edge of *CLK*1*B* and *CLK*2*B* arrive, charging C_2. As a result, the circuit generates a delay which is a weighted sum of the delays from the two input pairs with different arrival time [27], [28].

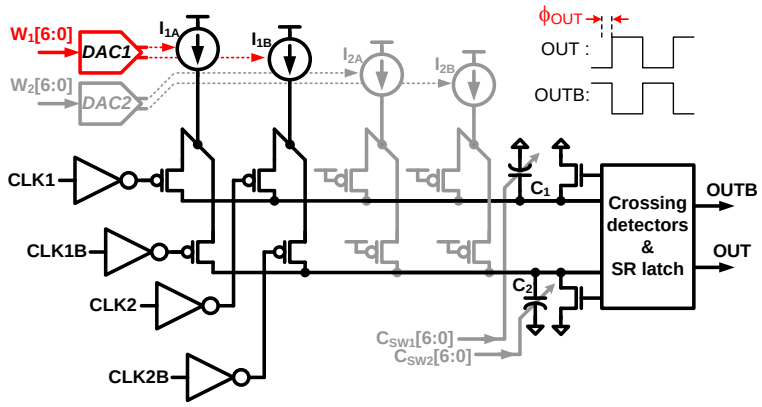


Fig. 2.26 The TCAB configuration as a phase interpolator.

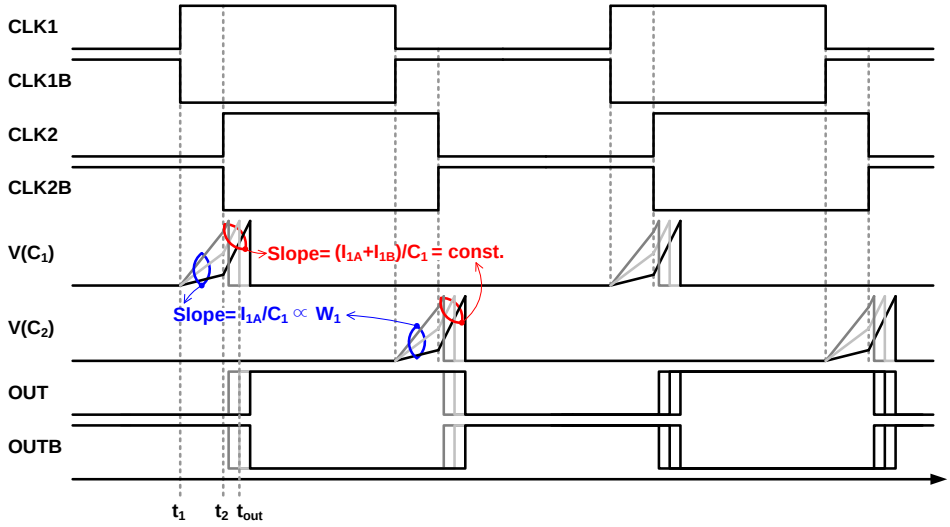


Fig. 2.27 Timing diagram of the TCAB when configured as a phase interpolator.

2.3.7. Multiphase DCO

As an example to show that more than two TCABs are configured to operate as a time-domain analog block, Fig. 2.28 presents an example that the two TCABs are combined together in order to operate as a four phase DCO whose four output pulses have 90 degree space. *OUT* and *OUTB* of TCAB1 are connected to *IN*[1][5] and *IN*[0][4] of TCAB2, respectively. Likewise, *OUT* and *OUTB* of TCAB2 are connected to *IN*[1][5] and *IN*[0][4] of TCAB1, respectively. Those two TCABs have common input digital code word W_1[6:0]. Once C_1 in TCAB1 is charged and reaches V_{th} of the ensuing crossing detector, *OUT*[2] (i.e., *OUT* of TCAB1) is asserted and *OUT*[0] (i.e., *OUTB* of TCAB1) toggles to zero. Then, C_2 in TCAB2 takes turn being charged and *OUT*[3] is asserted and *OUT*[1] toggles to zero. In this way, a total of the four capacitors in the two TCABs are alternately charged in sequence of C_1 in TCAB1, C_2 in TCAB2, C_2 in TCAB1, C_1 in TCAB2, C_1 in TCAB1, …, and then 4 output pulses are generated. This sequence is illustrated with timing diagram

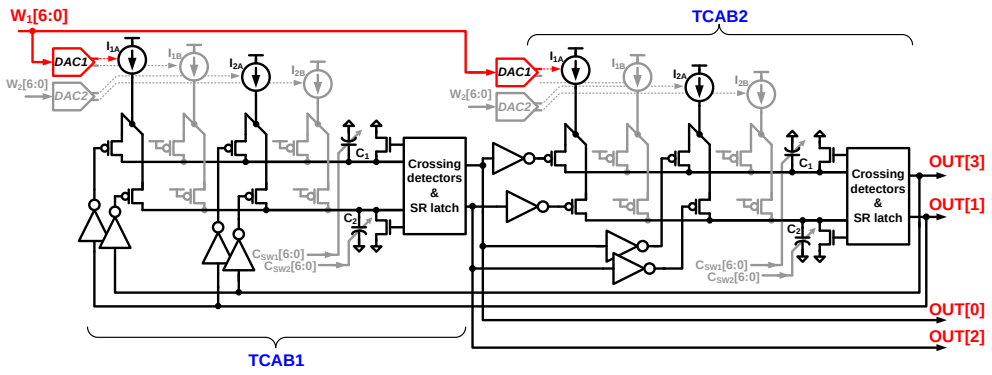


Fig. 2.28 The TCABs configuration as a multiphase (4-phase) DCO.

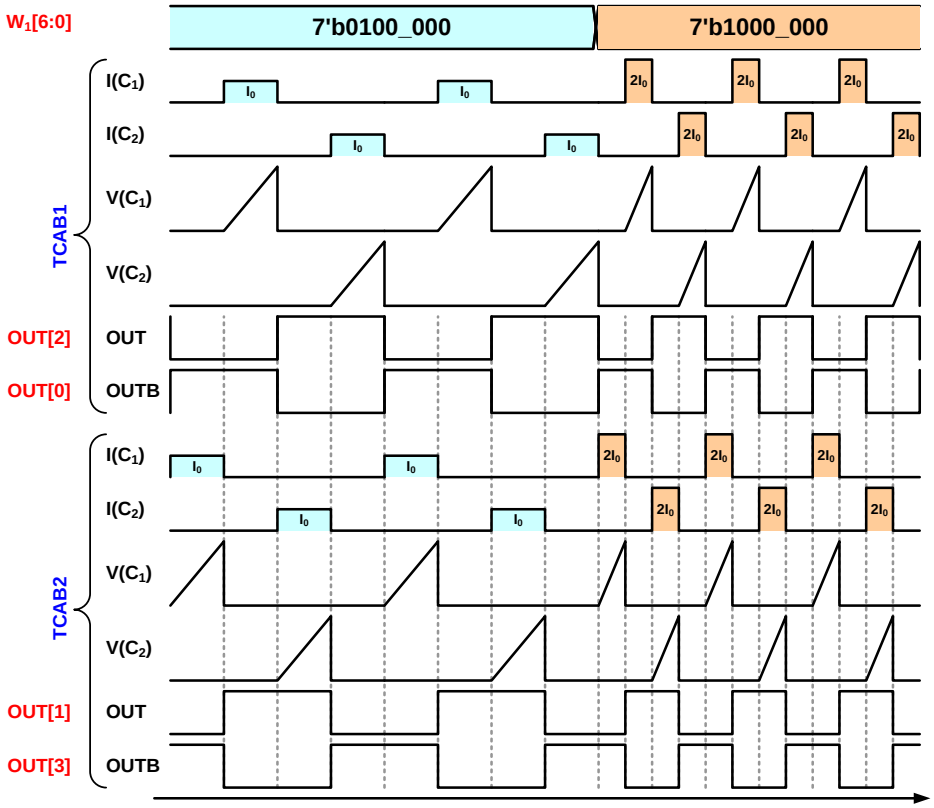


Fig. 2.29 Timing diagram for the operation of the TCABs as a multiphase DCO.

in Fig. 2.29.

Its oscillating frequency can be controlled by adjusting charging current I_{1A} both in TCAB1 and TCAB2 via W_1[6:0]. That is, if capacitors in the two TCABs are programmed to have equal capacitances and both I_{2A} are configured to flow same amount of current, its oscillating frequency f_{osc} is given by

$$f_{osc} = \frac{1}{\frac{4V_{th}C_1}{I_{1A}+I_{2A}} + 4\left(t_{xing}+t_{logic}+t_{reset}\right)} \cong \frac{I_{1A}+I_{2A}}{4V_{th}C_1} = \frac{k\times W_1 + I_{2A}}{4V_{th}C_1}, \qquad (2.3.18)$$

In general, 2*N* phase DCO can be programmed by configuring *N* TCABs in a similar way of Fig. 2.28

2.3.8. Non-overlapping Pulse Generator

Another example in Fig. 2.30 shows that the two TCABs are combined together in order to generate non-overlapping pulses. Each TCAB receives the common pulse input and operates as a digitally-controlled delay cell described earlier in Fig. 2.24. In this time, C_{SW1}[6:0] and C_{SW2}[6:0] of each TCAB are programmed with constants so that C_{SW1}[6:0] of TCAB1 is larger than that of TCAB2 and C_{SW2}[6:0] of TCAB2 is

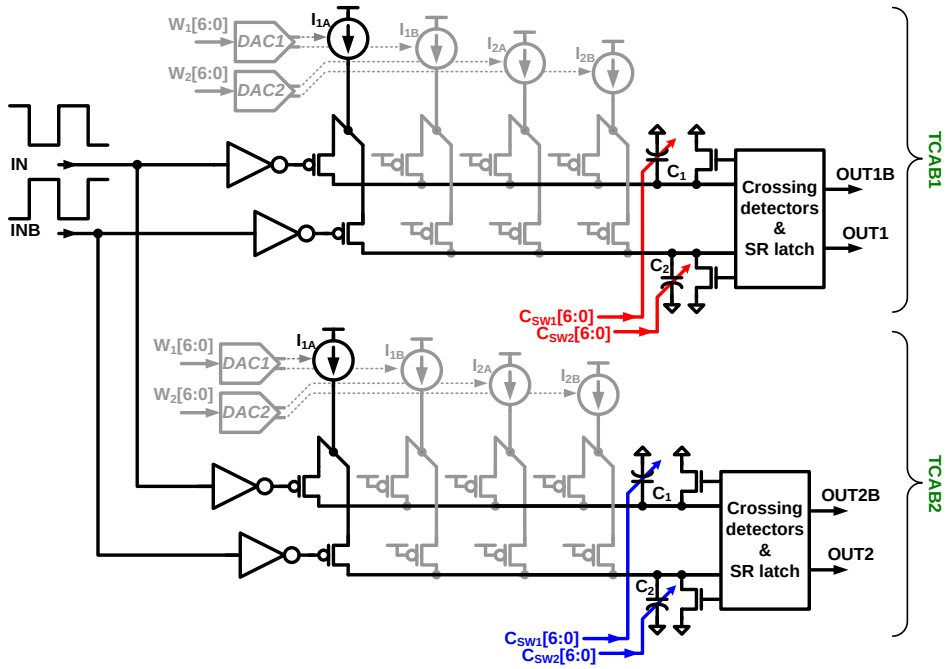


Fig. 2.30 The TCABs configuration as a non-overlapping pulse generator.

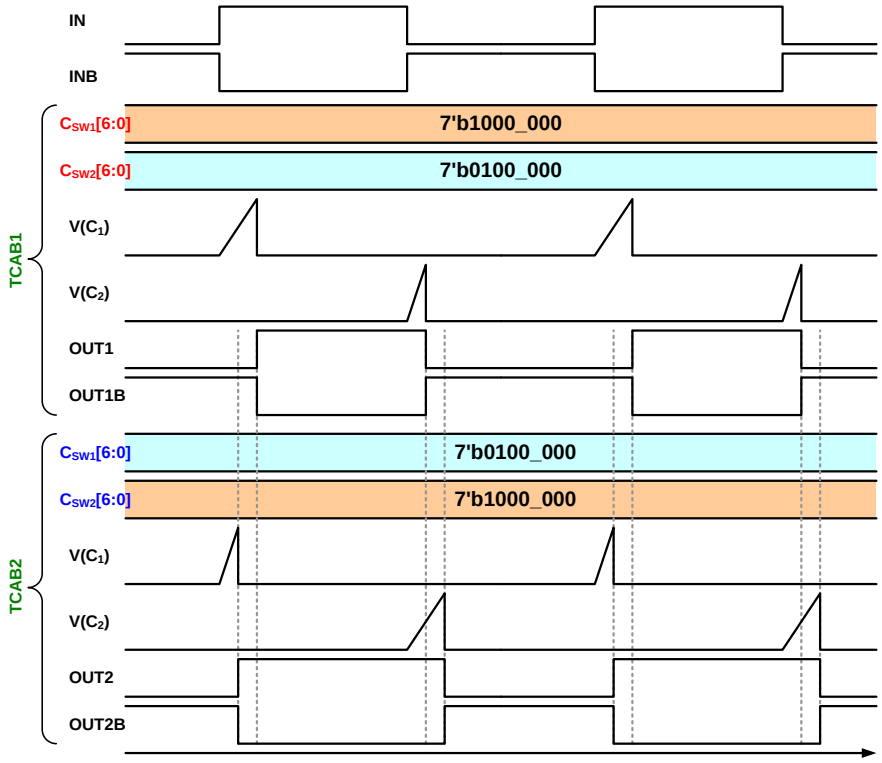


Fig. 2.31 Timing diagram for the operation of the TCABs as a non-overlapping pulse generator.

smaller than that of TCAB2. Then, *OUT*2 is always asserted earlier than *OUT*1 and *OUT*1*B* is always asserted earlier than *OUT*1*B* as shown in timing diagram (Fig. 2.31). Their timing difference is expressed as:

$$t_{rise1-rise2} = t_{fall2-fall1} = \frac{V_{th}C_{1,1}}{I_{1A}} - \frac{V_{th}C_{2,1}}{I_{1A}}. \qquad (2.3.19)$$

As a result, among the four output signals, *OUT*1 and *OUT*2*B* become the final output pulses that have no time period of being turned on simultaneously.

2.4 TCAB Array with Programmable Interconnects

This subchapter describes how multiple TCABs are assembled in an array together with programmable interconnects. The implementation of the programmable interconnects (i.e., connection block and switch block) in the array is also presented.

2.4.1. TCAB Array Composition

The TCAB array composition follows a traditional 2-D island-style FPGA architecture which is commonly adopted among commercial FPGAs [42], as illustrated in Fig. 2.32. The TCABs are regularly placed on 2-D grid and each TCAB is surrounded by wire tracks and programmable interconnect blocks of switch blocks (SB) and connection blocks (CB). The directional 4 wires are placed in both horizontal and vertical way around each TCAB. Input and output signals of each TCAB are connected the surrounding wire tracks via connection blocks. The adjacent wire tracks are interconnected via switch blocks that are placed at the intersection of horizontal and vertical tracks.

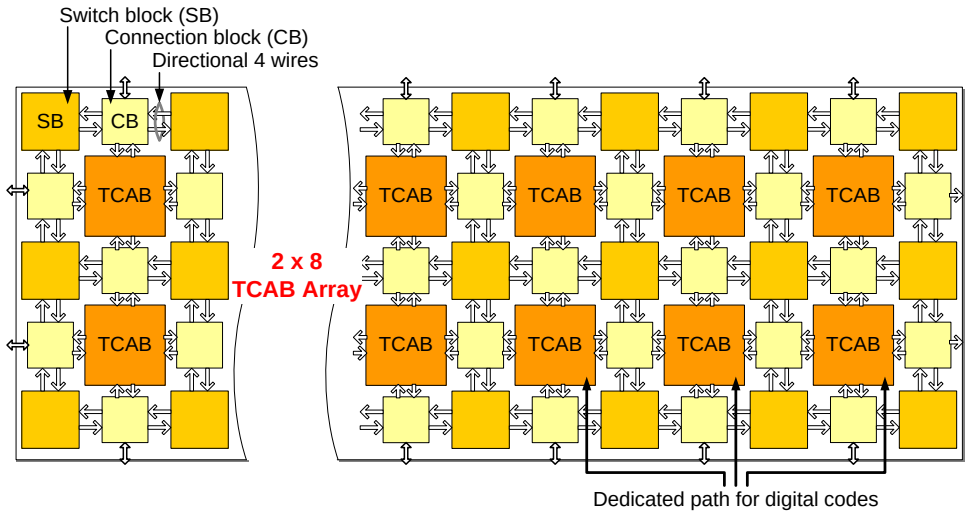


Fig. 2.32 Composition of the TCAB array.

2.4.2. Programmable interconnects

As the TCABs receive and produce digital pulses, both switch block and connection block in the TCAB array are simply implemented based on digital tri-state inverters, as shown in Fig. 2.33. Therefore, highly programmable connectivity comparable to that of digital FPGAs is achieved.

Depending on which tri-state inverters are turned on, the connection block decides which routing wires to be connected to the input and output signals of the TCABs, Likewise, the tri-state inverters in switch blocks decide the received signals to go forward, left or right. The architecture of switch blocks follows that of [43] in order to provide higher flexibility in interconnect than other architectures. This programmable routing architecture with connection blocks and switch blocks

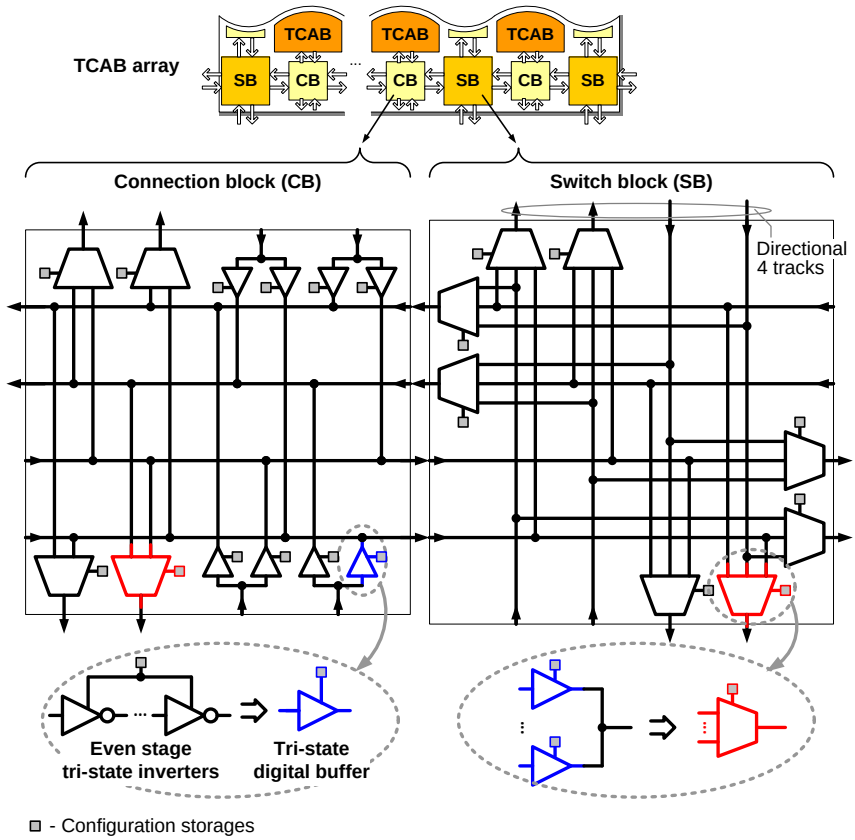


Fig. 2.33 Implementation of the programmable interconnects in the TCAB array.

follows that of commercial FPGAs [42] so that the TCAB array facilitates high programmability on signal path.

Among input and output signals of TCAB, only input pulses (i.e., *IN*[7:0]) and output pulses (i.e., *OUT* and *OUTB*) are conveyed through the described programmable interconnects. In specific, a single TCAB receives 8 input pulses from four-sided adjacent connection blocks. Two output pulses, *OUT* and *OUTB*, of each TCAB can be connected to its all the four adjacent connection blocks.

The other input signals (i.e., digital codes - W_1[6:0], W_2[6:0], C_{SW1}[6:0], and C_{SW2}[6:0]) are either programmed with fixed constants or directly connected to output of ALU array. The former case is when the TCAB is programmed to a fixed-frequency oscillator, fixed-frequency gated oscillator, or fixed-delay cell whose frequency or delay does not have to change during run time. On the other hand, the latter case is when the TCAB is programmed to a DCO, DPWM, digitally-controlled delay cell, or phase interpolator whose output frequency, duty, delay or phase is controlled by input digital codes in real time. In most cases of mixed-signal systems, the input digital codes of an analog block are either results of digital filters or digital calibrators or received ones from external via I/O. In order to receive the digital codes, three TCABs in the lower left corner of the TCAB array have dedicated signal path as shown earlier in Fig. 2.32. As described in Chapter 3, the digital code words are from the adjacent array of arithmetic logic units (ALUs).

To illustrate how the signals are propagated via the programmable interconnects within the TCAB array, Fig. 2.34 (b) shows a single TCAB and its adjacent connection box are utilized to configure the relaxation oscillator in Fig. 2.34 (a). First, *OUT* and *OUTB* of the TCAB are connected to the right connection box. Then, *IN*[2] and *IN*[3] can be connected to *OUTB* and *OUT*, respectively, via the right connection box. The other input pulse signals *IN*[1:0], [7:4], and W_1[6:0] are not connected to any connection box, being tied to ground by the multiplexers (not shown in the figure, refer Fig. 2.13). Likewise, W_2[6:0], C_{SW1}[6:0], and C_{SW2}[6:0] are connected to the proper constants, which is programmed by users, for the intended operating frequency.

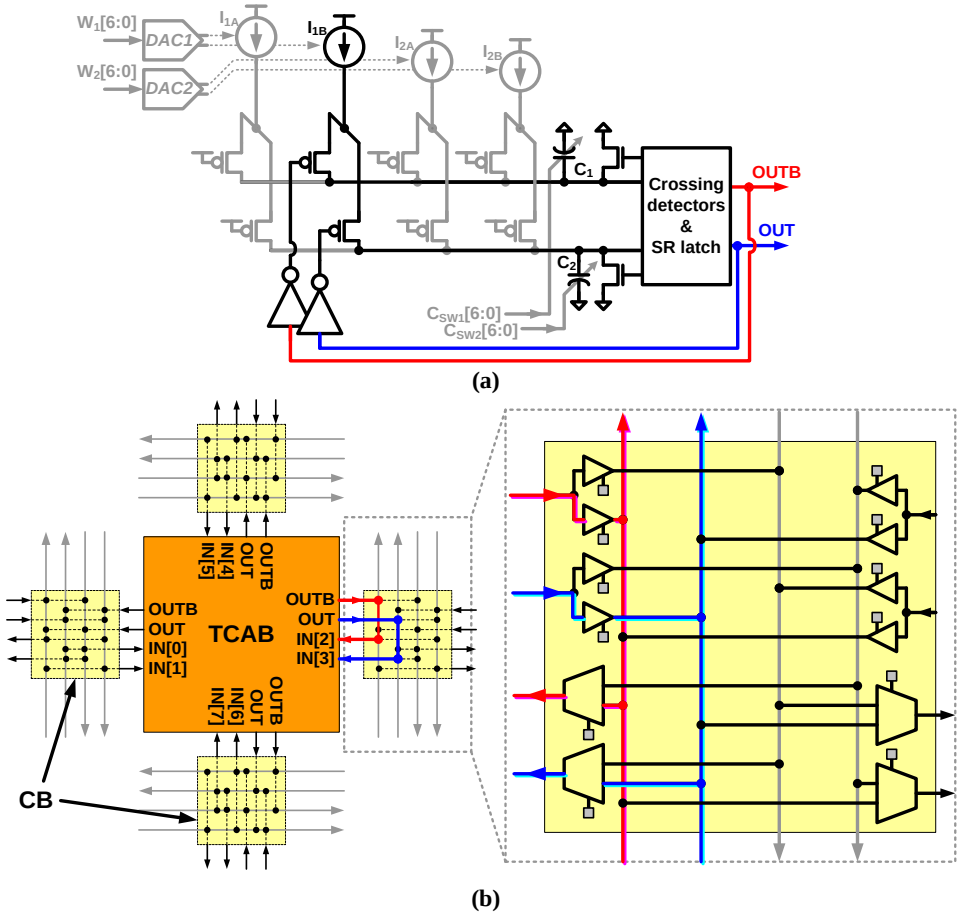


Fig. 2.34 Example of programmable signal path in the TCAB array to configure a single TCAB as the relaxation oscillator.

Fig. 2.35 also illustrates the case when two TCABs and their adjacent connection boxes and switch boxes are utilized to configure a four phase DCO. First *OUT* and *OUTB* of TCAB1 are connected to its upper wire tracks via connection box. Then, the left switch box passes the signals to its left connection box which connects the carried signals to *IN*[4:5] of TCAB2. The leftmost switch box passes *OUT* and

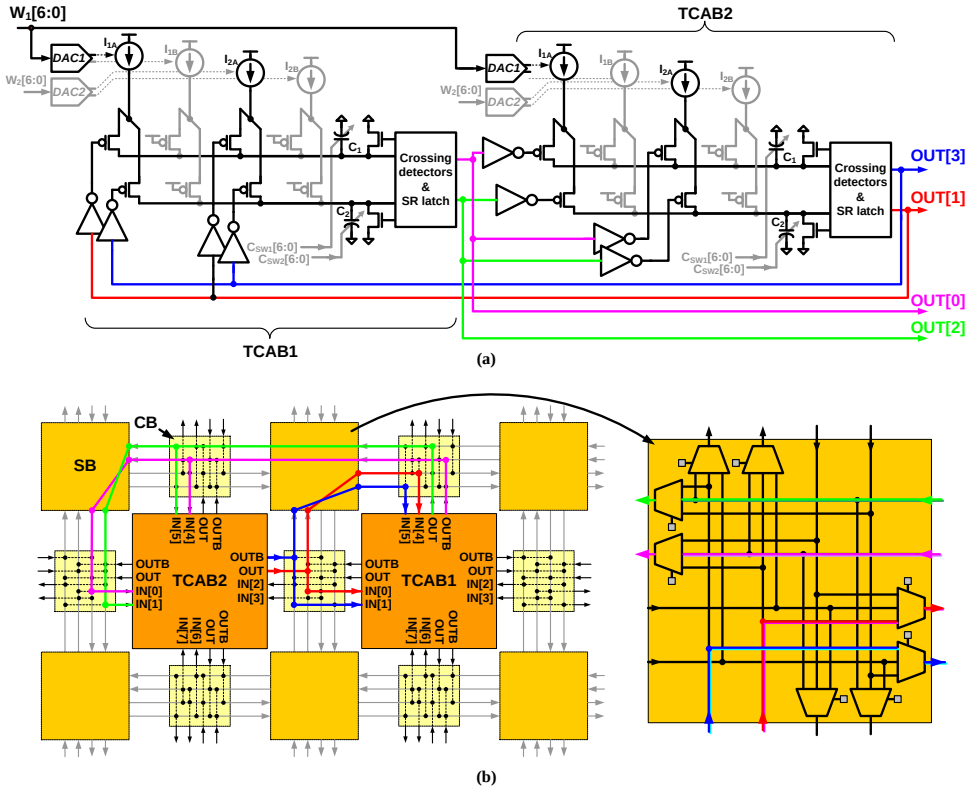


Fig. 2.35 Example of programmable signal path in the TCAB array to configure two TCABs as the four phase DCO.

OUTB of TCAB1 to lower connection box, which is left to TCAB2. Finally, *IN*[0:1] of TCAB2 are also connected. In this manner, *OUT* and *OUTB* of TCAB2 are also connected to *IN*[1][5] and *IN*[0][4] of TCAB1, respectively.

Chapter 3

Proposed Architecture for Field-Programmable Mixed-Signal IC

Before introducing the proposed architecture, the architectural features of various mixed-signal systems are briefly reviewed. Today's integrated systems consist of tightly coupled analog circuits and digital logic blocks. In most cases, the digital blocks are included to perform a variety of adaptation or calibration and closely interact with analog blocks [29]-[31]. Also, as technology scales, digitally-assisted analog design techniques [32]-[35] have been widely used to overcome the difficulties in design of analog circuits (e.g., matching, non-linearity, gate leakage or low supply voltage) by replacing a few analog circuits with digital ones or relaxing non-ideality effect of analog circuits with digital calibration engine. Specifically, it is usual in feedback systems to adopt the topology consisting of analog sensor, digital controller, and analog actuator. For example, digital PLLs are composed of TDC, digital loop filter, and DCO [27], [36]-[38]. This mixed-signal feedback

structure is also utilized when implementing DC-DC converters with ADC, digital loop filter, and DPWM [24], [39]-[41].

In order to program such mixed-signal feedback systems or digitally-assisted analog systems, the proposed IC has the architecture as illustrated in Fig. 3.1 [18].

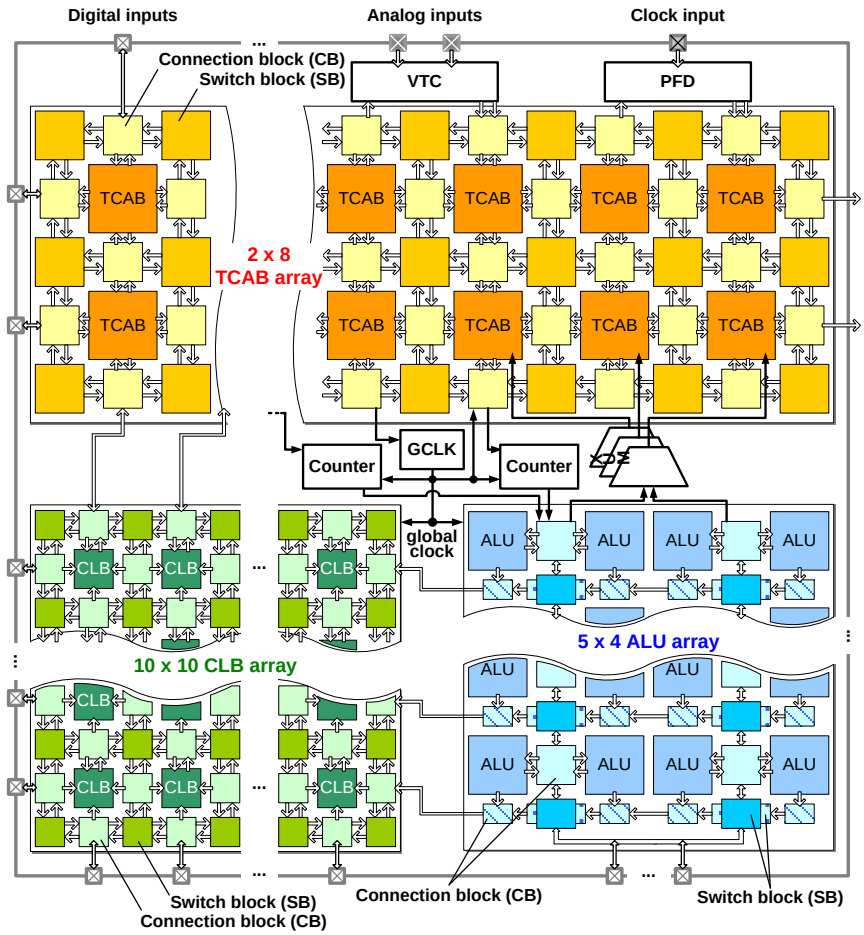


Fig. 3.1. Architecture and floorplan of the proposed field-programmable mixed-signal IC.

The IC largely consists of three arrays of TCABs, configurable logic blocks (CLBs), and programmable arithmetic logic units (ALUs). In each array, the TCABs, CLBs, or ALUs are placed regularly and surrounded by tracks of wires and programmable interconnects (i.e., connection blocks and switch blocks). It also includes gluing blocks such as a voltage-to-time converter block (VTC), phase-frequency detector block (PFD), and counter block to interface among the three arrays or between an array and I/O.

Various analog/mixed-signal feedback systems can be programmed on the proposed IC by mapping their analog sensors and actuators to TCABs and digital controllers to ALUs or CLBs, as shown in Fig. 3.2. That is, users change input-to-output function of each TCAB to perform the function of analog blocks required in the intended system. Then, Boolean logic required in the system is programmed on the array of the CLBs, each of which is basically a programmable look-up table (LUT). Lastly, digital arithmetic logic is programmed on the IC by programming each ALU to perform one of arithmetic operation among addition, subtraction, accumulation, and arithmetic shift. For instance, one can program a digital PLL on the IC by configuring TCABs to operate as TDC and DCO and programming digital loop filter to ALUs. Then, CLBs are programmed to lock detection logic which detects whether the PLL is locked, observing the loop condition. Similarly, it is also possible to configure DC-DC converter on the IC by programming ADC and DPWM on TCABs and mapping digital filter on ALUs.

Likewise, Fig. 3.3 illustrates how the digitally-assisted analog systems can be programmed on the proposed IC, configuring analog function on the TCABs and programming digital calibration engine on the ALUs or CLBs.

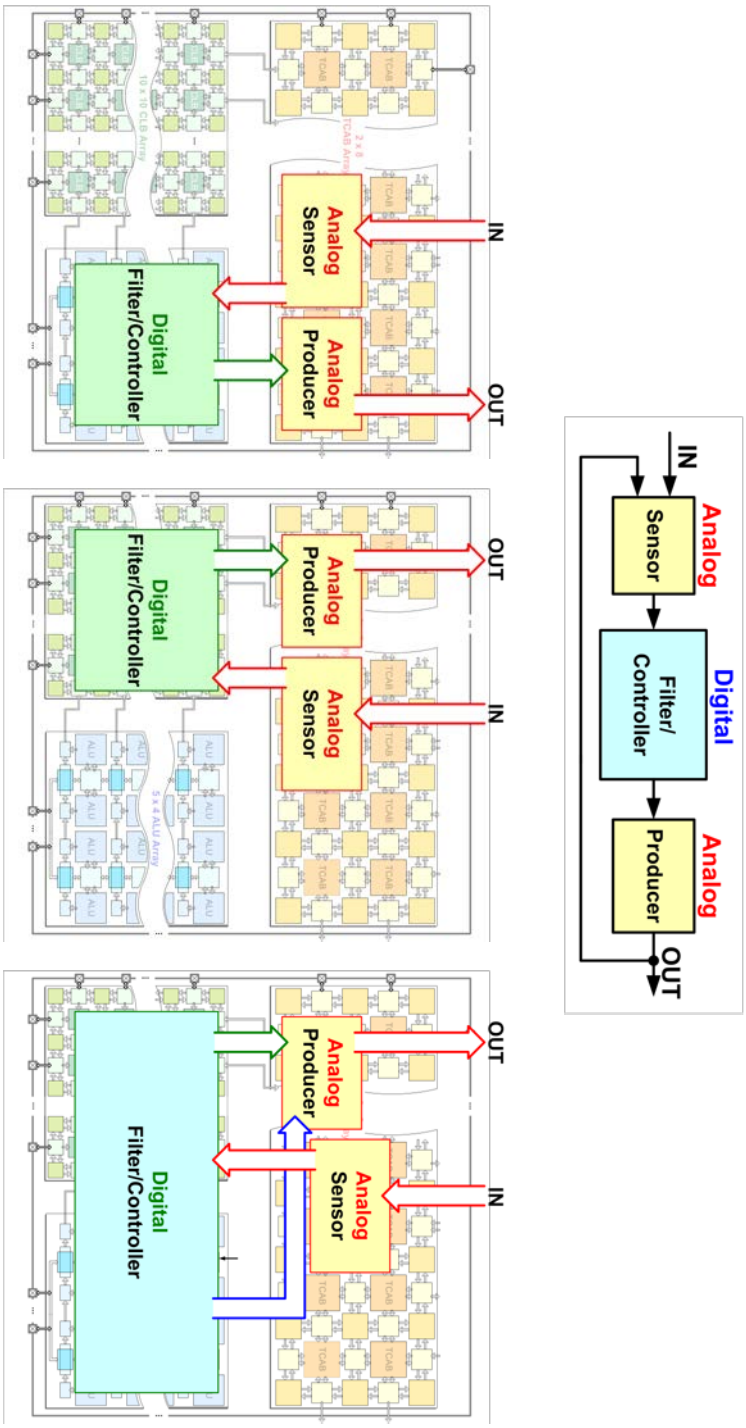


Fig. 3.2 Three types of programming of the mixed-signal feedback systems on the proposed IC.

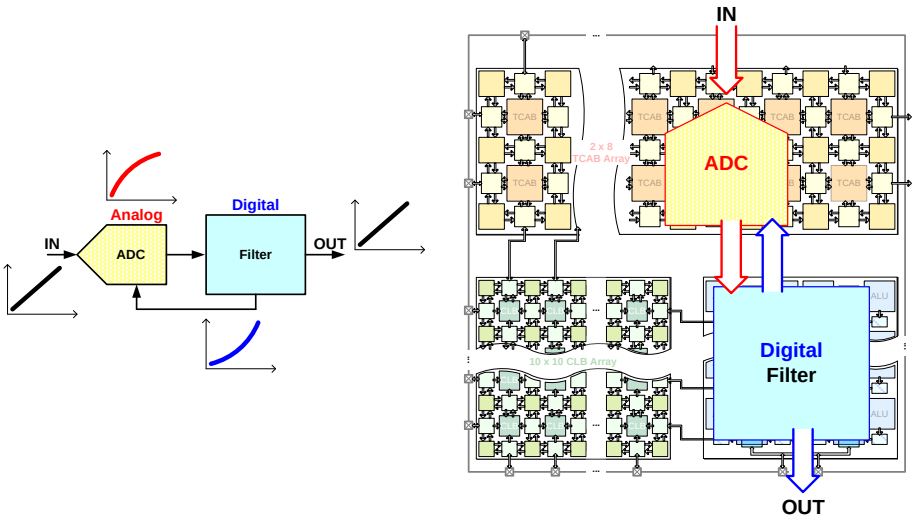


Fig. 3.3 Programming of the digitally-assisted analog systems on the proposed IC.

Chapter 4

Circuit Implementation

In addition to the array of the TCABs for programmable analog function, the proposed field-programmable IC also includes the other two arrays of configurable logic blocks (CLBs) and arithmetic logic units (ALUs) for programmable digital function and interfacing blocks at the boundary of each array of the programmable blocks as described in Chapter 3. Their role and circuit implementation are presented in following subchapters. Lastly, the method to program the whole chip based on scan chain is also presented.

4.1 Configurable Logic Block Array

4.1.1. Configurable Logic Block

In order to program arbitrary digital logics required in the intended mixed-signal systems, the IC contains configurable logic blocks (CLBs) based on look-up table (LUT). Each CLB consists of a programmable LUT whose output is connected to D flip-flop followed by a multiplexer to select the final output of CLB between output of LUT and output of D flip-flop, as shown in Fig. 4.1. The size of the included LUT is determined as 4 inputs and 16 rows, considering the trade-off between area and delay when multiple CLBs compose the array [44]. Therefore, a single CLB is capable of implementing any Boolean logic with 4 inputs depending on how the LUT is programmed. Then, the programmed logic becomes either combinational or sequential according to selection of the multiplexer. For the sequential logic, the

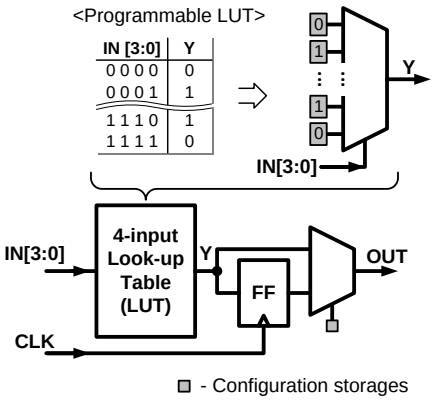


Fig. 4.1 Circuit implementation of the CLB.

CLBs also receive a common triggering clock of D flip-flop which transmitted from GCLK block. The more complex logic with more than 4 inputs is implemented by combining multiple CLBs.

4.1.2. CLB Array

The multiple CLBs (10 x 10) are grouped in the array together with connection blocks and switch blocks, following 2-D island-style like the TCAB array. The overall array composition is illustrated in Fig. 4.2. The only difference between the ALU array and TCAB array is the number of wires in a wire track. That is, the CLB array has 6 wires for each wire track, whereas the TCAB array has 4 for each track. The connection blocks and switch blocks in the CLB array are implemented with digital tri-state inverters like those in the TCAB array. Each CLB receives each digit

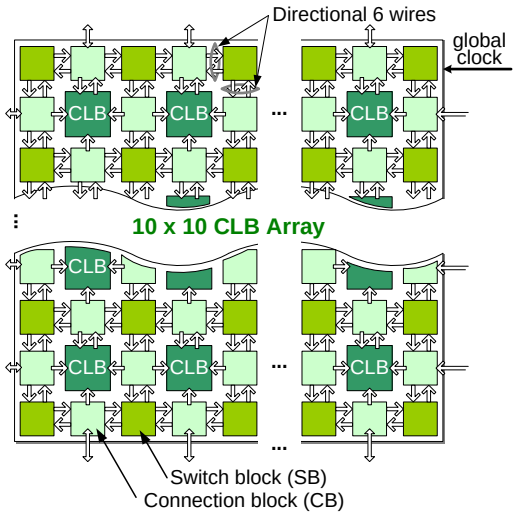


Fig. 4.2 CLB array composition with programmable interconnects.

of 4-bit input from 4-sided adjacent connection blocks and transmits output only to the upper side connection block.

The arbitrary digital logic written in hardware description language (e.g., Verilog) is synthesized and P&R (Place-and-route) onto the CLB array is performed, utilizing an open-source academic software suite, VTR [45]-[47]. Fig. 4.3 shows the visualized results of VTR after it synthesizes and performs P&R of a logic block including 4-bit Gray decoder which is written in Verilog.

```
module dut (
   input clk,
   input rst_n,
   input [3:0] Din,
   output [3:0] Dout,
);
reg  [3:0] Dprev;
wire [3:0] Dcurrent;

assign Dout = Dcurrent ^ Dprev;
always @(posedge clk or negedge rst_n) begin
   if(!rst_n) begin
       Dprev <= 4'b0000;
   end
   else begin
       Dprev <= Dcurrent;
   end
end

gray_decoder dec(.Din(Din), .Dout(Dcurrent));

endmodule

module gray_decoder (
   input [3:0] Din,
   output [3:0] Dout
);
     ……
endmodule
```

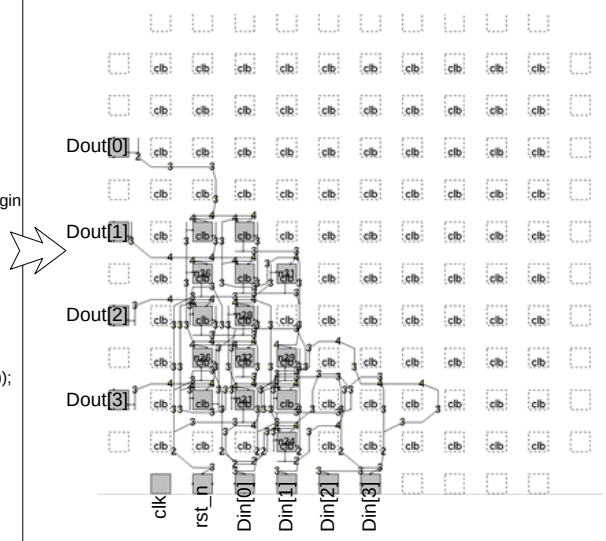


Fig. 4.3 Exemplary VTR results of Verilog module including 4-bit Gray decoder (input: low side ports, output: right side ports).

4.2 Arithmetic Logic Unit Array

In addition to CLBs for programming Boolean logic, the proposed IC also contains programmable arithmetic logic units (ALUs) as additional programmable digital resource. Although the CLB array alone can afford to be programmed to any combinational or sequential logic including arithmetic logic, ALU array is additionally employed to reduce the overhead in area, performance degradation or wasting of CLBs that can occur when performing digital arithmetic operation only with LUT based CLB array. This is a similar strategy of many modern FPGAs that contain specific purpose blocks such as memory, adders, multipliers or DSP blocks [3], [4], [48]. In case of this work, ALU array is in charge of arithmetic such as addition, subtraction, or arithmetic shift. Therefore, digital filters in mixed-signal feedback systems can be programmed onto the ALU array with higher logic density and shorter critical path delay.

4.2.1. Arithmetic Logic Unit

As illustrated in Fig. 4.4, each ALU includes an adder capable both of addition and subtraction, shifter, flip-flop, and five multiplexers, receiving up to two 8-bit operands and producing an 8-bit operation result and flag signals. Arithmetic flags are produced as subsidiary results in every ALU. For instance, the flag bits indicate which one is larger between two operands of the adder or whether those two are same.

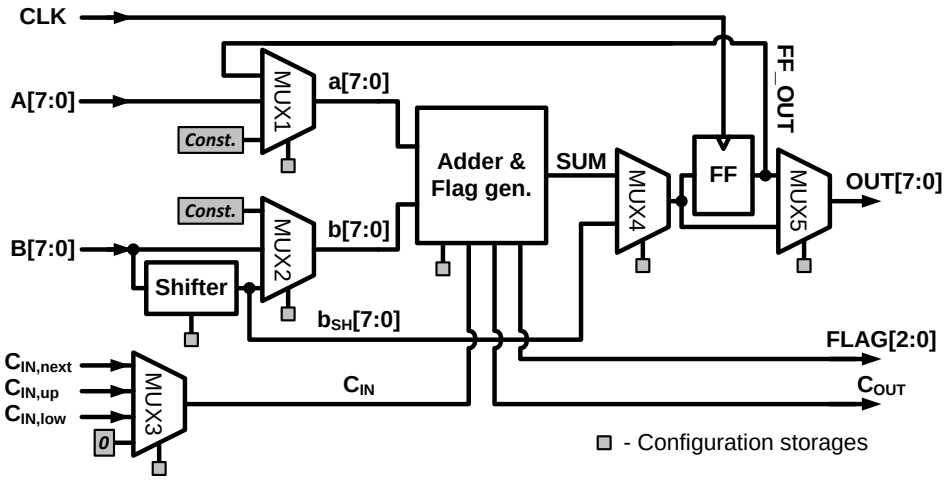


Fig. 4.4 Circuit implementation of the ALU.

It performs arithmetic operations such as addition, subtraction, accumulation, or arithmetic shift depending on how it is programmed. For example, an ALU is configured as an accumulator that accumulates input *B*[7:0] if the included adder is programmed to perform addition and MUX1 through MUX5 are programmed to select *FF_OUT*, *B*[7:0], 0, *SUM*, and the output of MUX4, respectively, as shown in Fig. 4.5. Fig. 4.6 also shows that the ALU is programmed as a arithmetic shifter that shifts *B*[7:0] to the right in amount of 2 bits, extending sign bit. For this configuration, the shifter in the ALU is programmed to perform right-shift and MUX4 and MUX5 are programmed to select b_{SH}[7:0] and the output of MUX4, respectively.

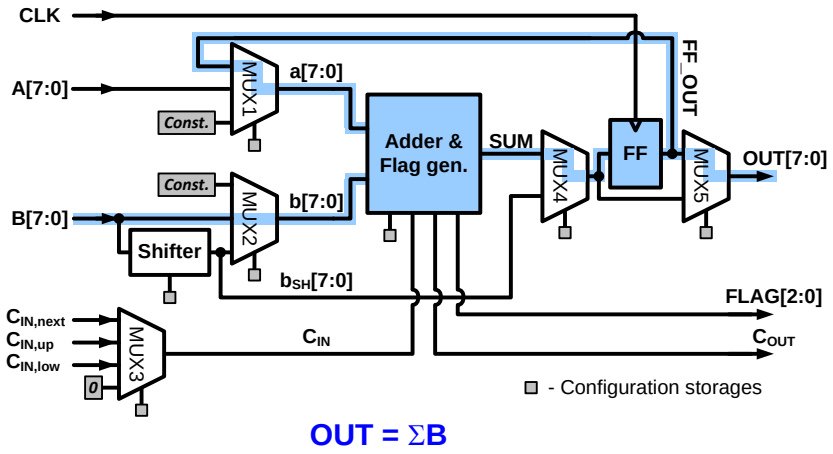


Fig. 4.5 ALU configuration as an accumulator.

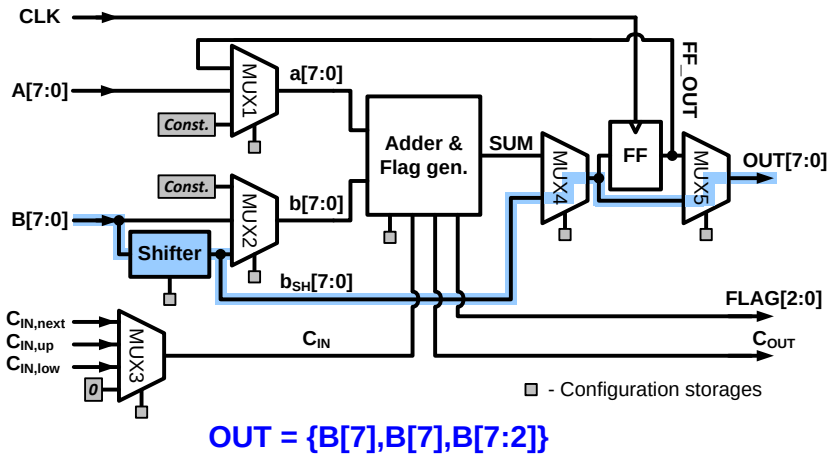


Fig. 4.6 ALU configuration as an arithmetic shifter.

The ALUs are also capable of supporting wider bit-width operands. Adjacent two or three ALUs are extended to 16-bit or 24-bit ALU, exchanging carries each other. In order to facilitate bit-expanded configuration, a single ALU receives carry bits from its upper, lower, or next ALU.

4.2.2. ALU Array

The ALU array is composed of 20 (5 x 4) programmable ALUs and two different sets of programmable interconnects, as illustrated in Fig. 4.7. Whereas the 8-bit operands or results are conveyed through vertical wire tracks, the resulting flags are conveyed through horizontal wire tracks and eventually transferred to CLB array, as shown in Fig. 4.8. Like those in TCAB array or CLB array, connection blocks and switch blocks in the ALU array are implemented with tri-state inverters. Especially, each wire track for operands is bidirectional so that the wire tracks can convey the signals either up or down. The ALU array can receive 8-bit input operands from counter blocks or external and feed its final results into the TCAB array or transmit them to the external.

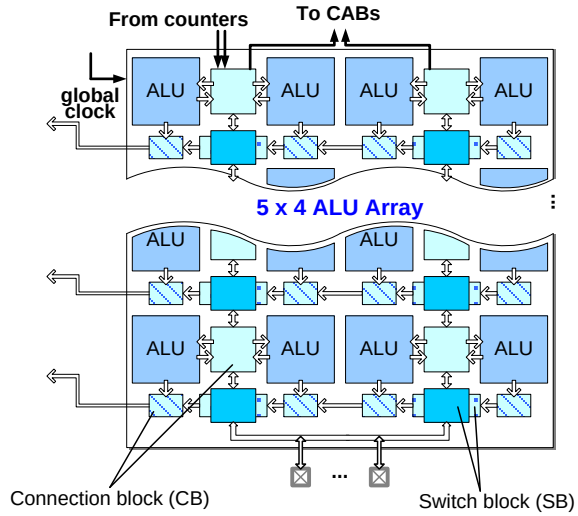


Fig. 4.7 ALU array composition.

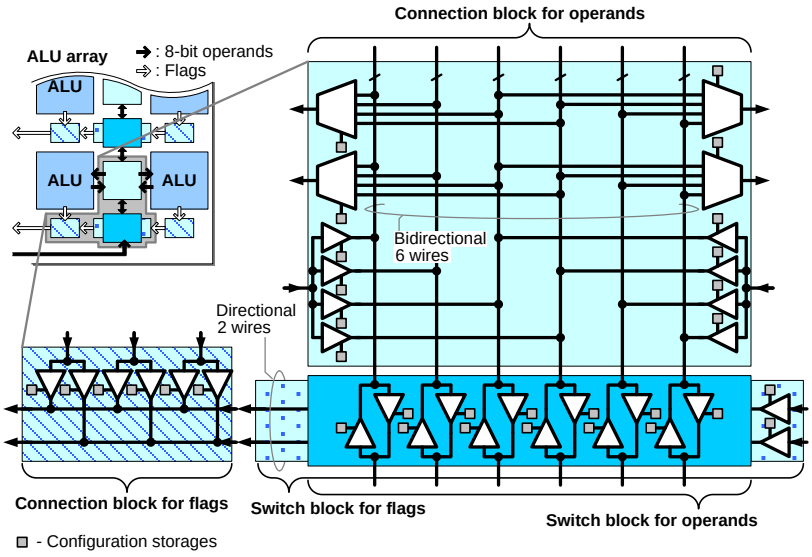


Fig. 4.8 ALU array composition with programmable interconnects.

4.3 Interfacing Blocks

The described three arrays of programmable function blocks (i.e., TCAB array, CLB array, and ALU array) interact with external I/O or with each other at the array boundary through not only direct connections but also gluing blocks, as illustrated earlier in Fig. 3.1. Due to the fact that not only the digital programmable blocks, CLBs and ALUs, but also the analog programmable blocks, TCABs, receive and produce binary digital signals, it is possible to implement IC only with direct connection among the three arrays. However, if the IC only includes the three arrays of configurable units, input signal type of the IC is limited to digital pulse or binary digits which TCABs, CLBs, and ALUs can take as input signal. By employing interfacing blocks that convert external signals to pulse-width modulated signals, the IC can take various external analog signals as input. For example, voltage-to-time converter (VTC) converts voltage magnitude to time-domain pulse-widths and phase frequency detector (PFD) converts clock phase or frequency difference between two inputs to pulse-widths. Similarly, counter block converts time-domain pulse into 8-bit binary digits when signals are transferred from TCAB array to ALU array. Lastly, global clock unit (GCLK) distributes clock with optional frequency division. The remainder of this subchapter describes circuit implementation of VTC, PFD, and counter block. In addition, description of time-to-voltage converter (TVC) is also introduced as an inverse of VTC.

4.3.1. Voltage-to-Time Converter

The VTC which is adopted to take an external voltage as input of the IC is implemented and behaves in similar way of TCAB, as shown in Fig. 4.9. The VTC is composed of a current source, I_S, whose output current is steered by a pair of pMOS, the other two current sources that directly charge following capacitor, reset switches for the capacitors, two pairs of crossing detector and SR latch, and a pulse generator that sets the SR latches. Once *CLK* is asserted, the pulse generator makes short pulse, *SET*, to make both two SR-latch outputs, OUT_P and OUT_N, high and release reset switches beside capacitors. Then, the current sources start charging the capacitors. Particularly, I_S is steered by the difference between the input voltages, V_P and V_N. Therefore, the time which it takes for each output to make falling transition (i.e., pulse-width of output) since the corresponding capacitor starts being charged is given by

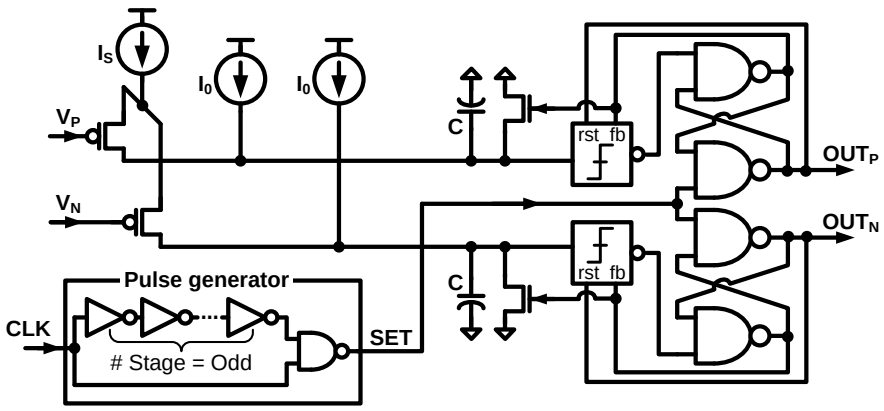


Fig. 4.9 Circuit implementation of the VTC.

$$T_{on,P} = \frac{CV_{th}}{I_0 + I_S + g_m(V_P - V_N)} + t_{xing} + t_{logic},$$
$$T_{on,N} = \frac{CV_{th}}{I_0 + I_S - g_m(V_P - V_N)} + t_{xing} + t_{logic}, \quad (4.3.1)$$

where g_m is transconductance of input transistors, t_{xing} and t_{logic} denote delay of crossing detector and logic gates delay from the SR-latch inputs to OUT_P or OUT_N, respectively. As a result, the voltage difference between V_P and V_N is converted into digital pulses of which pulse-width is a function of $V_P - V_N$.

4.3.2. Phase-Frequency Detector

The other block between external I/O and TCAB array is phase-frequency detector (PFD) that converts phase difference or frequency difference between two clock signals to pulse-width-modulated signals. As shown in Fig. 4.10, the PFD includes two sub-blocks and a multiplexer to select the final output between outputs of those two blocks. The block consisting of two pulse generators and an SR-latch can compare only phase difference between two inputs which have same frequency. The pulse-width difference between two outputs of this block indicates phase

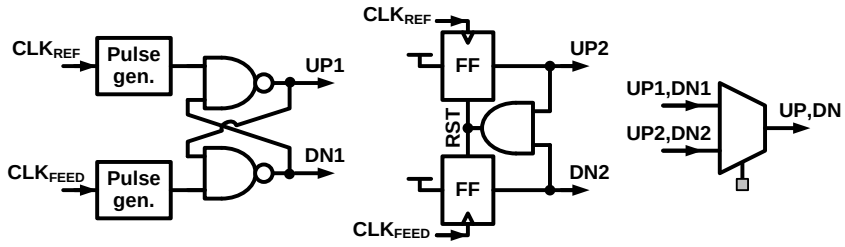


Fig. 4.10 Circuit implementation of the PFD.

difference between the two inputs. For example, if CLK_{REF} leads the inverse of CLK_{FEED} more than 180 degree, pulse-width of UP_1 is longer than that of DN_1 and vice versa. When CLK_{REF} and CLK_{FEED} have equal phase, the block generates two output pulses, UP_1 and DN_1, with identical pulse-width and 50% duty-cycle. The other which is composed of two resettable flip-flops can compare both phase and frequency difference between the two inputs. For example, if frequency of the CLK_{REF} is faster than that of CLK_{FEED} or CLK_{REF} leads CLK_{FEED}, pulse-width of UP_2 is longer than that of DN_2 and vice versa. If the two inputs have same frequency and phase, the block generates identical output pulses on UP_2 and DN_2 with the very short pulse corresponding the reset path delay of the flip-flops (i.e., sum of CK-q delay of the flip-flop, and logic delay, reset-q delay of the flip-flop). In this way, the phase or frequency difference of the two inputs is converted to two time-domain digital pulses.

4.3.3. Counter Block

Digital counter blocks are employed to interface TCAB array and ALU array. Although input and output of both TCAB and ALU are binary, the way they represent the information is different. Whereas TCAB encodes information into time-domain quantity of pulse, ALU presents it with 8-bit binary numbers. Therefore, in order to pass the information from TCAB to ALU, translation of time-domain information into binary number is performed by the counters. Basically, it counts the number of edge transition in output pulse of a TCAB into an 8-bit binary digital number and delivers the binary number to the ALU array. As shown in Fig. 4.11, the

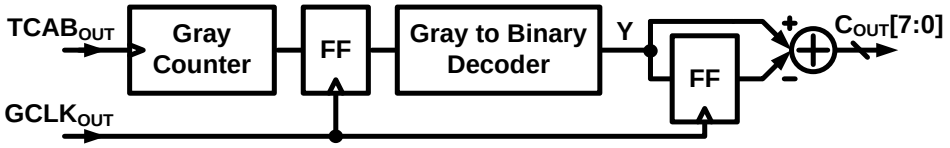


Fig. 4.11 Circuit implementation of the counter block.

counter block receives two pulse signals, $TCAB_{OUT}$ and $GCLK_{OUT}$. At every rising edge of the received $TCAB_{OUT}$, the Gray counter [49] increases its output. Then, the result is sampled by the following flip-flop of which triggering clock is $GCLK_{OUT}$. Instead of binary counter, the Gray counter is adopted to minimize the hazard of sampling wrong bit stream that frequently occurs if $GCLK_{OUT}$ is asserted while counter output is in transition. After being decoded into binary number, the current counted number, $C_{OUT}[7:0]$, is computed by subtracting the previous sampled number from the current one (i.e., $C_{OUT} = Y[n] - Y[n-1]$, where $Y[n]$ denotes Y which is sampled at n-th timestep). As a result, counter block is capable of representing how fast pulse the TCAB generates.

4.3.4. Time-to-Voltage Converter

Although the proposed architecture in Fig. 3.1 does not include a time-to-digital (TVC), as an inverse of the voltage-to-time converter, which can generate analog voltage output of the IC from pulse modulated signals of the TCAB array, one can

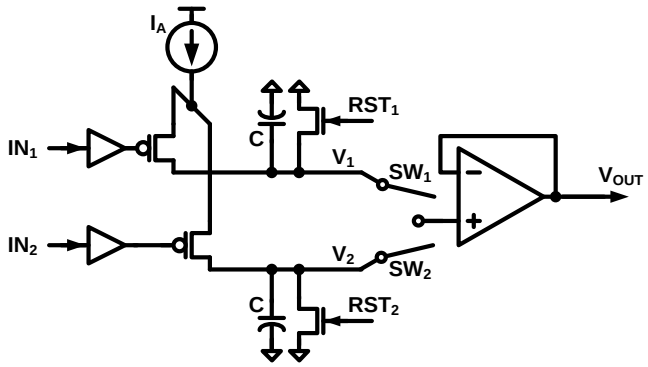


Fig. 4.12 Circuit implementation of the TVC.

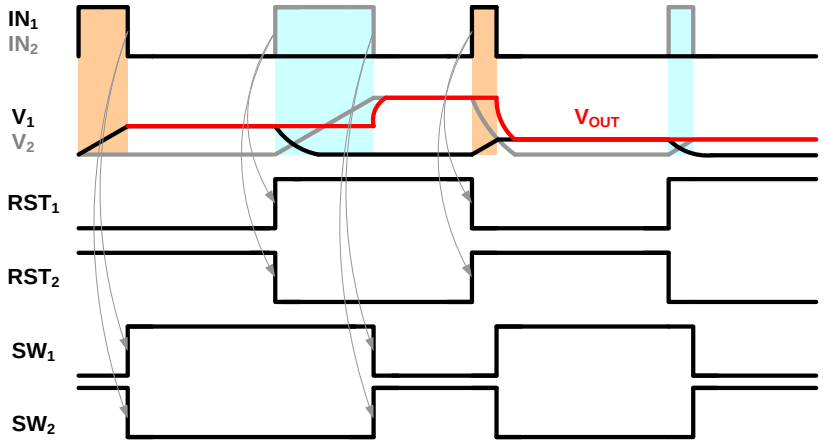


Fig. 4.13 Timing diagram of the TVC.

simply implement the TVC as shown in Fig. 4.12. Its operating timing diagram is given in Fig. 4.13. Like VTC, it is also implemented and behaves in similar way of TCAB. The notable difference is that it additionally include unit-gain amplifier and switches to select the input signal of the amplifier.

Basically, it receives two pulse inputs, IN_1 and IN_2, to generate a single analog voltage output V_{OUT}. Internally, it generates RST_1, RST_2, SW_1, and SW_2 in order to control the switches inside it. It is assumed that the two input pulses are maintained high simultaneously. The capacitors in the TVC are charged only when IN_1 and IN_2 are high, respectively. Then, the internal nodes, V_1 and V_2, finally reach the voltage proportional to on-time of IN_1 and IN_2, respectively, when IN_1 and IN_2 toggle low. By selecting between V_1 and V_2, the TVC can produce analog voltage whose amplitude is proportional to the input pulses.

4.4 Program Method

In the proposed IC, scan chain is adopted in order to program the whole chip. Specifically, the included scan chain is a series of the two phase latch as shown in Fig. 4.14 (a) and series composition of the blocks is illustrated in Fig. 4.14 (b). Considering that more than ten thousands of the latches are included and placed on all over the whole chip, the two phase latch instead of D flip-flop is adopted as a base block to always ensure the timing margin when programming. Each latch

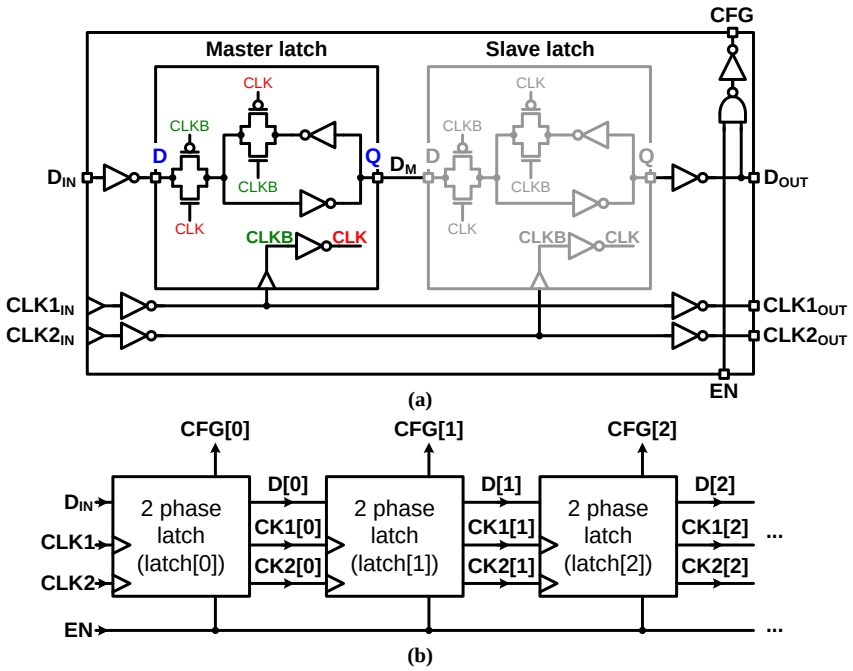


Fig. 4.14. (a) Implementation of 2 phase latch including buffers and logic for enable option and (b) scan chain based on the 2 phase latches.

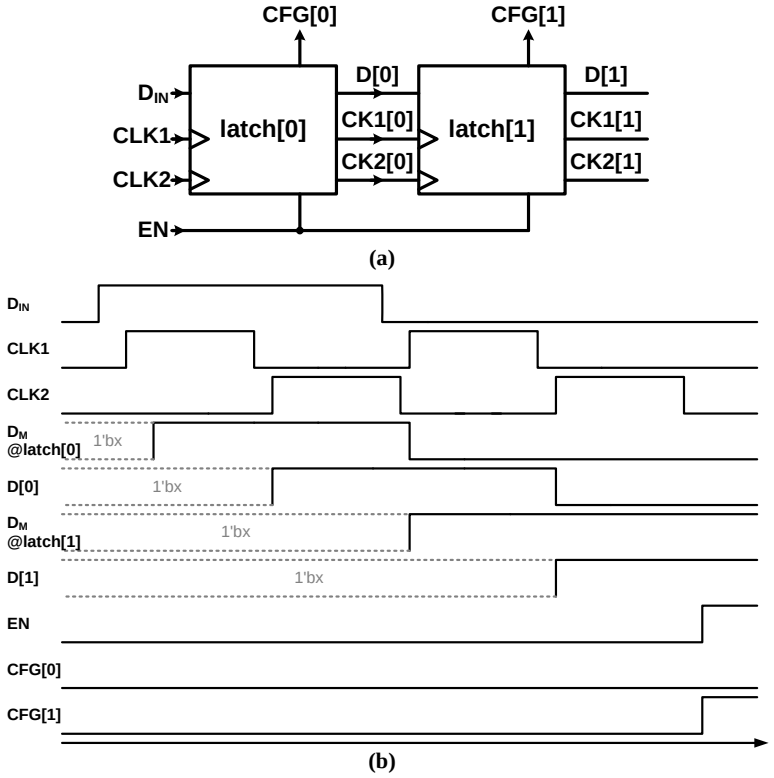


Fig. 4.15. (a) An example scan chain with two latches and (b) timing diagram for its operation.

receives data input and two phase clock signals and transfers the stored data and buffered clock signals to the next stage latch.

Once *EN* is asserted after the whole bit sequence of the programming code is saved on each latch, the final stored data, *CFG*, is connected to the each programmable bit of the programmable function blocks and programmable inter connects. The programming sequence is illustrated with timing diagram in Fig. 4.15 (b), assuming the chip requires 2-bit program code. In the proposed IC, 12,626

latches are included to program and store the configuration bits, 2,195 bits for TCAB array, 1,150 bits for ALU array, 9,240 bits for CLB array, and the rest for the other blocks.

Chapter 5

Mixed-Signal Examples and Experimental Results

The prototype IC is fabricated in a 65-nm LP CMOS technology and operates with a 1.2-V supply. Its chip photograph is shown in Fig. 5.1 and its characteristic summary is given in Table. 5.1. The chip occupies 2.411 mm^2, including the scan-chain flip-flops storing a total of 12,626 configuration bits. Table. 5.2 presents comparison of prior field-programmable analog/mixed-signal ICs architectures in [6], [8], [9], [10], [11], and [12].

The programmability of the TCAB is first demonstrated by configuring the IC as DCO, DPWM, and gated oscillator and measuring their characteristics. Then, the versatile programmability of the IC is demonstrated by configuring the IC as three representative mixed-signal systems, a PLL, ADC, and DC-to-DC converter, and measuring their characteristics. The remainder of this chapter presents more detail

on the configuration and measurement results of TCABs and the three mixed-signal feedback systems.

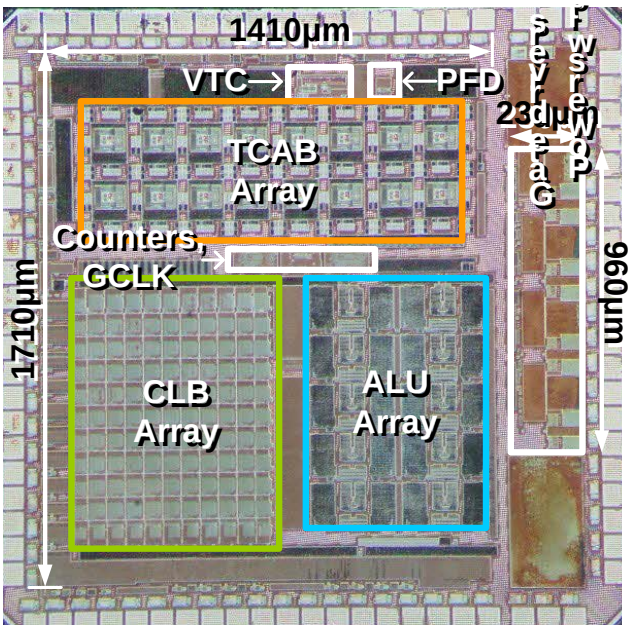


Fig. 5.1 Chip micrograph (active layers only).

Table. 5.1. Characteristic summary of the prototype IC

Process	CMOS 65 nm LP 1P9M
Supply	1.2 V
Area	1.41 x 1.71=2.411 mm^2 TCAB array (0.534 mm^2) CLB array (0.523 mm^2) ALU array (0.454 mm^2)
Analog Function Block	TCAB
Digital Function Block	LUT based CLBs, Programmable ALUs

Table. 5.2. Comparison of prior field-programmable analog/mixed- signal ICs architectures

	This work	**JSSC 03' [8]**	**ISSCC 08' [6]**	**JSSC 10' [9]**	**JSSC 11' [11]**	**TVLSI 13' [10]**	**TCAS-1 16' [12]**
Process	65 nm	N/A	130 nm	350 nm	65 nm	350 nm	65 nm
Type	Mixed-signal system	Mixed-signal system	Analog system	Analog system	Analog system	Mixed-signal system	Analog system
Area	2.41 mm^2	N/A	1 mm^2	9 mm^2	0.31 mm^2	N/A	3.46 mm^2
Supply	1.2 V	3.3 V	1.2 V	2.4 V	1 V	2.4 V	1.2 V
Presented examples	PLL, ADC, DC-DC converter	A part of 300-baud modem	Analog filters	AM receiver, analog speech processor	Pipeline ADC, low pass filter	ADCs	biasing cir-cuits, analog filters
Programmable analog function block	TCAB	X	X	X	X	X	X
Selectable analog block	TCAB	Tunable amplifier	Tunable G_m cell	Multiplier, transconductor, transistor, C	Zero crossing detector	Multiplier, transconductor, transistor, C	Programmable transistor, R, C
Programmable routing	O	△ (Limited)	X	△ (Limited)	X	△ (Limited)	△ (Limited)
A2D conversion	8 bit	1 bit	-	-	-	1 bit	-
D2A conversion	7 bit	1 bit	-	-	-	1 bit	-

5.1 Measurement Results of TCAB

5.1.1. Digital Pulse-Width Modulator

In order to test the proposed TCAB as a DPWM described in Chapter 2.3.3, the prototype IC is programmed as shown in Fig. 5.2. Then, the IC can receive an external digital input code, *Dctrl*[6:0], transfer it to a TCAB which is programmed as DPWM, and transmit output of the TCAB to the external. Fig. 5.3 shows equipment setup to program and test the IC. Users write program code of TCABs, ALUs, CLBs, and interconnects with PC. Then, the program code is converted to electrical signal for the IC by USB I/O device and the IC operates according to users' program code.

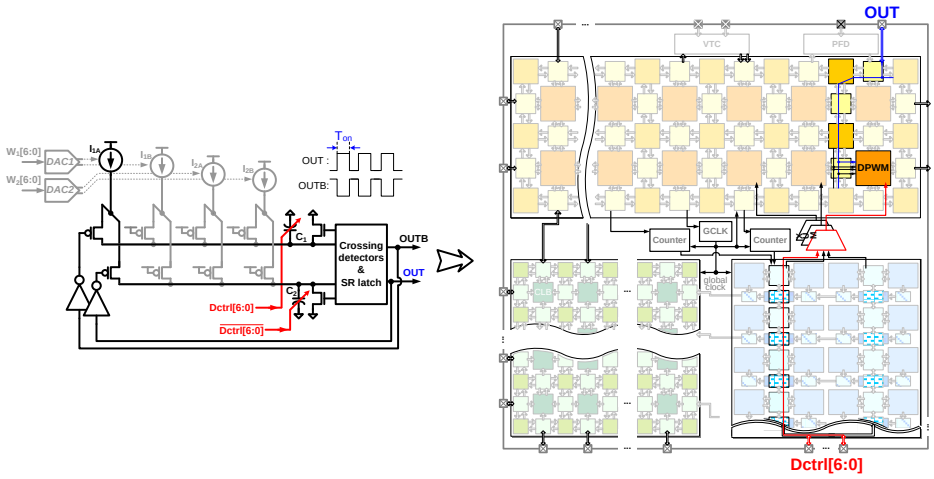


Fig. 5.2 Placement and routing in the prototype IC to test a TCAB as DPWM.

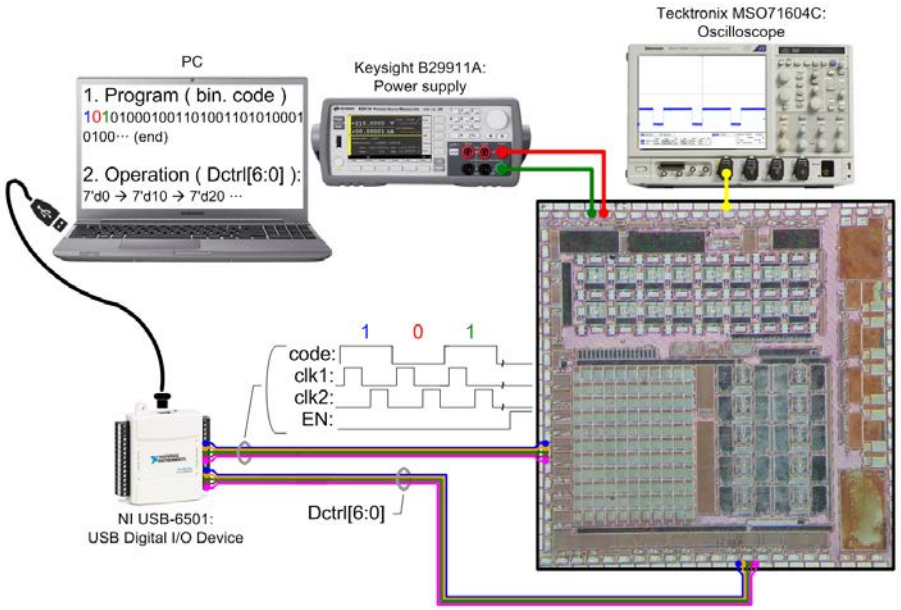


Fig. 5.3 Experiment setup to program and test the IC.

Fig. 5.4 shows the measured waveform when the IC is programmed as 1.6 MHz DPWM and 25.3 MHz DPWM. One can change the frequency of output pulse by programming the DAC in the TCAB, which controls output current of I_{1A}, with different code. As described in Eq. (2.3.13), the period of output pulse depends on the charging current level. Fig. 5.5 shows the plot of digital input code to duty cycle of output pulse of the two DPWMs. They covers same range of duty cycle, producing different frequency output.

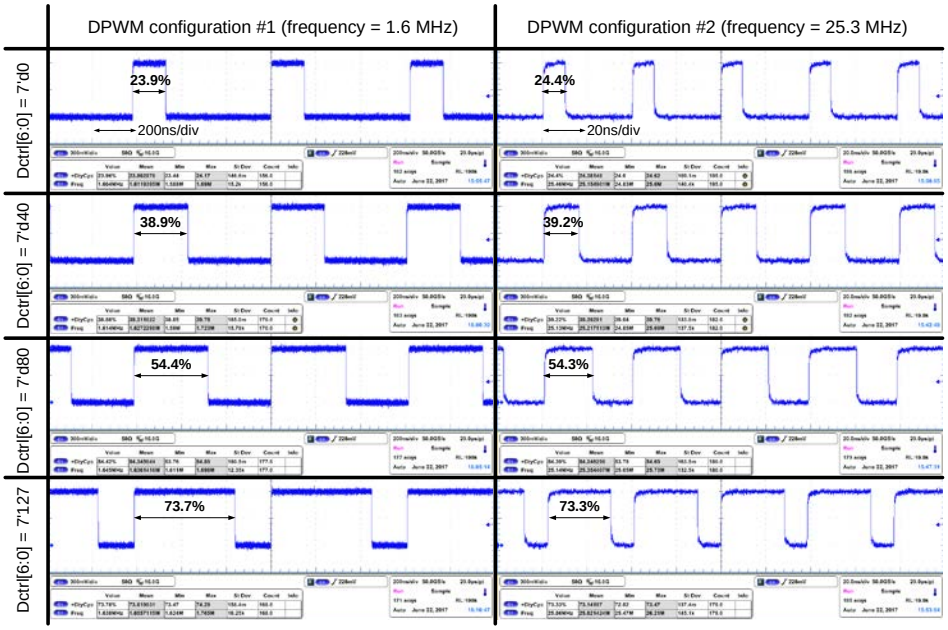


Fig. 5.4 Measured waveforms when the IC operates as DPWM producing 1.6 MHz and 25.3 MHz output.

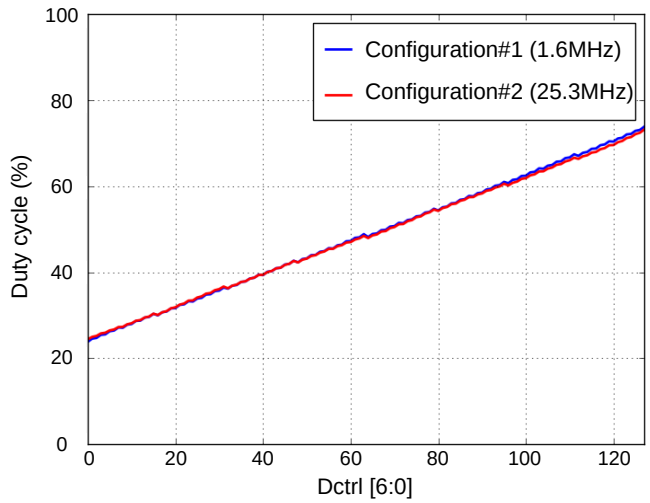


Fig. 5.5 Measured transfer function of digital input code to duty cycle of output pulse.

5.1.2. Digitally-Controlled Oscillator

Among the program code for the DPWM in Chapter 5.1.1, the part related TCAB function and connection block around the TCAB is modified to configure the TCAB as DCO in Chapter 2.3.2 and the prototype IC is programmed as shown in Fig. 5.6. Then, output pulse frequency is adjusted by the external digital input code. As expressed in Eq. (2.3.6), the TCAB can operate as different DCO with different frequency tuning range by programming. Fig. 5.7 shows the measured transfer function of input digital code to output frequency of the six different DCO configuration. Fig. 5.8 shows the measured phase noise when the programmed DCO produces 1.002 GHz output clock. Its phase noise at 10 MHz offset is −109.8 dBc/Hz.

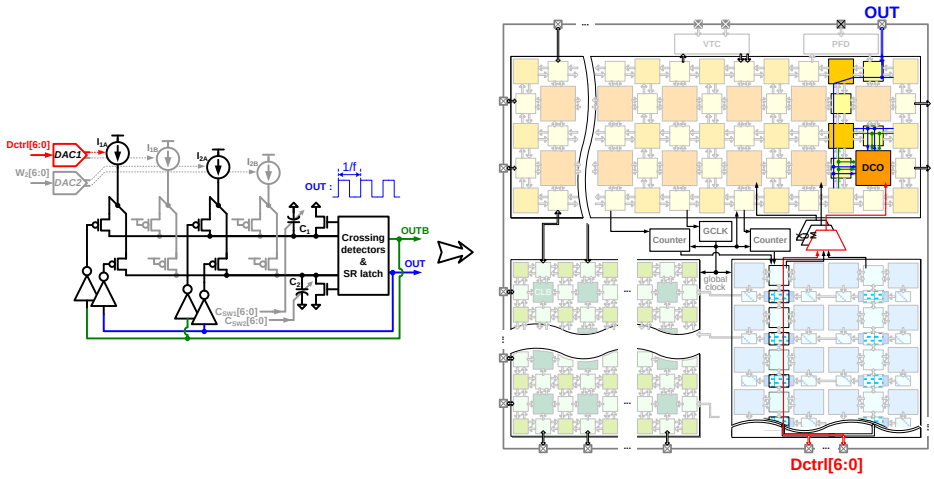


Fig. 5.6 Placement and routing in the prototype IC to test a TCAB as DCO.

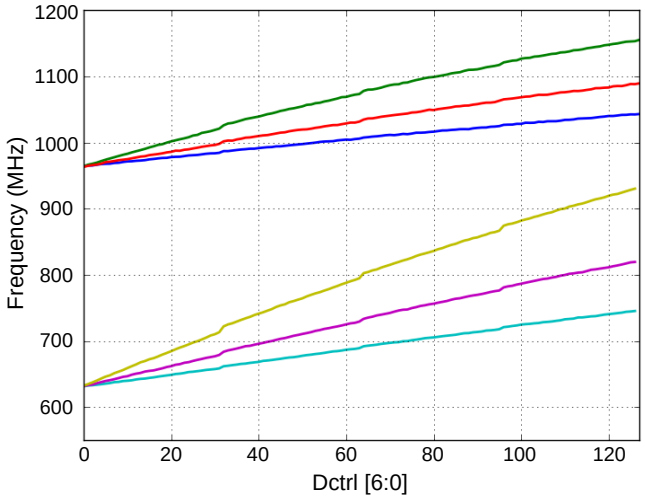


Fig. 5.7 Measured transfer function of digital input cod e to frequency of output pulse.

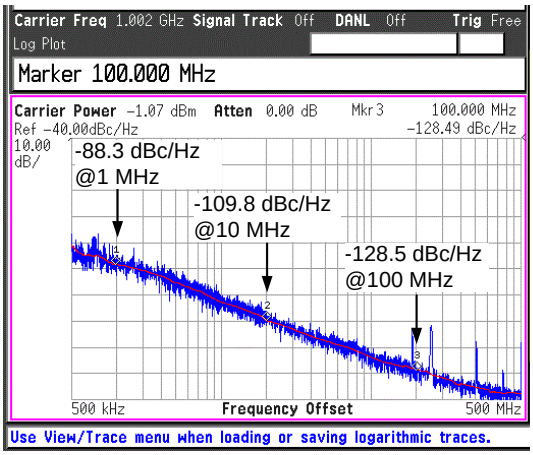


Fig. 5.8 Measured phase noise of the programmed DCO when its output frequency is 1.002 GHz.

5.1.3. Gated Oscillator

Next, In order to test the proposed TCAB as a gated oscillator described in Chapter 2.3.4, the prototype IC is programmed as shown in Fig. 5.9. Fig. 5.10 shows the measured waveform when the IC is programmed as different gated oscillator with different output frequency, receiving pulse input. One can change the oscillating frequency by re-programming C_{SW1}, C_{SW2}, W_1, and W_2 in the TCAB with different value.

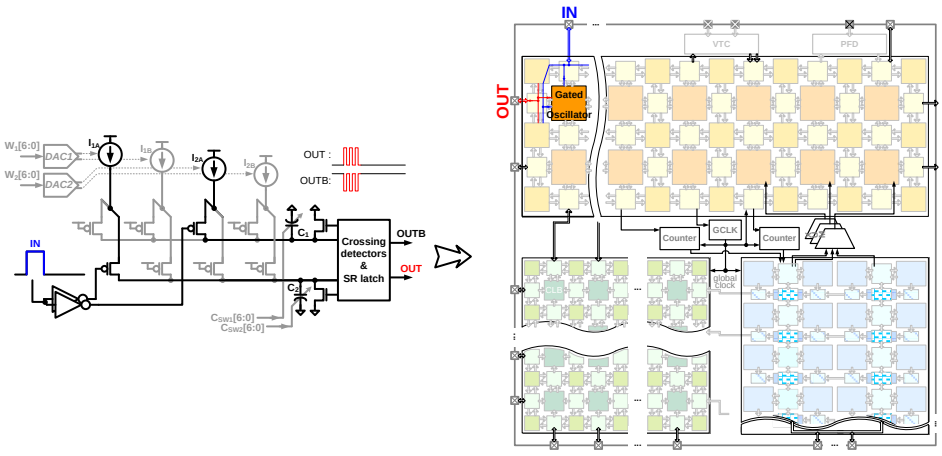


Fig. 5.9 Placement and routing in the prototype IC to test a TCAB as gated oscillator.

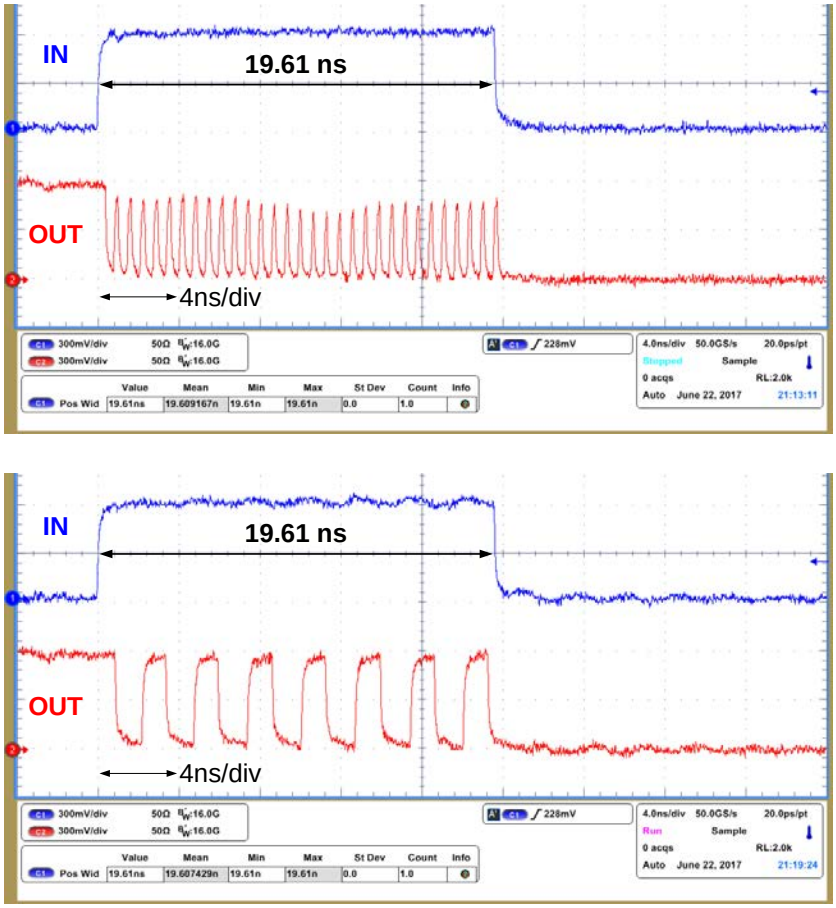


Fig. 5.10 Measured waveform of the input and output when the IC operates as gated oscillator.

5.2 Digital Phase-Locked Loop

Fig. 5.11 illustrates the block diagram of a 1-GHz PLL with x 8 multiplication and Fig. 5.12 shows how it is programmed on the proposed IC. First, one of the gluing blocks, PFD, converts the timing error between input reference clock and divided clock to two pulse-widths. To quantize the two pulses, two pairs of TDC each of which consists of a TCAB programmed as gated oscillator and a counter as described in Chapter 2.3.4 are configured. The following digital loop filter consisting of a proportional path and integral path (i.e., PI compensator) [50] is mapped to ALUs in order to compensate the timing error. Then, DCO is realized with a single TCAB as described in Chapter 2.3.2 and adjusts its output frequency according to the digital input code received from the preceded filter. GCLK block is also used for dividing DCO clock and distributing the divided clock. Besides the feedback loop, lock detector logic which indicates whether the PLL is in lock-condition is programmed to ALUs and CLBs.

The measured phase noise characteristics of the IC as the described PLL are

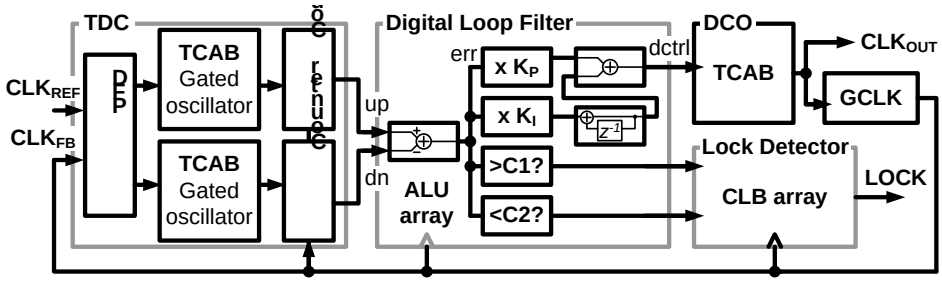


Fig. 5.11 The chip configuration as a 1-GHz digital PLL.

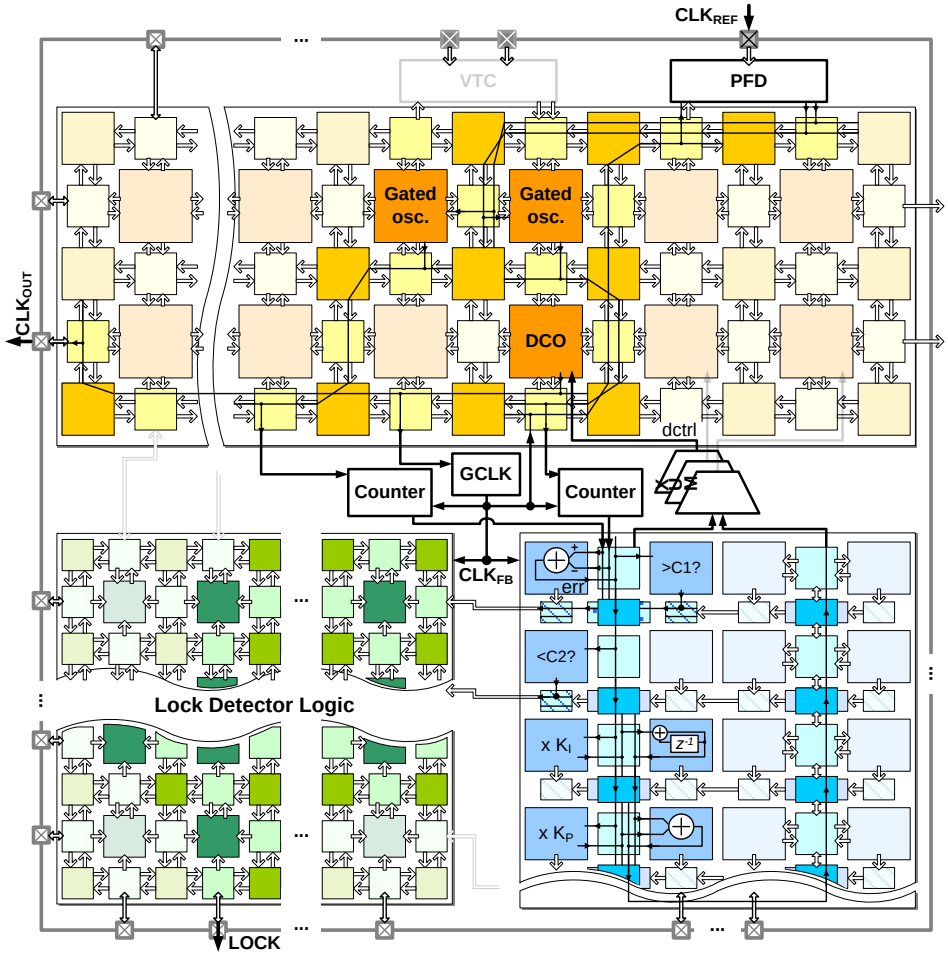


Fig. 5.12 Exemplary placement and routing of the digital PLL.

shown in Fig. 5.13. The TCAB programmed as DCO operates over frequency range from 0.98 GHz to 1.08 GHz with an average resolution of 0.78 MHz/bit. The programmed PLL successfully synthesizes a 1-GHz clock from a 125-MHz reference clock input. Its measured integrated jitter is 12.3 ps_{rms} and phase noise is −102.91 dBc/Hz at 10 MHz offset, while dissipating 33.6 mW. Also, the measured

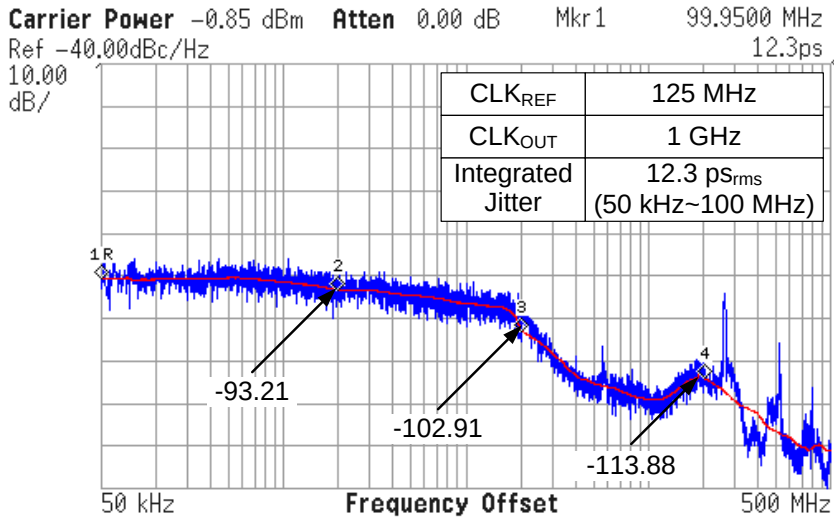
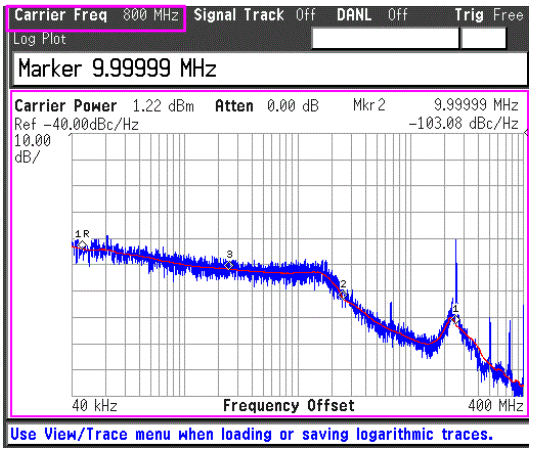


Fig. 5.13 The measured phase noise of the programmed digital PLL.

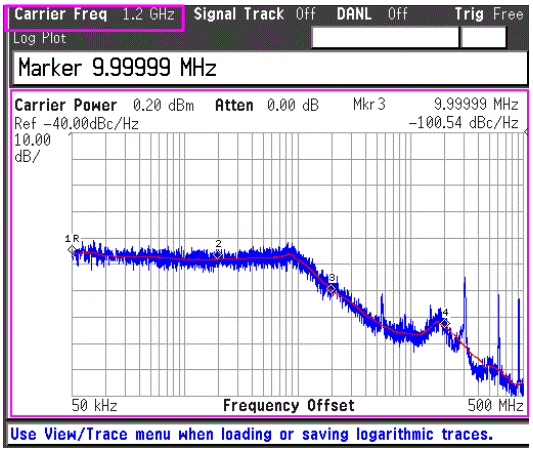
waveforms of CLK_{REF}, CLK_{OUT}, and *LOCK* during initial locking transient are shown in Fig. 5.14.

Fig. 5.14 The measured voltage waveforms during initial locking transient of the programmed digital PLL.

It is also possible to reconfigure the IC to operate different digital PLL with different output frequency range. In fact, the digital PLL in Fig. 5.11 is capable of generating clock whose frequency range spans from 0.98 GHz to 1.08 GHz. If the included DCO is re-programmed to operate to generate clock with different



(a)



(b)

Fig. 5.15 The measured phase noise of the programmed digital PLL when the included DCO is programmed to cover operating frequency of (a) 800 MHz (b) 1.2 GHz.

frequency range, the PLL can receive a reference clock with different frequency and produce output clock with different frequency. Fig. 5.15 shows the digital PLL is re-programmed to generate output frequency of 800 MHz and 1.2GHz, receiving 100 MHz and 150 MHz reference clock, respectively.

5.3 Analog-to-Digital Converter

Fig. 5.16 illustrates block diagram of a 7-bit, 50-MS/s ADC and Fig. 5.17 shows how it is programmed on the proposed IC. The programmed ADC basically has time-domain architecture. First, the VTC converts the differential voltage between V_P and V_N to two pulses, T_P and T_N. Then, pulse-widths of the two are quantized by the following TDCs each of which consists of a TCAB programmed as gated oscillator and a counter. Each gated oscillator oscillates only when T_P or T_N is high and its oscillating frequency is controlled by adjusting capacitance in the TCAB depending on the received digital code, 64+D[6:0] or 64−D[6:0]. The feedback controller programmed on the ALU array compares the two counter outputs and adjusts the capacitances in the gated oscillator TCABs with complementary digital codes 64+D[6:0] and 64−D[6:0] until the counter outputs are equal. The resulting D is then a digitized version of V_P−V_N and is determined as zero if V_P and V_N are equal.

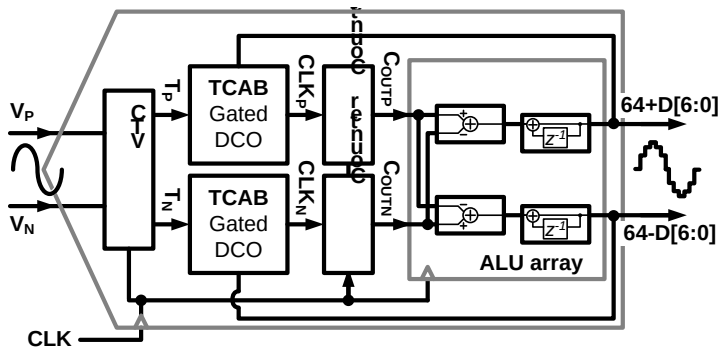


Fig. 5.16 The chip configuration as a 50 MS/s ADC.

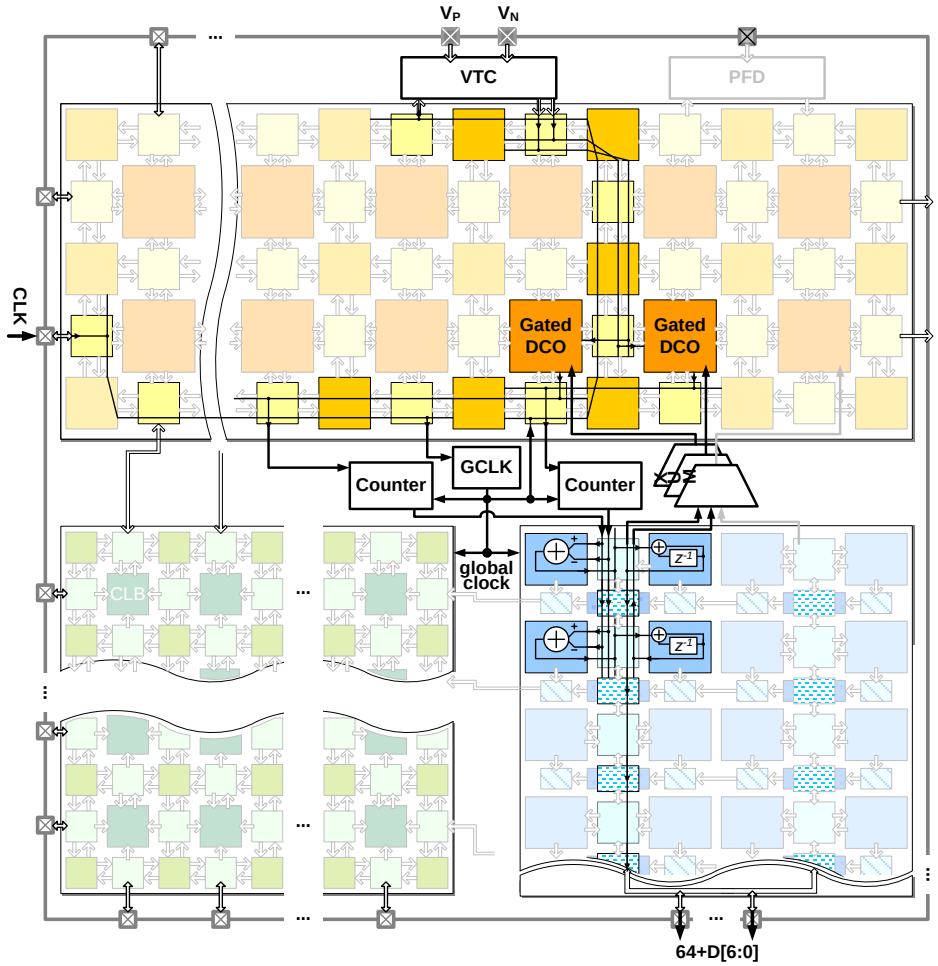


Fig. 5.17 Exemplary placement and routing of the ADC.

The detailed principle of how the output D quantizes $V_P - V_N$ is given as follows. As described earlier in Chapter 4.3.1, the VTC generates two pulses, T_P and T_N, and their on-time, $T_{on,P}$ and $T_{on,N}$, are given by Eq. (4.3.1), as a function of input voltage difference. Then, the following gated oscillators are activated with the oscillating period of $T_{period,P}$ and $T_{period,P}$, while each received pulse, T_P or T_N is high. The

number of edge transitions in each oscillator output is recorded at counters. The two counter outputs of every sample, C_{OUTP} and C_{OUTN}, are $T_{on,P}/T_{period,P}$ and $T_{on,N}/T_{period,N}$, respectively. Receiving the two digital values, the feedback controller tries to make C_{OUTP} and C_{OUTN} equal by adjusting the oscillating period of gated oscillator in each TDC. If it is assumed that t_{xing}, t_{logic} and t_{reset} in TCAB and VTC are relatively small, the condition to satisfy the described relationship is given by

$$\begin{aligned} C_{OUTP} &= C_{OUTN} \\ \frac{T_{on,P}}{T_{period,P}} &= \frac{T_{on,N}}{T_{period,N}} \\ \frac{\dfrac{CV_{th}}{I_0 + I_s - g_m\Delta V}}{\dfrac{\left(C_0 + (64+D)C_{step}\right)V_{th}}{I_{1A}}} &= \frac{\dfrac{CV_{th}}{I_0 + I_s + g_m\Delta V}}{\dfrac{\left(C_0 + (64-D)C_{step}\right)V_{th}}{I_{1A}}} \\ \frac{C_0 + (64-D)C_{step}}{I_0 + I_s - g_m\Delta V} &= \frac{C_0 + (64+D)C_{step}}{I_0 + I_s + g_m\Delta V}. \end{aligned} \tag{5.3.1}$$

Therefore, a solution of Eq. (5.3.1) is determined so that D is proportional to $V_P - V_N$.

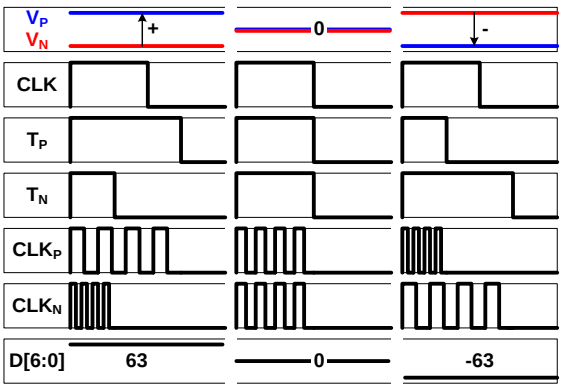


Fig. 5.18 Operating principle of the programmed ADC.

The described operating principle is illustrated with the conceptual timing diagram in Fig. 5.18 where relative pulse-width or frequency difference is shown.

The characteristics of the proposed IC as the described ADC was measured. Fig. 5.19 shows the dynamic performance of the programmed ADC at 50 MS/s with 100-kHz sinusoidal input. The programmed ADC achieves an SNDR of 32.5 dB and ENOB of 5.11, while dissipating 10.8 mW. Fig. 5.20 also shows the static performance of the ADC. The measured INL and DNL are in the ranges from −2.04 to 0.84 LSB and from −0.59 to 1.03 LSB, respectively.

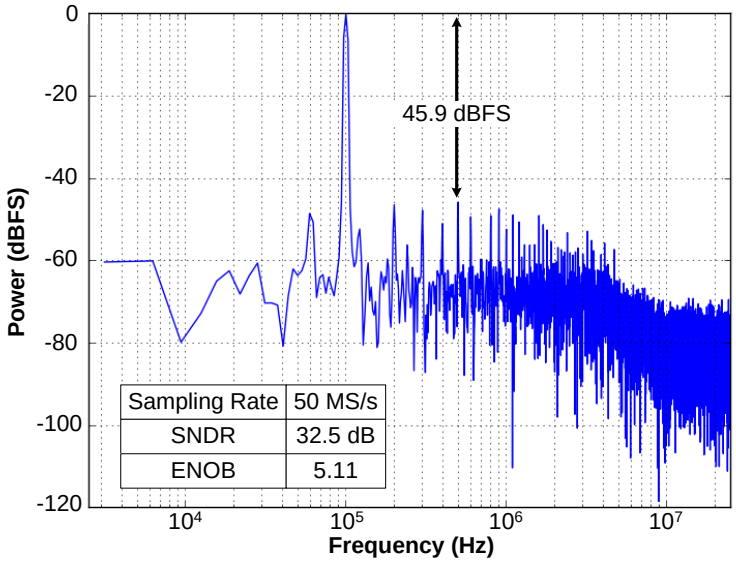


Fig. 5.19 Measured dynamic performance of the programmed ADC.

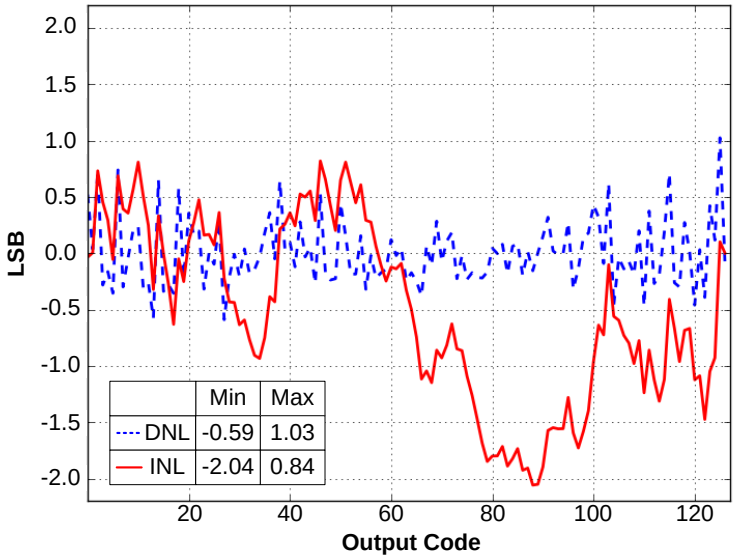


Fig. 5.20 Measured static performance of the programmed ADC.

5.4 DC–DC Converter

Fig. 5.21 illustrates the configuration of the proposed IC as a DC–DC converter and Fig. 5.22 shows how it is programmed on the IC. The programmed DC–DC converter consists of the described 7-bit ADC in Fig. 5.16 as well as a digital PID compensator mapped to ALUs, DPWM and delay cells for non-overlapping pulse generation realized with the proposed TCABs. In order to generate the non-overlapping pulses, two TCABs are configured as delay cells whose common input is CLK_{SW} and outputs are P_{SW} and N_{SW}, respectively, as illustrated in Fig. 2.30. Each delay cell is configured with fixed amount of delay so that $t_{rise,P}$ (i.e., the rising delay between CLK_{SW} and P_{SW}) is shorter than $t_{rise,N}$ (i.e., the rising delay between CLK_{SW} and N_{SW}) and $t_{fall,P}$ (i.e., the falling delay between CLK_{SW} and P_{SW}) is longer than $t_{fall,N}$ (i.e., the falling delay between CLK_{SW} and N_{SW}). The buck converter stage is composed of gate driver and on-chip power transistors included as dedicated blocks within the fabricated IC with an off-chip 3.3-μH inductor and 0.22-μF capacitor.

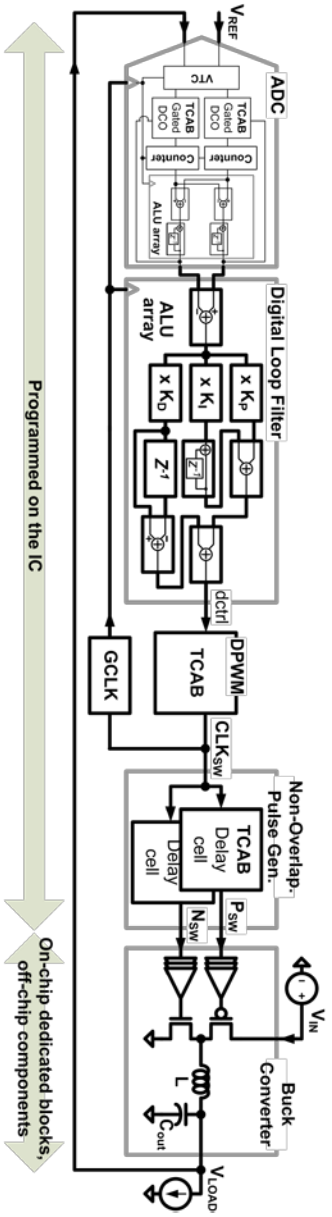


Fig. 5.21 The chip configuration as a DC–DC converter.

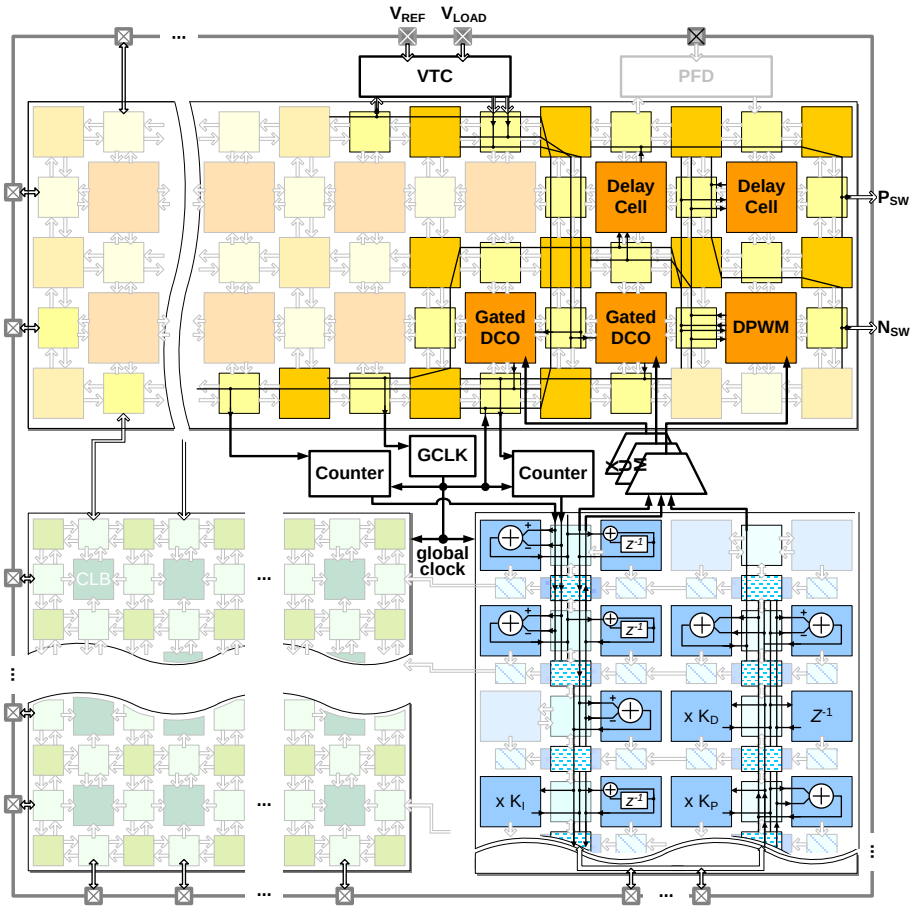
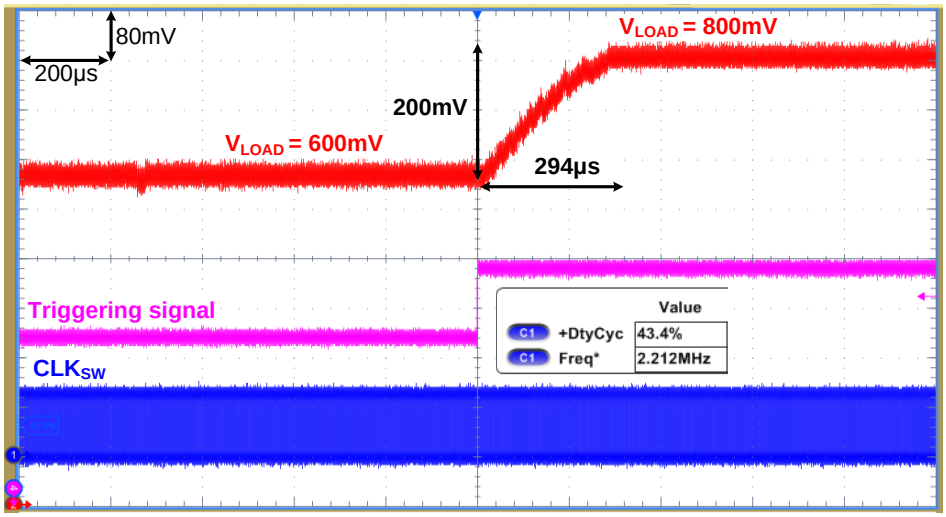
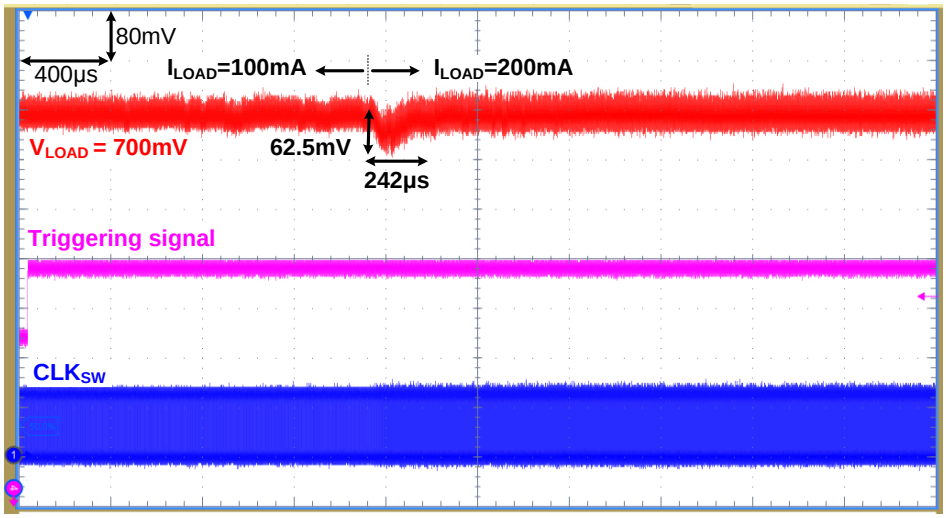


Fig. 5.22 Exemplary placement and routing of the DC–DC converter.

Reference tracking/load regulation waveforms are shown in Fig. 5.23. When V_{REF} has a step from 600 mV to 800 mV, V_{LOAD} successfully tracks the step input with 294-μs settling time, supplying 150 mA to the load as shown in Fig. 5.23 (a). Fig. 5.23 (b) also demonstrates that the programmed feedback controller is capable of regulating the load transition of 100-to-200 mA step in I_{LOAD}.



(a)



(b)

Fig. 5.23 Measured output voltage waveforms of the programmed DC–DC converter in (a) reference tracking (600-to-800 mV step transition with a 150 mA load current) and (b) load transient (100-to-200 mA step transition with a 700 mV output voltage).

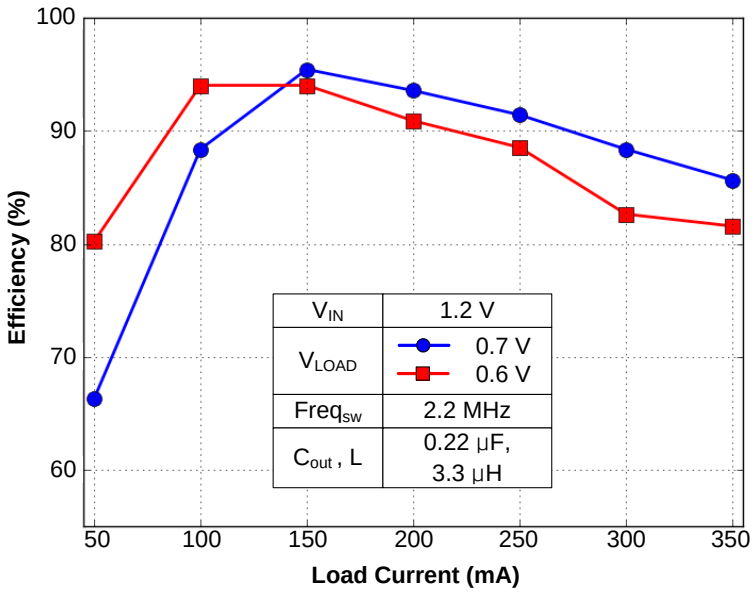


Fig. 5.24 Conversion efficiencies for different load conditions of the programmed DC–DC converter.

The conversion efficiencies for different load conditions are presented in Fig. 5.24. While converting a 1.2-V input to a 0.7-V output and supplying 150 mA, the programmed DC-to-DC converter switching at 2.2 MHz achieves the peak efficiency of 95.5 %.

Chapter 6

Conclusion

In this thesis, design of a field-programmable IC to enable the rapid and low-cost prototyping of analog/mixed-signal systems has been presented.

To realize the field-programmable analog functionality, TCAB has been proposed. A single TCAB can be programmed to various analog circuits, including a time-to-digital converter, digitally-controlled oscillator, digitally-controlled delay cell, digital pulse-width modulator, and phase interpolator. In addition, the TCABs express analog information using the frequency, pulse width, delay, or phase of digital pulses or pulse sequences, rather than using analog voltage or current signals for less susceptibility to attenuation and noise. This expression of analog information in the digital pulses also makes it easy to implement scalable programmable interconnects among the TCABs.

The proposed field-programmable IC also includes arrays of configurable logic blocks (CLBs) and programmable arithmetic logic units (ALUs) for programmable

digital functions. Therefore, by programming the functionality of the TCAB, CLB, and ALU arrays and configuring the interconnects, the chip can implement various mixed-signal systems.

The versatile programmability of the TCABs and the IC has been demonstrated by programming a prototype IC fabricated with 65-nm CMOS technology to diverse mixed-signal systems and measuring their performances. The programmed IC successfully operated as a 1-GHz phase-locked loop with a 12.3-ps_{rms} integrated jitter, as a 50-MS/s analog-to-digital converter with a 32.5-dB SNDR, and as a 1.2-to-0.7 V DC–DC converter with 95.5 % efficiency.

Bibliography

[1] S. M. Trimberger, “Three Ages of FPGAs: A Retrospective on the First Thirty Years of FPGA Technology,” *Proceedings of the IEEE*, vol. 103, no. 3, pp. 318-331, Mar. 2015.

[2] S. Ahmad, V. Boppana, I. Ganusov, V. Kathail, V. Rajagopalan, and R. Wittig, “A 16-nm Multiprocessing System-on-Chip Field-Programmable Gate Array Platform,” *IEEE Micro*, vol. 36, no. 2, pp. 48-62, Mar.-Apr. 2006.

[3] FPGA Overview, [Online] Available: https://www.altera.com/products/fpga/overview.html

[4] All Programmable FPGAs and 3D ICs, [Online] Available: https://www.xilinx.com/products/silicon-devices/fpga.html

[5] W. Carter, K. Duong, R. H. Freeman, H. Hsieh, J. Y. Ja, J. E. Mahoney, L. T. Ngo, and S. L. Sze, ‘‘A User Programmable Reconfigurable Gate Array,’’ in *Proc. Custom Integrated Circuits Conference*, pp. 233-235, May 1986.

[6] J. Becker, F. Henrici, S. Trendelenburg, M. Ortmanns, and Y. Manoli, “A Continuous-Time Hexagonal Field-Programmable Analog Array in 0.13µm CMOS with 186MHz GBW,” in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 70-71, Feb. 2008.

[7] B. Pankiewicz, M. Wojcikowski, S. Szczepanski, and Y. Sun, “A Field Programmable Analog Array for CMOS Continuous-Time OTA-C Filter Applications,” *IEEE Journal of Solid-State Circuits*, vol. 37, no. 2, pp. 125-136, Feb. 2002.

[8] M. Mar, B. Sullam, and E. Blom, “An Architecture for a Configurable Mixed-Signal Device,” *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 565-568, Mar. 2003.

[9] A. Basu, S. Brink, C. Schlottmann, S. Ramakrishnan, C. Petre, S. Koziol, F. Baskaya, C. M. Twigg, and P. Hasler, “A Floating-Gate-Based Field-Programmable Analog Array,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 9, pp. 1781-1784, Sep. 2010.

[10] R. B. Wunderlich, F. Adil, and P. Hasler, “Floating Gate-Based Field Programmable Mixed-Signal Array,” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 8, pp. 1496-1505, Aug. 2013.

[11] P. Lajevardi, A. P. Chandrakasan, and H.-S. Lee, “Zero-Crossing Detector Based Reconfigurable Analog System,” *IEEE Journal of Solid-State Circuits*, vol. 46, no. 11, pp. 2478-2487, Nov. 2011.

[12] N. Suda, J. Suh, N. Hakim, Y. Cao, and B. Bakkaloglu, “A 65 nm Programmable ANalog Device Array (PANDA) for Analog Circuit Emulation,” *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 63, no. 2, pp. 181-190, Feb. 2016.

[13] J. Suh, N. Suda, C. Xu, N. Hakim, Y. Cao, and B. Bakkaloglu, “Programmable ANalog Device Array (PANDA): A Methodology for Transistor-Level Analog Emulation,” *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol. 60, no. 6, pp. 1369-1380, Jun. 2013.

[14] R. Zheng, J. Suh, C. Xu, N. Hakim, B. Bakkaloglu, and Y. Cao, “Programmable Analog Device Array: A Platform for Transistor-Level Analog Reconfigurability,” in *Proc. Design Automation Conference*, pp. 322-327, Jun. 2011.

[15] D. Fernandez, L. Martinez-Alvarado, and J. Madrenas, “A Translinear, Log-Domain FPAA on Standard CMOS Technology,” *IEEE Journal of Solid-State Circuits*, vol. 47, no. 2, pp. 490-503, Feb. 2012.

[16] P. Chow, P. Chow, and P. G. Gulak, “A Field-Programmable Mixed-Analog-Digital Array,” in *Proc. ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pp. 104-109, Feb. 1995.

[17] J. C. Kemerling, R. Greenwell, and B. Bharath, “Analog- and Mixed-Signal Fabrics,” *Proceedings of the IEEE*, vol. 103, no. 7, pp. 1087-1101, Jul. 2015.

[18] Y. Choi, Y. Lee, S.-H. Baek, S.-J. Lee, and J. Kim, “A Field-Programmable Mixed-Signal IC with Time-Domain Configurable Analog Blocks,” in *Proc. IEEE Symposium on VLSI Circuits*, PP. 138-139, Jun. 2016.

[19] M. Z. Straayer and M.H. Perrott, “A 12-Bit, 10-MHz Bandwidth, Continuous-Time ΣΔ ADC with a 5-Bit, 950-MS/s VCO-Based Quantizer,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, pp. 805-814, Apr. 2008.

[20] J. Kim and S. Cho “A Time-Based Analog-to-Digital Converter Using a Multi-Phase Voltage Controlled Oscillator,” in *Proc. IEEE International Symposium on Circuits and Systems*, pp. 3934-3937, May 2006.

[21] T. Oh, H. Venkatram, and U.-K. Moon, “A Time-Based Pipelined ADC Using Both Voltage and Time Domain Information,” *IEEE Journal of Solid-State Circuits*, vol. 49, no. 4, pp. 961-671, Apr. 2014.

[22] P. Chen, C.-C. Chen, Y.-H. Peng, K.-M. Wang, and Y.-S. Wang, “A Time-Domain SAR Smart Temperature Sensor With Curvature Compensation and a 3σ Inaccuracy of $-0.4°C\sim+0.6°C$ Over a 0°C to 90°C Range,” *IEEE Journal of Solid-State Circuits*, vol. 45, no. 3, pp. 600-609, Mar. 2010.

[23] Y. Lee, T. Kang, and J. Kim, “A 9-11-Bit Phase-Interpolating Digital Pulsewidth Modulator With 1000x Frequency Range,” *IEEE Transactions on Industry Applications*, vol. 51, no. 4, pp. 3376-3384, Jul.-Aug. 2015.

[24] M. Lee, Y. Choi, and J. Kim, "A 500-MHz, 0.76-W/mm^2 Power Density and 76.2% Power Efficiency, Fully-Integrated Digital Buck Converter in 65nm CMOS," *IEEE Transactions on Industry Applications*, vol. 52, no. 4, pp. 3315-3323, Jul.-Aug. 2016.

[25] B. M. Helal, M. Z. Straayer, G.-Y. Wei, and M. H. Perrott, "A Low Jitter 1.6 GHz Multiplying DLL Utilizing a Scrambling Time-to-Digital Converter and Digital Correlation," in *Proc. IEEE Symposium on VLSI Circuits*, pp. 166-167, Jun. 2007.

[26] M. Z. Straayer and M. H. Perrott, "An Efficient High-Resolution 11-Bit Noise-Shaping Multipath Gated Ring Oscillator TDC," in *Proc. IEEE Symposium on VLSI Circuits*, PP. 82-83, Jun. 2008.

[27] S. Ryu, H. Yeo, Y. Lee, S. Son, and J. Kim, "A 9.2 GHz Digital Phase-Locked Loop with Peaking-Free Transfer Function," *IEEE Journal of Solid-State Circuits*, vol. 49, no. 8, pp. 1773-1784, Aug. 2014.

[28] A. Agrawal, J. F. Bulzacchelli, T. O. Dickson, Y. Liu, J. A. Tierno, and D. J. Friedman, "A 19-Gb/s Serial Link Receiver with Both 4-Tap FFE and 5-Tap DFE Functions in 45-nm SOI CMOS," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 12, pp. 3220-3231, Dec. 2012.

[29] J. F. Bulzacchelli, T. O. Dickson, Z. T. Deniz, H. A. Ainspan, B. D. Parker, M. P. Beakes, S. V. Rylov, and D. J. Friedman, "A 78mW 11.1Gb/s 5-tap DFE Receiver with Digitally Calibrated Current-Integrating Summers in 65nm CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 368-369, Feb. 2009.

[30] S. Son, H.-S. Kim, M.-J. Park, K. Kim, E-H. Chen, B. Leibowitz, and J. Kim, "A 2.3-mW, 5-Gb/s Low-Power Decision-Feedback Equalizer Receiver Front-End and its Two-Step, Minimum Bit-Error-Rate Adaptation Algorithm," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 11, pp. 2693-2704, Nov. 2013.

[31] R. Xu, B. Liu, and J. Yuan, "Digitally Calibrated 768-kS/s 10-b Mini-

mum-Size SAR ADC Array With Dithering," *IEEE Journal of Solid-State Circuits*, vol. 47, no. 9, pp. 2129-2140, Sep. 2012.

[32] B. Murmann, "Digitally Assisted Analog Circuits," *IEEE Micro*, vol. 26, no.2, pp. 38-47, Mar.-Apr. 2006.

[33] H-Y Shih, C-N Kuo, W-H Chen, T-Y Yang, and K-C Juang, "A 250 MHz 14 dB-NF 73 dB-Gain 82 dB-DR Analog Baseband Chain With Digital-Assisted DC-Offset Calibration for Ultra-Wideband," *IEEE Journal of Solid-State Circuits*, vol. 45, no. 2, pp. 338-350, Feb. 2010.

[34] R. Gangarajaiah, M. Abdulaziz, H. Sjoland, P. Nilsson, and L. Liu, "A Digitally Assisted Nonlinearity Mitigation System for Tunable Channel Select Filters," *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol. 63, no. 1, pp. 69-73, Jan. 2016.

[35] P. Amberg, F. Liu, M. Dayringer, J. Lexau, D. Patil, J. Gainsley, H. F. Moghadam, E. Alon, X. Zheng, J. E. Cunningham, A. V. Krishnamoorthy, and R. Ho, "Digitally-Assisted Analog Circuits for a 10 Gbps, 395 fJ/b Optical Receiver in 40 nm CMOS," in *Proc. IEEE Asian Solid State Circuits Conference*, pp. 29-32, Nov. 2011.

[36] R. B. Staszewski, J. Wallberg, S. Rezeq, C.-M. Hung, O. Eliezer, S. Vemulapalli, C. Fernando, K. Maggio, R. Staszewski, N. Barton, M.-C. Lee, P. Cruise, M. Entezari, K. Muhammad, and D. Leipold, "All-Digital PLL and GSM/EDGE Transmitter in 90nm CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 316-317, Feb. 2005.

[37] M. Lee, M. E. Heidari, and A. A. Abidi, "A Low-Noise Wideband Digital Phase-Locked Loop Based on a Coarse/Fine Time-to-Digital Converter With Subpicosecond Resolution" *IEEE Journal of Solid-State Circuits*, vol. 44, no. 10, pp. 2808-2816, Oct. 2009.

[38] G. Marzin, S. Levantino, C. Samori, and A. Lacaita, "A Background Calibration Technique to Control Bandwidth in Digital PLLs," in *IEEE Inter-*

national Solid-State Circuits Conference Digest of Technical Papers, pp. 54-55, Feb. 2014.

[39] Z. Lukic, N. Rahman, and A. Prodie, "Multibit Σ-Δ PWM Digital Controller IC for DC-DC Converters Operating at Switching Frequencies Beyond 10 MHz," *IEEE Transactions on Power Electronics*, vol. 22, no. 5, pp. 1693-1707, Sep. 2007.

[40] B.J. Patella, A. Prodic, A. Zirger, and D. Maksimovic, "High-Frequency Digital PWM Controller IC for DC-DC Converters," *IEEE Transactions on Power Electronics*, vol. 18, no. 1, pp. 438-446, Jan. 2003.

[41] S. J. Kim, R. K. Nandwana, Q. Khan, R. Pilawa-Podgurski, and P. K. Hanumolu, "A 1.8V 30-to-70MHz 87% Peak-Efficiency 0.32mm^2 4-Phase Time-Based Buck Converter Consuming 3μA/MHz Quiescent Current in 65nm CMOS," in *IEEE International Solid-State Circuits Conference Digest of Technical Papers*, pp. 216-217, Feb. 2015.

[42] V. Betz, J. Rose, and A. Marquardt, *Architecture and CAD for Deep-Submicron FPGAs*, MA, USA, Kluwer Academic Publishers Norwell, 1999.

[43] S. J. E. Wilton, "Architecture and Algorithms for Field Programmable Gate Arrays with Embedded Memory," Ph. D. dissertation, Department of Electrical and Computer Engineering, University of Toronto, 1997.

[44] I. Kuon and J. Rose, "Area and Delay Trade-offs in the Circuit and Architecture Design of FPGAs," in *Proc. ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pp. 149-158, Feb. 2008.

[45] P. A. Jamieson, K. B. Kent, F. Gharibian, and L. Shannon, "Odin II - An Open-Source Verilog HDL Synthesis Tool for CAD Research," in *Proc. International Symposium on Field-Programmable Custom Computing Machines*, pp. 149-156, May 2010.

[46] Berkeley Logic Synthesis and Verification Group ABC: A System for

Sequential Synthesis and Verification, [Online] Available: http://www.eecs.berkeley.edu/~alanmi/abc/

[47] J. Luu, I. Kuon, P. Jamieson, T. Campbell, A. Ye, W. Fang, and J. Rose, "VPR 5.0: FPGA CAD and Architecture Exploration Tools with Single Driver Routing, Heterogeneity and Process Scaling," in *Proc. ACM/SIGDA International Symposium on Field Programmable Gate Arrays*, pp. 133-142, Feb. 2009.

[48] U. Farooq, Z. Marrakchi, and H. Mehrez, *Tree-based Heterogeneous FPGA Architectures: Application Specific Exploration and Optimization*, New York, USA, Springer Science+Business Media, 2012

[49] D. I. Porat and S. Wojcicki, "Fast Synchronous Gray Counter," *Nuclear Instruments and Methods*, vol. 169, no. 1, pp. 243-244, Feb. 1980.

[50] V. Kratyuk, P. K. Hanumolu, U.-K. Moon, and K. Mayaram, "A Design Procedure for All-Digital Phase-Locked Loops Based on a Charge-Pump Phase-Locked-Loop Analogy," *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol. 54, no. 3, pp. 247-251, Mar. 2007.

초 록

다양한 전자기기의 빠른 개발을 위해서는 새로운 혼성신호 IC 들을 빠른 시간 내에 적은 비용으로 개발할 수 있어야만 한다. 현장 프로그램 가능 게이트 어레이 (FPGA)가 디지털 시스템 개발시의 비용과 시간에 대한 요건을 충족시키기 위한 해법으로 확실히 자리 매김 한 것에 비하여, 혼성신호 회로들을 위한 프로그램 가능한 IC 들은 여전히 연구가 진행 중이다. 본 논문은 시간 영역상에서 아날로그적 기능을 수행하도록 함으로써 기존의 연구들에서 해결하지 못했던 여러 문제점들을 극복한 현장 프로그램 가능 IC 의 설계를 다룬다.

아날로그 회로의 기능을 프로그램 하여 바꿀 수 있는 가변기능형 아날로그 블록 (TCAB)이 제안되었다. 하나의 TCAB 는 시간-디지털 변환기, 디지털 신호로 제어되는 발진기, 디지털 신호로 제어되는 지연시간 조절회로, 디지털 선호로 제어되는 펄스 폭 변조기, 위상 조절기 등과 같은 다양한 아날로그 회로로써 동작할 수 있도록 프로그램 가능하다. 그리고, 이 TCAB 는 아날로그 정보를 전압이나 전류 형태로 표현하는 것이 아니라, 디지털 펄스의 주파수, 폭, 위상, 펄스들의 순서 등으로 표현하기 때문에 잡음이나 감쇄에 대해 덜 민감해진다. 이러한 디지털 펄스를 이용한 아날로그 정보의 표현 방식은 여러 TCAB 사이를 연결하는 프로그램 가능한 연결 블록들을 확장이 쉬운 디지털 방식으로 구현하는 데에 도움이 된다. 또한, 최신의 다양한 혼성신호 시스템들의 구조를 그대로 프로그램 할 수 있는 IC 구조도 제안된다. 제안하는 IC 에는 TCAB 들 뿐만 아니라, 재구성 가능한 로직 블록 (CLB)들과

프로그램 가능한 수리 연산 디지털 블록 (ALU)들도 포함되어 있다. TCAB, CLB, ALU 의 기능과 이 블록들 사이의 연결상태를 프로그램 함으로써, 제안하는 IC 는 다양한 혼성신호 시스템으로 프로그램 되어 동작할 수 있다.

제안한 TCAB 와 IC 가 다양한 시스템으로 프로그램 가능함을 보이기 위하여 65 nm CMOS 공정을 이용하여 시작품 IC 를 제작하였으며, 제작된 IC 는 12.3 ps_{rms} 의 잡음성능을 갖는 1 GHz 출력의 위상동기화 루프, 32.5 dB 의 신호 대 잡음 비를 갖는 50 MS/s 아날로그-디지털 변환기, 95.5 % 의 효율을 갖는 1.2 V 입력 0.7 V 출력의 직류-직류 변환기의 제어회로 등으로 프로그램 되어 성공적으로 동작하였다.

.

주요어 : 현장 프로그램이 가능한 혼성신호 집적회로, 현장 프로그램이 가능한 아날로그 어레이, 재구성 가능한 구조, 재구성이 가능한 아날로그 어레이, 혼성신호 집적회로.

학 번 : 2013-30264