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Ph.D. Dissertation

DESIGN OF A LOW-POWER SIGNAL-SPECIFIC SAR ADC FOR ECG MONITORING APPLICATIONS

심전도 감시 분야를 위한 저전력 신호 특화된 축차 비교형 아날로그-디지털 변환기의 설계

by

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AUGUST 2017

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ABSTRACT

DESIGN OF A LOW-POWER SIGNAL-SPECIFIC SAR ADC FOR ECG MONITORING APPLICATIONS

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Electrocardiography is an indispensable tool employed for diagnosis of cardiovascular diseases. When electrocardiograms (ECGs) need to be monitored for a long time, e.g. to diagnose arrhythmia, a device has to be worn or implanted under the skin, which requires low energy consumption.

Successive approximation register analog-to-digital converters (SAR ADCs) have been especially preferred in low power applications, while the recent trend of ADC designs shows that the SAR ADCs find a much wide range of applications, and are the most versatile ADC architecture.

The subject of the dissertation is the design of a signal-specific SAR ADC scheme that reduces the power consumption by exploiting the characteristics of the input signal of a particular type whose signal activity is low on average and dichotomous, as best

exemplified by ECGs. This dissertation presents a 1.8-V 10-bit 1-kS/s low-power SAR ADC with the proposed signal-specific switching algorithm. The proposed adaptive switching algorithm has two operation modes suitable for the dichotomous activity of the ECG: full switching mode that resolves the full range of the input as an ordinary SAR ADC, and reduced switching mode that assumes 5 MSBs will not change and samples just the rest LSB portion and resolves it in 5 bitcycles. The reduced number of bitcycles yields saving in switching power consumption. For smooth mode change adaptive to the input signal activity, an additional function in each mode, viz., MSBs tracking in full switching mode and LSBs extrapolation in reduced switching mode, runs concurrently with the respective main operation.

A behavioral model of the proposed SAR ADC with the segmented capacitor digital-to-analog converter (CDAC) topology was created in MATLAB and was used in the tests, which verified the function and effectiveness of the adaptive switching algorithm. The model describes the evolution of all internal node voltages in the CDAC by each switching action, from which the charge variation in each capacitor and the switching energy consumption can be computed. The model was extensively used for the development and analysis of the idea. The 5-bit size of the MSB section was determined from the simulation results with the behavioral model.

A prototype chip was fabricated in 0.18-μm CMOS technology. Measurements with an ECG type input proved the suitability of the adaptive switching for ECG monitoring. The power reduction by the adaptive switching in each of comparator, logic, and DAC power domains was calculated from the measurements of both cases of the adaptive-

switching and fixed-full-switching operations, the latter of which is equivalent to the conventional SAR ADC operation. It achieved a reduction in comparator power consumption by 39%. The DAC power, i.e. the switching power consumed in the CDAC, achieved a reduction by 1.28 nW, which is close to the result of the behavioral model simulation. The reduction in the logic power domain was 12%. In terms of total power consumption, the adaptive switching consumed 91.02 nW while the fixed full switching consumed 107.51 nW. The reduction corresponds to 15.3% in proportion. In addition, the intrinsic performance of the ADC was measured using a sinusoidal input. It achieved a signal-to-noise-and-distortion ratio of 56.24 dB and a spurious-free dynamic range of 62.00 dB. The maximum differential nonlinearity of +0.39/−1 LSBs and maximum integral nonlinearity of +0.86/−1.5 LSBs were measured. The main source of the nonlinearity is the capacitor mismatch in the CDAC.

Keywords: SAR ADC, ECG, signal activity, adaptive switching, signal-specific.

Student Number: 2011-30973

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CHAPTER 1

INTRODUCTION

1.1 ELECTROCARDIOGRAPHY

In the modern world, the mortality rate from cardiovascular disease is increasing, which is epidemiologically attributed to the population growth and the aging of populations [1]. According to the World Health Organization, cardiovascular disease is the most common among the causes of global mortality: an estimated 17.7 million people died from cardiovascular diseases in 2015, representing 31% of all global deaths. [2]. Electrocardiography (ECG[1]) is one of the most useful tools for diagnosis of cardiovascular disease [3]. It is the process of recording the electrical activity of the heart. Around the heart is an electric field in which currents flow in repetitive patterns with each cardiac cycle [4]. The currents are detected at the skin by electrodes, is amplified, and then displayed on an oscilloscope or written on a strip recorder [4]. Fig. 1.1 shows a typical waveform of a record (electrocardiogram). A skilled cardiologist can interpret one to find out the information about the structure and function of the heart.

1 The acronym can also stand for an electrocardiogram. The context clarifies which is meant.

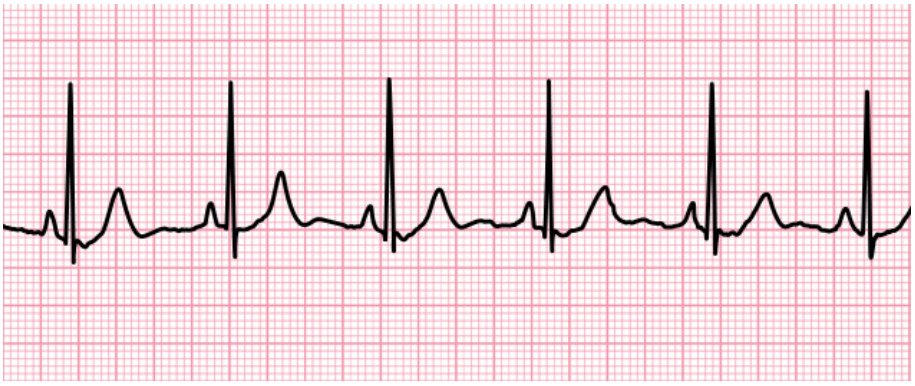


Fig. 1.1 Typical electrocardiogram.[2]

One feature of modern ECG is the widespread use of computerized systems for storage and analysis [5]. After conversion to digital, the signals are analyzed by computer software that measures ECG intervals and amplitudes, and even provides instantaneous interpretations [5].

A standard ECG records the signals for only a few seconds [6], but there are occasions when ECG is conducted for a long time. In particular, diagnosis of arrhythmia requires the ECG signals be recorded for full 24- or 48-hour period [6] because arrhythmia can occur very rarely (e.g., only a few times a day) with each event lasting only a handful of seconds [7]. A Holter monitor is worn for this [6], or a small implantable ECG recorder is injected under the skin [7]. While the wearable approach is simpler, it causes inconvenience for the patient in daily life, and it is prone to external noise as it is exposed outside. The implantable approach is freer of the interference from

2 Normal sinus rhythm. Digital image adapted from the original animation. AED Superstore. Accessed April 21, 2017. http://www.aedsuperstore.com.

external noise, whereas surgery may be needed for injection of the ECG recorder. There is an attempt to design a syringe-implantable system in order to avoid the hassle [7]. Nevertheless, low power design is important in either approach for longevity of battery life [7]. For example, literature focusing on low-power successive approximation register analog-to-digital converters (SAR ADCs) for ECG applications is found in [8]–[10].

1.2 RECENT TRENDS IN SAR ADC DESIGNS

The past decade witnessed the revival of SAR ADCs [11], and the current decade is watching that they have become the most popular ADC architecture [11], [12], leading in state-of-the-art ADC designs [13]. One of the reasons for this is ascribed to the architecture itself, whose most components such as MOS switches and digital circuits can strongly benefit from technology scaling [13]. A schematic diagram of the conventional SAR ADC design is depicted in Fig 1.2. It consists of a capacitive digital-to-analog converter (CDAC), SAR logic circuit, and a comparator. A dynamic latch alone is often used as the comparator. As the architecture does not include any static power consuming component such as an amplifier, it consumes the lowest power among the ADC architectures. Furthermore, exploitation of the benefits from technology scaling and

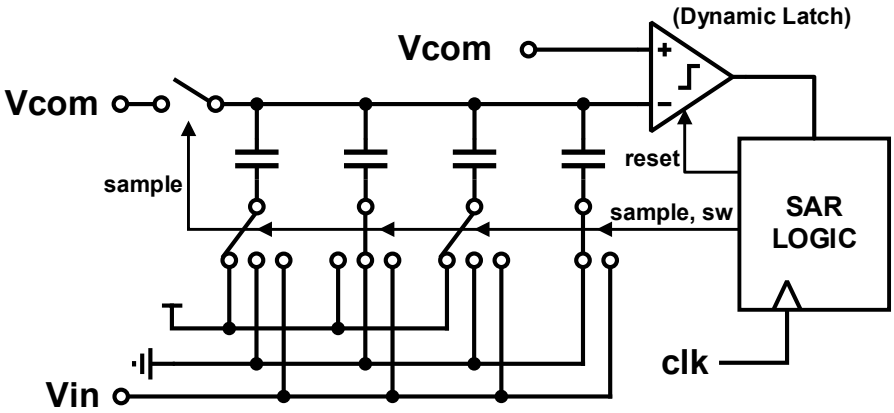


Fig. 1.2 Schematic diagram of the conventional SAR ADC.

recent innovations have helped extend the available ranges of speed and resolution, encroaching on the realms in which the flash and pipelined ADCs and ΔΣ ADCs were formerly dominant, respectively [11], [14]. With the wide coverage of performance and lowest energy consumption, SAR ADCs are now a versatile building block applicable in a broad range of areas [13].

Fig. 1.3 shows the energy consumption versus signal-to-noise-and-distortion ratio (SNDR) of ADC designs published in the IEEE International Solid-State Conference and the IEEE Symposium on VLSI Circuits in the latest couple of decades [15]. As expected, the SAR ADC designs exhibit the lowest energy consumption among the entire ADC designs. Along the SNDR axis, however, they are confined mostly under 75 dB, which corresponds to an effective number of bits (ENOB) about 12 bits. This indicates that the ENOB of 12 bits is the normally achievable upper limit of resolution without inventive techniques, such as oversampling [16] and noise shaping [17].

Fig. 1.4 shows the Walden figure of merit versus sampling rate of the same ADC designs [15]. It exhibits that the SAR ADC designs cover the widest range of speed with good figures of merit. Their sampling rates could reach tens of GS/s by application of time interleaving [18]–[20] and aggressively scaled technology [20]. Over the sampling rate range from 1 kS/s to tens of MS/s, they manifest much superior figures of merit to the contenders such as ΔΣ ADCs [16], [21], [22]. The achievement of low power is partly attributed to the almost digital implementation of the SAR ADC architecture, which allows the use of low supply voltages [21], [22].

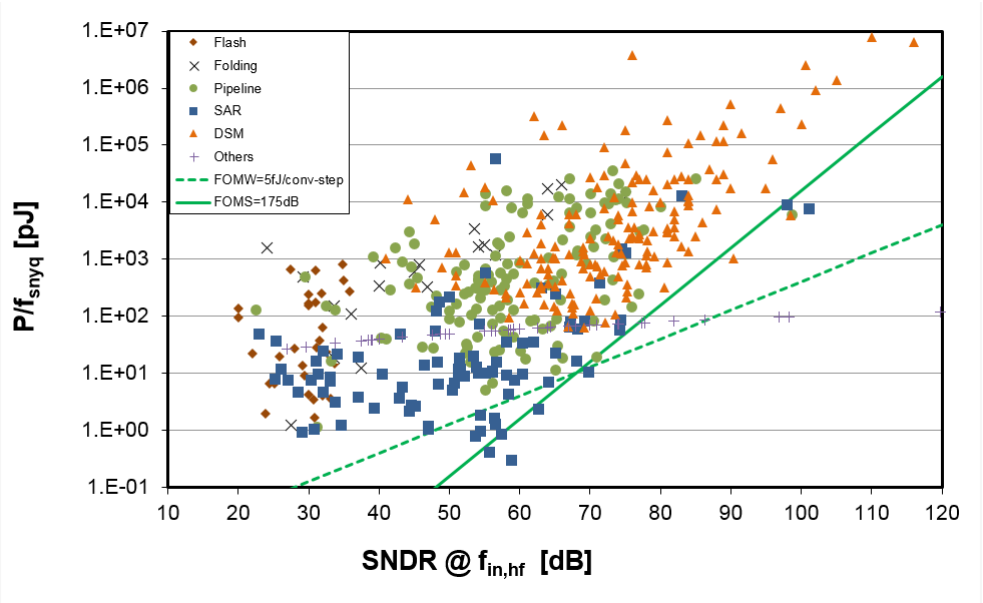


Fig. 1.3 Energy consumption vs. SNDR of recent ADC designs.

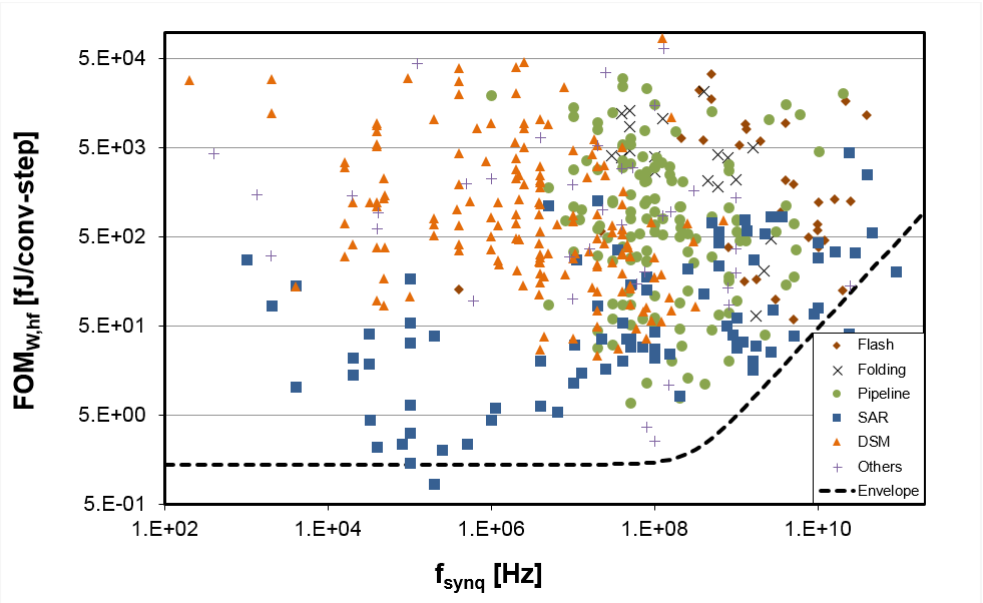


Fig. 1.4 Walden figure of merit vs. sampling rate of recent ADC designs.

1.3 DISSERTATION CONTRIBUTIONS AND ORGANIZATION

The dissertation presents a low-power SAR ADC design suitable for long-term ECG monitoring applications, especially wearable or implantable monitoring systems. The proposed signal-specific switching algorithm, called adaptive switching, employs two switching modes to exploit the dichotomy in the activity of ECG signals for power reduction [23]. Moreover, the proposed algorithm is applicable as well to other input signals as far as their signal activity is dichotomous like that of ECGs.

A behavioral model has been developed in MATLAB to investigate the effectiveness of the proposed adaptive switching. The evolution of all internal voltages of the segmented CDAC by each switching operation was derived from the law of conservation of charge. The detailed model is useful in analysis as it can be used to compute the switching energy consumption in the SAR ADC with the segmented CDAC topology. It has never been done in the literature so far, to the best knowledge of the author.

Chapter 2 briefly introduces the operation principle of the SAR ADC and describes general design issues such as power reduction, offset, noise, linearity, and area. This chapter focuses especially on power reduction switching techniques as it is the main theme of the dissertation.

Chapter 3 explains the adaptive switching algorithm in detail. It is organized to show the progress of the idea development, from the motivation of the idea to the behavioral model tests to the circuit implementation. It first provides brief information on the

characteristics of the ECGs and the specifications of typical ECG readout circuits. The second section introduces a few related works that employ signal-specific techniques. Section 3.3 explains the proposed adaptive switching algorithm step by step from the motivation. As the behavioral model simulations were heavily relied on in multiple stages of the algorithm development, a good deal of space is devoted to the description of the model development and simulations. The derivation of the formula for the switching energy computation in the segmented CDAC is presented in detail. The applicability of the adaptive switching to other applications is briefly discussed at the end of the section. Finally, Section 3.4 presents the circuit implementation.

Chapter 4 presents the measurements of the prototype and the discussions of the results. The conclusion is presented in Chapter 5.

CHAPTER 2

SAR ADC OPERATION AND DESIGN ISSUES

2.1 OPERATION PRINCIPLE

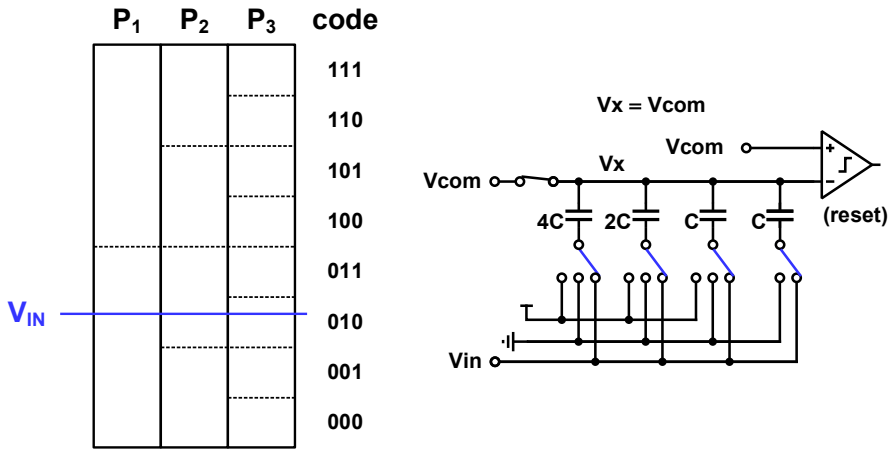
The conventional SAR ADC in Fig. 1.1 was originated from the innovative work in the 1970s [24]. The underlying principle is charge redistribution: the input is sampled as charge (sampling phase), then binary search is conducted by charge redistribution by the law of conservation of charge, until the digital output is found (conversion phase). The timing for the phases and internal actions in them is derived from the clock signal. Fig. 2.1(a) shows the schematic diagram of the SAR ADC in the sampling phase. The top plates of the capacitors of the DAC are connected to the common mode V_{com}, which is half of V_{ref}. All bottom plates are connected to the input. The amount of charge sampled in the capacitors settles to the value representing the input voltage:

$$\begin{aligned} Q_{\text{samp}} &= \sum_i C_i \left(V_X - V_{\text{in}} \right) \\ &= 8C \left(V_{\text{com}} - V_{\text{in}} \right), \end{aligned} \tag{2.1}$$

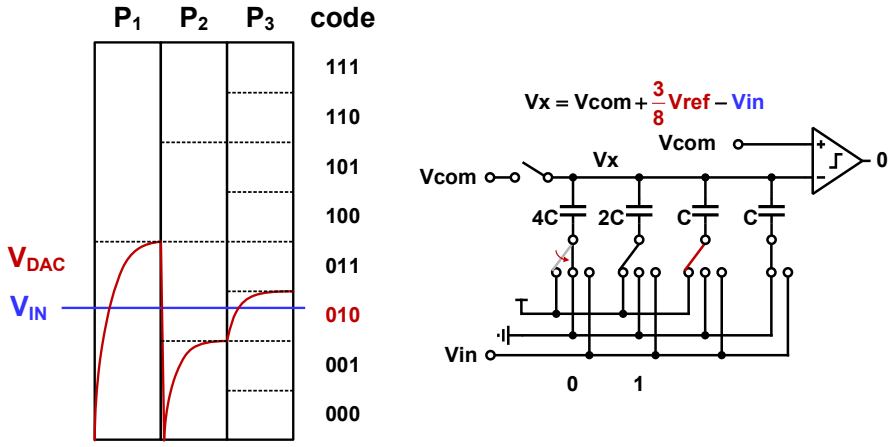
where Q_{samp} is the charge sampled onto the DAC, and V_X is the output voltage of the DAC

and the input to the comparator.

In the conversion phase, the DAC are disconnected from V_{com} and V_{in}, as shown in Fig. 2.1(b). The DAC output voltage node is floated so that the sampled charge Q_{samp} is conserved during the conversion phase. In the first cycle, the bottom plate of the MSB capacitor is connected to V_{ref} and the rest bottom plates are connected to 0, which represents comparing the input with the common mode. The comparison result determines the MSB. The MSB switch is then thrown to the appropriate reference source: if the comparison result is 1, the switch remains at V_{ref}; otherwise, the switch is thrown to 0. Next, the switch of the next bit is thrown to V_{ref} to determine the value of the bit. This procedure repeats until the LSB is determined.



(a)



(b)

Fig. 2.1 Conventional SAR ADC operation (a) in the sampling phase and (b) in the conversion phase.

2.2 SWITCHING ALGORITHMS FOR POWER REDUCTION

As the subject of the dissertation is about low-power design, power reduction is the most important design issue to be treated. The most straightforward method to reduce power consumption is to apply a lower supply voltage, or a clock with a slower frequency. However, this approach may be undesirable as they are usually specified as fixed values to satisfy the design requirements. Another method is to adopt a more power efficient switching algorithm. This section introduces a series of switching algorithms developed over time, each of which improves the prior one. Their operation principles and how they achieve reductions in energy consumption are explained.

2.2.1 COMPUTATION OF SWITCHING ENERGY CONSUMPTION

It is instructive to review how the energy consumption is computed in switching transitions in a CDAC. Fig 2.2 shows a 2-bit CDAC example that transitions from the

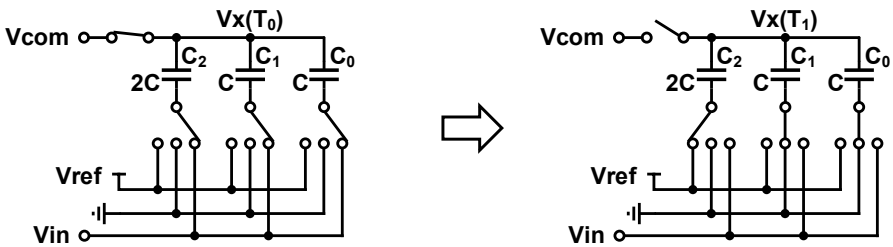


Fig. 2.2 Switch transition over time interval [T_0, T_1].

sampling phase to the first cycle of the conversion phase; the time interval is denoted as $[T_0, T_1]$ below. Over the time interval, the MSB switch is thrown from V_{in} to V_{ref} and the others are from V_{in} to 0 to determine the MSB. Only C_2 is connected to the V_{ref} source, thus the energy consumption is computed from the current to C_2:

$$i_{ref} = -\frac{dQ_{C2}}{dt}. \tag{2.2}$$

The DAC output voltages at T_0 and T_1 are expressed as

$$V_X(T_0) = V_{com} = \frac{V_{ref}}{2} \tag{2.3}$$

and

$$V_X(T_1) = V_{ref} - V_{in}. \tag{2.4}$$

Combining equations (2.2), (2.3), and (2.4), the energy dissipation over the time interval is computed as

$$\begin{aligned} E(T_0,\ T_1) &= V_{ref}\int_{T_0}^{T_1} i_{ref}(t)dt = -V_{ref}\int_{Q_{C2}(T_0)}^{Q_{C2}(T_1)} dQ_{C2} \\ &= -V_{ref}\cdot 2C\left\{\left[V_X(T_1) - V_{ref}\right] - \left[V_X(T_0) - V_{in}\right]\right\} \\ &= CV_{ref}^2. \end{aligned} \tag{2.5}$$

If the comparator output is 0, the MSB switch is thrown to 0 and the next switch is thrown to V_{ref} to determine the next bit in the next cycle (Fig. 2.3). In this case, the reference source provides current for C_1. Thus,

$$i_{ref} = -\frac{dQ_{C1}}{dt} \tag{2.6}$$

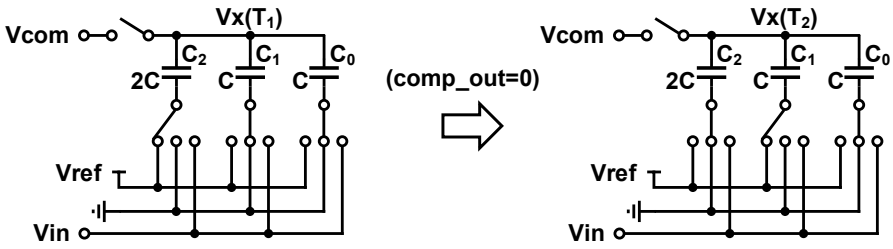


Fig. 2.3 Switch transition over time interval [T_1, T_2].

and

$$V_X(T_2) = \frac{3}{4}V_{\text{ref}} - V_{\text{in}}. \tag{2.7}$$

Combining equations (2.4), (2.6), and (2.7), the energy dissipation over [T_1, T_2] is computed as

$$\begin{aligned} E(T_1,\ T_2) &= V_{\text{ref}} \int_{T_1}^{T_2} i_{\text{ref}}(t)dt = -V_{\text{ref}} \int_{Q_{C1}(T_1)}^{Q_{C1}(T_2)} dQ_{C1} \\ &= -V_{\text{ref}} \cdot C\left\{\left[V_X(T_2) - V_{\text{ref}}\right] - V_X(T_1)\right\} \\ &= \frac{5}{4}CV_{\text{ref}}^2. \end{aligned} \tag{2.8}$$

If the comparator output at time T_1 is 1, V_{ref} sources both C_1 and C_2, hence (2.6) is replaced by

$$i_{\text{ref}} = -\frac{dQ_{C1}}{dt} - \frac{dQ_{C2}}{dt}. \tag{2.9}$$

Substituting (2.9) into (2.8) yields $E(T_1, T_2) = \frac{1}{4}CV_{\text{ref}}^2$.

2.2.2 CONVENTIONAL CHARGE-REDISTRIBUTION SWITCHING

Fig. 2.4 shows the conventional switching algorithm for a 3-bit fully differential SAR ADC. The energy dissipation for every transition is presented in the figure. The first cycle of the conversion phase dissipates energy. The evolution of the switching in the CDAC to the positive input to the comparator is identical to that in the conventional

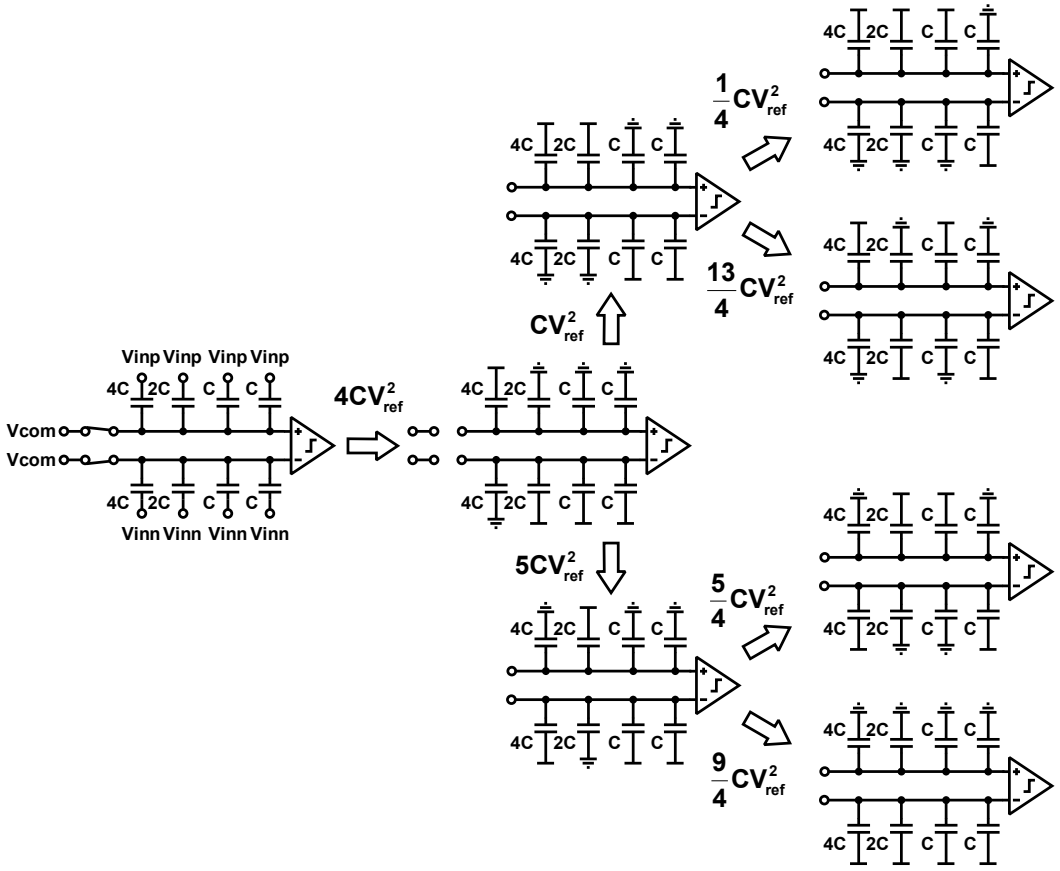


Fig. 2.4 Conventional switching algorithm.

single-ended SAR ADC in Section 2.1. Since the switching on the negative side is just complementary to the positive side, the explanation below will deal with the positive side only without loss of generality.

In each cycle of the conversion phase, the switch of the corresponding bit is thrown to V_{ref} for determination. If the comparator produces an output of 1, the switch stays put, thus the stored charge is largely reusable in the next cycle. As the next bit switch is thrown to V_{ref} (up transition), the reference source needs only to fill up the relatively small difference. However, when the comparison result is 0, the switch at V_{ref} is thrown to 0 (down transition), and some charge is discarded. The reference source has to redevelop the charge needed for the up transition in the next cycle. The down transition at a switch causes relatively large energy dissipation, which is clearly shown in the computed values in Fig. 2.4. The waveform of V_{DAC} in Fig. 2.1(b) visualizes this.

2.2.3 SPLIT-CAPACITOR SWITCHING

The drawback of the conventional switching is that down transitions dissipate more energy, which results in input-dependent imbalance in the energy consumption. Fig. 2.5 shows the operation of the split-capacitor switching algorithm that splits the MSB capacitors into binary weighted sub-capacitor arrays [25]. It alleviates the energy imbalance between up and down transitions in the conventional switching and reduces the energy dissipation by switching the half capacitance in the subarray of the MSB instead

of performing a conventional down transition. The average switching energy is reduced by 38% compared to the conventional switching at the expense of twice as many switches and more complex switching algorithm.

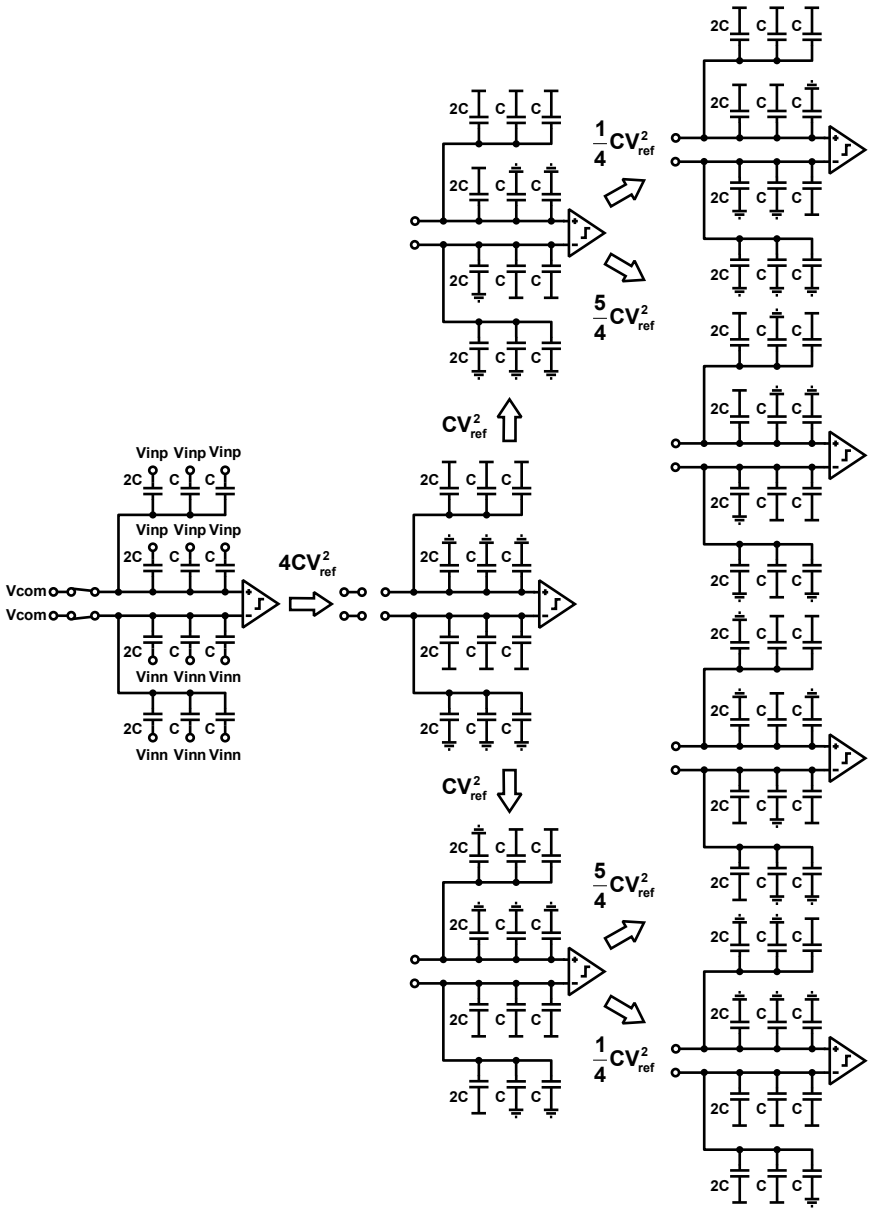


Fig. 2.5 Split-capacitor switching algorithm.

2.2.4 ENERGY-SAVING SWITCHING

Both conventional and split-capacitor switching algorithms consume quite large energy in the first conversion cycle. The energy-saving switching algorithm tackles the problem [26]. It applies V_{ref} onto the top plates in the sampling phase, instead of V_{com}. Thus the up transition in the first cycle is unnecessary for extra charge by the elevated voltage is added onto the capacitors in the sampling phase. The gist of the idea is illustrated in Fig. 2.6. In the first cycle of the conversion phase, all bottom-plate voltages are discharged to ground, which consumes no energy. Moreover, the split-capacitor

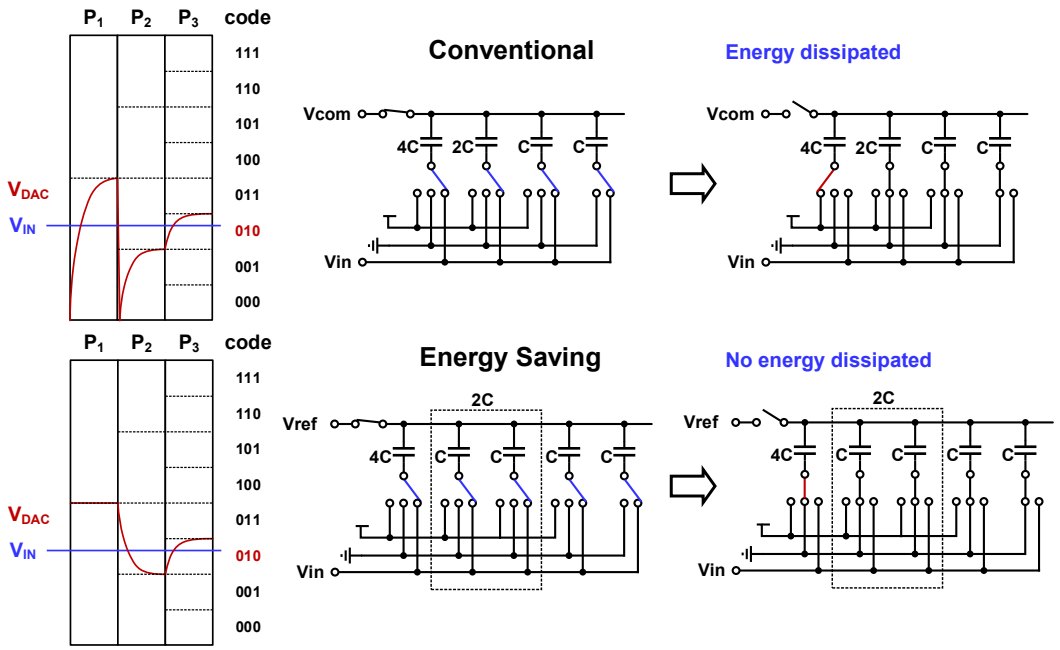


Fig. 2.6 Operation principle of energy-saving switching.

approach [25] is applied to the second MSB capacitors. The energy-saving switching algorithm achieves a 56% energy reduction compared to the conventional switching. Fig. 2.7 presents the operation and energy consumptions of the energy-saving switching [26].

It is noteworthy that it suffers from distortion by parasitics unlike the conventional and split-capacitor switching algorithms. While the CDAC has parasitic elements in parallel with the nominal capacitors, their effect is canceled out if the initial and final voltages on the top plates are the same since the net change in the charge stored in the parasitic capacitors is 0. In both conventional and split-capacitor switching, the top-plate voltages start at V_{com} and return to V_{com}, thus the net parasitic effect is nil. In the energy-saving switching, however, the initial voltage on the top plates is V_{ref} whereas the final voltage is V_{com}. The difference in the parasitic charge joins in the charge redistribution during the conversion phase, affecting the accuracy of the ADC output.

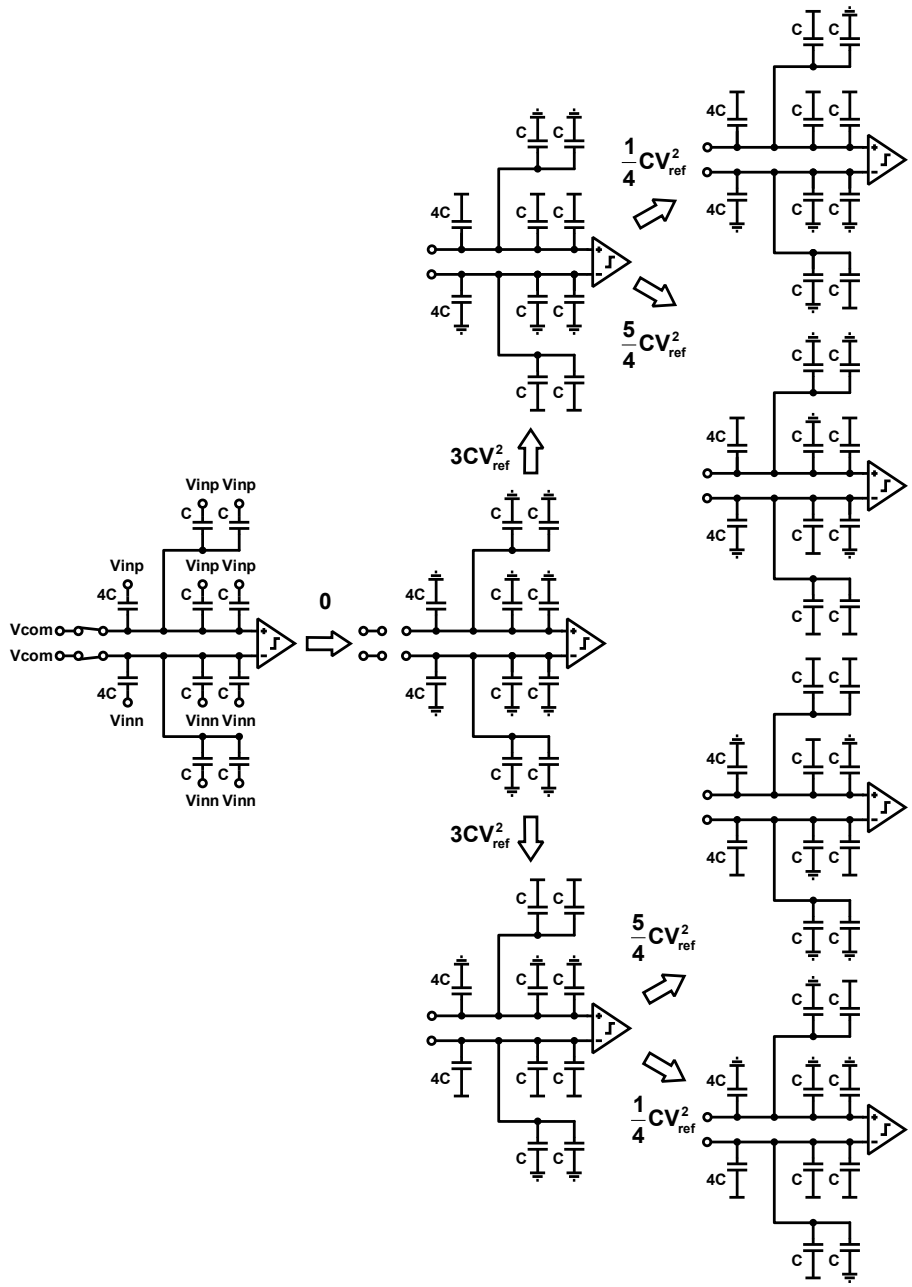


Fig. 2.7 Energy-saving switching algorithm.

2.2.5 SET-AND-DOWN SWITCHING

Fig. 2.8 shows the operation of the set-and-down switching algorithm [27]. It samples the inputs on the top plates (top-plate sampling), while the bottom plates are charged with V_{ref}. As the top plates directly hold the input voltages, the MSB is found right away. Since then, the switches are thrown to 0 one by one, so monotonic down transitions take place only, which accounts for energy reduction. Another advantage comes from that it switches on one side only at a time. Thus for an N-bit ADC, it only requires a total of 2^{N-1} unit capacitors, reducing the DAC area by half. The adoption of the algorithm achieves an 81% power reduction from the conventional switching.

This algorithm has two drawbacks, however. One is the parasitic effect due to the different initial and final voltages on the top plates like the case of the energy-saving switching. The initial voltages on the top plates on both positive and negative sides are V_{inp} and V_{inn}, respectively, and they drop monotonically during the conversion phase, resulting in distortion. The second problem is that the input common mode of the comparator changes in each conversion cycle. This alters the offset of the comparator in every conversion cycle, hence degrades the linearity performance. The comparator design can be difficult to prevent the performance degradation.

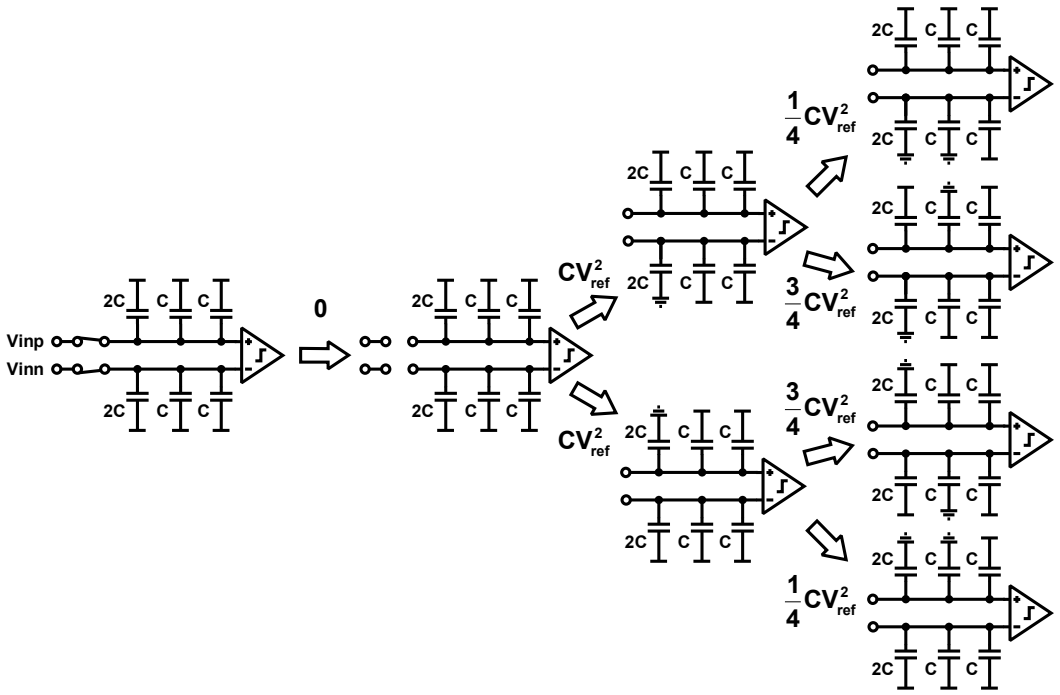


Fig. 2.8 Set-and-down switching algorithm.

2.2.6 MERGED-CAPACITOR SWITCHING

The conspicuous property of the merged-capacitor switching (Fig. 2.9) is the employment of V_{com} as an additional reference [28]. This category of using three reference levels is often designated in other literature as the tri-level [29], [30] or Vcm based [31], [32] switching. This algorithm also uses the top-plate sampling, thus no energy is consumed in the first cycle of the conversion phase. In the sampling phase, V_{com} is applied onto all bottom plates. In the conversion phase, the switches are thrown to

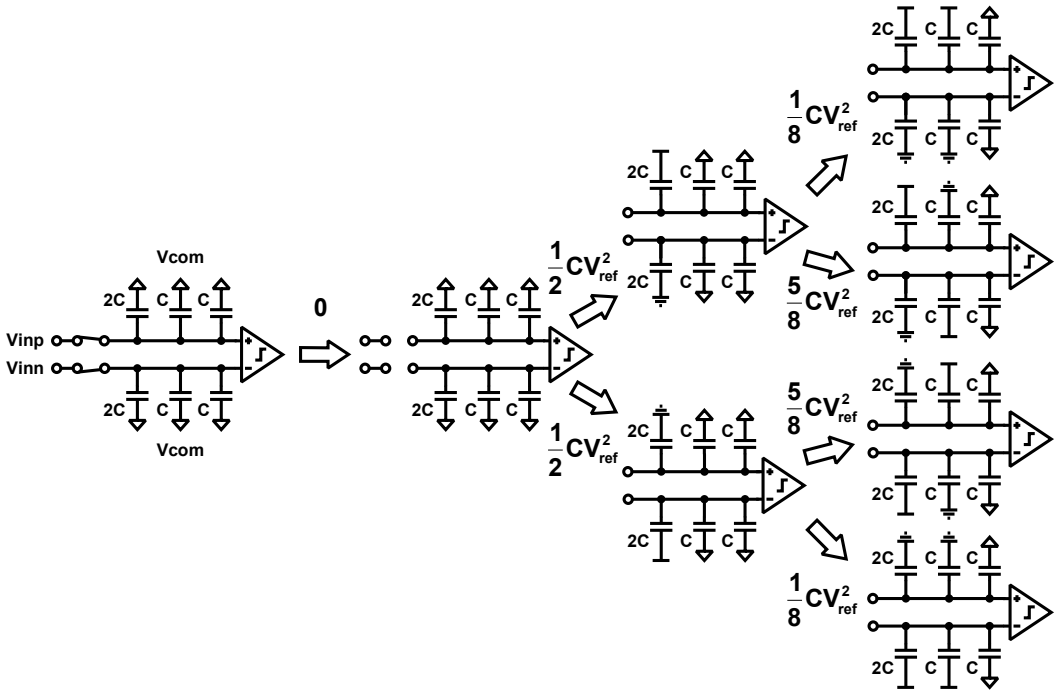


Fig. 2.9 Merged-capacitor switching algorithm.

either V_{ref} or 0 according to the comparison results. The switching on the positive side is complementary to that on the negative side, so that the input common mode of the comparator is held at V_{com}, easing the comparator design. The advantages of the algorithm are as follows. First, the use of three reference levels reduces the number of capacitors by half, therefore the energy consumption is greatly reduced. Second, since the capacitors are charged or discharged by the voltage half of V_{ref} (i.e. V_{com} to V_{ref} or V_{com} to 0, not 0 to V_{ref} or V_{ref} to 0), the energy dissipation is further reduced. Compared to the conventional switching, the merged-capacitor switching consumes 94% less energy. Third, the implementation of the logic is even easier than the conventional switching.

The primary drawback of introducing an additional reference is that its matching

with the other reference levels affects the linearity. An inaccurate V_{com} with respect to the other references produces large spikes on the differential nonlinearity (DNL) waveform. The parasitic effect due to the top-plate sampling also plays a role, whereas bottom-plate-sampling variants get around this problem [33], [34]. There are attempts to further reduce energy from the merged-capacitor switching by switching only one side [30] or integrating the monotonic approach into it [32], at the expense of respective problems introduced by the additional elements, e.g. the variable input common mode of the comparator, which has been discussed in Subsection 2.2.5.

2.3 OFFSET AND NOISE

Fig. 2.10 shows the StrongARM latch [35], [36], which is the most prevalent dynamic comparator structure used in SAR ADCs. Its popularity is attributed to simple design, fast speed, and no static power consumption. Also it can generate rail-to-rail outputs [36]. The detailed operation principle is referred to [36]. Both offset and thermal noise issues appear in the comparator design. The offset arises from the mismatch among the devices, thus increasing the device sizes can be a solution. The most critical devices to the input-referred offset are the input devices, since they act as an amplifier in the early stage of the operation [36], [37]. For the input-referred thermal noise, the input devices are the most critical by the same token. The thermal noise can be reduced by increasing the device sizes, too. The transistors constituting the latch contribute little to noise

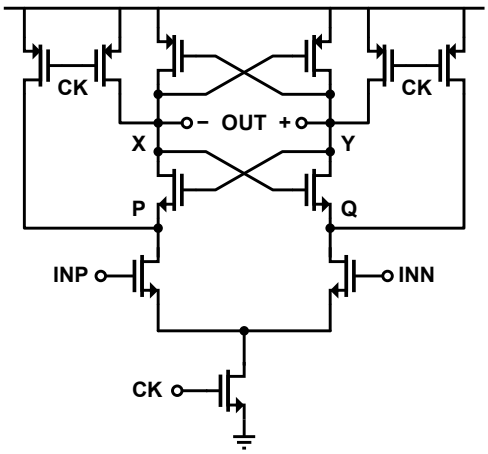


Fig. 2.10 StrongARM latch.

because nodes P, Q, X, and Y are periodically reset. Detailed analysis for this is referred to [38]. Calibration of the output capacitance can address the offset, too [38], [39]. Fig. 2.11 shows the schematic diagram. Another more popular approach is to add a preamplifier before the dynamic latch [37], as shown in Fig. 2.12. The preamplifier greatly cuts down the offset by its gain, however it consumes static power energy, which is so large that the SAR ADC loses its strength in low power consumption.

Kickback noise arises between the CDAC and comparator (Fig. 2.13(a)). The footer device of the comparator receives a clock through its gate. As the node is coupled with

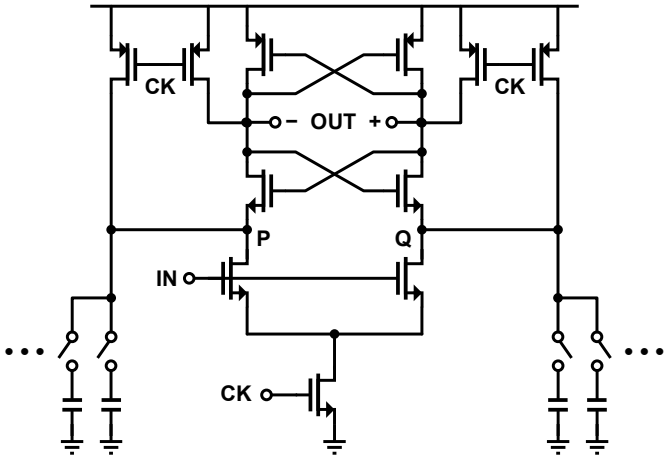


Fig. 2.11 Calibration for the offset cancellation.

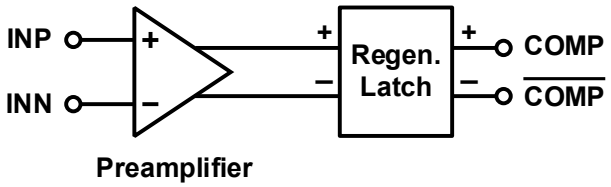
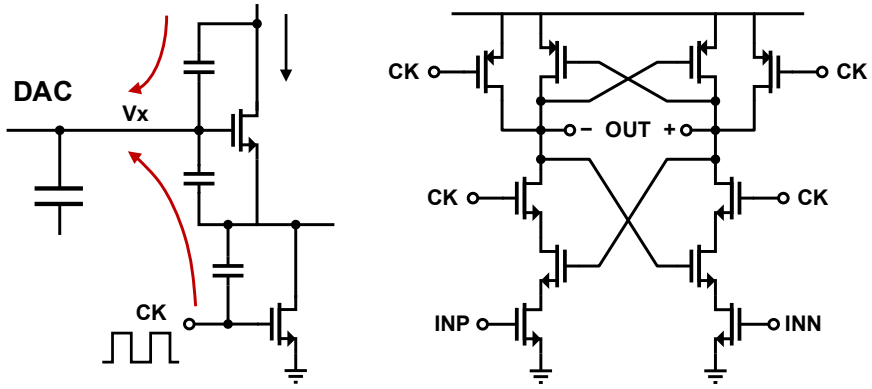


Fig. 2.12 Comparator block diagram composed of a preamplifier and a regenerative latch.

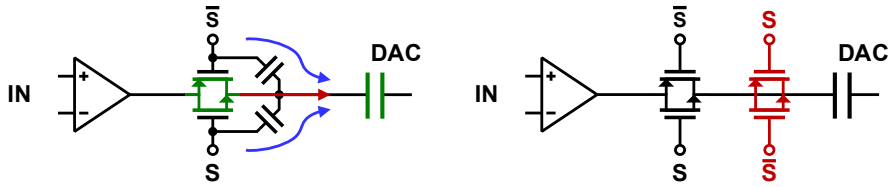
the CDAC output node, charge moves over the coupled capacitor to the CDAC and contaminates the sampled charge. A modified topology can address the kickback noise (Fig. 2.13(b)) [36], [40]. The drawback is the increased offset because the input devices operate in the linear region when they are in the amplification mode [36].

The switches and the CDAC are also noise sources as illustrated in Fig. 2.14. As they form a switched capacitor circuit, the average power of the thermal noise is kT/C [41], [42]. It provides a guideline for the minimum capacitor size for a given noise specification. Increasing the capacitor size achieves noise reduction and higher resolution, but it increases the area, settling time, and switching power consumption. Clock feedthrough arises from the switching operation of the switch through the overlap capacitance. It induces a constant offset on the voltage with a ratio of the overlap capacitance (C_{OV}) and the sampling capacitance plus C_{OV} [41], [42]. The turn-off of the switch causes charge injection, which is approximately half of the charge on the channel [41], [42]. Using a transmission gate switch (Fig. 2.14(a)) can mitigate the problems but it cannot cancel them out without precise control [41], [42]. Using too large a size for the switch is discouraged (a tradeoff between speed and precision [42]). Using a dummy switch is a solution for a single transistor switch [41], [42] but it may be applied to a transmission gate switch as well (Fig. 2.14(b)). For the switches to the references, a single transistor suffices (a PMOS for V_{ref}, an NMOS for 0) because the reference levels are fixed.



(a) (b)

Fig. 2.13 (a) Kickback noise and (b) a solution by a modified topology.



(a) (b)

Fig. 2.14 (a) kT/C noise (green), clock feedthrough (blue), and charge injection (red); (b) Dummy switch to prevent charge injection.

2.4 LINEARITY

Good device matching is crucial for linearity. The capacitors and switches must be well matched to maintain the binary weights. The matching of capacitors and transistors follow Pelgrom's model (Fig. 2.15) [43], [44]. Increasing the sizes of the capacitors and switches will improve matching at the expense of more switching energy, more clock feedthrough, and more charge injection. Adoption of calibration enables to keep the capacitance small while the static error due to mismatch is reduced by the calibration. However, its implementation usually requires a complex digital system, which is often a processor to run a calibration algorithm [33].

Fig. 2.16 illustrates that the CDAC operates as parallel switched capacitors and the settling error dwindles exponentially with time. For linearity, the final error at each bit must be kept equal, i.e. all RC time constants are equal. Therefore, the switches must be

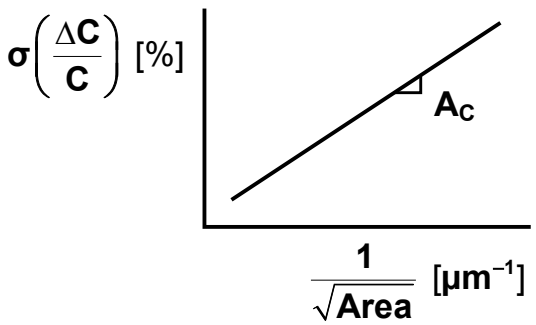


Fig. 2.15 Pelgrom model profile. Coefficient A_C is a technology-dependent parameter.

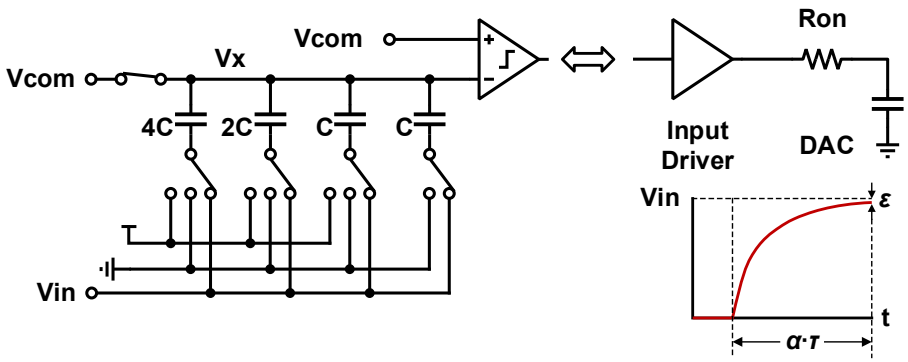


Fig. 2.16 Schematic diagram of a CDAC and a comparator. The DAC operates as parallel switched capacitors in the sampling phase.

well matched. Also long settling time is essential for high resolution and accurate results. One way to obtain both speed and accuracy is to employ redundancy. It provides error tolerance by mapping multiple raw codes to a single true code, but at the cost of more steps than the resolution and more complicated hardware [45]. Fig. 2.17 illustrates an example of error tolerance of redundancy against error-intolerant binary search employed by a SAR ADC without redundancy. Redundancy enables to shorten the time for each bitcycle as far as the increased settling error. Considering the exponential nature of the settling error, the sampling period can be shortened even though redundancy introduces extra steps.

It is customary in layout that, in order to address the first-order global mismatch generated during the process, the capacitor array is designed as a common centroid arrangement of multiple unit capacitors [24], [46]–[51]. A common centroid arrangement, however, makes routing among the capacitors intricate, thus the resultant interconnect parasitics are large [49] and difficult to control. Sometimes the interconnect parasitics for

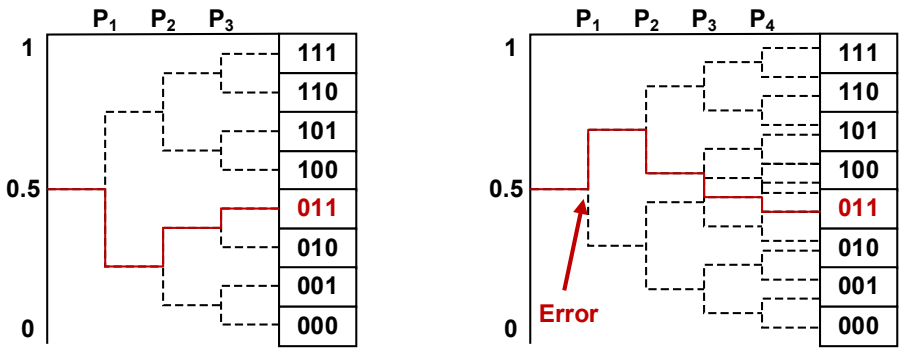


Fig. 2.17 Error tolerance of redundancy.

common centroid arrangement can be a major source of nonlinearity [50], [51].

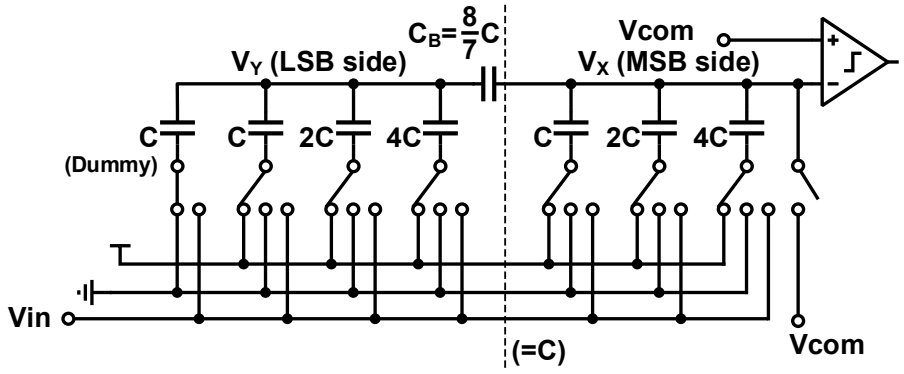
Parasitic capacitance at the CDAC output node affects linearity, too. The parasitic capacitor joins in sampling with the nominal capacitors, and its charge is redistributed. If the net voltage change across the parasitic capacitor is 0, the charge contribution by the parasitic capacitor cancels out. Switching algorithms using the top-plate sampling are prone to this effect, as reviewed in Section 2.2. If the top-plate sampling should be adopted in design, the parasitic effect should be reduced by either increasing the capacitor sizes or introducing calibration.

2.5 AREA

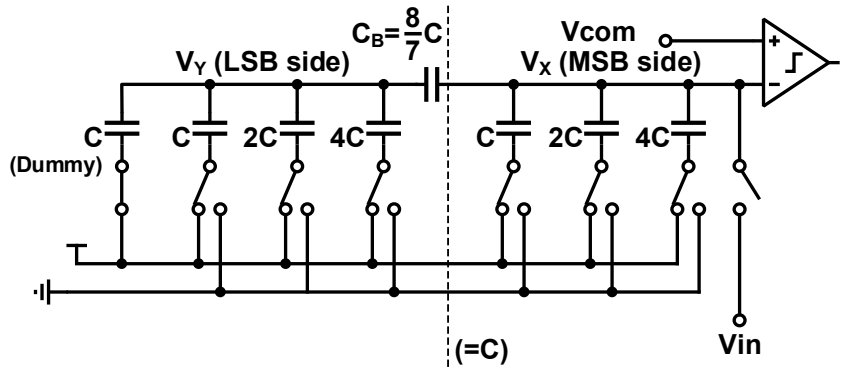
With conventional binary weighted CDAC topology, one more resolution increases the area for the capacitor array by a factor of 2, which can lead to the most area of a high-resolution SAR ADC to be assigned for the capacitors only. The segmented CDAC topology is a solution (Fig. 2.18). It inserts a bridge capacitor (C_B in Fig. 2.18) to split the capacitor array into two arrays. By carefully choosing an appropriate value for C_B, the equivalent capacitance on the LSB side in series with C_B seen from the MSB side can be the unit capacitance. Hence the MSB capacitors can be sized from the unit capacitance again. The bridge capacitor is alternatively called the attenuation capacitor from its role described above.

The segmented CDAC topology becomes more powerful in higher resolution ADC. However it comes with degraded linearity. The appropriate value for the bridge capacitor is often difficult to manufacture and match precisely because the ideal value is fractional. For example, in Fig. 2.18, C_B must be exactly 8/7 times the unit capacitance to maintain the linearity. Even a slight deviation from it is harmful. Calibration is often employed to mitigate the problem.

If the top-plate sampling is employed, the input is connected onto the MSB side, as shown in Fig. 2.18(b). The input charge is stored on the capacitors on the MSB side and the bridge capacitor. The charge on the bridge capacitor induces the charge on the LSB side. Subsection 3.3.4 deals with the computation of the sampled charge.



(a)



(b)

Fig. 2.18 Schematic diagram of a segmented CDAC with a comparator with (a) bottom-plate sampling and (b) top-plate sampling.

CHAPTER 3

ADAPTIVE SWITCHING SAR ADC FOR ECG MONITORING APPLICATIONS

3.1 ECG CHARACTERISTICS AND READOUT CIRCUIT

3.1.1 ECG SIGNALS AND CHARACTERISTICS

Fig. 3.1 presents a normal ECG signal printed on a grid. The maximum magnitude of a typical ECG signal is in the order of 1 mV [3]. Three entities of unique pattern are typically observed in normal rhythm, viz., a P wave, QRS complex, and T wave. They represent atrial depolarization, ventricular depolarization, and ventricular repolarization of the heart, respectively. Useful information for diagnosis is often found in the intervals between two curves, as depicted in Fig. 3.1. For example, RR intervals are of primary concern for diagnosis of arrhythmia.

If a term signal activity is defined as the rate of change of the signal with respect to time [52], it is noticeable in Fig. 3.1 that the signal activity around QRS complexes is very high while it is low elsewhere. As the width of the QRS complex is usually narrow,

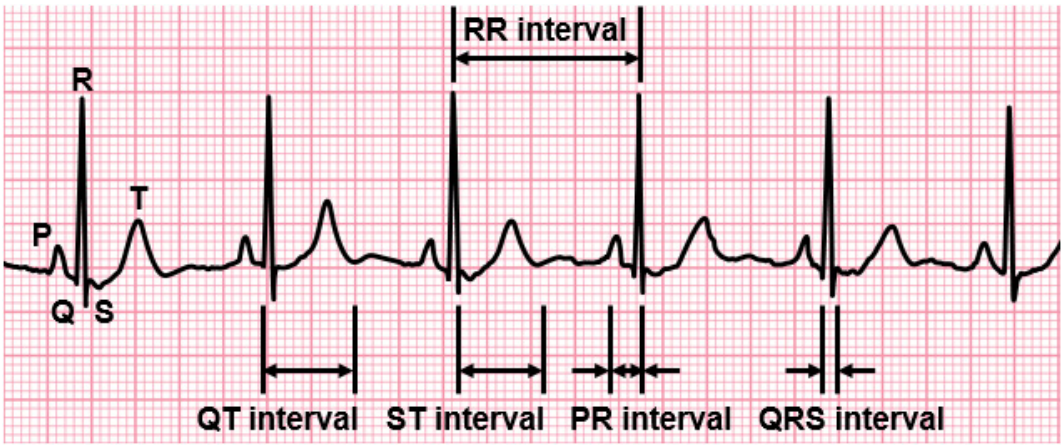


Fig. 3.1 ECG waveform (Fig. 1.1) with designations.

the mean activity is low. It is known that the fundamental frequency of the QRS complex is about 10 Hz at the body surface, and most informative content is within 100 Hz [5].

The baseline of ECG signals can wander with a low frequency. If the power line interferes with the signal, it wanders with the line frequency. Motion can also cause the baseline wander, as the impedance between the patches and skin is changed by the motion.

3.1.2 ECG Readout Circuit

It is necessary to know the design of and requirements for the readout circuit, in which an ADC is a component. Many current ECGs involve computer-based digital processing [5]. In preparation for this, the ECG input needs to be conditioned in the analog front-end (AFE) of the readout circuit beforehand. Fig. 3.2 shows a simple block

diagram of the circuit. It should be designed to comply with the standards and recommendations by the American National Standards Institute (ANSI), the Association for the Advancement of Medical Instrumentation (AAMI), and the American Heart Association (AHA). According to the recommendations, the amplitude resolution of the readout circuit should be in microvolts [5], and the allowed error tolerance is ±5% [53]. The ratio of the amplitude resolution to the maximum input magnitude indicates an ADC resolution of 10 bits is fair enough. In the first stage, the small input signal with a few millivolt magnitude is amplified, and bandpass filtering is applied. The 1975 AHA recommendations include a 0.05-Hz low-frequency cutoff for diagnostic electrocardiography [53], which preserves the fidelity of the signal [5]. The upper-frequency cutoff is recommended to be 150 Hz [5], which includes margin as the important information for diagnosis is contained within 100 Hz. The ADC should, however, sample it with a rate of a significant multiple of the upper-frequency cutoff to provide recommended bandwidth in the digitized signal [5], to ensure unequivocal results [3]. For many routine ECG recordings, a sampling rate of 1 kS/s is sufficient [3].

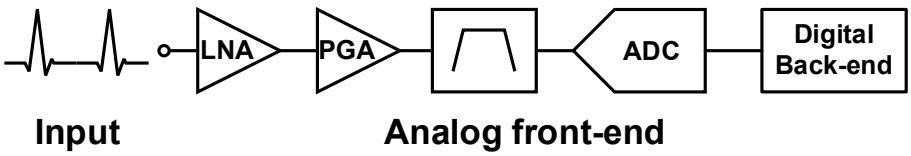


Fig. 3.2 Block diagram of an ECG readout system.

3.2 RELATED SIGNAL-SPECIFIC WORKS

There have been signal-specific approaches to reduce power consumption for similar biomedical signals. The ideas vary by the signal characteristics and requirements. This section reviews selected works and assesses its applicability to ECG monitoring.

3.2.1 SAR ADC WITH A BYPASS WINDOW FOR NEURAL SIGNALS

It is known that a neural signal is composed of action potentials and baseline noise. In a wide variety of neuroscientific and neurophysiological fields, it is the action potentials that carry the useful information [54]. A 10-bit SAR ADC with a bypass window has been proposed [54]. Parts of the input signal that exceed the window are regarded as useful action potentials, and those within the window are regarded as baseline noise (Fig. 3.3 [54]). If the signal is within the bypass window, the differential DAC output voltage falls below the window voltage in an early phase of conversion. If it is the

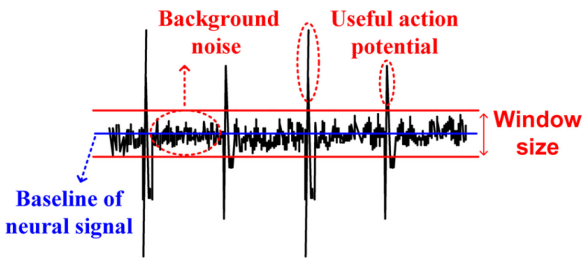


Fig. 3.3 Neural signal. © 2012 IEEE. Reprinted.

case, it is bypassed to a later phase of conversion (Fig. 3.4 [54]). With a smaller number of switching, power consumption is greatly reduced. This technique, however, may be inappropriate for ECG monitoring applications in a general sense. First, the fixed window cannot respond to the wandering of an ECG baseline. Second, it can alter the waveform around the baseline, which may cause difficulty to interpret the result. nonetheless, it may

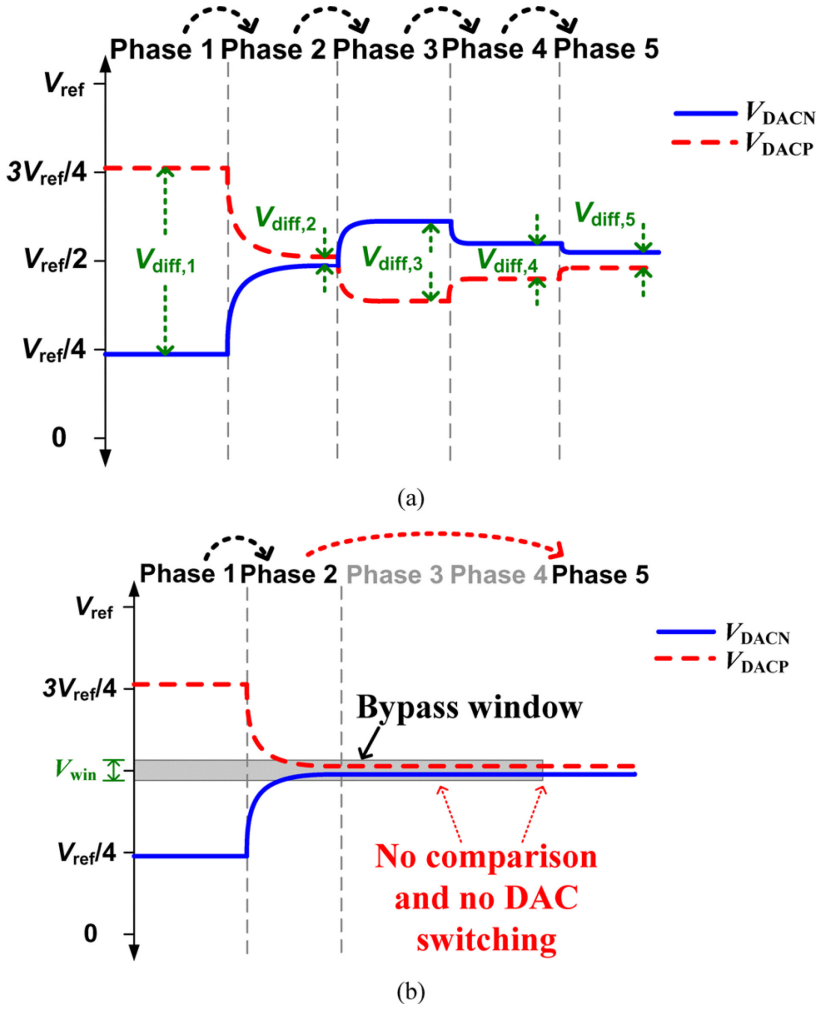


Fig. 3.4 Conversion process of (a) conventional and (b) bypass window SAR ADC.
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be applicable to detection of R peaks only for a way of arrhythmia diagnosis under restricted circumstances.

3.2.2 LSB-First Successive Approximation

This signal-specific algorithm for a 10-bit ADC aims at signals with low mean activity, which exhibit small variations but abrupt great changes occasionally [52]. ECGs are a very good candidate, and they are used for the experiment in [52]. The basic idea is as follows. Since small variations are rendered into a change of only a few LSBs, the scheme starts from the previous code and switch from the LSB toward the MSB, hence fewer bitcyles than the resolution are sufficient. If the sample has changed by a great amount, the approximation may reach to the MSB and return toward the LSB. In this case, the number of bitcycles can become greater than the resolution, and more energy is wasted than the conventional switching. Fig. 3.5 illustrates operation examples [52]. The detailed algorithm flowchart is referred to [52, Fig. 2]. However, it can enjoy power benefit against the conventional switching only for signals having a mean code variation smaller than 32, as illustrated in Fig. 3.6 [52]. The algorithm is applicable to ECG monitoring but the poor performance with highly active signals is a defect.

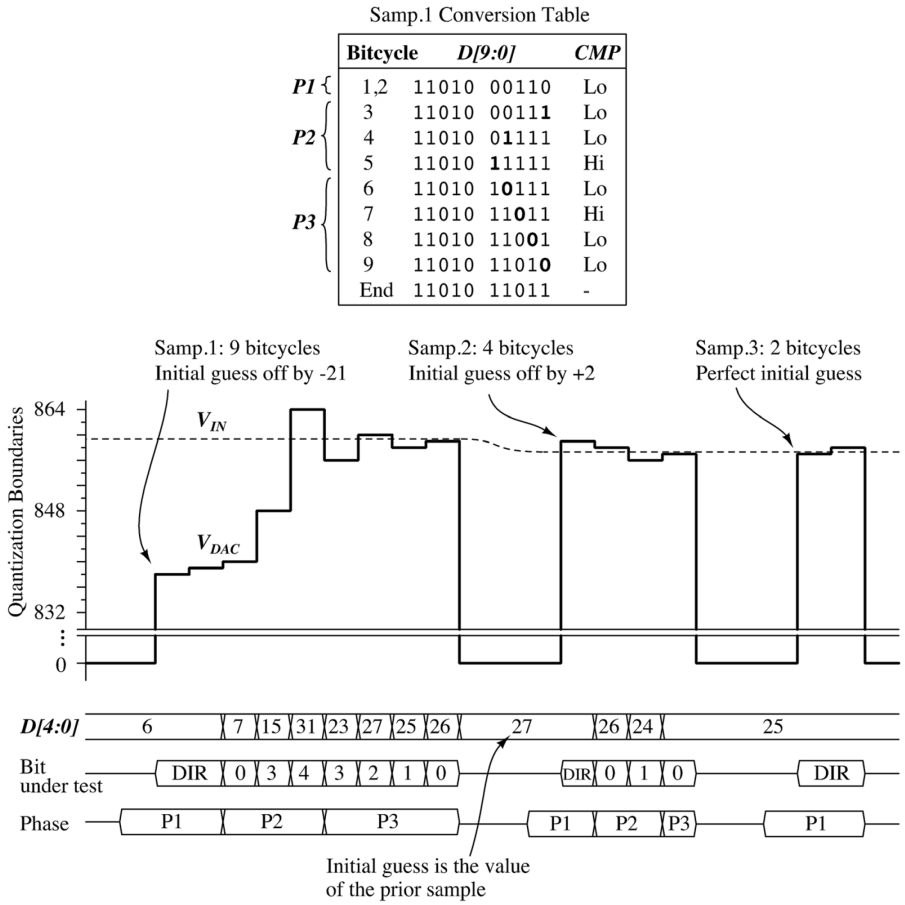


Fig. 3.5 Operation examples of the SAR ADC with LSB-first successive approximation. © 2014 IEEE. Adapted.

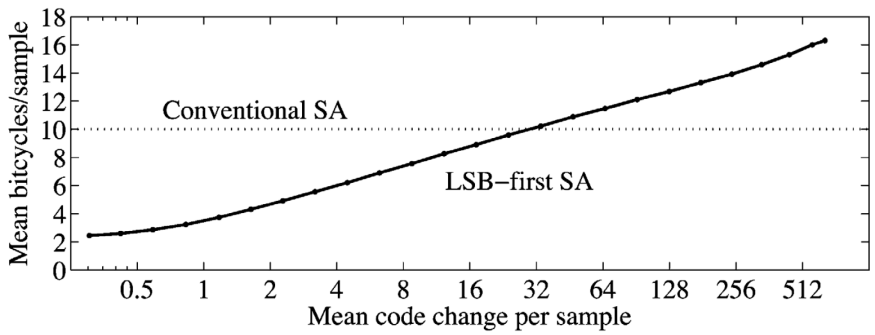


Fig. 3.6 Measured mean bitcycles/sample and mean energy consumption at f_S = 10 kHz and V_{DD} = 0.6 V. © 2014 IEEE. Adapted.

3.3 ADAPTIVE SWITCHING

In the previous chapter, various techniques to reduce the power consumption of the SAR ADC were reviewed. The tri-level switching was the most favorable as it greatly reduces the power consumption while logic implementation is easy. It will be combined with the proposed adaptive switching for greater power benefit. The adaptive switching makes use of the dichotomous signal activity of the ECG input signals in order to further reduce power consumption [23].

3.3.1 MOTIVATION

Section 3.1 reviewed the basic characteristics of ECGs. The signal activity around the QRS complex is very high while it is quite low elsewhere. This clear dichotomy in their signal activity is utilized by the proposed switching algorithm. It has two operation modes with regard to the dichotomous signal activity as shown in Fig. 3.7. The underlying idea is, when the input is highly variant, the SAR ADC operates in an ordinary manner (full switching mode); but when the input enters the low activity regime, MSBs are hardly changing, thus their switching could be safely skipped to avoid unnecessary switching energy dissipation for the MSBs (reduced switching mode).

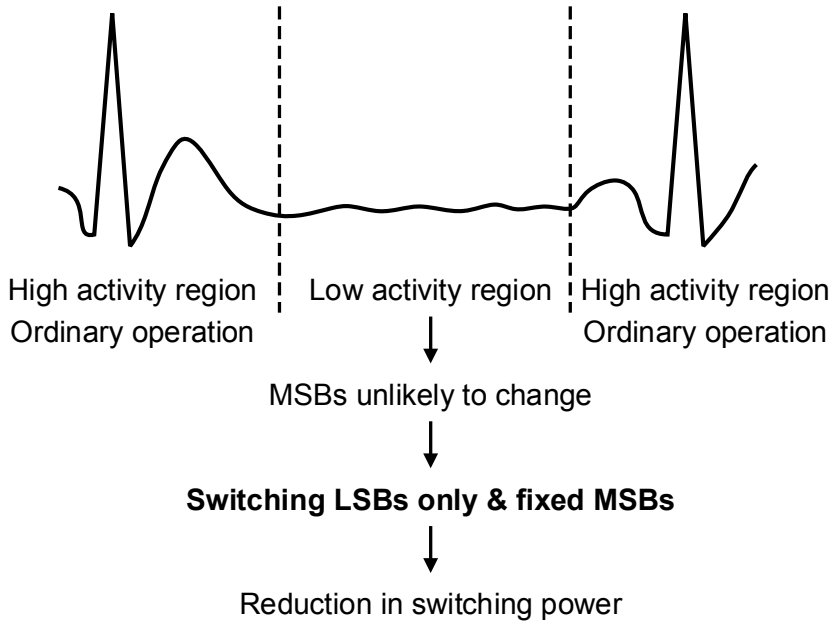


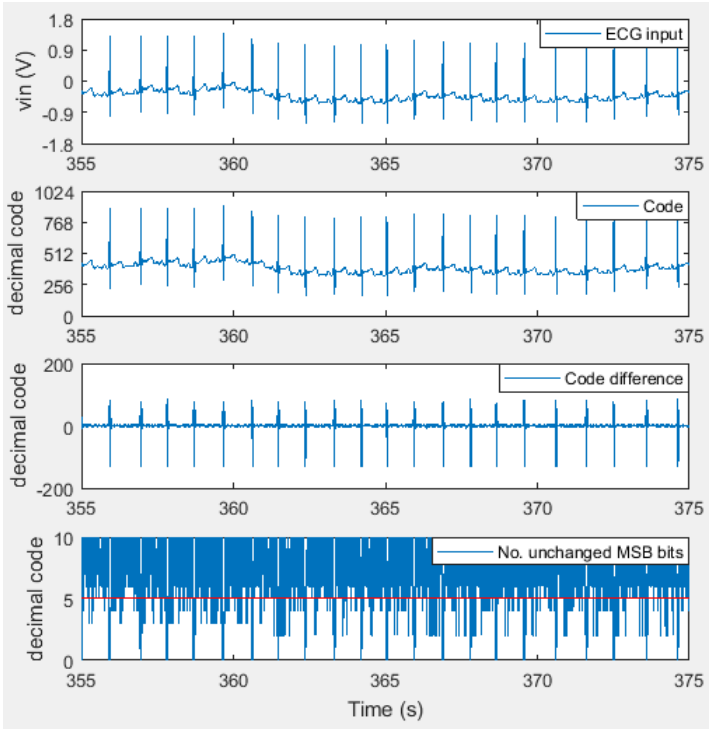
Fig. 3.7 Two-mode approach with regard to dichotomous signal activity.

3.3.2 PRELIMINARY TEST

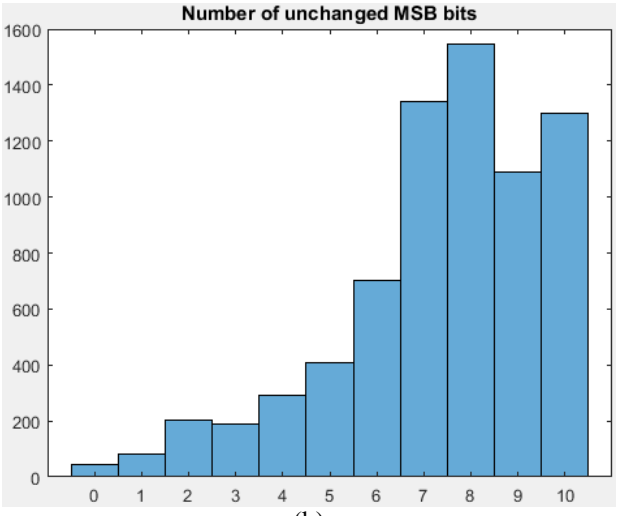
In order to investigate the actual signal activity of the ECG signals and the applicability of the above idea, a test was carried out in MATLAB using real ECG recordings obtained from the MIT-BIH Arrhythmia Database provided by PhysioNet [55], [56]. The database has established real ambulatory ECG recordings collected from 47 subjects, who are a mixed population of inpatients and outpatients [56]. In the test, two recordings were selected from the database, and converted to 10-bit digital code sequences and, for each clip, the number of unchanged MSB bits in every pair of adjacent digital codes was obtained.

The selected recordings were Records 105 and 115. Since the records were too long (30 minutes), the 20-second sample of interest was clipped off each record. The clip from Record 115 represents normal rhythm, while the clip from Record 105 represents an artifact by noise. Assuming that an amplifier in the front end to be used with the proposed ADC in the system would amplify the input with a fixed gain, the clips were linearly scaled with the gain. As the original records mostly display a signal range of roughly ±2.5 mV, the artificial gain was chosen to be 720 to amplify the range to ±1.8 V, which is the maximum range of the differential input to the proposed SAR ADC designed at a 1.8-V supply voltage. The scaled clips were converted to 10-bit digital code sequences as stated above, and for each case, every pair of adjacent codes was compared and the code difference was computed and the number of unchanged MSB bits was obtained.

Fig. 3.8(a) shows the results of the test with the normal signal. The first panel displays the scaled clip and the second shows its 10-bit digital code version in decimal representation. The difference in every pair of adjacent codes is exhibited on the third panel. As expected, large code differences are observed around the QRS complexes. From the comparison between every pair of adjacent codes, the number of the unchanged MSB bits can be obtained. The result is shown on the last panel, and its histogram is presented in Fig. 3.8(b). In the same fashion, the test results with the abnormal noisy signal are shown in Fig. 3.9. Both extreme but realistic cases reveal a tendency of relatively more counts of high numbers of unchanged MSBs, which would imply that this general tendency holds for most of real signals. However, the test results do not provide a clear

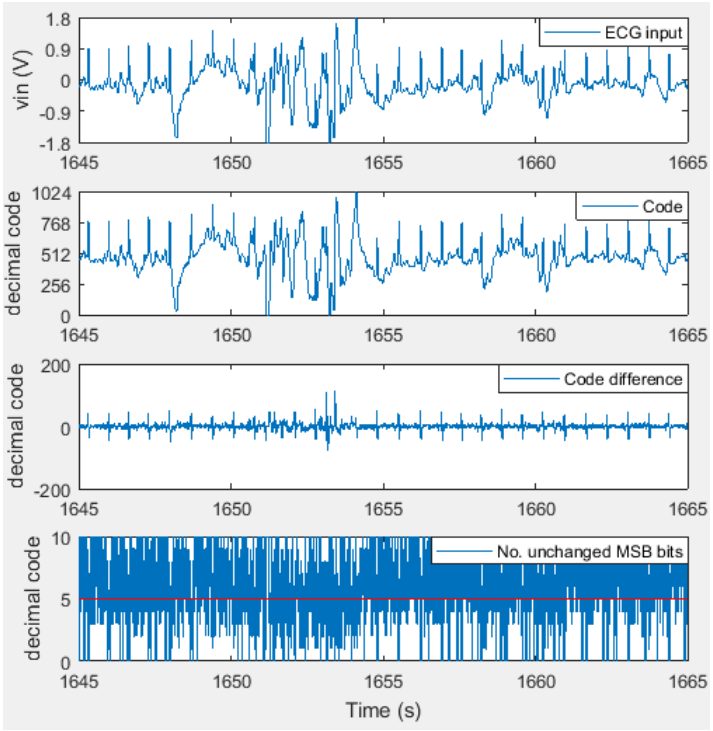


(a)

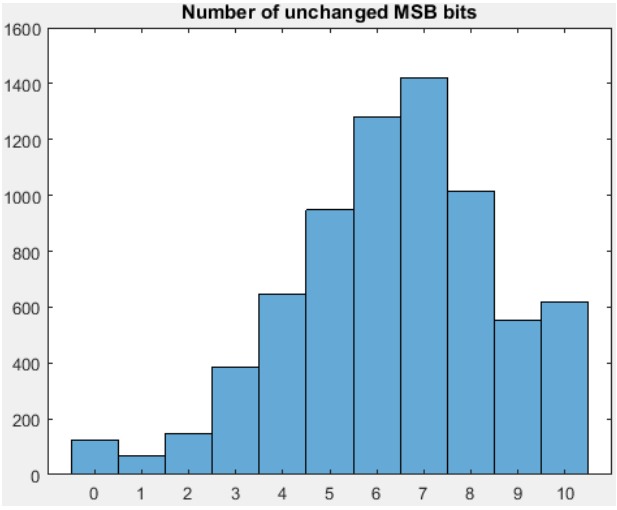


(b)

Fig. 3.8 Signal activity test with a normal ECG recording in MATLAB (a) code difference and number of unchanged MSB bits, and (b) histogram of the number of unchanged MSB bits.



(a)



(b)

Fig. 3.9 Signal activity test with an abnormal noisy ECG recording in MATLAB (a) code difference and number of unchanged MSB bits, and (b) histogram of the number of unchanged MSB bits.

basis to determine how many MSB bits should skip switching in the operation mode for the low activity region, as Figs. 3.8(b) and 3.9(b) do not show a clear boundary between the high and low activity regions. It is easily inferable that the results would vary with respect to the position of the baseline and the magnitude of the signal, so that the optimum boundary does not exist in the perspective of signal activity only. Nonetheless, it could be found in terms of optimum power consumption instead. Let K be the number of the MSB bits to skip switching in the low active region. If a high value is chosen for K, low switching power consumption can be obtained in a single reduced-switching-mode operation, but entering the mode happens on relatively rare occasions; if K is a low value, the power benefit in reduced switching mode is little but it will operate frequently in the mode. This tradeoff in the decision of K is the motivation of another test with a SAR ADC model that implements both the proposed algorithm and the computation of the switching energy consumption.

3.3.3 ALGORITHM

The adaptive switching algorithm [23] has two operation modes, viz., full switching mode and reduced switching mode. In full switching mode, all 9 capacitors are switched for conversion like an ordinary 10-bit tri-level SAR ADC. In reduced switching mode, the K MSB capacitors are not switched, assuming that the K-bit MSB code does not change from the previous one. The rest $(9 - K)$ capacitors are switched for conversion. Such an

operation is achieved by employing a modified sampling and switching scheme that samples just the (10 – *K*)-bit LSB portion of the input using the previous MSBs and resolves it. In order to apply this switching technique to the CDAC, adoption of the top-plate sampling is inevitable.

Figs. 3.10 and 3.11 illustrate the sampling and conversion operations in full and reduced switching modes, respectively [23]. The segmented CDAC topology is used for area reduction. The terms MSB section and LSB section are introduced to mean the *K*-bit MSB section and (10 – *K*)-bit LSB section, and distinguished from MSB side and LSB side denoting the physically divided top plates in the segmented CDAC topology. For

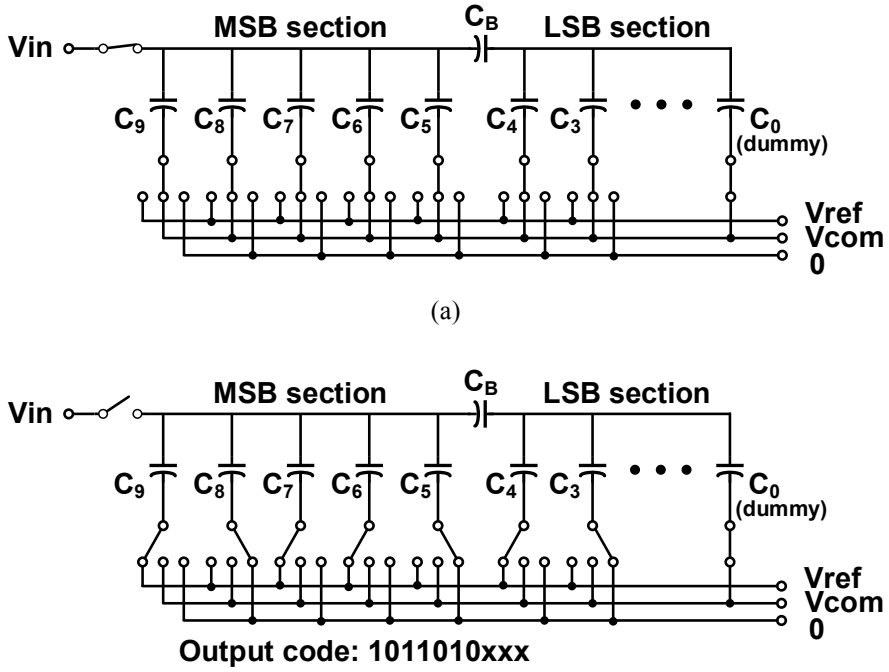


Fig. 3.10 CDAC in full switching mode: (a) sampling phase and (b) conversion phase.

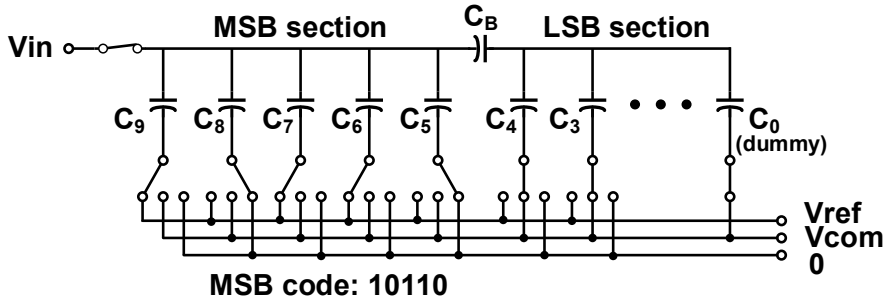
convenience, $K = 5$ is assumed in all figures in this subsection.

The total charge sampled on the capacitors $Q_{\text{samp,F}}$ in full switching mode is computed by the law of conservation of charge as

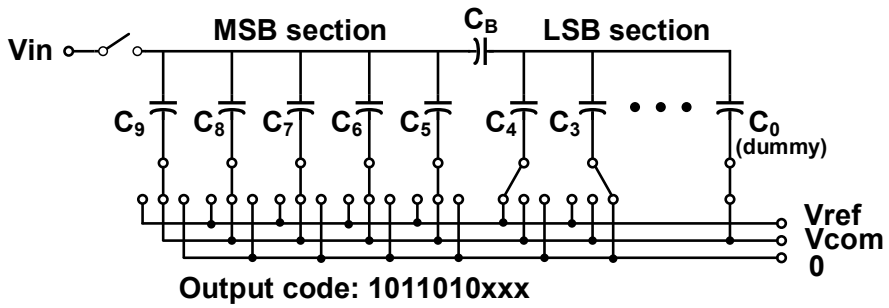
$$Q_{\text{samp,F}} = \sum_i C_i \left[V_{\text{in}} - V_{\text{bot}}(i) \right]$$

$$= \sum_{i=0}^{9} C_i V_{\text{in}} - \sum_{i=0}^{9} C_i V_{\text{com}} \tag{3.1}$$

where C_i is the capacitance of ith bit, V_{in} is the input voltage, $V_{\text{bot}}(i)$ is the voltage on the



(a)



(b)

Fig. 3.11 CDAC in reduced switching mode with $K = 5$: (a) sampling phase and (b) conversion phase. © 2017 IEEE. Adapted.

bottom plate of C_i, and V_{com} is the common-mode voltage (Fig. 3.10(a)). The first term on the right side of (3.1) indicates the sampled input, and the second term is a static offset term due to all $V_{bot,i} = V_{com}$ in the sampling phase. This analysis applies to any conventional tri-level SAR ADC. The conversion proceeds like an ordinary SAR ADC as shown in Fig. 3.10(b).

In reduced switching mode, the input is sampled while the bottom plates of the K MSB capacitors are connected to the reference sources corresponding to the previous K-bit MSB code. The total charge sampled on the capacitors $Q_{samp,R}$ is expressed as

$$Q_{samp,R} = \sum_{i=0}^{9-K} C_i \left(V_{in} - V_{com}\right) + \sum_{i=10-K}^{9} C_i \left[V_{in} - V_{bot}(i)\right], \tag{3.2}$$

where $V_{bot}(i)$ are the preset MSB voltages (Fig. 3.11(a)). Equation (3.2) can be rearranged as

$$Q_{samp,R} = \sum_{i=0}^{9} C_i V_{in} - \sum_{i=10-K}^{9} C_i V_{bot}(i) - \sum_{i=0}^{9} C_i V_{com}. \tag{3.3}$$

Like in (3.1), the last term on the right side of (3.3) is the static offset term, and the rest terms indicate that, the sampled quantity equals the input voltage minus the voltage corresponding to the K-bit MSB portion. If the previous MSB code is correct, i.e. equal to the *true* MSB code of the input, the sampled quantity will be just the (10 – K)-bit LSB portion. The *partial sampling* is achieved thus. In the conversion phase, the sampled charge must be treated as though it were stored and redistributed in a (10 – K)-bit CDAC to resolve it in (9 – K) bitcycles. This effect is realized by throwing the MSB switches to V_{com} in the first conversion cycle. A qualitative explanation for this is that it nullifies the

MSB portion added in the DAC output (V_X) upheld by $V_{bot}(i)$ in the sampling phase. It shifts V_X back to the common mode level for appropriate comparison with the common mode. Note that the switch connections of the MSB section for the reduced switching mode is opposite to those for the full switching mode. At the end of the conversion, V_X naturally converges to V_{com}, hence the charge stored in the MSB section ends up minimal.

An extra function is needed to determine the operation mode for each period and to change mode adaptively. Both full and reduced switching modes need to watch whether the *K*-bit MSB code is changing, but the realization differs in them.

In full switching mode, the MSB code can be directly watched and tracked. The ADC keeps running in full switching mode while the MSB code is changing. If it is not changing over a number of periods, it is highly likely the case that the signal activity of the input has subsided enough and this low activity will be kept for a while, considering the characteristic dichotomy in the signal activity of ECG signals. Therefore, it is reasonable to switch to reduced switching mode. This function in full switching mode is called MSBs tracking. Its operation is depicted in Fig. 3.12 [23]. It tracks the *K*-bit MSB code of every sample and checks equality between the previous and current MSB codes.

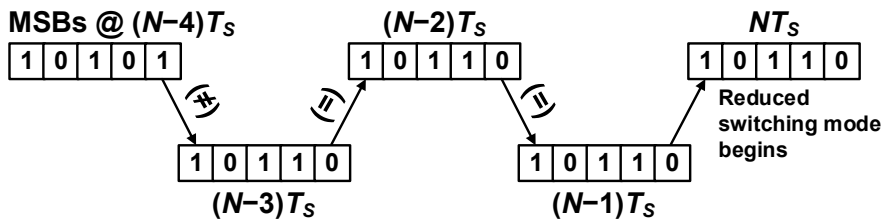


Fig. 3.12 Operation example of MSBs tracking with $K = 5$. © 2017 IEEE. Reprinted.

If three consecutive MSB codes are equal, the operation mode changes to reduced switching mode. This arbitrary number was chosen based on the following guess: if the three latest MSB codes are equal, the average signal activity may have fallen to a level lower than the half of the range determined by a single MSB code ($2^{10-K}/2$); in other words, three or more periods are taken to traverse the range with that signal activity, as illustrated in Fig. 3.13 for comprehension. Moreover, the signal activity may drop further as it has been decreasing. If so, the ADC will run in reduced switching mode for a while. Of course the guess is perfect by no means. It is possible that the MSB code changes in the fourth sample and, if it happens, the ADC runs with a wrong MSB code and produces an error. It may appear safer to wait for more samples with the same MSB code. However, given the randomness exhibited enough in the preliminary test, this option will not completely rule out error occurrences. Rather, it will make the implementation more complicated. Moreover, the value of K exercise more significant influence on the incidence and magnitudes of errors.

In reduced switching mode, the true MSB code cannot be directly watched. Instead, the evolution of the (10 – K)-bit LSB code is utilized to predict whether the true MSB

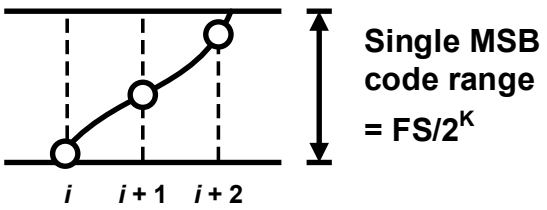


Fig. 3.13 Worst case before entering reduced switching mode with three-sample-equality-check.

code will change in the next period. The code difference mostly arises within the LSB code because the signal activity is low. The next LSB code is estimated as the linear extrapolation of the two latest LSB codes. If it overflows or underflows, it means that the estimated next code has a different MSB code, indicating that the true MSB code will change in the next period, therefore the ADC switches to full switching mode to cope with it. Fig. 3.14 depicts an example of the operation of LSBs extrapolation [23]. This approach is simple and easy to implement, but at the expense of possible occurrence of errors. Fig. 3.14 deliberately illustrates the inaccurate prediction of the LSB code. The accurate prediction of the LSB code is not of interest, but the inherently limited accuracy of linear extrapolation can lead to a wrong judgment. If the true MSB code changes while it is predicted not to do, the digital output is produced with the wrong MSB code, giving rise to an error. The partial input sampled with the wrong MSB code is beyond the range that can be represented by any (10 – K)-bit code, hence the LSB code becomes either

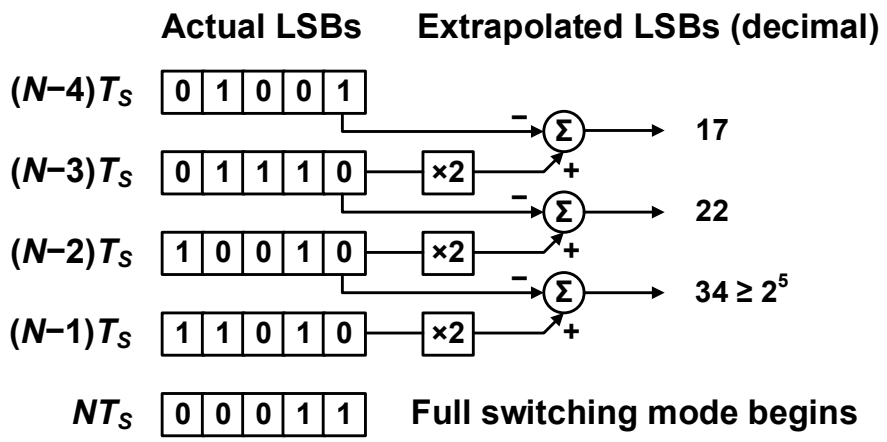


Fig. 3.14 Operation example of LSBs extrapolation with K = 5. © 2017 IEEE. Reprinted.

00…0 or 11…1. If the LSB code is detected to be either, the operation mode is changed to full switching mode to prevent further error occurrences. This algorithm allows error, but the amount should be kept tolerable ($|\varepsilon| < 5\%$ [53]). As stated above, the choice of K affects the magnitudes and frequency of the errors.

The adaptive switching algorithm described so far can be expressed as a flowchart like shown in Fig. 3.15. The default mode is full switching mode: if the ADC is just activated or reset, it first runs in the mode.

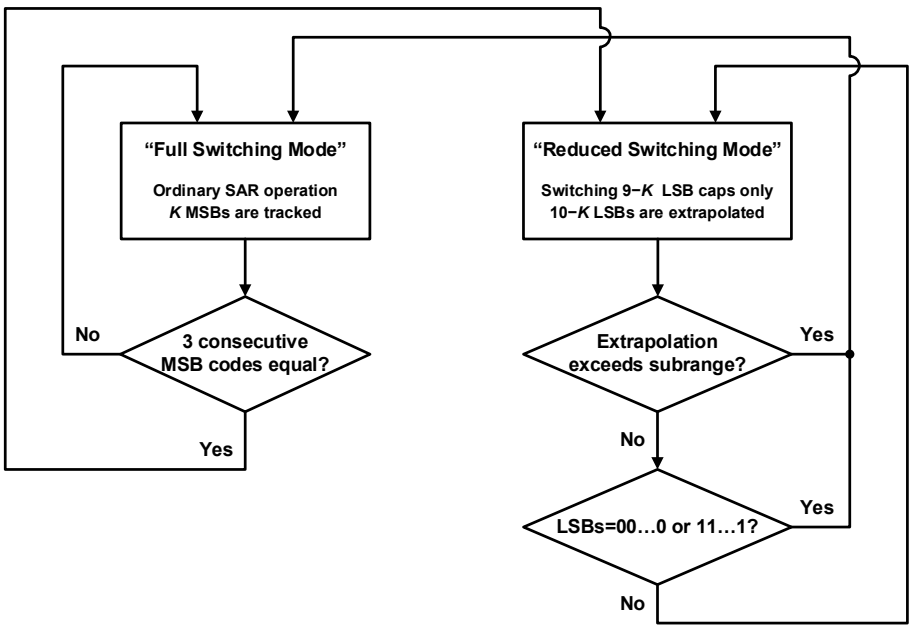


Fig. 3.15 Flowchart of the proposed adaptive switching scheme. © 2017 IEEE. Adapted.

3.3.4 ENERGY CONSUMPTION OF SAR ADC WITH SEGMENTED CDAC

The behavioral model of an *N*-bit SAR ADC that implements the proposed adaptive switching with variable *K* and the detailed computation model of switching energy consumption was developed in MATLAB to verify the proposed algorithm and determine the value for *K*. The model computes the switching energy consumption for a single period based on the same principle introduced in Subsection 2.2.1, but the computation for the segmented CDAC topology is much more complicated because of the presence of a series capacitor between the two floating nodes. Therefore the formula specific to this topology needs to be derived from scratch. Fig. 3.16 shows a schematic diagram of a top-plate sampling segmented CDAC. The bridge capacitor splits the top plate node into two, of which the one on the LSB side (V_Y) remains always floating. The other on the MSB side (V_X) is floating in the conversion phase, but is connected directly to the input in the sampling phase ($V_X = V_{in}$). By the discrete-time nature of switching, every voltage is expressed as a discrete-time sequence with time index *i*. All voltages on the bottom plates are independent variables that become V_{refp}, V_{com}, or V_{refn} in the *i*th cycle by the algorithm

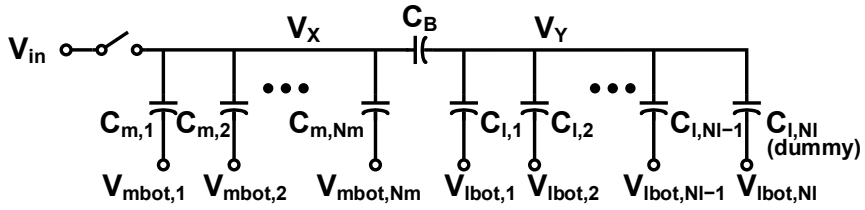


Fig. 3.16 Schematic of the split CDAC

and the input. With those known values, the unknown floating node voltages, V_X and V_Y, are computed by the law of conservation of charge. In this way, all voltages are determined for a particular switching occasion. This procedure is repeated until the conversion is over, with the total sampled charge conserved throughout the period.

The model first creates the CDAC with the MSB capacitors $C_{m,j}$, bridge capacitor C_B, and LSB capacitors $C_{l,j}$. The 10-bit segmented CDAC model has 5 MSB capacitors (N_m = 5) and 4 LSB capacitors and one dummy (N_l = 5). Here the terms MSB and LSB capacitors should not be confused with the MSB and LSB sections in the adaptive switching, as the former are physically separated by the bridge capacitor while the latter are the algorithmically separated in the adaptive switching.

Both MSB and LSB sides are binary weighted with the unit capacitance, C_0, and the bridge capacitance has the ideal value of $16/15C_0$. The values for the capacitances can be alternatively assigned with individual values with mismatch if needed. This feature can be used in the analysis of the measured linearity.

In the sampling phase (i = 1), the sampled charge is computed from the input

$$V_X(1) = V_{\text{in}} \tag{3.4}$$

and the bottom plate voltages, which are the appropriate values determined by the operation mode. The input voltage is directly applied onto the top plates of the MSB side and the bridge, on which the corresponding charge is stored. The charge equal in magnitude and opposite in sign is induced on the opposite plates and the LSB side, as illustrated in Fig. 3.17. Since the V_Y node is floating, the charge at the node cannot change.

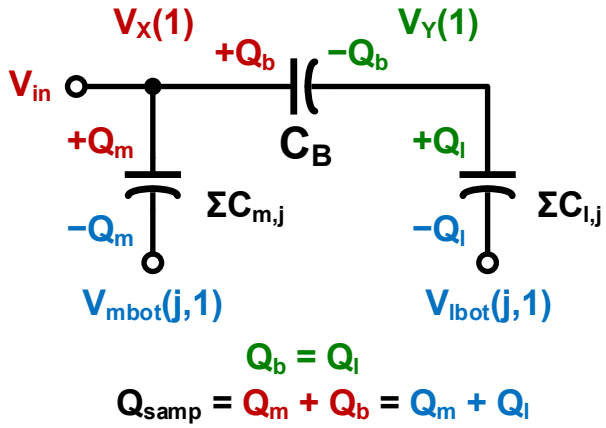


Fig. 3.17 Simplified schematic of the split CDAC in the sampling phase.

Thus the charge sampled on the bridge capacitor induces the same amount of charge on the LSB side, and this relationship holds for all time:

$$Q_B(i) = \sum_{j=1}^{N_l} Q_l(j,i), \tag{3.5}$$

where $Q_B(i)$ is the charge stored on the bridge capacitor and $Q_l(j,i)$ is the charge induced on the jth capacitor on the LSB side, both at time i. If the initial charge at node V_Y is 0, the right side of (3.5) becomes equal to the stored charge on the LSB side. Since the changes in the quantities are of interest, the initial charge at node V_Y need not be known as it cancels out in the process of taking the difference. Thus, it is assumed to be 0 without loss of generality. Equation (3.5) is alternatively expressed by

$$C_B\left[V_X(i) - V_Y(i)\right] = \sum_{j=1}^{N_l} C_{\mathrm{lsb},j}\left[V_Y(i) - V_{\mathrm{lbot}}(j,i)\right], \tag{3.6}$$

which derives

$$V_Y(i) = \frac{C_B V_X(i) + \sum_{j=1}^{N_l} C_{\text{lsb},j} V_{\text{lbot}}(j,i)}{C_B + \sum_{j=1}^{N_l} C_{\text{lsb},j}}. \tag{3.7}$$

The sampled charge Q_{samp} is given by

$$Q_{\text{samp}} = Q_{\text{tot}}(i) = \sum_{j=1}^{N_m} Q_m(j,i) + Q_B(i) = \sum_{j=1}^{N_m} Q_m(j,i) + \sum_{j=1}^{N_l} Q_l(j,i), \tag{3.8}$$

where $Q_{\text{tot}}(i)$ is the total charge and $Q_m(j,i)$ is the charge induced on the jth capacitor on the MSB side, both at time i. By the law of conservation of charge,

$$Q_{\text{tot}}(i) = Q_{\text{tot}}(i-1), \tag{3.9}$$

or

$$\begin{aligned} &\sum_{j=1}^{N_m} C_{m,j}\left[V_X(i) - V_{\text{mbot}}(j,i)\right] + C_B\left[V_X(i) - V_Y(i)\right] \\ &= \sum_{j=1}^{N_m} C_{m,j}\left[V_X(i-1) - V_{\text{mbot}}(j,i-1)\right] + C_B\left[V_X(i-1) - V_Y(i-1)\right]. \end{aligned} \tag{3.10}$$

Rearranging (3.10) gives an expression in terms of the finite differences of V_X and V_Y:

$$\begin{aligned} &\left[V_X(i) - V_X(i-1)\right]\left(C_B + \sum_{j=1}^{N_m} C_{m,j}\right) \\ &= C_B\left[V_Y(i) - V_Y(i-1)\right] + \sum_{j=1}^{N_m} C_{m,j}\left[V_{\text{mbot}}(j,i) - V_{\text{mbot}}(j,i-1)\right]. \end{aligned} \tag{3.11}$$

Substituting (3.7) into (3.11) yields

$$\left[V_X(i)-V_X(i-1)\right]\left(C_B+\sum_{j=1}^{N_m}C_{m,j}\right)=\frac{C_B^2}{C_B+\sum_{j=1}^{N_l}C_{\text{lsb},j}}\left[V_X(i)-V_X(i-1)\right]$$

$$+\frac{C_B}{C_B+\sum_{j=1}^{N_l}C_{\text{lsb},j}}\sum_{j=1}^{N_l}C_{\text{lsb},j}\left[V_{\text{lbot}}(j,i)-V_{\text{lbot}}(j,i-1)\right]$$

$$+\sum_{j=1}^{N_m}C_{m,j}\left[V_{\text{mbot}}(j,i)-V_{\text{mbot}}(j,i-1)\right], \tag{3.12}$$

which is rearranged into

$$V_X(i)=V_X(i-1)+\frac{\left(C_B+\sum_{j=1}^{N_l}C_{l,j}\right)\sum_{j=1}^{N_m}C_{m,j}\left[V_{\text{mbot}}(j,i)-V_{\text{mbot}}(j,i-1)\right]}{\left(C_B+\sum_{j=1}^{N_l}C_{l,j}\right)\sum_{j=1}^{N_m}C_{m,j}+C_B\sum_{j=1}^{N_l}C_{l,j}}$$

$$+\frac{C_B\sum_{j=1}^{N_l}C_{\text{lsb},j}\left[V_{\text{lbot}}(j,i)-V_{\text{lbot}}(j,i-1)\right]}{C_B\left(\sum_{j=1}^{N_l}C_{\text{lsb},j}+\sum_{j=1}^{N_m}C_{\text{msb},j}\right)+\sum_{j=1}^{N_m}C_{\text{msb},j}\sum_{j=1}^{N_l}C_{\text{lsb},j}}. \tag{3.13}$$

Using (3.13) and (3.7), the values for V_X and V_Y in every cycle are found. Since all capacitances and voltages are known at any instance of time, it is possible to compute the charge stored in every capacitor and the energy provided by each reference source to charge the capacitors with which it is connected, in a similar manner presented in Subsection 2.2.1:

$$E_{\text{refp}}(i) = -V_{\text{refp}} \left\{ \sum_{j \in M_P(i)} C_{m,j} \left[V_X(i) - V_{\text{refp}} \right] + \sum_{j \in L_P(i)} C_{l,j} \left[V_Y(i) - V_{\text{refp}} \right] \right\}, \tag{3.14}$$

$$E_{\text{com}}(i) = -V_{\text{com}} \left\{ \sum_{j \in M_C(i)} C_{m,j} \left[V_X(i) - V_{\text{com}} \right] + \sum_{j \in L_C(i)} C_{l,j} \left[V_Y(i) - V_{\text{com}} \right] \right\}, \text{ and} \tag{3.15}$$

$$E_{\text{refn}}(i) = -V_{\text{refn}} \left\{ \sum_{j \in M_N(i)} C_{m,j} \left[V_X(i) - V_{\text{refp}} \right] + \sum_{j \in L_N(i)} C_{l,j} \left[V_Y(i) - V_{\text{refp}} \right] \right\}, \tag{3.16}$$

where

$$M_P(i) = \left\{ j : V_{\text{mbot}}(j,i) = V_{\text{refp}} \right\}, \; L_P(i) = \left\{ j : V_{\text{lbot}}(j,i) = V_{\text{refp}} \right\},$$
$$M_C(i) = \left\{ j : V_{\text{mbot}}(j,i) = V_{\text{com}} \right\}, \; L_C(i) = \left\{ j : V_{\text{lbot}}(j,i) = V_{\text{com}} \right\},$$
$$M_N(i) = \left\{ j : V_{\text{mbot}}(j,i) = V_{\text{refn}} \right\}, \text{ and } L_N(i) = \left\{ j : V_{\text{lbot}}(j,i) = V_{\text{refn}} \right\}.$$

The total energy consumption is

$$E_{\text{tot}} = \sum_{i=1}^{N} \left[E_{\text{refp}}(i) + E_{\text{com}}(i) + E_{\text{refn}}(i) \right] \tag{3.17}$$

in full switching mode. In reduced switching mode, the conversion ends at i = N − K + 1, which replaces the upper bound of summation in (3.17).

3.3.5 BEHAVIORAL MODEL SIMULATIONS

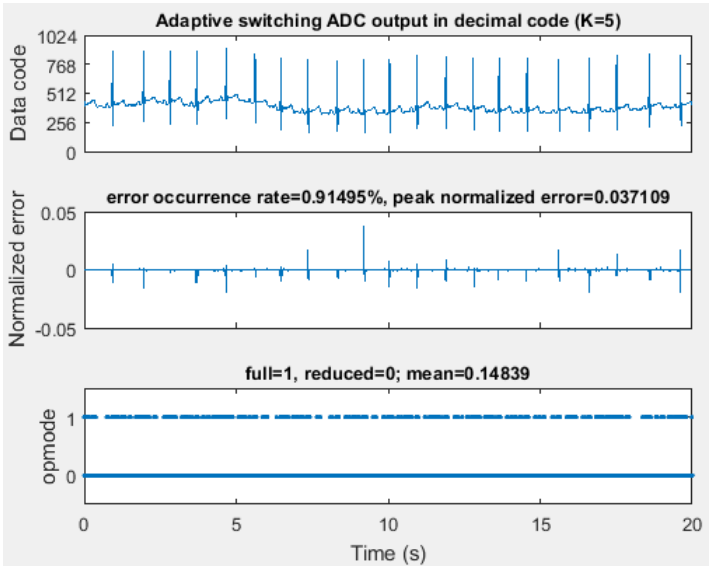
In order to verify the proposed algorithm, demonstrate the operation with realistic signals, and specify the value of K, the behavioral model was simulated with five selected ECG recordings from the MIT-BIH Arrhythmia Database (Recordings 100, 105, 106, 115,

202) [56]. As stated above, the behavioral model implements the proposed adaptive switching algorithm with variable K (Subsection 3.3.3) with the detailed switching actions in the CDAC, the evolution of the DAC output voltage, and the computation of the switching energy consumption (Subsection 3.3.4). The same value of the unit capacitance (26.6 fF) that was to be used in the chip design was used for the model. Second-order effects such as parasitics and leakage were not considered for simplicity, while the model is extendable to encompass them. The supply voltage, V_{DD}, the resolution, N, and the sampling rate, f_S, were set to 1.8 V, 10, and 1 kS/s, respectively, complying with the planned design specifications. As in the preliminary test (Subsection 3.3.2), the 20-second sample was clipped off each of the selected recordings. Each clip represents a specific diagnostic sign or artifact, i.e. normal rhythm (Recording 115), noise (Recording 105), premature ventricular contraction (Recording 100), ventricular tachycardia (Recording 106), and aberrated premature atrial contractions (Recording 202). Among those, the clips from Recordings 105 and 115 are identical to those used in the preliminary test.

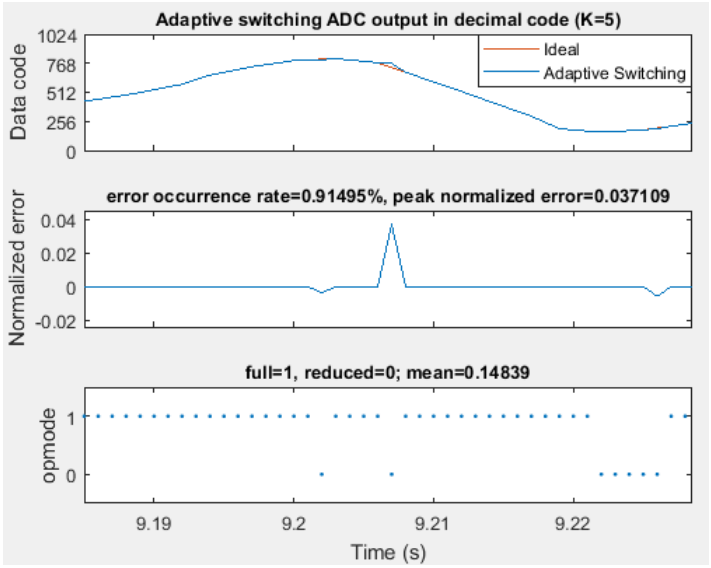
The simulations were designed to demonstrate the function of and the power benefit in the adaptive switching algorithm. The digital outputs of the model and the ideal ADC are compared. For every sample, an instance that the two ADCs give different outputs is counted as an error. The magnitudes and incidence of the errors are evaluated. In addition, the operation mode for every instance is obtained and the proportion of full-switching-mode instances to reduced-switching-mode instances is evaluated.

The first simulation checked the function of the adaptive switching for the five

inputs. The K was fixed to an arbitrary value of 5. Fig. 3.18(a) presents the simulation result with the normal rhythm input (clip from Recording 115). The outputs of both the ideal ADC and the model are presented on the first panel, but they almost overlap and the errors are invisible on the scale. The second panel shows the errors, calculated as the code difference of the two sequences and normalized to the full scale (2^{10}). About 0.91% out of all samples are erroneous. As expected, errors are mainly located near QRS complexes. The greatest normalized error was found to be 0.037109, which is within the recommended error tolerance of ±5% [53]. The third panel shows *opmode*. It is the name of a logical flag indicative of the current operation mode, being 1 in full switching mode and 0 in reduced switching mode. Hence the mean value is the indicator of the proportion of full switching mode. Statistically, the ADC operated in reduced switching mode 85.2% of the time. The zoomed-in view around the greatest error is presented in Fig. 3.18(b) to show it clearly. The error occurred due to the failure of the MSB prediction in reduced switching mode. The simulation data revealed that the three previous samples had the same MSB code (11000) which made the operation mode change to reduced switching. As the input signal fell lower than predicted by the linear extrapolation (the ideal code of the instance was 1011011010), the output code was confined within the range with the previous MSB code, and stuck at the erroneous code of 1100000000. Furthermore, the simulation results with the selected abnormal ECG samples demonstrate that the adaptive switching can work fine with any realistic ECG input. Figs. 3.19, 3.20, 3.21, and 3.22 show the simulation results with the clips from Records 100, 105, 106, and 202, respectively. As exhibited in the figures above, most errors are found around high



(a)



(b)

Fig. 3.18 (a) Behavioral model simulation result with the clip from ECG Recording 115 and $K = 5$ and (b) its zoomed-in view.

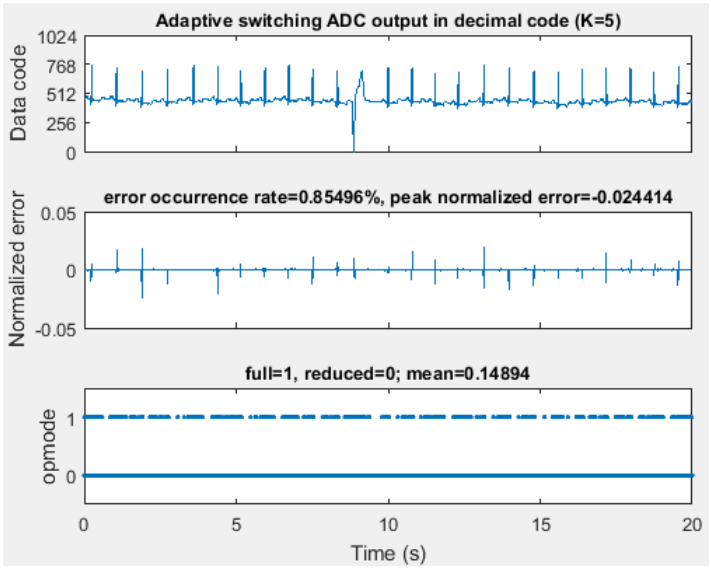


Fig. 3.19 Behavioral model simulation result with the clip from ECG Recording 100 (premature ventricular contraction) and $K = 5$.

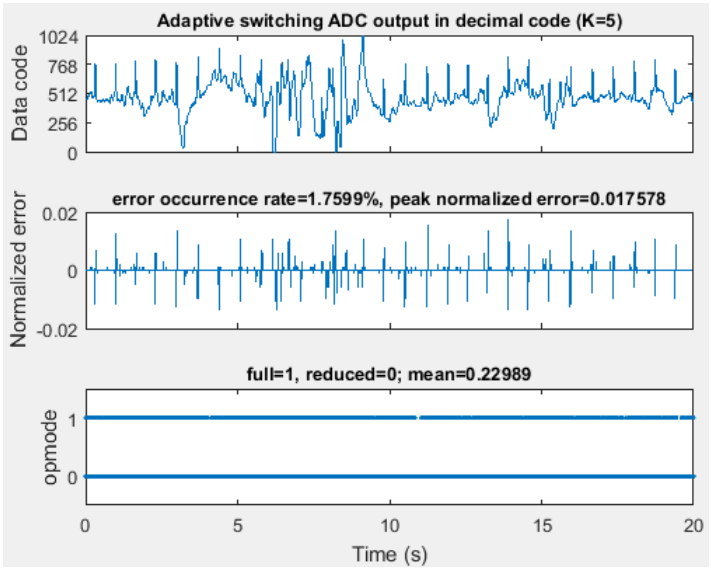


Fig. 3.20 Behavioral model simulation result with the clip from ECG Recording 105 (noise) and $K = 5$.

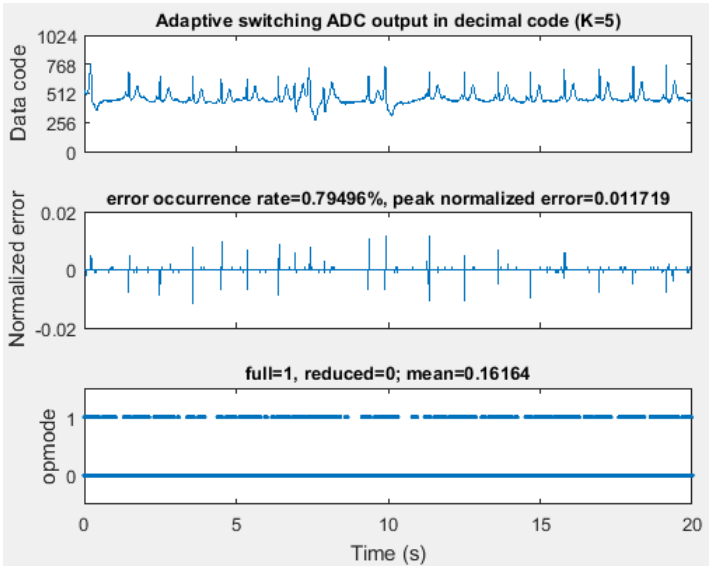


Fig. 3.21 Behavioral model simulation result with the clip from ECG Recording 106 (ventricular tachycardia) and $K = 5$.

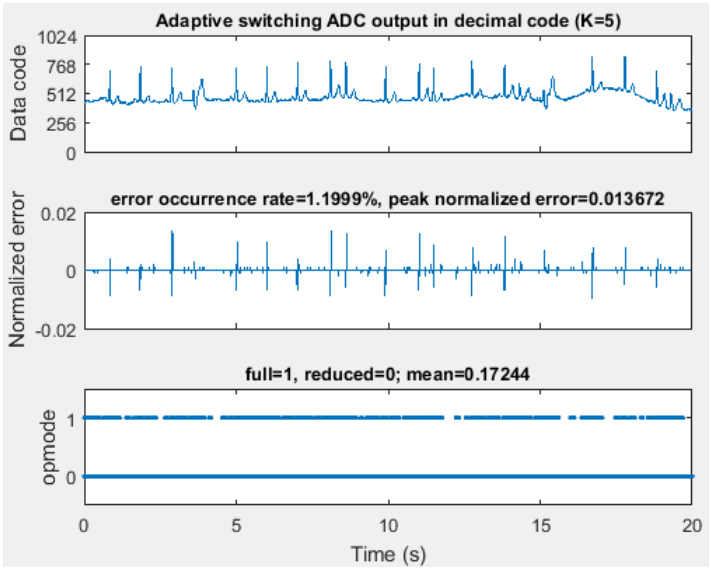
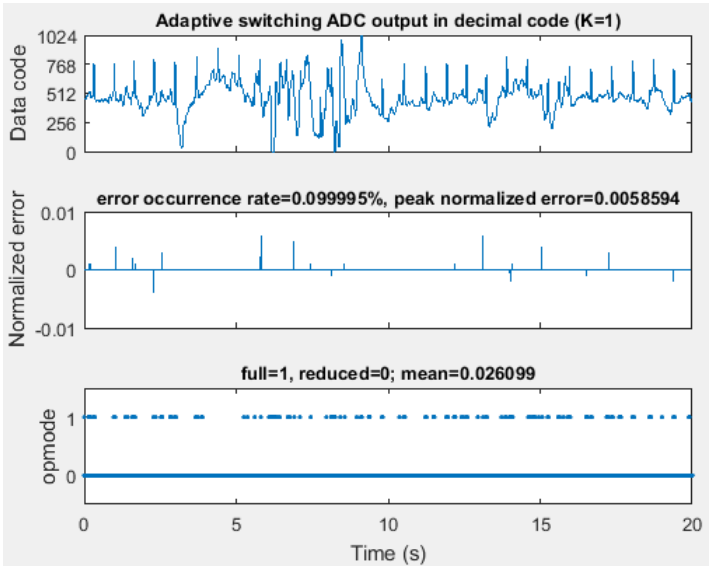


Fig. 3.22 Behavioral model simulation result with the clip from ECG Recording 202 (aberrated premature atrial contractions) and $K = 5$.

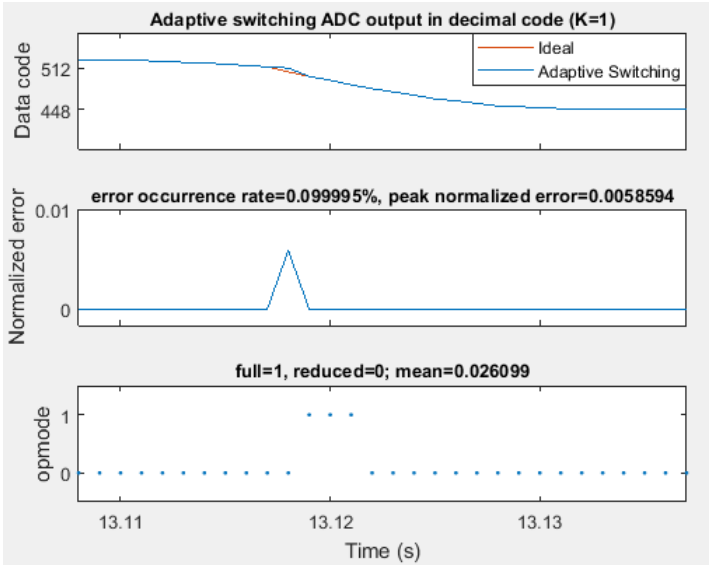
signal variations, but the typical traits of the diseases and artifacts are all caught in the outputs, such as the abnormally wider QRS complex following a deep fall for premature ventricular contraction (Fig. 3.19). The toughest one would be the noisy case because of the wild variation (Fig. 3.20), but the error magnitudes are kept small (< 1.8%). The ADC operated in reduced switching mode 77% of the time.

The second simulation verified the function of the adaptive switching with various K values. The clip from Record 105 (noise) was selected for the input because of the wild variation (Fig. 3.20), to make a harsh condition. Five cases (K = 1, 3, 5, 7, and 9) were tested and the results are presented in Figs. 3.23, 3.24, 3.25, 3.26, and 3.27, respectively. As shown in the figures, the adaptive switching works for various K values. The outputs in all cases have good quality with invisibly small errors on the scale. The incidence and magnitudes of errors are observed to increase and decrease by the rise of K, respectively. The zoomed-in views show that the errors do not form a cluster by the algorithm that switches to full switching mode if the LSB code is all 0's or all 1's. Since reduced switching mode is entered at least three periods later, errors cannot occur in series. It is manifested in Figs. 3.24(b) and 3.25(b).

As anticipated in Subsection 3.3.2, there are marked differences in the proportions of the reduced-switching-mode operation with different K values. The ADC ran in reduced switching mode more frequently for lower K: it was in the mode 97.4% of the time for K = 1, and 10% for K = 9. It is an obvious consequence considering the value of K determines the size of the range within which signal variations are deemed little active, which decreases by a power of 2 as K increases.

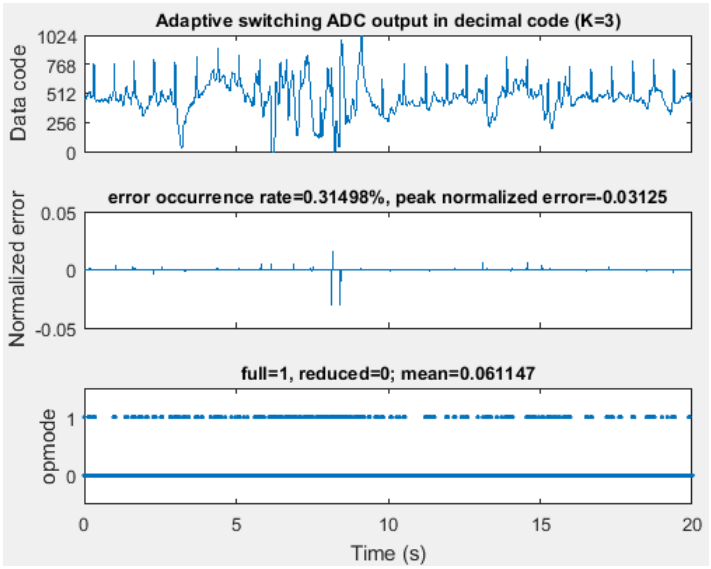


(a)

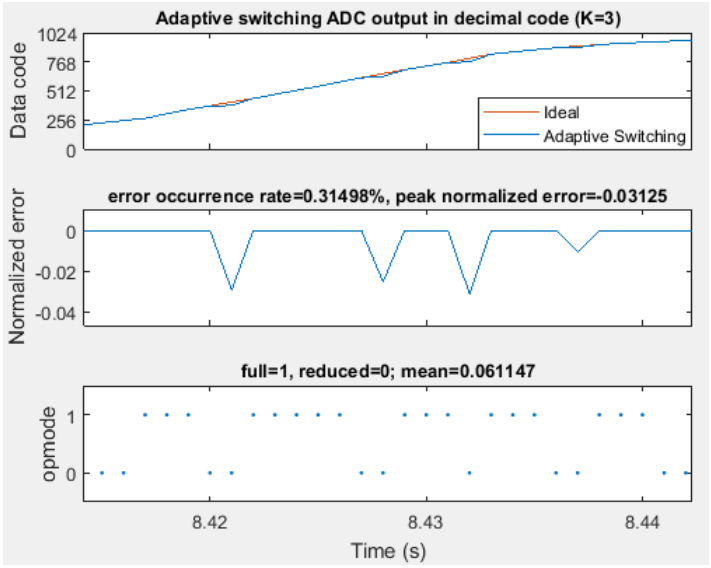


(b)

Fig. 3.23 (a) Behavioral model simulation result with the clip from ECG Recording 105 (noise) and $K = 1$ and (b) its zoomed-in view.

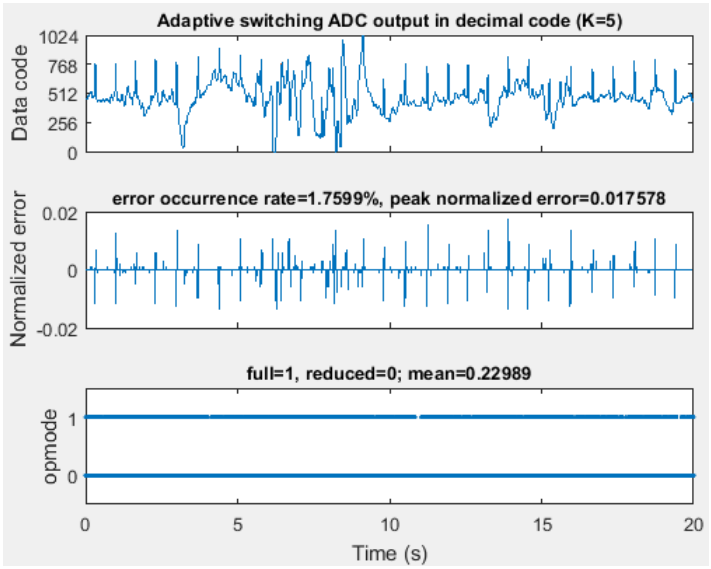


(a)

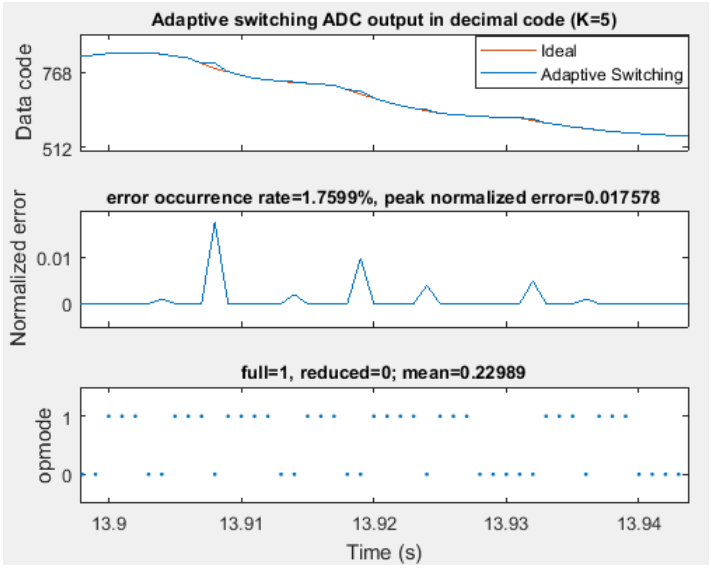


(b)

Fig. 3.24 (a) Behavioral model simulation result with the clip from ECG Recording 105 (noise) and $K = 3$ and (b) its zoomed-in view.

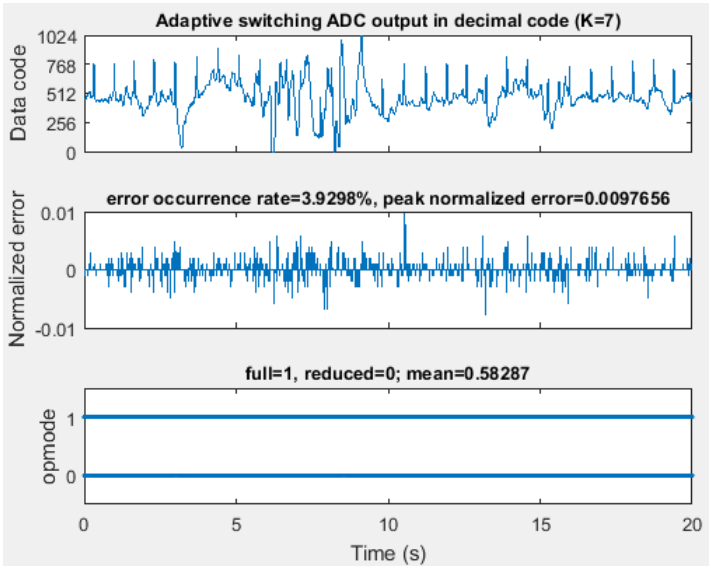


(a)

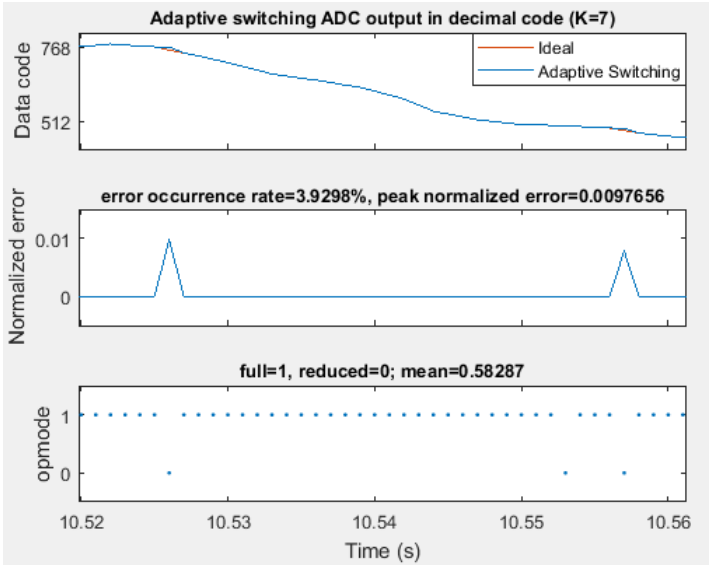


(b)

Fig. 3.25 (a) Behavioral model simulation result with the clip from ECG Recording 105 (noise) and $K = 5$ and (b) its zoomed-in view.

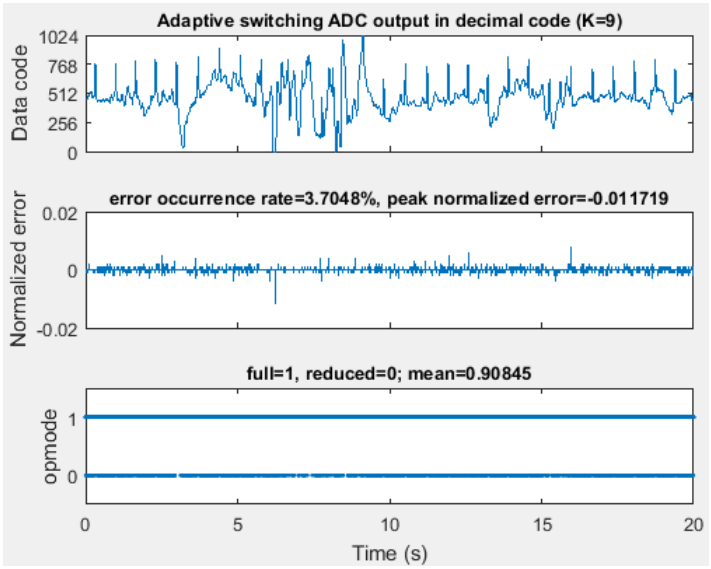


(a)

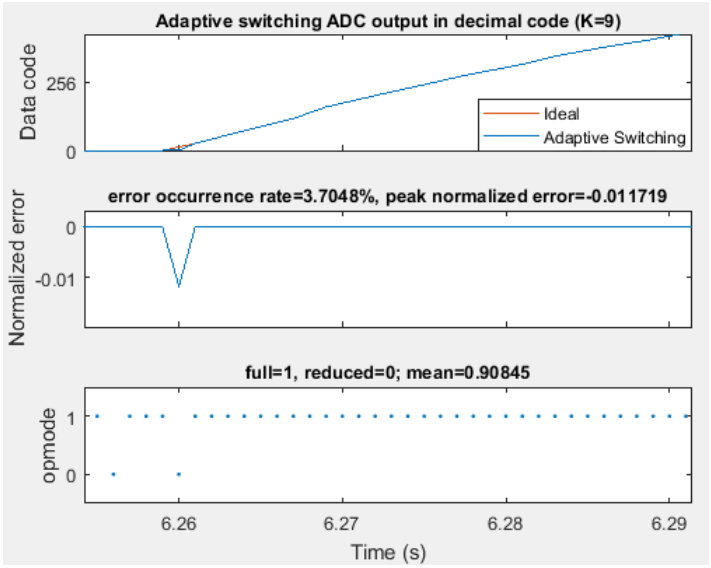


(b)

Fig. 3.26 (a) Behavioral model simulation result with the clip from ECG Recording 105 (noise) and $K = 7$ and (b) its zoomed-in view.



(a)



(b)

Fig. 3.27 (a) Behavioral model simulation result with the clip from ECG Recording 105 (noise) and $K = 9$ and (b) its zoomed-in view.

The third simulation examined the power consumption and the error incidence with all possible K values from 0 to 9. Among these, the $K = 0$ case is the case that it always runs in full switching mode. As the input, the clips from Recording 115 (normal rhythm) and Recording 105 (noise) were selected, which are representatives of good and bad conditions. Fig. 3.28 shows that the average switching power consumptions of both inputs have bowl-shaped curves with respect to K. For low values of K, the power drops as K rises because fewer capacitors are switched. For high values of K, however, an opposite trend is observed. In fact, it agrees with the anticipation in Subsection 3.3.2 that, with higher K, the ADC runs more likely in full switching mode, losing the power benefit from the higher K. Thus the minimum switching power consumption is found in the middle: $K = 6$ for the normal rhythm, $K = 4$ for the noisy input. Fig. 3.29 shows the mean of the opmodes. The aforementioned dominance of full switching mode at high K is manifest.

The incidence of the errors are presented in Fig. 3.30, showing almost monotonic profiles such that errors occur more frequently as K rises. This result is attributed to the narrow range for low activity, from which the true output codes escape frequently. On the other hand, the sensitiveness to errors helps keep their magnitudes small. This is well represented in Fig. 3.31 which shows the magnitude of the greatest normalized error by K. As K increases, the peak magnitude becomes smaller. The worst case is with $K = 3$. The small magnitudes of the greatest error for $K < 3$ indicates that the range bound by an MSB code is wider than the greatest errors possible by both inputs. Interestingly, the peak magnitudes of errors of the normal rhythm case is greater than those of the noisy case.

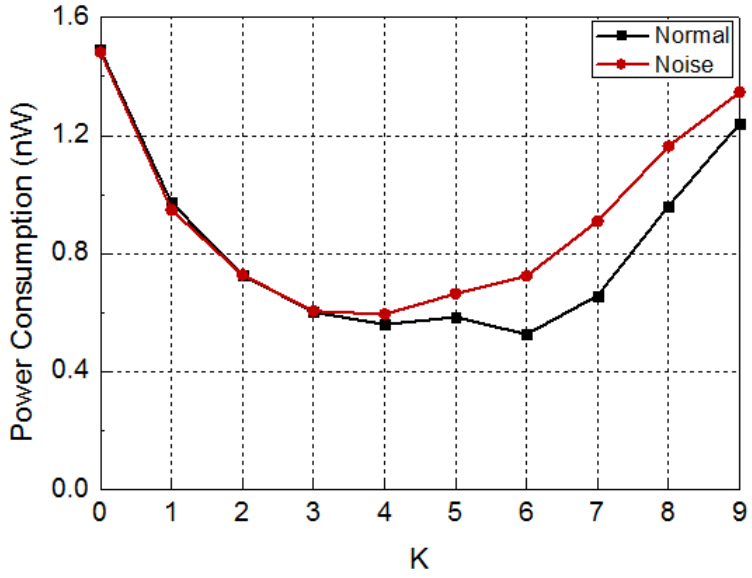


Fig. 3.28 Simulated average switching power vs. *K*

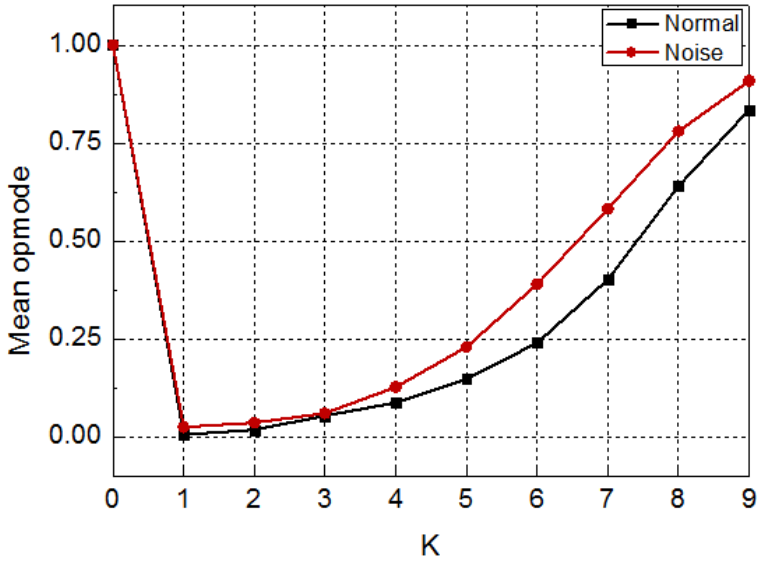


Fig. 3.29 Simulated mean opmode vs. *K*.

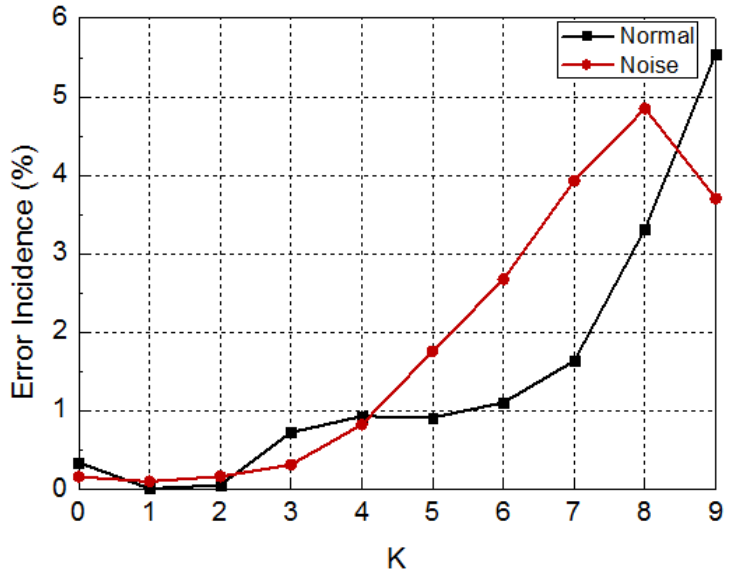


Fig. 3.30 Simulated error incidence vs. *K*

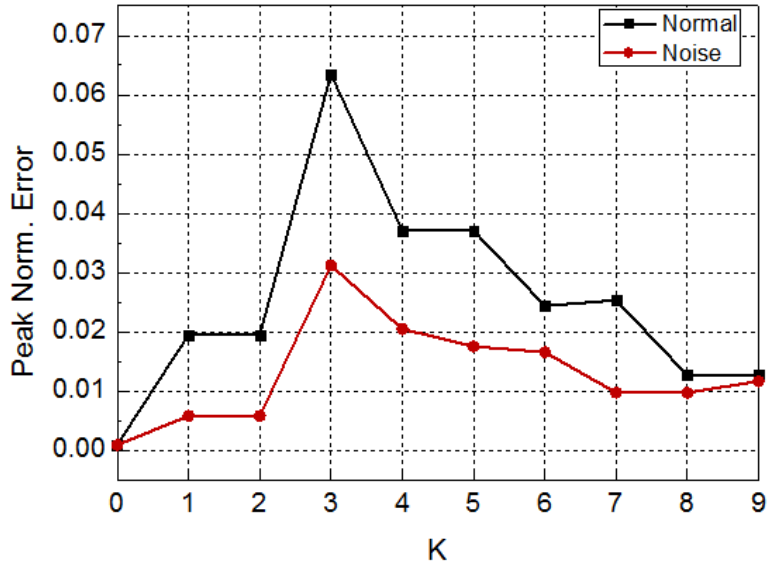


Fig. 3.31 Simulated peak normalized error vs. *K*.

This might be related to the smaller error incidence and mean of the opmodes of the normal rhythm case.

The simulations above demonstrated that the proposed adaptive switching algorithm works for various realistic inputs and K values. The results showed that the drawback of the adaptive switching—that errors take place when prediction of the next MSB code fails—turned out tolerable for all inputs used and with $K = 5$, that the magnitudes did not exceed the specification, ±5%. In addition, the variation of K affected the properties of errors and the proportion of reduced switching mode. As K increased, more errors with smaller magnitudes resulted, and a lower proportion of reduced switching mode was observed. The latter influenced the switching power consumption, so that the minima were found around the middle values of K.

There is no single optimum K applicable to any ECG input, but it is possible to narrow the range based on the simulation results. Only a few ECG inputs, although selected to represent a variety of cases, were used for the simulations; however, the results could have generality because the common characteristics of ECGs limit the diversity in the target signals. The criteria for specification of K are (a) the errors must be within the tolerable range, and (b) the switching power consumption should be as low as possible, which rule out the low and high ranges. As a compromise, $K = 5$ was selected for the circuit realization. It is the median of the simulated optima. Even though it happens to be not optimum for the current input which the ADC is processing, it is still beneficial enough in that its optimum must be near, and the power loss to be out of the optimum is minimal, as displayed in Fig. 3.28.

3.3.6 CONSIDERATION ON OTHER APPLICATIONS

The motivation of the adaptive switching algorithm was originally to utilize the dichotomous nature of the ECG signal activity; this by no means limits the applications within ECG monitoring only, however. If the signal other than ECG has a similar characteristic, the algorithm is applicable. Particular examples include blood pressure and blood oxygen saturation monitoring using a mobile device [57]. As they are closely related to the ECG, the waveforms have similar traits. The pulse waveform [57, Fig. 1] and hemoglobin saturation waveform [57, Fig.2] closely follow the ECG.

3.4 CIRCUIT IMPLEMENTATION

3.4.1 OVERVIEW

Fig. 3.32 exhibits the schematic diagram of the proposed 1.8-V 1-kS/s 10-bit adaptive switching SAR ADC [23]. The CDAC is designed to have a fully differential tri-level segmented topology using the top-plate sampling. The logic is largely divided into two parts, which implement full and reduced switching modes. The control signals are denoted by C and D in Fig. 3.32. The C signals are associated with the common mode V_{com}, and the D signals are with V_{refp} or V_{refn} upon the comparator output. If a C signal is

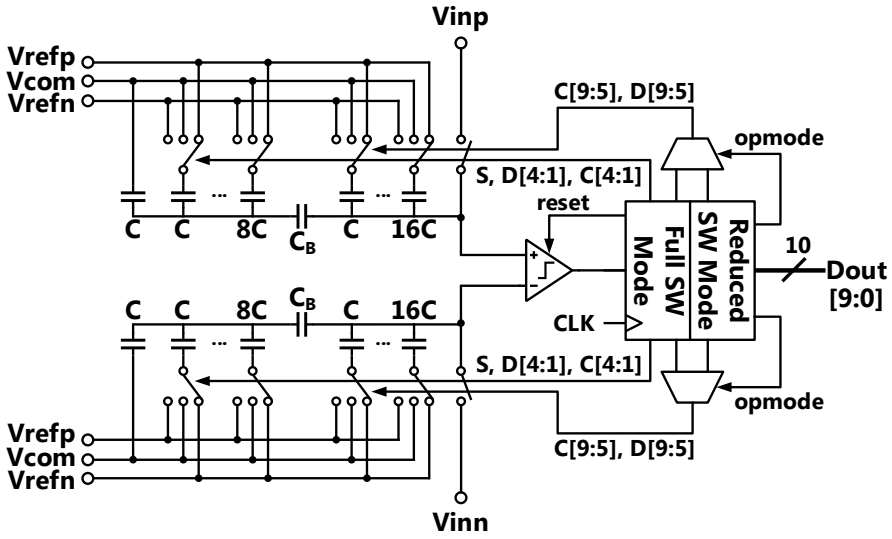


Fig. 3.32 Schematic diagram of the adaptive switching SAR ADC. © 2017 IEEE. Adapted.

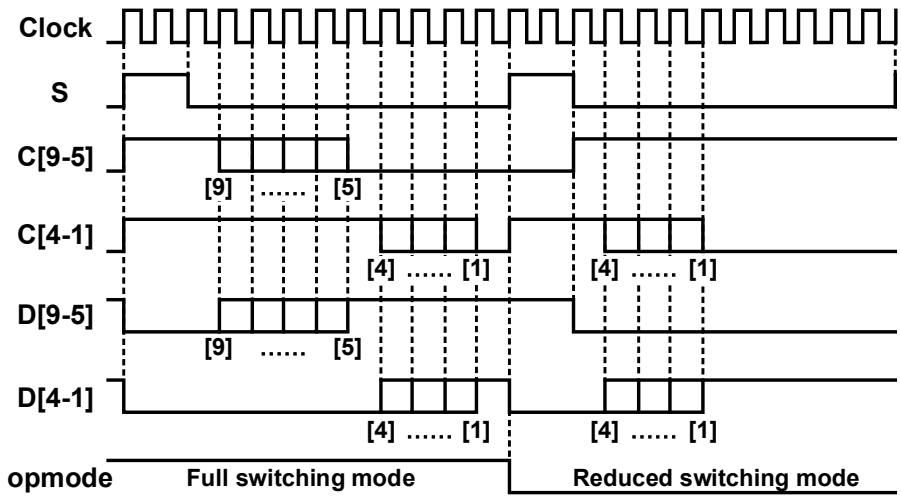


Fig. 3.33 Timing diagram of the key signals. © 2017 IEEE. Reprinted.

high, the bottom plate of the corresponding capacitor is connected to V_{com}. If a D signal is high, the bottom plate of the corresponding capacitor is connected to V_{refp} or V_{refn}, with respect to the comparator output. For a particular capacitor, both C and D are not turned on at the same time. Both modes generate their own set of control signals and the proper set is selected by signal opmode.

Fig. 3.33 shows the waveforms of the key signals. The system clock has a frequency of 12 kHz. The first two cycles out of 12 are assigned to the sampling phase. The S signal being 1 indicates it is the sampling phase. Otherwise, it is the conversion phase. Full switching mode uses all 10 remaining cycles for conversion, as does the ordinary SAR ADC. On the contrary, reduced switching mode takes 5 cycles for conversion because switching the 5 MSB capacitors is skipped. For the remaining 5 cycles, the ADC idles. The previous MSB code is used in the sampling phase. Therefore the D signals of the

MSB section, D[9:5], are 1, connecting either V_{refp} or V_{refn} with respect to the code, and the C counterparts, C[9:5], are 0. The conversion procedure of the LSB section follows the sampling phase right away. The signals of the MSB section are inverted.

3.4.2 COMPARATOR AND CDAC

Since the operation speed is slow (1 kS/s) and the resolution is not high (10 bits), the comparator consumes very little power and the performance requirement is not demanding. Fig. 3.34 shows the schematic diagram of the comparator. The conventional design of the StrongARM latch [36] is sufficient to meet the required specifications. The input devices are designed larger than the transistors of the latch and reset switches in size to increase the gain. The footer device is the largest in size so that it drains its drain node

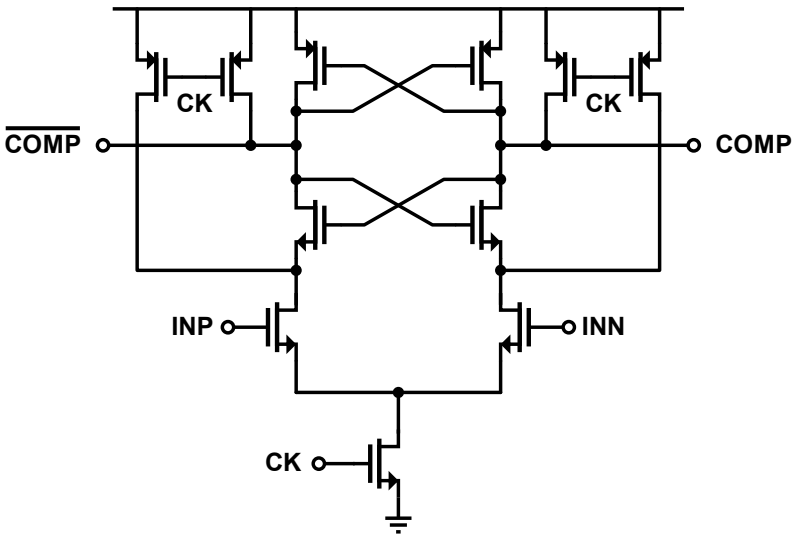


Fig. 3.34 Schematic diagram of the comparator.

completely before the input devices operate to *split* the initially minute divergence.

The CDAC is the building block whose design is critical to the performance of the ADC. A fully differential tri-level segmented CDAC topology is adopted for the DAC to receive a differential input and reduce the total area. Fig. 3.35 presents the schematic diagram of a single side of the DAC. The input is sampled on the top plates of the capacitors to implement the partial sampling. The unit capacitance is 26.6 fF, which is the minimum metal-insulator-metal (MIM) capacitance available by the process. The capacitances and the corresponding switches are binary weighted, which keeps the RC time constants equal so as to maintain the linearity performance. The value of the bridge capacitance is 1.07 times the unit capacitance, which is the closest value available in the process to the ideal value of 17/16 times the unit capacitance. The three references are externally provided. In addition, care was taken in the layout of the CDAC to address the mismatch problem. The routing and interconnect parasitics were the primary concerns in the layout. The capacitors were arranged to have the terminal of each bottom plate on the edge where the signal lines from the switches end, so as to minimize the interference from the lines to other capacitors. Fig. 3. 36 shows the arrangement of the capacitor array.

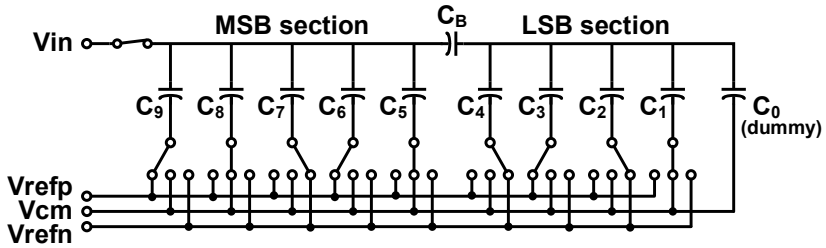


Fig. 3.35 Schematic diagram of a single side of the CDAC.

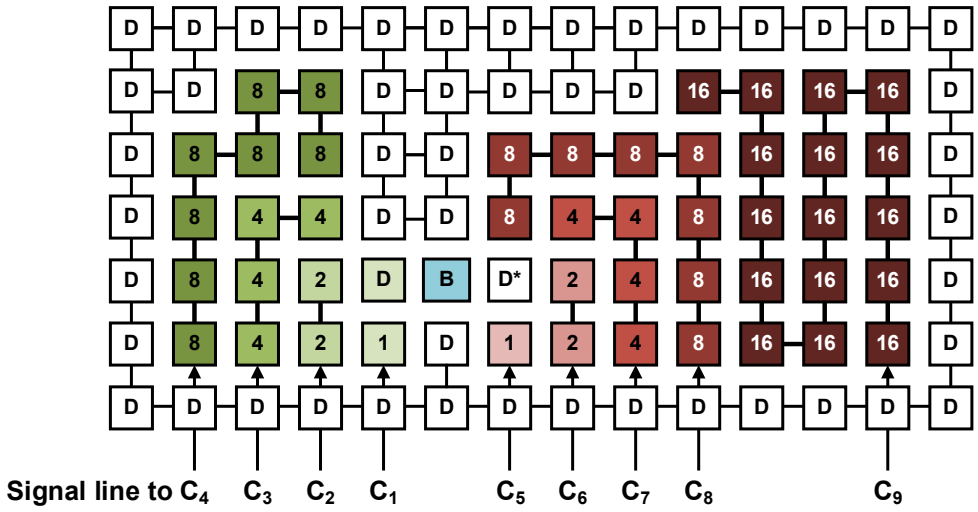


Fig. 3.36 Arrangement of the capacitors in the layout. The routing on the top plates is omitted. B for bridge capacitor, D for dummy, D* has no insulator.

The capacitors are grouped as depicted in Fig.3.36. All top plates on each of the MSB and LSB sides are connected. The bottom plates of each group are connected by an Eulerian trail to minimize the interconnect parasitics. The top plates on the MSB side is connected to the bottom plate of the bridge capacitor. D* in Fig. 3.36 is the empty space for the metal line from the MSB top plates to descend on the bottom plate layer. It was put there at the expense of inevitable nonlinearity due to the irregularity, which tweaks the balance in the parasitics in the vicinity.

3.4.3 ADAPTIVE SWITCHING LOGIC

The circuit implementation for the adaptive switching logic is the core of the proposal. It is largely done as an extension of the conventional SAR ADC logic. Fig. 3.37 conveys the gist concisely. Full switching mode logic is essentially conventional SAR logic plus MSBs tracking. A set of modified signals to the SAR logic yields the main operation of reduced switching mode. Adding circuitry of LSBs extrapolation to it completes reduced switching mode. The flags from MSBs tracking and LSBs extrapolation are used to generate the opmode signal.

The implementation of the conventional differential tri-level SAR ADC logic, which is the basis of the adaptive switching logic, is shown in Fig. 3.38. It is an adaptation of the basic SAR logic [58] to the differential, tri-level, and top-plate sampling topology. The loosely described D signals in Subection 3.4.1 are realized as the separate DH and DL signals associated with V_{refp} and V_{refn}, respectively. They are generated from the code

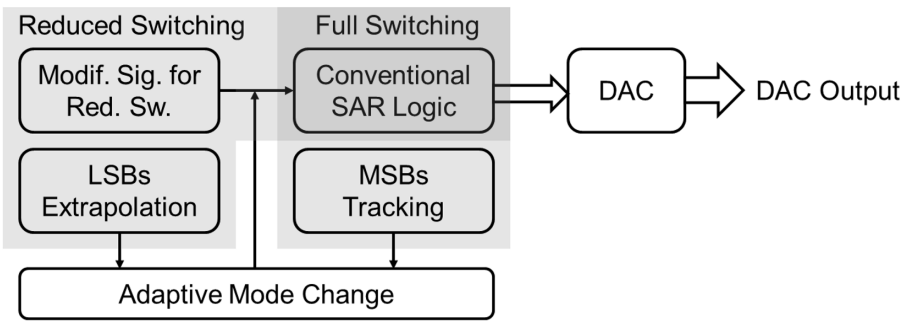


Fig. 3.37 Block diagram of the adaptive switching SAR ADC logic and DAC.

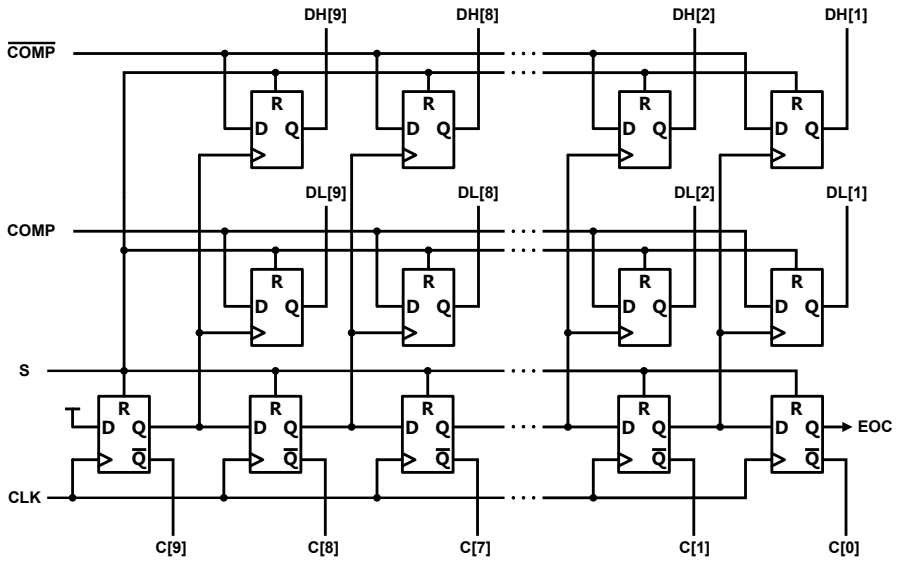


Fig. 3.38 Schematic diagram of the conventional 10-bit SAR ADC logic.

registers receiving the differential output of the comparator. The top-plate sampling accounts for the reversed polarity. The sequencer generates both the timing signals for the code registers and the C signals, which are inverse to each other.

The conventional SAR logic circuit is extended to have the proposed two-mode operation as shown in Fig. 3.39. Multiplexers select the proper set of inputs by opmode. In full switching mode (opmode = 1), it reduces to the conventional case in Fig. 3.38 in function. In reduced switching mode (opmode = 0), $\overline{S}$ replaces the conventional C signals for the MSB bits (Fig. 3.39(a)), resulting in the waveforms of C[9:5] in reduced switching mode in Fig. 3.33. The MSB code registers are updated with the previous MSB code at S to sample with it as shown in Fig. 3.11(a), and is then reset, as shown in Fig. 3.11(b), achieving the waveforms of D[9:5] in reduced switching mode in Fig. 3.33. The

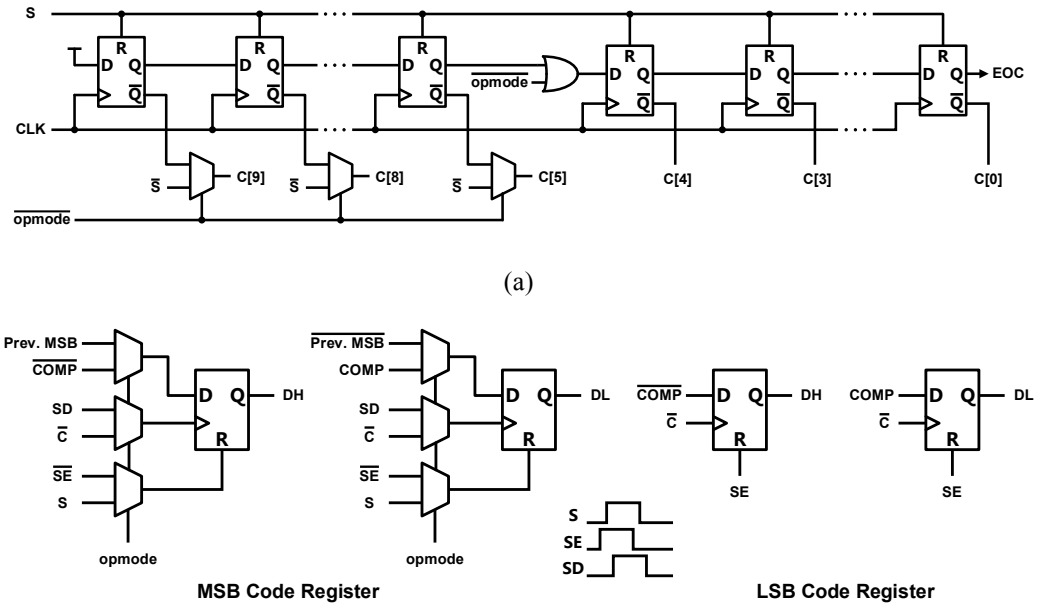


Fig. 3.39 Extension of the SAR ADC logic for adaptive switching: (a) sequencer and (b) code register.

sequencer and code registers of the LSB section need no such extension except the ORing with $\overline{\text{opmode}}$: it makes the bit first in line, skipping the MSB section switching. Timing signals such as SD and SE were generated from the sampling signal S to achieve appropriate timing.

The MSBs tracking logic was designed as depicted in Fig. 3.40 [23]. The existing output register is involved in this logic. The input and output of the MSB section of the output register are the current and previous MSB codes, respectively. The equality information of the two codes are stored in the additional flip flop. Taking its input and output again, the equality of three consecutive MSB codes can be examined in every

period. If they are equal, the opmode reset signal, R, becomes 1. The MSB portion of the output register is frozen for the use in the upcoming reduced switching mode.

The linear extrapolation of the LSB code is achieved by left shifting and a 6-bit subtractor as shown in Fig. 3.41 [23]. The left shifting is done by proper wiring without additional circuitry. The MSB bit of the subtractor indicates either overflow or underflow in the 2's complement representation. If it is 1, it implies that the MSB code would change in the next period. The detection of the current LSB code being either 00000 or 11111 is also carried out. If either of the above cases takes place, the opmode set signal, F, becomes 1.

The opmode signal is generated by an SR flip flop (Fig. 3.42). If F is 1, opmode is set to 1 and full switching mode starts. If R is 1, opmode is reset to 0 and reduced switching mode begins.

The remaining part of the logic is the output register and the idle counter. The output register holds the signals converted out (DL signals) and outputs at S. The idle counter runs when conversion is finished in reduced switching mode. It counts 5 before the next period to maintain the sampling period.

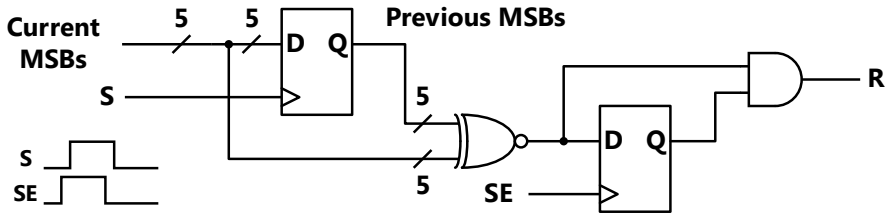


Fig. 3.40 Schematic diagram of the MSBs tracking logic. © 2017 IEEE. Reprinted.

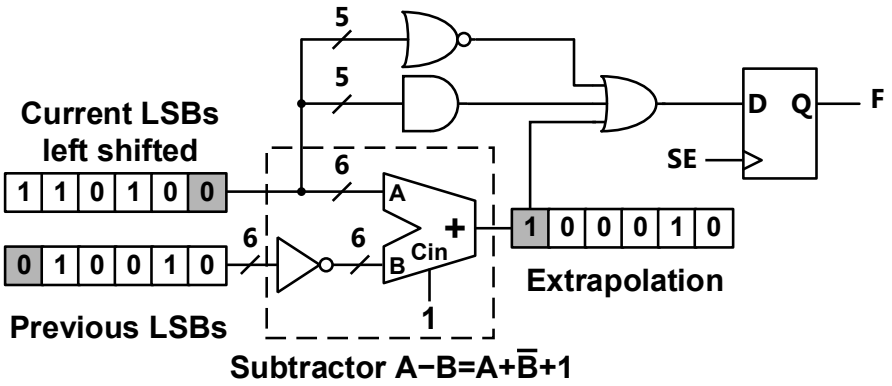


Fig. 3.41 Schematic diagram of the LSBs extrapolation logic. © 2017 IEEE. Reprinted.

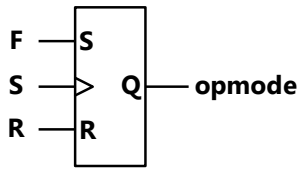


Fig. 3.42 opmode generation.

CHAPTER 4

PROTOTYPE EXPERIMENTS

4.1 FABRICATION AND EXPERIMENT SETUP

A prototype of the proposed adaptive switching SAR ADC was fabricated in a 0.18-μm CMOS process. The layout and chip micrograph are presented in Fig. 4.1 [23]. The active area is 0.096 mm^2.

Fig. 4.2 shows the experiment setup used in the measurement. The differential input

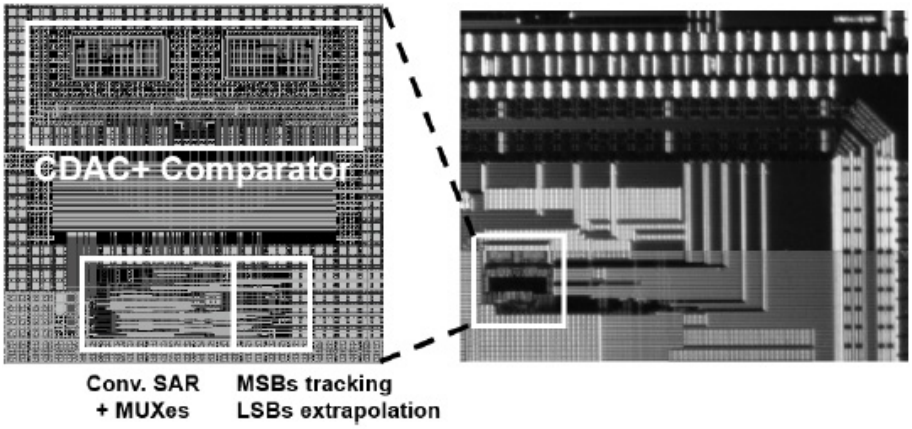


Fig. 4.1 Layout and chip micrograph of the adaptive switching SAR ADC. © 2017 IEEE. Reprinted.

and clock signal were generated using Keysight 81160A, which is a function generator that supports sinusoidal, clock, and cardiac pattern signals. An oscilloscope (Tektronix MSO4104) was used to get the waveform of the differential input. The DC power supply (Keysight 3631A) provided the supply voltage (1.8 V) and ground to the test board. The regulators on the test board generated the analog and digital supply voltages (V_{DDA}, V_{DDD}), reference voltages (V_{refp}, V_{com}, V_{refn}), and ground. The currents from them were measured through a multimeter (Kesight 34411A). The values were used to compute the power consumption. The 10-bit parallel output of the ADC was transmitted to Logic Analyzer (TLA 7012A) for analysis.

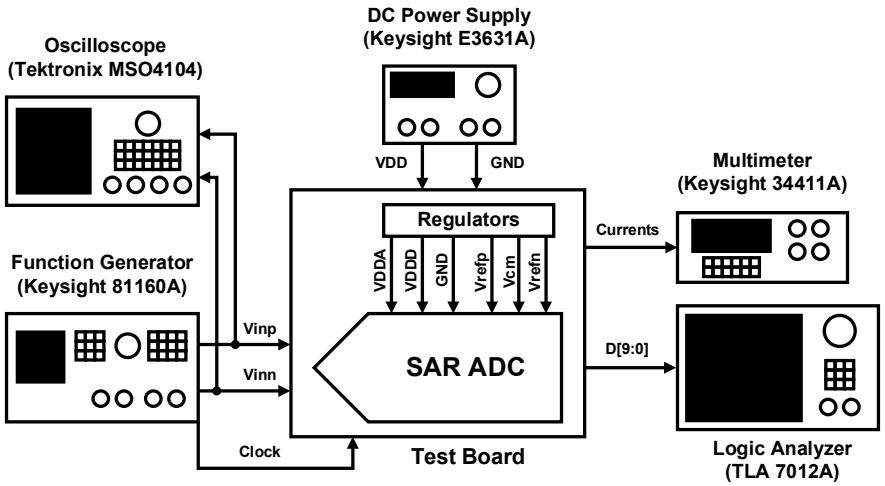


Fig. 4.2 Experiment setup.

4.2 MEASUREMENTS

Two experiments were conducted with the test board. First, an ECG type signal was applied as the input to examine the function and power benefit of the proposed adaptive switching. Second, a sinusoidal input was applied to the ADC to measure its intrinsic performance.

4.2.1 POWER REDUCTION MEASUREMENT WITH ECG-TYPE INPUT

Keysight 81160A can generate a signal with a fixed ECG pattern with the user-controllable variables of the common mode, magnitude, and frequency. Table 4.1 presents the values used to generate the differential ECG-type signal. The values were decided on the assumption that an instrument amplifier provides an amplified differential signal. The common-mode voltage was chosen to be half the supply voltage, and the peak-to-peak voltage was chosen to have margin from both power rails. The frequency determines the

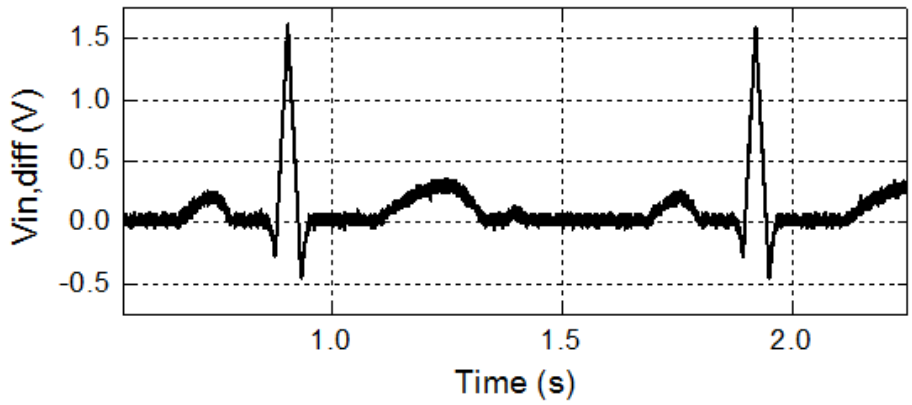
Table 4.1 Variables used for the ECG generation in Keysight 81160A

Variable	Value
Common-mode voltage	0.9 V
Peak-to-peak voltage	1.65 V
Frequency	985 mHz

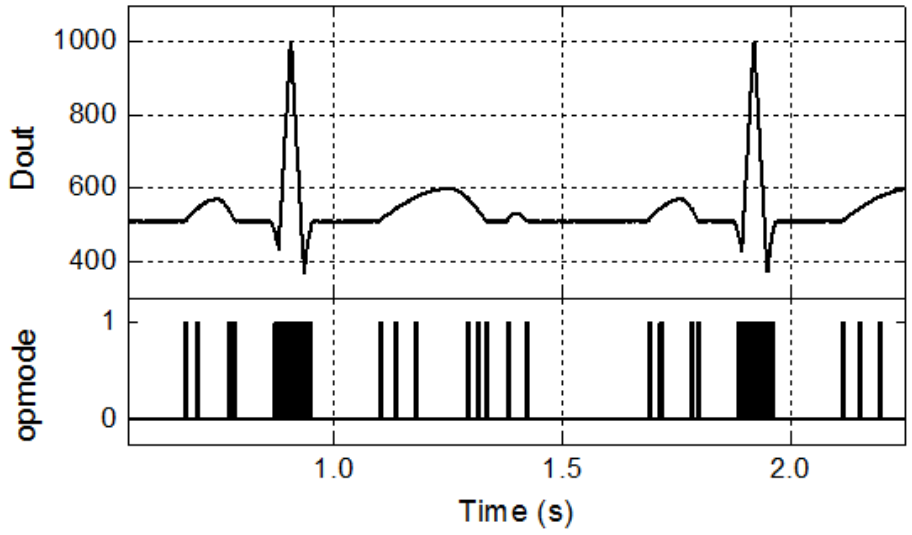
R-R intervals. The value was obtained from Recording 115 of the MIT-BIH Arrhythmia Database (Figs. 3.8(a) and 3.18(a)). The generated signal was applied to the ADC running with the adaptive switching algorithm.

Fig. 4.3 shows the function of the adaptive switching with the ECG-type input. The measured input is shown in Fig. 4.3(a), and the reconstructed waveform from the ADC digital output code and the opmode waveform are shown in Fig. 4.3(b). It is demonstrated that mode change was conducted so smoothly that the reconstructed ECG waveform from the digital output of the ADC maintains good quality, as the output given by the behavioral model simulations.

In order to measure the power benefit by the adaptive switching, the ADC was run both with the adaptive switching algorithm and in fixed full switching mode for the same input, and the power consumptions were measured and compared. The power domains were split into the comparator, logic, and DAC, and measured separately. The analog supply voltage V_{DDA} supplied the comparator and the bulk of the DAC switches, the latter of which consumed a negligible amount. The digital supply voltage V_{DDD} concerned from the adaptive switching SAR logic to the switch driving elements. Since all power domains used the same voltage level (1.8 V) and the sizes of switches were small, the drivers were not physically separated and hence no separate power domain for them. The last domain, DAC power, is that provided by the external reference sources to charge and discharge the capacitors in the CDAC. It is the switching power consumption that was modeled and examined in the behavioral model simulations to quantify the effectiveness by the adaptive switching.



(a)



(b)

Fig. 4.3 (a) The measured waveform of the differential input voltage on the oscilloscope; and (b) the output code of the ADC represented in decimal, and the opmode waveform. © 2017 IEEE. Reprinted.

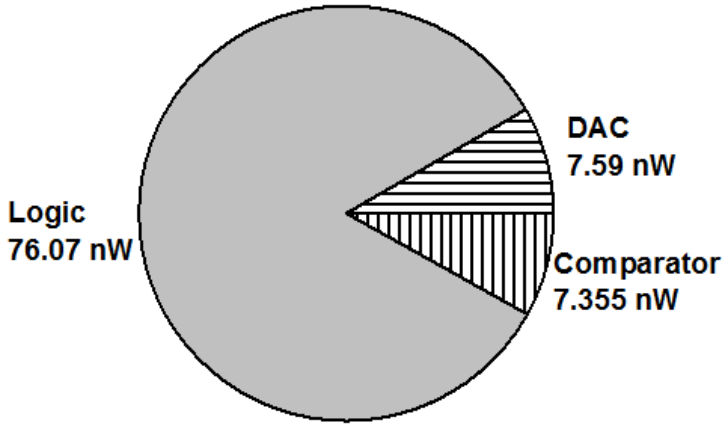
Table 4.2 presents the measurements of power consumptions of the two cases and Fig. 4.4 displays the power breakdowns of the two cases. In both cases, the logic power is dominant. It is obvious in that the digital logic circuit is much larger than the comparator

Table 4.2 Measurements of the power consumption

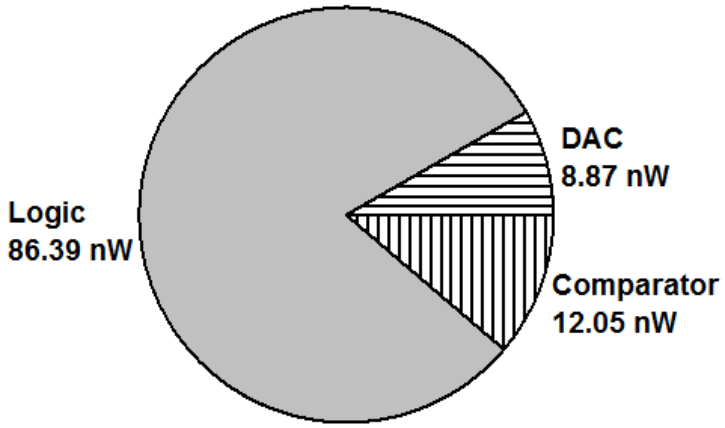
	Comparator	Logic	DAC	Total
Adaptive switching	7.355 nW	76.07 nW	7.59 nW	91.02 nW
Fixed full switching	12.051 nW	86.39 nW	8.87 nW	107.51 nW
Reduction rate	39%	12%	14.4%	15.3%

in size, and the segmented CDAC topology greatly scales down the capacitance hence a small share of it results. The use of the same voltage of 1.8 V for both V_{DDA} and V_{DDD} also contributed to the large share of the logic power. Obviously, a far lower value of V_{DDD} is enough for functioning. Some works employ a lower voltage for V_{DDD}, as in [59], at the expense of the necessity of level shifters.

The power consumption was reduced in all domains in different degrees. A significant reduction of 39% was observed in the comparator domain, which is an expected result because the comparator power is directly affected by the reduced number of bitcycles. It is proportional to it because static power is not consumed and it is not activated in the idle cycles. The logic power, however, has overhead that is not scalable directly with the number of bitcycles. The additional circuitry such as MSBs tracking, LSBs extrapolation, and the idle counter consumes the overhead power. A reduction by 10.3 nW, or 12%, was obtained in the logic power domain. The DAC power consumption was reduced by 1.28 nW, or 14.4% in proportion. The simulation result was right in that the power saving was about 1 nW (see Fig. 3.28), but the measurements turned out to be much greater. Their discrepancy in size is attributable to the existence of the parasitics on



(a)



(b)

Fig. 4.4 Power breakdown of (a) the adaptive switching and (b) the fixed full mode switching.

the routes from the reference sources to the DAC, whose charging and discharging lead to an increase in the reference currents in both fixed full switching and adaptive switching. This added amount, which appears like a static offset, was unexpectedly larger than the power benefit. Compared to those, the parasitics in parallel with the DAC capacitors to cause mismatch contributed a negligible amount to the power.

The aforementioned parasitics must have arisen from the coupling between the decoupling capacitors and the reference metal paths running from the pads to the core (the area of the ADC proper). The decoupling capacitors are the MOS capacitors deployed outside the core to surround it, and connected to either analog or digital power supplies through metal, which surrounds other signal metal lines running to the core from outside, including the reference metal paths. The enormous quantity of the decoupling capacitors inhibited a complete post-layout simulation to investigate the total effects by the decoupling capacitors before the fabrication. The partial effects were indirectly observed in the post-layout simulation of the core and a few layers of decoupling capacitors around it, in which the supply currents increased by a few nanoamperes. The measured figures would have been improved with optimized design of decoupling capacitors.

4.2.2 Intrinsic Performance Measurement with Sinusoidal Input

The second experiment was conducted with a differential sinusoidal input with fixed full switching mode to measure the intrinsic static and dynamic performance of the ADC. The differential input has a peak-to-peak voltage of 3.15 V, and a frequency of 443.153 Hz, which is close to the Nyquist rate. The power spectral density of the fast Fourier transform of the ADC output is presented in Fig. 4.5. A total of 32768 points were taken for the FFT, and the Blackman-Harris window was used. The SNDR was measured to be

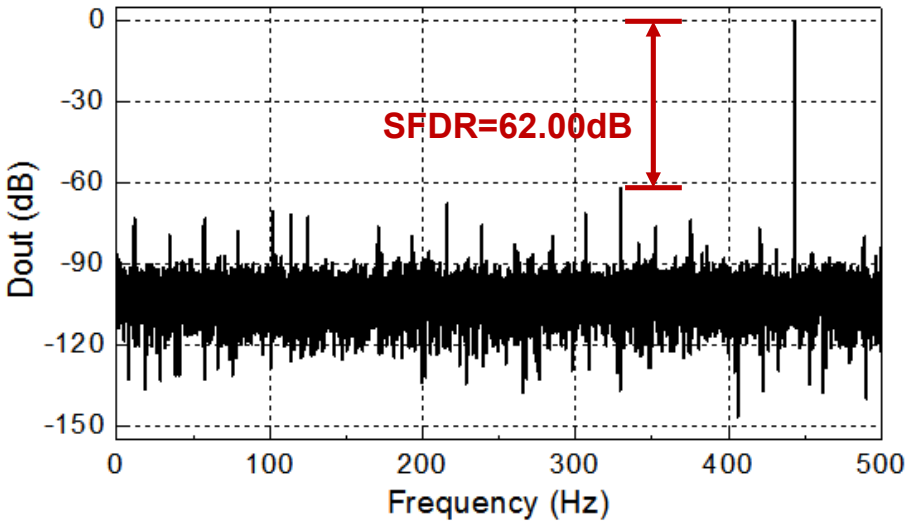


Fig. 4.5 FFT spectrum of the ADC output for the sinusoidal input.

56.24 dB, which is translated into an effective number of bits (ENOB) of 9.05 bits. The spurious-free dynamic range (SFDR) was measured to be 62.00 dB.

Fig. 4.6 shows the measured DNL and the integral nonlinearity (INL). It is a typical profile of capacitor mismatch in the segmented CDAC that the INL plot has slopes and steps [60]. It is understandable that such a static source of nonlinearity is the dominant factor as the ADC runs at a very slow rate. Since the capacitance at a particular bit is translated into the weight in the digit, mismatch in the capacitance of the bit alters the weight and shifts the decision level [60]. Also, the decision level shifts appear symmetrically [60]. The largest DNL spike at the center (= 2^9) indicates that the largest mismatch is between the MSB capacitor and the rest capacitors. It is trivial that the worst case is found where all bits change, i.e. between codes $2^{N-1}-1$ and 2^{N-1} [46]. Similarly, notable spikes on DNL are found periodically with intervals of 128 (= 2^7), suggesting

significant mismatch around the third MSB capacitor. The false dummy created next to the bridge capacitor (Fig. 3.36) can be a source of the above mismatches. The second MSB capacitor is next to it, hence the parasitic capacitance seen by the second MSB capacitor is out of balance, which in turn affects the capacitors nearby, i.e. the first and third MSB capacitors. Another pattern is found with intervals of 32 (= 2^5), which implies the mismatch in the bridge capacitor. After all, its capacitance is not the exact fractional value, hence mismatch is unavoidable. The maximum DNL and INL were measured as +0.39/−1 LSBs and +0.86/−1.5 LSBs, respectively.

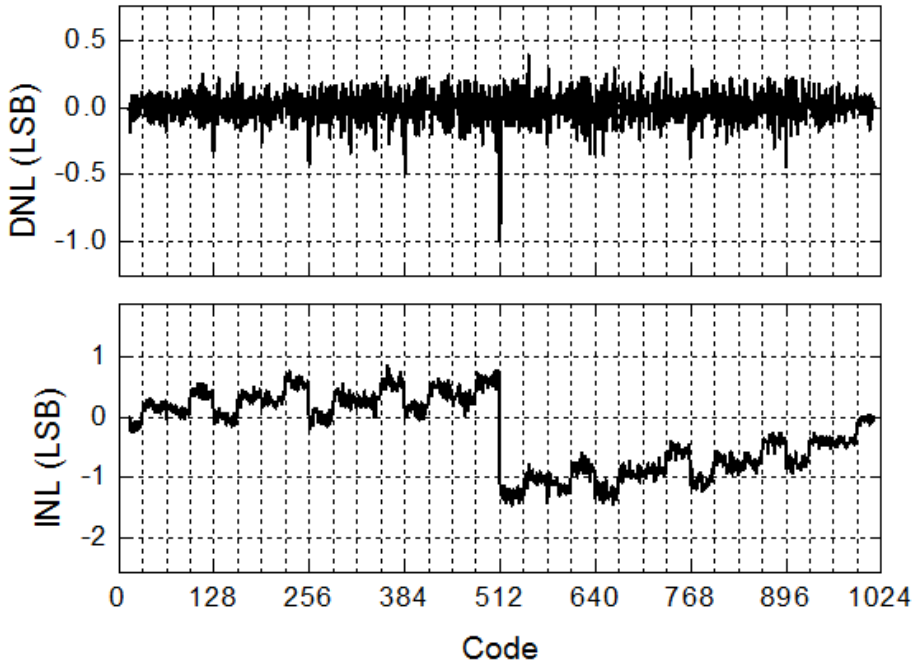


Fig. 4.6 Measured DNL and INL of the ADC output.

4.2.3 SUMMARY OF THE MEASUREMENTS AND SPECIFICATIONS

Table 4.3 shows the specifications and measurements of the proposed SAR ADC with the adaptive switching algorithm. For an ECG-type input, the ADC with adaptive switching achieved a 15.3% power reduction, consuming 91.02 nW. The measurement with a sinusoidal input demonstrated an ENOB of 9.05 bits.

Table 4.3 Measurements and specifications

Specification	Value
Technology	0.18-μm CMOS
Resolution	10 bits
Supply voltage	1.8 V
Sampling rate	1 kS/s
Differential input range	3.15 V_{P-P}
Total power consumption (ECG)	91.02 nW (adaptive switching) 107.51 nW (fixed full switching) (15.3% reduction)
Power consumption in comparator domain (ECG)	7.355 nW (adaptive switching) 12.05 nW (full switching) (39% reduction)
Power consumption in DAC domain (ECG)	7.59 nW (adaptive switching) 8.87 nW (full switching) (14.4% reduction)
Power consumption in logic domain (ECG)	76.07 nW (adaptive switching) 86.39 nW (full switching) (12% reduction)
SNDR (sinusoidal)	56.24 dB @ 443.153 Hz
ENOB (sinusoidal)	9.05 dB @ 443.153 Hz
SFDR (sinusoidal)	62.00 dB @ 443.153 Hz
DNL (sinusoidal)	+0.39/−1 LSBs
INL (sinusoidal)	+0.86/−1.5 LSBs
Active area	0.096 mm^2

CHAPTER 5

CONCLUSION

In this dissertation, a 1.8-V, 10-bit 1-kS/s SAR ADC with input activity adaptive switching specific to ECG monitoring applications has been proposed. The proposed adaptive switching algorithm has two switching modes to utilize the dichotomous nature of the ECG signal activity for power efficient operations. The essence of the proposed adaptive switching is to skip switching of some MSB bits (MSB section) in the low activity region in which they do not change, and thereby achieves a reduction in switching power consumption (reduced switching mode), while ordinary full switching is chosen in the high activity region. The size of the MSB section should be carefully determined to maximize the power reduction. There is, however, a drawback that it has to tolerate an error if prediction of the next code of the MSB section in reduced switching mode fails.

In order to examine the design issues and their effects, a behavioral model was developed. It closely modeled the SAR ADC with the segmented CDAC topology and implemented the switching actions in detail. The model contains the switching energy

consumption model developed for the topology and identification of occurrences of errors and their magnitudes. The simulations carried out with the behavioral model suggested that the incidence and magnitudes of errors would be within the permitted range, recommended by the American Heart Association. The simulations also enlightened that the tradeoff among the size of the MSB section, errors, and switching power consumption limits the candidates for the optimum size of the MSB section within the narrow middle range. In the implementation, 5 bits was selected.

A prototype was fabricated in 0.18-μm CMOS technology for the experiments. The active area of the prototype is 0.096 mm^2. The experiment conducted with an ECG type input examined and verified the function and power benefit of the proposed adaptive switching. Mode change was successful that the ADC resolved the highly active area such as QRS complexes, P and T waves in full switching mode while it entered in reduced switching mode in low activity regions. The power benefit by the adaptive switching was measured by comparing the power consumptions by both operations of the fixed full switching and adaptive switching. The power consumptions were measured separately by domain, viz., comparator, logic, and DAC. While the comparator power consumption directly influenced by the number of bitcycles showed a reduction by a factor of 39%, the reduction factor for the logic was just 12% because of the overhead that is not directly scalable with the adaptive switching. The DAC power domain, which provides the energy for switching in the DAC, showed a reduction by 1.28 nW. it is similar to that anticipated in the behavioral model simulation. However, the measured figures in both cases were greater than the simulated ones as if a static offset were added. It is attributed to the

parasitics by the decoupling capacitors outside the ADC core. All in all, the total power consumption was reduced by 16.49 nW or 15.3% in proportion. It is 91.02 nW with the adaptive switching, and 107.51 nW with fixed full switching operation.

The intrinsic performance of the ADC was measured with a sinusoidal input with a peak-to-peak magnitude of 3.15 V and a frequency of 443.153 Hz gave dynamic performance figures of an SNDR of 56.24 dB and an SFDR of 62.00 dB, and static performance figures of the maximum DNL of +0.39/−1 LSBs and INL of +0.86/−1.5 LSBs. The main contributor to nonlinearity is the capacitor mismatch. Especially, the exceptional irregularity allowed for routing between the MSB side and the bridge capacitor can account for the mismatch in the first and third MSB capacitors.

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한글초록

심전도는 심혈관계 질환의 진단을 위한 중요한 자료로서 감시 및 기록된다. 때로 부정맥 진단 등을 위하여 심전도를 오랜 시간 관찰해야 할 경우, 착용 가능한(웨어러블) 장비나 체내에 이식할 수 있는 장비를 사용해야 하는데, 이들은 전력 소비가 적어야 한다.

축차 비교형 아날로그-디지털 변환기(SAR ADC)는 저전력 응용 분야에서 주로 선호한 구조였으나 최근 아날로그-디지털 변환기 설계의 추세는 SAR ADC가 훨씬 넓은 응용 분야에 적용 가능하며 가장 넓은 범용성을 가진 구조임을 보여준다.

본 논문의 주제는 심전도 신호처럼 양분된 신호 활성도를 가지면서 평균 신호 활성도는 낮은 유형의 신호를 대상으로, 이 특성을 이용하여 전력의 소비를 낮추는 신호 특화된 스위칭 기법을 적용한 SAR ADC 설계이다. 본 논문에서는 신호 특화된 기법을 적용한 1.8V, 10 bit, 1kS/s의 저전력 SAR ADC 설계를 제시한다. 제안하는 적응형 스위칭 기법은 ECG의 양분된 신호 활성도 특성에 맞추어, 일반적인 SAR ADC처럼 입력의 전체 범위를 처리하는 full switching mode와, 5-bit MSB code가 변하지 않을 것이라는 가정하에 나머지 LSB 부분만 샘플링하고 처리하는 reduced switching mode의 두 가지 동작 모드를 가진다. 입력 신호 활성도에 따라 유연하게 동작 모드를 전환하기 위하여,

full switching mode는 MSBs tracking, reduced switching mode는 LSBs extrapolation라는 부가 기능이 각 모드의 주 기능과 함께 동작한다.

제안한 SAR ADC의 behavioral model을 MATLAB에서 만들었고, 이를 이용한 여러 테스트에서 적응형 스위칭 기법의 기능과 효과를 검증하였다. 이 behavioral model은 SAR ADC 내에 있는 segmented CDAC의 모든 내부 node 전압의 변화를 개별 스위칭 동작에 대해 기술하므로, 이를 이용하여 각 캐패시터에 저장된 전하의 변화량이나 스위칭 에너지 소비량을 계산할 수 있다. 이 model을 idea 개발 및 분석에 광범위하게 이용하였다.

0.18μm CMOS 공정에서 시제품 칩을 제작하였다. 심전도 유형의 입력 신호를 이용한 측정을 통해 제안한 적응형 스위칭 기법이 심전도 감시 분야에 적합함을 증명하였다. 제안한 기법으로 얻어지는 ADC의 전력 감소는 제안한 적응형 스위칭으로 동작한 경우와 full switching mode로 고정된 경우(기존의 SAR ADC 동작에 해당)에서 비교기, 논리 회로, DAC 3개 영역의 전력 측정값에서 계산하였다. 비교기 회로의 전력 소비는 39% 줄었다. DAC에서 소비된 전력, 즉 CDAC의 switching 전력 소비량은 1.28 nW가 감소했는데, behavioral model의 simulation 결과와 비슷한 값이다. 논리 회로 영역에서는 12%가 줄었다. 전체 전력 소비는 적응형 스위칭 기법을 적용했을 때 91.02 nW, full switching mode로 고정했을 때 107.51 nW으로 15.3% 감소하였다. 또, sine 입력을 이용하여 설계한 ADC의 기본 성능을 측정하였다. 그 결과 56.24dB의

SNDR과 62.00 dB의 SFDR을 얻었고, 비선형성 지표인 최대 DNL과 INL은 각각 +0.39/−1 LSBs와 +0.86/−1.5 LSBs 을 얻었다. 이 비선형성 특성은 주로 CDAC 내의 캐패시터 미스매치에 기인한 것이다.

주요어: SAR ADC, 심전도, 신호 활성도, 적응형 스위칭, 신호 특화.

학번: 2011-30973