Ph.D. DISSERTATION

A STUDY ON HIGH EFFICIENCY HIGH VOLTAGE ENVELOPE TRACKING RF POWER AMPLIFIER

고효율 고전압 포락선 추적 전력 증폭기에 관한 연구

BY

SUNGHWAN PARK

AUGUST 2017

SCHOOL OF ELETRICAL ENGINEERING AND
COMPUTER SCIENCE COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

A STUDY ON HIGH EFFICIENCY HIGH VOLTAGE ENVELOPE TRACKING RF POWER AMPLIFIER

고효율 고전압 포락선 추적 전력 증폭기에 관한 연구

지도 교수 서 광 석

이 논문을 공학박사 학위논문으로 제출함

2017 년 8 월

서울대학교 대학원

전기 · 컴퓨터 공학부

박 성 환

박성환의 공학박사 학위논문을 인준함

2017 년 8 월

위 원 장 남 상 욱 (인)

부위원장 서 광 석 (인)

위 원 권 영 우 (인)

위 원 천 창 율 (인)

위 원 김 정 현 (인)

Abstract

In this dissertation, two advanced techniques to solve system issues in envelope tracking power amplifier (ET PA) is presented.

First of all, a two-stage broadband CMOS stacked FET RF power amplifier (PA) with a reconfigurable interstage matching network is developed for wideband envelope tracking (ET). The proposed RF PA is designed based on Class-J mode of operation, where the output matching is realizedwith a two-section low-pass matching network. To overcome the bandwidth (BW) limitation from the high-interstage impedance, a reconfigurable matching network is proposed, allowing a triple frequency mode of operation using two RF switches. The proposed RF PA is fabricated in a 0.32- m silicon-on-insulator CMOS process and shows continuous wave (CW) power-added efficiencies (PAEs) higher than 60% from 0.65 to 1.03 GHz with a peak PAE of 69.2% at 0.85 GHz. The complete ET PA system performance is demonstrated using the envelope amplifier fabricated on the same process. When measured using a 20-MHz BW long-term evolution signal, the overall system PAE of the ET PA is higher than 40% from 0.65 to 0.97 GHz while evolved universal terrestrial radio access (E-UTRA) adjacent channel leakage ratios (ACLRs) are better than –33 dBc across the entire BW after memoryless digital pre-distortion. To our knowledge, this study represents the highest overall system performance in terms of PAE and BW among the published broadband ET PAs, including GaAs HBT and SiGe BiCMOS.

Second, a high-efficiency gallium-nitride (GaN) envelope amplifier (EA) is developed using class-E^2 architecture for wideband LTE applications. The proposed

EA consists of a class-E^2 resonant converter which output voltage is controlled by a frequency modulator. With a pulse frequency modulation (PFM) signal, the output of the converter can achieve a linear response to the input wideband envelope signal. The frequency modulator with a cross-coupled oscillator and a driver using stacked-FETs structure is fabricated using 0.28-μm SOI CMOS process. The class-E^2 converter and PA have been implemented using a commercial GaN device. The envelope amplifier (EA) achieves 74.7% efficiency into a 50 Ω load for a 20-MHz BW LTE signal with a 7.5 dB peak-to-average power ratio (PAPR) and there is no efficiency degradation as the LTE signal bandwidth increases to 160-MHz. The ET transmitter system demonstrated using the CMOS and GaN shows an overall system efficiency of 47.4% at 35.4 dBm with 20-MHz BW LTE signal centered at 3.5 GHz. The measured E-UTRA ACLR of ET PA is –33.8 dBc at 34.4 dBm output power before linearization and –42.9 dBc at the same output power after memory digital pre-destination (DPD). When tested using 80-MHz BW LTE signal, the overall system PAE reaches 46.5% at 35.3 dBm output power and E-UTRA ACLR was measured by –31.5 dBc at 34.4 dBm output power. A wideband performance is characterized using various bandwidth LTE signals which shows only 2.3 dB ACLR degradation without PAE degradation as the signal bandwidth is increased from 20- to 80-MHz. The proposed method is a first demonstration of GaN EA cover 160-MHz BW LTE signals and overcomes the efficiency degradation of the conventional EA as the signal bandwidth increase.

Keywords : Broadband, class-J, class-E^2 resonant converter, CMOS, dc-dc converter, digital pre-distortion (DPD), efficiency, envelope amplifier (EA),

envelope tracking (ET), GaN, long term evolution (LTE), long term evolution-advanced (LTE-A), multiband, power amplifier (PA), silicon-on-insulator (SOI), stacked FET, VCO, wideband.

Student number : 2012-20769

Contents

List of Tables

List of Figures

Chapter 1

Introduction

1.1 Motivation

Modern wireless communication system uses 4G long term evolution (LTE), and long term evolution-advanced (LTE-A) over 3G wideband code division multiple access (W-CDMA) and evolves into various complex modulation method. In the communication system, power amplifier (PA) is important component, which consumes the most power in the system. Thus, it is special challenge to design high-efficiency PA.

One issue in the PA design is to cover the bands of several fragmented modulation signals using a single-core high-efficiency PA. Fig. 1.1 shows LTE bands in use at sub-1 GHz by region. Due to the recent LTE deployment, it is possible around the world to reallocate the occupied frequency bands (called as “frequency re-farming”) at below 900 MHz. Therefore, it require one PA to cover all of these LTE bands, which will lead to advantage of reduction in size and cost of the system in accordance with the trend that make smartphone is getting smaller and thinner in recent mobile market.

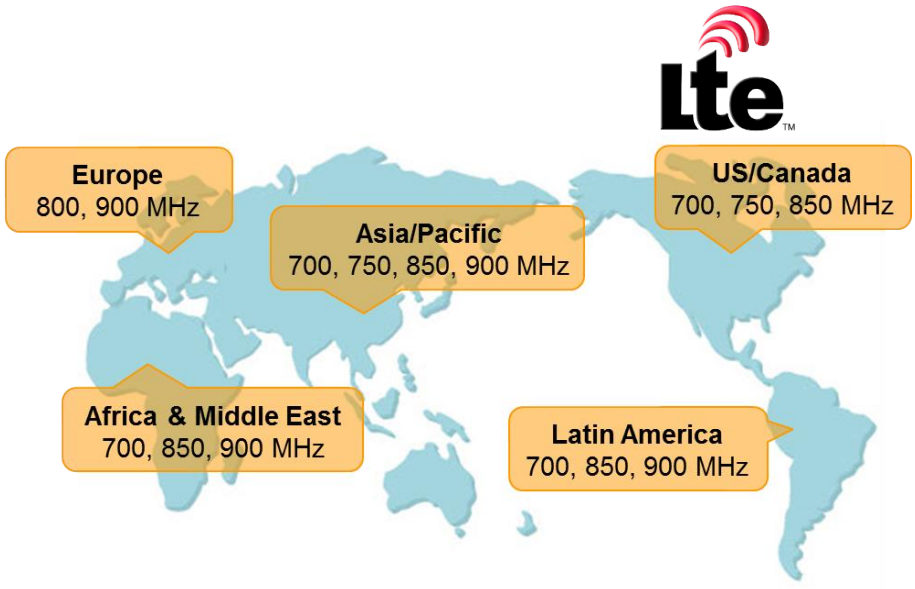


Fig. 1.1. LTE frequency band allocations by region

Another issue in PA is to increase efficiency in back-off power level. Recent PA needs to support the digital modulation signals with a wide range of peak-to-average power ratio (PAPR) such as quadrature phase-shift-keying (QPSK) and 16/64-quadrature-amplitude-modulation (16/64-QAM). It means that the PA should be operated in the back-off power region to meet the stringent linearity specification, which results in significant efficiency degradation. Moreover, the PAPR of wideband LTE-A signals whose maximum bandwidth is extended to 100-MHz by aggregating 5 carriers is generally higher than 9~10 dB. To improve the low efficiency at the back-off power, many efficiency enhancement techniques have been researched. The dynamic load modulation (DLM) techniques such as Doherty PA and adaptive load PA have been investigated for high efficiency at the back-off power. In case of Doherty PA, efficiency at the back-off power is increased by active load modulation of an auxiliary amplifier according to the power level using an impedance inverter.

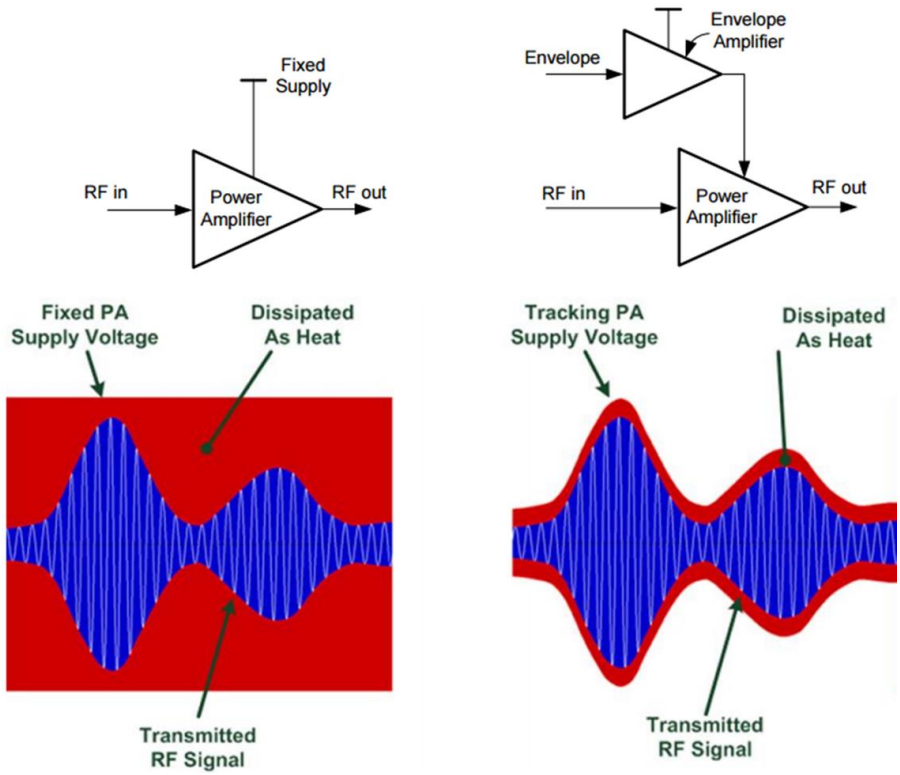


Fig. 1.2. The concept of envelope tracking RF power amplifier.

The load modulation is often achieved by a quarter-wavelength transformer, which has a limit for broadband operation. In addition to, Doherty PA has a nonlinearity problem due to auxiliary amplifier biased class-C. The adaptive load PA is a technique that changes the load impedance at the specific back-off power using a diode or switch devices. This technique has disadvantage that a step of AM-AM or AM-PM occurs at the time of load change, which worsens the linearity.

Recently, dynamic bias modulation technique such as envelope tracking (ET) is widely investigated. Fig. 1.2 shows the concept of the basic ET PA architecture. For the ET operation, the PA sets another additional circuit block called envelope amplifier (EA) or supply modulator (SM). In ET PA system, the drain (or collector)

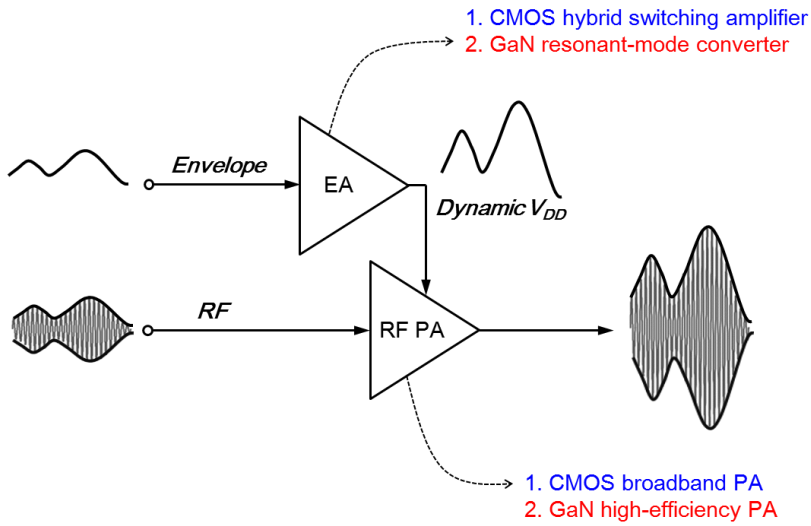


Fig. 1.3. The envelope tracking RF power amplifier architecture and scope of this work.

bias of the RF PA is dynamic modulated by the EA and its output tracks the shape of the input envelope so that the PA operates always in a saturation mode. Therefore, high efficiency can be maintained regardless of the output power level. In this dissertation, there are two system for ET technique. The one ET PA is fabricated in silicon-on-insulator (SOI) CMOS process and another ET PA is implemented by both SOI CMOS and commercial GaN device. In addition to, two advanced design techniques to overcome the several system level issues inherited by the inferior RF characteristics of the CMOS/GaN have been presented.

1.2 Dissertation organization

Fig. 1.3 is a block diagram that shows the scope of this dissertation. The scope of this work to design and implement the envelop amplifier (EA) and RF power amplifier (PA) for mobile and base-station applications. In the first ET PA system, a broadening technique for RF bandwidth of ET PA is introduced for mobile

applications. Second ET PA system is a widening technique for envelope bandwidth of ET PA for base-station applications.

In chapter 2, a two-stage stacked CMOS RF PA for broadband ET operation to cover the entire low-band LTE frequencies is presented. Although many researches have demonstrated broadband PA using class-J technique, most of reported PAs are designed using a single-stage architecture and the study of PAs using multi-stage hardly have been presented. In order to design broadband PA, high-Q limitation of interstage matching must be overcome. In this chapter, a reconfigurable interstage matching network is proposed, allowing a triple frequency mode of operation using two RF switched. The performance of the overall ET PA system with a proposed method has been measured using 20-MHz BW LTE signals, which indicates 13% enhancement of RF fractional BW showing higher than 40% PAE.

Chapter 3 focuses on the design of the EA that overcomes problems inherited from the conventional hybrid type EAs and the typical switched mode EAs. The proposed EA which is composed of frequency modulator and class-E^2 resonant converter is introduced in this chapter. To overcome limitation of typical pulse width modulation (PWM), pulse frequency modulation (PFM) method is applied and its operation principle and potential for wideband ET application are demonstrated. A wideband ET PA test using 80-MHz BW LTE signal is presented to clearly demonstrate the advantages of the proposed concept.

Finally the dissertation ends with conclusions in Chapter 4 which summarizes the three design techniques for RF PA and EA, demonstrated in this dissertation.

Chapter 2

Broadband CMOS Stacked Power Amplifier Using Reconfigurable Inter-stage Network for Envelope Tracking Application

2.1 Introduction

Rapid development of mobile communication calls for highly efficient RF power amplifiers (PAs) for extended battery life. However, to meet the stringent linearity requirement of the digital modulation signals, a PA should be operated in the back-off region, which results in significant efficiency degradation. The PA efficiency problem has become more serious with the introduction of the fourth generation long term evolution (4G LTE) standard, which requires peak-to-average power ratio (PAPR) as high as 6~7 dB. To overcome this problem, an envelope tracking (ET) technique is widely investigated, and several papers have reported excellent overall system PAEs using 10-/20-MHz bandwidth (BW) LTE signal [1]-[8]. Another challenge of the RF PA for LTE mobile phones is the need to cover a number of highly fragmented LTE bands using a single PA chain. The authors have

demonstrated a port-reconfigurable PA using a frequency reconfiguration network (FRN) in the output matching network to cover various frequency bands from a single output port [9]. However, PA reconfiguration for a given output port has limited practicality unless the duplexer filters following the PA can also be made frequency-tunable, which is technically difficult at this stage. More practical approach is to develop a broadband PA followed by a distribution switch to branch out the signals to each of the dedicated-band duplexer filter. Although there have been several reports for broadband PAs, most of works focused on the design of broadband load matching network for single-stage PAs [4], [10], [11]. However, multiple-stage design is required for the mobile phone PAs due to the high gain requirement. In the multi-stage PA design, the main design challenge for broadbanding may not come from the output load matching, but rather from the interstage matching which often turns out to be high-Q matching with narrow-band characteristics [12], [13].

In this work, a two-stage stacked CMOS RF PA is developed for broadband ET operation to cover the entire low-band LTE frequencies from 0.65 to 1.0 GHz. The output stage is based on a class-J architecture using the multi-section matching network with integrated Miller capacitors. Broadband matching in the interstage network is realized with a reconfigurable matching network using silicon-on-insulator (SOI) CMOS switches to select desired frequency bands. In this way, the matching bandwidth limitation set by Bode-Fano criteria can be overcome. This paper is an extended version of our previous paper [5] which reported the overall design concept and the first results using a single reconfiguration switch. The extended paper contains detailed operation principle and design procedure as well as

the updated results with wider RF bandwidth using two reconfiguration switches in the interstage network.

This paper is organized as follows. Section 2.2 gives a basic idea of the proposed broadband class-J PA with reconfigurable interstage matching network. In Section 2.3, the detailed design procedure of the proposed PA is presented using SOI CMOS FETs. Also shown in this section is the design of the envelope amplifier (EA) fabricated in SOI CMOS process. In Section 2.4, the measured PA characteristics are presented together with the time-domain waveform measurement to verify true Class-J operation. The entire ET PA system performance with 20-MHz BW LTE signal across the entire frequency range is also demonstrated in this section.

2.2 Two-stage Broadband Class-J PA

2.2.1 Review of the class-J PA

The core idea of class-J PA is to use second harmonic control to shape the voltage waveform close to half-sinusoid. To drive ideal impedance of class-J amplifier, a simplified analysis is required. Fig. 2.1 shows equivalent circuit of a FET. The active device is appropriately represented by a voltage controlled current source, shunted by a capacitor C_{ds}. Neglecting for simplicity other device parasitic phenomena and assuming a unilateral device, the current I_D supplied by the controlled source is imposed by the input driving signal only. The corresponding harmonic components (I_n) are given by:

$$I_n = \begin{cases} \frac{I_{max}}{\pi} \cdot \frac{\alpha - \sin(\alpha)}{1 - \cos\left(\frac{\alpha}{2}\right)} & n = 1 \\ \frac{2 \cdot I_{max}}{\pi} \cdot \frac{\sin\left(n \cdot \frac{\alpha}{2}\right) \cdot \cos\left(\frac{\alpha}{2}\right) - n \cdot \sin\left(\frac{\alpha}{2}\right) \cdot \cos\left(n \cdot \frac{\alpha}{2}\right)}{n \cdot \left(n^2 - 1\right) \cdot \left[1 - \cos\left(\frac{\alpha}{2}\right)\right]} & n \geq 2 \end{cases} \quad (1)$$

Where α is the represents the entire angle of conduction. Adopting simplified model, voltage harmonic components V_n are generated through the impedances loading the current source for each respective frequency. Thus, the output voltage waveform is consequently expressed as:

$$V_{DS} = V_{DD} - V_1 \cdot \cos(\omega t) - V_2 \cdot \cos(\omega t) - V_3 \cdot \cos(\omega t) + \cdots \quad (2)$$

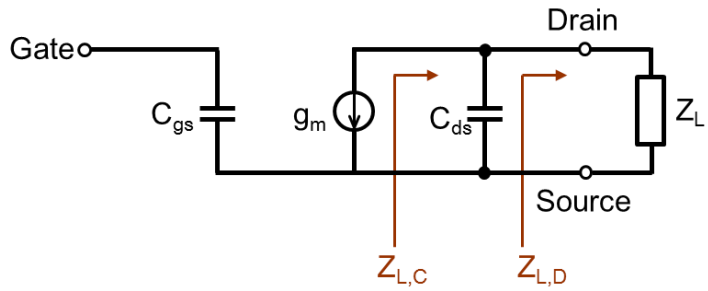


Fig. 2.1. Equivalent circuit of a FET for design of class-J.

Where V_{DD} is the dc bias voltage and the voltage harmonic component V_n is expressed as:

$$V_n = Z_n \cdot I_n \tag{3}$$

To simplify equation (2), normalized harmonic components to fundamental one is used as follow:

$$h_n = \frac{V_n}{V_1} \tag{4}$$

Assuming the higher order harmonic impedance is shorted by drain-source capacitance, the voltage waveform can be rearranged as:

$$V_{DS} = V_{DD} - V_1 \cdot \left[\cos(\omega t) - h_2 \cdot \cos(\omega t) \right] \tag{5}$$

For the conventional PA design, the optimum fundamental impedance is expressed as:

$$R_{opt} = \frac{V_1}{I_1} = 2\pi \cdot \frac{V_{DD} - V_k}{I_{max}} \cdot \frac{1 - \cos\left(\frac{\alpha}{2}\right)}{\alpha - \sin(\alpha)} \tag{6}$$

Where V_k is the device knee voltage limitation. For example, when the conventional PA is biased at the class-B, the optimum fundamental impedance can be expressed as:

$$R_{opt}\big|_{\alpha=\pi} = \frac{2\cdot(V_{DD} - V_k)}{I_{max}} \tag{7}$$

Because the class-J operation is biased at the class-B condition for half-sinusoidal current waveform, the conduction angle (α) of class-J amplifier is also π.

As mentioned earlier, the voltage waveform for the class-J amplifier is half-sinusoidal. To shape the voltage waveform close to half-sinusoid, the phase shift between current and voltage need to be 90° at second harmonic for reactive second harmonic termination. The mutual phase shift at fundamental frequency will therefore be 45° [15]. Also, the appropriate magnitude of the fundamental and second harmonic voltage is required. When a voltage gain function given by the ratio of the resulting fundamental voltage component $V_{1,J}$ of class-J PA normalized to the class-B PA case V_1, the function of voltage gain is expressed as:

$$\beta_J = \frac{V_{1,J}}{V_1} \tag{8}$$

Consequently, the load impedances for class-J amplifier are expressed as:

$$Z_1 = \beta_J \cdot \frac{2\cdot(V_{DD} - V_k)}{I_{max}} \angle 45^\circ \tag{9}$$

$$Z_2 = \beta_J \cdot h_2 \cdot \frac{3\pi}{2} \cdot \frac{(V_{DD} - V_k)}{I_{max}} \angle 90^\circ \tag{10}$$

In particular, the maximum-voltage gain condition ($\beta_J = \sqrt{2}$) can be achieved when normalized second harmonic component (h_2) is $-\sqrt{2}/4$ [15]. Thus, the ideal fundamental and second harmonic impedances of the class-J amplifier are given by $Z_1 = R_{opt} \cdot (1 + j)$, $Z_2 = -j3\pi \cdot R_{opt}/8$ at the intrinsic drain current source.

2.2.2 Bandwidth Limitation in Multi-stage PAs and Proposed Solution

Generally, more than two-stage design is required to achieve the gain requirement for the handset RF PAs (>24 dB). In a two-stage RF PA, the bandwidth limitation may not come from the output matching, but from high-Q interstage matching due to the excessively large input capacitances of the power cell. In other words, the broadband output load matching alone may not be sufficient in meeting the required PA specification in terms of efficiency, gain and power. For example, if the bandwidth of the interstage matching is small, the drive power to the main stage will not be sufficient at the band edges to meet the overall gain and power target, let alone the efficiency.

To investigate the bandwidth limitation of the interstage matching, we have modeled the input of the power stage transistor as a series combination of a resistor,

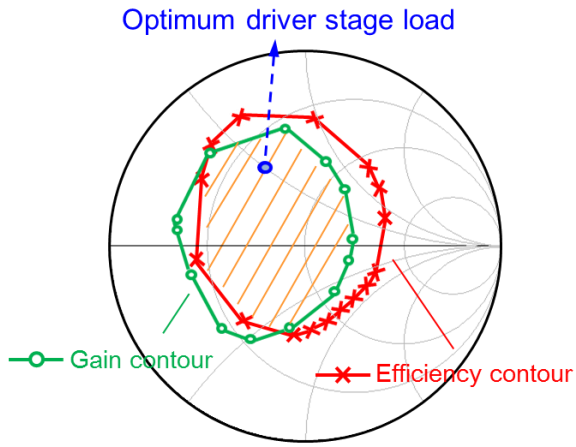


Fig. 2.2. Simulated driver-stage loadpull contour representing the load contours that generate the same output power as that available from the optimum load impedance shown with the blue dot. The red curve with cross represents the load contour that increases the driver current by 50%. The green curve with circle represents the load contour that decreases the gain by 6 dB. To meet both gain and efficiency targets, the driver-stage mismatch should stay within the shaded area across the entire bandwidth.

R, and a capacitor, *C*, which is a valid equivalent circuit representation of a common-source CMOS FET. For example, CMOS triple-stacked power cell used in our work has an input capacitance (*C*) of 36 pF with a series resistance (*R*) of 1 Ω at 0.85 GHz. The theoretical bandwidth limit of the interstage matching network can be expressed as Eq. (1) using Bode-Fano criteria [14].

$$\int_0^\infty \frac{1}{\omega^2} \ln \frac{1}{|\Gamma(\omega)|} d\omega < \pi RC \tag{11}$$

where Γ(ω) is the reflection coefficient referenced to the optimum load impedance of the driver stage transistor. To estimate the bandwidth limitation, we need to set the allowable mismatch, |Γ(ω)|, for the interstage matching.

There can be two criteria in setting the allowable mismatch, $|\Gamma(\omega)|$. First, the overall efficiency of the two-stage PA should remain higher than a certain threshold across the entire bandwidth. Even if the power stage remains unchanged in terms of gain and efficiency across the entire bandwidth, the load mismatch to the driver stage will increase the overall dc current, which is the sum of the driver-stage current and the power-stage current. Fig. 2.2 shows the loadpull contours of the driver stage only. The red curve with cross represents the driver load contour, which results in 50% increase in the driver-stage current while meeting the same output power target compared with the optimum driver-stage load point, shown as a blue dot. The actual two-stage stacked CMOS PA without the interstage reconfiguration is used in the loadpull simulation. The detailed PA circuit design will be described in Section 2.3.

Another criterion is the overall gain. The load mismatch to the driver stage results in the degradation of the driver gain, which should be less than a certain limit so that the overall gain can still meet the pre-defined system specification across the entire bandwidth. We have used 6 dB gain window as a criterion. The green curve with circle in Fig. 2.2 shows the load contour that results in 6 dB gain degradation in the driver stage while meeting the same output power target as that from the optimum load point (blue dot). To meet both gain and efficiency targets for the two-stage PA, the driver-stage load mismatch should stay within the overlap area between these two contours, represented as shaded region in Fig. 2.2, across the entire RF bandwidth.

From the circuit simulation of the two-stage PA used in this work, the maximum achievable fractional bandwidth is only 23.5% (0.75 to 0.95 GHz) to stay within the shaded region if a single-section matching is used for interstage matching. The

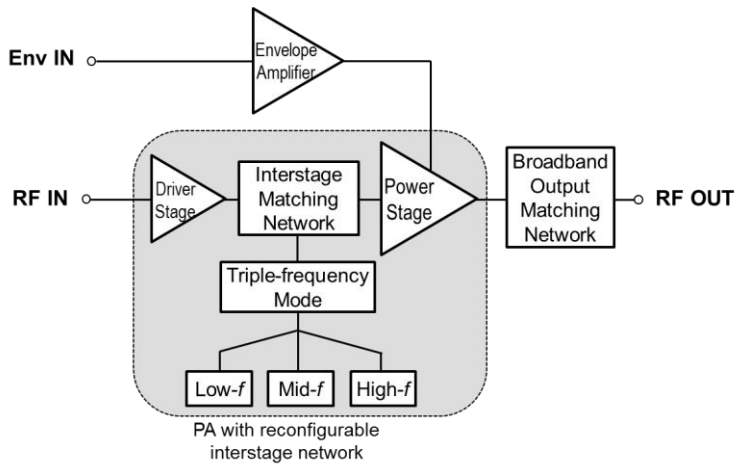


Fig. 2.3. The basic block diagram of the proposed broadband ET PA with reconfigurable interstage matching.

bandwidth can increase by employing a larger number of sections, but is still bound by Eq. (11), which applies to the case of the infinite number of sections. There is a practical limit in the number of sections for interstage matching in terms of the die size and the associated loss in the matching circuit. It is also worthwhile to note that the driver-stage mismatch analysis presented above is based on the assumption that the power stage is of infinite bandwidth and does not impose any bandwidth limitations, which of course is not always true in the practical PA design. The actual bandwidth of the two-stage PA will be smaller than those predicted in our analysis.

To extend the fractional bandwidth above 40% using the two-stage PA design, which is required to cover all the LTE bands below 1 GHz using a single PA chain, we would need a different design methodology for interstage matching. In this work, a frequency-selective reconfigurable interstage matching network is proposed as a solution. The key idea is to divide the frequency range into several frequency sub-bands and change the matching component values of the interstage matching

network according to the sub-divided frequency bands. In this way, the aforementioned bandwidth limitation can be overcome and the optimum load impedance can be presented to the driver stage at each sub-band.

The Fig. 2.3 is the overall block diagram of the proposed broadband ET PA with a reconfigurable interstage network. Overall efficiency enhancement at the back-off power is achieved through the use of envelope tracking, where the envelope signal is amplified by the envelope amplifier and applied to the drain bias for dynamic bias modulation. The reconfigurable matching network is employed in the high-Q interstage matching network, where the three different modes are selected according the frequencies. Finally, the broadband output matching is implemented through the use of class-J operation as will be explained in the next sub-section.

2.2.3 Output Matching Network

As explained in the previous chapter 2.2.1, the output matching network for class-J operation should provide the optimum impedances at each harmonic frequency as governed by following three equations [15]

$$Z_1 = \frac{2\sqrt{2}\cdot(V_{DD}-V_k)}{I_{max}}\angle 45^\circ \tag{12}$$

$$Z_2 = -\frac{3\pi}{4}\cdot\frac{(V_{DD}-V_k)}{I_{max}}\angle 90^\circ \tag{1(3)}$$

$$Z_n(n>2) = 0 \tag{14}$$

The third condition is typically satisfied by assuming that third and higher order harmonic currents are short-circuited through the drain-source capacitance (C_{ds}) of

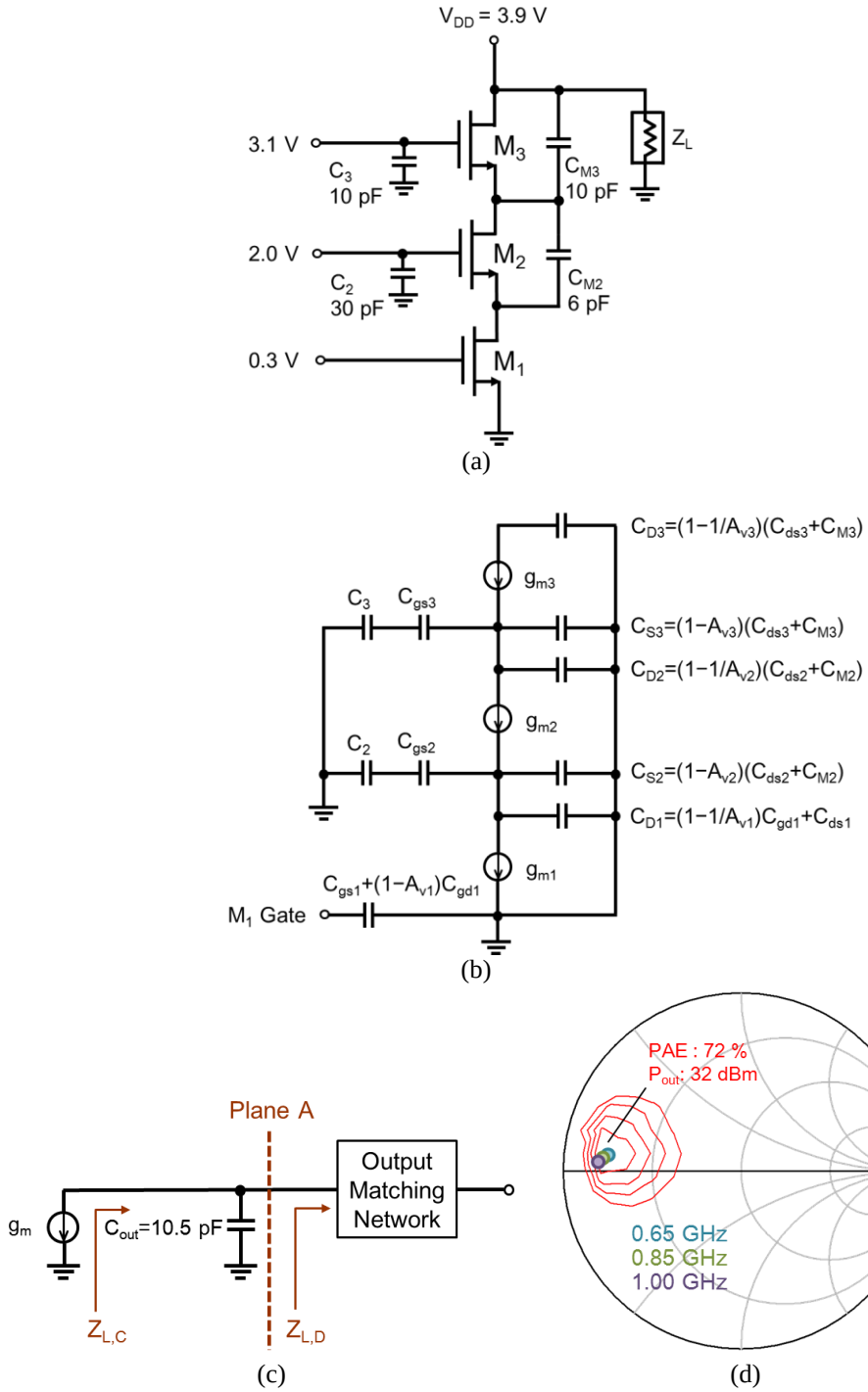


Fig. 2.4. (a) Schematic of the triple-stack power cell. (b) The detailed equivalent circuit of the power cell with the Miller capacitors decomposed. (c) The simplified equivalent circuit of the power cell. (d) The fundamental loadpull contours of the power cell simulated at Plane A for 0.65, 0.85 and 1 GHz.

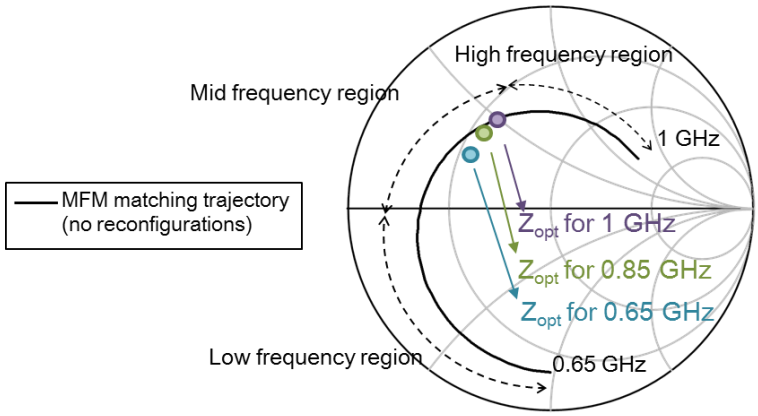
the power cell. If C_{ds} of the power cell is not large enough to short third harmonic currents, extra shunt capacitor is needed at the drain node of the power cell. In this work, as shown in Fig. 2.4 (a), triple-stacked CMOS FET with a unit gate width of 20 mm is used as a power cell, whose C_{ds} is 15.5 pF. The value of C_{ds} of the 20 mm unit transistor is extracted using the device model and confirmed by *S*-parameter simulation using ADS. The detailed equivalent circuit of the output portion of the triple stack cell is shown in Fig. 2.4 (b), where the output capacitors across each FET stack are decomposed to the Miller capacitors. Based on this equivalent circuit, the overall output capacitor (C_{out}) of the triple stack is calculated to be 10.5 pF. The simplified equivalent circuit shown in Fig. 2.4 (c) is used when calculating the load impedance at the current source plane. This overall output capacitance provides a reactance of only $-j6\ \Omega$ at third harmonic frequency (2.55 GHz), which is sufficient to short-circuit third harmonic current.

The loadpull simulation is performed at the plane A shown in Fig. 2.4 (c) at 0.65, 0.85, 1 GHz. For the loadpull simulation in Fig. 2.4, the input power and impedance are fixed at 21 dBm and 50 Ω, respectively, and V_{DD} is 3.9 V. The fundamental load was varied for loadpull simulation while the second harmonic impedance was fixed at the optimum values for PAE. Fig. 2.4 (d) shows the optimum load impedances for PAE at the plane A the fundamental frequencies. The optimum load impedances at the fundamental frequencies are centered around $5.2 + j4.1\ \Omega$ from 0.65 to 1 GHz. It is worthwhile to note that $5.2 + j4.1\ \Omega$ is the impedance at the plane A ($Z_{L,D}$), which does not include the effect of C_{out}. The load impedance seen at the current generator plane ($Z_{L,C}$) is $7.2 + j3\ \Omega$. Even though it is not the ideal class-J load, it stays within class-J load region and provides the optimum performance between the output power

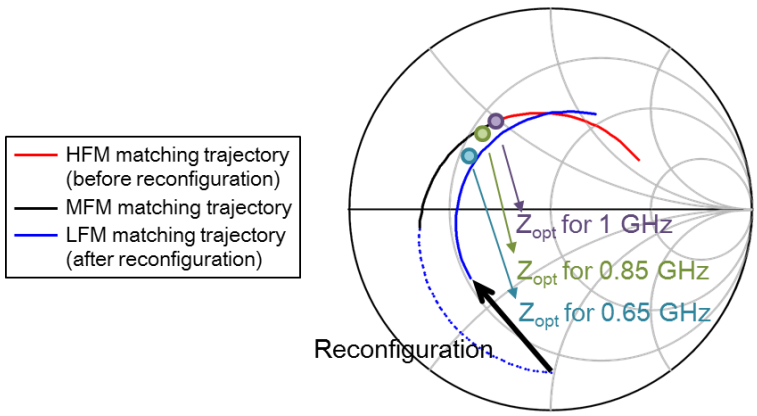
and the efficiency, as demonstrated in [16]; slight load tuning helps to increase the output power while achieving the similar level of PAEs. In this case, one then needs to design a broadband load matching circuit to satisfy the intrinsic impedances conditions of (13) and (14) at the harmonic frequencies while hitting the optimum load condition of (12) at the fundamental frequencies. As the optimal fundamental impedances have low Q factor (~0.79), it can be possible to design the broadband matching network. There are numerous impedance matching circuit topologies to realize broadband matching with a 1:n impedance transform ratio [14], [17]. In this work, a two-section low-pass network consisting of transmission lines and two shunt capacitors is used to synthesize near-optimum load impedances from 0.65 to 1.0 GHz, corresponding to the fractional bandwidth of ~40%. Detailed design of the load matching circuit and the simulation results are shown in Section 2.4.

2.2.4 Reconfigurable Interstage Matching Network

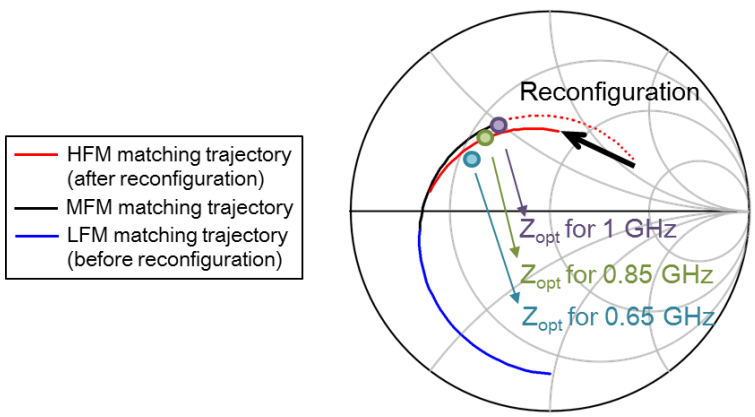
The simulated driver impedances optimum for PAE are shown with dots in Fig. 4 for 0.65, 0.85 and 1.0 GHz. As in the load impedance simulation results in Fig. 2.5 (b), the optimum driver impedances are scattered around $21 + j20\ \Omega$, and the input impedances seen looking into the power cell are around $1.1 - j7.2\ \Omega$. The corresponding Q factor is around 6.5, which is much higher than that of the optimum load impedance of the power cell (0.79) in Fig. 2.4 (d). To show the challenges of a typical interstage circuit to transform the input impedance of the power cell to the optimum driver impedance across the entire frequency range, the impedance trajectory versus frequency with a typical *C-L-C* interstage matching network optimized at 0.85 GHz is also plotted in the Fig. 2.5 (a). It can be noticed from Fig.



(a)



(b)



(c)

Fig. 2.5. Simulated optimum load impedances of the driver stage at 0.65, 0.85 and 1 GHz and the driver load trajectory from 0.65 to 1.0 GHz. (a) Without any interstage reconfiguration. (b) With LFM reconfiguration. (c) With HFM reconfiguration.

2.5 (a) that the driver impedance trajectory sweeps almost half of the Smith chart from 0.65 to 1 GHz, resulting in large impedance mismatches at the band edges. This will lead to the excessive power consumption from the driver stage, and makes it impossible to meet the overall PAE target from the two-stage PA, especially at low and high frequency edges.

Instead of a fixed matching network, a reconfigurable interstage matching network is employed in this work to reconfigure the interstage matching according to the frequency of operation. The entire frequency range is divided into three sub-bands, low from 0.65 to 0.8 GHz, mid from 0.8 to 0.9 GHz and high from 0.9 to 1 GHz. Depending on the frequency of operation, the interstage matching component is reconfigured to provide the optimum matching for each sub-band. In this way, bandwidth requirement can be reduced. For example, when the RF PA is operated in the mid frequency sub-band (0.8 to 0.9 GHz), the interstage matching network remains in the mid frequency mode (MFM), which is “as-is” state, to provide the optimum driver impedance at the 0.85 GHz as shown with a black curve in the Fig. 2.5 (a). When operated in the low frequency sub-band, the interstage matching network is reconfigured to the low frequency mode (LFM), where the matching network components are optimized for 0.75 GHz as depicted with blue curve in Fig. 2.5 (b). Similarly, for high frequency sub-band, the interstage matching network is reconfigured to the high frequenjcy mode (HFM) for optimum performance at 0.95 GHz, as represented with red curve in the Fig. 2.5 (c). The additional components required for the interstage circuit reconfiguration are two RF switches and extra capacitor and inductor. Detailed design procedure to implement reconfigurable interstage matching network is presented in the next section.

2.3 Design and Implementation of ET PA

2.3.1 Power Amplifier Design

Overall circuit schematic of a proposed two-stage class-J CMOS PA is shown in Fig. 2.6. Triple-stacked FET structure is selected for both stages to overcome the low breakdown voltage problem of CMOS FETs [18]. The gate widths of the unit FETs are 2 mm and 20 mm for driver stage and power stage, respectively. Gate terminal capacitors, $C_{g,5}$, $C_{g,4}$, $C_{g,3}$ and $C_{g,2}$ are designed to 3, 6, 10 and 30 pF, respectively, to ensure that the voltage swing can be evenly distributed to each FET in the stack. As shown in Fig. 2.6, the gate bias of the common-source FET (M_1) is applied directly through a bias resistor while the gate biases of the common-gate transistors (M_2 and M_3) are applied using a resistor-based voltage dividing circuit. The gate bias level for the common-source FET is set for Class-B operation to generate the half-sinusoid current while the biases to the common-gate FETs are selected to achieve uniform voltage swing between M_2 and M_3. The gate length for all FETs is 0.32-μm, which is selected based on the breakdown requirement.

Two Miller capacitors ($C_{M,3}$,=10 pF, $C_{M,2}$=6 pF) are added across M_3 and M_2 to adjust the second harmonic impedance seen at the inner stacks of the power cell. Fig. 2.7 (a) shows the second harmonic loadpull simulation at the drain node of the M_2, which was performed in MFM at the drain of M_2 while the output impedance of the entire triple stack was fixed at the optimal load impedance shown in Fig. 2.4 (d). The same conditions were used for V_{DD}, input power and impedance as the fundamental loadpull simulation shown in Fig. 2.4. Fig. 2.7 (a) clearly shows that the high-efficiency region is shifted from the capacitive to inductive region due to the reactive effect of C_{ds} in M_2. Unfortunately, the load impedance seen from M_2, which is the

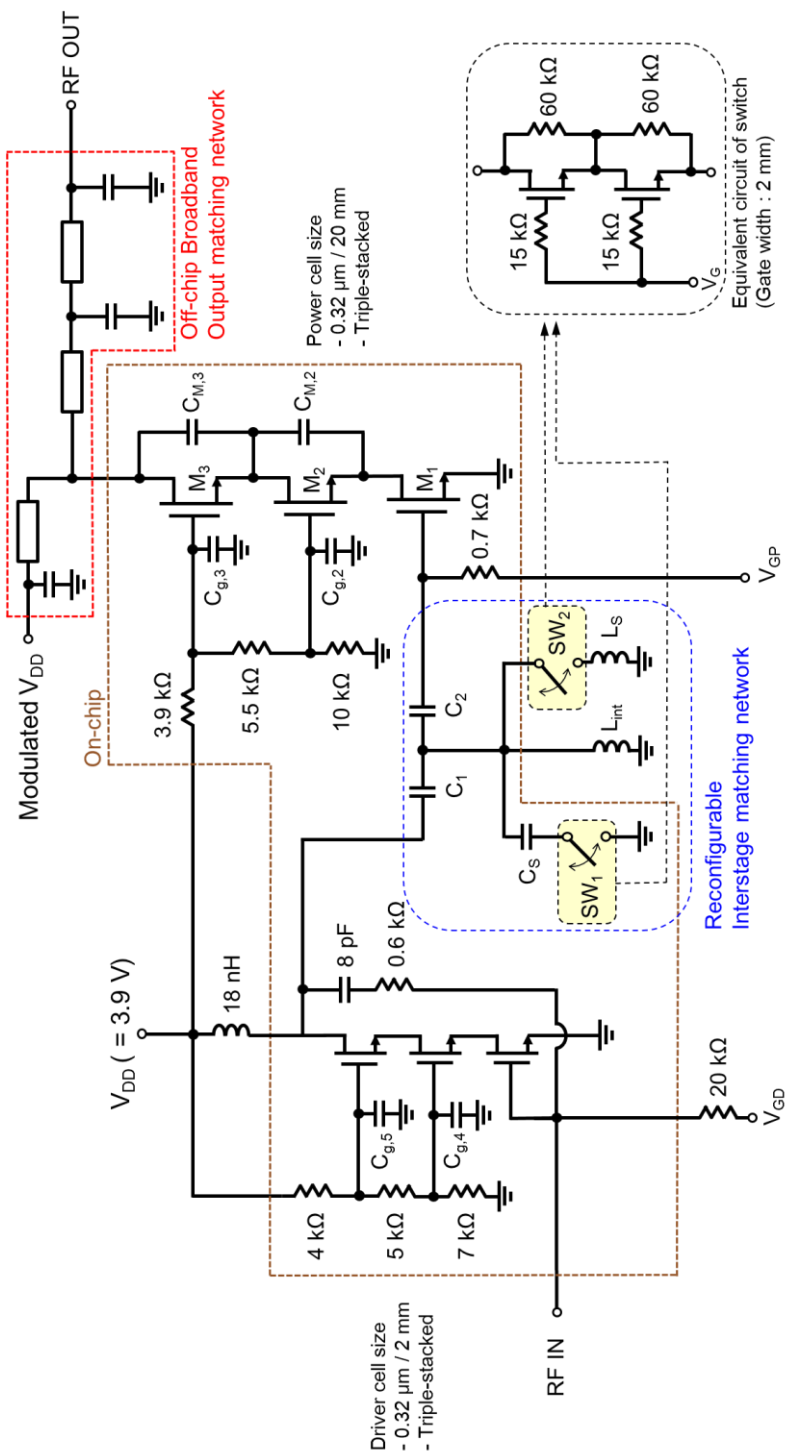


Fig. 2.6. Detailed circuit schematic of the proposed 2-stage CMOS stacked PA with reconfigurable interstage network.

input source impedance of M_3, at the second harmonic frequency lies in the capacitive region, resulting in low PAE. This is due to the large input capacitance of M_3 ($C_{eq,3}$), which consists of $C_{g,3}$ and $C_{gs,3}$, where $C_{gs,3}$ is the gate-source capacitances of the M_3. This problem can be solved by adding Miller capacitor across the drain and source terminals of M_3, which transforms the second harmonic impedance to the inductive region by adding negative capacitance. As shown in Fig. 2.7 (b), Miller capacitor can be replaced with two equivalent shunt capacitors at the source ($C_{n,3}$) and drain ($C_{p,3}$) terminals. The shunt capacitor values are expressed as

$$C_{p,3} = \left(1 - \frac{1}{A_{v,3}}\right) \cdot C_{M,3} \tag{15}$$

$$C_{n,3} = \left(1 - A_{v,3}\right) \cdot C_{M,3} \tag{16}$$

where $A_{v,3}$ is an intrinsic voltage gain of CG-FET (M_3) and $C_{M,3}$ is Miller capacitor across the source and drain terminals of CG-FET. As the CG-FET has positive voltage gain ($A_{v,3}$) greater than unity, the equivalent capacitor at the source node ($C_{n,3}$) has large negative capacitance. The positive term ($C_{p,3}$) can be used as a part of output capacitances for satisfying Eq. (14). The negative capacitor ($C_{n,3}$) effectively transforms the second harmonic load impedance of M_2 to the high PAE region by canceling out a portion of $C_{eq,3}$. This effect is shown in the simulated second harmonic load impedance of M_2 in Fig. 2.7 (a). Similar effects can be seen for M_1 harmonic load impedances from Miller compensation applied to M_2.

The effect of Miller capacitors is also verified by the voltage waveform analysis in the power cell. Fig. 2.7 (c) is the simulated drain-source voltage swing of M_1, M_2

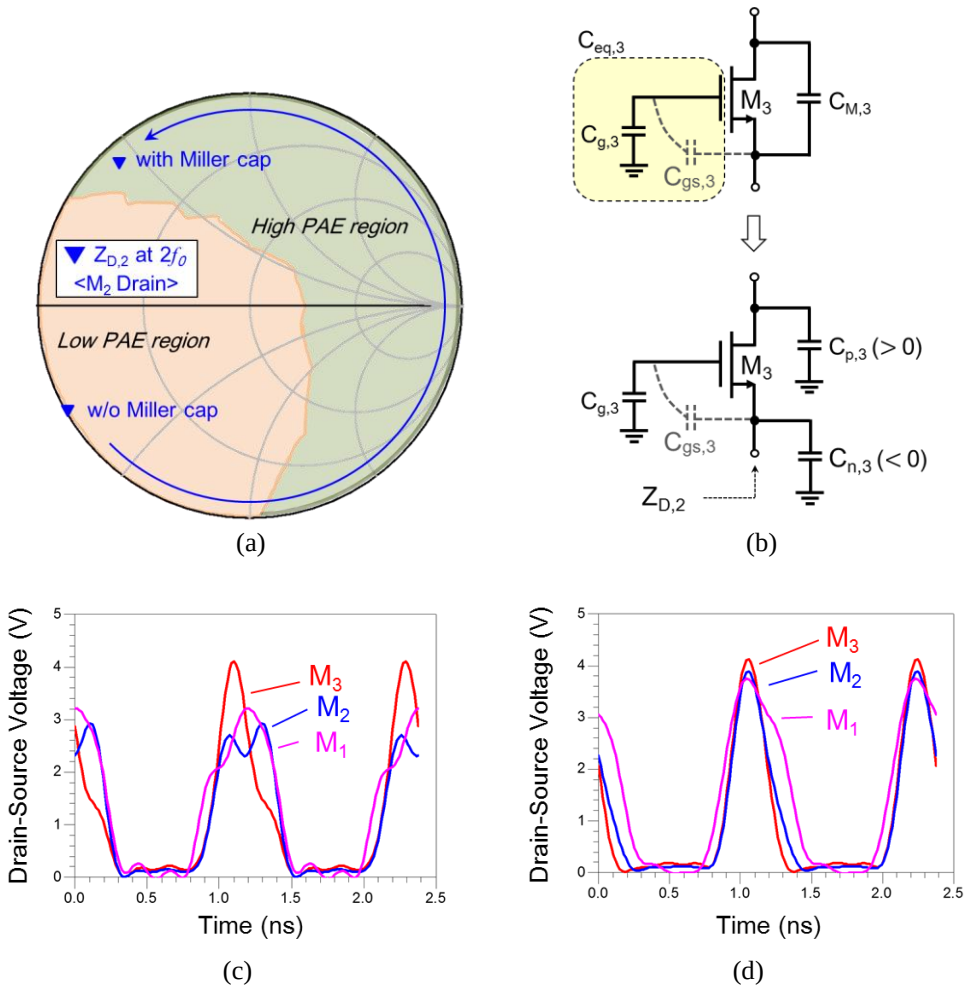
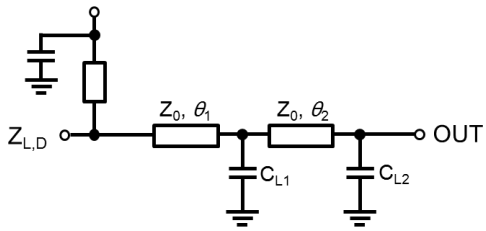


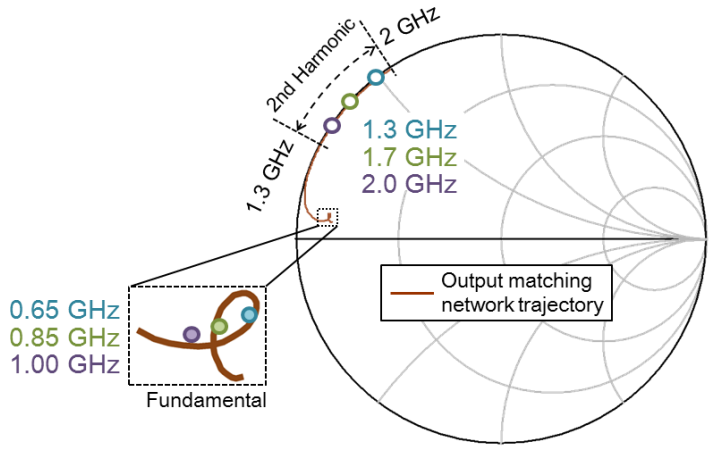
Fig. 2.7. (a) Simulated loadpull contour and load impedance presented to M_2 drain with and without Miller capacitor. (b) Effect of Miller capacitance. Simulated drain voltage waveforms. (c) Without Miller capacitors and (d) With Miller capacitors.

and M_3 without Miller capacitors. Unlike the drain-source voltage swing across M_3, which is close to the ideal waveform of half sinusoid, the voltage swing across M_1 and M_2 are heavily distorted due to the effect of capacitive second harmonic load impedance. The effect of Miller capacitances can be clearly observed in the waveform plot of Fig. 2.7 (d), where the same waveform simulation is performed by adding two Miller capacitors. Due to the negative capacitance effect, the overall

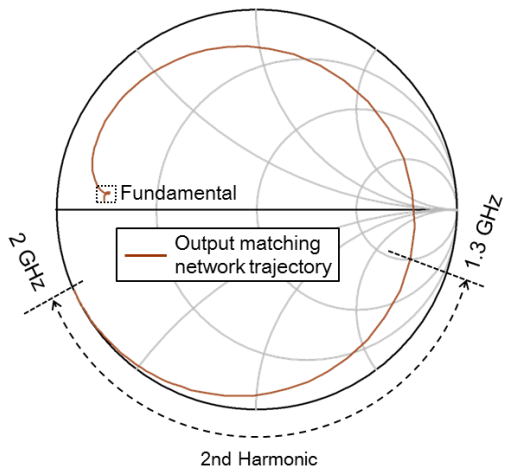


Components in OMN	
θ_1	11.6˚
C_{L1}	15 pF
θ_2	36.8˚
C_{L2}	4.3 pF

(a)



(b)



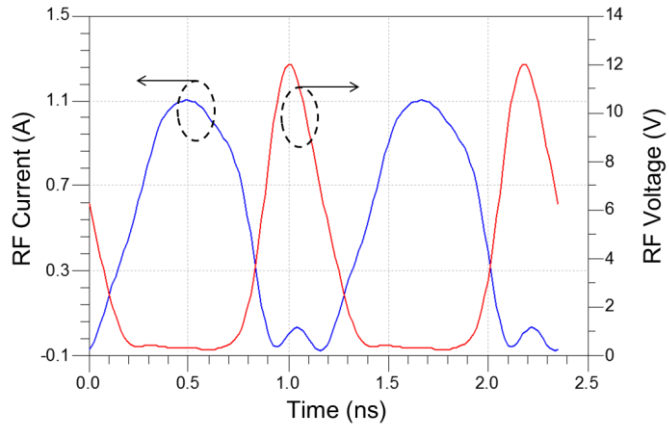
(c)

Fig. 2.8. (a) Circuit schematic of the two-section low-pass matching network used as the output load matching. (b) Optimum load impedance targets from 0.65 to 1.0 GHz and the simulated impedance trajectory of the output load matching circuit at the plane A ($Z_{L,D}$). (c) Simulated impedance trajectory of the output load matching circuit at the current generator plane ($Z_{L,C}$).

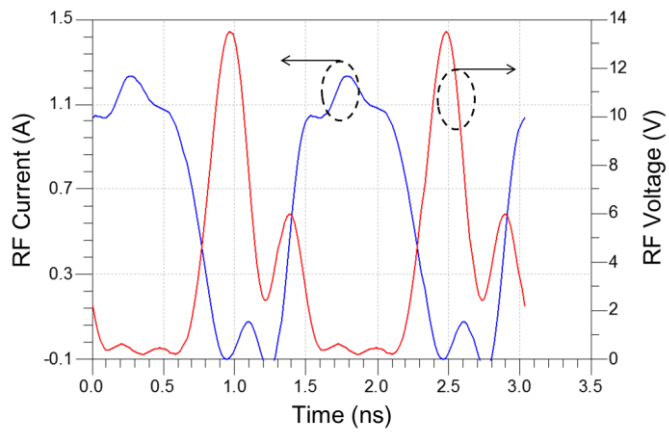
capacitive loading has been vastly reduced and the voltage swing is now recovered to almost half sinusoid, close to the ideal class-J operation.

The broadband output matching network is realized using the two-section low-pass matching network with an impedance transform ratio of 1:10 extracted from [17]. The design parameters of the output matching network are shown in Fig. 2.8 (a) while the simulated load impedance trajectory from 0.65 to 1 GHz is shown in Fig. 2.8 (b). The fundamental load impedance from 0.65 to 1 GHz is centered around the target impedance of 5.2 + *j*4.1 Ω, which was calculated from the loadpull simulation of the power cell shown in Fig. 2.4 (d). After de-embedding the overall output capacitance (C_{out}) of 10.5 pF, the fundamental impedance (Z_{Fund}) and the second harmonic impedance (Z_{H2}) at the current generator plane are calculated as 7.2 + *j*3 Ω and 0.11 − *j*12 Ω, respectively, at 0.85 GHz (see Fig. 2.8 (c)). These impedances show the typical characteristics of class-J PA with the inductive fundamental load and capacitive second harmonic load. Simulated insertion loss of the output matching network at 0.85 GHz is 0.3 dB.

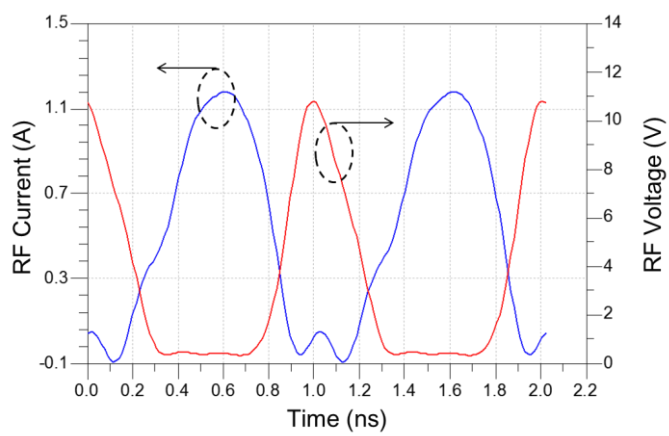
To verify class-J operation across the entire bandwidth, the voltage and current waveforms have been simulated at the current generator plane of the power cell at *P*1 dB condition. At the center frequency of 0.85 GHz shown in the Fig. 2.9 (a), the voltage waveform shows clean half sinusoid with the corresponding PAE of 72.3%, which validates optimal class-J operation. As the operating frequency is lowered, the third harmonic currents are no longer shorted through C_{out} of the power cell, which builds up third harmonic voltage components and distorts the voltage waveform as shown in the simulation results at 0.65 GHz (see Fig. 2.9 (b)). The distortion in the voltage waveform increases the overlap between the current and voltage waveforms



(a)



(b)



(c)

Fig. 2.9. Simulated voltage and current waveforms at the current generator plane of the power cell at (a) 0.85 GHz. (b) 0.65 GHz. (c) 1 GHz.

and degrades PAE to 64.4%. On the other hand, as the frequency increases, the peak voltage level decreases since the second harmonic current bypasses through C_{out} and fails to build up the second harmonic voltage, as shown in the simulation results at 1 GHz (see Fig. 2.9 (c)). The corresponding PAE degradation is around 6% at 1 GHz. This basically shows that there is a practical limit in extending the bandwidth due to the non-ideal Class-J operations of the power cell at the band edges. The goal of the reconfigurable interstage matching network is to extend the bandwidth of the entire two-stage PA as wide as the limit set by the power cell and the output matching network used in this work.

The reconfigurable interstage network introduced in the previous section is realized using two RF switches, which are fabricated using the same SOI CMOS process. 2-mm double-stacked NFET is used as a switch unit cell. One switch (SW_1) is integrated with the driver and power cell FETs, and the other switch (SW_2) is externally added for the high frequency mode (HFM) operation, as shown in Fig. 2.6. The overall interstage matching network is a high-pass network consisting of a series C_1 (=5 pF), a shunt L_{int} (=1.5 nH) and a series C_2 (=20 pF). For matching reconfiguration, the equivalent inductance of L_{int} is changed according to the operation frequency. When the RF PA is operated in the mid frequency mode (MFM, 0.8 to 0.9 GHz), both switches remain in the OFF-state to provide the "as-is" shunt inductance (L_{int}=1.5 nH). This provides the optimum driver load impedance of 21.3 + j19.8 Ω at 0.85 GHz. Therefore, the overall PAE peaks to 72.3% at the 0.85 GHz degrades at the band edges. To boost the efficiencies at lower frequencies, the interstage matching network is reconfigured to the low frequency mode (LFM, 0.65 to 0.8 GHz) by turning on SW_1, which effectively adds a shunt capacitance, C_S, and

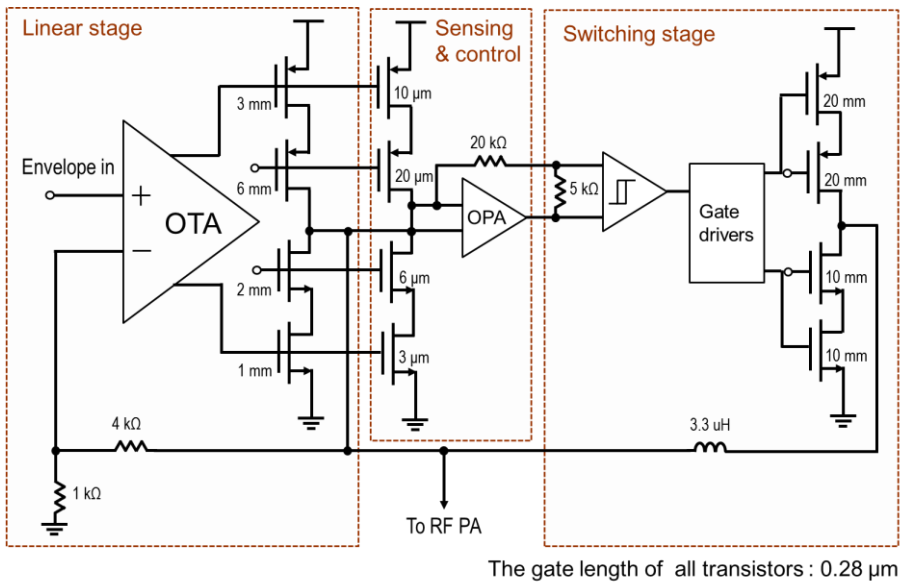


Fig. 2.10. Schematic of the designed envelope amplifier.

thus increases the equivalent shunt inductance to $L_{int} / (1 - \omega^2 \cdot L_{int} \cdot C_S)$. In this case, the optimum load impedance is presented to the driver stage at 0.7 GHz, where PAE improvement as much as 8% is achieved from the simulation. On the other hand, for efficiency boosting in high frequency mode (HFM, 0.9 to 1 GHz), SW_2 is turned on to add a shunt inductance (L_S=7 nH), which reduces the equivalent shunt inductance to $L_{int} \cdot L_S / (L_{int} + L_S)$. The simulated PAE improvement by HFM reconfiguration is as much as 5% at 1 GHz.

2.3.2 Envelope Amplifier Design

We have also designed an envelope amplifier to demonstrate entire ET PA system performance. A typical hybrid type envelope amplifier is designed to achieve both high efficiency and linearity [1]-[8]. Fig. 2.10 shows an overall schematic of the designed envelope amplifier. Output FETs for both stages are cascoded to avoid

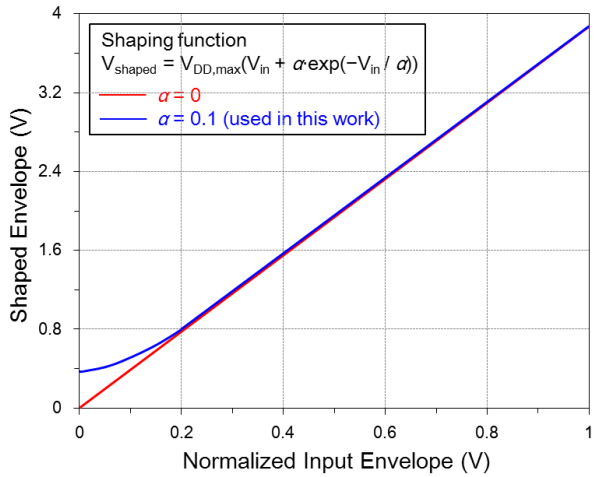


Fig. 2.11. Envelope shaping function used for ET testing

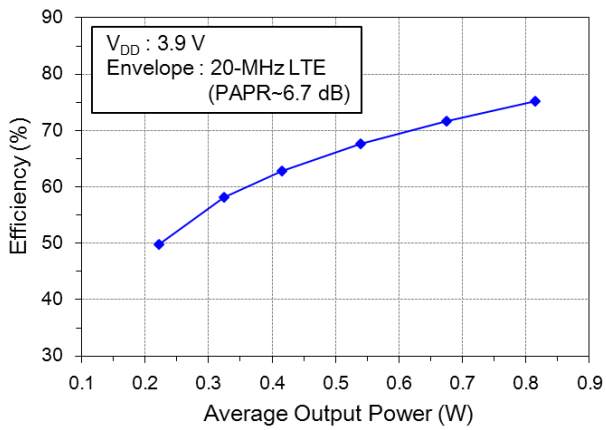


Fig. 2.12. Measured efficiency of the envelope amplifier when the input signal is the envelope of 20-MHz BW 6.7 dB PAPR QPSK LTE signal.

drain-source voltage breakdown thus operated with 3.9 V V_{DD} supply [19]. According to the small signal simulation, the gain bandwidth product of the linear stage is 170 MHz with 70˚ phase margin, which is sufficient to handle 20-MHz BW LTE signal. Fig. 10 shows the shaping function used in the ET testing to avoid the device shut down at the low envelope levels [7]. The measured efficiency of the

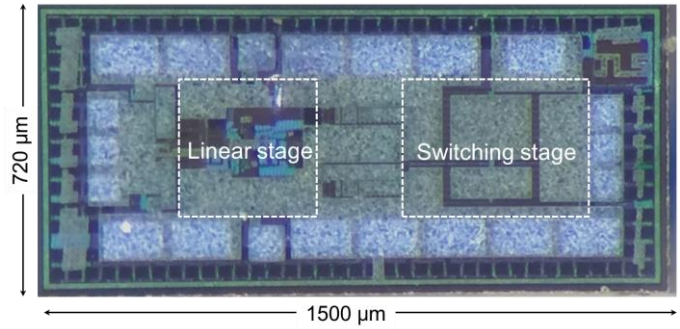
envelope amplifier with 20-MHz BW, 6.7 dB PAPR QPSK LTE envelope signal with 7.5 Ω resistive load is plotted in the Fig. 2.12, showing 74% average efficiency. This efficiency is smaller than the-state-of-the-art results of 86% [20] due to less sophisticated design. However, since the main purpose of this work is to demonstrate the broadband ET PA with a reconfigurable network, all the ET system measurements were taken with the fabricated EA.

2.4 Measurement Results

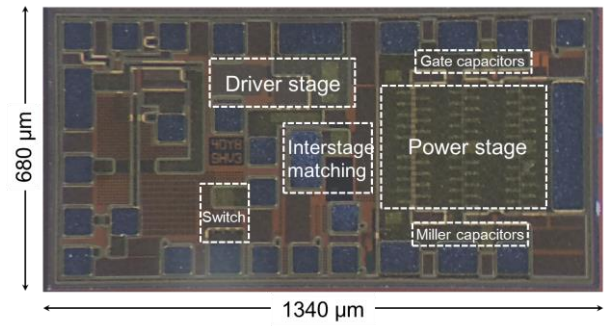
Two-stage stacked-FET PA with the proposed reconfigurable interstage matching network is fabricated using 0.32-μm SOI CMOS process. Fig. 2.13 (a) and (b) show the die photographs of the fabricated EA and PA, respectively. The chips are mounted on a 400-μm thick, 5 cm × 5 cm sized FR4 PCB (ε_r ~ 4.6, tanδ = 0.025), where the load matching circuits are realized and external components are mounted. The circuit components outside the dotted box in Fig. 2.6 are off-chip components mounted on the PCB.

Fig. 2.14 shows the measured small-signal *S*-parameters of the fabricated PA module. The PA shows different gain and return loss profiles according to each frequency mode. Fig. 2.15 shows CW power sweep data measured at 0.65 GHz to demonstrate the effect of the interstage reconfiguration. The output power is 29.8 dBm with 52.3% peak PAE without interstage reconfiguration. With interstage reconfiguration, peak PAE improves by ~9% while the output power and gain increase by 1.2 and 1.9 dB, respectively. *P*1 dB shows similar improvement from 28.6 to 29.7 dBm. Fig. 2.16 shows the measurement result of the intermodulation distortion (IMD) using two-tone signals with 20-MHz tone spacing.

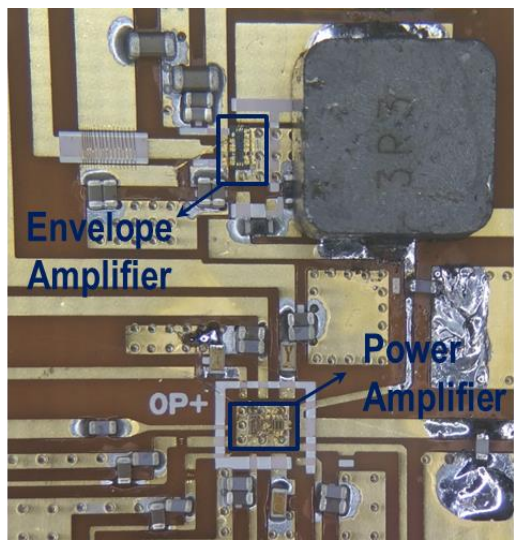
Broadband CW performance of the PA is measured from 0.65 to 1.05 GHz with and without interstage reconfiguration, as shown in Fig. 16. The applied gate and drain biases for both stages are 0.3 V and 3.9 V, respectively, resulting in a total quiescent current of 70 mA, and the CW test was performed at the maximum PAE point at each frequency. As shown in Fig. 2.17 (a), a maximum PAE of 69.2% is observed at 0.85 GHz, which corresponds to the “as-is” state in MFM. Without the interstage reconfiguration, PAEs degrade abruptly at band edges. With the



(a)



(b)



(c)

Fig. 2.13. Chip photographs of the fabricated (a) Envelope amplifier. (b) 2-stage PA and (c) Photograph of the test module.

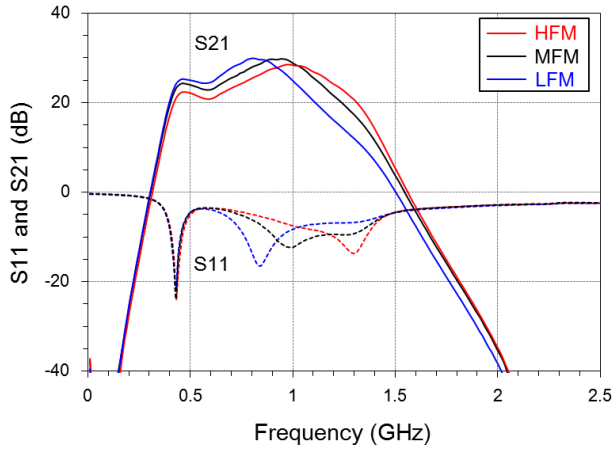


Fig. 2.14. Measured small-signal *S*-parameters at three different frequency modes

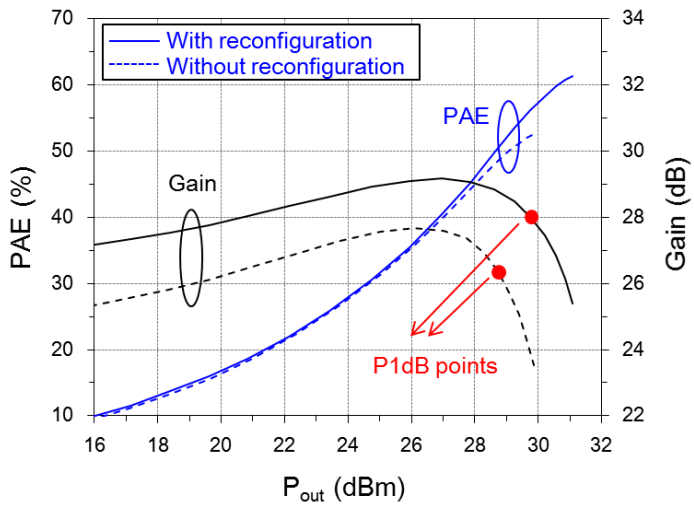


Fig. 2.15. Measured CW power sweep data of the PA at 0.65 GHz with and without interstage reconfiguration.

interstage reconfiguration, the peak PAEs maintain higher than 60% from 0.65 to 1.03 GHz, corresponding to a fractional bandwidth (FB) of 45%. The efficiency boosting is most pronounced in LFM (0.65 to 0.8 GHz), showing PAE improvement up to 9%. In HFM (0.9 to 1 GHz), PAE improvement up to 5% has been achieved.

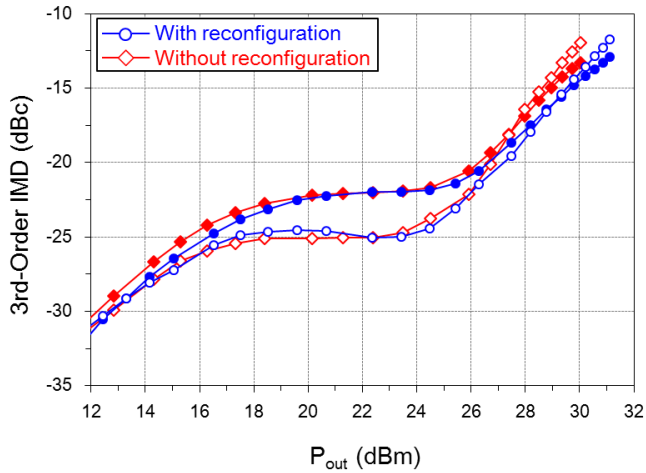
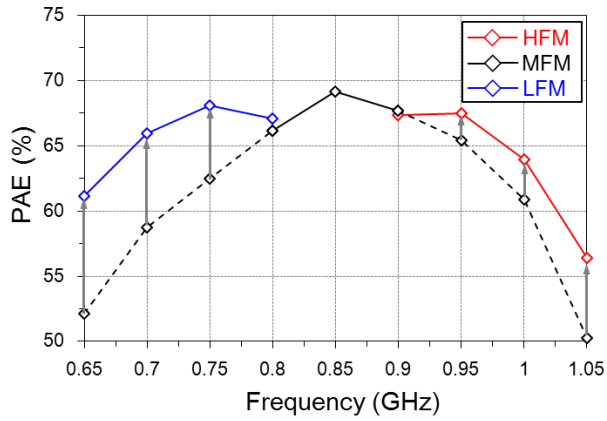


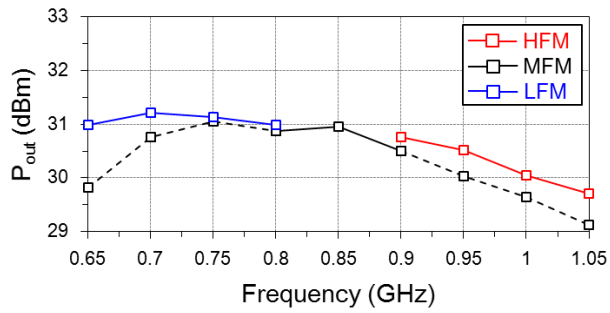
Fig. 2.16. Measured IMD characteristics of the PA at 0.7 GHz with and without interstage reconfiguration. (filled: lower IMD, hollow: upper IMD)

The measured output power over the entire bandwidth ranges from 29.7 to 31.1 dBm while the gain stays between 25.1 and 25.8 dB.

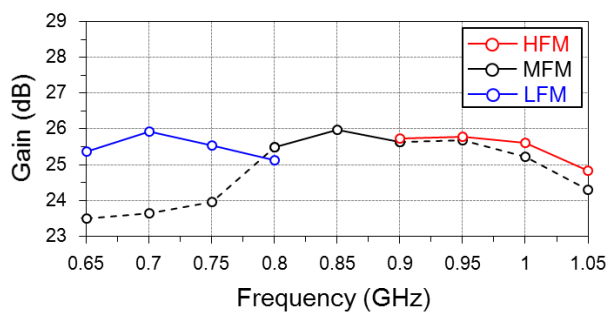
Class-J operation is experimentally verified across the entire frequency bandwidth by measuring the voltage waveform at the drain node of the power stage, as shown in Fig. 2.18. For this measurement, we used Agilent N2751A differential probe, which has only 700 fF internal capacitance. Since the output of the power cell is heavily loaded by C_{out} of the power cell itself, the additional 700 fF from the differential probe does not significantly affect the output matching. Half-sinusoidal voltage waveforms are well maintained at mid-frequencies, as predicted from the simulation results in Fig. 2.9 (a). Distortions at the low frequencies due to the finite third voltage component, predicted in Fig. 2.9 (b), are also clearly observed in this measurement. Likewise, the reduced voltage peaks are observed at high frequencies as predicted in Fig. 2.9 (c).



(a)



(b)



(c)

Fig. 2.17. Measured CW performance of the fabricated PA from 0.65 to 1.05 GHz. (a) PAE. (b) Output power. (c) Gain. The test was performed at the output power that shows the highest PAE at each frequency.

Table 2.1 compares CW performance of the published broadband PAs showing PAEs higher than 60%. The PA of this work shows 45% fractional bandwidth (for 60% PAE or higher).

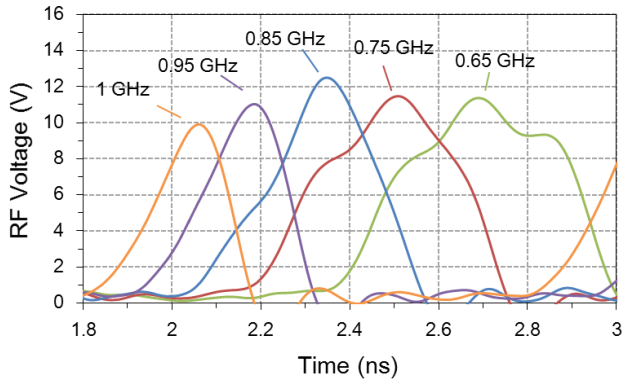


Fig. 2.18. Measured voltage waveforms at the drain node of the power cell

The performance of the entire ET PA system consisting of the fabricated two-stage ET PA and EA is measured using fully-loaded, 20-MHz BW, 6.7 dB PAPR, and QPSK-modulated LTE signal. Fig. 2.19 is a block diagram of the ET PA measurement setup [21]. The input envelope to the EA is generated using original I/Q data of the LTE signal and the exponential shaping function shown in Fig. 2.11. Then, the input envelope and original I/Q data are downloaded to two synchronized Agilent E4438C signal generators so that one works as an envelope source while the other as an RF source. The output of the ET PA is captured using Agilent N9020A signal analyzer, and the dynamic characteristics are measured using 89604L distortion suite. To correct for the phase distortions in the stacked CMOS RF PA, a simple memory-less digital pre-distortion is used to linearize the ET PA system. The pre-distorted I/Q are re-downloaded to the RF signal generator and then up-converted again to test ET PA with pre-distorted signal.

To show the effect of interstage reconfiguration, the ET PA system is measured at 0.7 GHz using 20-MHz BW LTE signals at 0.7 GHz with and without interstage reconfiguration. The power sweep data is shown in Fig. 2.20. QPSK-modulated LTE

TABLE 2.1

Performance Comparison Table of Broadband High Efficiency (> 60% CW PAE) PAs

Reference	[22]	[23]	[10]	[4]	**This work**
Frequency (GHz)	1.4~2.0	0.6~0.85	0.6~0.7	0.65~1.05	**0.65~1.03**
Fractional BW (MHz)	35	34	15	47	**45**
PA Technology	0.28-μm CMOS	65-nm EDCMOS[2]	0.35-μm SiGe BiCMOS	0.35-μm SiGe BiCMOS	**0.32-μm SOI CMOS**
No. of Stage	Two	Two	Single	Single	**Two**
P_{out} (dBm)	23	30	30.9~31.5	31.5~33.1	**29.7~31.1**
PAE (%)	60~67	60~65[3]	-	61.2~72.1	**60~69.2**
DE/CD (%)	62~72[4]	70~76	60~68.9[3]	65~74	**62.7~75.6[4]**
Gain (dB)	-	16	10	12.5	**25.1~25.8**
V_{DD} (V)	2.5	5	4.2	5	**3.9**

[1]: Drain efficiency/collector efficiency

[2]: Extended-drain, thick-oxide device

[3]: This result is graphically estimated

[4]: Drain efficiency of the power stage only

signal shows a PAPR of 6.7 dB with 0.01% probability. The gain and PAE of the standalone RF PA (non-ET, fixed bias mode) is also shown in the same chart as a reference. The overall system PAE at the maximum output power (26 dBm) of the ET PA with interstage reconfiguration is 42.2%, which corresponds to 2.2% efficiency improvement. The overall system PAE includes the power consumption from the envelope amplifier, RF PA, and loss from matching networks. Compared with the standalone RF PA case, the ET PA shows an efficiency boost up to 4.8%.

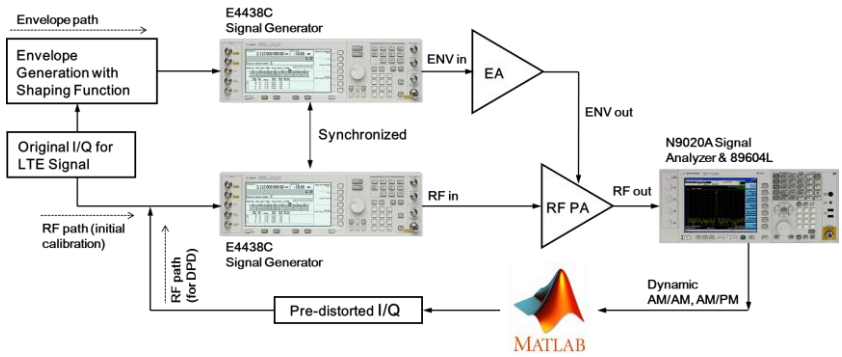


Fig. 2.19. Measurement setup used for testing ET PA system.

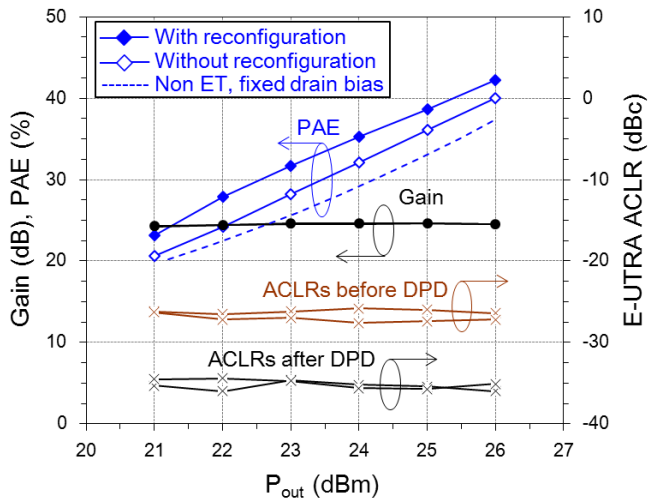


Fig. 2.20. Measured performance of the overall ET PA system as a function of the output power using 20-MHz LTE signal at 0.7 GHz with and without interstage reconfiguration.

The evolved universal terrestrial radio access (E-UTRA) adjacent channel leakage ratio (ACLR) after digital pre-distortion at the 26 dBm is measured to –35.1 dBc, which corresponds to 5.1 dB margin from the system specification.

To show the bandwidth performance, the ET PA system is measured using the same 20-MHz LTE signal while sweeping the carrier frequencies from 0.65 to 1.05 GHz as shown in Fig. 2.21. The maximum overall system PAE of 43.8 % is achieved

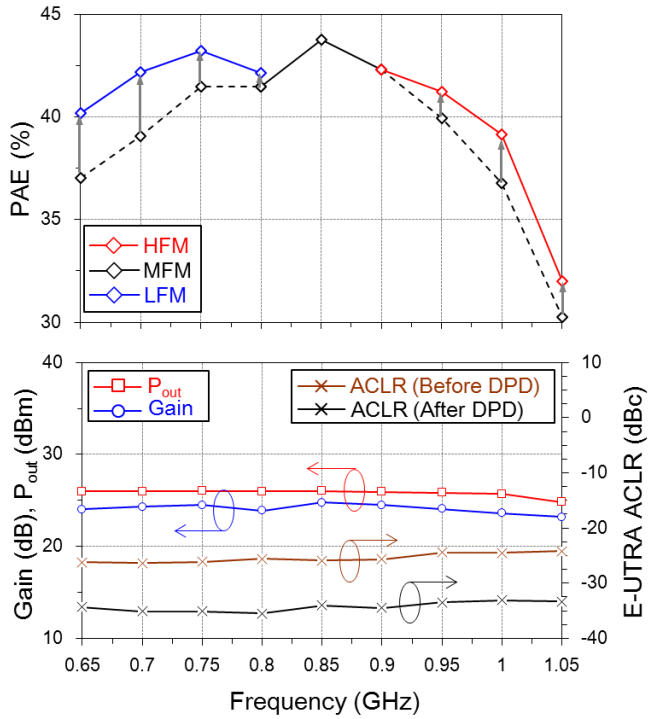


Fig. 2.21. Measured performance of the overall ET PA system using 20-MHz LTE signal from 0.65 to 1.05 GHz.

at 0.85 GHz with –34 dBc E-UTRA ACLR. With the interstage reconfiguration, the frequency bandwidth showing higher than 40% PAE is extended from 0.225 GHz (27% bandwidth) to 0.32 GHz (40% bandwidth). The gain of the ET PA across the entire bandwidth stays between 23.4 and 24.8 dB while the output power is between 25.4 and 26.1 dBm. The measured E-UTRA ACLRs across the entire test bandwidth is better than –33 dBc.

Fig. 2.22 is the measured output spectrum of the ET PA at 0.85 GHz with the output power of 26.1 dBm with and without pre-distortion. The digital pre-distortion used in this work improves ACLR by 8.4 dB.

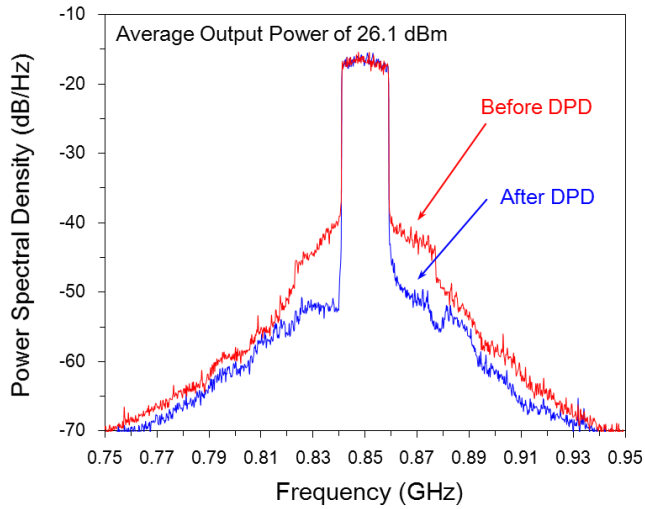


Fig. 2.22. Measured output power spectrum of the entire ET PA system using 20-MHz LTE signals before and after memory-less digital pre-distortion.

Table 2.2 is a performance comparison table for state -of-the-art broadband ET PA system for envelope tracking application. Even if CMOS FET used in this work, our work shows the best system PAE among the published works, including GaAs HBT and SiGe BiCMOS PAs.

TABLE 2.2

Performance Comparison Table of Broadband LTE Mobile Terminals

Reference	[1]	[2]	[3]	[4]	[5]	[6]	[7]	**This work**
Frequency (GHz)	1.85	1.7	1.85	0.7	0.85	1.7	2.535	**0.85**
RF FBW[1] (%)	16	16	16	-	42	16	-	**47**
Signal BW (BW)	10	10	10	20	10	10	20	**20**
PAPR (dB)	7.5	7.5	7.5	7.5	6.7	7.5	6.6	**6.7**
PA Technology	GaAs HBT	GaAs HBT	0.18-μm CMOS	0.35-μm SiGe BiCMOS	0.32-μm SOI CMOS	0.18-μm CMOS	GaAs HBT	**0.32-μm SOI CMOS**
P_{out} (dBm)	27.8	27	26	27.6	25	26.5	29	**26.1**
PAE[2] (%)	39	39.5	34.1	36.4	44	38.6	43	**43.8**
E-UTRA ACLR (dBc)	–34	–33.1	–34.2	N/A	–35.5	–35.3	N/A	**–34**
Output matching	Off-chip	Off-chip	Off-chip	Off-chip	Off-chip	On-chip	Off-chip	Off-chip
V_{DD} (V)	3.4	3.4	5	5	3.5	3.5	6	**3.9**

[1]: RF signal fractional bandwidth

[2]: Peak value within the frequency range

2.5 Conclusions

In this work, we have developed a broadband 2-stage SOI CMOS stacked-FET PA with reconfigurable interstage matching network for envelope tracking application. The power stage is based on Class-J mode of operation, where output matching is realized using two-section low-pass network. To guarantee Class-J mode of operation for the inner stacked FETs as well, Miller capacitors have been added across the drain-source terminals of the common-gate FETs in the stack.

With the broadband output matching, the practical bandwidth limitation to guarantee high overall gain and PAE over the entire bandwidth comes from high-Q interstage matching. To overcome the bandwidth limitation imposed by Bode-Fano criteria, a reconfigurable matching network is employed between the two stacked FETs. Two RF switches made of the same SOI CMOS process as the PAs have been employed to offer three different matching modes according to the operation frequency. This is achieved by changing the effective inductance value of the shunt inductor in the high-pass *C–L–C* interstage network. The fabricated PA shows CW efficiencies in excess of 60% from 0.65 to 1.03 GHz. When tested with an envelope amplifier, the overall ET system efficiency higher than 40% has been achieved using 20-MHz LTE signals from 0.65 to 0.97 GHz. The time-domain waveform measurement shows that the efficiency degradation at the extreme band edges arises from non-ideal output matching as the PA deviates from the ideal Class-J mode of operation, as expected from the simulation results. This work represents one of the widest RF bandwidth demonstration for LTE ET PAs for mobile phone applications. As the number of LTE bands increases, the need for PA sharing and wideband

operation will ever increase. The proposed idea of reconfigurable interstage matching can provide a practical solution to the bandwidth problems for LTE PAs.

2.6 References

[1] D. Kang, D. Kim, J. Choi, J. Kim, Y. Cho, and B. Kim, "A multimode/ multiband power amplifier with a boosted supply modulator," *IEEE Trans. Microw. Theory Techn.*, vol. 58, no. 10, pp. 2598–2608, Oct. 2010.

[2] Y. Cho, D. Kang, J. Kim, D. Kim, B. Park, and B. Kim, "A dual powermode multi-band power amplifier with envelope tracking for handset applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 4, pp. 1608–1619, Apr. 2013.

[3] D.Kang, B.Park, D.Kim, J.Kim, Y.Cho, and B.Kim, "Envelope-tracking CMOS power amplifier module for LTE applications," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 10, pp. 3763–3773, Oct. 2013.

[4] R. Wu, Y. Liu, J. Lopez, C. Schecht, Y. Li, and D. Y. C. Lie, "Highefficiency silicon-based envelope-tracking power amplifier design with envelope shaping for broadband wireless applications," *IEEE J. SolidState Circuits*, vol. 48, no. 9, pp. 2030–2040, Sep. 2013.

[5] S.Park, J.Woo, M.Jeon, U.Kim, and Y.Kwon, "Broadband CMOS stacked power amplifier using reconfigurable interstage network for envelope tracking application," in *Proc. IEEE RF Integr. Circuits Symp. Dig.*, Jun. 2014, pp. 145–148.

[6] S. Jin, K. Moon, B. Park, J. Kim, Y. Cho, H. Jin, D. Kim, M. Kwon, and B. Kim, "CMOS saturated power amplifier with dynamic auxiliary circuits for optimized envelope tracking," *IEEE Trans. on Microw. Theory Techn.*, vol. 62, no. 12, pp. 3425–3435, Dec. 2014.

[7] M. Hassan, L. E. Larson, V. W. Leung, D. F. Kimball, and P. M. Asbeck,"A wideband CMOS/GaAs HBT envelope tracking power amplifier for 4G LTE mobile terminal applications," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 5, pp. 1321–1330, May 2012.

[8] J. Woo, S. Park, U. Kim, and Y. Kwon, "Dynamic stack-controlled CMOS RF power amplifier for wideband envelope tracking," *IEEE Trans. on Microw. Theory Techn.*, vol. 62, no. 12, pp. 3452–3464, Dec. 2014.

[9] U. Kim, S. Kang, J. Woo, Y. Kwon, and J. Kim, “A multiband reconfigurable power amplifier for UMTS handset applications,” *IEEE Trans. on Microw. Theory Techn.*, vol. 60, no. 8, pp. 2532–2542, Aug. 2012.

[10] D. R. Wu, J. Lopez, Y. Li, and D. Y. C. Lie, “A highly efficient 1-watt broadband class-J SiGe power amplifier at 700MHz,” ” in *Proc. 12th Top. Silicon Monolithic Integr. Circuits in RF Syst. Meeting*, 2012, pp. 69–72.

[11] N. Tuffy, L. Guan, A. Zhu, and T. J. Brazil, “A simplified broadband design methodology for linearized high-efficiency continuous class-F power amplifiers,” *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 6, pp. 1952–1963, Jun. 2012.

[12] K. Mori, S. Shinjo, F. Kitabayashi, A. Ohta, Y. Ikeda, and O. Ishida, “An L-band high-efficiency and low-distortion power amplifier using HPF/LPF combined interstage matching circuit”, *IEEE Trans. Microw. Theory Tech.*, vol. 48, no. 12, pp. 2560–2566, Dec. 2002.

[13] J. R.Tomar and P. Bhartia., “A simple inter-stage matching technique for designing hybrid microwave power amplifiers, “*IEEE Microw. Mag.*, vol. 4, no. 3, pp. 67–84, Sep. 2003.

[14] D. M. Pozar, *Microwave Engineering*, 3rd ed. New York, NY, Wiley, 2005.

[15] P. Wright, J. Lees, J. Benedikt, P. J. Tasker, and S. C. Cripps, “A methodology for realizing high efficiency class-J in a linear and broadband PA,” *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 12, pp. 3196–3204, Dec. 2009.

[16] C. M. Andersson, D. Gustafsson, K. Yamanaka, E. Kuwata, H. Otsuka, M. Nakayama, Y. Hirano, I. Angelov, C. Fager, and N. Rorsman, “Theory and design of class-J power amplifiers with dynamic load modulation,” *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 12, pp. 3778–3786, Dec. 2012.

[17] G. L. Matthaei, “Tables of Chebyshev impedance-transforming networks of low-pass filter form,” *Proc. IEEE*, vol. 52, no. 8, pp. 939–963, Aug. 1964.

[18] M. Jeon, J. Woo, Y. Kwon, “A high-efficiency CMOS stacked-FET power amplifier for W-CDMA applications using SOI technology,” *Electron. Lett.*, vol. 49, no. 8, pp. 564–566, Apr. 2013.

[19] M. Hassan, P. M. Asbeck, L. E. Larson, “A CMOS dual-switching power-supply modulator with 8% efficiency improvement for 20 MHz LTE envelope

tracking RF power amplifiers," in *IEEE Int. Solid-State Circuits Conf. Tech. Dig.*, Feb. 2013, pp.366–367.

[20] P. Arnò, M. Thomas, V. Molata, T. Jeřábek, "Envelope modulator for multimode transmitters with AC-coupled multilevel regulators," in *IEEE Int. Solid-State Circuits Conf. Tech*. Dig., Feb. 2014, pp.296–297.

[21] J. Woo, M. Jeon, and Y. Kwon, "Dynamic FET stack control for enhanced efficiency in envelope tracking power amplifiers," in *IEEE MTT-S Int. Microw. Symp. Dig*., Jun 2014, pp.1-4.

[22] S. A. Mazzanti, L. Larcher, R. Brama, and F. Svelto, "Analysis of reliability and power efficiency in cascode class-E PAs," *IEEE J. Solid-State Circuits,* vol. 41, no. 5, pp. 1222–1229, May 2006.

[23] M. R. Zhang, M. Acar, M. P. Heijen, M. Apostolidou, L. C. N. Vreede, and D. M. W. Leenaerts, "A 550–1050MHz +30dBm class-E power amplifier in 65nm CMOS," in Proc. IEEE RF Integr. Circuits Symp. Dig., Jun 2014, pp. 1–4.

Chapter 3

A GaN Envelope Amplifier Using Class-E^2 for Wideband Envelope Tracking Applications

3.1 Introduction

In order to increase a data rate of the future wireless communication beyond 4G, it is necessary to apply complex modulation method of signal. Such signals have high peak-to-average power ratio (PAPR) and wide bandwidth (BW), which means that the radio frequency power amplifier (RF PA) should be operated in a low-efficiency back-off power range to satisfy the linearity specification. Envelope tracking (ET) is one of the most popular technique to enhance the overall efficiency at back-off power of a transmitter, when handling various signals with the high PAPR and wide BW [1]-[7]. A key component in the wideband ET system is envelope amplifier (EA) to adjust the drain bias of RF PA dynamically. The most widely used EA architecture is a hybrid switching amplifier (HSA) which consists of a linear stage for high-fidelity and a switching stage for high-efficiency [1], [4], [5], [7], [10], [11] (Fig. 3.1. (a)). However, when the HAS handles wideband LTE envelope signals, its efficiency is degraded due to the increased switching loss in the switching stage.

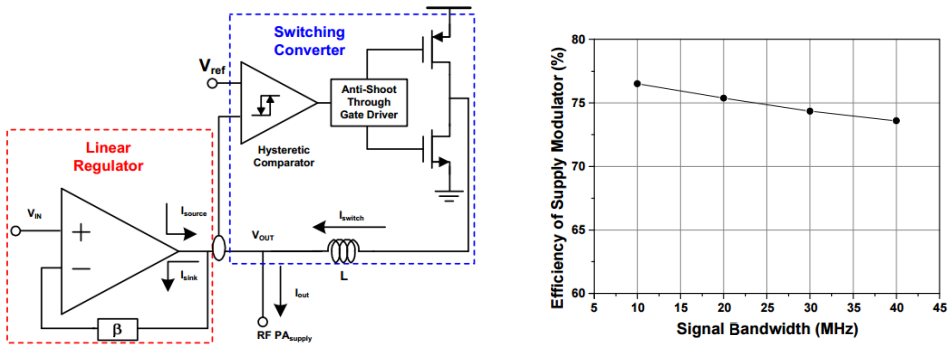


Fig. 3.1. (a) The simplified circuit schematic of the conventional hybrid switching amplifier (HSA). (b) The measured efficiency of HSA according to LTE bandwidth [1].

According to the [1], the efficiency of the EA decrease by 2.8% as LTE signal bandwidth is increased from 10- to 40-MHz as plotted in Fig. 3.1 (b). Moreover, large field effect transistors (FETs) in the linear stage is required to satisfy the desired slew rate and speed for the high fidelity, leading to speed limitation and efficiency degradation, which is not desirable in wideband operation.

Another topology of EA is a switched-mode converter (SMC), which uses only the switching stage operating at several hundreds of megahertz to track the input envelope signal with high linearity as depicted in Fig. 3.2 (a). In particular, wide bandgap devices and technologies such as gallium-nitride (GaN) enable high efficiency SMC operate at high frequencies [2], [3]. However, SMC design using GaN high electron mobility transistors (HEMTs) has some problems. First of all, to follow the envelope without degradation of the system linearity, the operating frequency of SMC should be 10 times the envelope frequency. This causes a large switching loss and leads to a large efficiency reduction. Second, SMC require pulse width modulation (PWM) signal for the amplitude modulation given the input

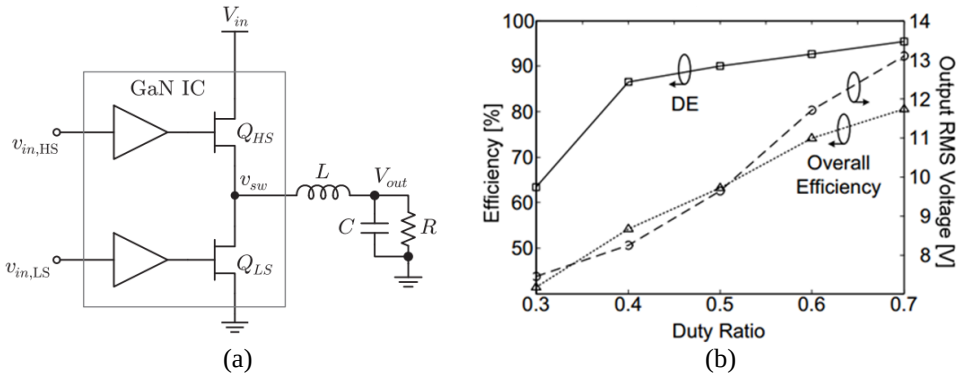


Fig. 3.2. (a) The simplified circuit schematic of the conventional switched-mode converter (SMC). (b) The measured efficiency of SMC using GaN device according to the duty ratio [2].

envelope. It is very difficult to generate at high frequencies, and efficiency dramatically decrease if a proper pulse is not generated. Finally, a series switch should be employed. In order to drive the series switch, the gate of the transistor should be fed a sufficiently large voltage swing, resulting in suffer from low efficiency especially at the low duty cycle due to the dc power consumed by the gate driver. For example, authors in [2] demonstrated 200 MHz switching SMC to handle 20-MHz LTE application, and shows very high drain efficiency (~90%). However, the overall efficiency of the EA suffers from the current consumption in the gate driver, which results in 26 % efficiency degradation as shown in Fig. 3.2 (b).

To overcome these problems, we propose a high-efficiency GaN EA using a class-E^2 resonant converter with not PWM but pulse frequency modulation (PFM) signal to handle 80-MHz LTE applications in this work. A simplified block diagram of the proposed ET PA is shown in the Fig. 3.3. The system consists of the GaN class-E^2 converter whose output is adaptively adjusted by a CMOS controller, and a 3.5 GHz high-efficiency harmonic tuned GaN RF PA. The CMOS controller generate

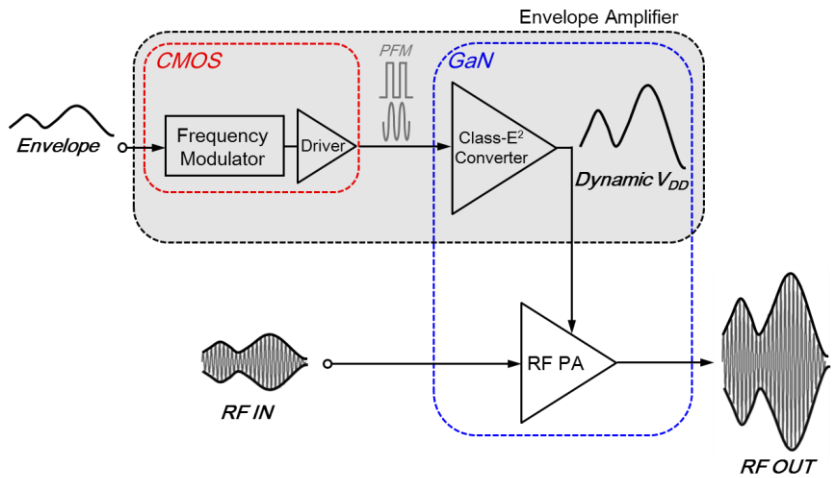


Fig. 3.3. . Simplified block diagram of the proposed envelope amplifier.

frequency modulated signal depending on the magnitude of the envelope signal, which operates the converter. The output of the converter can achieve a large dynamic V_{DD} enough to operate GaN RF PA. According to the measurement results, the proposed EA is not exposed to the efficiency and linearity degradation in wideband operation, thus maintain 74% efficiency as the signal bandwidth is increased from 20- to 160-MHz. The overall ET PA system is tested under 80-MHz LTE signal and shows 46.5% overall drain efficiency (DE) at 35.3 dBm average output power.

This paper is organized as follows. Section 3.2 introduces operation principle of the proposed EA. In Section 3.3, the detailed circuit design of the proposed EA and the harmonic tuned GaN RF PA are presented together. Section 3.4 presents the measurement results of the implemented ET PA system with various LTE bandwidth (20- to 160-MHz). Finally, this paper ends with conclusions in Section 3.5.

3.2 Operation Principle of the Proposed Envelope Amplifier

3.2.1 Operation Principle of Class-E Inverter and Rectifier

The detailed circuit schematic of class-E^2 resonant converter is shown in Fig. 3.4. It consists of two main parts; class-E inverter and class-E rectifier. This topology has an advantage that the shunt switch is used with GaN HEMT, which can overcome the problem caused by using the series switch. When the high frequency pulse train is applied to the gate node of the class-E inverter, it produces a sinusoidal current waveform by a series-resonator circuit (L_S-C_S) from dc supply (V_{DD}) and transfers to the class-E rectifier, which provides dc current again by a low pass filter (LPF) from the inverter. Since both the class-E inverter and rectifier operate in zero voltage switching (ZVS) and zero derivative voltage switching (ZDVS) conditions, it can maintain high efficiency regardless of the switching frequency [12]-[14].

The class-E inverter is composed of one active device as a switch (*SW*), an inductor (L_{RFC}) for dc feed, shunt capacitor (C_P), and a series LC resonator (L_S-C_S) as shown in Fig. 3.5 (a) [15], [16].

To analyse into operation of the class-E inverter, there are several assumptions to make it simple. First, Q factor of the series LC resonator is large enough so that the harmonics except the fundamental signal cannot pass through. Second, Inductance of the dc feed inductor (or RF choke inductor) is large enough so that the ac ripple of the input current can be neglected. Because of the series LC resonator, a fundamental sinusoidal current (I_{RF}) flows through a load (R_L) of the inverter. Fig. 3.5 (b) shows sum of sinusoidal current wave and dc current (I_{DC}) supplied.

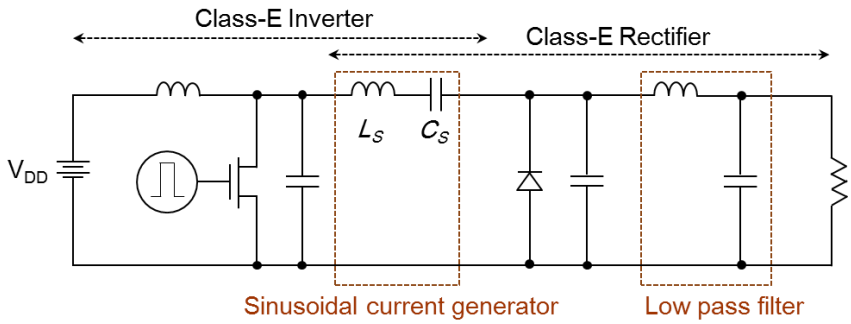


Fig. 3.4. Overall schematic of the class-E^2 resonant converter.

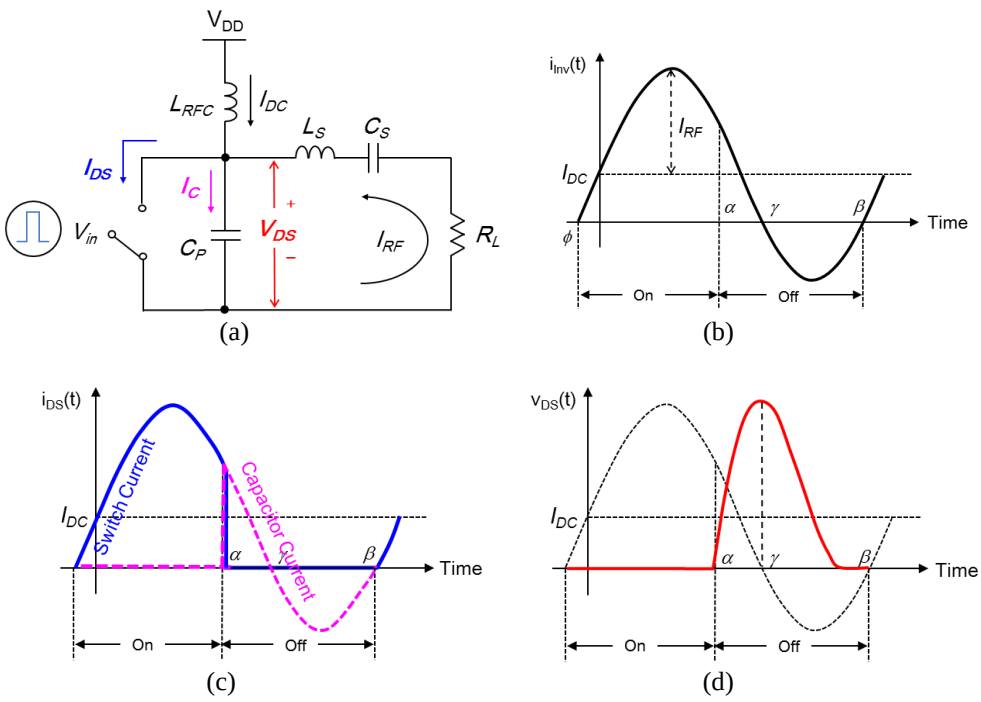


Fig. 3.5. (a) Basic schematic of class-E inverter. (b) Total summation of RF and dc current waveforms. (c) Current waveforms flowing in the switch (or transistor) and the capacitor. (d) Voltage waveform across the switch

The corresponding current $i_{Inv}(t)$ flowing through the parallel combination of the switch and the capacitor is always sinusoidal waveform with dc current, given by:

$$i_{Inv} = I_{DC} + I_{RF} \cdot \sin(\theta) \tag{1}$$

This current (i_{Inv}) is divided into the switch current (i_{DS}) and the capacitor current (i_C) by the duty ratio of the pulse signal applied to the switch (*SW*). The current in the switch is:

$$i_{DS}(\theta) = \begin{cases} I_{DC} + I_{RF} \cdot \sin(\theta) & 0 \le \theta \le \alpha \\ 0 & \alpha \le \theta \le \beta \end{cases} \tag{2}$$

The current given by Eq. (2) flows in the switch (or transistor) when the switch is in its ON-state; otherwise it flows in the capacitor (C_P) when the switch is OFF-state. The resulting current flowing through the different circuit elements is shown as Fig. 3.5 (c). The drain-source voltage $v_{DS}(t)$ across the switch device becomes and remains zero along the time interval ON-state, in the time interval OFF-state can be inferred by integration of the current flowing through the capacitor (C_P), thus resulting in the voltage waveform shown in Fig. 3.5 (d). The switch and capacitor voltage waveform $v_{DS}(t)$, is given by:

$$v_{DS}(\theta) = \frac{1}{\omega \cdot C_P} \cdot \int_{\alpha}^{\theta} \left[I_{DC} + I_{RF} \cdot \sin(\theta) \right] \cdot d\theta \tag{3}$$

Thus obtaining the following expression for the voltage $v_{DS}(t)$, valid in ON-state.

As a consequence, the voltage waveform across the switch (*SW*) and capacitor (C_P) is described by:

$$v_{DS}(\theta)=\begin{cases}0 & 0\le\theta\le\alpha\\ \dfrac{1}{\omega\cdot C_P}\cdot\left\{I_{DC}\cdot(\theta-\alpha)-I_{RF}\cdot\left[\cos(\theta)-\cos(\alpha)\right]\right\} & \alpha\le\theta\le\beta\end{cases} \quad (4)$$

Referring to Fig. 3.5 (d) and Eq. (4), when θ is α, the voltage $v_{DS}(t)$ is zero while its derivate is positive. When θ is β, $v_{DS}(t)$ shows zero derivative while its value is zero in order to satisfy ZVS and ZDVS condition. When θ is γ, $v_{DS}(t)$the voltage has the maximum value and its derivative becomes zero.

To investigate the relationship between the output voltage of the inverter and the frequency, the voltage depicted in Fig. 3.5 (d) can be expressed as Fourier coefficients as follows.

$$V_{DS,f_0}(\theta)=V_{DS,f_0,I}+j\cdot V_{DS,f_0,Q} \quad (5)$$

where

$$V_{DS,f_0,I}=\frac{1}{\pi}\cdot\int_{\alpha}^{\beta}V_{DS}(\theta)\cdot\cos(\theta)\,d\theta \quad (6)$$

$$V_{DS,f_0,Q}=\frac{1}{\pi}\cdot\int_{\alpha}^{\beta}V_{DS}(\theta)\cdot\sin(\theta)\,d\theta \quad (7)$$

The Fourier coefficient for the fundamental components can be expressed as:

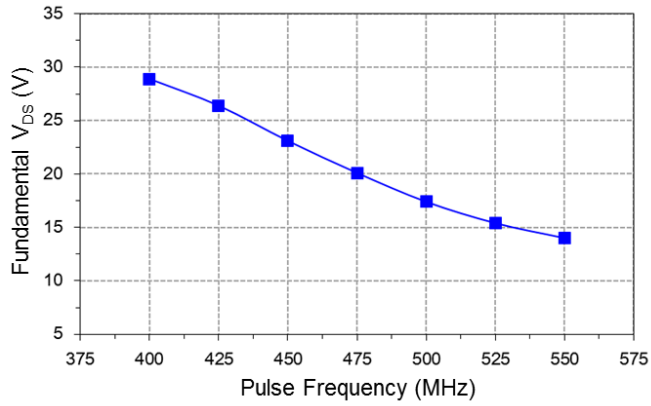


Fig. 3.6. Simulated fundamental output voltage of the inverter according to the pulse frequency.

$$V_{DS,f_0,I} = \frac{1}{\pi}\cdot\frac{I_{RF}}{\omega\cdot C_P} \times\left\{\begin{array}{l}\cos(\phi)\cdot\left[2\cos(\beta)+2\beta\sin(\beta)-2\alpha\sin(\beta)-2\cos(\alpha)\right]\\ +\left[\alpha-\beta+2\cos(\alpha)\sin(\beta)-\cos(\alpha)\sin(\alpha)-\cos(\beta)\sin(\beta)\right]\end{array}\right\} \quad (8)$$

$$V_{DS,f_0,Q} = \frac{1}{\pi}\cdot\frac{I_{RF}}{\omega\cdot C_P}\cdot\left\{\begin{array}{l}\cos(\phi)\cdot\left[\sin(\beta)-\sin(\alpha)+\alpha\cos(\beta)-\beta\cos(\beta)\right]\\ +\left[\frac{1}{2}\cdot\left[\cos(\alpha)^2\right]-\cos(\alpha)\cos(\beta)\right]\end{array}\right\} \quad (9)$$

Eq. (8) informs that the real component for the fundamental voltage is proportional to the magnitude of the current delivered to the output load, while inversely proportional to the frequency. Because of the high-Q value of the series-resonator, the transmitted power becomes smaller at frequencies higher than the resonance frequency. Therefore, as the current flowing in the load is inversely proportional to the frequency, the voltage can be expressed as a function of the frequency and an inverse relationship can be obtained.

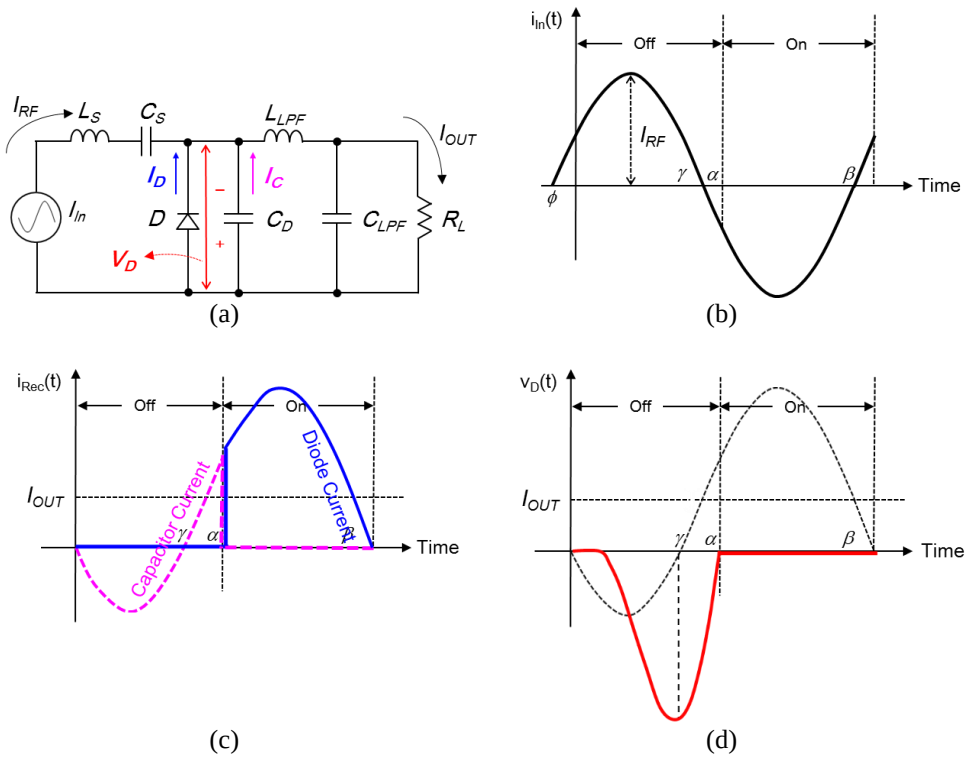


Fig. 3.7. (a) Basic schematic of class-E rectifier. (b) Current waveform flowing. (c) Current waveforms flowing in the diode and the capacitor. (d) Voltage waveform across the diode

To check the relationship between the output voltage and the input frequency, we have performed a transient simulation on class-E inverter. In this simulation, the all components that make up the converter including capacitor, inductor, have been used as ideal lossless model except the inverter switch (*SW*) (See Fig. 3.5). The switch model used in the simulation is commercially available Wolfspeed GaN HEMT CGH60015D. On resistance of this model is 1 Ω and the input, output capacitance is 4.1 pF, 0.9 pF, respectively. Fig. 3.6 shows that the simulated fundamental output voltage of the inverter according to the pulse frequency from 400 MHz to 550 MHz. The simulation result validates the theoretical predictions based on Eq. (8), which the output voltage has inversely linear response according to the frequency.

The class-E rectifier consists of a shunt diode (D), shunt capacitor (C_D), and LPF as shown in Fig. 3.6 (a) [17], [18]. To analyse into operation of the class-E inverter, there are several assumptions to make it simple. First, the rectifier diode is ideal, which has the zero threshold voltage, the zero on resistance, the infinity off resistance, and zero the reverse-recovery time. Second, the rectifier is driven by an ideal sinusoidal current source. Third, the filter inductance (L_{LPF}) is large enough so that the ac ripple of the output current can be neglected.

The corresponding current $i_{Rec}(t)$ flowing through the parallel combination of the diode and the capacitor is always sinusoidal waveform, given by:

$$i_{Rec} = I_{OUT} - I_{RF} \cdot \sin(\theta + \phi) \tag{10}$$

Where ϕ can be expressed as a function of the duty ratio [12].

Since $i_{Rec}(t)$ become zero, when $\theta = 0$,

$$I_{OUT} = I_{RF} \cdot \sin(\phi) \tag{11}$$

From which it follows that

$$\begin{aligned} i_{Rec} &= I_{RF} \cdot \left[\sin(\phi) - \sin(\theta + \phi)\right] \\ &= I_{OUT} \cdot \left[1 - \frac{\sin(\theta + \phi)}{\sin(\phi)}\right] \end{aligned} \tag{12}$$

This current (i_{Rec}) is divided into the diode current (I_D) and the capacitor current (I_D). The current in the diode is:

$$i_D(\theta) = \begin{cases} 0 & 0 \le \theta \le \alpha \\ I_{RF} \cdot \left[\sin(\phi) - \sin(\theta + \phi) \right] & \alpha \le \theta \le \beta \end{cases} \quad (13)$$

The resulting current flowing through the different circuit elements is shown as Fig. 3.7 (c). The voltage $v_D(t)$ across the diode and capacitor becomes and remains zero along the time interval ON-state, in the time interval OFF-state can be inferred by integration of the current flowing through the capacitor (C_D), thus resulting in the voltage waveform shown in Fig. 3.7 (d). The voltage waveform $v_D(t)$, is given by:

$$v_D(\theta) = \frac{1}{\omega \cdot C_D} \cdot \int_0^{\theta} \left\{ I_{RF} \cdot \left[\sin(\phi) - \sin(\theta + \phi) \right] \right\} \cdot d\theta \quad (14)$$

Thus obtaining the following expression for the voltage $v_D(t)$, valid in ON-state. As a consequence, the voltage waveform across the switch (D) and capacitor (C_D) is described by:

$$v_D(\theta) = \begin{cases} \frac{I_{RF}}{\omega \cdot C_D} \cdot \left[\theta \cdot \sin(\phi) + \cos(\theta + \phi) - \cos(\phi) \right] & 0 \le \theta \le \alpha \\ 0 & \alpha \le \theta \le 2\pi \end{cases} \quad (15)$$

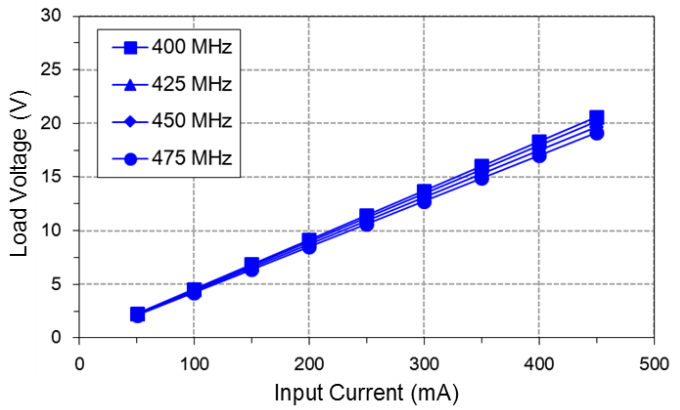


Fig. 3.8. Simulated fundamental output voltage of the rectifier according to the amplitude of RF current and the pulse frequency.

Referring to Fig. 3.7 (d) and Eq. (15), when θ is 0, the voltage $v_D(t)$ shows zero derivative while its value is zero in order to satisfy ZVS and ZDVS condition. When θ is α, $v_D(t)$ is zero while its derivate is positive. When θ is γ, $v_D(t)$the voltage has the maximum value and its derivative becomes zero.

To investigate the relationship between the output dc voltage of the rectifier and the input RF current, the voltage depicted in Fig. 3.7 (d) can be expressed as the average value as follows.

$$\begin{aligned} V_{OUT,DC} = \overline{v_D} &= \frac{1}{2\pi}\cdot\frac{1}{\omega\cdot C_D}\cdot\int_0^{\alpha}\left\{I_{RF}\cdot\left[\sin(\phi)-\sin(\theta+\phi)\right]\right\}\cdot d\theta \\ &= \frac{1}{2\pi}\cdot\frac{I_{RF}}{\omega\cdot C_D}\cdot\left[\alpha\sin(\phi)-\alpha\cos(\phi)+\sin(\alpha+\phi)-\sin(\phi)\right] \end{aligned} \tag{16}$$

Eq. (16) informs that the average output voltage is proportional to the amplitude of the current transferred from the input current source, while the frequency is relatively less effective to the voltage. Therefore, as the output load voltage is mainly

proportional to the RF current, the voltage can be expressed as a function of the RF current.

To check the relationship between the output voltage and the amplitude of the input current, we have performed a transient simulation on class-E rectifier. The simulation conditions are the same as those of the inverter. Fig. 3.8 shows that the simulated dc output voltage of the rectifier according to the amplitude of the input RF current from 50 mA to 450 mA and the pulse frequency from 400 MHz to 475 MHz. The simulation result validates the theoretical predictions based on Eq. (16), which the output voltage has linear response according to the input current.

3.2.2 Operation Comparison of Class-E^2 between PWM and PFM

As explained in the previous chapters, class-E^2 converter can operate with high efficiency due to ZVS and ZDVS. However, at the duty ratio of the converter become smaller, the efficiency decreases drastically. When the duty ratio become lower, the conduction angle becomes smaller from the optimal angle and no longer satisfies ZVS operation [16]. It is the main problem that the converter using PWM signal can maintain high efficiency at only specific duty ratio. This means that efficiency of the converter only peaks at certain output level, and degraded at other regions, which is not desirable for ET applications.

To investigate how the decreased duty ratio affects the overall efficiency of the converter, we have performed a transient simulation on class-E^2 converter. In this simulation, the all components that make up the converter including capacitor, inductor, and diode have been used as ideal lossless model except the inverter switch (*SW*) (See Fig. 3.5). The switch model used in the simulation is commercially

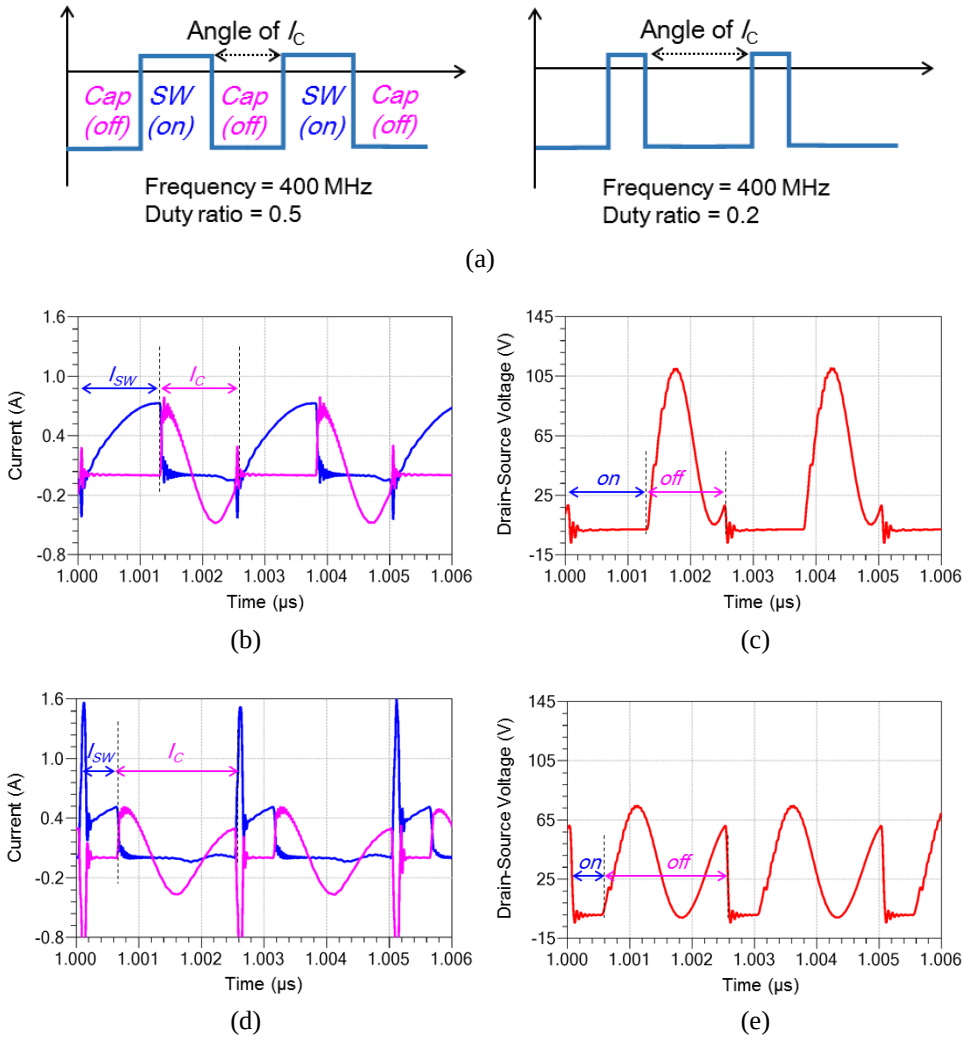


Fig. 3.9. Simulated drain current and voltage waveforms with the same frequency of 400 MHz. (a) Simplified PWM signal as its duty ratio decreases. (b) Current at the duty ratio of 0.5. (c) Voltage at the duty ratio of 0.5. (d) Current at the duty ratio of 0.2. (e) Voltage at the duty ratio of 0.2.

available Wolfspeed GaN HEMT CGH60015D that is same as the transistor used in the simulation in the chapter 3.2.1.

Fig. 3.9 (a) shows PWM signal, which is simply represented according to the duty ratio of 0.5 and 0.2. Fig. 3.9 (b), (c) show the simulated current and voltage waveforms at the drain node of the HEMT switch when an ideal pulse signal with a

frequency of 400 MHz and a duty ratio of 0.5 is applied to the gate node of the class-E inverter. In the current waveform shown in Fig. 3.9 (b), the current flows properly to the switch (*SW*) and capacitor (C_P) respectively. In particular, the capacitor is fully charged and discharged without the wasted of energy stored in the capacitor. As a result, the converter can operate with ZVS condition as shown in Fig. 3.9 (c), and the simulated overall efficiency of the converter is as high as 88%.

On the other hand, when the duty ratio of the pulse signal is lower to get the smaller converter output voltage, the situation become different. Fig. 3.9 (d), (e) show the simulated current and voltage waveforms at the drain node of the HEMT switch when an ideal pulse signal with the same frequency (400 MHz) and a duty ratio of 0.2 is applied. If the duty ratio is less than 0.5, the proportion of the current flowing to the capacitor (C_P) increase. In this case, the time for the switch (*SW*) being in ON-state is decreasing while the OFF-state is increasing as the duty ratio decreases. This results in increase of time for current to flow into the capacitor (C_P) too long that before the capacitor is fully discharged, the inverter switch will turn on. Fig. 3.9 (d) shows the remaining charges in capacitor than flows through the ON-state switch resulting in waste of energy. As a result, the converter can no longer operate with ZVS condition as shown in Fig. 3.9 (e), and the simulated overall efficiency of the converter is reduced to 62.5%.

A new modulation scheme is required to overcome the problem when using PWM control. Instead of PWM control, pulse frequency modulation (PFM) is adopted in order to avoid the waste of energy stored in the capacitor (C_P). As mentioned in section 3.2.1, the output voltage of class-E^2 converter can be regulate by varying frequency. Because of high-Q series resonator and Eq. (8) which is the characteristic

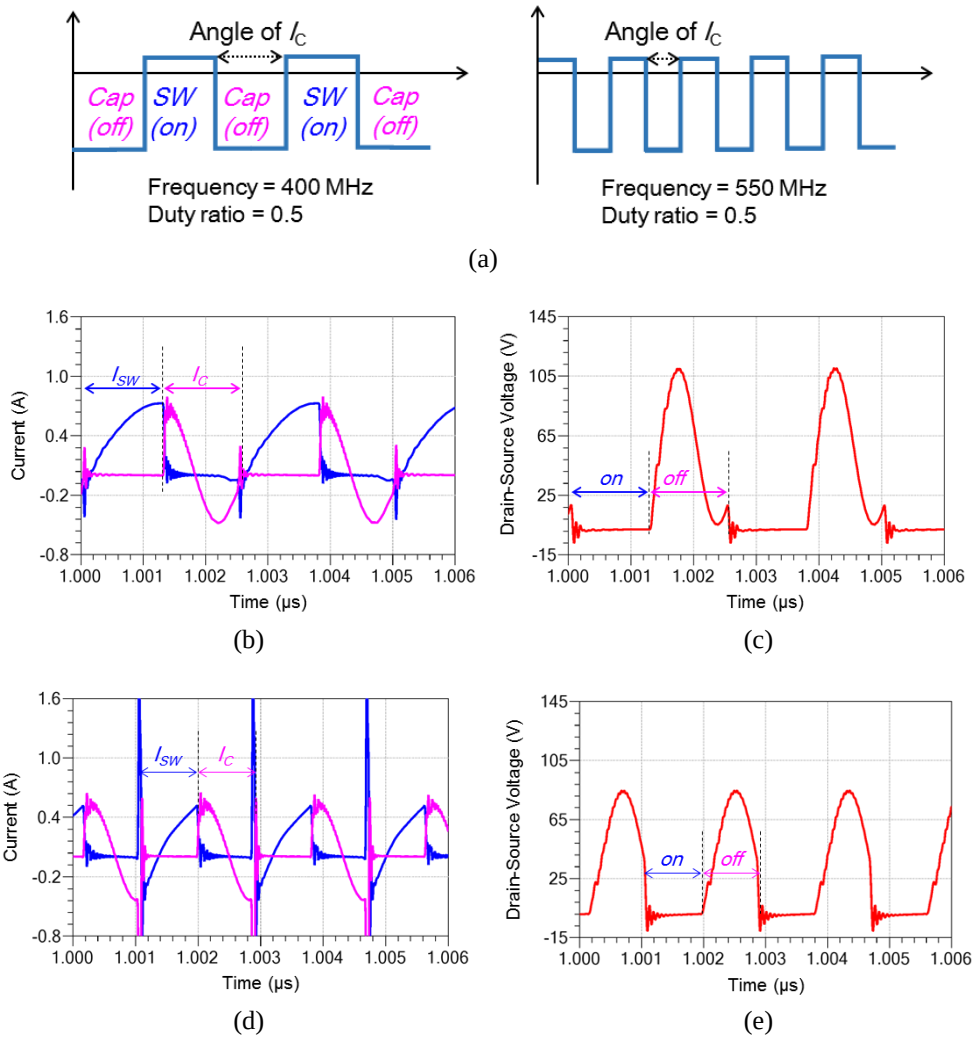
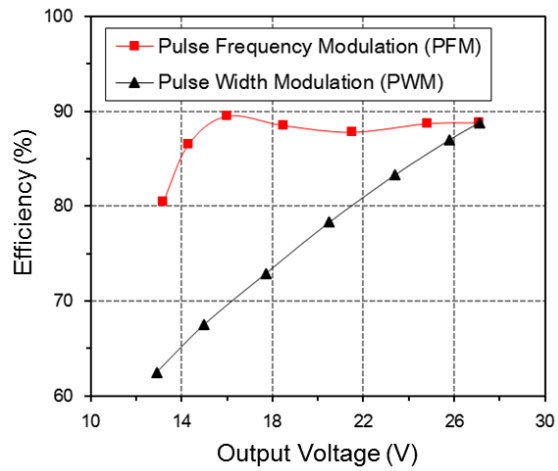


Fig. 3.10. Simulated drain current and voltage waveforms with the same duty ratio of 0.5. (a) Simplified PFM signal as it gets higher frequency. (b) Current at the frequency of 400 MHz. (c) Voltage at the frequency of 400 MHz. (d) Current at the frequency of 550 MHz. (e) Voltage at the frequency of 550 MHz.

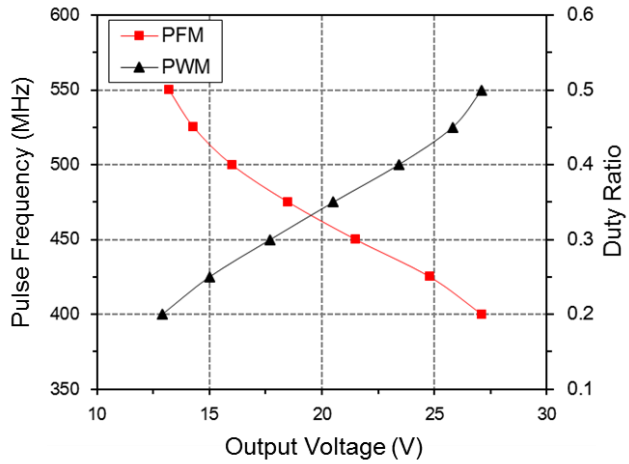
of the class-E inverter, the class-E inverter can generate an inversely proportional current and voltage according to input pulse frequency. At the same time, the rectifier can achieve dc output voltage according to amplitude of input current from the inverter. Therefore, if input frequency linearly changed by PFM control, a linear output response of the converter can be obtained. Fig. 3.10 (a) shows PFM signal,

which is simply represented according to the frequency of 400 MHz and 550 MHz. Fig. 3.10 (b), (c) show the simulated current and voltage waveforms at the drain node of the HEMT switch when an ideal pulse signal with a frequency of 400 MHz and a duty ratio of 0.5 is applied to the gate node of the class-E inverter. As described above, the converter can achieve high efficiency at the high output voltage. To get the smaller output voltage, the frequency of the pulse signal is increased to 550 MHz from 400 MHz with fixed duty ratio of 0.5. Fig. 3.10 (d), (e) show the simulated current and voltage waveforms at the drain node of the HEMT switch when an ideal pulse signal with the frequency of 550 MHz and the duty ratio of 0.5 is applied. If the frequency is larger than 400 MHz, the proportion of the current flowing to the capacitor (C_P) maintain due to the fixed duty ratio. In this case, the time for the switch (*SW*) being in ON-state is same as the OFF-state. This results in keep of time ratio for current to flow into the capacitor (C_P) can make the capacitor is fully discharged shown in Fig. 3.10 (d). As a result, the converter can operate with ZVS condition as shown in Fig. 3.10 (e), and the simulated overall efficiency of the converter is 80.5%. Unlike PWM control which changes the duty ratio using in typical dc-dc converter, PFM control can avoid the waste of energy stored in the drain capacitor, overcoming low efficiency at the low output voltage.

Fig. 3.11 (a) shows the graphical representation of efficiency depending on output voltage. The line with rectangular symbols indicates PFM controlled converter performance while the line with triangular symbols shows the previously built PWM controlled converter performance. From the simulation, it is noticeable that at about 12 V of output voltage, about 18% of efficiency increased. Fig. 3.11 (b) shows the linear response of the output voltage according to the frequency or duty ratio. It



(a)



(b)

Fig. 3.11. Simulation comparison between pulse width modulation (PWM) and pulse frequency modulation (PFM). (a) The overall efficiency versus the output voltage of the converter. (b) The output voltage versus pulse frequency (and duty ratio).

shows that by changing the frequency linearly, the output voltage can be changed in linear, as getting the linear output voltage by changing duty ratio.

We can summarize the contents described so far and arrange them as shown in following figures. Fig. 3.12 shows the operation principle of the proposed envelope amplifier using graphs with the simplified transfer functions of the each component.

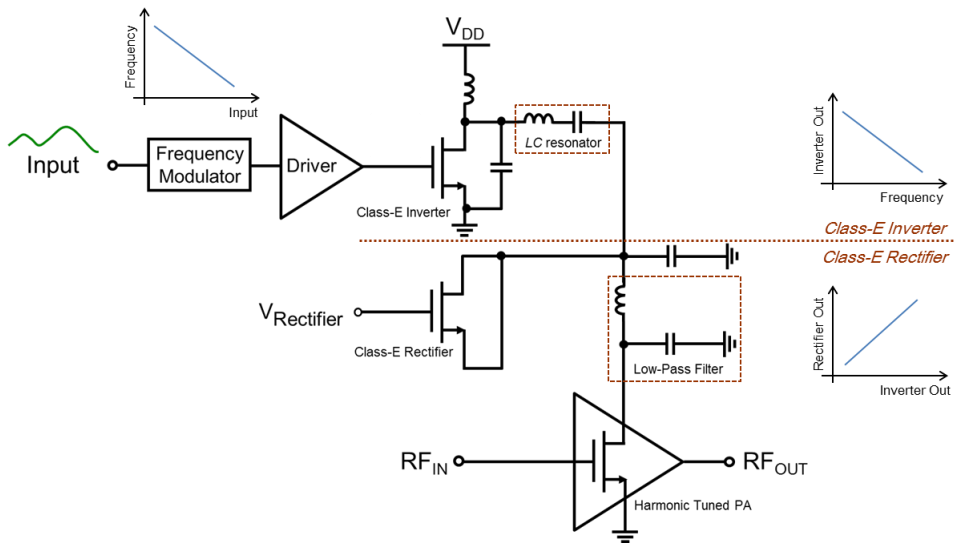


Fig. 3.12. The operation principle of the proposed envelope amplifier using graphs with the simplified transfer functions of the each component.

The first transfer function is represented at a graph to depict the frequency modulator. The role of the frequency modulator is to produce a pulse signal with the frequency inversely proportional to the magnitude of the given input envelope. The frequency modulated signal with high frequency activates the class-E inverter through a driver. Second, the other transfer function is represented by operation of the class-E inverter. The role of the inverter is to amplify the frequency modulated signal received from the driver. Through the inverter, the output can get inversely proportional response to the frequency. The final transfer function is represented by operation of the class-E rectifier. The role of the rectifier is to rectify the amplified signal from the inverter, which can deliver the linear envelope current (or voltage) to the RF PA. Fig. 3.13 shows the operation principle of the proposed envelope amplifier using graphs with the simplified magnitude at the frequency-domain of the each component. At node “A”, the amplified RF signal with rectangular pulse shape coexist with the relatively

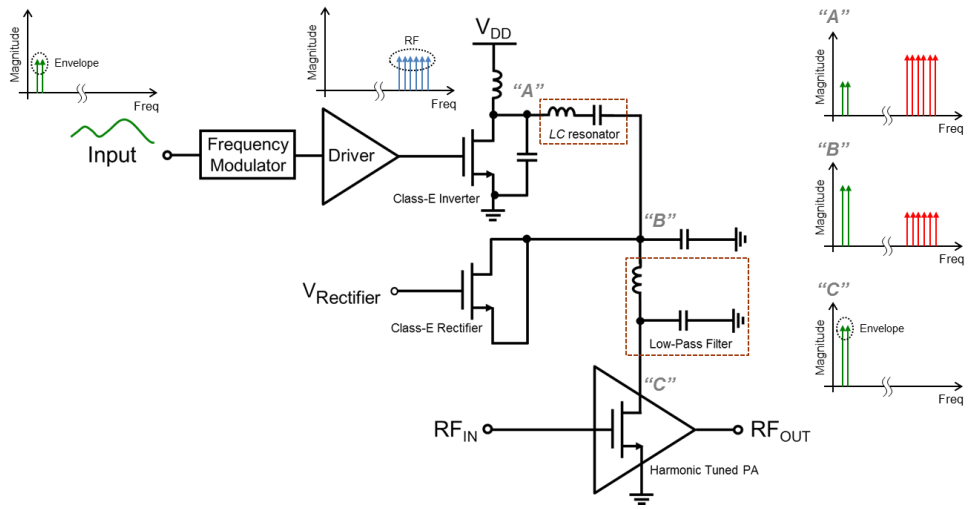


Fig. 3.13. The operation principle of the proposed envelope amplifier using graphs with the simplified magnitude at the time-domain of the each component.

small envelope signal. At node "B", the amplified RF signal is rectified by the class-E rectifier, however, some unwanted RF signal remain. To filter out these signal, low pass filter (LPF) is responsible for reconstructing the original envelope signal large enough to operate GaN RF PA. At node "C", the only baseband frequency envelope current (or voltage) remains through LPF.

The advantages and disadvantages of EA and proposed EA are summarized as follows. For the conventional HSA for EA, the efficiency decreases as the BW increases. Also noise caused by the switching stage can cause problems with the Rx band. The conventional SMC for EA has the problem of using series switch, reducing efficiency at low duty ratio and also issue of implementing PWM system. On the other hand, the proposed EA has the following advantages. First, the basic operation is the same as a normal ET PA. Second, efficiency does not decrease as BW increases. This is because the converter operates at the same frequency range even if the

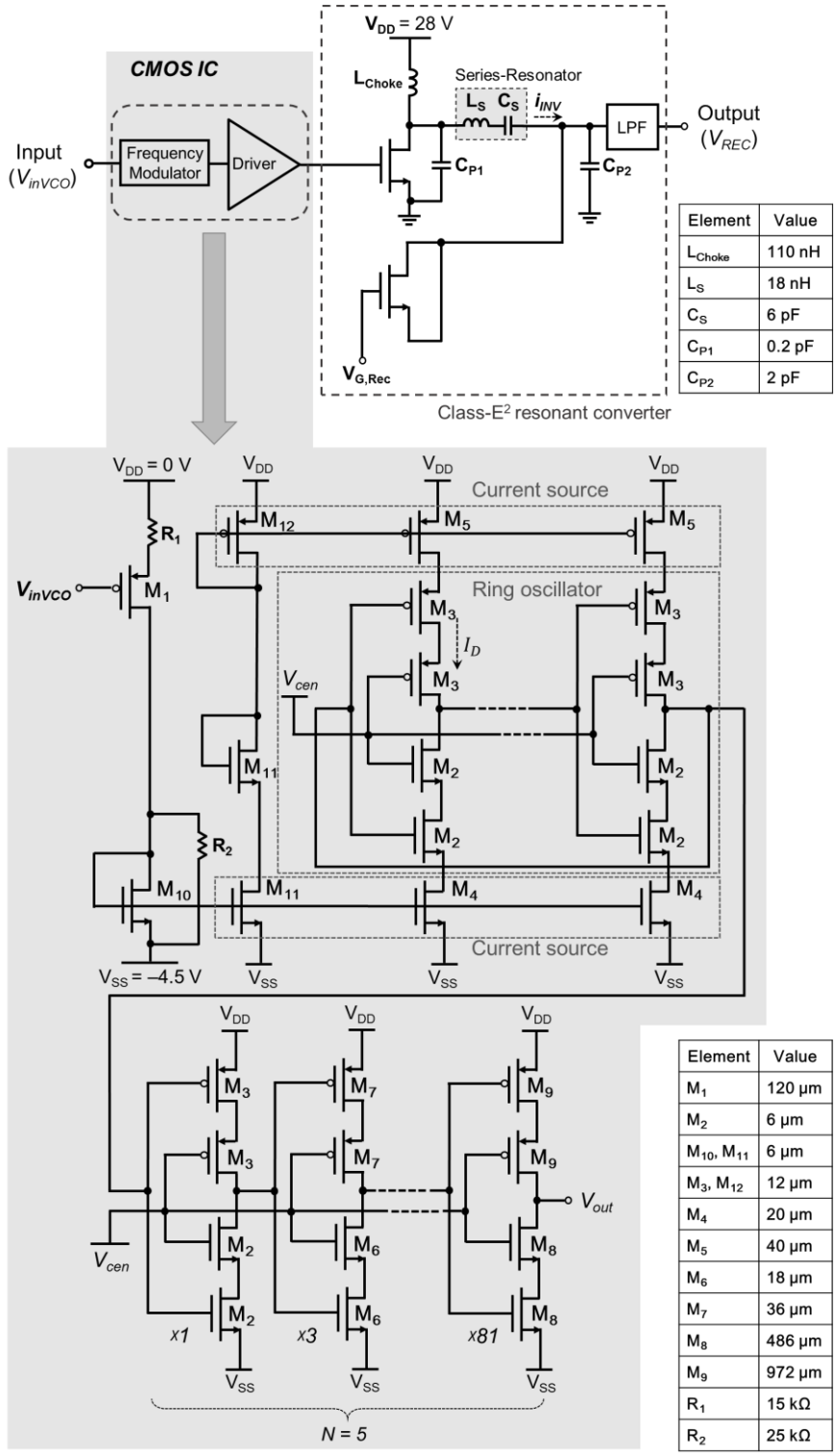
envelope frequency (or envelope signal BW) increases. Third, no additional equipment or circuit is required to generate the PWM signal [2], [3], which can reduce the complexity of the system.

3.3 Detailed ET PA Design and Simulation

3.3.1 Envelope Amplifier Design using Current-Starved VCO (CSVCO)

The detailed circuit schematic of the proposed EA is shown in Fig. 3.14. The proposed EA is composed of frequency modulator, a gate driver, and class-E^2 resonant converter. First, the class-E^2 converter is divided into a class-E inverter and class-E rectifier. This topology has an advantage that the shunt switch is used with GaN HEMT, which can overcome the problem caused by using the series switch. When the high frequency pulse train is applied to the gate node of the class-E inverter, it produces a sinusoidal current waveform by a series-resonator circuit and transfers to the class-E rectifier, which provides dc current again by a low pass filter (LPF). As mentioned above, since both the class-E inverter and rectifier operate in zero voltage switching (ZVS) and zero derivative voltage switching (ZDVS) conditions, it can maintain high efficiency regardless of the switching frequency.

The current-starved VCO (CSVCO) is used as the frequency modulator to generate PFM signal. Its operation is similar to the basic ring oscillator. N-type MOSET M_2 and p-type MOSFET M_3 operate as an inverter, which are designed using stacked structure to overcome breakdown voltage. The MOSFETs M_4 and M_5 operate as current source, which limit the current available to the inverter. The currents in M_1 and M_{10} are the same, which set by the input control voltage (V_{inVCO}). The currents in M_1 and M_{10} are mirrored in each MOSFETs M_{11} and M_{12}, which mirror again the current to current source stage. The ring oscillator is starved for the current in mirrored by M_{11} and M_{12} and its output frequencies are changed by the input voltage (V_{inVCO}) of p-type MOSFET (M_1). We suppose the drain current flowing



Element	Value
L_{Choke}	110 nH
L_S	18 nH
C_S	6 pF
C_{P1}	0.2 pF
C_{P2}	2 pF

Element	Value
M_1	120 µm
M_2	6 µm
M_{10}, M_{11}	6 µm
M_3, M_{12}	12 µm
M_4	20 µm
M_5	40 µm
M_6	18 µm
M_7	36 µm
M_8	486 µm
M_9	972 µm
R_1	15 kΩ
R_2	25 kΩ

Fig. 3.14. Detailed circuit schematic of the designed frequency modulator using current-starved VCO (CSVCO) with gate driver.

in the ring oscillator to I_D and its number of stage to N, the frequency of the VCO output the oscillation current can be expressed as follows [19]:

$$f_{OSC} = \frac{I_D}{N \cdot C_{tot} \cdot V_{DD}} \tag{17}$$

When the input voltage of the CSVCO increase, the current flowing through the M_1 and M_{10} decrease. In addition, the reduced current in the current source is mirrored, which causes the output frequency to decrease. As analyzed in previous chapter, the frequency modulator requires the output frequency response that is inversely proportional to the input voltage. Therefore, p-type can be used for input control MOSFET. If you want the response proportional to the input voltage, applying n-type MOSFET instead of p-type.

Typical CSVCO is nonlinear because the input is applied directly to the gate of MOSFET. In general, the drain current flowing to MOSFET is proportional to the square of the gate-source voltage. To make a linear drain current to the input voltage of the CSVCO, we applied source-degeneration method using R_1 and the method of widening the gate width of M_1 compared to M_{10}. In the source-degeneration method, a constant gate-source voltage is applied to the MOSFET regardless of the gate voltage. The gate width of M_1 is made wider than M_{10} so that M_1's gate-source voltage becomes always approximately threshold voltage, which is independent to the input voltage (V_{inVCO}). The resistor R_2 connected in parallel with M_{10} controls the output frequency tuning range by adjusting the VCO gain.

The input capacitance of GaN HEMT used in the class-E inverter is 4.1 pF. This capacitance behaves as the output load capacitance of the VCO. However, the open circuit capacitance of the VCO is very small, which is insufficient to drive the load capacitance of 4.1 pF. Thus, a gate driver is required to drive the pulse voltage between GaN HEMT and the VCO. The gate driver consists of chain of the inverters as shown in the Fig. 3. 14. It is well known that in order to achieve the optimized delay time of the pulse signal for cascaded inverter chains, the size of the inverters must be designed to be increased by about three times [20]. To drive the load capacitance of 4.1 pF, the inverter chains with 5-stage are required and its size of the final stage is 486 μm (NMOS, PMOS: 972 μm). When V_{DD} and V_{SS} are 0 V and – 4.5 V respectively, the total dissipated power of the overall circuit is 1.05 W using transient simulations. Since the power of consumed in the CSVCO and gate driver is considerably large, the efficiency of the entire EA greatly decrease. How to overcome this problem is explained in the following sub chapter.

3.3.2 Envelope Amplifier Design using Cross-Coupled VCO (CCVCO)

Although the gate driver with inverter chain is widely used to operate the various converters, generating a precise square voltage waveform and driving it to a gate terminal of large FET wastes huge dc power especially when the switching frequency exceeds hundreds MHz [21]. It is well known that a sinusoidal voltage behaves as an ideal pulse signal when its magnitude is large enough. To quantify how the sinusoidal voltage signal affect the class-E inverter, we have compared the drain current/voltage waveforms using harmonic balance simulation between pulse and sine signal as depicted in Fig. 3.15. Fig. 3.15 (a), (b) show the ideal pulse signal

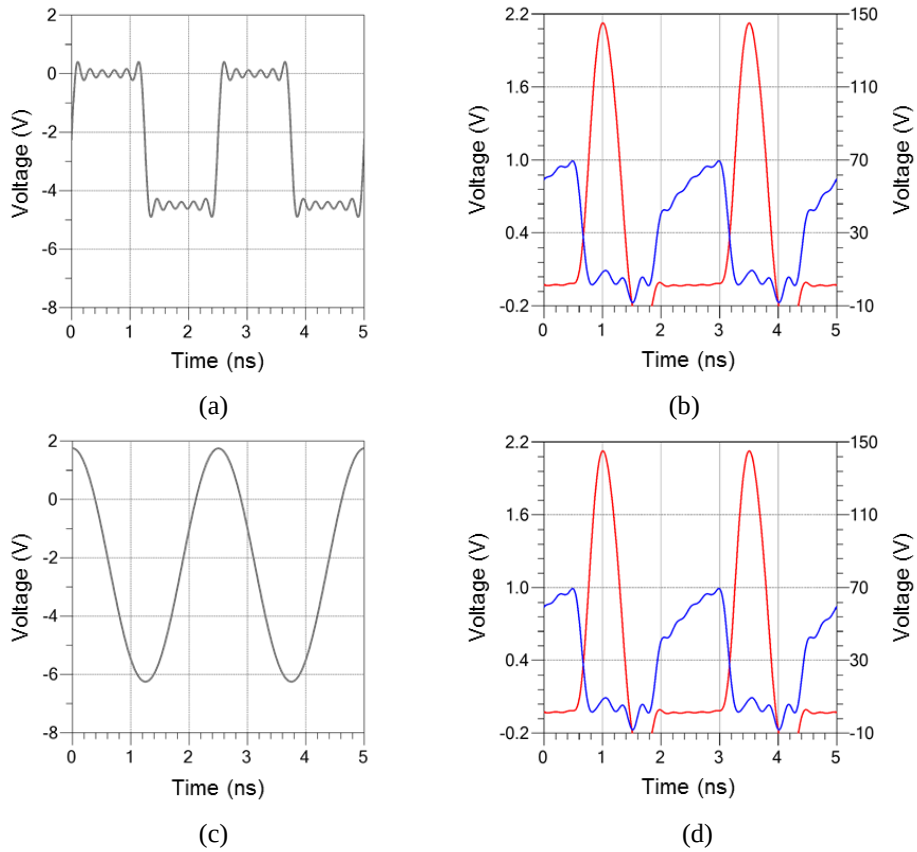


Fig. 3.15. The simulation comparison of class-E inverter waveforms between pulse and sine signal. (a) The ideal pulse signal with maximum harmonic order of 7. (b) Current and voltage waveforms using the ideal pulse. (c) The sine signal with amplitude of 4 V with –2.25 V dc voltage. (d) Current and voltage waveforms using the sine.

applied to the input of the class-E inverter and its simulated current/voltage waveforms. As shown in this figure, the waveforms clearly represents the converter has ZVS and ZDVS condition as in discussed in the previous chapter. Likewise, Fig 3.15 (b), (c) illustrate the ideal sine signal applied to the inverter. The simulated results using large sine signal indicates that the inverter to operate identically when simulated using pulse signal. As a results, it is worthwhile that the ideal pulse signal can be replaced to sinusoidal wave if its amplitude is large enough. In order to verify

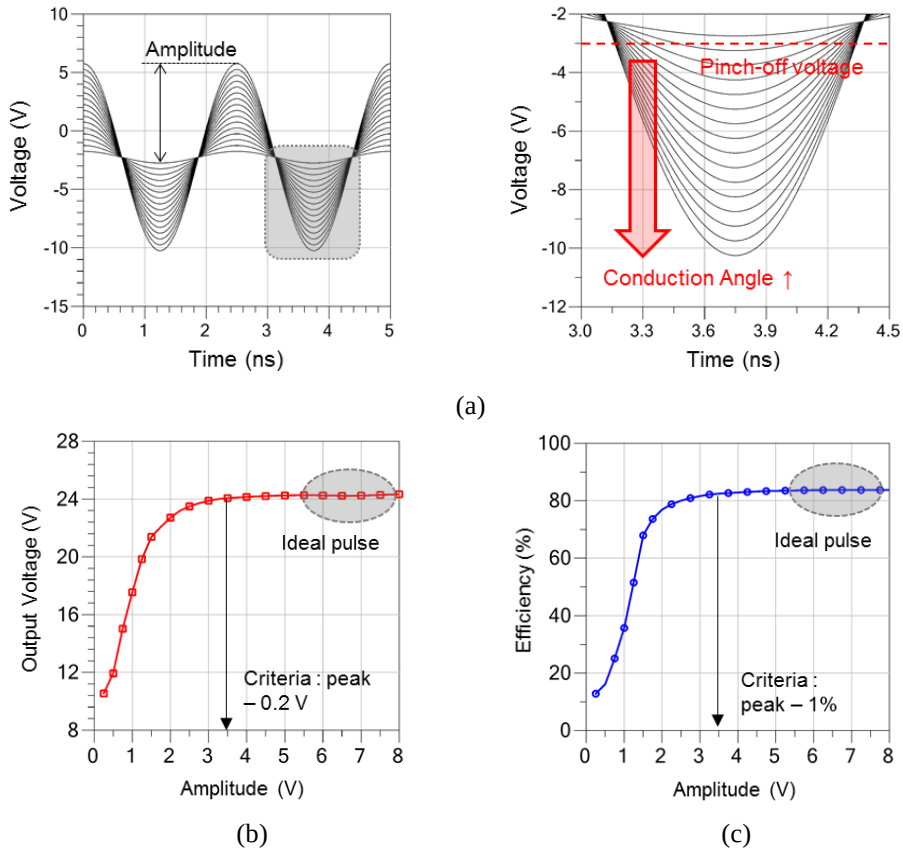
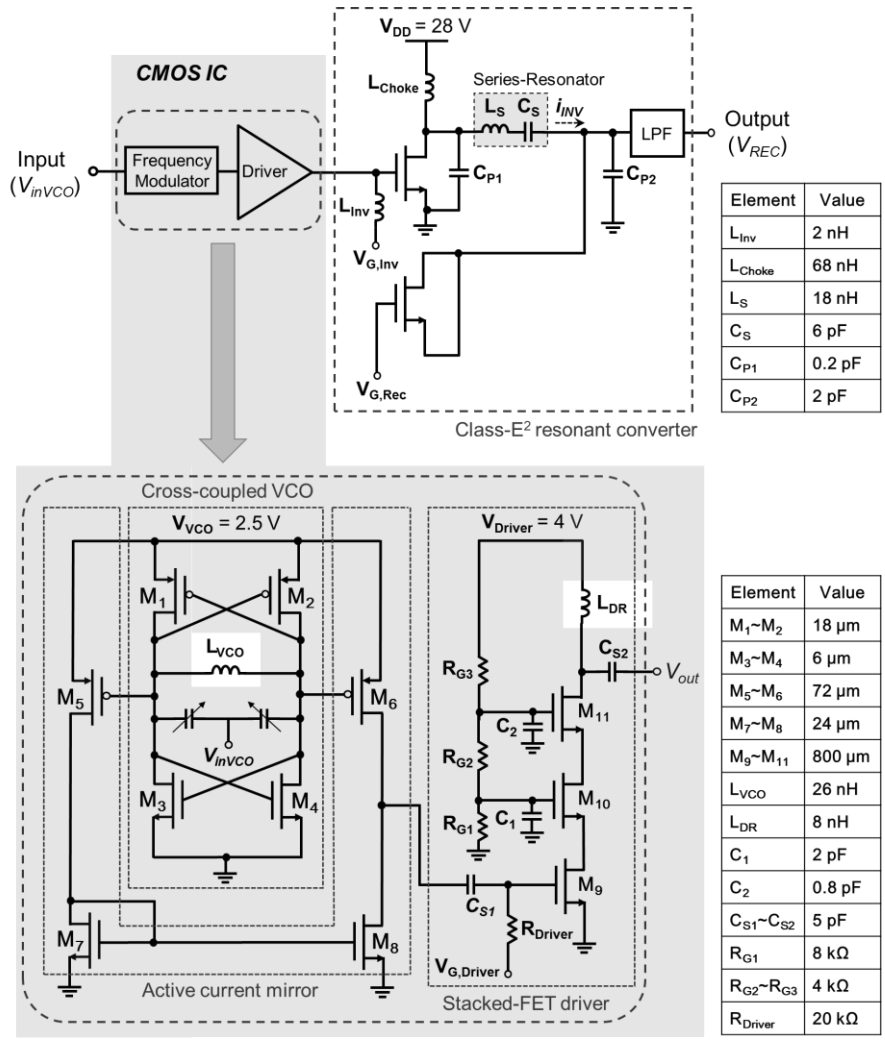


Fig. 3.16. (a) Simulated voltage waveforms by sweeping amplitude from 0.5 V to 8 V with –2.25 V dc voltage. (b) Simulated output voltage and efficiency of the class-E^2 converter according to the amplitude of input sine voltage.

the sine signal that makes the same result as the pulse signal, parameter simulation has been performed. Fig. 3.16 shows the simulated output voltage and efficiency of the converter according to the amplitude of ideal input sine voltage. At amplitude above 3.5 V, there is little output voltage and efficiency degradation. To generate the frequency modulated AC signal depending on the input voltage, a cross-coupled VCO (CCVCO) is designed as the frequency modulator depicted as Fig. 3.17. The oscillation frequency of the CCVCO is determined by the resonance frequency of LC tank [22], which can be controlled by varying the capacitance according to the

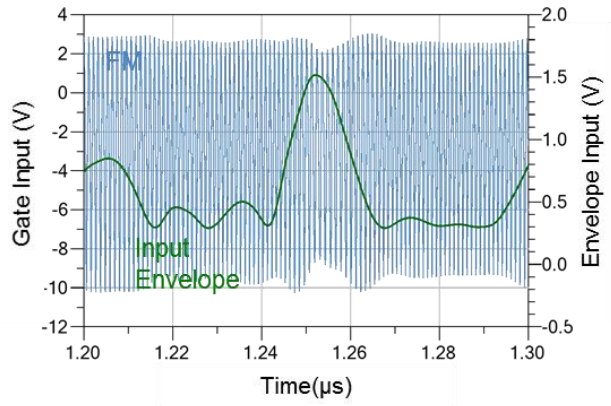


Element	Value
L_{Inv}	2 nH
L_{Choke}	68 nH
L_S	18 nH
C_S	6 pF
C_{P1}	0.2 pF
C_{P2}	2 pF

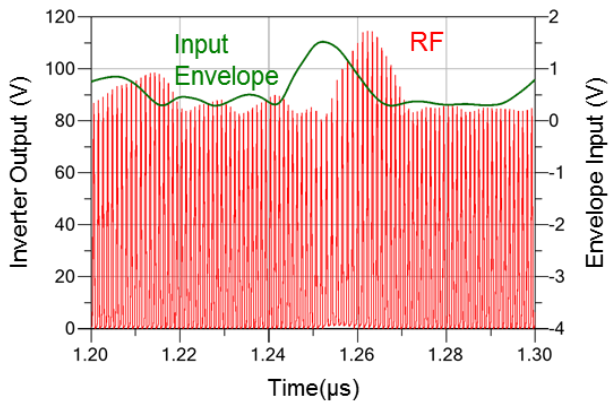
Element	Value
M_1~M_2	18 μm
M_3~M_4	6 μm
M_5~M_6	72 μm
M_7~M_8	24 μm
M_9~M_{11}	800 μm
L_{VCO}	26 nH
L_{DR}	8 nH
C_1	2 pF
C_2	0.8 pF
C_{S1}~C_{S2}	5 pF
R_{G1}	8 kΩ
R_{G2}~R_{G3}	4 kΩ
R_{Driver}	20 kΩ

Fig. 3.17. Detailed circuit schematic of the designed frequency modulator using cross-coupled VCO (CCVCO) with stacked-FET driver.

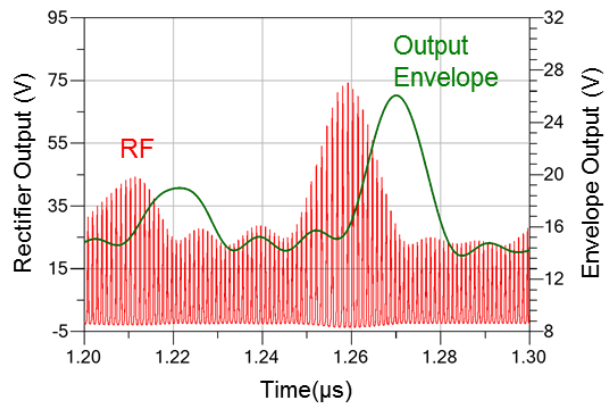
input control voltage (V_{inVCO}). We use a stacked-FETs structure as a driver cell instead of using the inverter chain. The stacked-FETs can generate a sine wave for driving GaN HEMT with a small current. According to the simulation, the proposed stacked-FET driver only consumes 166 mW to drive the class-E inverter while the gate driver mentioned in chapter 3.3.1 consumes 980 mW.



(a)

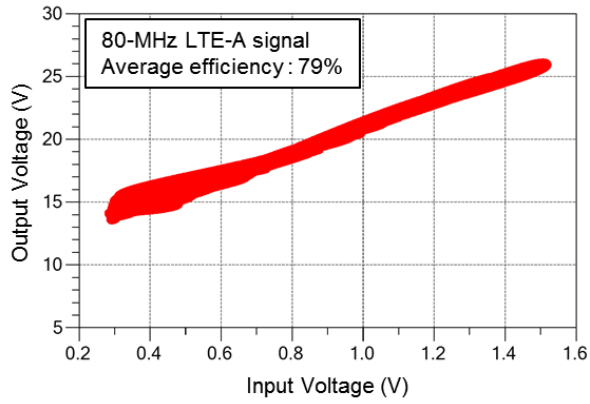


(b)

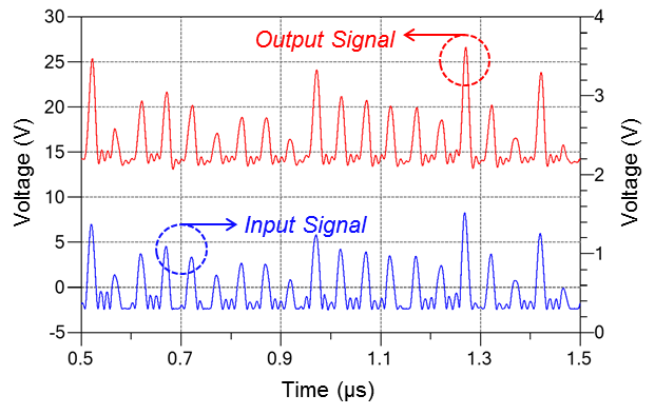


(c)

Fig. 3.18. Transient simulation results of the proposed EA using 80-MHz BW LTE-A signal. (a) Simulated gate voltage according to input envelope voltage. (b) Simulated output voltage of the class-E inverter. (c) Simulated output voltage of the class-E rectifier.



(a)



(b)

Fig. 3.19. (a) Simulated input and output voltage response (AM-AM plot). (b) Simulated input and output envelope signal of the envelop amplifier.

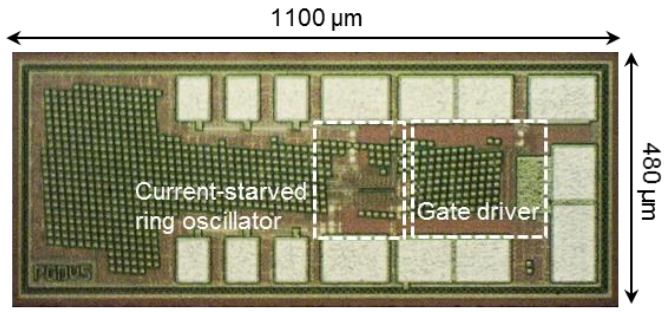
Fig. 3.18 shows the transient simulation results of the designed frequency modulator using 80-MHz BW, intra-band contiguous carrier-aggregated signal. The simulated input and the corresponding PFM signal are depicted in Fig. 3. 18 (a). According to the simulation, when the amplitude of the input envelope changes from 0.3 to 1.5 V, the output frequency of the CCVCO is modulated from 1003 MHz to 850 MHz. The PFM signal make the amplified RF signal in the drain node of class-E inverter as shown in Fig. 3. 18 (b). It is inform that the amplified RF signal has a little envelope frequency components. The rectified signal by class-E rectifier

contains both RF and envelope frequency components. The rectified voltage waveform at the cathode of the rectifier diode is shown in Fig. 3. 18 (c). By eliminating the high frequency (RF) component from the LPF, the proposed EA can obtain the output envelope signal large enough to operate the GaN PA. Fig. 3.19 (a) is the simulated input and output voltage response using 80-MHz LTE-A signal. Fig. 3.19 (b) shows the simulated time domain waveforms of the input and output envelope signal of the EA. The simulated output voltage of the EA is 13.6 to 27.2 V and efficiency of with the LTE-A signal with 50 Ω resistive load is 79%. The simulation indicates that the proposed EA is able to track the input envelope signal even with a wide BW of 80-MHz.

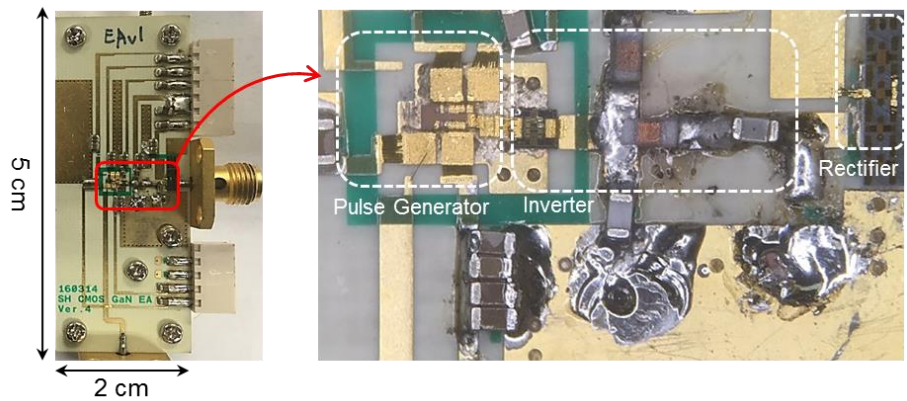
3.4 Measurement Results

Fig. 3.20 shows the photograph of the fabricated EA, and the implemented test module on 2cm x 5cm Duroid RO4350B substrate ($\varepsilon_r \sim 3.66$, $\tan\delta = 0.0037$). The proposed EA has the advantage that the module can be implemented in relatively small size compared to the conventional HAS, since the proposed EA does not contain a bulky external inductor. Fig. 3.20 (a) is the chip photograph of the frequency modulator using the CSVCO and the gate driver, whose size is 1100 μm x 480 μm including bond pads. An enlarged photograph of the entire EA circuit is also depicted as Fig. 3.20 (b). The VCO and the gate driver are fabricated using 0.28-μm SOI CMOS process and integrated on a single chip. The switch of class-E inverter employed in the EA is commercially available Wolfspeed GaN HEMT CGH60015D bare-die chip, which is the same transistor used in the RF PA. Class-E rectifier uses a transistor fabricated using a commercial 0.25-μm GaN pHEMT foundry process. The high-Q air coil inductors from Coilcraft were used as the resonators circuit and RF choke. The LPF used in the class-E rectifier was a Mini-circuit's SLP-120 for low insertion loss and high power endurance.

First of all, performance such as a tuning range and pulse shaping of the frequency modulator is characterized with various input dc voltage. Fig. 3.10 shows the measured pulse frequency of the frequency modulator using the CSVCO according to the input dc voltage. For this measurement, V_{in} is swept from –4 V to –0.8 V to check the output response and the supply voltage of the frequency modulator and the gate driver are 4.5 V (0 V V_{DD}, –4.5 V V_{SS}). When the input dc voltage varies from –4 V to –0.8 V, the output pulse signal of the frequency modulator can have a linear tuning range of about 332 MHz to 584 MHz. This tuning range of the frequency



(a)



(b)

Fig. 3.20. Chip and test module photographs. (a) Die photograph of frequency modulator using the CSVCO and the gate driver. (b) The implemented test module photograph of the EA.

modulator allows to track the envelope up to 40-MHz LTE signals. At least the switching frequency must be 10 times the envelope bandwidth so that it can be distortion-less tracking without degrading linearity of the overall system. To verify that the class-E inverter can operate properly, we performed the measurement that the voltage waveform for the output of the frequency modulator. Fig. 3.2 (a), (b) are the measured voltage waveforms on the gate node of GaN HEMT at oscillation frequencies of 332 MHz (V_{in} = –0.8 V) and 584 MHz (V_{in} = –4 V), respectively. For this measurement, we used R&S RT-ZS60 single-ended probe, which has only 300

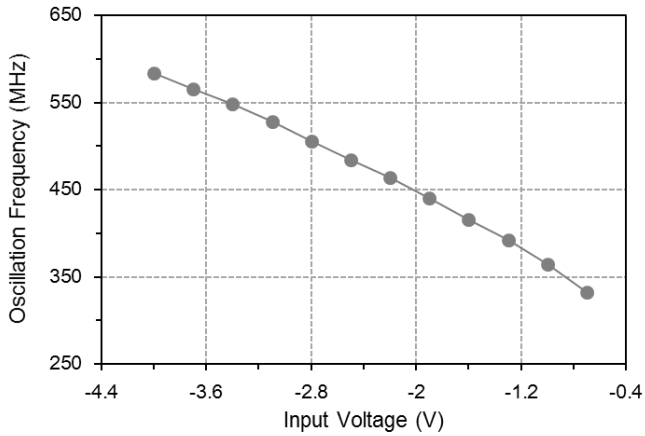
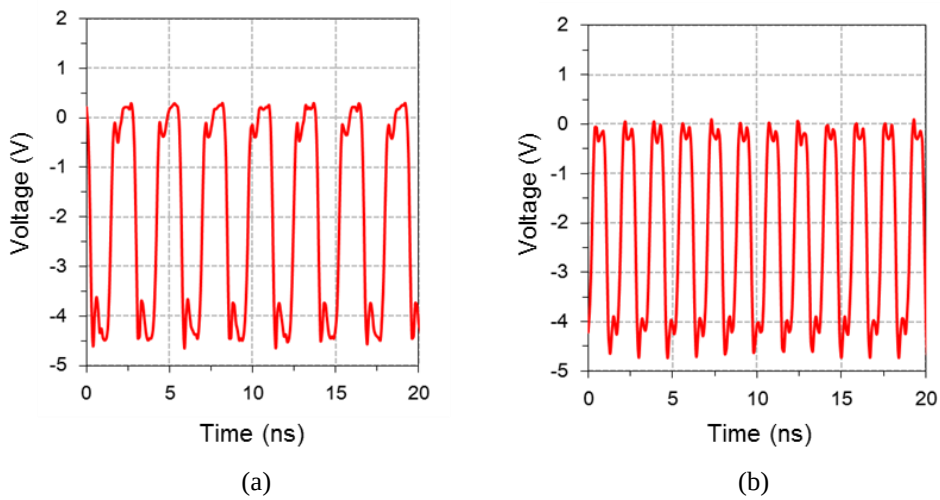


Fig. 3.21. Measured pulse frequency of the CSVCO according to the input dc voltage.



(a) (b)

Fig. 3.22. Measured voltage waveforms on the gate node of GaN HEMT. (a) Oscillation frequency of 332 MHz. (b) Oscillation frequency of 584 MHz.

fF internal capacitance. Since the input of the class-E inverter is heavily loaded by a gate-source capacitance (C_{gs}) of GaN HEMT, the additional 300 fF from the single-ended probe does not significantly affect the matching between the inverter and the frequency modulator. The measured pulse signals have a sufficient swing value to turn-on and -off HEMT from –4.5 V to –0 V (pinch-off voltage of HEMT

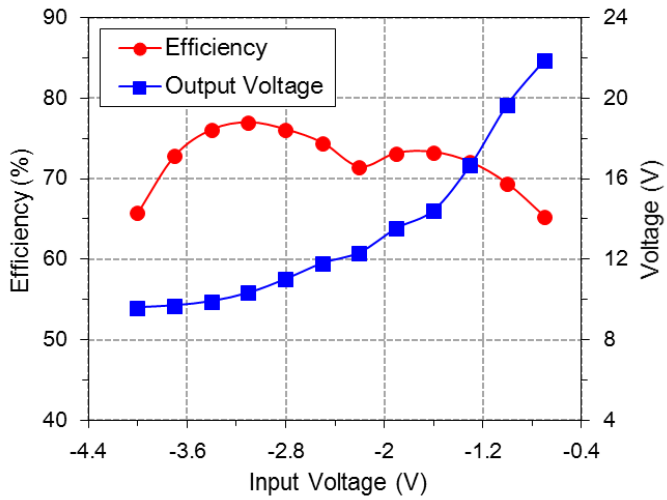
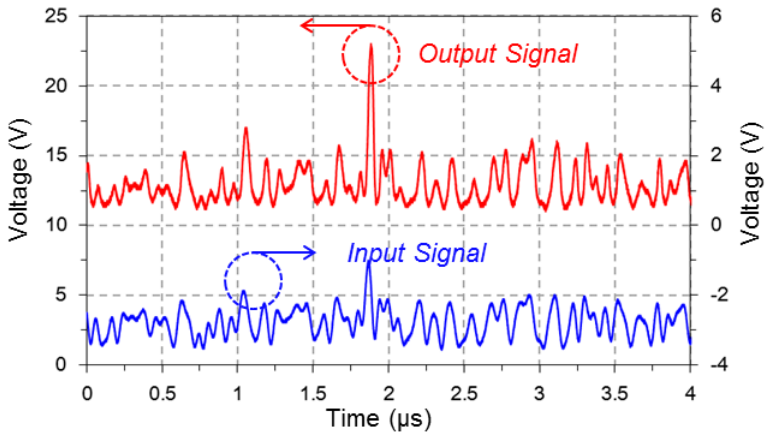


Fig. 3.23. Measured results of the output voltage and efficiency of the EA using the CCVCO according to the input dc voltage.

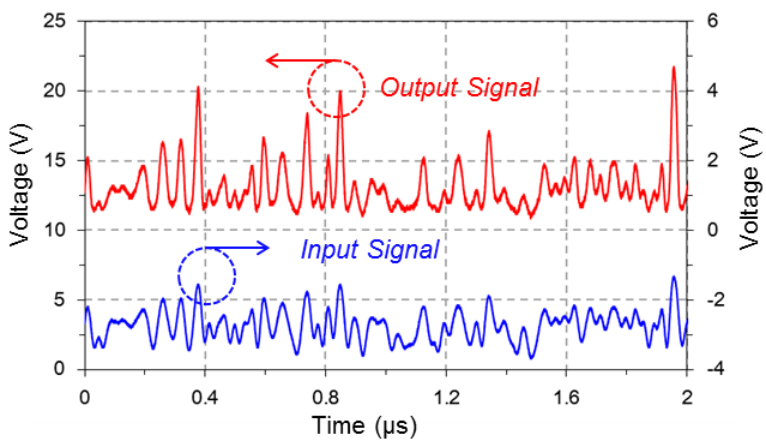
CGH60015D ~ –3.0 V), indicating that the oscillation frequency is modulated properly by the input dc voltage.

Next, static performance of the EA including the class-E^2 converter is characterized with various input dc voltage. Fig. 3.23 shows the measured output voltage and efficiency of the EA with 50 Ω resistive load according to the input dc voltage. As the input dc voltage is changed from –4 V to –0.8 V, the output voltage of the EA can achieve a linear response from 9.6 V to 22 V with a supply voltage of 28 V while maintaining a high efficiency better than 65%. Although the minimum efficiency of the EA is 65%, the maximum efficiency is 77% when the input dc voltage is –3.1 V.

Further investigation of the EA is performed by measuring the dynamic characteristic using LTE signal. Fig. 3.24 shows the measured time domain waveforms of the proposed EA for a load impedance of 50 Ω with 20-MHz and 40-



(a)



(b)

Fig. 3.24. Measured time domain waveforms of the proposed EA with different bandwidth. (a) 20-MHz LTE. (b) 40-MHz LTE.

MHz LTE signals (QPSK, PAPR: 7.5 dB). Since the LTE signals wider than 20-MHz were not readily available in our lab, 40-MHz BW compatible LTE signals was constructed by increasing the sampling rate of the fully loaded 20-MHz LTE signal. The measured output voltage shows the EA is able to track the input envelope dynamics with small dispersion for both 20-MHz and 40-MHz LTE signals. The EA shows 72% efficiency for 7.5 dB PAPR 20-MHz BW signal at 4.7 W average output

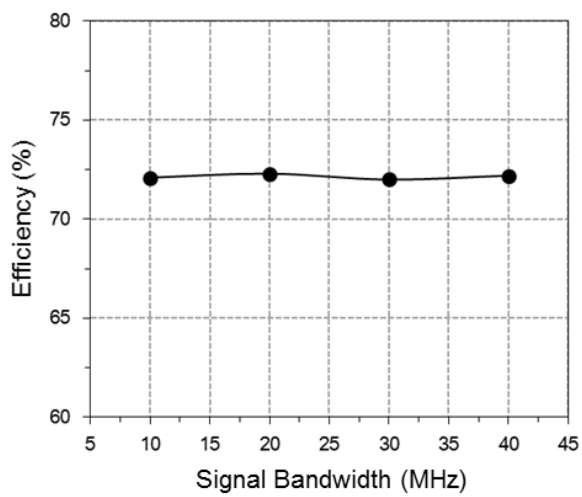
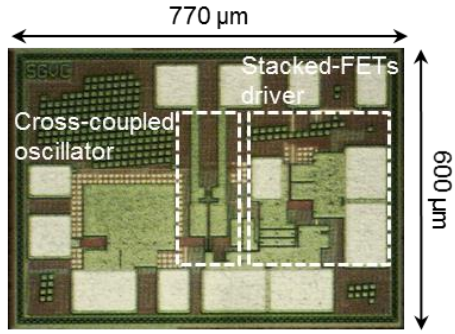


Fig. 3.25. Measured efficiency of the proposed EA according to the LTE signal bandwidth.

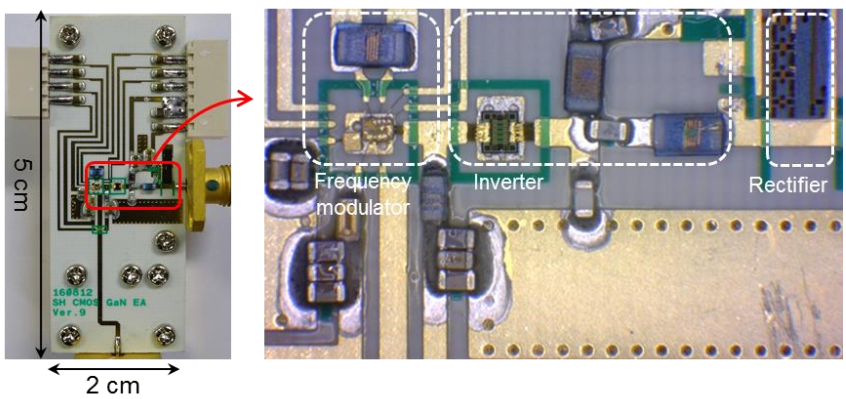
power with 28 V supply.

Fig. 3.25 shows the measured efficiency of the EA according to the signal BW. The measured average efficiencies of over 72% are achieved for signals with modulation BW up to 40-MHz. Even if the signal BW increases, efficiency of the proposed EA does not decrease since the class-E^2 converter has the identical operation frequency, as explain in the chapter 3.2.2. However, the efficiency does not include dc power consumed by the gate driver. When using a current-starved VCO as in the previous chapter, the large dc power is consumed by the shoot-through current of the gate driver. For example, when LTE signals are applied to the proposed EA as shown in Fig. 3.24, the measured dc power consumed by the gate driver is 0.8 W, which significantly reduces the overall average efficiency form 72% to 65%.

Fig. 3.26 shows the photograph of the fabricated EA, and the implemented test module on 2cm ⅹ 5cm Duroid RO4350B substrate ($\varepsilon_r \sim 3.66$, $\tan\delta = 0.0037$). Fig. 3.26 (a) is the chip photograph of the frequency modulator using the CCVCO and



(a)



(b)

Fig. 3.26. Chip and test module photographs. (a) Die photograph of the frequency modulator using the CCVCO and the stacked-FETs driver. (b) The implemented test module photograph of the EA.

the stacked-FETs driver, whose size is 600 μm x 500 μm including bond pads. An enlarged photograph of the entire EA circuit is also depicted as Fig. 3.26 (b). The VCO and the driver are fabricated using the same 0.28-μm SOI CMOS process and integrated on a single chip. All devices, including the switch, rectifier diode, high-Q inductor, were the same as those used to implement the EA using CSVCO. However, we used a different filter (SLP-300), because it must have a large passband to reconstruct the envelope with a wider bandwidth than 40-MHz.

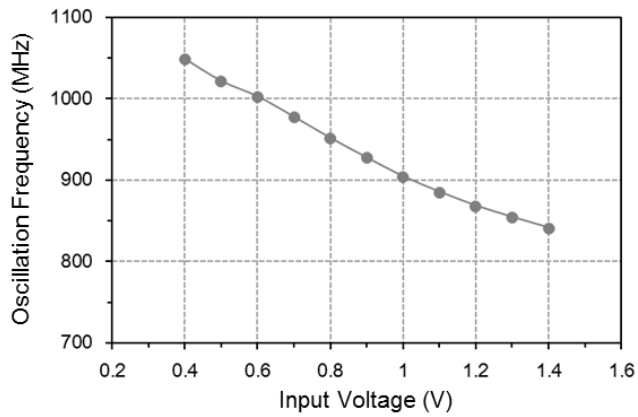
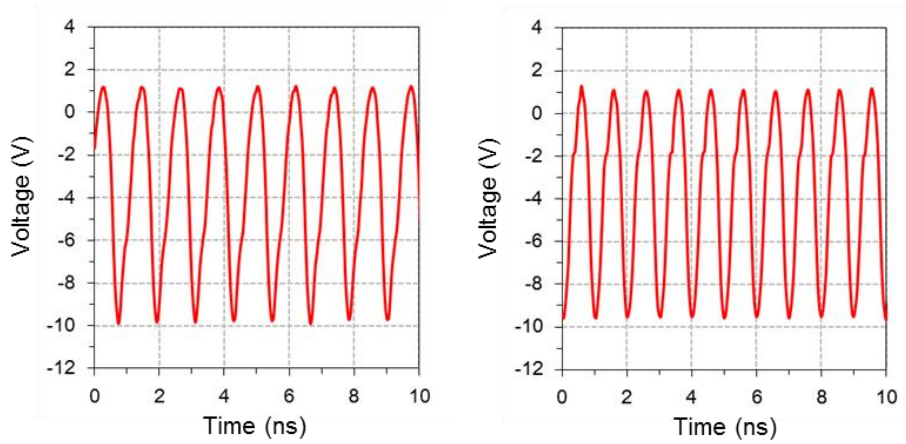


Fig. 3.27. Measured frequency of the CCVCO according to the input dc voltage.



(a) (b)

Fig. 3.28. Measured voltage waveforms at the gate node of GaN HEMT. (a) Oscillation frequency of 842 MHz. (b) Oscillation frequency of 1049 MHz.

Fig. 3.27 shows the measured output frequency of the frequency modulator using CCVCO according to the input dc voltage. When the input dc voltage varies from 0.4 V to 1.4 V, the output pulse signal of the frequency modulator can have a linear tuning range of about 842 MHz to 1058 MHz. This tuning range of the frequency modulator allows to track the envelope up to 80-MHz LTE signals. To verify that the

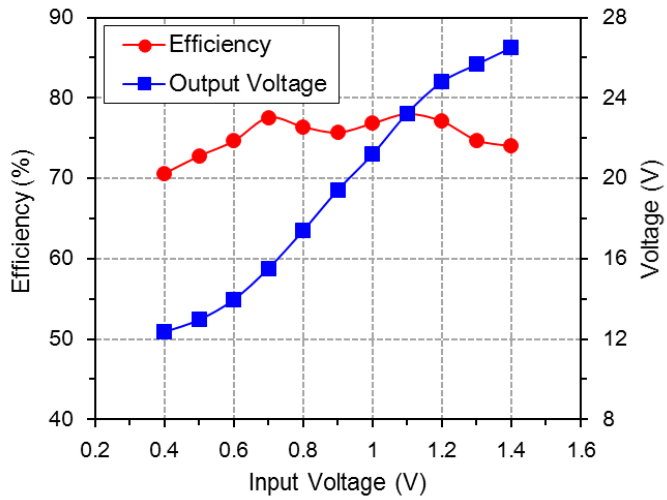
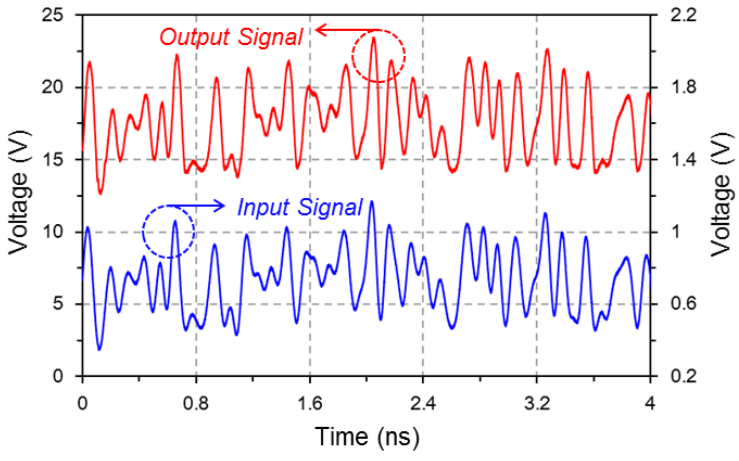


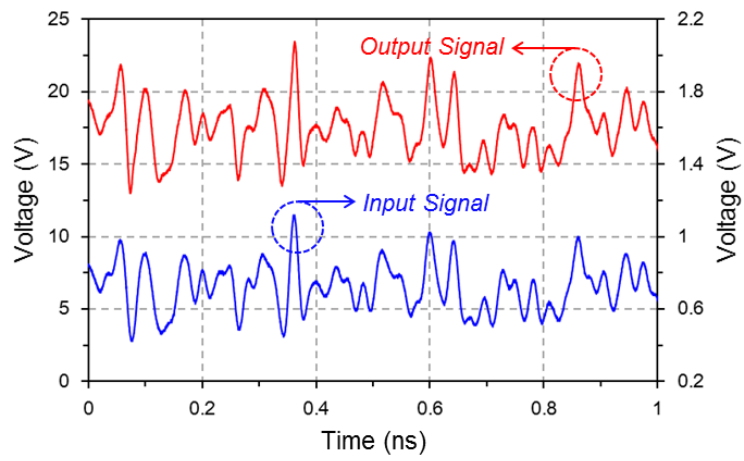
Fig. 3.29. Measured results of the output voltage and efficiency of the proposed EA using the CCVCO according to the input dc voltage.

class-E inverter can operate properly, we performed the measurement that the voltage waveform for the output of the frequency modulator. Fig. 3.28 (a), (b) show the voltage waveforms measured at the gate node of GaN HEMT at oscillation frequencies of 842 MHz and 1058 MHz, respectively. As we have analyzed in the previous chapter, a sinusoidal signal that is larger than a certain amplitude can behave like ideal pulse. The measured voltage waveforms have a sufficient swing value from –10 V to 1 V to be seen as a quasi-pulse at the gate of transistor, indicating that the oscillation frequency is modulated properly by the input dc voltage.

Fig. 3.29 shows the measured output voltage and efficiency of the EA with 50 Ω resistive load according to the input dc voltage. As the input dc voltage is changed from 0.4 V to 1.4 V, the output voltage of the EA can achieve a linear response from 12.5 V to 26.5 V with a supply voltage of 28 V while maintaining a high efficiency better than 70%. The maximum efficiency is 77.5% when the input dc voltage is 0.7 V.



(a)



(b)

Fig. 3.30. Measured time domain waveforms of the proposed EA with different bandwidth. (a) 20-MHz LTE. (b) 80-MHz LTE.

We have also measured the dynamic characteristics of the EA using LTE signals. Fig. 3.30 shows the measured time domain waveforms of the proposed EA for a load impedance of 50 Ω with 20-MHz and 80-MHz LTE signals (QPSK, PAPR: 7.5 dB). The measured output voltage shows the EA is able to track the input envelope dynamics with small dispersion for both 20-MHz and-80 MHz LTE signals. As mentioned above, 80-MHz LTE signal was used by increasing the sampling rate of

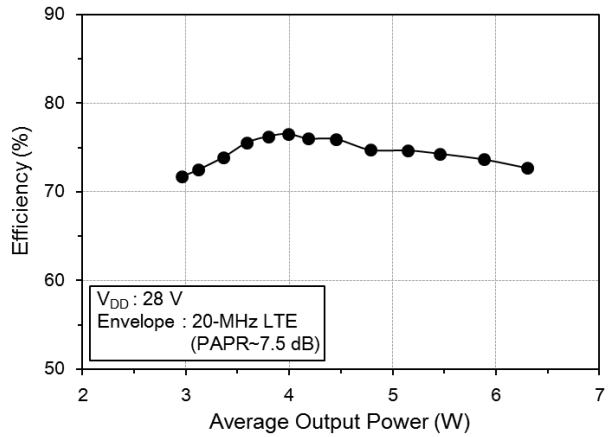


Fig. 3.31. Measured efficiency of the EA with 20-MHz LTE envelope signal.

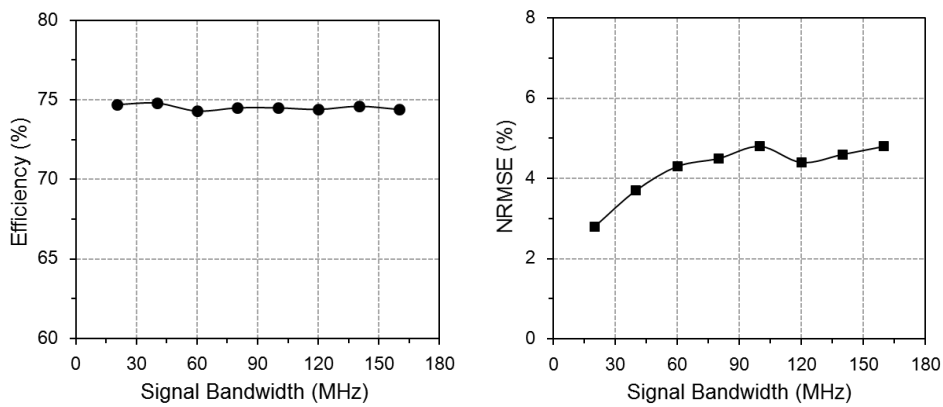
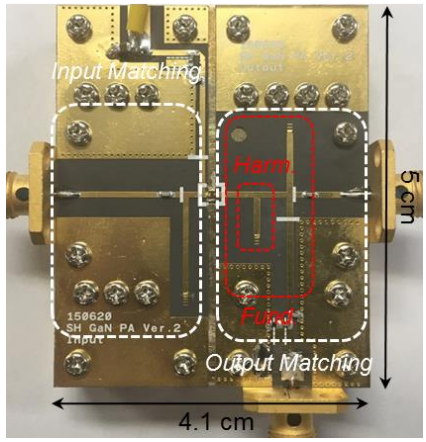
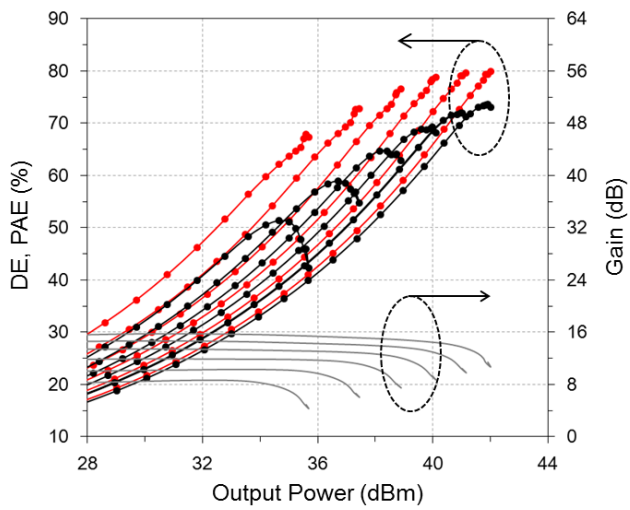


Fig. 3.32. Measured efficiency and NRMSE of the proposed EA according to the LTE signal bandwidth.

20-MHz LTE signal. The measured average efficiency of the EA using 20-MHz BW LTE signal is depicted in Fig. 3.31. The EA shows 74.7% efficiency for 7.5 dB PAPR 20-MHz BW signal at 5.1 W average output power with 28 V supply. The measurement results informs that efficiency can maintain over 70% at low power level, which is another advantage of using PFM control.



(a)



(b)

Fig. 3.33. (a) Implemented GaN RF PA on RT5880 substrate. (b) Measured CW performance of PA at 3.5 GHz by sweeping the drain bias form 13 to 28 V.

Although Fig. 3.30 compares the input and output envelope waveforms to check the linearity of the proposed EA, more accurate index are needed to verify the linearity. Normalized root mean square error (NRMSE) is widely used to represent the linearity metric [2], which can be expressed by the following equation:

$$\text{NRMSE} = \sqrt{\frac{\sum_{n=1}^{N}\left(V_{out\_nor}[n] - V_{in\_nor}[n]\right)^2}{N}} \tag{18}$$

In order to explain the equation, we first need to set the sequences of the input voltage and the output voltage. The sequences $V_{in}[n]$ contains the samples of the input envelope voltage, and $V_{out}[n]$ are the samples of the EA output voltage. By making the peak value of each voltage equal to 1, the normalized sequences $V_{in\_nor}[n]$ and $V_{out\_nor}[n]$ can be expressed as following:

$$\begin{aligned} V_{in\_nor}[n] &= \frac{V_{in}[n]}{\max\left(V_{in}[n]\right)}, \\ V_{out\_nor}[n] &= \frac{V_{out}[n]}{\max\left(V_{out}[n]\right)} \end{aligned} \tag{19}$$

We suppose that the error sequences of the measured input/output voltage is $V_{out\_nor}[n] - V_{in\_nor}[n]$, NRMSE of Eq. (18) can be obtained by comparing the error sequences to the number of total sample (*N*).

Fig. 3.32 shows the measured efficiency and NRMSE of the EA according to the signal BW. Efficiencies of over 74% are achieved for signals with modulation BW up to 160-MHz. The NRMSE increases from 2.8% for 20-MHz signal to 4.8% for 160-MHz signal, indicating a little degradation of linearity for the EA. Even if the

signal BW increases, efficiency of the proposed EA does not decrease since the class-E^2 converter has the identical operation frequency, as explain in the chapter 3.2.2.

Fig. 3.33 (a) shows the photograph of the implemented GaN PA using Duroid RO5880 substrate. The transistor used in the proposed PA is commercially available Wolfspeed GaN HEMT CGH60015D bare-die chip, which is mounted with sintering epoxy to reduce the thermal effect. GaN RF PA is designed using harmonic controlled technique for high efficiency [23]-[25]. Output matching is designed by waveform engineering based on load-pull simulation to obtain the optimum fundamental and harmonic impedances. The optimum fundamental impedance is resistive with slight reactance (Z_1= 24.9 + j23.4 Ω) and the second harmonic impedance is purely reactive (Z_2= j16.4 Ω) for high efficiency operation.

Fig. 3.33 (b) shows measured continuous wave (CW) characteristic at 3.5 GHz by sweeping the drain bias form 13 to 28 V. The applied gate bias is –2.8 V, resulting in a quiescent current of 24 mA when the drain bias is 28 V. A performance of 28 V V_{DD} RF PA is plotted in this figure which shows 74% peak power-added efficiency (PAE) at the 42 dBm output power with gain of 12.4 dB. Peak drain efficiency (DE) at the same output power is as high as 79.8%. In 7 dB back-off power level, 65% DE was measured.

To obtain optimal efficiency and flat gain in ET test using LTE signal, the following shaping function was applied to the EA as:

$$V_{env}(t) = V_{DD} \cdot \left(v_{in}(t) + \alpha \cdot e^{-\left(v_{in}(t)/\alpha\right)} \right) \tag{20}$$

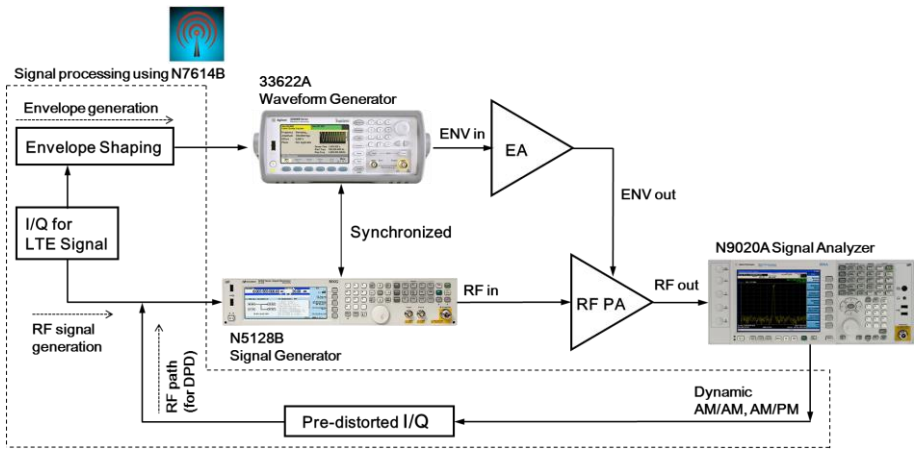


Fig. 3.34. Measurement setup for testing ET PA system

Where V_{DD} is a supply voltage to the EA (28 V) and is detroughing constant, which provides dc-offset bias to prevent the gain collapse in the low power region.

Fig. 3.34 is a block diagram of the measurement setup for testing ET PA system. The LTE envelope and RF signal are generated by Keysight N7614B signal studio software and downloaded to the waveform generator (Keysight 33622A) and RF generator (Keysight N5182B). The incoming envelope signal is modified by the iso-gain shaping function using Eq. (20) and downloaded to the 33622A. The modulated RF signal is generate by the N5182. Timing delay between envelope and RF path for AM and PM correction is adjusted sequentially by observing the ACLR imbalance [26]. The output of the ET PA is captured by Keysight N9020A signal analyzer to measure the ACLR and dynamic characteristics. To correct for the amplitude and phase distortions in the GaN RF PA, a memory digital pre-distortion (DPD) is used to linearize the ET PA system. The pre-distorted I/Q are re-downloaded to the RF signal generator and then up-converted again to test ET PA with pre-distorted signal.

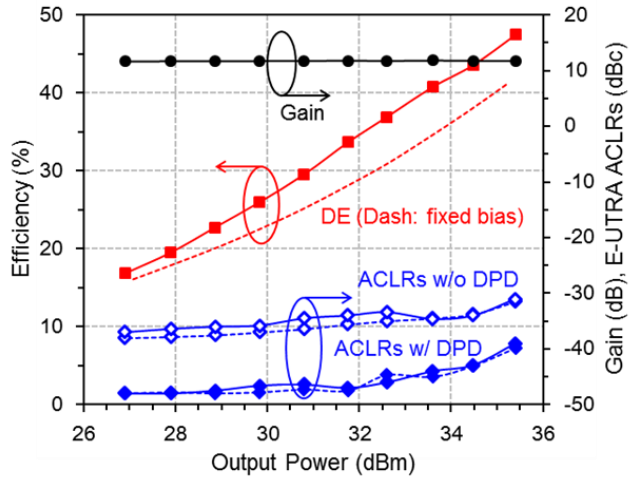


Fig. 3.35. Measured performance of the ET PA using 20-MHz bandwidth LTE (PAPR=7.5 dB). Non-ET performance is also shown as a reference.

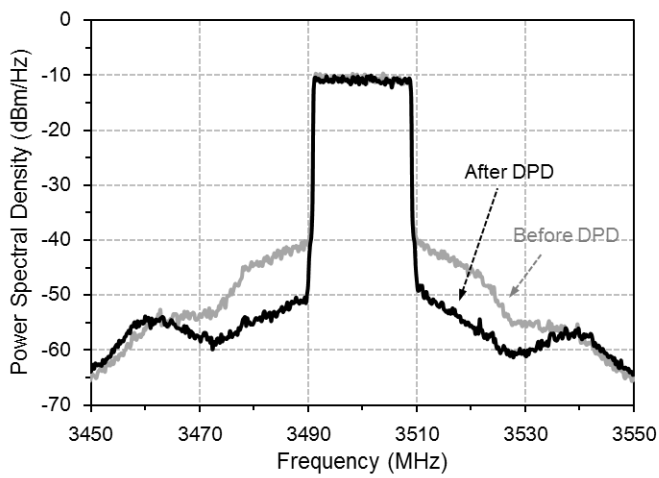


Fig. 3.36. Measured output power spectrum of the entire ET PA system using 20-MHz LTE signals before and after memory digital pre-distortion.

LTE test is performed at the same frequency using 20-MHz BW signal with a PAPR of 7.5 dB at 0.01% probability. Fig 3.35 shows the measured performance of the EA PA using 20-MHz LTE signal. The maximum linear output power reaches 35.4 dBm with a flat gain of 11.7 dB. The overall system DE is 47.4% including the

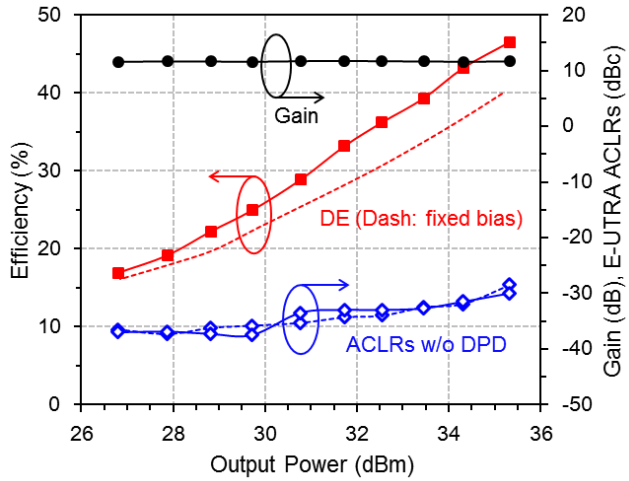
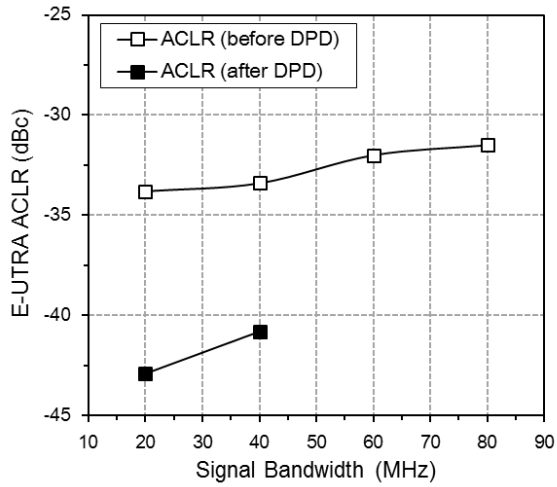


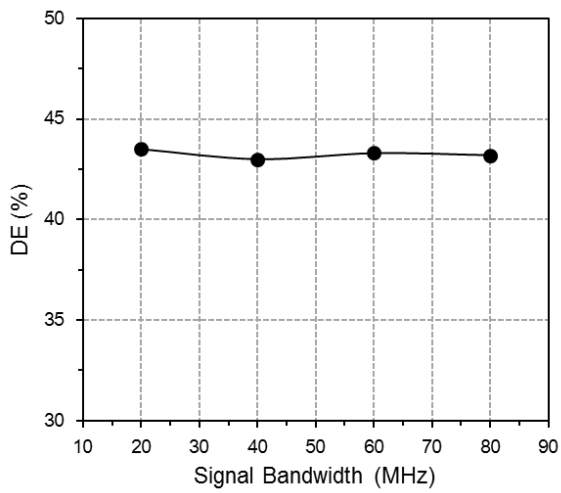
Fig. 3.37. Measured performance of the ET PA using 80-MHz bandwidth LTE (PAPR=7.5 dB) compatible. Non-ET performance is also shown as a reference.

efficiency of the EA. Without ET operation, the same RF PA showed DE of 41.5 with a fixed drain bias of 28 V. So, the DE boosted by ET operation is as much as 5.9%. The measured E-UTRA ACLR of ET PA is –31.2 dBc before linearization and –40.5 dBc at 35.4 dBm after memory digital pre-distortion using N7614B. Fig. 3.36 is the measured output spectrum of the ET PA at 3.5 GHz with the output power of 34.4 dBm with and without pre-distortion. The digital pre-distortion used in this work improves ACLR by 9.3 dB.

To verify the performance using wider BW LTE signal, 80-MHz LTE test is also performed as shown in Fig. 3.37. Compared to Fig. 3.35, the overall system efficiency, gain, and E-UTRA ACLR show very similar characteristics to the 20-MHz BW LTE test. The overall system DE at 35.3 dBm output is 46.5% at 11.7 dB gain and –28.5 dBc E-UTRA ACLR. Like the 20-MHz LTE test, ET can provide 5.5% efficiency improvement in 80-MHz LTE testing.



(a)



(b)

Fig. 3.38. (a) Measured E-UTRA ACLR, and (b) overall system DE of the ET PA at the maximum linear output power according to the LTE signal bandwidth.

Figures 3.38 (a) and (b) show the performance of ET PA with various signal bandwidths. In these figure, the overall system DE and E-UTRA ACLR of the ET PA at 34.4 dBm output is shown as a function of the signal bandwidth from 20- to 80-MHz. Overall system DE is maintained at about 43% from 20- to 80-MHz and the ACLR is slightly reduced by 2.3 dB at 80-MHz LTE compared to 20-MHz. In

TABLE 3.1

Performance Comparison Table of the Reported EAs for Base-station Terminals

Reference	[2]	[3]	[4]		[5]	[6]	[7]	**This work**	
EA Topology	SMC with PWM	SMC with PWM	HSA		Multi-linear Regulator	SMC with PWM	HSA	**Class-E^2 Converter with PFM**	
Application	LTE	LTE	LTE-A		LTE	OFDM	LTE	**LTE**	
PAPR (dB)	7.7	7.7	6.6		8.5	8.8	6.6	**7.5**	
Signal BW (MHz)	20	20	10	60	10	5	20	**20**	**160**
Efficiency (%)	64.1	73	75.7	72.3	76	-	73.2	**74.7**	**74.4**
NMSE (%)	-	-	-	-	-	0.79	-	**0.42**	**1.2**
NRMSE (%)	5.7	2.8	1.48	6.69	-	-	3.41	**2.8**	**4.8**

case of 60-MHz and 80-MHz LTE signal, digital pre-distortion could not be applied to the ET PA since the equipment in our lab has hardware limitations such as high oversampling ratio and baseband signal BW issue.

Table 3.1 summarizes the measured results of our work for 20-/80-MHz BW signals and compares them to the state-of-the-art EAs published to date. To the best of our knowledge, this is the first demonstration of a GaN EA to cover 160 MHz LTE bandwidth. Table 3.2 compares the performance of the wideband ET PA with other published works. Most of published ET PAs has been measured using 10- or 20-MHz BW LTE signals. Even though the most of reported ET PAs suffer from increased memory effect and decreased efficiency of the EA in wideband signal, the EA PA using the proposed EA can support wideband signal up to 80-MHz.

TABLE 3.2

Performance Comparison Table of the Reported ET PAs for Base-station Terminals

Reference	[8]	[9]	[4]	[5]	[10]	[7]	**This work**	
EA Technology	Discrete	Discrete	Discrete	Discrete	GaN HEMT	Discrete	**0.28-μm SOI CMOS / GaN HEMT**	
Application	WiMAX	WiMAX	LTE	LTE	WCDMA	LTE	**LTE**	
PAPR (dB)	8.8	8.5	6.6	8.5	6.6	6.6	**7.5**	
Signal BW (MHz)	10	10	60	10	5	20	**20**	**80**
Frequency (GHz)	2.14	3.54	9.23	2.6	0.88	0.88	**3.5**	
Pout (dBm)	44.2	40	30	40.8	40.1	38.7	**35.4**	**35.3**
Gain (dB)	10.5	10	7.4	10	12.9	15.3	**11.7**	
Overall System DE (%)	57	44	32.4	47.8	50.1	54.4	**47.4**	**46.5**
EA Efficiency (%)	70.1	73.7[2]	72.3	76	80	73.2	**74.7**	**74.5**
E-UTRA ACLR (dBc)	**–28** **–48.3**[1]	**–28.5**[2] **–45.5**[1]	N/A	**–29.4**[2] **–47.8**[1]	**–50.6**[3]	**–25.2** **–48.5**[1]	**–31.2** **–40.5**[1]	**–28.5**

[1]: ACLR after DPD

[2]: This result is graphically estimated

[3]: Adjacent channel power ratio (ACPR) after DPD

3.5 Conclusions

In this work, a GaN EA using class-E^2 architecture for wideband ET system is demonstrated to cover 80 MHz LTE signal. To guarantee a linear output response to the input envelope signal and high-efficiency operation, the PFM concept has been applied to the class-E^2 converter. The system consists of the GaN class-E^2 converter which output is adaptively adjusted by a CMOS controller, and a 3.5 GHz high-efficiency harmonic tuned GaN RF PA. The CMOS controller generate frequency modulated signal depending on the magnitude of the envelope signal, which operates the converter. A detailed analysis to verify operation principle of the proposed EA has been presented, it has been confirmed that the EA can achieve better performance by using pulse frequency modulation (PFM) instead of typical pulse width modulation (PWM) method.

According to the measurement results, the EA delivers more than 74% measured efficiencies using 20-MHz LTE envelope signals. The EA is not exposed to efficiency and linearity degradation in wideband operation, thus maintaining efficiency as the signal bandwidth increases from 20-MHz to 160-MHz. The measured output of the EA can achieve a large dynamic V_{DD} enough to operate GaN RF PA from. The overall ET PA system is tested under 80-MHz LTE signal and shows 46.5% overall drain efficiency (DE) at 35.3 dBm average output power. As a result of the measurement using various LTE signals, the ACLR of the proposed ET PA system is degraded by only 2.1 dB without degrading efficiency.

To our knowledge, this work is the first demonstration of a GaN ET PA system for 80-MHz LTE applications. The proposed method has potential to cover even wider BW signals for future wireless communication standards.

3.6 References

[1] J. Kim, D. Kim, Y. Cho, D. Kang, S. Jin, B. Park, K. Moon, H. Jin, S. Koo, and B. Kim, “Wideband envelope amplifier for envelope-tracking operation of handset power amplifier,” in *Proc. Microwave Conference (EuMC), Dig.*, Oct. 2014, pp. 1352-1355.

[2] S. Shinjo, Y-P. Hong, H. Gheidi, D. F. Kimball, P. Asbeck, “High speed, high analog bandwidth buck converter using GaN HEMTs for envelope tracking power amplifier applications,” in *Proc. IEEE Topical Conf. Wireless Sensors and Sensor Networks (WiSNet), Dig.*, Jan. 2013, pp. 13-15.

[3] Y.-P. Hong, K. Mukai, H. Gheidi, S. Shinjo, and P. Asbeck, “High efficiency GaN switching converter IC with bootstrap driver for envelope tracking applications,” in *Proc. IEEE RF Integr. Circuits Symp. Dig*., Jun. 2013, pp. 353-356.

[4] P. T. Theilmann, J. J. Yan, C. Vu, J.-S. Moon, H. P. Moyer, and D. F. Kimball, “A 60MHz bandwidth high efficiency X-band envelope tracking power amplifier,” in *Proc. IEEE Compound Semicond. Integr. Circuit Symp. (CSICS), Dig.*, Oct. 2013, pp. 1-4.

[5] J. H. Kim, H. S. Son, W. Y. Kim, C. S. Park, "Envelope amplifier with multiple-linear regulator for envelope tracking power amplifier", *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 11, pp. 3951-3960, Nov. 2013.

[6] M. Liu, D. Zhang, and Z. Zhou, “Linear regulator design considerations of the serial linear-assisted switching converter used as envelope amplifier,” *IEEE Trans. Power Electronics*, vol. 31, no. 5, pp. 3673-3689, May. 2016.

[7] Y. Liu, C.-S. Yoo, J. Fairbanks, J. Yan, D. Kimball, and P. Asbeck, “A 53% PAE envelope tracking GaN power amplifier for 20MHz bandwidth LTE signals at 880MHz,” in *Proc. IEEE Topical Conf. on Power Amplifier for Wireless and Radio Appl. (PAWR) Dig.*, Jan. 2016, pp. 30-32.

[8] C. Hsia, A. Zhu, J. J. Yan, P. Draxler, D. F. Kimball, S. Lanfranco, and P. M. Asbeck, “Digitally assisted dual-switch high-efficiency envelope amplifier for envelope-tracking base-station power amplifiers,” *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 11, pp. 2943-2952, Nov. 2011.

[9] J. H. Kim, G. D. Jo, J. H. Oh, Y. H. Kim, K. C. Lee, J. H. Jung, and C. S Park, “High-efficiency envelope-tracking transmitter with optimized class-F^{-1} amplifier and 2-bit envelope amplifier for 3G LTE base station,” *IEEE Trans. Microw. Theory Techn.*, vol. 59, no. 6, pp. 1610-1621, Sep. 2011.

[10] C.-S. Yoo, Y. Liu, J. Fairbank, P. Asbeck, P. Theilmann, and D. Kimball, “High efficiency multi-band envelope tracking power amplifier with tunable output frequency bands,” in *Proc. IEEE Wireless and Microw. Techn. Conf. (WAMIC ON), Dig.*, Jun, 2015, pp. 1-4.

[11] M. Kwak, D. F. Kimball, C. D. Presti, A. Scuderi, C. Santagati, J. J. Yan, P. M. Asbeck, L. E. Larson, “Design of a wideband high-voltage high-efficiency BiCMOS envelope amplifier for micro-base-station RF power amplifiers,” *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 6, pp. 1850-1861, Jun. 2012.

[12] M. K. Kazimierczuk, and J. Jozwik, “Resonant DC/DC converter with class-E inverter and class-E rectifier,” *IEEE Trans. Ind. Electon.*, vol. 36, no. 4, pp. 468-478, Nov. 1989.

[13] J. J. Jozwik, and M. K. Kazimierczuk, “Analysis and design of class-E^2 DC/DC converter,” *IEEE Trans. Ind. Electon.*, vol. 37, no. 2, pp. 173-183, Apr. 1990.

[14] H. Kozumi, M. Iwadare, and S. Mori, “Class E^2 DC/DC converter with second harmonic resonant class E inverter and class E rectifier,” in *Proc. 3rd Annu. Appl. Power Electron. Conf.*, Feb. 1994, pp. 1012-1018.

[15] F. H. Raab, “Idealized operation of the class-E tuned power amplifier,” *IEEE Trans. Circuits Syst.*, vol. CAS-24, no. 10, pp. 725-735, Dec. 1977.

[16] M. K. Kazmierczuk, and K. Puczko, “Exact analysis of class E tuned power amplifier at any Q and switch duty cycle,” *IEEE Trans. Circuits Syst.,* vol. 36, no. 2, pp. 149-159, Feb. 1987.

[17] M. Kazimierczuk, “Analysis of class E zero-voltage-switching rectifier,” *IEEE Trans. Circuits Syst.,* vol. 37, no. 6, pp. 747-755, Jun. 1990.

[18] M. Kazimierczuk, and K. Puczko, “Class E low dv/dt synchronous rectifier with controlled duty ratio and output voltage,” *IEEE Trans. Circuits Syst.,* vol. 38, no. 10, pp. 747-755, Oct. 1991.

[19] P. K. Rout, D. P. Acharya, and G. Panda, “A multiobjective optimization based fast and robust design methodology for low power and low phase noise current starved VCO,” *IEEE Trans. Semicond. Manuf.,* vol. 27, no. 1, pp. 747-755, Feb. 2014.

[20] D. A. Hodges, H. G. Jackson, and R. A. Saleh, *Analysis and Design of Digital Integrated Circuits,* 3rd ed. New York, NY, McGraw-Hill, 2004.

[21] M.-S. Jeon, J.-L. Woo, S. Park, and Y. Kwon, “A pulsed dynamic load modulation technique for high-efficiency linear transmitters,” *IEEE Trans. Microw. Theory Techn.,* vol. 63, no. 9, pp. 2854-2866, Jul. 2015.

[22] D. Ham, and A. Hajimiri, “Concepts and methods in optimization of integrated LC VCOs,” *J. Solid-State Circuit*, vol. 36, no. 6, pp. 896-909, Jun. 2001.

[23] J. H. Kim, S. J. Lee, B. H. Park, S. H. Jang, J. H. Jung, C. S. Park, “Analysis of high-efficiency power amplifier using second harmonic manipulation: inverse class-F/J amplifiers,” *IEEE Trans. Microw. Theory Techn.,* vol. 59, no. 8, pp. 2024-2036, Aug. 2011.

[24] K. Clen, and D. Peroulis, “Design of highly efficient broadband class-E power amplifier using synthesized low-pass matching networks,” *IEEE Trans. Microw. Theory Techn*., vol. 59, no. 12, pp. 3162-3173, Dec. 2011.

[25] J. Xia, X.-W. Zhu, and L. Zhang, “A linearized 2–3.5 GHz highly efficient harmonic-tuned power amplifier exploiting stepped-impedance filtering matching network,” *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 9, pp. 602-604, Sep. 2014.

[26] J. Jeong, G. Chaudhary, and Y. Jeong, “Time mismatch effect in linearity of hybrid envelop tracking power amplifier,” *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 8, pp. 550-552, Jun. 2015.

Chapter 4

Conclusions and Future Works

In this dissertation, two advanced techniques to solve system issues in envelope tracking PAs are developed.

The second chapter developed a broadband 2-stage SOI CMOS stacked-FET PA with reconfigurable interstage matching network for envelope tracking application. The power stage is based on Class-J mode of operation, where output matching is realized using two-section low-pass network. To guarantee class-J mode of operation for the inner stacked FETs as well, Miller capacitors have been added across the drain-source terminals of the common-gate FETs in the stack.

With the broadband output matching, the practical bandwidth limitation to guarantee high overall gain and PAE over the entire bandwidth comes from high-Q interstage matching. To overcome the bandwidth limitation imposed by Bode-Fano criteria, a reconfigurable matching network is employed between the two stacked FETs. Two RF switches made of the same SOI CMOS process as the PAs have been employed to offer three different matching modes according to the operation frequency. This is achieved by changing the effective inductance value of the shunt inductor in the high-pass *C–L–C* interstage network. The fabricated PA shows CW

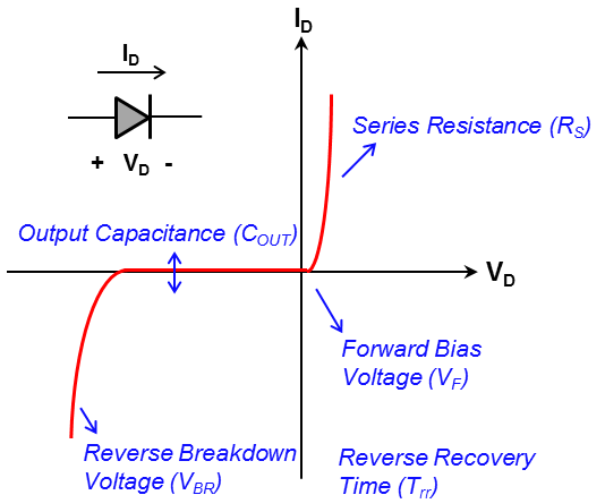


Fig. 4.1. The simplified I-V characteristics of the rectifier diode and its design parameters.

efficiencies in excess of 60% from 0.65 to 1.03 GHz. When tested with an envelope amplifier, the overall ET system efficiency higher than 40% has been achieved using 20-MHz LTE signals from 0.65 to 0.97 GHz. This work represents one of the widest RF bandwidth demonstration for LTE ET PAs for mobile phone applications. As the number of LTE bands increases, the need for PA sharing and wideband operation will ever increase. The proposed idea of reconfigurable interstage matching can provide a practical solution to the bandwidth problems for LTE PAs.

In the third chapter, a novel envelope amplifier has been demonstrated to overcome problems inherited from the conventional hybrid and switch-mode envelope amplifiers. The operation principle and efficiency estimation of the proposed envelope amplifier is investigated using basic class-E amplifier theory and waveform based analysis, also transient simulation using LTE waveform is presented. It is worthwhile that pulse frequency modulation (PFM) control is superior to pulse width modulation (PWM) control in our work. The designed EA using PFM cover

160-MHz BW LTE signal with a little degradation of linearity. The implemented ET PA system demonstrated high efficiency with –28.5 dBc ACLR with 80-MHz BW LTE signal. However, the one of the main drawback of this work is that the proposed EA requires additional circuit to generate PFM signal such as frequency modulator with driver and its dissipated dc power exposes efficiency degradation. Moreover, the rectifier diode in class-E rectifier is the major factor of design elements. It is important to choose the proper diode, since the proposed envelope amplifier can achieve the best performance by considering the various elements of the diode. Fig 4.1 shows the simplified I-V characteristics of the rectifier diode and its design parameters. The reverse recovery time (T_{rr}) must be sufficiently small to satisfy the speed of the rectifier and satisfy the ZVS condition with low forward-bias voltage (V_F). It is also necessary to minimize the loss when the rectifier diode become on-state with a small series resistance (R_S). In addition to, the diode should have an appropriately sized output capacitance to operate as the class-E rectifier. Finally, designer need to have a large breakdown voltage (V_{BR}) to ensure the reliability and dynamic range of the EA system. Therefore, a further work is required to investigate and select the optimal diode for class-E rectifier.

초록

본 학위 논문에서는 고효율 고전압 포락선 추적 전력 증폭기 구현을 위한 시스템 문제를 해결하기 위한 두 가지 기술들을 제안하였다.

첫 번째, 재구성 가능한 단간 정합 네트워크가 있는 2 단 광대역 CMOS 스택 FET RF 전력 증폭기가 광대역 포락선 추적용으로 개발되었다. 제안된 RF 전력 증폭기는 class-J 동작 원리를 기반으로 설계되었으며, 출력 매칭은 2 단 저역통과 매칭 네트워크로 구현되었다. 높은 Q 값을 갖는 중간단 임피던스의 대역폭 제한을 극복하기 위해서 재구성 가능한 매칭 네트워크를 제안하였고, 2 개의 RF 스위치를 사용하여 3 중 주파수 동작 모드가 가능하도록 만들었다. RF 전력 증폭기는 0.32μm SOI CMOS 공정으로 제작되었으며, 0.65 ~ 1.03 GHz 에서 60 % 이상의 효율을 보여 주고 중심주파수 0.85 GHz 에서 최대 효율 69.2 % 를 얻을 수 있었다. 포락선 추적 전력 증폭기 시스템 성능은 동일한 공정으로 제작된 포락선 증폭기를 사용하여 측정하였다. 20-MHz 대역 LTE 신호를 사용하여 측정 한 경우, 전체 시스템은 0.65 GHz 에서 0.97 GHz 까지 40 % 가 넘는 고효율을 얻을 수 있었고, E-UTRA ACLR 은 메모리가없는 디지털 선형 왜곡 이후 전체 대역폭에서 -33dBc 보다 높은 선형성을 얻었다. 본 연구는 GaAs HBT 및 SiGe

BiCMOS 를 포함한 현재까지 발표된 광대역 전력 증폭기 중 효율 및 대역폭 측면에서 가장 높은 시스템 성능을 보여주었다.

두 번째, calss-E^2 구조를 사용한 고효율 GaN 포락선 증폭기가 광대역 LTE 용으로 개발되었다. 제안된 포락선 증폭기는 Calss-E^2 공진 컨버터와 주파수 변조기로 구성되며 컨버터의 출력 전압은 주파수 변조기에 의해 제어되도록 설계하였다. 펄스 주파수 변조 (PFM) 신호를 이용하여 컨버터의 출력은 입력 포락선 신호에 대해 선형 응답을 얻을 수 있었고, 동시에 낮은 전압에서 효율이 감소하는 문제를 해결하였다. 교차 결합 전압 조정 발진기를 이용한 주파수 변조기와 스택 FET 구조의 드라이버는 0.28μm SOI CMOS 공정을 사용하여 제작되었으며, 포락선 추적 시스템을 구성하는 class-E^2 컨버터 및 전력 증폭기는 상용 GaN 소자를 사용하여 구현하였다. 포락선 증폭기는 7.5 dB PAPR 을 갖는 20-MHz 대역 LTE 신호에 대해 50 Ω 부하에서 74.7 %의 효율을 얻었으며, LTE 신호 대역폭이 160-MHz 로 증가함에 따라 효율 저하를 보이지 않았다. CMOS 및 GaN 소자를 사용한 포락선 추적 송신기 시스템은 3.5 GHz 중심주파수에서 20-MHz 대역폭 LTE 신호를 사용했을 때 출력전력 35.4 dBm 에서 47.4 %의 전체 시스템 효율을 보여주었다. 포락선 추적 전력증폭기의 측정된 E-UTRA ACLR 은 선형화 이전에 34.4 dBm 출력에서 -33.8 dBc 이었고, 메모리 디지털 선형화를 적용시켰을 때 동일한 출력에서 -42.9 dBc 로 개선되었다. 80-MHz 대역 LTE 신호를 사용하여 측정 한 결과 전체 시스템 효율은 출력 35.3 dBm 에서

46.5%의 효율을 얻을 수 있었고, 출력 34.4 dBm 에서 -31.5 dBc E-UTRA ACLR 을 얻었다. 포락선 증폭기의 광대역 성능은 신호 대역폭이 20-MHz 에서 80-MHz 로 증가함에 따라 효율 감소 없이 2.3 dB 의 ACLR 차이만을 보여주었다. 본 연구를 통해서 신호 대역폭이 증가함에 따라 기존 포락선 증폭기의 효율 저하 문제를 극복하였으며, 160-MHz LTE 신호를 다룰 수 있는 GaN 포락선 증폭기를 최초로 제안 하였다.

주요어 : 광대역, class-J, class-E^2 공진형 컨버터, CMOS, DC-DC 컨버터, 디지털 선형왜곡 (DPD), 효율, 포락선 증폭기, 포락선 추적 기법 (ET), GaN, LTE, 다중 밴드, 전력 증폭기, SOI, 스택 FET, 전압 조정 발진기.

학번 : 2012-20769