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**Ph.D. DISSERTATION**

**Oxide Based RRAM: Area Effect on Reset  
Current Reduction in Unipolar RRAM by  
using Scaled Cell Structure**

산화물 기반의 저항 메모리의 동작 특성과 스케일링  
효과를 기반으로 한 저항 메모리의 저전력화 연구

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**AUGUST 2012**

**DEPARTMENT OF INTERDISCIPLINARY  
IN NANO-SCIENCE AND TECHNOLOGY  
COLLEGE OF NATURAL SCIENCES  
SEOUL NATIONAL UNIVERSITY**

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이 論文을 工學博士 學位論文으로 提出함

2012 年 6 月

서울대학교 大學院

協同課程 나노科學技術專攻

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柳 庚 昶의 工學博士 學位論文을 認准함

2012 年 6 月

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# Abstract

Over the recent years, rapid progress of information technology (IT) has enabled many researchers to focus on developing the “new memories”. Compared to other conventional memories such as dynamic random access memory (DRAM) and flash memory, new memory has numerous advantages such as low writing power, fast access time, and superb scalability. In particular, the development of resistive random access memory (RRAM), which is a low cost memory using resistance difference depending on the applied electrical signals, may enable the massive production due to its great compatibility with the complementary metal oxide semiconductor (CMOS) process.

However, even though RRAM is very promising in many respects as described above, some shortcomings such as limited understanding of switching mechanism and relatively high switching current still need to be improved. In addition, in unipolar resistive switching, it is very difficult to implement high-density RRAM with conventional metal-insulator-metal (MIM) structure due to large reset/set distribution, large access device

related with current compliance, and relatively high power consumption.

To solve these problems in RRAM research, a few breakthroughs based on the correct understandings of resistive switching mechanism should occur. In these respects, the relations of analytical resistive switching parameters and switching characteristics, which are very important factors for understanding conductive filament (CF) in unipolar RRAM cell, are investigated. In addition, the effects of CF modulation at the switching interface and its area- and structure-related switching characteristics are also discussed.

Particularly in this thesis, the evidence of switching area scaling effect on reset current ( $I_{RESET}$ ) reduction in unipolar RRAM is investigated. Especially, a novel metal-insulator-metal (MIM) structure designed for low-power RRAM application (called crown shape RRAM structure) is proposed to elucidate the area effect for the first time. We demonstrate that the control of contact size and deposition orientation of resistive material is useful in improving the initial CF formation in a crown shape cell. Simple fabrication flow and device performances are also evaluated in terms of forming-less process. Numerical simulation is also performed using 3D random circuit breaker model (RCB) to verify the proposed structure.

In the end,  $I_{RESET}$  reduction is finally confirmed by using highly scaled hole contact cell structure. We fabricated this scaled hole contact cell, which makes it possible to reduce the total area of CF ( $A_{CF}$ ) by reducing the switching area. It is verified that the decrease of CF area in the critical switching region contributes to  $I_{RESET}$  reduction. It is clear that the effect of switching area reduction is significant. Various evidences of  $A_{CF}$  modulation such as increase in on-state resistance ( $R_{ON}$ ) and reset voltage ( $V_{RESET}$ ), decrease in  $I_{RESET}$  and switching power are investigated. Elimination of unwanted leakage current in a scaled contact hole structure is realized by adopting a double-deposited inter layer dielectric (ILD) mold process. These results strongly support the scaling approach, which contributes to the  $I_{RESET}$  reduction in low-power unipolar RRAM application.

*Key Words* – new memory, RRAM, resistive switching, unipolar, scaling, conductive filament, reset current, crown shape, hole contact

**Student Number: 2008 - 30129**

# Contents

<b>Abstract .....</b>	<b>i</b>
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## **Chapter 1**

### **Introduction**

<b>1.1 Overview of RRAM .....</b>	<b>1</b>
-----------------------------------	----------

## **Chapter 2**

### **Unipolar Resistive Switching**

<b>2.1 Conductive Filament (CF) in Initial Resistive Cell States ·</b>	<b>14</b>
<b>2.2 CF Control in Switching Interface in Single Layer Cell ···</b>	<b>19</b>
<b>2.3 CF Control in Switching Interface in Bi-layer Cell .....</b>	<b>32</b>
<b>2.3.1 Bi-layer cell with conductive defect effect .....</b>	<b>32</b>

2.3.2 Bi-layer cell with thickness effect .....	38
2.3.3 Experimental results: Al inserted bi-layer structure .....	44
2.3.4 Experimental results: statistical analysis .....	50
2.4 Reset Current Reduction and CF Modulation .....	56
2.5 Summary .....	61

## **Chapter 3**

### **Scaling Feasibility in Crown Shape RRAM**

3.1 Introduction .....	63
3.2 Experimental Results .....	65
3.3 Summary .....	91

## **Chapter 4**

### **Scaling Characteristics in Trench Contact RRAM**

4.1 Introduction .....	93
4.2 Experimental Results .....	95



**4.3 Summary .....119**

## **Chapter 5**

**Conclusion .....121**

**Bibliography .....123**

**Abstract in Korean .....132**

# Chapter 1

## Introduction

### 1.1 Overview of RRAM

Demands for high-density and low-power non-volatile memories for mass production with low cost process have explosively increased in the last decade.

Scaling of dynamic random access memory (DRAM) and flash memory for high-density memory application have been pursued by the major semiconductor companies and perfervid scientists [1].

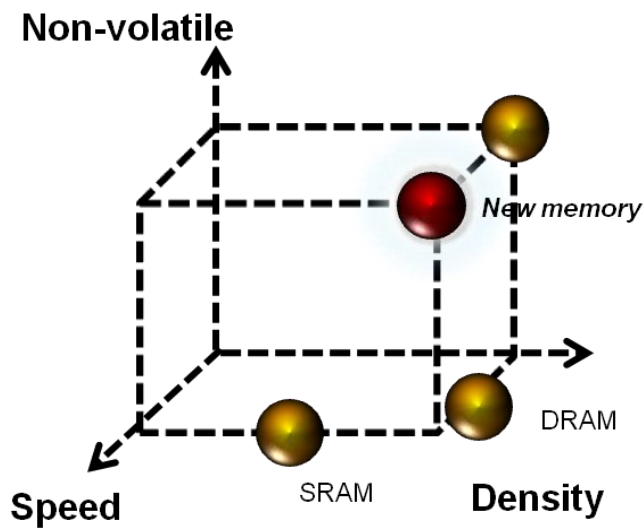
However, as the density of memory device increases while the memory cell size decreases, these conventional memories - such as DRAM and flash memory with operation fundamentals based on charge storage - face the issue of ensuing decrease in charge volume. So the scaling of such charge-based conventional memory appears to face serious limitations, due to the loss of memory cell electrostatic integrity [2].

In order to solve these kinds of scaling issues, various studies on novel material-based memories such as phase change RAM (PRAM), resistive RAM (RRAM) and magnetic RAM (MRAM) have been conducted as next-generation nonvolatile memories in these days due to their advantages such as low writing power, fast writing time, good reliability and possibility of outstanding scalability [1-10]. Among these, RRAM, a new memory using resistance change is considered extremely important as a next-generation memory [11-22].

Since first resistive switching characteristics and their memory application were reported by J.F. Gibbons and J.G. Simmons in 1960s, various properties of resistive switching materials and their switching mechanisms have been reported [24]. Moreover, many researchers have elucidated its strong feasibility for next generation memory. For these reasons, RRAM is widely pursued in these days [1-11].

As illustrated in Fig.1.1, new memories show some important characteristics. First, unlike DRAM and SRAM which are advantageous in high speed yet difficult in high-density and non-volatility, new memory has non-volatile characteristics [11-24]. In addition, as opposed to flash memory which is non-volatile and capable of high-density application yet relatively slow in speed, it is faster in a few ns level. Along with non-volatile characteristics yet fast

switching speed, high-density can be achieved through their already mentioned strong point such as simple structure and scalability, therefore it has advantages of an ideal memory which satisfies all these three important characteristics of a memory [22-39]. Thus, it is expected to be a memory representative of future information technology (IT) industry which will demand fast speed, high-density and low-power. Therefore, new memory studies satisfying such memory characteristics are being actively conducted by researchers studying next generation memory.



**Fig. 1.1** Illustration of important memory requirements such as density, speed, and non-volatility [5].

Table. 1.1 shows the comparison between new memories and other conventional devices [23-26]. Unlike conventional memories, new memory has numerous

advantages such as low writing power, long endurance property and excellent scalability [33-54]. In particular, RRAM is a memory using resistance difference which depends on the applied voltage, and its low cost and CMOS process compatibility can make it advantageous for mass production.

Despite such advantages, it has several issues such as unknown switching mechanism and high switching current [1-22]. Moreover, it is very difficult to accomplish high-density memory with conventional structure due to limitation of photolithography [45-56].

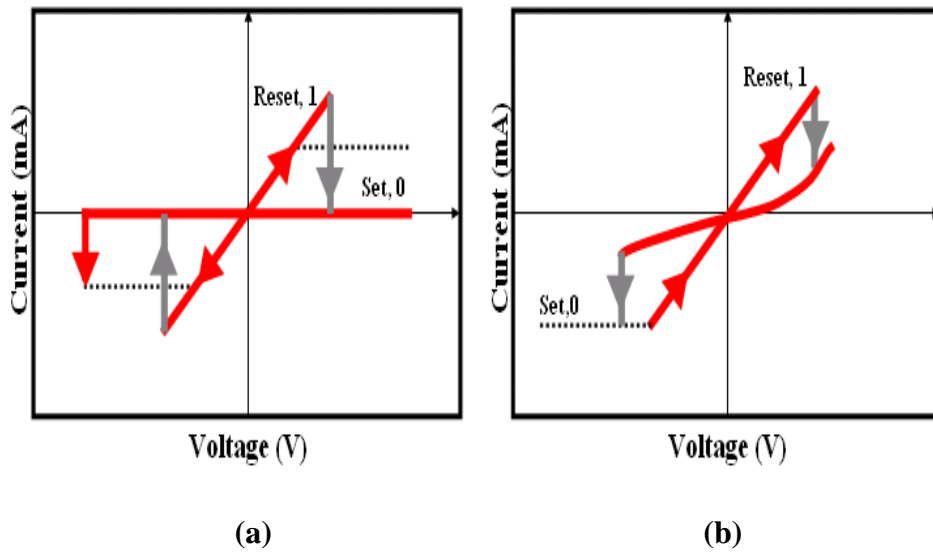
Parameter/Type	DRAM	NAND FLASH	NOR FLASH	MRAM	PRAM	RRAM
Random Access	O	X	O	O	O	O
Power	Low	High	High	High	Low	Low
MLC	X	O	X	X	O	O
Technology Maturity	Mature	Mature	Mature	Not mature	Not mature	Not mature
Scalability	Medium	Good	Medium	Bad	Medium	Good
Scalability limits	Capacitor	Coupling	Drain Disturb	$I_{RESET}$	$I_{RESET}$	$I_{RESET}$
Endurance	$\infty$	$\sim 10^5$	$\sim 10^6$	$\sim 10^8$	$\sim 10^8$	$\sim 10^8$

**Table. 1.1** Comparisons between new memory like PRAM, MRAM, and RRAM and other competitive conventional memories.

Among these kinds of new memories, RRAM, especially the unipolar switching based RRAM is being intensively studied as a next generation memory. Unipolar

RRAM, which is based on thermo-chemical resistive switching mechanism is called non-polar RRAM because the same bias polarity can be used in resistive switching. Many resistive switching for unipolar switching has been reported since early 1960's [93]. NiO, TiO<sub>2</sub>, ZrO, CuO, HfO, Al<sub>2</sub>O<sub>3</sub>, Nb<sub>2</sub>O<sub>5</sub>, CuSiO, MgO<sub>x</sub>, Ga<sub>2</sub>O<sub>3</sub>, CoO, and SiO<sub>x</sub> are representative resistive materials that show thermo-chemical resistive switching [68-87].

Among many kinds of memories, unipolar RRAM device is categorized as the non-volatile memory which is operated by electrical signals [2]. It is basically operated by controlling reversible resistive material, showing two different resistive states such as reset state with high resistance, and set state with low resistance [1-4]. Figure 1.2 shows typical I-V curves for (a) unipolar resistive switching (URS) [1] [3] and (b) bipolar resistive switching (BRS) [1-4]. In unipolar switching, there is no need to change the polarity. The switching direction depends on the power of positive applied voltage. I-V curves enable us to predict both types of resistive cell material and direction of current flow. In general, unipolar type cell structure using diode has smaller cell size than that of bipolar type cell structure.



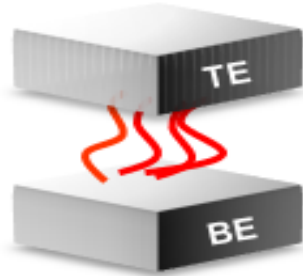
**Fig. 1.2** Typical I-V curves for unipolar (nonpolar) switching (a) and bipolar switching (b).

Figures 1.3 (a) and 1.3 (b) show the models of set and reset states of filamentary conducting paths [2-6], and Figs. 1.3 (c) and 1.3 (d) show the models of set and reset states of n-type interface conducting path [4]. In case of filamentary conduction path model, electroforming process similar to soft breakdown is needed [5]. There have been many researches assuming that it is correlated with the fundamental properties of each resistive cell material. However, it has not been identified which model is more useful for effective resistive switching [7].

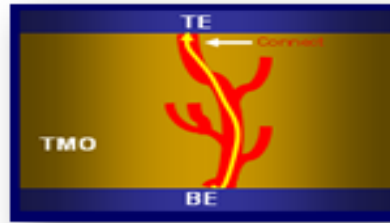
### Filamentary Conduction Path Model

- Electro-forming process is needed.

- TMO (NiO, NbO<sub>2</sub>)



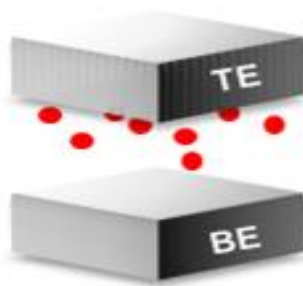
(a)



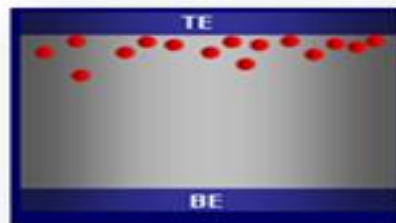
(b)

### Interface Conduction Path Model

- Perovskite / Ferroelectric / TMO (TaO, TiO<sub>2</sub>)



(c)



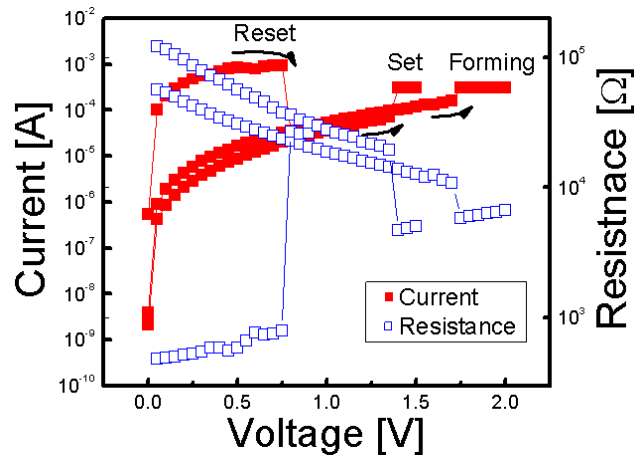
(d)

**Fig. 1.3** Sketches of set (a) and reset (b) states of filamentary path model, and set (c) and reset (d) states of n-type interface conducting path model.

Figure 1.4 shows the typical I-V and R-V curves based on our fabricated NiO material based unipolar RRAM structure [8].  $I_{RESET}$  is  $\sim 1\text{mA}$  at reset voltage



( $V_{RESET}$ ) = 0.6V, and  $V_{SET}$  = 1.2V. The  $R_{ON/OFF}$  ratio is over  $10^3$ . In case of unipolar switching, there is no need to change the polarity. We can reduce the unit cell size in unipolar RRAM cell since unipolar switching RRAM can implement vertical diode type rectifying element which has a smaller access device area than that of larger area of bipolar type. Due to its structural advantages [8-9], we have adopted unipolar type cell with filamentary conduction path model in this thesis [1] to accomplish high-density RRAM application.



**Fig. 1.4** Typical I-V and R-V curves of our fabricated unipolar RRAM with planar MIM structure which show forming, reset, and set states.

In order to demonstrate unipolar switching RRAM, transition metal oxide such as NiO, TiO<sub>2</sub> is used as the resistive switching material because of its unipolar switching characteristics [9-28]. In this thesis, we adopted NiO and TiO<sub>2</sub> with

filamentary conduction path model followed by Joule heating reset process to demonstrate high-density RRAM application.

Table 1.2 summarizes the pros and cons of unipolar switching based RRAM.

As shown in the table below, unipolar RRAM has great potential for high density and low-power RRAM application due to the fast writing time, feasibility of high-density, and compatibility to conventional CMOS process [1-11]. However, poor understandings of physical switching mechanism, unstable unipolar operation, high reset current, and relatively high forming voltage are crucial problems for unipolar RRAM research. Better reliability characteristics and standard fabrication process are also needed. In addition, for high-density application, the feasibility of 3-D stack RRAM is important [12]. Therefore, numerous studies are being conducted to understand resistive switching characteristics in unipolar RRAM, but it is still unclear. Recent study on RRAM using NiO has been reported by Baek et al with possibility of mass production [12]. These materials using TMO are low-cost and can explain characteristics fairly well with CF theory [23-33]. Recent study by Chae, et al. has developed numerical simulation model with which macroscopic TMO RRAM characteristics have been predicted with this simulation [45]. TiO<sub>2</sub> is one of important TMO based RRAM materials that follow filamentary switching model. In case of TiO<sub>2</sub>,

Hwang's group further developed its physical switching mechanism, thermal modeling, and possibilities of practical implications.

Direct observation of CF is also reported recently due to improved understandings of CF's characteristics. Kwon, et al. observed the magnetic phase CFs directly in TiO<sub>2</sub> [89], and Yoo, et al. observed the metallic Ni CF phase in NiO [90]. These research results give us some insights for more understandings of unipolar RRAM even though we still have many issues for industrial application.

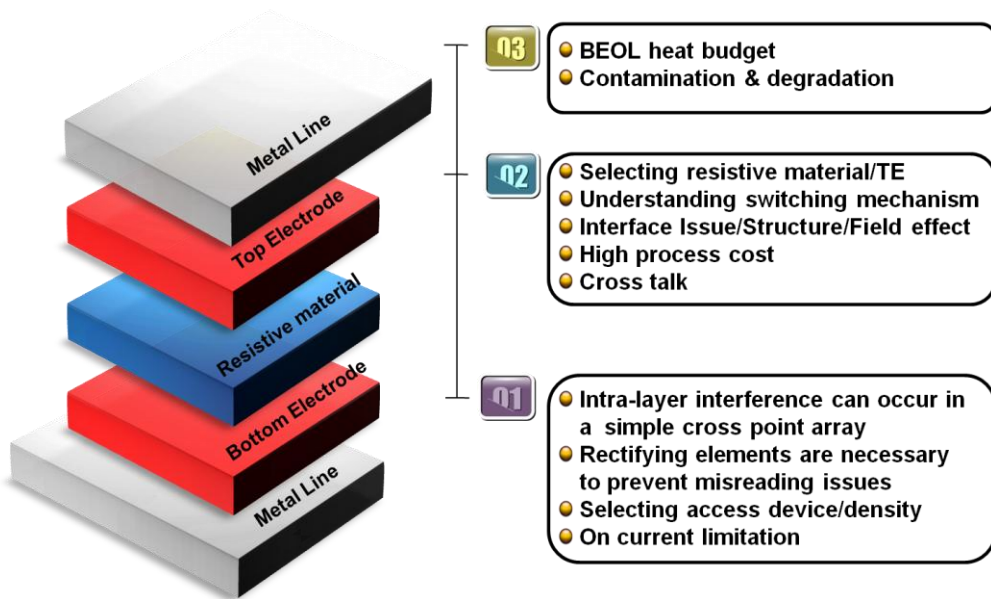
Pros: Potential for high density and low power	Cons: Poor understanding and characteristics
<ul style="list-style-type: none"> <li>▪ Good potential for scaling below 10nm</li> <li>▪ <b>Photolithography &amp; ALD deposition for low switching</b></li> </ul>	<ul style="list-style-type: none"> <li>▪ <b>Poor understanding of physical switching mechanism</b></li> </ul>
<ul style="list-style-type: none"> <li>▪ Fast read and write times switching &lt; 10ns</li> </ul>	<ul style="list-style-type: none"> <li>▪ Robust of filament structure (reliability)</li> </ul>
<ul style="list-style-type: none"> <li>▪ <b>Low write current in <math>\mu</math>A range</b></li> <li>▪ <b>High reset current (1~10mA)</b></li> </ul>	<ul style="list-style-type: none"> <li>▪ Need better endurance and retention</li> </ul>
<ul style="list-style-type: none"> <li>▪ Compatible with CMOS (materials, processing)</li> </ul>	<ul style="list-style-type: none"> <li>▪ <b>Unstable unipolar operation : poor uniformity</b></li> </ul>
<ul style="list-style-type: none"> <li>▪ <b>Possible unipolar operation</b></li> </ul>	<ul style="list-style-type: none"> <li>▪ <b>High reset current (unipolar)</b></li> </ul>
<ul style="list-style-type: none"> <li>▪ <b>Possible crossbar structure with potential for multiple layers</b></li> </ul>	<ul style="list-style-type: none"> <li>▪ <b>Current requires an initial forming process</b></li> </ul>
<ul style="list-style-type: none"> <li>▪ Possible MLC (multi bit/cell storage)</li> </ul>	<ul style="list-style-type: none"> <li>▪ Per bit cost savings of 3-D stack RRAM is questionable</li> </ul>
<ul style="list-style-type: none"> <li>▪ Reasonable ON/OFF ratio</li> </ul>	<ul style="list-style-type: none"> <li>▪ <b>No standard process (material integration, theory etc.)</b></li> </ul>

**Table. 1.2** Pros and cons of unipolar RRAM [74].

Fabrication convenience is also one of important points in this respect. Although RRAM fabrication process is theoretically possible at low-cost, there are still many severe issues to be resolved for effective scaling with mass production.

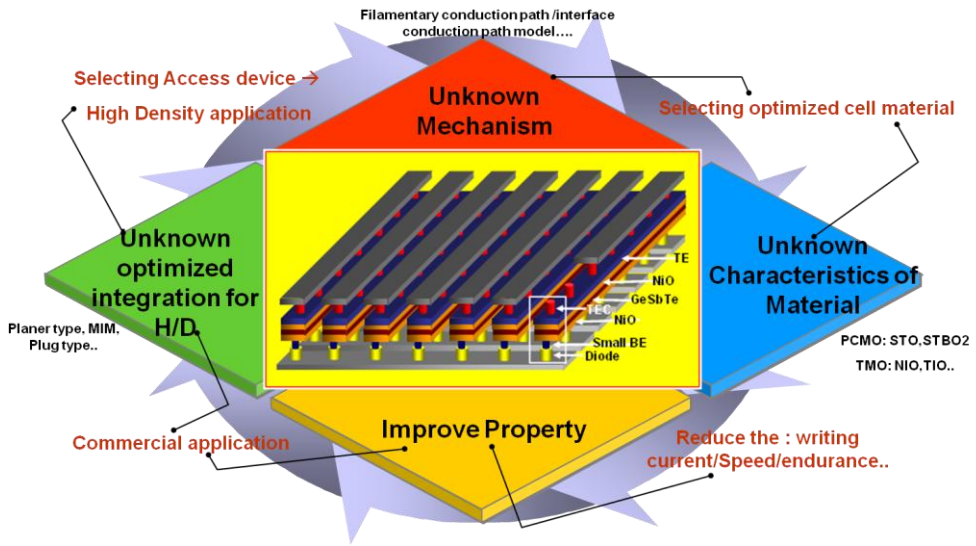
Figure 1.5 shows the current fabrication process issues of RRAM research [2]. Firstl, in front-end-of-line (FEOL) fabrication, interlayer interference can occur in a simple cross point RRAM structure, so rectifying elements are needed to prevent such misleading issues. Then, selecting optimized rectifying device is crucial. As the cell size is decreased, current limitation should be considered. Moreover, it is very difficult to reduce cell area mainly due to the photo-lithography issue [3].

In case of middle-end-of-line (MEOL) fabrication process, selecting optimized resistive material and top electrode are important. Unfortunately, resistive switching mechanism is still ambiguous, the issues such as cell interface, structure optimization, and electric field concentration need to be considered. Cost down should also be achieved for mass production. In addition, as the cell size is decreased, cross talk issue should be considered. Finally, in back-end-of-line (BEOL), we have to consider cell contamination and thermal budget during high temperature process.



**Fig. 1.5** Current process issues of unipolar RRAM fabrication.

Figure 1.6 shows the simple illustration of the current RRAM issues. Despite latent advantages of RRAM, it has still crucial problems as illustrated below. So, it is still very difficult to fix the orientation of unipolar RRAM research. Therefore, we have to focus on the detailed understandings of RRAM switching mechanism and its resistive switching characteristics [22].



**Fig. 1.6** Schematic drawing of important four issues for mass production of RRAM research.

In this context, 4 chapters will be presented in this thesis as follows. The motivation of this study is described in Chapter 2. Basic resistive switching characteristics of conventional unipolar RRAM and the results regarding the simulation and experimental study of various conventional cell conditions are also presented in Chapter 2. The results regarding the fabrication process and experimental study of scaling effects of crown shape structure will be presented as a feasibility study of area effect on CF modulation in Chapter 3, and the resistive switching characteristics of highly-scaled hole contact structure are presented to confirm it in Chapter 4. In the end, the conclusion is discussed in Chapter 5.

# Chapter 2

## Unipolar Resistive Switching

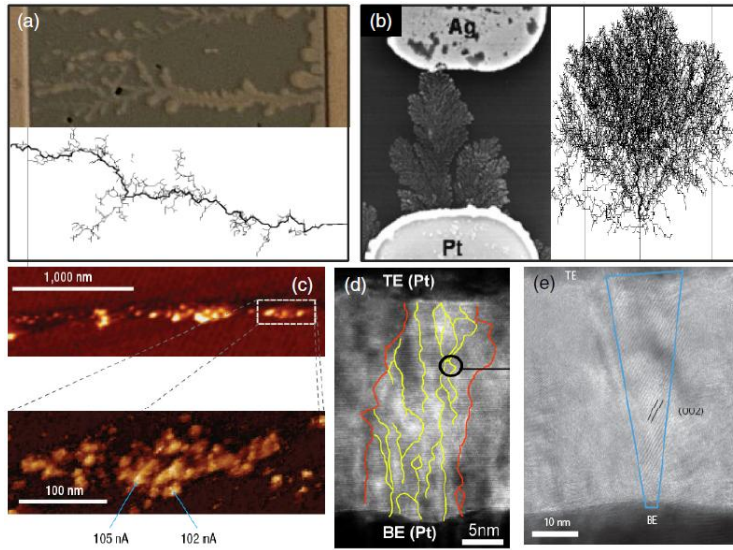
### 2.1 Conductive Filament (CF) in Initial Resistive cell States

In order for unipolar RRAM to have low power with uniform resistive switching, it is necessary to accomplish very stable CF dimension associated with resistive switching. Recently, many reports have been published that CF is one of important resistive switching sources in unipolar RRAM due to thermo-chemical model [42-45]. In the early stages of RRAM research, indirect evidence of CF was reported by using conductive atomic force microscopy (CAFM) method [93]. However, direct observation of localized CF in resistive cell has been reported in recent years due to the improved measurement technique. Figure 2.1 shows the CF observation data in various resistive switching materials. CFs in (a) ~ (e) in Fig. 2.1 indicate the Ag CF in Ag/Ag-Ge-Se/NiNi (a), Ag CF in Ag/H<sub>2</sub>O/Pt (b), dislocation shape CF in single crystal SrTiO<sub>3</sub> (c), metallic Ni CF in Pt/NiO/Pt (d),

CF with magneli phase in Pt/TiO<sub>2</sub>/pt (e), respectively [93], [98], [101] - [104], and [49].

Even though their switching condition is quite different, their localized switching behaviors are similar to each other. Among them, NiO and TiO<sub>2</sub> resistive switching material are one of important candidates for unipolar RRAM though they have different CF shapes. The different CF shapes originate from different major injection carrier mechanism, electron affinity, and sub-oxide phase stability [83-100]. The most significant thing is that CF is an obvious meaningful resistive switching source in unipolar RRAM following thermo-chemical resistive switching model. Even though they have different CF shapes and dimensions, controlling CF shape and area is a useful way to improve resistive switching characteristics.





**Fig. 2.1** Various CF observation with different switching material reproduced with permission from [93], [98], [101] - [104], and [49].

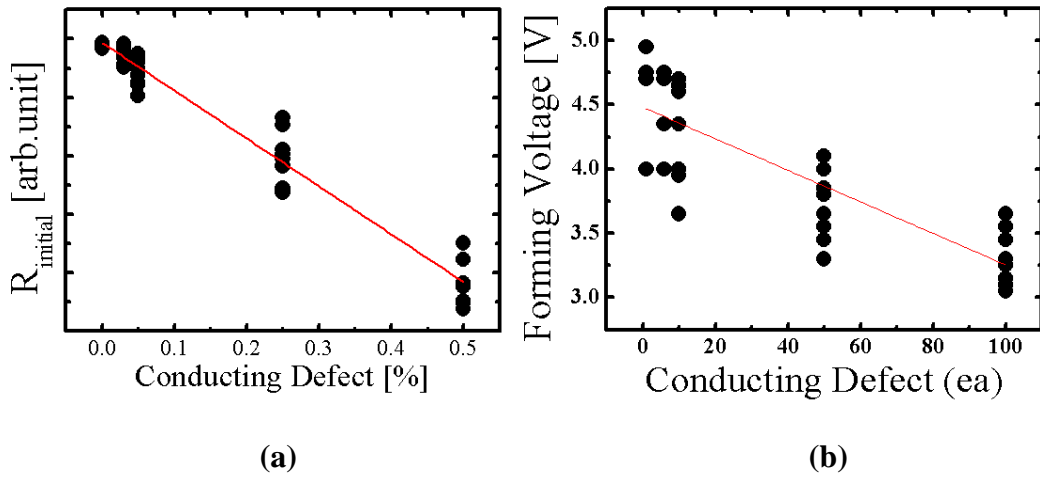
In this context, by controlling the amount of CF branch at resistive cell material/TE interface, irregular switching can also be decreased significantly, and this is an important factor to determine  $I_{RESET}$  level. Because the CF is located in a very localized area, the reduction of switching area to the area of CF dimension can be one of the effective solutions to control the CF.

Therefore, in this section, resistive switching parameter relationships are considered in the first place between CF and resistive switching characteristics [23] by random circuit breaker (RCB) simulation model, which is a dynamic percolation model for unipolar resistive switching followed by randomized reset

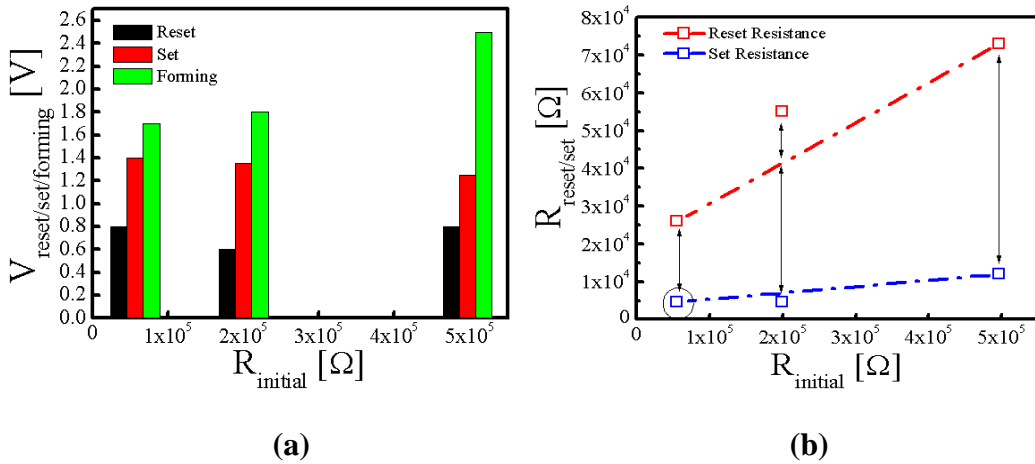
process.

Figure 2.2 shows the effect of conducting defect depending on initial cell resistance (a) and forming voltage ( $V_{FORMING}$ ) (b) on resistive switching. Conducting defect can be defined as partial length unit of CF in RCB model. It can be defined as CF source in real resistive material such as oxygen vacancy and metallic particle. This simulation model for unipolar switching has been proposed by Chae, et al. based on random circuit breaker network. This model easily explains the resistive switching behavior of unipolar RRAM with a relatively simple mechanism [4].

This indicates that there is an inverse relationship between the number of conducting defect and the  $R_{INITIAL}$  and  $V_{FORMING}$ . Figure 2.3 demonstrates the relationships between  $R_{INITIAL}$  and  $V_{RESET}$ ,  $V_{SET}$  and  $V_{FORMING}$  (a), and  $R_{RESET}$ ,  $R_{SET}$  and  $R_{FORMING}$  (b). In Fig. 2.3 (a), it is shown that  $V_{FORMING}$  increases if  $R_{INITIAL}$  is high, indicating that the initial voltage needs to be reduced in order to lower the operating voltage. However, if  $R_{INITIAL}$  is sufficiently low, the sensing margin is also reduced as shown in Fig. 2.3 (b). This suggests that determination of optimal process condition based on correct relationships between parameters is essential to evaluate RRAM cell which shows superb sensing margin.



**Fig. 2.2** Relationships between CF and initial cell resistance (a) and  $V_{FORMING}$  (b).

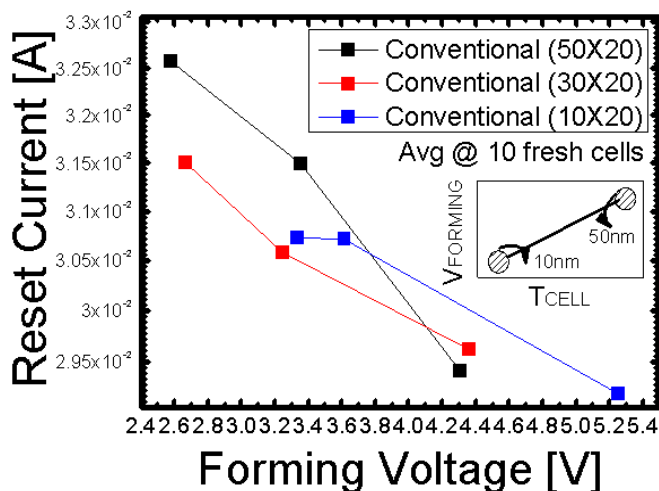


**Fig. 2.3**  $R_{INITIAL}$  as a function of reset/set/forming voltages (a) and reset/set resistances (b).

## 2.2 CF Control at the Switching Interface of a Single Layer Cell

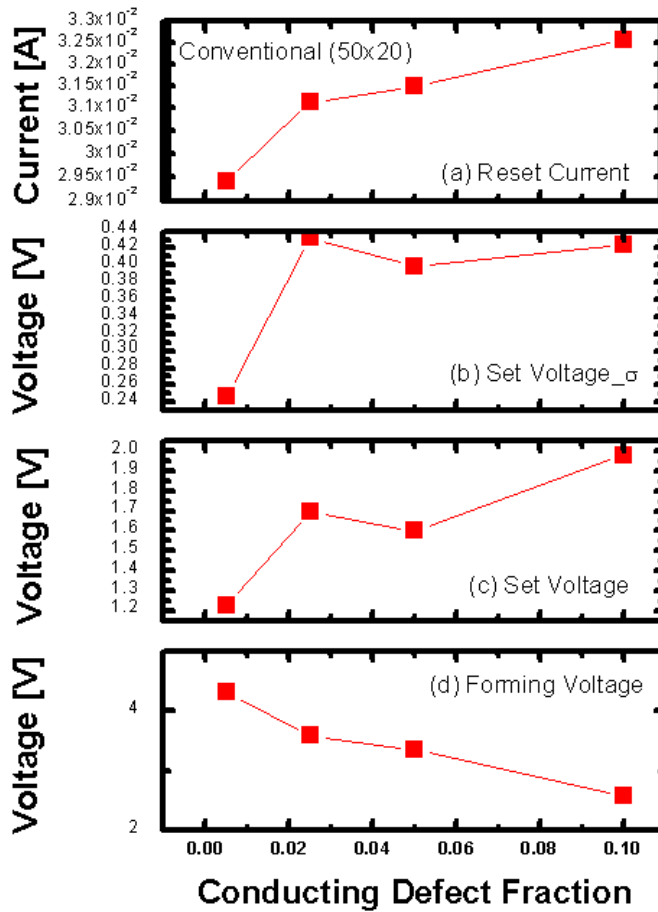
$I_{RESET}$  as a function of  $V_{FORMING}$  for different cell sizes is investigated by using RCB simulation model, which is a dynamic percolation simulation model for unipolar resistive switching research. [4]. Although  $I_{RESET}$  reduction mechanism has been reported by many researchers, it is still controversial [3-10]. Previous researches have shown that there is no relationship between  $I_{RESET}$  reduction and resistive cell area. This result comes from the relatively large cell size of over  $\mu\text{m}$  level, which causes the smaller CF area than the total, resulting in insignificant change in the set resistance. However, if resistive cell area becomes smaller (sub-nm level), the area of CF change becomes relatively larger than that of total cell area, making it possible for the difference between cell area and set resistance to be large. Particularly in RCB simulation model, the change in CF area becomes relatively larger than the change in total cell area since the size of this simulation is extremely small with the dimension of 50 by 20. Therefore, the effect of CF change can be conspicuous in sub-nm cell size. As shown in Fig. 2.4, the change in  $I_{RESET}$  for different cell contact areas can be identified. But there is a trade-off between  $I_{RESET}$  and  $V_{FORMING}$  in single layer cell structure as shown in Fig.

2.4. It gives some clues for possibility of  $I_{RESET}$  reduction with area scaling in sub-nm region.



**Fig. 2.4**  $I_{RESET}$  as a function of  $V_{FORMING}$  for single layer cell structure with various thicknesses by using RCB model.

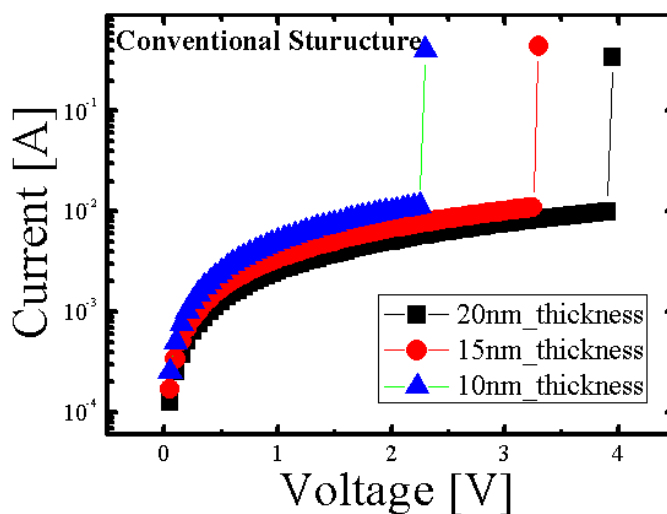
Figure 2.5 shows important resistive switching characteristics of single-layer cell structure for different conducting defect ratio by RCB simulation model. Here in Fig. 2.5, it is very difficult to reduce both  $I_{RESET}$  and  $V_{FORMING}$  due to different needs of conducting defect condition in single-layer cell structure. However, it gives some clues that one of important factor to reduce  $I_{RESET}$  is maintaining high  $R_{INITIAL}$  cell condition, even though it gives high  $V_{FORMING}$  results in high forming power.



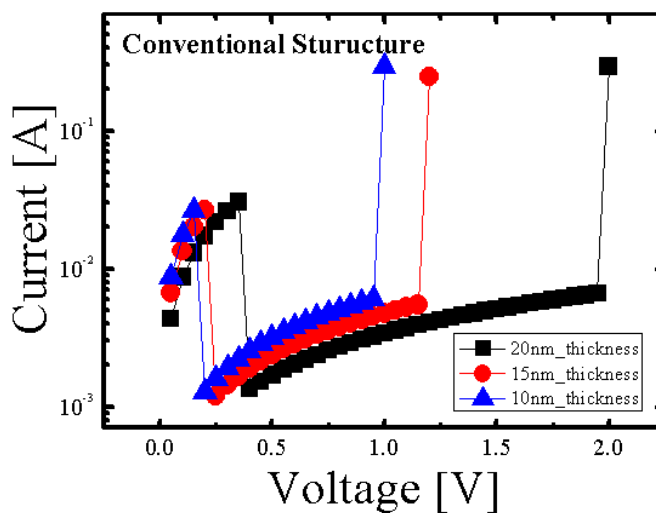
**Fig. 2.5** Resistive switching characteristics comparisons with different defect conditions in conventional cell in RCB model.

Therefore, controlling the  $R_{INITIAL}$  level is also a very important factor in determining the  $I_{RESET}$ . This  $R_{INITIAL}$  is related to the cell dimension, so the cell dimension must also be considered in controlling the resistive switching characteristics.

Figures 2.6 and 2.7 show the I-V curves of the forming, reset, and set characteristics as functions of the cell thickness obtained from the RCB model. As the cell thickness decreases from 20 to 10 nm in fig. 2.8, the  $V_{FORMING}$  also decreases from 4.2 to 2.4 V. Figure 2.7 shows that the  $I_{RESET}$  was over 10 mA. The on/off resistance ratio in the RCB simulation was larger than 1.5 in magnitude. This indicates that the cell thickness is strongly related to the  $V_{FORMING}$ . It was revealed that the thickness dependence is caused by the reduction in the total length of CF in a resistive cell. As shown in Fig. 2.7, however, there was no noticeable decrease in the  $I_{RESET}$  level. This signifies that the decrease in the cell thickness has insignificant impact on the decrease in the  $I_{RESET}$ .



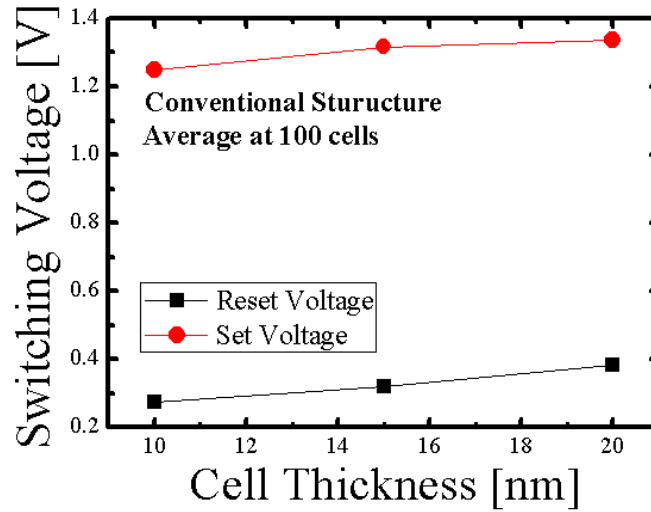
**Fig. 2.6** I-V curves of the forming characteristics with various cell thicknesses.



**Fig. 2.7** I-V curves of the reset and set characteristics with various cell thicknesses.

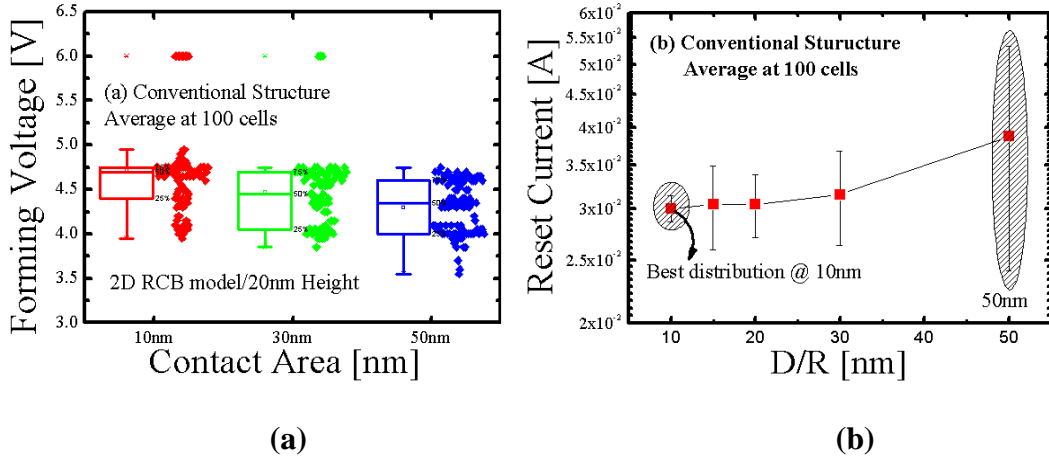
Nonetheless, it was identified that the cell thickness has little or no effect on the decrease in the set and reset switching voltages. Figure 2.8 shows the reset/set switching voltages for the 20nm, 15nm, and 10nm resistive cell thicknesses. There was a minimal change in the set and reset voltages regardless of the cell thickness. It was also verified that even with the decrease in the cell thickness from 20 to 10nm, the average value of the  $V_{SET}$  and the  $V_{RESET}$  decreased by 0.1 V each.





**Fig. 2.8** Switching voltages for the 20nm, 15nm, and 10nm resistive cell thicknesses.

Figure 2.9 shows the (a)  $V_{FORMING}$  and (b)  $I_{RESET}$  distributions as functions of the contact area for 50nm, 30nm, and 10nm in conventional structures. The dispersion is only weakly dependent on the contact area. Even when there is a large decrease in the contact area from 50nm to 10nm, there is a very small increase in the  $V_{FORMING}$ . This indicates that the forming process occurs in a limited area in RCB model.

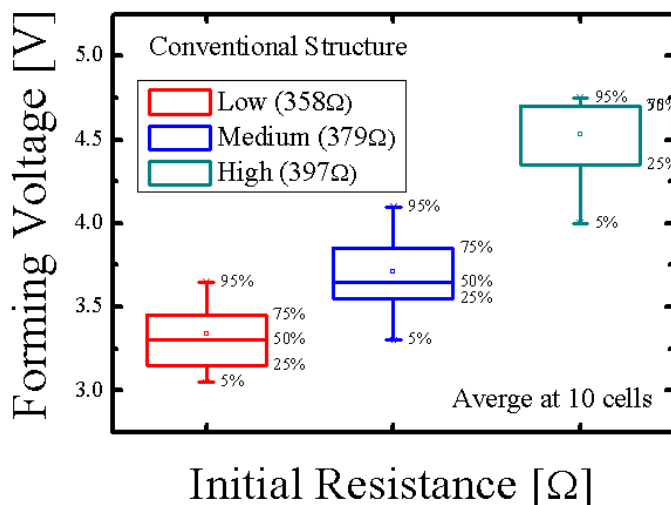


**Fig. 2.9** (a)  $V_{FORMING}$  and (b)  $I_{RESET}$  distributions as functions of the contact area for the 50nm, 30nm, and 10nm conventional structures. The dispersion was only weakly dependent on the contact area.

It was also verified that the initial cell characteristics critically affect the  $V_{FORMING}$ . Figure 2.10 shows the results of the statistical analysis of the  $V_{FORMING}$  distribution as a function of the  $R_{INITIAL}$  for a conventional structure. The dispersion is dependent on the  $R_{INITIAL}$ . As seen in Fig. 2.10, when the  $R_{INITIAL}$  decreases, the  $V_{FORMING}$  also decreases. This indicates that the driving force needed to form the initial CF is dependent on the resistance of the initial cell.

Such phenomenon expedites the increase in  $R_{INITIAL}$  as the cell area is decreased. Therefore, it needs to be considered even more in a small cell area. Considering the resistive switching, relationship with the  $V_{FORMING}$  and  $R_{INITIAL}$  needs to be constructed for effective rupturing.

Therefore, it is critical to select an optimum cell condition because a lower  $R_{INITIAL}$  may not only be helpful in lowering the  $V_{FORMING}$  but may also increase the  $I_{RESET}$  [10]. In short, there is a trade-off between the  $V_{FORMING}$  and the  $I_{RESET}$  in the same cell dimension. Thus, some modifications such as in the structural approach for finding an optimal cell condition or intrinsic cell property improvement are still needed to improve both the forming and reset characteristics.

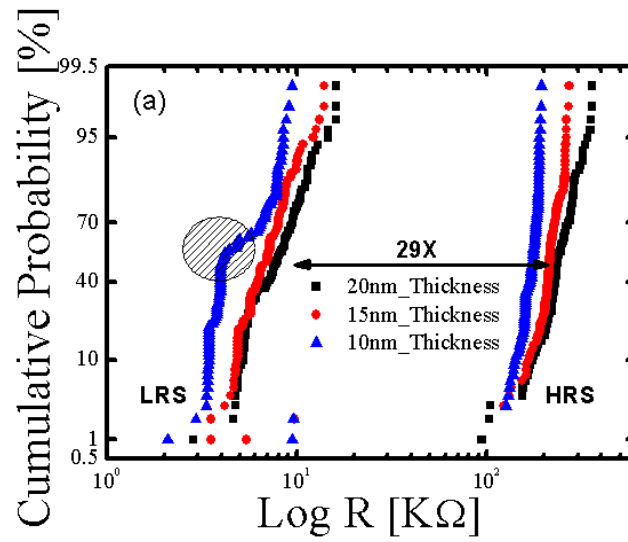


**Fig. 2.10**  $V_{FORMING}$  distribution curve as a function of the  $R_{INITIAL}$  for a conventional structure.

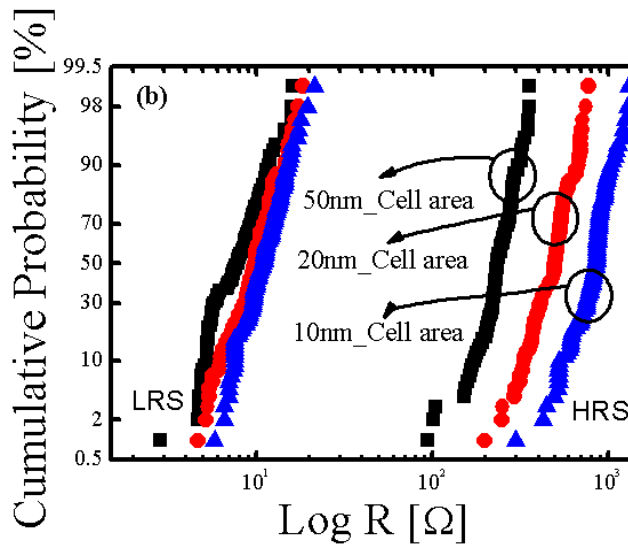
Figure 2.11 shows the resistance distributions of the reset and set states for various (a) cell thicknesses and (b) contact areas of 100 conventional cells in RCB model. The unit of nm is not real data due to this simulation model can not give an

actual result. This simulation model only expects its resistive switching tendency. However, this model can explain random CF rupture and disconnection following the unipolar based filamentary conduction model. (1nm in this simulation means 1 conducting defect in the resistive matrix.)

The on/off resistance ratio either increases or remains the same even though the cell thickness and the contact area decrease. This can be considered an important result that verifies the viability of RRAM as a high-density non-volatile memory because it can maintain excellent resistive switching characteristics even when its cell size is scaled down.



(a)

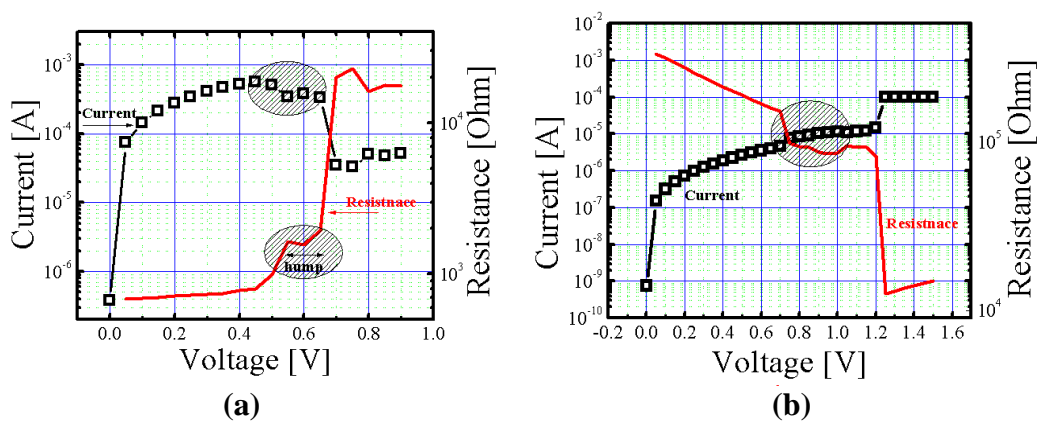


(b)

**Fig. 2.11** Switching resistance distributions for reset and set states of 100 conventional cells with different (a) cell thicknesses and (b) contact areas in RCB model.

It was also confirmed that as the cell thickness and the contact area decrease, the on/off resistance ratio increases in the sub-nm region using the RCB model.

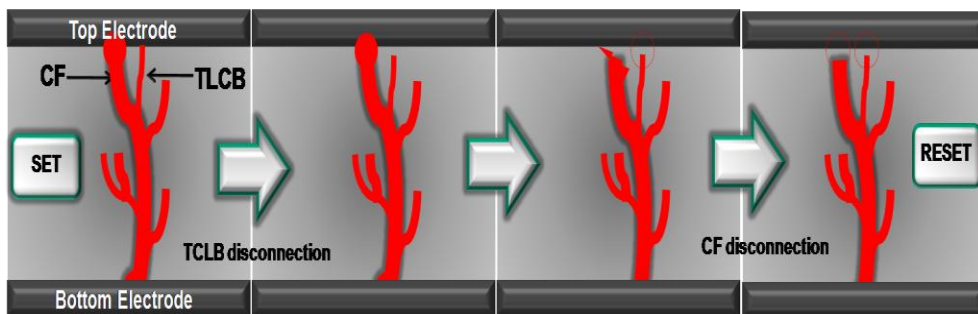
As we mentioned before, we adopted unipolar RRAM to filamentary conduction path model [1] to implement high-density memory. However, in Figs. 2.12 (a) and 2.12 (b), irregular reset (a) and set (b) switching behaviors occurred intermittently with conventional structure due to undesired CF interactions [8], especially at their initial state, and such changes can give an opposite effect on the cell distribution.



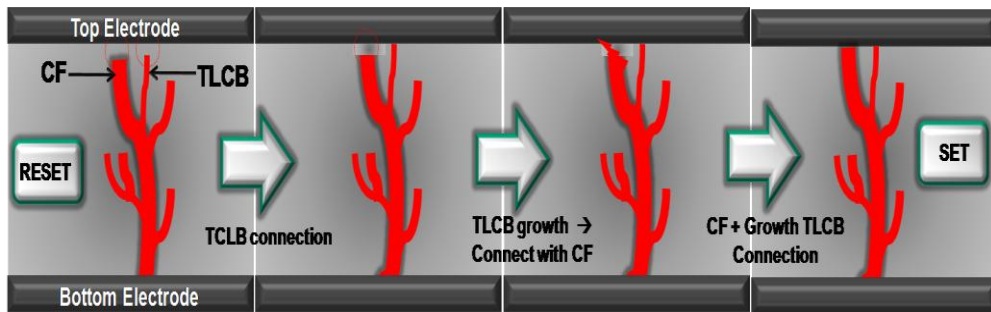
**Fig. 2.12** I-V curves showing irregular reset (a) and set (b) switching behaviors of our planar type cell structure.

In order to explain these initial irregular switching behaviors in more detail,

possible cases are investigated using CF shape and movement at the cell interface. Figure 2.13 illustrates that electrons can be transported to the top electrode by the formation of the initial CF when a bias of positive/negative values are applied close to the negative differential resistance (NDR) region. Such a pristine CF formed in the manufacturing process creates tiny lateral conducting branches different from initially formed CF before it breaks (reset) and connects (set) by the applied voltage. As seen in Figs. 2.13 (a) and 2.13 (b), tiny lateral conducting branches repeat connection and disconnection at the cell interface, which in turn affects initial switching, and eventually leads to switching behavior. Here we refer this to “filament branch effect” (FBE) [35]. If initial forming process is defective, such irregular switching fluctuation is observed more frequently. This clearly shows that there is a correlation between irregular switching characteristics and initial resistive cell condition, especially at the forming state.



(a)



(b)

**Fig. 2.13** Schematic drawings of filament branch effect (FBE). Possible scenario of irregular reset (a) and set (b) transition behaviors is explained above.

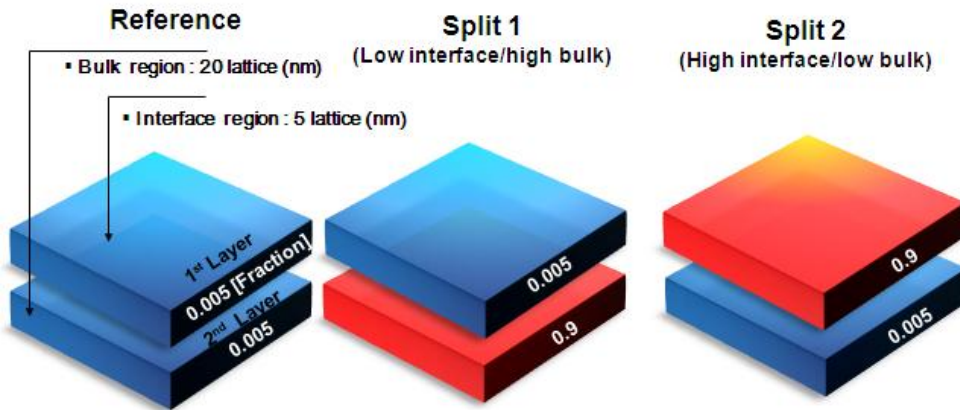


## 2.3. CF Control in Switching Interface in Bi-layer Cell

### 2.3.1 Bi-layer cell with conductive defect effect

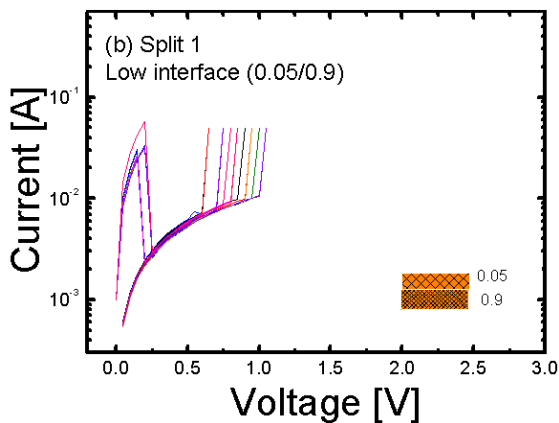
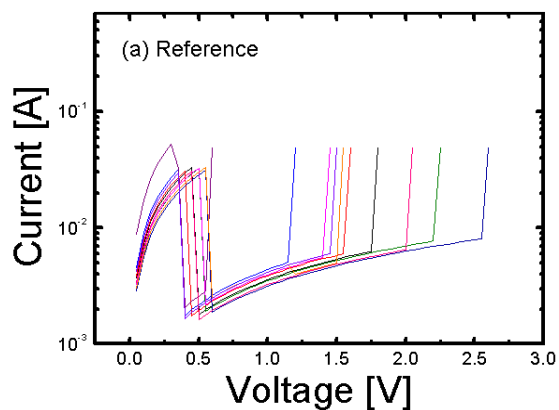
In order to understand the unipolar resistive switching and CF relationship, further research on cell interface where resistive switching occurs is needed [8-9].

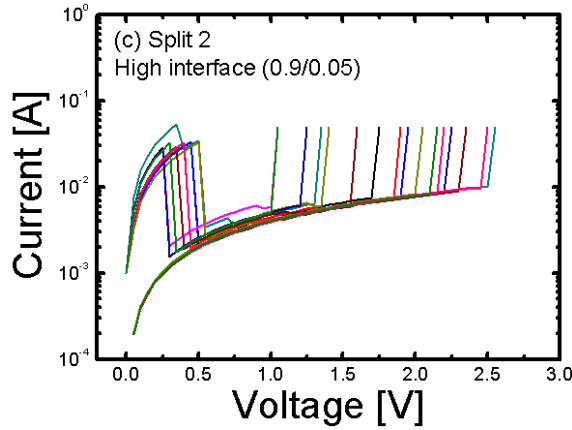
Therefore, interface effects are investigated for bi-layer cell structure by using RCB simulation model. We have prepared three different bi-layer cell structures as shown in Fig. 2.14 [105].



**Fig. 2.14** Cell preparation for switching comparisons with different cell conditions.

The first is a reference cell having uniform conducting defect ratio, the second is split1 cell having low conducting defect ratio (interface) with high conducting defect ratio (bulk), and the third is split 2 cell having high conducting defect ratio (interface) with low conducting defect ratio (bulk).



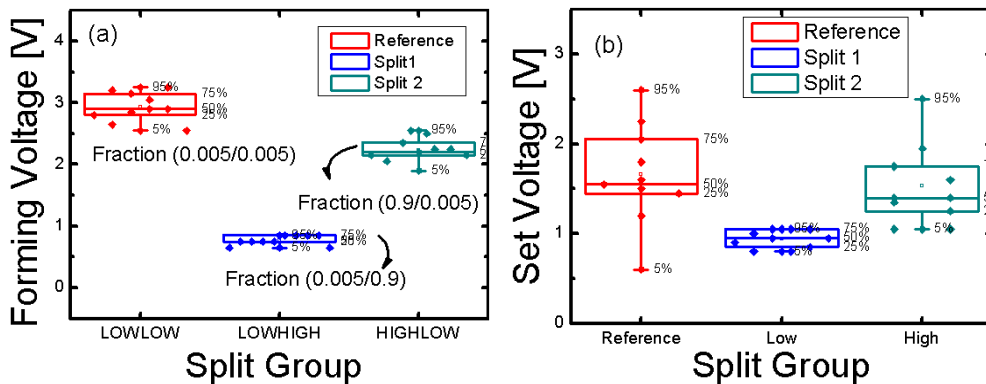


**Fig. 2.15** I-V curves of reference (a) and bi-layer cell with different defect conditions ((b) and (c)).

Figure 2.15 shows the simulated I-V characteristics of (a) reference cell, (b) low interface cell, and (c) high interface cell. Bi-layer cells show better resistive switching characteristics compared to that of reference cell. But in case of the split 2 cell having high conducting defect ratio (interface) with low conducting defect ratio (bulk), it shows worse  $V_{SET}$  distribution compared to those other split cells in this I-V curve. To show this effect, statistical analyses are performed.

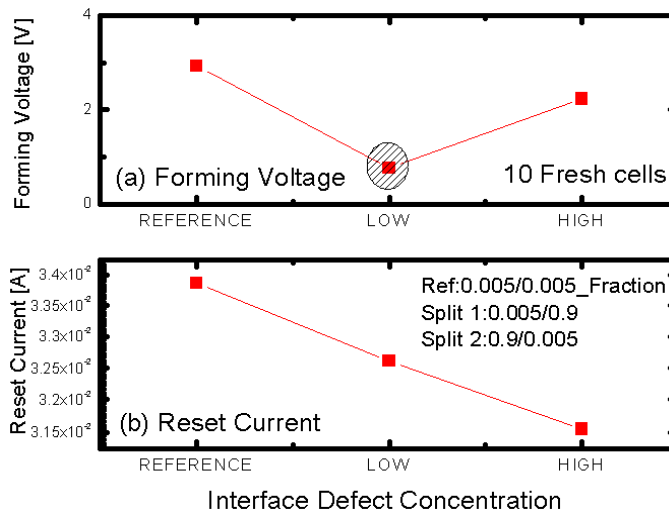
Figure 2.16 shows the statistical analysis of forming (a) and set (b) characteristics of various cell structures. Split bi-layer cells show better  $V_{FORMING}$  and  $V_{SET}$  characteristics. Especially in the case of split 1 cell, it shows excellent  $V_{FORMING}$  and  $V_{SET}$  characteristics. Moreover, it shows the best distribution characteristics compared to those of other different split cells. When using

bi-layer cell, CF is effectively formed at the switching interface. Especially, it has been verified that forming and set characteristics are improved more effectively than in the case of split 1 because conducting defect ratio in bulk region which forms initial filament is high, making it more advantageous for filament path to be formed. Split 2 also shows better switching characteristics because overall conducting defect ratio is higher than reference. However, it contributes relatively little to forming initial CF, because it is limited \to switching interface. Also in the case of split 1, relatively less conducting defects at interface make it possible for easier CF rupturing. Therefore, it is possible to predict better set characteristics as well. So determining optimal conducting defect ratio is very important to improve the resistive switching characteristics.



**Fig. 2.16** Statistical analysis of  $V_{FORMING}$  (a) and  $V_{SET}$  (b) characteristics with different cell conditions.

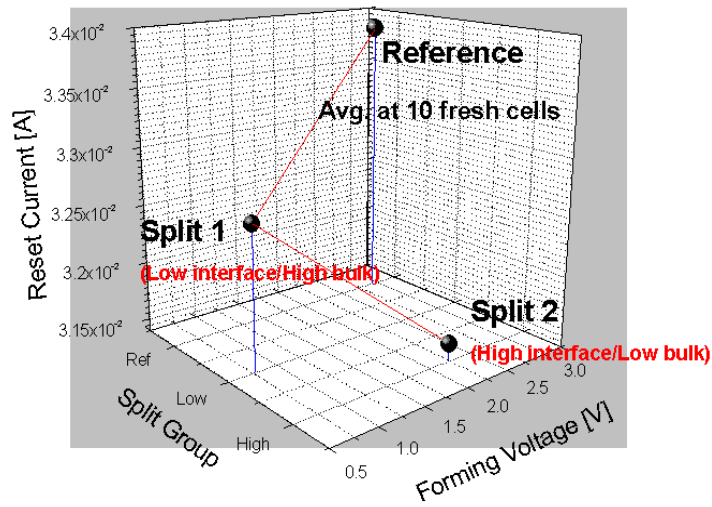
Figure 2.17 shows the  $V_{FORMING}$  and  $I_{RESET}$  characteristics as a function of various split groups. Compared with the single layer cell, both bi-layer cells show better  $V_{FORMING}$  and  $I_{RESET}$  characteristics. Surprisingly in both split bi-layer cells, they show better  $V_{FORMING}$  and  $I_{RESET}$  characteristics which are different results from reference cell. It means that an optimal process condition plays an important role in resistive switching, and bi-layer with different conducting defect ratio can be the solution for resistive switching improvement.



**Fig. 2.17**  $V_{FORMING\_μ}$  and  $I_{RESET\_μ}$  with different cell conditions.

Figure 2.18 summarizes the  $I_{RESET}$  and  $V_{FORMING}$  as a function of different split group. As shown in this figure, split bi-layer cells show better resistive switching

characteristics compared with the reference cell due to better CF controllability. However, improvements of both  $I_{RESET}$  and forming characteristics are a little bit different from conducting defect conditions in each bi-layer cell. So, optimal process condition with deep understanding of cell configuration is also needed.



**Fig. 2.18** Summary of resistive switching characteristics of 3 different split groups.

### **2.3.2 Bi-layer cell with thickness effect**

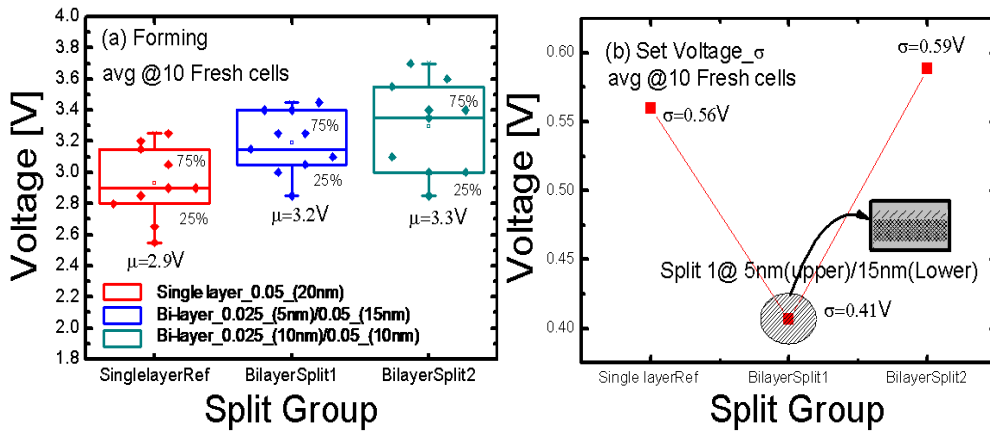
In bi-layer structure, resistive material is composed of two different parts. Even though we can use the same kind of bi-layers, layer thickness and conductive defect condition are different. Lower layer (2<sup>nd</sup> resistive layer) is acting as a forming assistance layer for low-power consumption. In unipolar RRAM switching, initial forming process is crucial since it determines the power consumption and further resistive switching uniformity. Upper layer (1<sup>st</sup> resistive layer) is used for controlling reset/set switching. Especially because resistive switching occurs at cell interface, interface engineering is very critical for improving resistive switching uniformity. So we adopted double resistive layers for satisfying both forming and reset/set switching. Charged particle which is a source of CF path such as oxygen vacancy and metallic ion in resistive cell can be defined as conductive defect. Conductive defect fraction is varied from 0.05 (lower layer) to 0.025 (upper layer), respectively. Conductive defect fraction of reference cell is 0.05. Each layer rules and their actions for bi-layered RRAM cell structure are summarized in Table 2.1.

Bi layered cell	Split/Required Conditions	Action	Materials
TE	▪High conductive/No interaction with Vo	▪Upper electrode	▪Ir/Pt/Ru
Upper Layer (1 <sup>ST</sup> layer)	▪ Conductive defect Fraction(circuit breaker)= 0.025 ▪ 5nm/10nm15nm thickness split (High R region)	▪Reset/Set Control	▪ NiO
Lower Layer (2 <sup>ND</sup> layer)	▪Conductive defect Fraction(circuit breaker)= 0.05 ▪ 15nm/10nm5nm thickness split (Low R region)	▪Forming Control	▪ NiO
BE	▪High conductive/No interaction with Vo	▪Lower electrode	▪Ir/Pt/Ru

**Table. 2.1** Cell layer rules and actions for bi-layered RRAM cell.

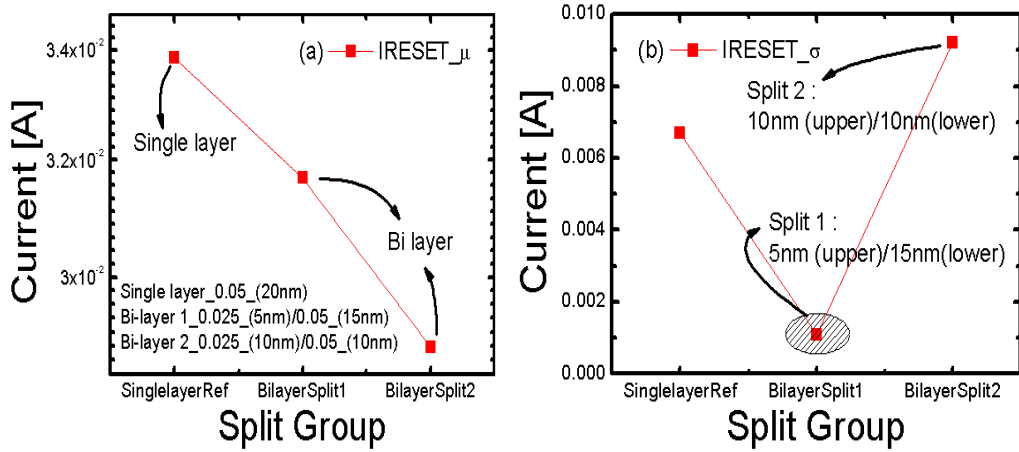
Figure 2.19 shows the statistical analysis of  $V_{FORMING}$  (a) and  $V_{SET}$  (b) characteristics with various cell conditions with bi-layer interface. Lower  $V_{FORMING}$  is addressed in a single layered cell due to its larger amount of conductive defects, but in the case of 5nm thickness of upper layer (split 1) cell, the mean value of forming voltage ( $V_{FORMING\_μ}$ ) difference is only 0.26V. Then again, the standard deviation of forming voltage ( $V_{FORMING\_σ}$ ) is better than that of single layered cell. As shown in Fig. 2.19 (b), the standard deviation of set voltage ( $V_{SET\_σ}$ ) is also drastically improved in case of split 1 cell. Also, in case of both split groups,  $I_{RESET}$  is decreased compared to single layered cell. It means that set switching controllability is enhanced because controlling the localized CF becomes easier as the amount of conductive defects switching interface is lowered due to optimization of total amount of CF associate with set process.





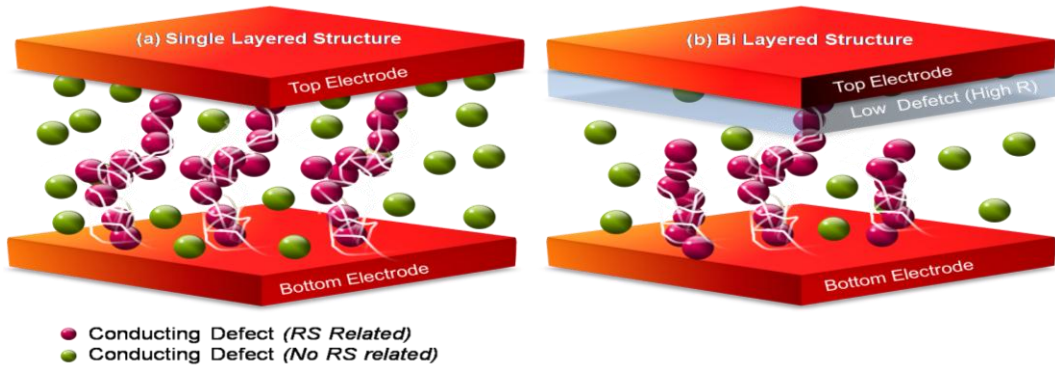
**Fig. 2.19** Statistical analysis of  $V_{FORMING}$  (a) and  $V_{SET}$  (b) characteristics with different layer thickness in bi-layer cell.

Figure 2.20 shows the standard deviation of reset current ( $I_{RESET\_σ}$ ) (a) and mean of reset current ( $I_{RESET\_μ}$ ) (b) with different cell conditions. Interestingly, in the case of split 1, it shows excellent distribution property. It reveals that lower conductive defect amount at cell interface gives an impact on CF rupturing. During the set process, thin and localized CF can be formed due to lower conductive defects. And it can also be easily ruptured by relatively low-power during reset process. It results in lower  $I_{RESET}$  with excellent uniformity.



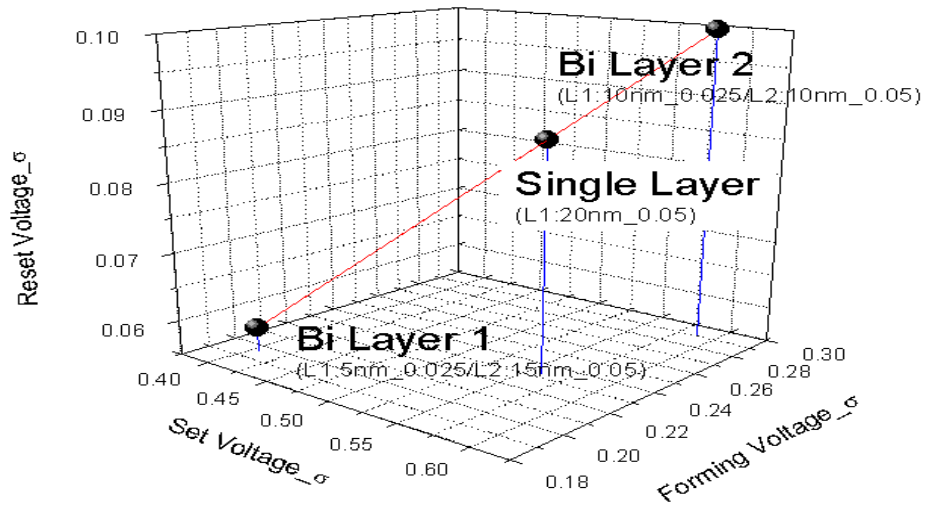
**Fig. 2.20** Mean value of reset current ( $I_{RESET-\mu}$ ) (a) and Standard deviation of reset current ( $I_{RESET-\sigma}$ ) (b) with different layer thickness in bi-layer cell.

Figure 2.21 shows the schematic drawings of possible scenario of CF movement at conventional single layered RRAM structure (a) and bi-layered RRAM cell structure (b). Distribution is improved due to reduction of CF associated with resistive switching by optimizing the thickness of conductive defect layer.



**Fig. 2.21** Schematic drawings of possible scenario of CF movement at conventional single layered RRAM structure (a) and bi-layered RRAM cell structure (b). Distribution is improved due to reduction of CF associated with resistive switching.

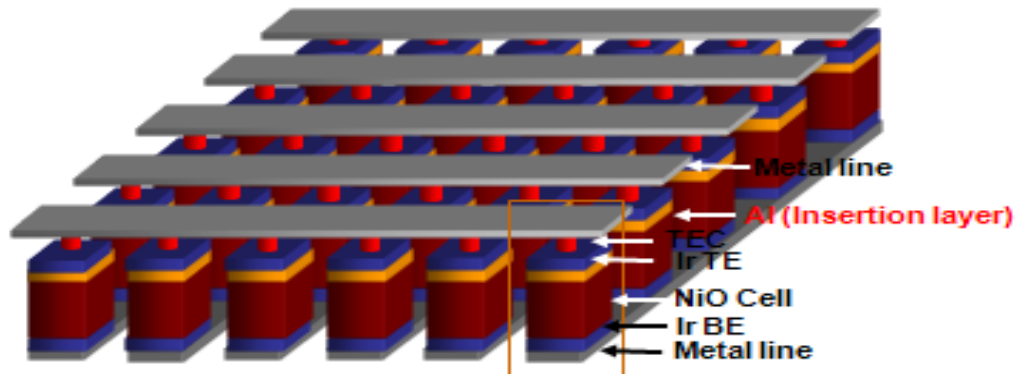
The uniformity of resistive switching parameters such as  $V_{FORMING}$ ,  $V_{SET}$  and  $I_{RESET}$  with various conditions of bi-layer structures are summarized as shown in Fig. 2.22. Standard deviations of important resistive switching parameters such as  $V_{FORMING}$ ,  $I_{RESET}$  and  $V_{SET}$  characteristics are all improved compared to single layered cell structure. Especially, split 1 cell having lower conductive defect amount by lower cell thickness shows best switching characteristics. It means that optimal upper layer thickness exists, thus finding an optimal integration has an important role in low-power RRAM application.



**Fig. 2.22** Uniformity comparisons with different bi-layer cells.

### 2.3.3 Experimental results: Al inserted bi-layer structure

In order to clarify the effect of bi-layer cell structure, Ir/AlO<sub>x</sub>/NiO/Ir bi-layer RRAM cell was fabricated. Figure 2.23 illustrates the proposed AlO<sub>x</sub> layer inserted bi-layer RRAM cell structure. This bi-layer cell is built in between two intersecting metal lines, which point to selected one from resistive cell materials, and from reading/writing data alternatively. By using additional AlO<sub>x</sub> layer at switching interface, joule-heating effect enhancement occurs with power of  $I^2RT$  during the reset state leading to uniform resistive switching and  $I_{RESET}$  reduction. This interface-engineered structure results in increased number of oxygen vacancies at cell interface, making metallic Ni movements and thermally activated diffusion process easier. Moreover, because of lower electro-negativity of Al than that of Ni, it is expected that filament disconnection becomes easier due to interfacial AlO<sub>x</sub> formation at reset state.

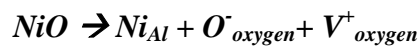


**Fig. 2.23** Schematic drawing of Al inserted cell structure.

Figure 2.24 shows the typical I-V curves for reset process in NiO (single layer) and AlO<sub>x</sub>/NiO (bi-layer) devices.

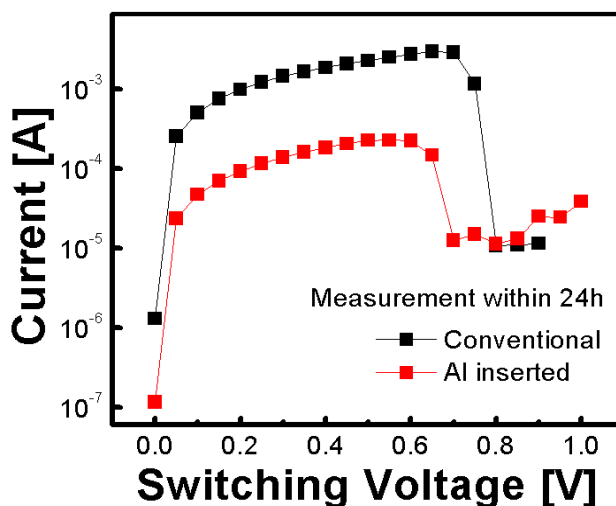
When additional AlO<sub>x</sub> layer is inserted in the Ir/NiO interface,  $I_{RESET}$  is decreased compared with the single layer cell, showing that AlO<sub>x</sub> layer is effective in  $I_{RESET}$  reduction, acting as buffer layer. The following explains the mechanism in which inserted Al layer contributes to  $I_{RESET}$  reduction.

We consider that Al insertion into NiO cell leads to the formation of defects at interface creating oxygen vacancies formed by Al atom [3].



Formation of metallic Ni and oxygen vacancy as a source of CF are generated

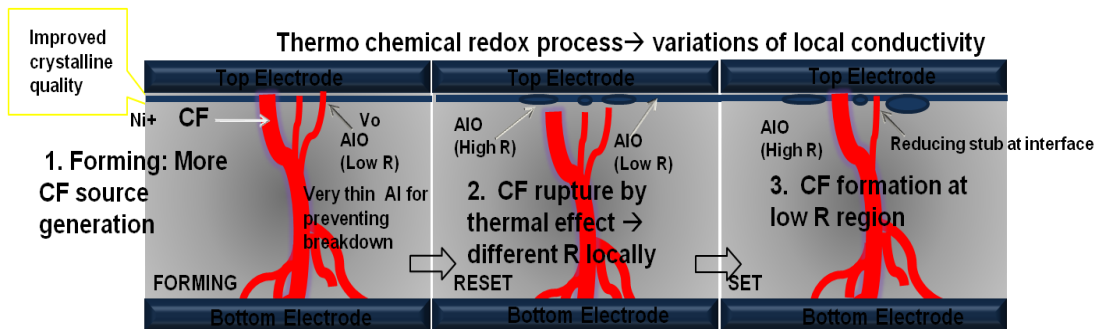
which results in the easy switching. And because of Al insertion, atomic diffusion rate and thermally activated diffusion process are enhanced during the reset process. Al atoms prefer oxidation due to a lower electro-negativity and higher binding energy with oxygen during the reset process.



**Fig. 2.24** Typical I-V curves for reset process in NiO (single layer) and AlO<sub>x</sub>/NiO (bi-layer) devices.

Such formed AlO<sub>x</sub> assists localized switching as shown in Fig. 2.25, improving irregular switching behavior and reducing  $I_{RESET}$ . Total area of CF associated with the reset state can also be reduced by formation of AlO<sub>x</sub> associated with CF localization at NiO/TE interface, resulting in  $I_{RESET}$  reduction. Then, optimal AlO<sub>x</sub> thickness and optimal initial cell condition are crucial for low  $I_{RESET}$ . As shown in

Fig. 2.24,  $I_{RESET}$  decreases when optimal cell oxidation and optimal inserted Al layer is applied. In Fig. 2.24,  $I_{RESET}$  efficiently decreases from 1.6mA at  $V_{RESET} = 0.8V$  to 0.15mA at  $V_{RESET} = 0.6V$  by more than one order compared to that of reference cell, respectively. Resistive switching is clearly observed with resistance change of 1.5 orders of magnitude. Set current is slightly decreased compared with our previous reference cell.  $V_{SET}$  difference is about 0.3V but in case of oxygen contents optimization, the difference is small. In other words  $R_{INITIAL}$  can be controlled through oxygen contents optimization and Al insertion, and as a result, good switching behavior can be obtained. Figure.2.26 shows I-V curves of forming (a) and reset (b) process in our reference cell and oxygen content optimized cell, respectively.



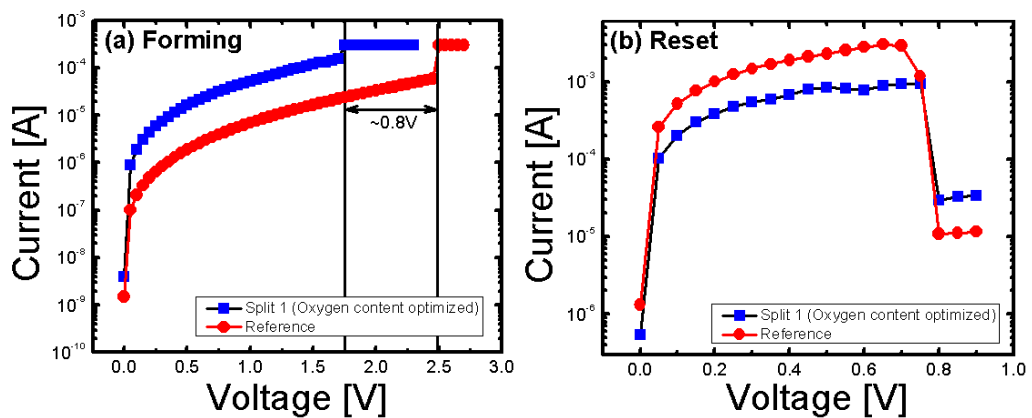
**Fig. 2.25** CF modulation effect without Al insertion layer



H. Lee, et al. reported that ‘hard breakdownlike’ phenomenon occurs if oxygen atoms would be impeded by the enhanced oxidation layer which is acting as a barrier of ionic movement [17]. It gives an adverse impact on a resistive switching process, and it means that, when we use the insertion material for improving resistive switching characteristics, finding an optimal process condition is crucial to avoid these effects. Particularly, determining oxygen contents in resistive cell and insertion layer is important in resistive switching.

We have investigated the oxygen content effect in resistive cell structure. When oxygen content in the cell is optimized,  $I_{RESET}$  slightly decreases compare to our previous reference cell. But  $V_{FORMING}$  is drastically decreased from 2.5V to 1.7V as shown in fig.2.26 (a), which means that optimal oxygen contents allow for both effective reset and forming process. Even though optimal oxygen content can help forming process, oxygen content difference alone is not the solution of the  $I_{RESET}$  improvement. And, if  $AlO_x$  thickness is sufficiently thick,  $I_{RESET}$  characteristics are not improved. Al thickness for our experiment is about 8Å. If Al thickness is over nm level,  $I_{RESET}$  is not reduced. Therefore, combining a bi-layer structure with optimal oxygen content and  $AlO_x$  thickness are needed to improve both forming and reset characteristics. In order to implement a low switching current RRAM, relationships between conducting defect and various related analytical

parameters have been investigated. Experimental and simulation data have shown that better resistive switching can be realized by bi-layer cell structure which is inserted in an  $\text{AlO}_x$  buffer layer between Ir/NiO interfaces. Sufficient, thermally activated diffusion process enhanced by joule-heating at reset state, an oxygen vacancy, and  $\text{AlO}_x$  formation due to lower electro-negativity of Al has sufficiently enabled the  $I_{RESET}$  to be reached below 0.15mA. Optimal formation of  $\text{AlO}_x$  interface with optimal oxygen content in resistive cell has led to uniform forming with low  $I_{RESET}$ .



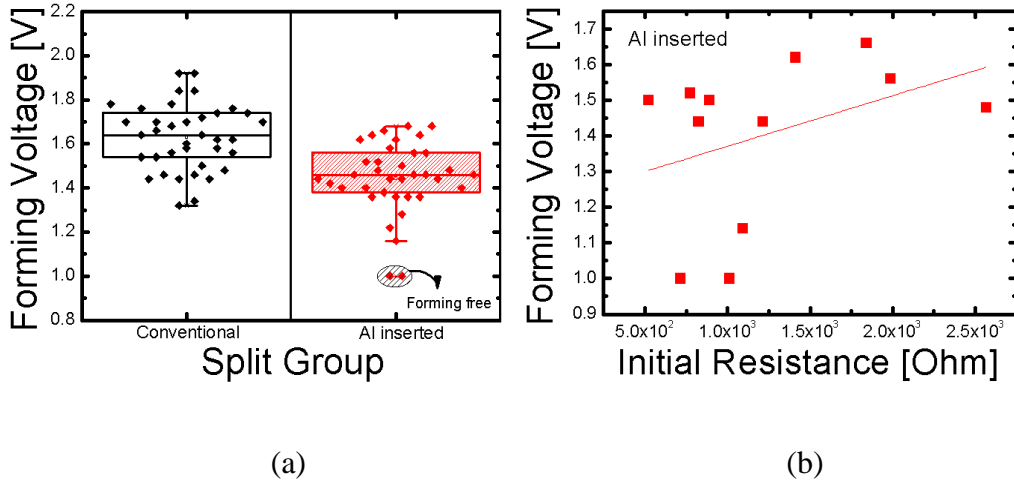
**Fig. 2.26** Forming (a) and reset (b) characteristics on the oxygen content difference in conventional resistive cell.

### 2.3.4 Experimental results: statistical analysis

In order to verify above experimental results in more detail, advantages of bi-layer RRAM structure over conventional structure will be explained using statistical analysis.

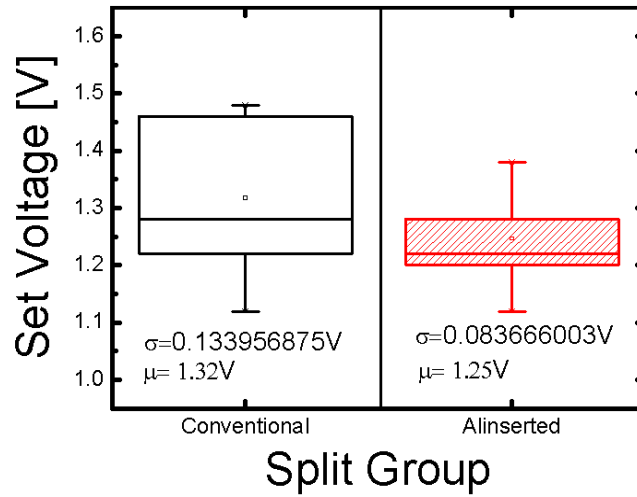
Figure 2.27 shows the statistical analysis of  $V_{FORMING}$  as a function of split group (b) and initial cell resistance of Al-inserted bi-layer structure. As shown in Fig.2.27 (a), mean value of  $V_{FORMING}$  of bi-layer group is slightly reduced from 1.6V to 1.4V due to easier CF source formation such as Vo and metallic Ni ion in bi-layer interfaces. Standard deviation and relative fluctuation of  $V_{SET}$  in each split cells were 0.15V ,0.16V ( $V_{SET\_σ}$ ), 9%, and /11% ( $σ/μ$ ), respectively. We know that CF forming is initiated by the residual conduction of the oxide.

As shown in Fig. 2.27(b), it is verified that  $V_{FORMING}$  increases when  $R_{INITIAL}$  is large. Based on experimental results, in the case of resistive switching layer with very thin additional top layer enough to have no involvement in switching,  $V_{FORMING}$  is improved, because very thin additional top layer would help to increase local oxygen migrations for CF formation [72-88].



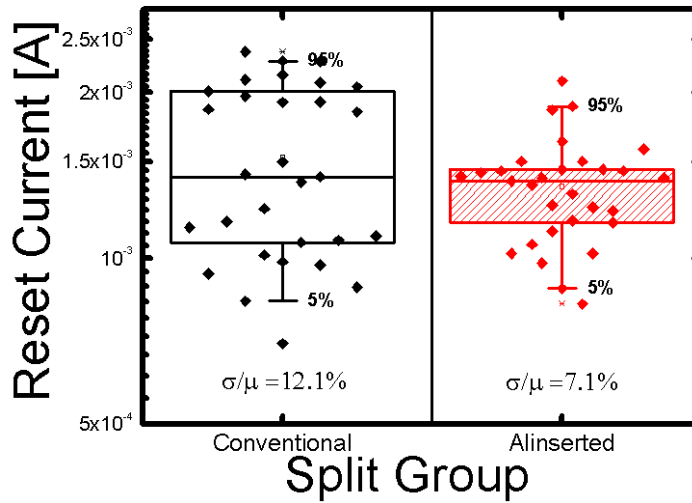
**Fig. 2.27**  $V_{FORMING}$  distribution characteristics as a function of split groups (a) and  $R_{INITIAL}$ .

Very thin additional Al upper layer effectively controls CF formation. Figure 2.28 shows the statistical analysis of  $V_{SET}$  as a function of split group. As shown in Fig. 16, mean value of set  $V$  ( $V_{SET\_μ}$ ) is slightly reduced from 1.32V to 1.25V.  $V_{SET\_σ}$  of Al-inserted structure is improved by about 37.6%, and relative fluctuation is decreased from 10.2% to 6.7% in  $V_{SET}$ . From these results, it is believed that very thin upper layer when set switching controls CF formation, therefore, it improves switching uniformity.



**Fig. 2.28**  $V_{SET}$  distribution difference of conventional and Al inserted cell.

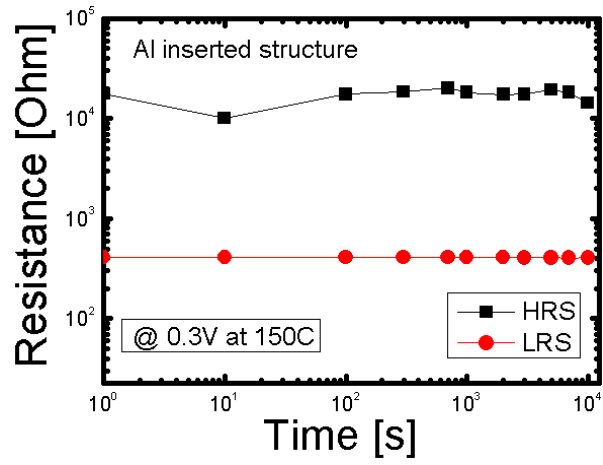
Figure 2.29 shows the statistical analysis of  $I_{RESET}$  as a function of split group.  $I_{RESET\_μ}$  is almost the same for both conditions as shown in Fig. 2.29.  $I_{RESET\_σ}$  of Al inserted structure is also effectively improved. So compared to conventional single cell structure, relative fluctuation of  $I_{RESET}$  is decreased from 12.1% to 7.1%. Therefore, the improvement of  $I_{RESET}$  distribution has been identified as well. Improved switching fluctuation of  $I_{RESET}$  means that more controllable CF is formed.



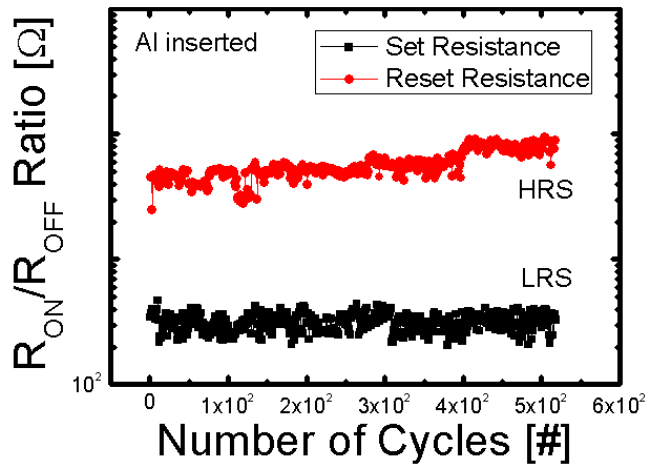
**Fig. 2.29**  $I_{RESET}$  distribution difference of conventional and Al inserted cell.

Data retention characteristics have been investigated. Figure 2.30 shows the retention (a) and switching endurance (b) characteristics of Al-inserted structure.

Bake retention results which are obtained after  $10^4$  seconds followed by baking at  $150^\circ\text{C}$  are satisfactory as shown in Fig. 2.30(a). In addition,  $5.24 \times 10^2$  cycling characteristics over 1.5 order of magnitude of  $R_{on}/R_{OFF}$  ratio without remarkable degradation is observed as depicted in Fig. 2.30(b).



(a)



(b)

**Fig. 2.30** Retention (a) and endurance (b) characteristics for Al-inserted cell.

From these results, it has been confirmed that CF can be effectively controlled, and particularly that CF distribution can be effectively improved by using Al-inserted cell which is bi-layer RRAM. Therefore, effective CF control affects switching characteristics in a great deal, and in turn becomes the most significant factor in improving unipolar resistive switching by CF control. Thus, next chapter will examine effective CF control, especially local formation of CF and switching characteristics in more detail [64].

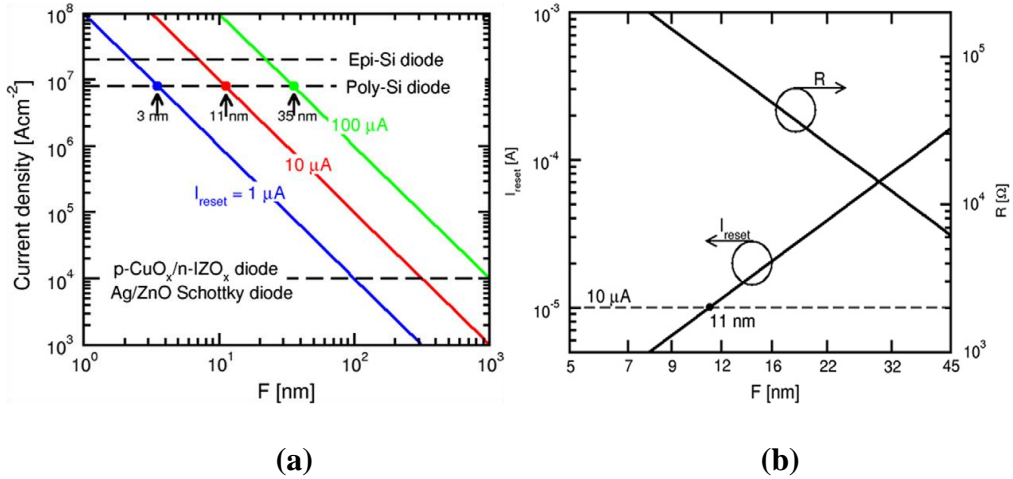


## 2.4 Reset current reduction and CF modulation

We have one important question. Why should we reduce  $I_{RESET}$  under sub- $\mu\text{A}$  region? Achieving sub-10  $\mu\text{A}$  for reset process is very crucial for further high-density RRAM application.  $I_{RESET}$  is directly correlated with the size of current source such as diode or transistor for a given current density under applied bias [82]. Figure. 2.31 shows the calculated reset current density  $J_{FWD} = I_{RESET}/F^2$  as a function of technology node defined as the minimum feature size controlling the half pitch [82-83]. The current density is calculated for three values of  $I_{RESET}$ , namely  $I_{RESET} = 1, 10$  and  $100$  mA [82]. The measured current density values for different current source technologies are also reported, including epitaxial Si p-n junction [30], poly-Si p-n junction [83], oxide hetero-junction diode [82-83] and Ag-ZnO Schottky diode [82-83]. The reference values for the forward current density were taken at a voltage of 2 V across the diode. For achieving low  $I_{RESET}$  level under  $10\mu\text{A}$ , Fig.3.31 (a) indicates that poly-Si-based diodes allow scaling to  $F = 11\text{nm}$  [82]. Only for the Si-based diodes, the scaling can be possible into the  $10\text{nm}$  area [82].

Fig. 2.31 (b) shows calculated values of  $I_{RESET}$  and  $R = V_{RESET} / I_{RESET}$ , assuming

$V_{RESET} = 1$  V and a polysilicon-diode forward current density [82]. It means that for a given current source technology using diode,  $I_{RESET}$  must be continuously scaled to allow scaling to a smaller design rule in a RRAM array structure.



**Fig. 2.31** Scaling perspective of 1R1D memory cells with different diode select devices (a) and  $I_{RESET}$  as a function of F (b). [82-83].

In order to achieve effective  $I_{RESET}$  scaling for unipolar RRAM application, thermo-chemical based switching parameter control is essential. Especially, CF control in resistive material is very important.

If the temperature in which reset occurs “ $T_{RESET}$ ”,  $T_{RESET}$  can be written by using joule-heating effect as follows [82].

$$T_{RESET} = T_0 + P = T_0 + I^2 R = T_0 + \frac{V^2}{R} \quad (2.1)$$

$$(T_{RESET} - T_0) = \frac{V^2}{R} \quad (2.2)$$

The second equation can be expressed as below by using Ohm's law,

$$I_{RESET} = (T_{RESET} - T_0)^{\frac{1}{2}} (R_{ON})^{-\frac{1}{2}} \quad (2.3)$$

Then, since resistance at  $I_{RESET}$  is related to  $R_{ON}$ ,  $I_{RESET}$  can be written as follows.

$$I_{RESET} \propto \frac{1}{R_{ON}} \propto A_{CF} \quad (2.4)$$

$$\therefore I_{RESET} \downarrow, A_{CF} \downarrow$$

In other words,  $I_{RESET}$  decreases proportionally to  $R_{ON}$ . It means that, to reduce  $I_{RESET}$ , controlling  $R_{ON}$ , which is a control factor of ACF, is important in unipolar RRAM followed by joule heating effect in reset process [83].

The effect of resistive switching area and structure on resistive switching in unipolar RRAM have been investigated, as well as the effect of conducting defect on resistive switching characteristics. It has been analyzed that the change in initial cell resistance and electric field due to various structures and switching area where switching occurs affect  $A_{CF}$  and its shape. By RCB simulation model, the effect of the scope of CF change at resistive switching compared to the entire resistive cell has been calculated, which had been difficult to verify with actual

experiment due to process limitations by current photo-lithography level. With this simulation model, it has been verified for the first time that, when switching area is reduced to sub-nm region,  $I_{RESET}$  may be reduced as well.

As we have mentioned previously, we used RCB simulation model to predict the resistive switching characteristics of unipolar RRAM. Particularly the statistical analysis using this simulation explains the difference between simulation and experimental study. These results show that cell area as well as  $A_{CF}$  in sub-nm region is closely related to  $I_{RESET}$ , and that it can be verified by simulation method [34].

Many researchers have reported that  $I_{RESET}$  is proportional to the  $A_{CF}$  relating to resistive switching [49-55]. Compliance current ( $I_{COMP}$ ) control is one of the effective and powerful methods to control the  $A_{CF}$  results in  $I_{RESET}$  reduction. Many previous reports support this  $I_{COMP}$  effect.  $R_{INITIAL}$  is one of effective ways to determine the  $I_{COMP}$  at initial state. If  $R_{INITIAL}$  is relatively high, we can control  $I_{COMP}$  level more effectively from low current to high current level. Area scaling is very easy and useful method to control its  $R_{INITIAL}$ . Therefore, area scaling can maximize the  $I_{COMP}$  related current scaling.

However, the studies have reported that  $I_{RESET}$  is not reduced in a few nm size of CF path as switching area is reduced because the change in  $R_{ON}$  originated from

$A_{CF}$  reduction is very small [3]. Also, other researchers have reported that  $I_{RESET}$  is drastically reduced in highly scaled cell [4].

Nonetheless there is no precise verification on whether  $I_{RESET}$  is reduced as  $A_{CF}$  reduces, and there have not been reports verifying such theory. The issue is that most reported cell size of experimental data is at the micro-meter level which is a very large area of cell size. Therefore, increase or decrease in the number of nm in CF take up rather very small portion, making it difficult to verify the effective CF change.  $A_{CF}$  change at the sub-nm region takes up a very small portion in a relatively large area, therefore it is difficult to precisely verify the  $A_{CF}$  change. And since such  $A_{CF}$  change is insignificant, it is difficult to understand an accurate resistive switching relationship between switching area and  $A_{CF}$ . Therefore, it is very important to understand such CF behaviors at sub-nm region which is highly scaled switching region. Since it is difficult to understand the switching behavior of CF using in current large area of cell size, we cannot conclude that  $I_{RESET}$  is irrelevant to switching area in sub-nm in which actual  $A_{CF}$  change may have relatively important meaning. In this context, we have proposed highly scaled RRAM cell structures to elucidate this area scaling effect in chapters 3 and 4.

## 2.5 Summary

In this chapter, we investigate that CF plays an important role in unipolar resistive switching by using single and bi-layer cell structure. It has been also shown that irregular resistive switching behavior is detected intermittently with a conventional large area cell due to the undesired CF interactions [10]. Therefore, controlling the localized CF in a unipolar resistive switching material is very important in understanding the resistive switching mechanism and controlling the switching characteristics [11]. In addition, in the case of unipolar RRAM operation under such a filament conduction model [4], switching interface will influence the CF control. In this context, we have investigated that it is particularly important to understand the relationships between CF modulation and various related analytical factors especially on the resistive switching area for reducing the  $I_{RESET}$ . Simulation and experimental results using various structures give us some important clues that the CF formation and rupturing process in unipolar switching are strongly related to the switching area in the sub-nm region, not only in terms of its vertical thickness but also of its horizontal length. With the optimal CF modulation having sufficient  $R_{INITIAL}$  and a low  $V_{FORMING}$ , the

achievement of the greatest feasibility of low  $I_{RESET}$  will be further accelerated. The on/off resistance ratio increases as the cell area decreases at the sub-nm level, and these phenomena are explained in terms of the relatively large  $R_{ON}$  change in a very small conventional cell area. In this respect, improved breakthrough should be addressed based on the correct understanding of resistive switching mechanism.

# Chapter 3

## Highly Scaled Crown Shape Cell

### 3.1 Introduction

It is crucial to study whether  $I_{RESET}$  can be reduced depending on cell area in order to materialize high-density and low-power RRAM application. However, this still is an object of controversy.

According to D. Ilemini et al,  $I_{RESET}$  needs to be reduced by an alternative approach because  $I_{RESET}$  does not change depending only on switching cell area [34]. Kim et al reports that  $I_{RESET}$  can be reduced by reducing contact area using very small electrode such as dash type BE [1-13]. Therefore, intensive study is still needed to understand the area scaling effect more accurately.

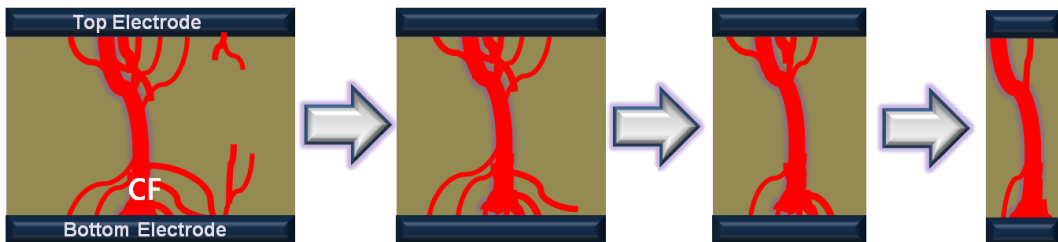
In this chapter, a novel MIM cell structure designed for low-power RRAM is proposed to find its area scaling feasibility. We show that controls of the switching area and deposition orientation of resistive material, where resistive



switching occurs at resistive cell material/TE interface are expected to reduce the  $I_{RESET}$ . We also examine that this modified cell area in turn affects the CF modulation results along with feasibility of low-power RRAM. Experimental results are presented to verify the crown shape cell.

## 3.2 Experimental Results

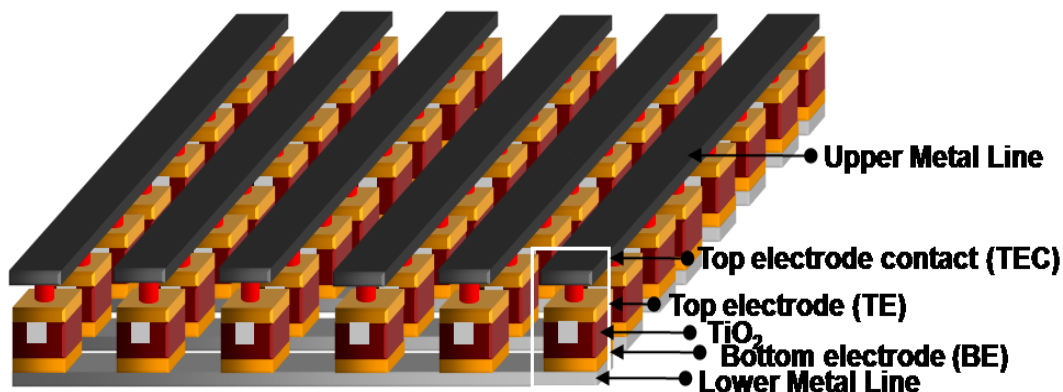
Figure 3.1 shows the schematic drawings of possible scenario of CF modulation for large cell (left side) and scaled cell (right side). The total demension of CF associated with resistive switching is reduced as switching area is reduced at critical area as shown in Fig. 1. Especially, tiny CF branches at switching interface in the cell are also reduced due to the switching area reduction in highly scaled cell contributing to the  $I_{RESET}$  reduction.



**Fig. 3.1** Schematic drawing of CF modulation effect by using resistive switching area control.

Figure 3.2 shows the schematics of proposed crown shape structure. The number of CF associated with reset state is reduced as the contact area  $a$  gets smaller. Contact area can be defined as the total length of interface region between

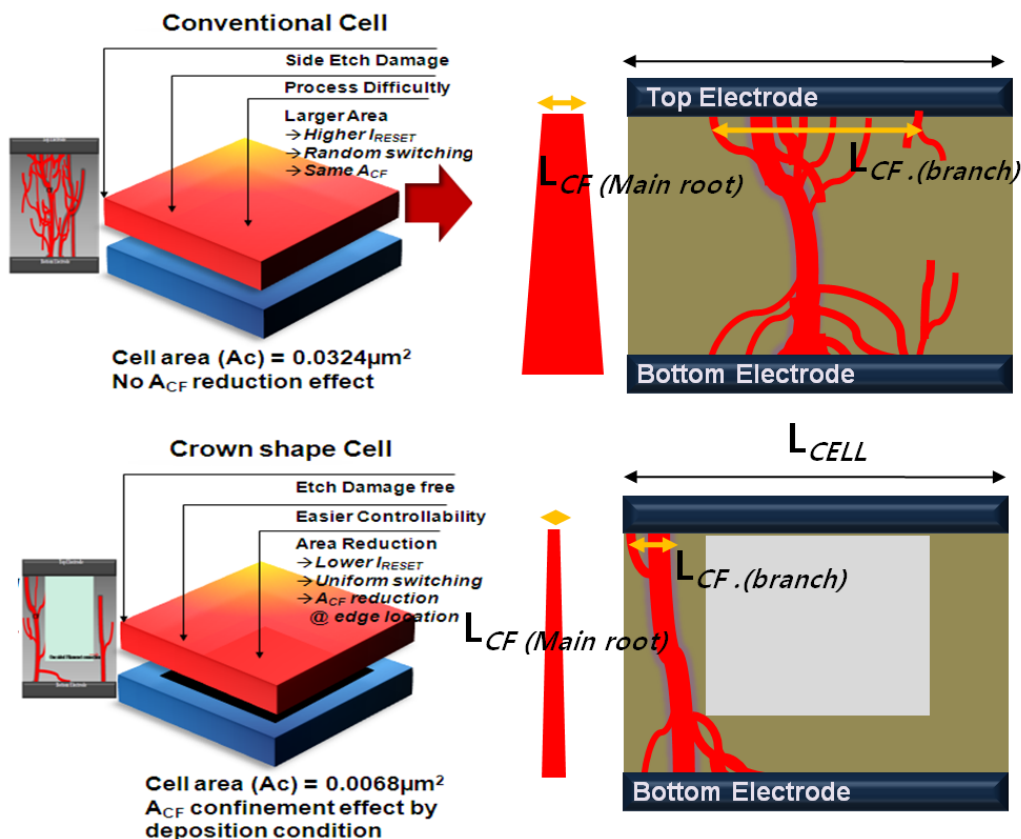
resistive switching material and top electrode.



**Fig. 3.2** Schematic drawing of our crown shape RRAM cell structure.

Figure 3.3 depicts the schematic drawings of contact area calculation of conventional cell and proposed crown shape cell. The contact area is reduced by up to 67% at the same design rule by using crown shape cell. Compared to the result when adapting the proposed structure, it makes not only the  $V_{SET}$  distribution controllable but also reduces  $V_{FORMING}$  by enhancing CF controllability. Moreover, we can easily control the switching area by controlling the deposition thickness of the resistive material. Although it still has limitation in total area reduction due to the current lithography issue, highly scaled switching layer formation is possible by using proposed structure since highly localized one directional switching region can be obtained due to its deposition controlled

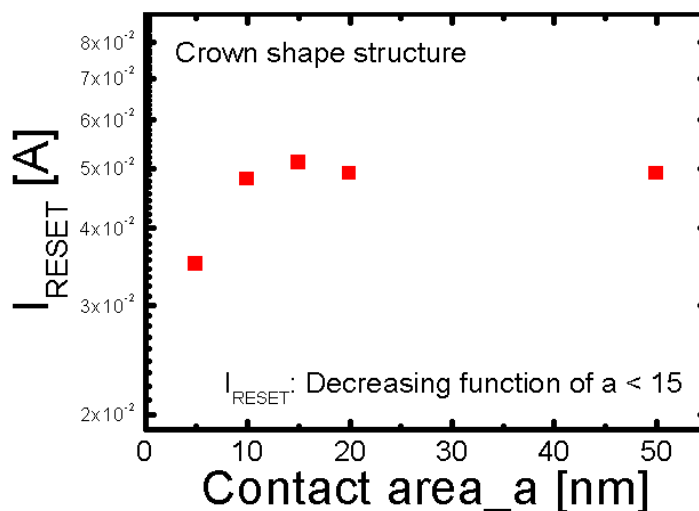
switching area formation. Therefore, we can expect the scaling effect by this structure without current photolithography limit.



**Fig. 3.3** Illustrations of calculated contact area of conventional cell and crown shape cell. Contact area is reduced up to 67% with 16nm switching layer deposition at the same design rule by using modified structure.

Here, we further investigate the effect of contact area of our structure depending on  $I_{RESET}$ . As the contact area  $a$  decreases in Fig. 3.4,  $I_{RESET}$  also decreases because

$I_{RESET}$  relies on the contact area of cell/TE interfaces. Based on the assumption that the critical contact area exists, determining optimal dimension of  $a$  is an important factor for reducing the  $I_{RESET}$  and cell distribution.

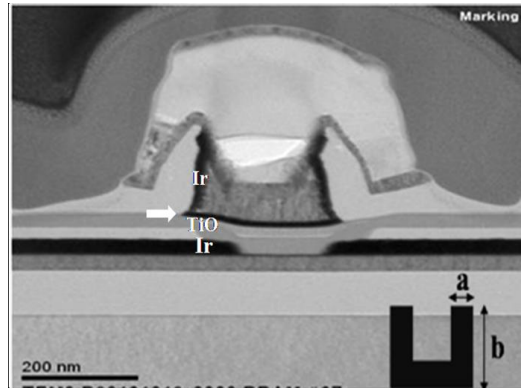


**Fig. 3.4** Effect of contact area ‘ $a$ ’ of crown shape RRAM as a function of  $I_{RESET}$ . Critical  $I_{RESET}$  reduction area exist.

The profile of crown shape cell has been observed with the transmission electron microscope (TEM). Figure 3.5 shows the cross-sectional TEM image of our proposed crown shape cell. The vertical stack of a resistive cell consists of a top electrode connected to Al metal line, a  $TiO_2$  cell having crown shape cell vertically, and a bottom electrode connected to lower metal line. As previously mentioned in Fig. 3.4, contact area ‘ $a$ ’ can be easily tuned by adjusting deposition

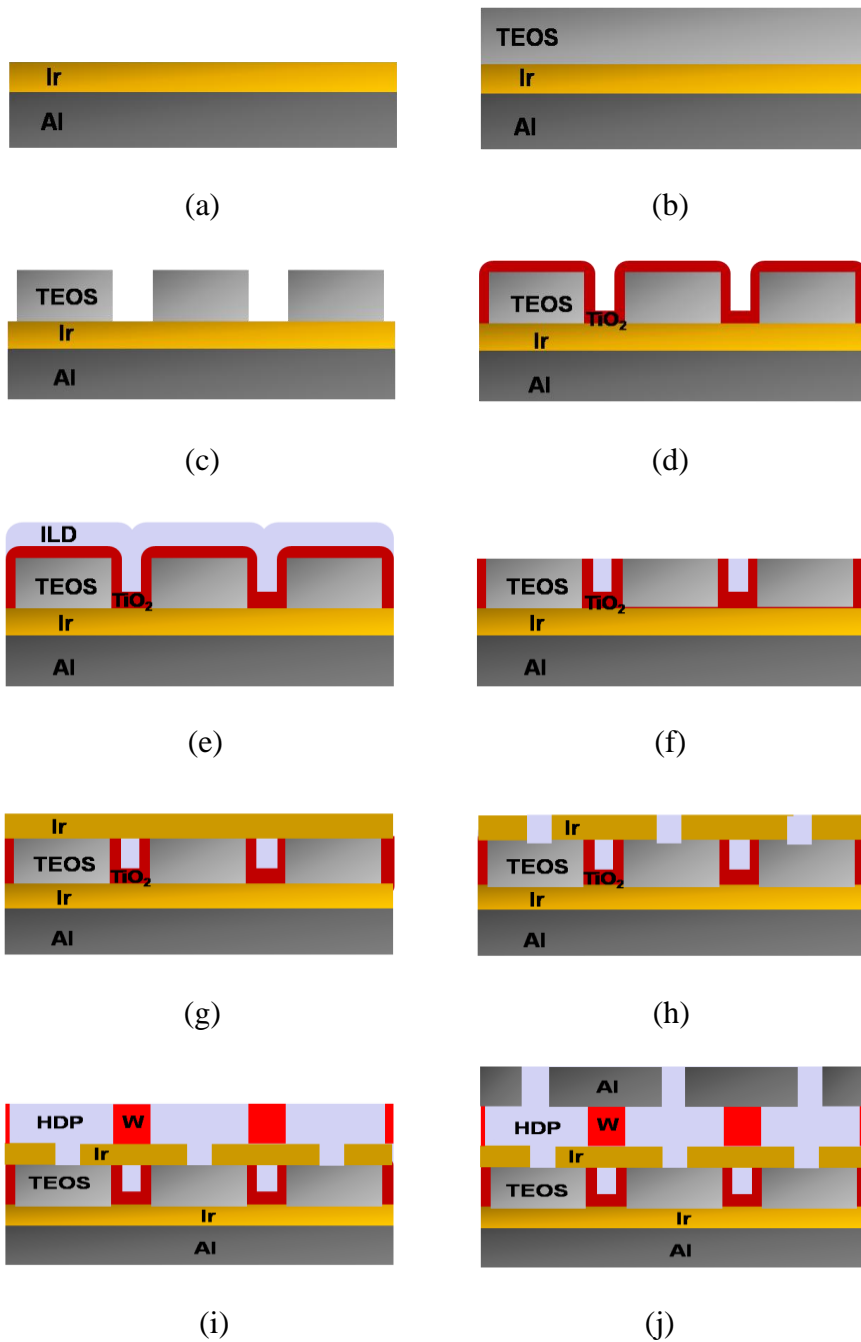
of resistive cell thickness, confirming the effectiveness of our proposed structure. Therefore, this structure can control programming current quite well in the same chip area without process difficulty.

It was difficult to identify the proposed structure due to the cutting issue. However, in the case of the TEM image, switching layer etch back was not completed and only a very small contact area was formed due to misalignment between top electrode and switching layer. It was identified that very low  $I_{RESET}$  level is obtained in such a case. For array fabrication, obtaining more effective process margin is necessary in order to prevent a short to the next cell array. However, in order to identify scaling effect, it was important to make localized cell area, and was identified in the proposed structure. In addition, when a large cell area is formed due to process variation issue, high  $I_{RESET}$  equal to conventional structure with large cell area was identified. Therefore, such structural effect helped to more effectively identify  $I_{RESET}$  and area effect.



**Fig. 3.5** Cross sectional TEM image of our proposed crown shape cell structure.

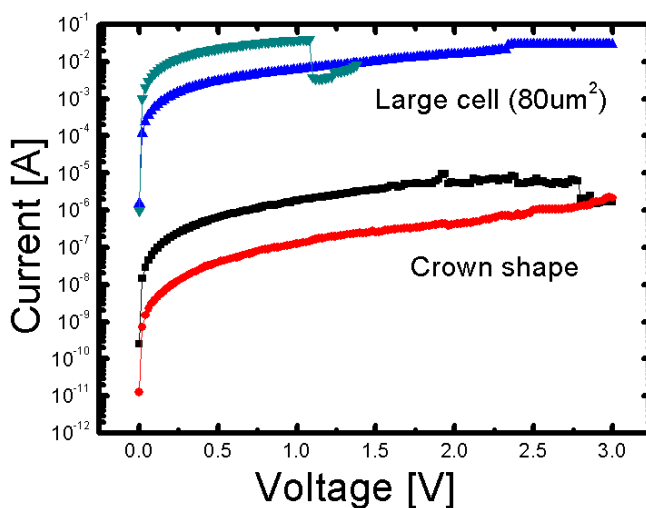
Figure 3.6 depicts the fabrication process of our proposed MIM cell structure: once Al lower metal line, Ir bottom electrode (BE) and mold oxide such as tetraethyl orthosilicate (TEOS) were performed, then mold oxide patterning was performed. After that,  $\text{TiO}_2$  resistive material and interlayer dielectric (ILD) materials were deposited on the mold to fill the contact hole. Particularly, Ti deposition step and plasma oxidation step were performed for formation of vertical conducting Ti path in the cell. After chemical mechanical planarization (CMP) process as shown in Fig. 3.6 (f), Ir TE deposition and etch process were carried out to define each resistive cell. Cell area was  $0.2 \text{ by } 0.2 \mu\text{m}^2$ . Finally, top electrode contact (TEC) and upper Al metal line were generated. An MIM cell structure was built in between two metal lines that are cross-pointed for selecting a resistive cell and for writing/reading data, respectively.



**Fig. 3.6** Illustration of fabrication process of our proposed crown shape cell.



Figure 3.7 shows typical I-V curve of large area ( $80\mu\text{m}^2$ ) conventional cell and crown shape RRAM. The  $I_{RESET}$  is drastically decreased to sub-10  $\mu\text{A}$  in crown shape cell compared to the large area cell that show a high  $I_{RESET}$  of 30 mA. The low  $I_{RESET}$  is attributed to the decreased contact area which is located between top electrode and resistive material in crown shape RRAM. The active area is calculated depending on the edge side of active area of crown shape RRAM in Fig 3.3. In addition, crown type contact structure itself can help to improve controllability of CF because it can be confined in a localized area [3]. The relationship between the  $I_{RESET}/R_{ON}$  and the active area size were studied recently [5] and our device samples are entirely consistent with this tendency in the inset of Fig. 3.7.

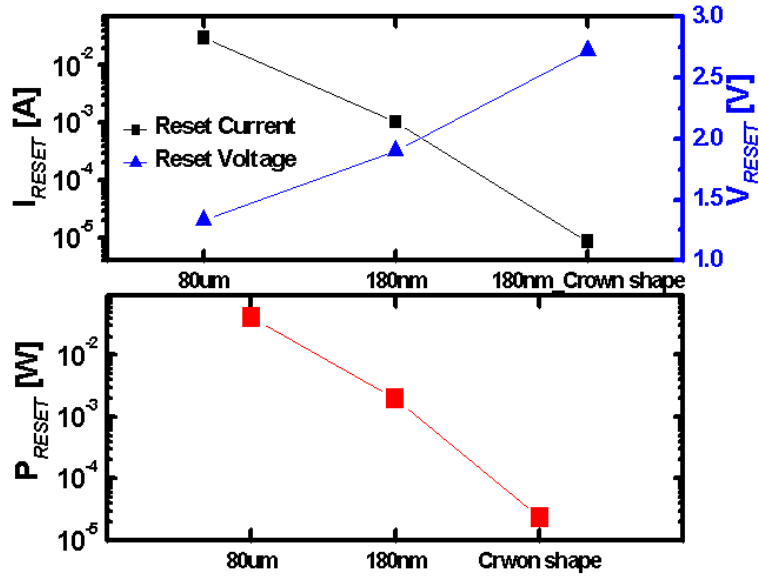


**Fig. 3.7** Typical I-V characteristics and LRS resistance of S1 with a large cell

and crown shape cell.

It is generally difficult to achieve a fabrication of conventional RRAM with a small cell size due to the limitation of lithography. On the contrary, the crown shape cell has device size margin in fabrication process by having modified structure.

Figure 3.8 shows  $I_{RESET}$ ,  $V_{RESET}$ , and reset power ( $P_{RESET}$ ) in large area of conventional cells and crown shape cell. Although the  $V_{RESET}$  is slightly increased in crown shape cell compared to large area cell, the  $I_{RESET}$  is drastically decreased to sub-10nm in crown shape cell for low-power switching. Another advantage of crown shape cell is that it shows forming-less characteristics. It is known that  $V_{FORMING}$  is generally increased with  $R_{INITIAL}$ . However, the crown shape cell is favorable to  $V_{FORMING}$  due to a structural advantage. Initial CF in pristine resistive cell is formed before forming process because a deposition orientation is in a vertical direction.

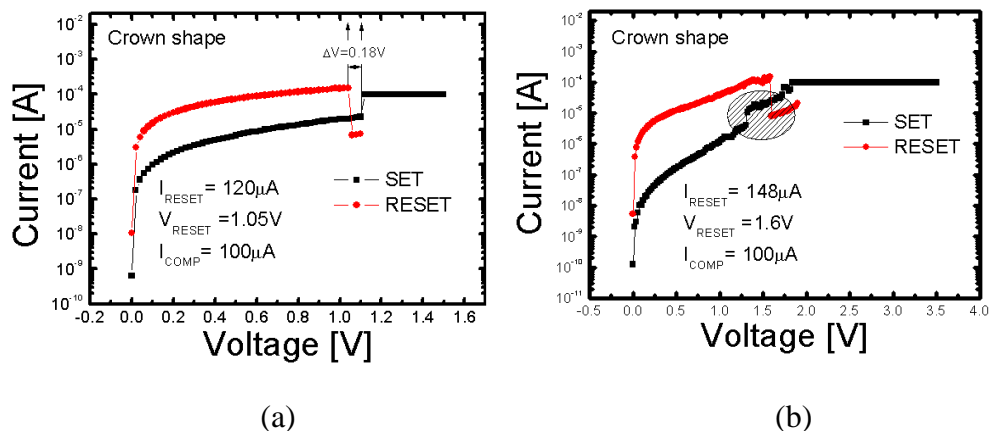


**Fig. 3.8**  $I_{RESET}$ ,  $V_{RESET}$  and power characteristics of conventional cells with different cell size and crown shape RRAM.

In order to test whether this proposed structure contributes to the improvement of switching characteristics, an electrical measurement was performed. Figure 3.9 shows the measured I-V curves of crown shape structure for different  $I_{RESET}$  level.

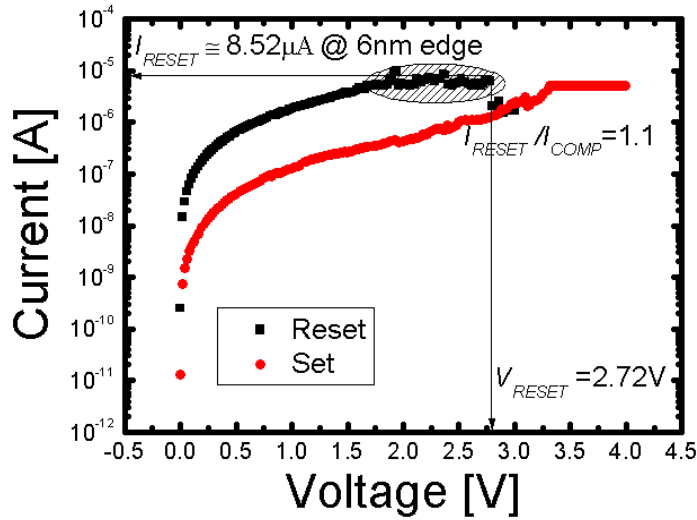
As shown in Fig. 3.9 below,  $I_{RESET}$  of  $120\mu\text{A} \sim 150\mu\text{A}$  was possible in the crown shape cell. In the proposed structure, whose contact area of one side is 16nm compared to conventional structure, the contact area is decreased by approximately 67.6%, but  $I_{RESET}$  is decreased by more than 1 order of magnitude. It signifies that  $I_{RESET}$  can be more effectively reduced as the area becomes smaller due to the proposed structural effect. Particularly, it means that such an area effect can be

accelerated as the cell area becomes small.



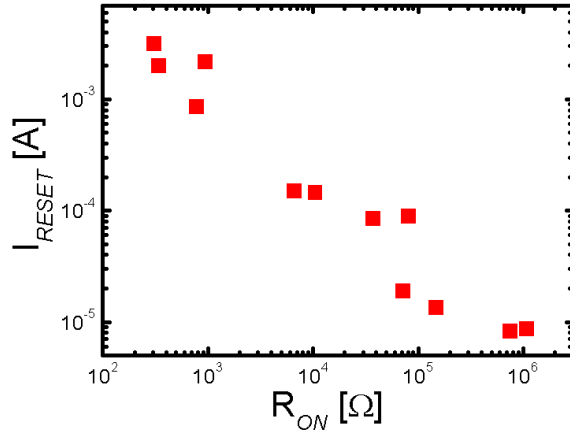
**Fig. 3.9** I-V curves of crown shape cells where the typical  $I_{RESET}$  level is from 120uA (a) to 150uA (b).

Also as shown in Fig. 3.10 below, best cell having low  $I_{RESET}$  under  $10\mu A$  was also obtained. It means that a tiny CF can be formed in a very small area without process variation, and it also implies that, by identifying optimal area, the security of cells with a very small reset energy may be guaranteed. Also as in the previously mentioned ITRS roadmap [15], obtaining  $10\mu A$   $I_{RESET}$  level cell signifies securing  $I_{RESET}$  possible in process under 2X design rule. It is an extremely meaningful data, reconfirming the advantages of RRAM possible for high-density mememory application.



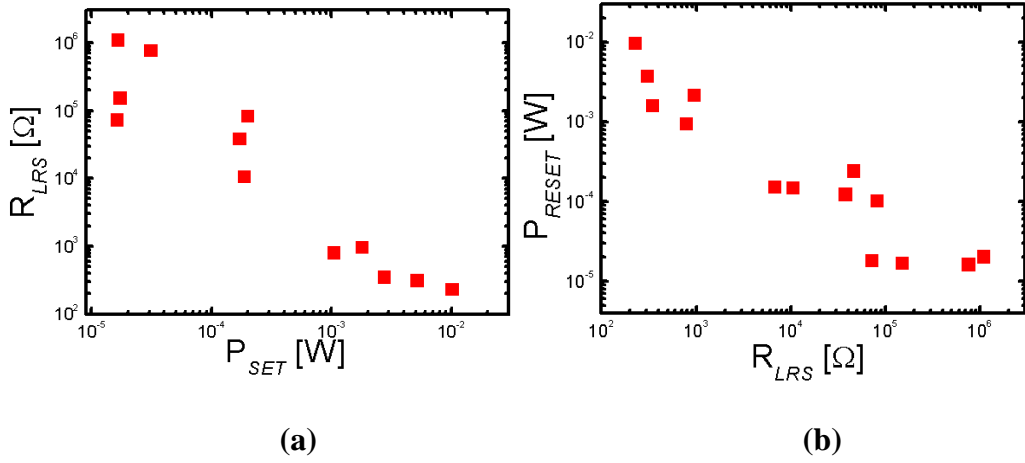
**Fig. 3.10** I-V curve showing best  $I_{RESET}$  characteristics of crown shape cell.

As previously mentioned,  $R_{ON}$  is closely related to  $I_{RESET}$  [15]. In other words,  $R_{ON}$  changes depending on the CF change. Therefore, through the relationship between  $R_{ON}$  and  $I_{RESET}$ , it is confirmed that the increase in  $R_{ON}$  has a direct relationship with the decrease in  $I_{RESET}$ . Figure 3.11 represents the relationship between  $R_{ON}$  and various  $I_{RESET}$  of crown shape samples. As shown in Fig.3.11, it is shown that  $\log I_{RESET}$  has a linear relationship with  $\log R_{ON}$ . Eventually, effective control of  $R_{ON}$  in unipolar RRAM is an important factor, and effective decrease in  $I_{RESET}$  may be achieved through such variation.



**Fig. 3.11**  $I_{RESET}$  of crown shape cells as a function of  $R_{LRS}$ .

Figure 3.12 shows the  $R_{LRS}$  as a function of  $P_{SET}$  (a) and  $P_{RESET}$  (b) in a crown shape cell. As shown in the figure below,  $R_{LRS}$  increases with decreasing  $P_{SET}$ . This result also gives a guideline for low-power RRAM by effective  $R_{LRS}$  control. Consistently,  $P_{RESET} = I_{RESET} \times V_{RESET}$  decreases with the increase of  $R_{LRS}$ . Therefore, in order to implement low-power RRAM,  $V_{RESET}$  control is also important.



**Fig. 3.12** Influence of  $P_{SET} = I_{COMP} \times V_{SET}$  on  $R_{LRS}$  (a) and subsequent effect of  $R_{LRS}$  on  $P_{RESET} = I_{RESET} \times V_{RESET}$  (b).

However,  $V_{RESET}$  generally seems to increase as  $I_{RESET}$  decreases. Figure 3.13 represents the relationship between  $V_{RESET}$  and  $I_{RESET}$ . It was verified that, in general,  $I_{RESET}$  decreases as  $V_{RESET}$  increases. Why does such a phenomenon occur? If the reset process is supposed to occur by joule heating in unipolar RRAM, defining “ $T_{RESET}$ ” as the temperature in which reset occurs,  $T_{RESET}$  can be given as Equation 2.1, Chapter 2[37].

From Eq. (2.1), we can obtain

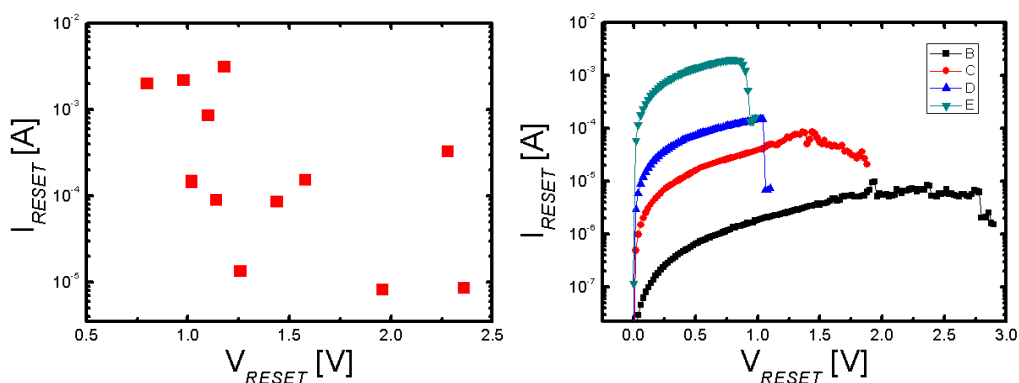
$$V = R^{\frac{1}{2}} (T_{RESET} - T_0)^{\frac{1}{2}}. \quad (3.1)$$

Since resistance at  $V_{RESET}$  is related to  $R_{ON}$ , Eq. (3.1) can be rewritten as [89].

$$V_{RESET} = R_{ON}^{\frac{1}{2}} (T_{RESET} - T_0)^{\frac{1}{2}}. \quad (3.2)$$

In other words,  $V_{RESET}$  increases as  $R_{ON}$  increases, meaning that as  $R_{ON}$  increases,

heat efficiency of CF decreases. Therefore in order to disconnect CF, a higher voltage needs to be applied. Such theory coincides with the previous study by D. Illemini [19], and such effect is actually confirmed using the proposed structure. Therefore,  $I_{RESET}$  and  $V_{RESET}$  have a trade-off relationship in the proposed structure, and it seems to be a very useful relationship in unipolar RRAM, in which Joule heating is the most important reset mechanism [76].



**Fig. 3.13**  $I_{RESET} - V_{RESET}$  characteristics of crown shape cells which shows trade off relationship between  $I_{RESET}$  and  $V_{RESET}$ .

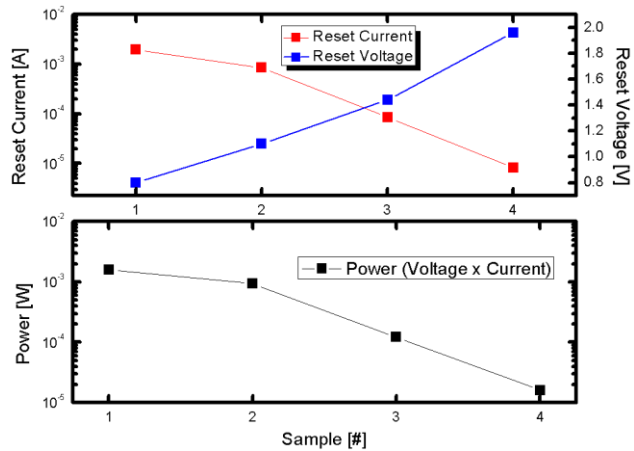
Although  $V_{RESET}$  increases with  $I_{RESET}$  decrease, overall switching power is decreased in the proposed crown shape cell even with the increase in  $V_{RESET}$ .

Figure 3.14 shows the  $I_{RESET}$ ,  $V_{RESET}$  and switching power of crown shape cell. As previously described, decrease in  $I_{RESET}$  is much larger than the increase in  $V_{RESET}$  in cell with low  $I_{RESET}$  though  $V_{RESET}$  increases. Therefore, switching power



decreases.

When Joule heating is used as the switching mechanism,, low switching power for reset means that the temperature generating reset process becomes low. Generating reset in low Joule heating means that relatively thin CF is formed. Thus, it is clear that effective CF reduction occurs in unipolar RRAM through switching power reduction.



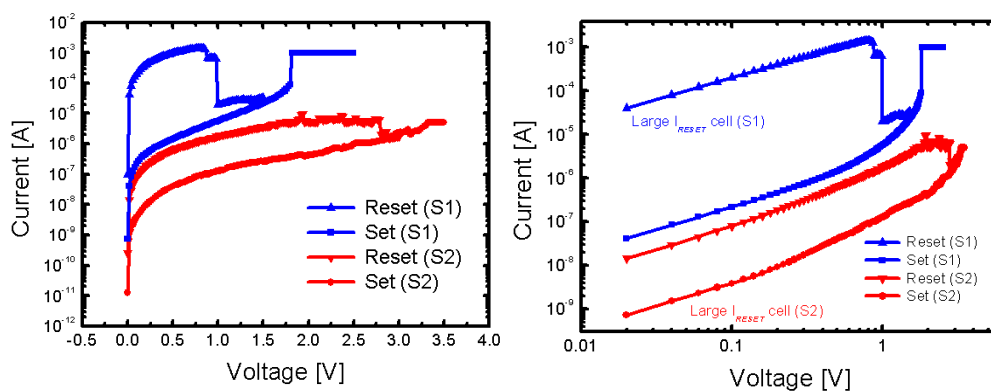
**Fig. 3.14**  $I_{RESET}$ ,  $V_{RESET}$  and switching power of crown shape RRAM.

Previous results show that CF area and shape play an important role in  $I_{RESET}$  reduction. Therefore, understanding the origin of CF itself is very important in predicting  $I_{RESET}$  level.

$I_{RESET}$  and CF relationship have been identified through various I-V fitting.

Figure 3.15 describes I-V (a) and log I-log V (b) characteristics of two samples (S1: high  $I_{RESET}$ , S2: low  $I_{RESET}$ ) of different  $I_{RESET}$  characteristics.

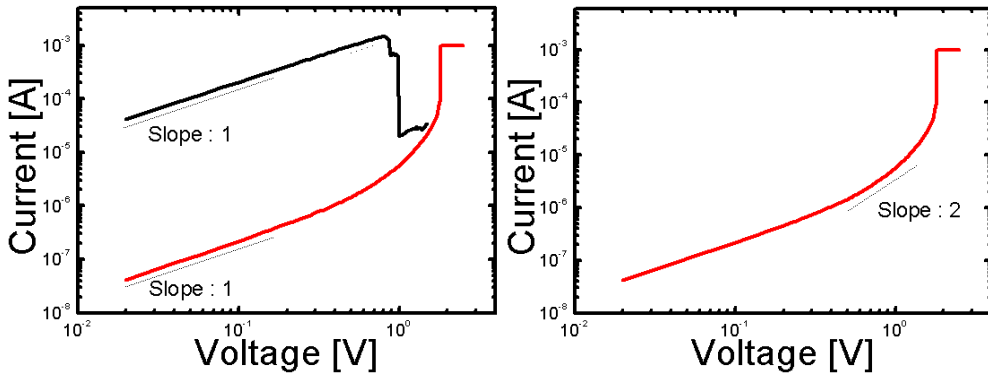
In order to predict CF characteristics formed at LRS and HRS states in two cells with different  $I_{RESET}$ , each I-V characteristic has been plotted.



**Fig. 3.15** I-V (a) and log I-log V (b) characteristics of two samples (S1: high  $I_{RESET}$ , S2: low  $I_{RESET}$ ) of different  $I_{RESET}$  characteristics.

First, as shown in Fig. 3.16, it is verified that S1 with high  $I_{RESET}$  level ( $\sim 1$  mA) in LRS state clearly shows linear log I vs log V graphs with a slope of 1 up to  $V_{RESET}$  which is 0.7 ~ 1V, whereas the HRS state shows linear behavior only in the low voltage region under 0.2V. In HRS state, linear fitting is relatively difficult, and SCLC fitting works better. HRS current curve shows an almost exponential increase with V in the high voltage region, meaning that conduction mechanism between LRS and HRS state is difficult. Such different behavior gives a clue to

understanding the CF nature. In S1 cell, which shows high  $I_{RESET}$ , it can be easily predicted that initial CF is in thick metallic filament in LRS state.

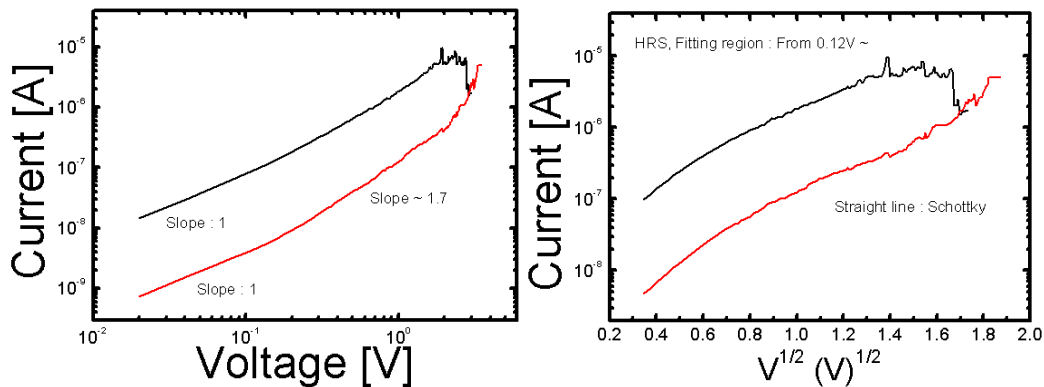


**Fig. 3.16** LogI-logV curves of HRS and LRS state (a) and LRS state only (b).

Unlike S1 cell, S2 cell with low  $I_{RESET}$  demonstrated different characteristics in LRS state. As shown in Fig. 3.17, S2 shows different characteristics with S1 cell which follows ohmic behavior in LRS state. This means that CF with different characteristics from the forming state is constructed. In other words, CF with relatively thick and metallic characteristics forms in S1. However, in the case of S2 cell, relatively tiny CF showing semiconductor behavior forms in LRS state. Therefore, it can be predicted that CF with low switching energy is needed in forming, and the probable conduction mechanism is electron hopping. In other words, it can be predicted that very tiny CF formed in the initial state can change

with relatively low switching energy, making it possible for effective switching [56].

As in Fig. 3.17, HRS state at a low voltage under 0.1V shows Ohmic characteristics. This demonstrates that very small residual filament is in effect in HRS state. However, in a higher voltage over 0.1V in HRS state, similar tendency to SCLC or P-F fitting is suitable. In HRS state, it can be seen that various conduction mechanisms, in which electrons can move via various defects, are at work. Therefore, in order to clearly understand such CF conduction mechanism, further researches need to be conducted. Particularly, temperature test and noise test are needed to verify its conduction mechanism.



**Fig. 3.17** I-V curves of HRS and LRS by fitting with various conduction mechanisms in small  $I_{RESET}$  cell.

$V_{FORMING}$  is also one of the important resistive switching characteristics for

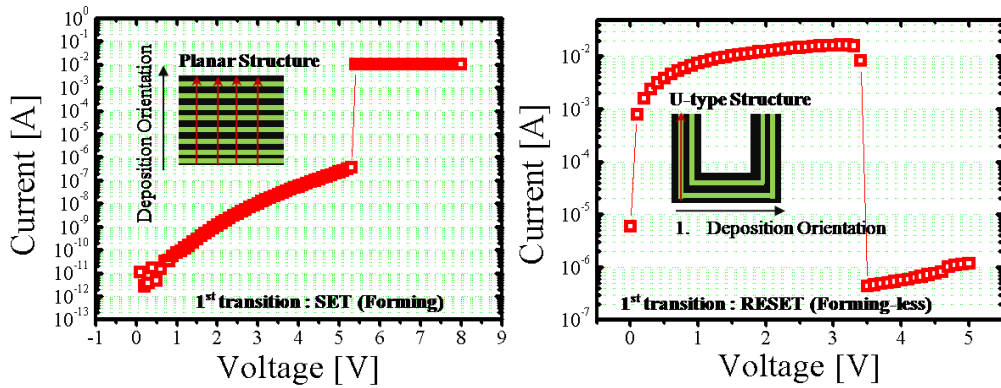
predicting CF and area relationship. In general,  $V_{FORMING}$  level is increased with decreasing device area in sub-nm region. However,  $V_{FORMING}$  level of the crown shape cell is relatively low compared that that of the conventional cell. This demonstrates that better CF controllability brings an advantage in total working voltage reduction. Such crown structure shows initial reset switching, and it is possible to reduce initial  $V_{FORMING}$  significantly. However,  $V_{SET}$  did not show much change in practice. It means that, because of initially formed tiny CF, it is almost completely erased in reset process. During the set switching in the next step, conduction along the original path does not occur, but CF can form again through a different path.

Although initial reset switching occurs,  $V_{SET}$  - similar to conventional - does not decrease in the next set switching as if a new CF forming occurred.  $V_{FORMING} - R_{INITIAL}$  relationships are well known through previous researches [1]. CF forming becomes more difficult with cell area reduction due to increase in surrounding resistance of the cell. In the case of crown shape structure, increase in cell resistance is the cause of  $V_{FORMING}$  increase. Therefore, if a path different from initially formed one occurs in the next set switching, decrease in  $V_{SET}$  cannot be expected.

Our previous data show that  $I_{RESET}$  of proposed structure is lower than

conventional structure without degradation of reset/set resistance ratio. However,  $V_{FORMING}$  level is sometimes higher than that of conventional planar structure compared with our pristine crown shape cell structure [see Fig. 3.20]. To address these issues, optimal process dimension has to be determined to implement excellent distribution property with suitable  $V_{FORMING}$  level. Under suitable optimal process condition, lower  $V_{FORMING}$  level can be achieved as shown in Fig. 3.20.

However, more work needs to be done because  $V_{FORMING}$  still remains on the high level. Interestingly, it is uniquely observed that forming-less process is possible when deposition orientation change of resistive material with multi-layered Ti and oxidation process is performed using crown shape cell structure.



**Fig. 3.20** First transition curves of conventional cell deposition orientation with forming (a) and our fabricated crown shape cell structure having vertical cell deposition orientation with forming-less process (b) [35].

The conformal resistive material of crown shape cell structure that are formed by multi-layered Ti deposition and plasma oxidation process can act as the initially generated pristine CF path in the TiO<sub>2</sub> cell. Since the metallic Ti layer deposition and plasma oxidation steps are repeated in the conventional structure [shown in Fig. 3.20 (a)], much more energy is needed for given applied electric field, meaning that high  $V_{FORMING}$  is required. However, in the case of Fig. 3.20 (b), multiple layers of tiny metallic Ti in crown shape structure act as pristine CF, enabling the forming-less process. Moreover, such changes may give rise to the change of interface state resistive switching. In the case of conventional structure, the cell interface states are all oxidized TiO<sub>2</sub>. However, in the case of the crown shape structure, the interface states are mixed between metallic Ti and TiO<sub>2</sub>. This initial metallic Ti existing at contact interface helps the forming process, and it implies that forming-less process can be observed in the case of crown shape cell having pristine CF layer, with first resistive switching showing reset state. Furthermore, the proposed structure can effectively control CF due to its easy controllability by using deposition time control. These findings imply that multi-layered crown shape cell structure with an optimal contact area can effectively provide initial CF, which can be used for forming-less RRAM

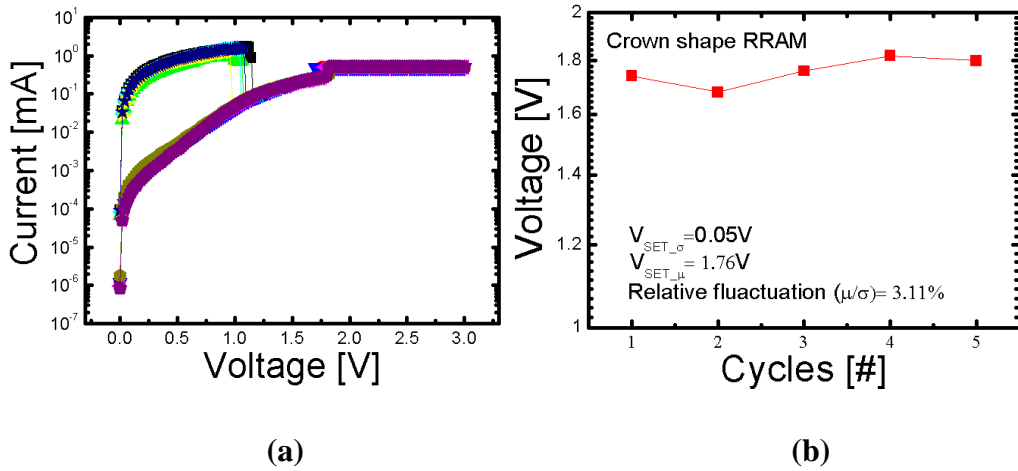
application. We have proposed a novel crown shape cell structure, which enables the reduction of the cell distribution by controlling the number of the electrical path between electrode and resistive cell interface. We have detected irregular resistive switching characteristics, and found the relationships between various resistive switching parameters and  $I_{RESET}$ . Numerical simulation was also performed using RCB model to investigate the optimal process condition. Forming-less process was realized through the proposed structure. The results strongly support that our proposed structure can play a significant role in contributing to the excellent cell distribution property with feasibility of forming-less process.

However, as previously described, various conditions need to be considered for effective decrease in  $V_{SET}$  fluctuation. Although initial reset occurs because CF forms initially due to formation of very small CF in small area, CF can be easily erased by relatively high  $V_{RESET}$  [106].

In this case it is difficult to expect  $V_{SET}$  reduction if new CF formation occurs in different cell area. However, if cell area effectively decreases such CF forming area becomes relatively small, making it possible to confine CF. Therefore, in this case, uniformity improvement is expected. Although proposed structure shows weak endurance characteristics due to other fabrication process issues such as



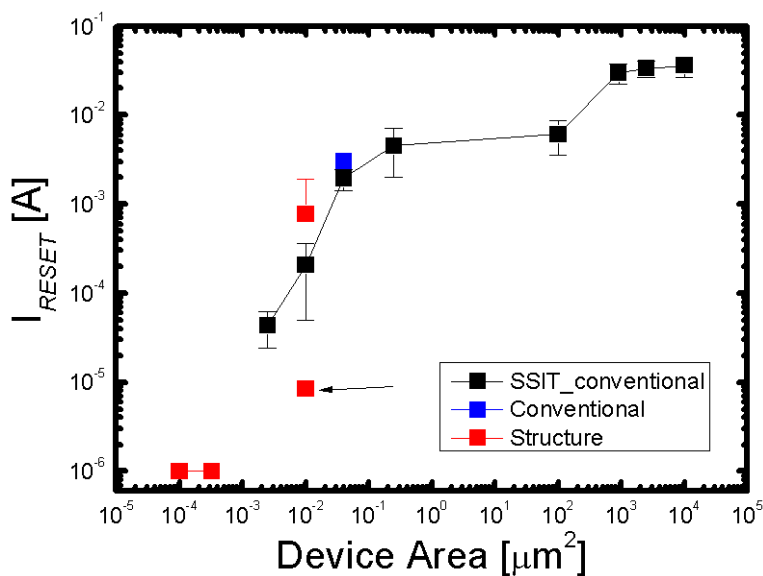
fundamental resistive switching material in Fig.3.21, uniform set characteristics are identified even in ten or so cycles by using crown shape cell.



**Fig. 3.21** I-V curve (a) and  $V_{SET}$  distribution (b) of crown shape cell.

To identify the scaling and structure effect, the  $I_{RESET}$  depending on contact area and technology node is investigated by comparing transition metal oxide (TMO) RRAM samples of other groups. Interestingly, there is a critical point of reduction in the  $I_{RESET}$  in Fig 3.22 (a) [106]. The size dependency is not noticeable in a relatively large scale. However, scaling effect is clearly observed as the active area decreases below critical point between  $0.01 \mu m^2$  and  $0.1 \mu m^2$ . In addition, the structure approach of crown shape RRAM is identified by comparing with samples at the same technology node in Fig. 3.22.

As we have previously described, conduction mechanism of large cell in LRS state shows Ohmic conduction behavior. However, small area cell such as the one with a crown shape shows Poole-Frenkel emission characteristics. It means that a CF characteristic in LRS shows semiconducting behavior, which is suitable for low-power switching [88].



**Fig. 3.22**  $I_{RESET}$  as a function of switching area with different RRAM structures.

### 3.3 Summary

We propose a novel RRAM structure, which makes it possible to reduce the  $I_{RESET}$  by controlling the number of electrical paths and electric fields occurring at the electrode and resistive cell interface.

Areal and structural effects of proposed crown shape structure are also systematically elucidated. Compared to the conventional structure, the proposed structure is more effective in improving  $I_{RESET}$ . In particular,  $V_{SET}$  distributions and  $V_{FORMING}$  are minimized due to CF controllability and field enhancement, which are not obtainable from the large area of conventional resistive cell structure. Increase in resistance ratio implies that reset resistance may deteriorate the CF originated from set resistance.

When the cell area is decreased to the point where it is similar to CF area, it is believed that the cell area dominates the behavior of resistive switching. However,  $I_{RESET}$  distribution still exists due to process variation and its fundamental structural limit. Although obtaining the clues of scaling feasibility is possible by using this structure, a clearer evidence of  $I_{RESET}$  reduction by switching area scaling is needed.

# Chapter 4

## Highly Scaled Hole Contact Cell

### 4.1 Introduction

As we mainly considered in this thesis, high  $I_{RESET}$  level is still one of the critical issues of current unipolar RRAM research. Many researchers have competitively reported that controlling CF dimension in resistive material is one of the effective ways to control the  $I_{RESET}$  level in unipolar RRAM [4]. However, more understandings of CF's role are needed.

As we have investigated in Chapter 3, we have introduced a crown shape RRAM and have evaluated the feasibility of area scaling effect by crown shape RRAM. Particularly, highly scaled nm level of switching area has many electrical advantages of reducing  $I_{RESET}$  level due to  $A_{CF}$  control enhancement effect [23].

In this chapter, we have fabricated a highly scaled hole contact structure that makes it possible to investigate the switching area –  $I_{RESET}$  relationship in more

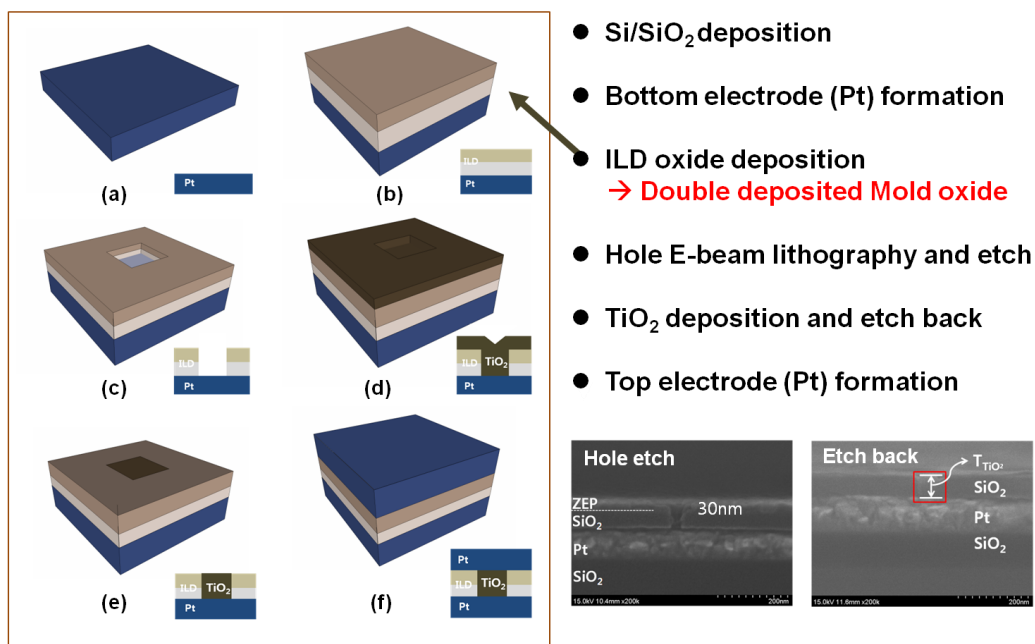
detail. There is no (or weak)  $I_{RESET}$  reduction in area scaling in large area cell due to no (or weak) CF modulation in large area cell. On the contrary, in highly scaled switching area, this tendency will be changed due to CF modulation effect. We found  $I_{RESET}$  reduction by scaled hole contact cell, and we have explained this  $I_{RESET}$  reduction with CF modulation effect. From these results, we have finally proposed CF modulation model in highly scaled RRAM cell.

While fabricating highly scaled hole contact cell, we have found that ILD deposition condition has a strong impact on the leakage current. A double-layer ILD deposition process, which is an effective method to eliminate the unwanted leakage current flow through the ILD mold oxide is performed. In order to determine the optimal dimension of resistive switching area that contributes to the improvement of  $A_{CF}$  controllability, the contact area of proposed structure is split. CF modulation in scaled cell has been verified by  $R_{ON}$  increase, which is important factor for  $I_{RESET}$  expectation in unipolar RRAM.

## 4.2 Experimental Results

Figure 4.1 depicts the schematic drawings of the process flow of the highly scaled hole contact cell structure. First, platinum (Pt) metal was sputtered on SiO<sub>2</sub>/Si wafer using the room temperature process as the bottom electrode (BE). The thickness of BE was 1000 Å. A SiO<sub>2</sub> layer as the mold oxide for defining highly scaled, small contact hole was deposited by double oxide deposition method to eliminate unwanted pin hole which is the source of leakage current on the Pt by using plasma enhanced chemical vapor deposition (PECVD). Process temperature and total thickness of doubly deposited oxide mold are 385 °C and 650 Å, respectively. Then, e-beam lithography process and the etch process were performed to define the small contact in which cell sizes were split from 80x80 μm<sup>2</sup> to 40x40 nm<sup>2</sup>. Small contact hole etch time is 16s at P-5000 equipment. We used the 80 by 80 μm<sup>2</sup> of shadow mask for top electrode formation. After that, TiO<sub>2</sub> material as the switching layer was ALD deposited at 250 °C to fill the contact hole. In order to define the contact hole, etch back process was carried out by using RIE 80 plus equipment. Finally, Pt was deposited by MHS-1500 metal sputter on the shadow mask to define the top electrode. In order to minimize the effect of top electrode size and to understand the effect of cell area, we have fixed

the top electrode size of all split cells to  $80 \times 80 \mu\text{m}^2$ . We have measured electrical characteristics of our fabricated cell by using Agilent 4156 semiconductor parameter analyzer at room temperature, where switching voltage was applied to the top electrode with the bottom electrode grounded. Other critical fabrication process steps are summarized in Fig. 4.2.



**Fig. 4.1** Illustration of fabrication process sequence and SEM image of 30nm contact size of hole contact cell.

Step #	Process	Material	Equipment	Process time	Process temp.	Target/ Data	Remark
1	Buffer oxide	SiO <sub>2</sub>	P-5000	10"	385 °C	1000 Å	
2	Glue Layer	Ti	MHS-1500	50"	room temp.	100 Å	
3	Bottom Electrode	Pt	MHS-1500 (metal sputter)	3'10"	room temp.	1000 Å	
4	ILD Oxide	SiO <sub>2</sub>	P-5000	(3.5"+3.2")	385 °C	650 Å / 680 Å	Double deposition
5	E-beam litho.	ZEP	JBX-6300FS (JEOL)	2 h	room temp.	-	
6	Mold Etch	SiO <sub>2</sub>	P-5000	16"	room temp.	-	
7	SL Deposition	TiO <sub>2</sub>	PE ALD	1537 cycle	250 °C	600 Å / 580 Å	
8	Etch Back	TiO <sub>2</sub>	RIE 80 plus (oxford)	97"	room temp.	-	
9	Top Electrode	Pt	MHS-1500 (metal sputter)	3'10"	room temp.	1000 Å	

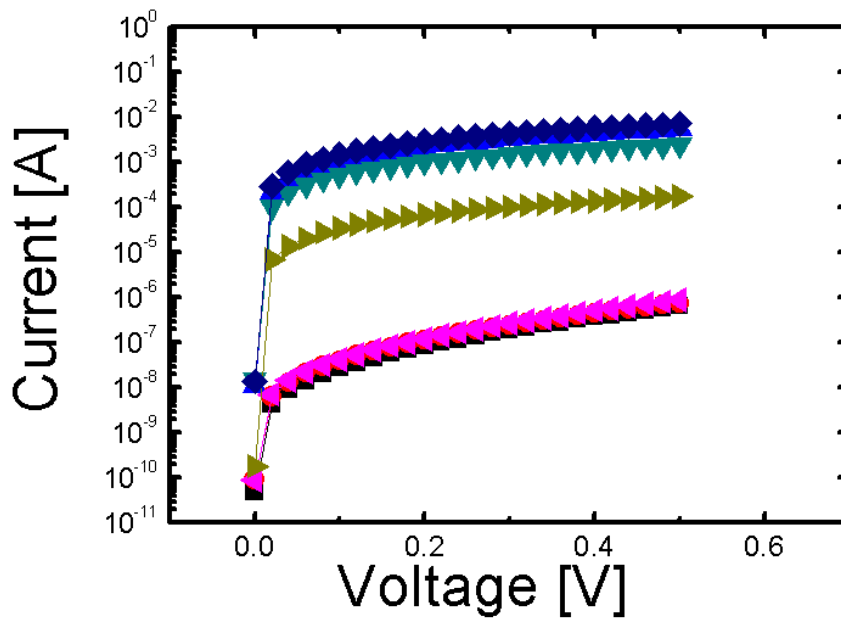
**Fig. 4.2** Fabrication sequence of hole contact cell.

In the first place, the relationship between initial voltage and current level has been identified in order to minimize fundamental process issues, especially to eliminate leakage current in electrode area and SiO<sub>2</sub> and to confirm it. Because we have used the 80x80um<sup>2</sup> area of TE by shadow mask to avoid photolithography difficulty, TE size is relatively large compared to resistive switching cell. Therefore, ILD mold oxide and large TE effect were considered. So, in order to clearly understand the area effect through highly scaled cell only, leakage current level in ILD mold oxide has been examined. Such examination can show the



effect of leakage current of mold oxide. By minimizing the electrode effect that can occur due to the relatively larger shadow mask size in such process, it can be shown that resistive switching characteristics in highly scaled cell are different from that of large cell.

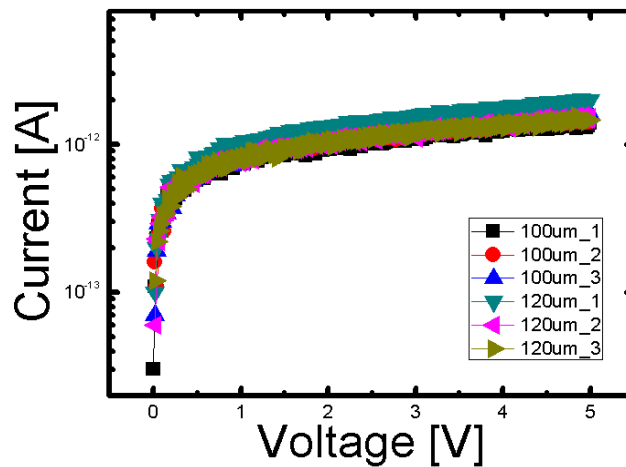
Figure 4.3 shows the initial current level as a function of voltage of ILD mold oxide. As shown in the figure below, the leakage level of ILD mold oxide was tested first to eliminate unwanted leakage current effect. The thickness of oxide mold was 500Å by single oxide deposition method. If the leakage current in mold oxide affects the resistive switching of small cell, it is very harmful for the area scaling. Therefore, effects of mold oxide quality on resistive switching should be considered first. In case of a single deposited ILD oxide mold, it is seen in the graph below that the leakage current level in the cell of the same process condition are varying widely. Leakage level under the same process condition fluctuates, and it varies from  $10^{-7}$  A to  $10^{-3}$  A at 0.2V. It means that leakage current of mold oxide should not be ignored when the singly deposited ILD mold oxide is used. Reasons for such a large leakage current seem to lie in some defects such as pinhole within ILD mold oxide. Therefore, in order to avoid such unwanted leakage current source like pinhole, a novel ILD mold oxide technique should be considered.



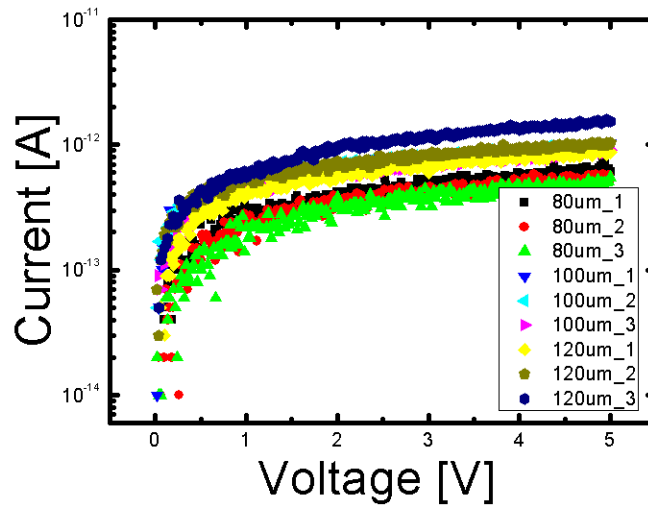
**Fig. 4.3** I-V characteristics for verifying leakage current level of single deposited ILD mold oxide.

To eliminate the leakage current of the ILD mold oxide, we have proposed the doubly-deposited ILD mold oxide method for elimination of leakage current. Figure 4.4 shows the I-V curves of doubly deposited ILD mold oxide (a) and double deposited ILD mold oxide with 10s etch back process to mimic the real fabrication condition (b). As shown in the figure below, the current at 1V is under pA level. It implies that the amount of leakage current can be ignored. As a cell with high resistance forms initially by decreasing cell area, CF dimension can be effectively controlled because it is relatively difficult to generate the excess CF

branches. Therefore, through the same phenomenon as in the case of crown shape, low  $I_{RESET}$  level can be predicted, and effective control of unnecessary external CF due to decrease in cell area can be predicted as well [33]. Also as shown in Fig. 4.5, since the leakage path can be easily blocked in doubly deposited ILD mold oxide, 50nm  $\text{SiO}_2$  can be used as an effective leakage barrier. Therefore, such process issue can be eliminated, and the current only flows through highly scaled  $\text{TiO}_2$  cell.

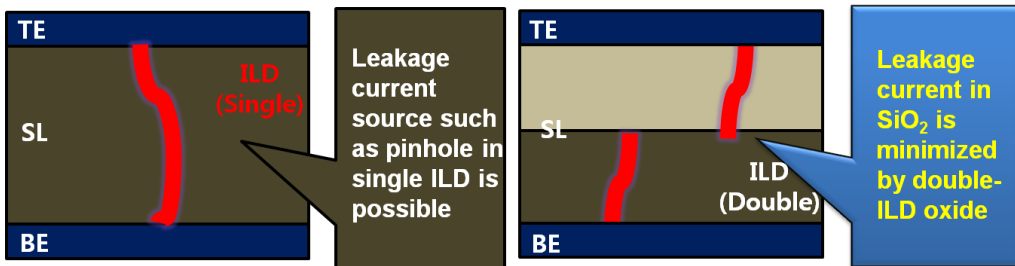


(a)



(b)

**Fig. 4.4** Leakage current level of double-deposited ILD mold oxide (a) and double-deposited ILD mold oxide with 10” etch back cell (b).

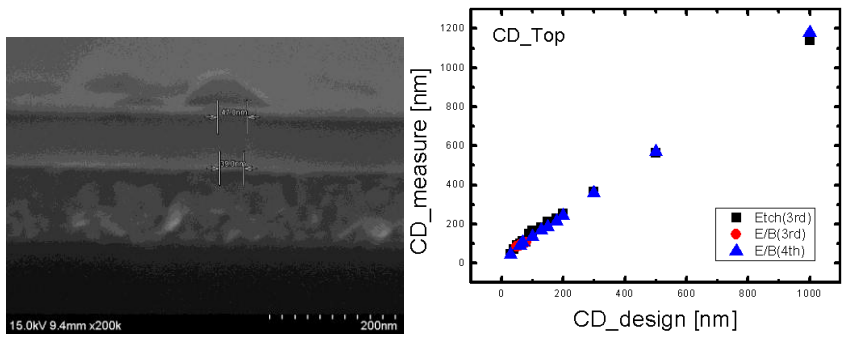


**Fig. 4.5** Illustrations of the doubly deposited ILD mold oxide effect in scaled cell.

Figure 4.6 shows the scanning electron microscope (SEM) image of highly

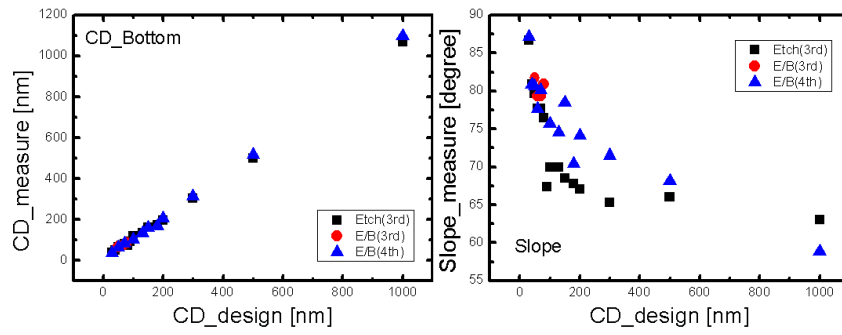
scaled contact hole structure (a), top CD (b), bottom CD (c), and their slope with different contact area (d). This value is obtained from more than 3 samples of each. Measured top and bottom CD of expected drawing 30nm CD is 46nm and 38nm respectively. Compared to expected CD, measured contact CD using SEM image is 8nm to 16nm larger.

On the average, 10nm increase in the bottom CD of hole contact and approximately 20nm increase in top CD occurred in a 40nm cell. However, as shown in Fig. 4.6 (b), drawing CD and measured CD increased in the same manner. These results shows that there is no issue to CD definition. Yet, the formation of very small contact hole of 20nm and below has not been confirmed in SEM obserbation. In order to establish smaller hole contact, additional process method such as side wall spacer porcess seems to be necessary. Also, as shown in Fig. 4.6(c), the slope of scaled hole increases as hole size decreases. For small CD size, more vertical and confined hole structure has been secured through the increase of slope. Table 4.1 summarizes this CD inspection results.



(a)

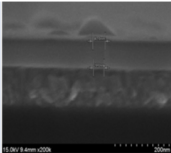
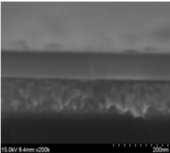
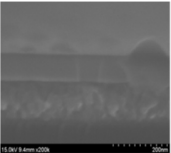
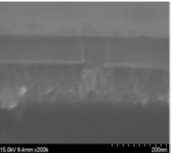
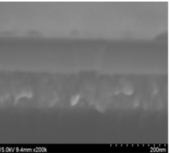
(b)



(c)

(d)

**Fig. 4.6** SEM image of highly scaled contact hole structure (a), top CD(b), bottom CD (c), and their slop with different contact area (d).

Target CD (a)	30nm	40nm	50nm	60nm	70nm
Image [SEM]					
Top CD (b)	46nm	70nm	88nm	96nm	107nm
Bottom CD (c)	38nm	48nm	66nm	67nm	80nm
Top Skew (Top-target)	16nm	30nm	38nm	36nm	37nm
Bottom Skew (Bottom-Target)	8nm	8nm	16nm	7nm	10nm
Skew (Top-Bottom)	8nm	22nm	22nm	29nm	37nm
Slope	87°	81°	81°	78°	79°
Shape	Cylindrical	Trapezoidal	Trapezoidal	Trapezoidal	Trapezoidal
Step	After oxide etch After TiO <sub>2</sub> etch back	After oxide etch After TiO <sub>2</sub> etch back	After oxide etch After TiO <sub>2</sub> etch back	After oxide etch After TiO <sub>2</sub> etch back	After oxide etch After TiO <sub>2</sub> etch back

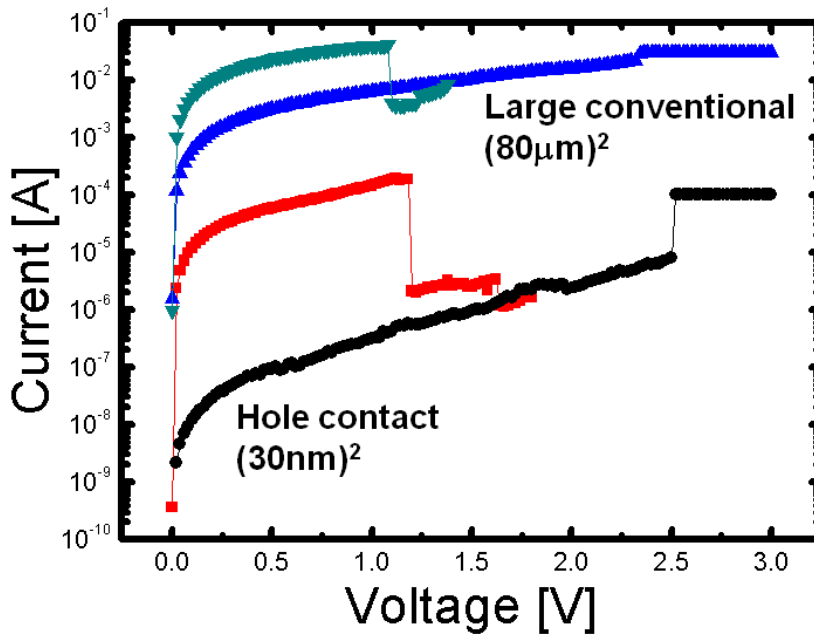
**Table. 4.1** Summary of the hole contact CD inspection results.

Figure 4.7 shows the current – voltage curve with different cell area. As shown in Fig. 4.7,  $I_{RESET}$  of 300 $\mu$ A at 2.5V was measured in 40nm<sup>2</sup> hole contact cell. Compared to 80x80 $\mu$ m<sup>2</sup> cell,  $I_{RESET}$  decreased more than 2 orders of magnitude. There may be a distribution issue in some cells because resistive switching is not well-observed due to some fabrication issues. However, such distribution characteristics are also observed in large area cells. Therefore, it seems to arise from irregular TiO<sub>2</sub> characteristics from fabrication rather than from the effect of area scaling. Most working cells showing low  $I_{RESET}$  under 1mA were obtained in

case of scaled cell.

It implies that tiny CF can be formed in a highly scaled switching area, and it also means that identifying area in which security of cells holding very small switching energy is possible. Also as in the case of crown shape cell previously mentioned, increase in  $V_{RESET}$  as well as decrease in  $I_{RESET}$  appear as the area decreases. It can be interpreted as in the previous case: along with formation of very thin CF involved in switching, heat efficiency of CF to disconnect such CF decreases as area decreases. and it can be understood that such effect increases  $V_{RESET}$ . However, such event is slightly different in each cell, and it can be defined that along with process conditions, various process variables other than intrinsic area effect issue for effective CF control involved in switching remain as in previously produced crown shape. Therefore, studies in such perspective are required.





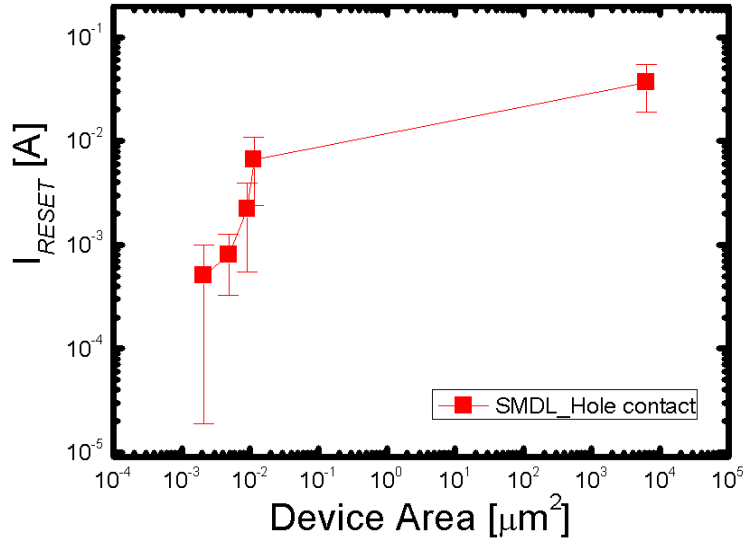
**Fig. 4.7**  $I_{RESET}$  scaling effect of highly scaled hole contact cell.

Figure 4.8 shows the  $I_{RESET}$  scaling trends as a function of switching area (a) and its comparison table (b). We can verify from the results that  $I_{RESET}$  is drastically reduced as the cell area is reduced down to  $80 \times 80 \text{ nm}^2$  region. In this figure, total area of CF generated from resistive switching as cell area is reduced from  $6400 \text{ } \mu\text{m}^2$  to  $0.0009 \text{ } \mu\text{m}^2$ ,  $I_{RESET}$  is reduced from  $36 \text{ mA}$  to  $500 \text{ } \mu\text{A}$ . Although we were not able to find the inflection point of  $I_{RESET}$ , we can explain the CF modulation in

scaled cell area. Assuming that a CF of 10nm is formed in a 1 $\mu$ m cell, the area which the CF occupies in the entire cell area is insignificant. However, assuming that a CF of 10nm is formed in a 50nm cell, the area which the CF occupies in the entire cell area is significant enough. In addition, the fact that  $I_{RESET}$  decreases as area decreases becomes more significant as it moves to sub-100nm region.

Distribution of  $I_{RESET}$  is not effectively reduced . It may be explained by the fact that our minimum scaling area is 30x30nm<sup>2</sup> in design size which might be too large for full CF modulation. Because CF size in TiO<sub>2</sub> resistive cell is only 3-10nm near the anode,  $I_{RESET}$  fluctuation can be still dominant in this 30x30nm<sup>2</sup> cell size.

In addition, measured top contact dimension (CD) of minimum size of 30nm<sup>2</sup> cell is larger than designed CD due to the difficult contact-defined etch process, and, for this reason, fully controlled CF modulation is impossible in this scaled region. However, clear scaling effect is observed in under 80x80nm<sup>2</sup> cell. It means that CF modulation happens in this scaled area of 80x80um<sup>2</sup> though more scaling is still needed.



(a)

	$(80\text{nm})^2 \rightarrow (30\text{nm})^2$	$(80\mu\text{m})^2 \rightarrow (80\text{nm})^2$
$A_{CELL}$	7.11	1000000
$I_{RESET}$	11.39	5.59

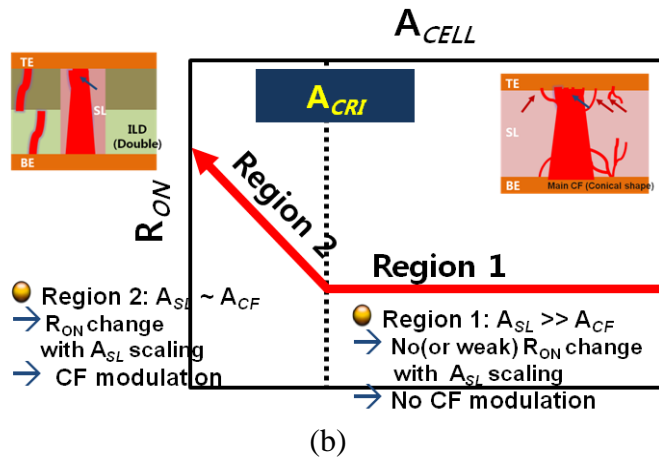
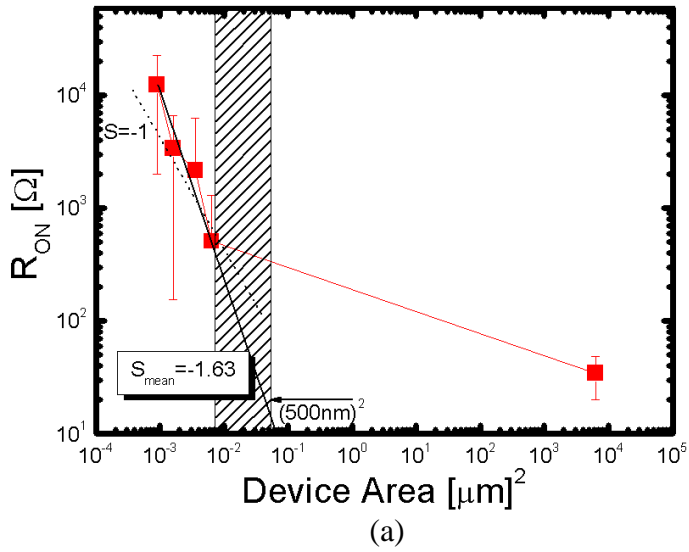
(b)

**Fig. 4.8**  $I_{RESET}$  scaling trends (a) and scaling as a function of switching area and area- current comparison table (b).

Figure 4.9 shows the  $R_{ON}$  as a function of contact area with various contact area (a) and illustration of area scaling (b). As in the figure below,  $R_{ON}$  can predict formed CF.  $R_{ON}$  drastically decreases in the area  $80 \times 80 \text{nm}^2$  and below as shown, through which it has been verified that CF rapidly affects area in certain critical

area. In this experiment,  $R_{ON}$  is drastically increased under  $80 \times 80 \text{ nm}^2$  area of cell size and below. Especially, in our measured minimum CF region of  $30 \times 30 \text{ nm}^2$ ,  $R_{ON}$  is rapidly increased. It means that CF modulation is quite active in this highly scaled area.

However, as in the case of crown shape cell, such tendency does not appear in all cells, which means that other variables still exist other than area. Therefore, decrease in  $I_{RESET}$  has been verified as area decreases, but decrease in CF has been more precisely identified by the increase in  $R_{ON}$ , and rapid increase in contact area of approximately  $30 \times 30 \text{ nm}^2$  has been verified. Detailed verification through acquisition of large amount of working cell seems to be needed in future research. However, increase of  $R_{ON}$  in local area has been clearly identified, and it seems that rapid increase of  $R_{ON}$  in specific area indicates that a specific switching area in which CF is affected exists. We estimate by extrapolation of slope of scaled cells as shown in Fig. 4.9 (a) that critical CF modulation occurs when the area is less than  $500 \times 500 \text{ nm}^2$ . Unfortunately, we do not know exactly where CF modulation starts, due to the absence of medium cell size. However, from the extrapolation method using the calculation of slope of measured scaled cells, we can estimate the CF modulation area.

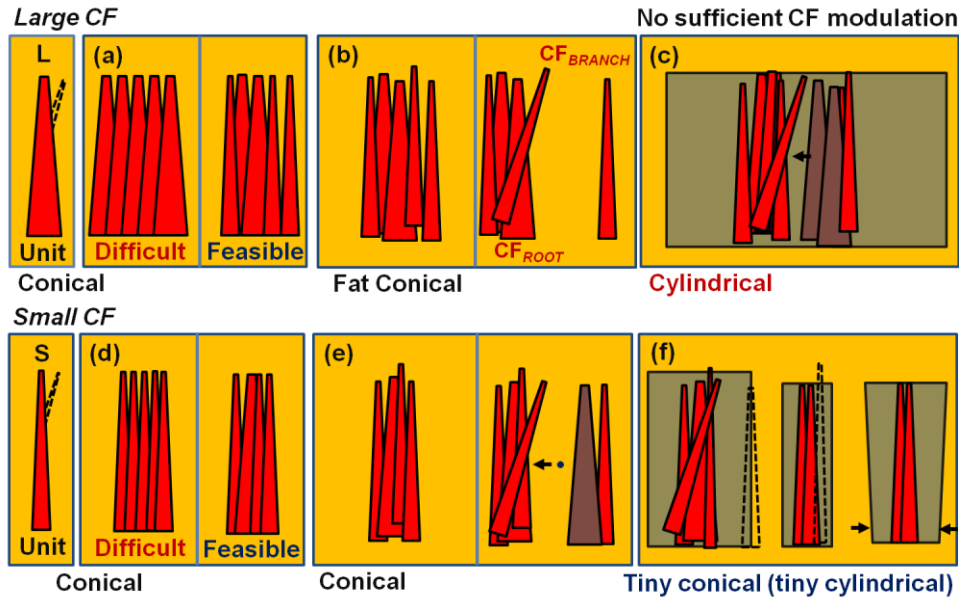


**Fig. 4.9** Statistical analysis of  $R_{ON}$  as a function of contact area (a) and illustration of  $R_{ON}$  increase with switching area (b).

Figure 4.10 illustrates the CF modulation due to area scaling. In the first stage, we assume that there are two CFs with different sizes. As shown in the Figs. 4.10 (a) and (d), a structure in which single CF repeats will occur when CF is

multi-filament shape. In the case of  $\text{TiO}_2$ , single filament is in a conical shape as Kim, et al. reported [93], therefore, will be shaped as in Fig. 4.10 (a). However, it is difficult for the filament of the same size to be repeatedly formed as in Fig. 4.10 (a). Therefore, it may be more feasible for CFs with different thickness to be mixed as in Fig 4.10 (a) and (d). However, CF in this case will also be in a conical shape. As shown in Figures 4.10 (b) and (e), CF can be formed randomly, or another single CF can be formed due to the Schottky barrier in another cathode site becomes lower for some reason. (Although unit CF may be different in shape and thickness, they will be in a similar trend). As switching is repeated, CFs around anode side will run into and fall apart from each other, creating a shape in which thick and thin CFs are mixed. This explains the formation of branch filament in anode interface. The number of CF increases even more in a large area, creating a cylinder-shaped CF that  $R_{ON}$  resistance is low, making it difficult for decrease in  $I_{RESET}$  and CF modulation. CF displays localized switching in this case as well, but CF area drastically increases for some complicated reason, making control difficult. However, if the switching area decreases, either additional formation of CF can be controlled or it becomes possible to make CF thinner. In turn, CF modulation becomes possible through which  $I_{RESET}$  is reduced. Eventually, CF path can be reduced by the area effect, and controllability can be

increased.



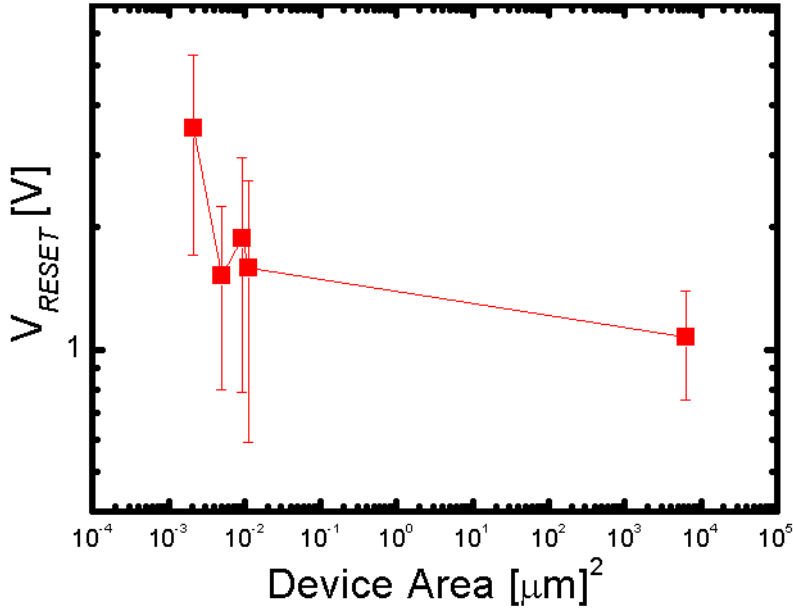
**Fig. 4.10** Simple illustration of CF modulation model in  $\text{TiO}_2$  cell.

Figure 4.11 shows the 10 cells of  $V_{RESET}$  characteristics as a function of switching active area. As shown in Fig. 4.10, the  $V_{RESET}$  is increased as the active area is decreased in the highly scaled hole contact cell structure. This indicates that the contact dimension plays an important role in CF geometry, so it can easily control the initial CF dimension in the sub-100nm region. A large  $V_{RESET}$  is needed in the case of scaled cell owing to its relatively poor heat efficiency of the CF for rupturing due to relatively tiny CF formation. Because a higher thermal

energy can disconnect the CF more easily, the  $V_{RESET}$  can be increased, which could lead to the CF rupturing in scaled cell area. However, it will change the CF conditions such as CF shape and number originated from their material-related characteristics. Cheng, et al. has recently reported that CF shape of  $TiO_2$  is generally conical in a large area cell [12]. In case of proposed scaled hole contact cell, CF shape can be changed from large number of conical shape to small number of more tiny conical shape due to the reduction of resistive switching area. Particularly in the case of conical shape of CF, CF size reduction of cathode side will be accelerated due to the asymmetric etch profile of the scaled cell. Therefore, tinier conical shape (or more cylindrical shape) with lower number of CF is generated in initial CF forming, and CF rupturing in reset process is more plausible. As CF size decreases in scaled hole contact cell, the shape of CF may change to tinier conical shape due to Joule heating, possibly moving the rupturing point from the interface area to the center of the cell. Therefore, it seems that distribution issues in unipolar RRAM can be improved by switching area reduction. However, there are still lots of resistive switching variation sources such as grain boundary effect, film defect, and roughness effect [67]. Especially as memory density increases, operation margin reduces due to cell-to-cell variation issue in unipolar RRAM. Therefore, such switching voltage value should be



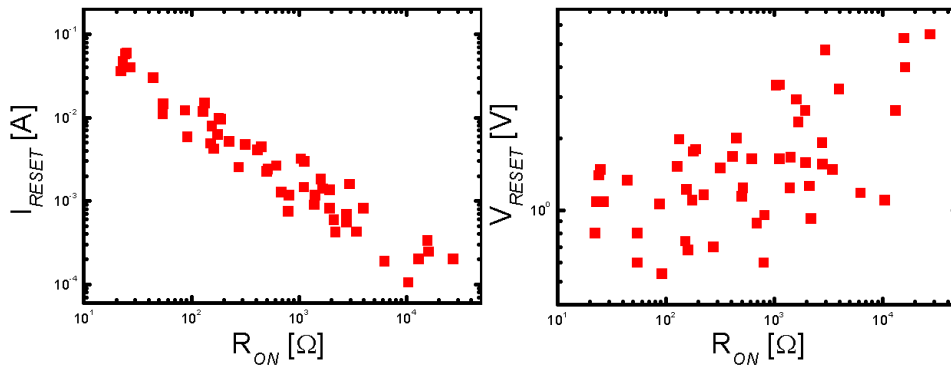
well-defined for mass production. Further intensive study is still needed to resolve such switching voltage distribution issues based on the CF theory.



**Fig. 4.11**  $V_{RESET}$  as a function of device area.

Figure 4.12 shows the  $R_{ON}$  dependency with  $I_{RESET}$  (a) and  $V_{RESET}$  (b). Over 50 cells are measured to explain their relationships. It is an important and powerful factor to determine the  $I_{RESET}$ .  $I_{RESET}$  decreases with increasing  $R_{ON}$  as shown in Fig.4.12 (a), and it signifies that CF modulation is possible in scaled cell area because of correlative  $I_{RESET}$  reduction. Understandings of  $V_{RESET}$  dependence on  $R_{ON}$  are still controversial due to the broad distribution of  $V_{RESET}$  as a function of

$R_{ON}$ .



**Fig. 4.12**  $I_{RESET}$  (a) and  $V_{RESET}$  (b) data as a function of  $R_{ON}$ .

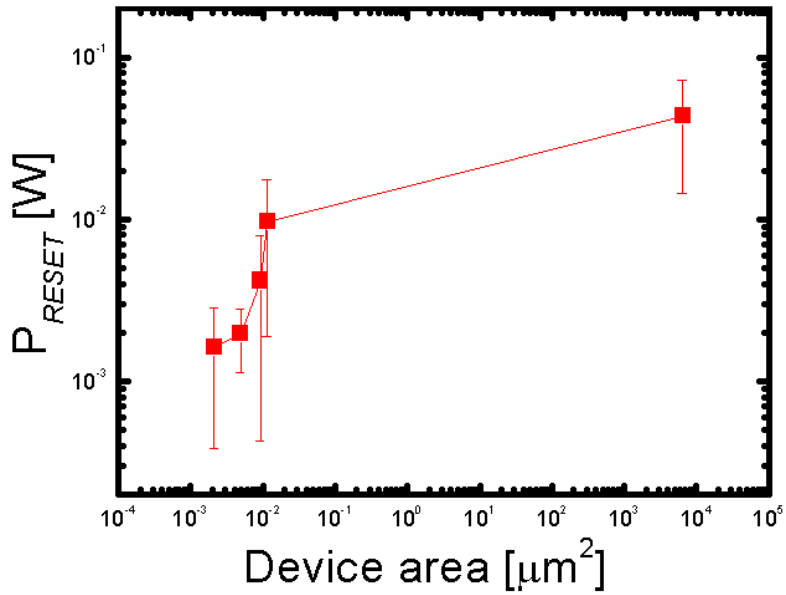
Figure 4.13 shows the  $P_{RESET}$  (a) and  $I_{RESET}$  (b) scaling tendency as a function of contact area with various structures.  $I_{RESET}$  reduction in various areas has been identified, so that the understanding of area effect is possible. As shown in the figure below, decrease of  $I_{RESET}$  for cell sizes from tens of  $\mu\text{m}$  to hundreds of nm is not significant compared with the decrease in area. This result supports previously mentioned theory as well as various other published studies. In other words, it is difficult to expect area effect in  $\mu\text{m}$  level cell area larger than which CF is involved in resistive material in which switching occurs in extremely local area. However, as the area decreases under sub-100nm level, such effect dramatically decreases  $I_{RESET}$ . In other words, scaling effect increases towards a very small size

which affects CF size and branch, therefore  $120\mu\text{A}$  level of  $I_{RESET}$  is obtained in area of  $30\text{nm}$  as shown below. It means that CF is more effectively controlled in a highly scaled cell.

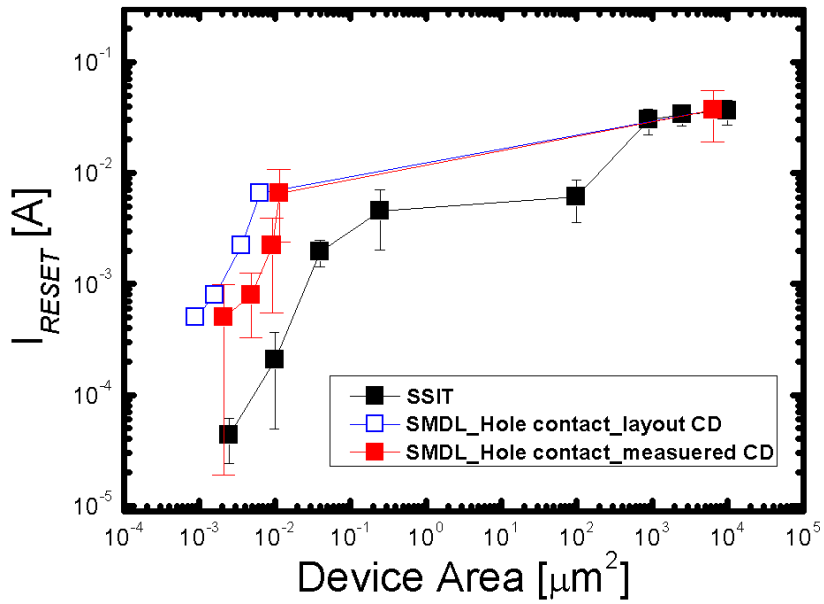
The development of improved low-power RRAM is possible through structural approach for future RRAM studies, through which a new direction significant in high-density and low-power RRAM can be proposed [see Fig. 4.13 (a)]. However, as in Fig. 4.13 (b), clear  $I_{RESET}$  reduction tendency is visible in small contact area, yet their distribution is still large. Such distribution is quite irregular and difficult to predict, and it seems to be an issue arising either from production of switching material such as  $\text{TiO}_2$ , or from other fabrication process. This distribution is indifferent to contact area especially in maximum value, and it seems to be an issue related in part to oxide quality around the scaled cell. Therefore, in order to resolve such an issue, a method to improve process for better distribution and to effectively control the cell area in small area should be proposed.

Moreover, further process improvement for more scaled switching area formation is needed. Our minimum scaled contact hole area is  $30 \times 30 \text{nm}^2$ . In this area region, complete  $A_{CF}$  control is still difficult due to the relatively large switching area compared with CF dimension. In addition, CF branches at switching interfaces still exist, which may affect the large  $I_{RESET}$  and resistive

switching distribution. Therefore, further scaling of hole contact area is required to obtain the complete CF modulation. Side-wall spacer process will be one of the effective methods to reduce the contact hole size.



(a)



(b)

**Fig. 4.13**  $I_{RESET}$  (a) and  $P_{RESET}$  (b) scaling tendency as a function of different switching area and structures.

### 4.3 Summary

We have fabricated highly scaled hole contact structure, which makes it possible to reduce the  $I_{RESET}$  by controlling the number of electrical paths and electric fields occurring at the electrode and resistive cell interface.

Particularly, such decrease in  $I_{RESET}$  accelerates as the switching area is scaled down. Also decrease of  $I_{RESET}$  as a function of  $R_{ON}$  is found. It appears that the decrease in CF area contributes to  $I_{RESET}$ . From the  $R_{ON}$  data with scaled cells with different contact area, we have extracted plausible CF modulation area. Effective reduction of CF in a very small cell is also identified in more detail without leakage current issue. However, switching distribution still exists. It is still difficult to reduce hole size due to various process issues. Therefore, further research is needed to accomplish complete CF modulation effect.

Nevertheless, the obtained characteristics impl that, for future research of scaled RRAM, production of RRAM with high-density and low-power at the same time is possible. This strongly supports the arguments that RRAM may be able to replace current conventional memories.

# Chapter 5

## Conclusion

Needs for high-density and low-power unipolar RRAM has been increasing for information technology (IT) application. Therefore, understanding basic characteristics of CF-based unipolar RRAM and their scaling effects are one of crucial tasks for RRAM research. However, there are electrical and physical limitations due to lack of understanding of CF-based switching characteristics and absence of the correct memory scheme. Highly scaled cells such as crown shape cell and hole contact cell are used and characterized in this thesis to elucidate the CF modulation which is a very important mechanism for low-power unipolar RRAM. By reducing switching area with highly scaled RRAM structures, it is expected to reduce  $I_{RESET}$  and power consumption, so that we are able to explain the switching scaling effect on CF modulation.

Scaled RRAM cells have high  $R_{ON}$  states because of the small number of switching-related CF. In this case as clearly seen in our results,  $R_{ON}$  is relatively

high compared with the conventional structure, having advantages in  $I_{RESET}$  due to tiny CF formation in initial state. Overall switching power is effectively decreased in proposed scaled cells even with the increase in  $V_{RESET}$ .

We expect that the progression of low-power unipolar RRAM will be further accelerated once a simple fabrication process is established along with the development for high-density memory application.



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## 초 록

저항 메모리는 여러가지 물질의 고유한 특성을 메모리 연구에 이용하고자 하는 연구방향에서 착안된 메모리로, 현재 그 잠재적인 다양한 장점으로 인하여 향후 기존의 메모리를 대체할 수 있는 유망한 메모리로 관심과 함께 다양한 방법론적인 방법에서의 접근이 시도되고 있는 메모리 연구분야이다. 하지만 아직 저항메모리는 다양한 물질의 동작 메커니즘을 비롯한 물리적인 특성에 대한 연구가 미흡하여, 기본적인 특성에 대한 연구가 아직 미진하며, 따라서 이러한 부분에 대한 다양한 연구 방법 및 방향이 명확하지 않아, 연구에 어려움이 있다. 특히 저항 메모리가 기존의 메모리들을 대체하기 위해서는 먼저 다양한 물질의 동작 메커니즘과 함께, 이러한 동작 전류의 감소를 통한 소비전력의 감소가 이루어져야 하며, 이를 통해 고집적 저전력 메모리로서의 가능성에 대한 다양한 연구 및 증명이 선행되어야 한다.

본 연구에서는 저항메모리 소자에 대한 기본적인 쓰기/지우기 동작 특성의 개선을 통한 새로운 메모리로서의 가능성에 대해서 제시하고 이를 위해 전도성 필라멘트를 효과적으로 제어할 수 있는 구조의 제안을

통해 이를 증명하였다. 먼저, 저전력, 고집적화가 가능한 단극성 저항 메모리의 특징을 살펴본후, 단극성 저항 메모리가 가지는 단점인 높은 쓰기전류 및 산포에 대해서 확인한후, 이러한 특성의 원인이 스위칭 동작에 관여하는 전도성 필라멘트의 형성 및 형태, 면적등의 요소와 이와 연계된 메커니즘과 관련이 있음을 설명하였다. 특히 이러한 메모리 동작에 관여하는 전도성 필라멘트의 다양한 제어기구를 단일소자와 제안된 이중층을 가지는 저항메모리를 통해 확인한후, 이러한 전도성 필라멘트와 쓰기면적의 감소와의 관계에 대해서 고찰하였다. 이러한 전도성 필라멘트의 감소를 통한 저전력 쓰기동작이 가능함을 면적을 효과적으로 제한할 수 있는 제시된 두가지의 국소화 면적 구조를 통해서 검증하고, 이를 통한 면적과 전도성 필라멘트의 형성기전에 대해서 설명하였다. 해당 구조를 통해서 향후 고집적화를 위한 저항층의 면적감소는 동작특성에 관여하는 전도성 필라멘트의 양과 모양을 보다 저전력에 동작 가능한 형태로 변형시켜, 이를 통한 고집적 저전력화의 동작이 가능함을 설명하였고, 특히 이러한 단극성 저항메모리에서 주울 히팅에 의한 전도성 필라멘트의 끊어짐 현상을 설명할 때, 실험결과와 보다 일치하는 결과를 도출할 수 있음을 확인하였다.

이 논문에서 제시한 구조와 제반 분석에 관한 연구는 새로운 저항 메모리의 저전력 고집적화에 있어 이의 가능성을 보다 실증적으로 예측할 수 있는 토대를 마련해주며, 근래 및 가까운 미래에 개발될 저항메모리의 저전력화를 통한 효과적인 양산화에 있어, 효과적인 방향을 제시할 수 있는 방법과 토대에 근거한 연구 결과를 제시한다.

주요어: 뉴메모리, 저항 메모리, 저항성 스위칭, 단극성, 면적감소, 전도성 필라멘트, 쓰기전류, 크라운 구조, 홀 컨택구조

학번: 2008 - 30129

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