**M.S. THESIS**

# A Highly Efficient Average Power Tracking Power Amplifier with CMOS Controlled GaN HEMT Supply Modulator

CMOS로 제어되는 GaN HEMT Supply Modulator를
이용한 고효율 Average Power Tracking 전력 증폭기

BY

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# Abstract

In this thesis, an Average Power Tracking (APT) system of a Power Amplifier (PA) using Cree Inc. CGH60 series GaN HEMT bare die is presented. IBM 0.18um SOI 2.5V RF technology is used to fabricate control circuits in supply modulator.

A Class $E^2$ DC-DC Converter is adopted as the supply modulator. Both Class-E inverter switch and Class-E rectifier switch uses GaN HEMT as a switch. Both switches are controlled by Pulse Width Modulation (PWM) generated by CMOS control circuit. The peak efficiency is 85% at 31V of output voltage with 0.5 duty cycle of 1MHz PWM when 28V is supplied.

Highly efficient 5.8GHz 2-Stage Class-E Power Amplifier is realized with GaN HEMT device. Numerical analysis has performed for initial design of PA then the ideal lumped elements are replaced with microstrip lines. The measurement results show the maximum PAE of 63.9% at 39.0dBm of output power with 15.8dB gain. The maximum power-stage drain efficiency is 76%

Average Power Tracking is applied in order to increase power-stage drain efficiency at back-off power. The system shows 1% of drain efficiency increment at 6-dB back-off and 5.7% increment at 9-dB back-off power. Since the supply modulator boosts up to 32-V, the maximum output power is increased to 38.7dBm from 37.9dBm.

Pulse Width and Frequency Modulation (PWFM) control method is introduced in place PWM control in supply modulator. The new supply modulator shows 11% of efficiency increment at 12V resulting in higher than 70% of efficiency over wide output voltage range. When Average Power Tracking is applied with the same PA, the peak PAE of 49.5% at 39.6dBm with gain of 15.6dB is resulted. At 6 dB and 9 dB back-off power, 4% and 3.5% of PAE is increased.

**Keywords:** Average Power Tracking (APT), Class-E Power Amplifier, Class $E^2$ DC-DC converter

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# 1. Introduction

A highly efficient Power Amplifier (PA) is a key element for the modern communication system because the PA is the most power consumer in the RF front end. This presents special challenge to the design of high-efficiency PA due to a wide range of peak to average power ratio (PAPR) of the transmitted signals. For example, W-CDMA downlink signal has a PAPR as high as 9dB translates into low efficiency of PA. Bias modulation techniques, especially Envelope Tracking (ET) and Envelope Elimination and Restoration (EER) have been widely investigated to enhance the back-off power efficiency.

Gallium Nitride (GaN) has been regarded as a promising device for the next generation because it has high breakdown voltage, high power density, and high efficiency. Highly efficient watt-level GaN PAs are reported in [1-6], mainly by using switching mode or adequate harmonic termination for high peak efficiency. Also, the mostly linear drain-to-source capacitance of the GaN device makes it more attractive for supply modulation because this nature guarantees high peak efficiency over various supply voltages. Therefore, a few supply modulation techniques using GaN PA are recently reported in [7-8].

A typical supply modulator consists of a linear stage and a switcher stage. Both of these components are achieving high efficiency and fidelity individually. However, this topology has two main problems. The first one is the in-band switching noise deteriorating adjacent or alternative channel mask requirements. Moreover, because of the large output capacitances of the PA and the supply modulator, phase margin issue is arisen which limits operation bandwidth.

A switching mode supply modulator, only using a high speed switching DC-DC converter is rising for substitution. If higher switching frequency is allowed, the switching noise exists farther away from the carrier frequency and can easily suppressed by a filter. Also, the bandwidth of the supply modulator is now the only the function of the switching frequency. Recently, a few switching mode GaN DC-DC

converter for envelope tracking has been reported in [7-8]. As reported, to demonstrate a conventional buck converter with GaN, gate driver to control the switch is essential. However, this results in suffer from low efficiency due to gate driver power consumption.

In near future, fabrication technology will evolve to fabricate GaN and Complementary Metal-Oxide Semiconductor (CMOS) on one wafer enabling System on Chip (SoC). As a result, a single chip can handle the circuit where one part of it requires specified advantages of GaN, such as high efficiency, high voltage breakdown, and high power density while the other part requires CMOS advantages, small, high speed logic circuit.

In this thesis, the Average Power Tracking (APT) PA system using commercial GaN HEMT from Cree Inc. and IBM 0.18 um SOI CMOS process is demonstrated as shown in Figure 1. The supply modulator having 1MHz switching frequency adopts the topology of Class $E^2$ DC-DC converter and is controlled by a CMOS chip which consumes low power. In Chapter 2, principle of operation for a Class $E^2$ DC-DC converter, Pulse Width Modulation (PWM) control method, CMOS design, hybrid implementation and measurement results will be discussed while Chapter 3 discusses the topology of Class-E PA, design procedures, hybrid implementation and measurement results. Based on the implementation in Chapter 2 and 3, the overall APT PA system is realized to increase Drain Efficiency (DE) of PA at back-off power and is discussed in Chapter 4. A newly introduced Pulse Width and Frequency Modulation (PWFM) control method for the supply modulator is introduced in Chapter 5 leading to higher efficient APT PA system.

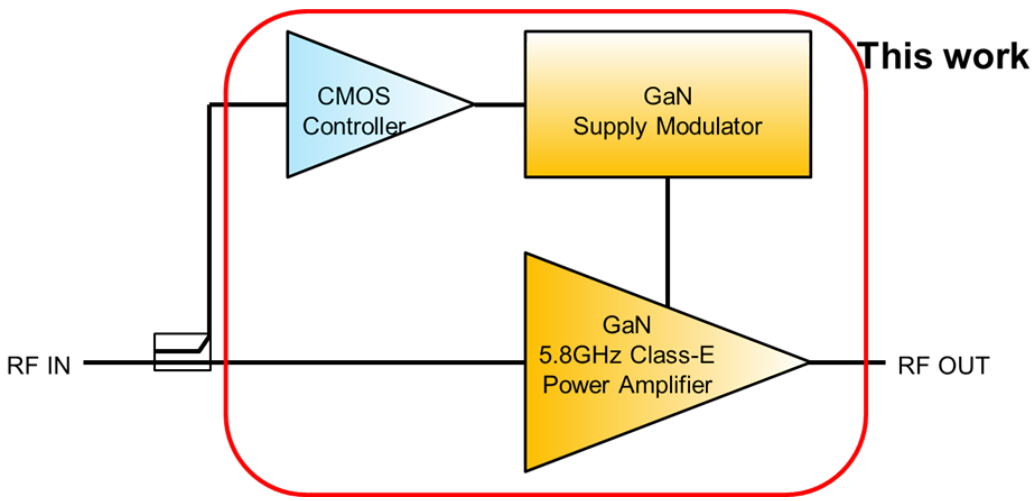



**Figure 1 Overview scheme of this thesis.**

# 2. Supply Modulator

## 2.1. Introduction

Gallium Nitride (GaN) High Electron Mobility Transistor (HEMT) Power Amplifier (PA) requires a typical value of 28V supply voltage. Thus if a modulator wants to be used, it should be able to produce at least 28V in order to modulate supply voltage of the PA. The most widely used modulators are known as DC-DC converters, such as buck converter, boost converter, cuk converter, and SEPIC converter. However, those converters consists of at least one series switch. It is not the problem when the GaN HEMT transistor is used as a series switch, but careful attention is required when its source swings from ground to 28V. It is known that the GaN HEMT operates when the gate-to-source voltage is in the range of -10V to 2V. The DC-DC converters listed above needs at least a series switch with its either side of drain or source tied to supply and the other to the output where 0 to 28V swing is produced. In order to control the series switch, the gate of the transistor should be fed by -10V to 30V. It is reckless to make a switch controller handling such large voltage because the power consumed by the controller would not be able to ignore. As a result, a topology for a DC-DC converter with only shunt switches is desired.

One solution to this is a Class $E^2$ DC-DC Converter. It consists of one shunt switch and a shunt diode. Since one side of both switches is tied at ground, the gate-to-source voltage can be in a small range – just enough to turn on and off the transistor completely. This topology has very strong advantages that the switch may be used with GaN HEMT and since its gate control can be done with small voltage range, Complementary Metal-Oxide Semiconductor (CMOS) circuit can fully handle it. The use of CMOS circuit as a control circuit in a supply modulator is the greatest advantage since CMOS technology now is unbelievably optimized to the digital logic circuit; fast, cheap, and small. Another advantage of the Class $E^2$ DC-DC Converter over typical buck converter is the availability of high switching frequency. The output of the buck converter is precisely defined as square wave which is hard to achieve

when switching frequency is over 200MHz due to the parasitic capacitances of power transistors. However, because the principle of the Class $E^2$ DC-DC Converter is zero voltage switching (ZVS) by using the parasitic capacitances - surely, additional shunt capacitor can be used, this type of the converter has a potential to work with higher switching frequency than the buck converter. With the advantage of GaN HEMT and CMOS technology, this topology will result in a highly efficient supply modulator.

The overview of the proposed Class $E^2$ DC-DC Converter is depicted in Figure 2. In this chapter, a CMOS control circuit is designed and fabricated. With the fabricated CMOS, hybrid supply modulator with GaN HEMT as switches is implemented.

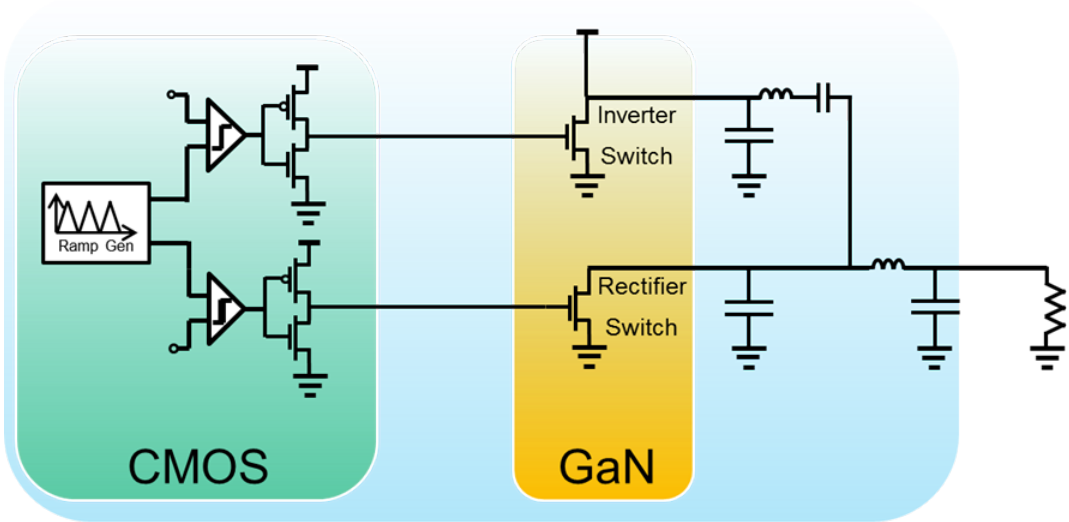



**Figure 2 Overview of the Class $E^2$ DC-DC Converter.**

## 2.2. Class $E^2$ DC-DC Converter

Overall schematic of a Class $E^2$ DC-DC Converter is illustrated in Figure 3. It consists of two main parts; Class-E inverter and Class-E rectifier. Basically, the Class-E inverter produces a current sine wave from the DC power supply and transfers to the Class-E rectifier and the rectifier produces DC current again with the sine wave obtained from the inverter.

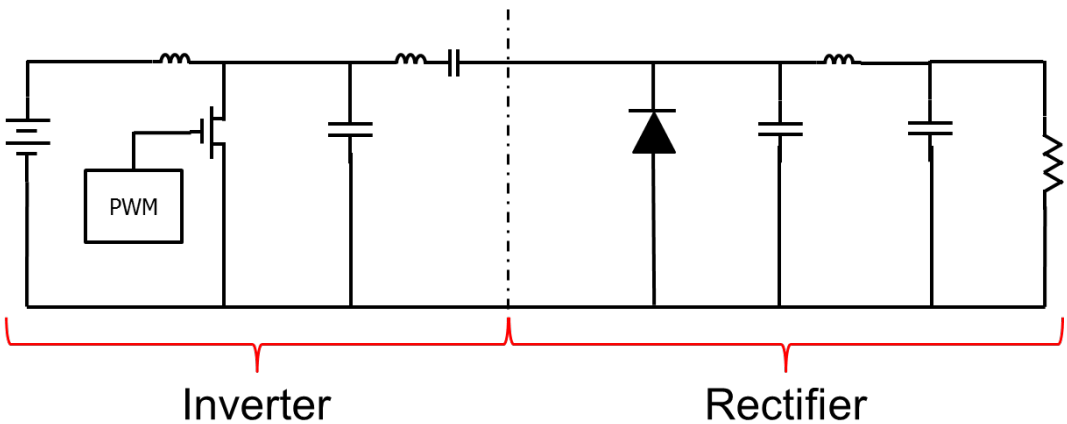



**Figure 3 Overall Schematic of the Class $E^2$ DC-DC Converter.**

The Class-E inverter consists of four major elements; an inductor, a shunt switch, a shunt capacitor, and a series LC resonant circuit. To explain how the inverter works, assume the inductor having a very large value so that it forces the current from the power supply direct current (DC). The series LC resonant circuit produces alternating current (AC) according to its resonant frequency. Thus, by Kirchhoff's Current Law (KCL), the sum of current flowing through the shunt switch and the shunt capacitor is equal to the difference of DC from the power supply and the AC passing through the LC resonant circuit.

If the switch is on for half time of the period, the current will flow to ground

through the switch and is shown as red line in Figure 4. During the other half of time, the switch is turned off and the current flows to the shunt capacitor, shown as blue line in Figure 4. When the current flowing into the capacitor is positive, it will charge the capacitor and if the current flowing into the capacitor is negative, it will discharge. When charging the capacitor, the voltage level increases as shown in Figure 5. When the current flowing into the capacitor turns negative, at 1.00065ms in Figure 4, the capacitor starts to discharge as the slope starts decreasing in Figure 5. At the time when the polarity of current changes from negative to positive, the capacitor is fully discharged and starts charging again as current becomes positive. With the voltage swing produced, the power is transferred through the LC resonant circuit to the Class-E rectifier.

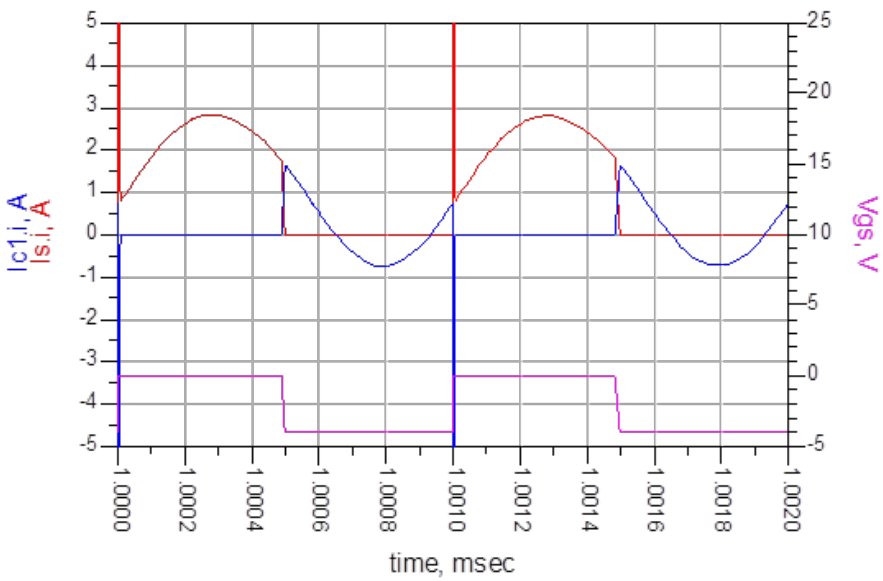



**Figure 4 Current waveform. Red line shows the current through the inverter switch and blue line shows the current through the shunt capacitor. Pink line shows the voltage waveform at the gate of the inverter switch.**

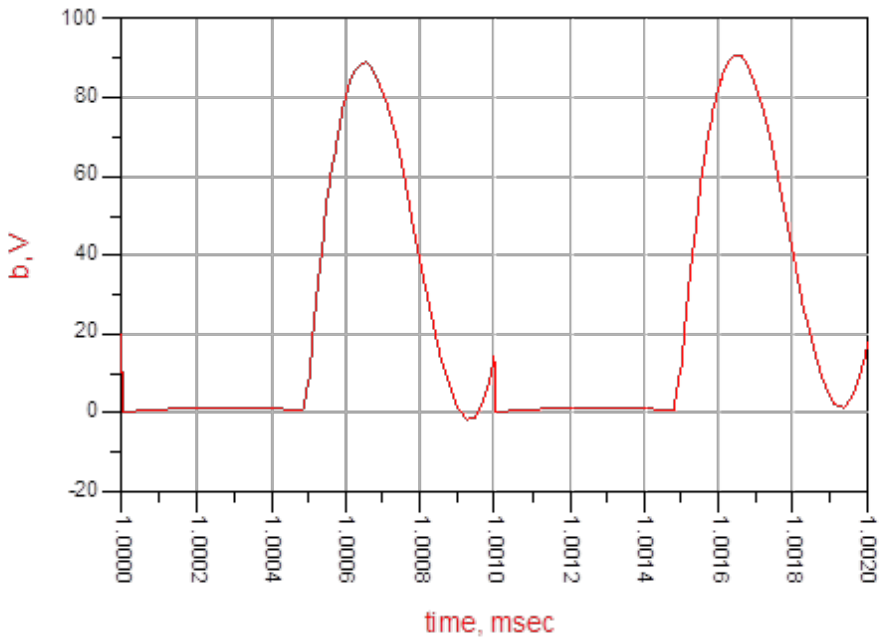


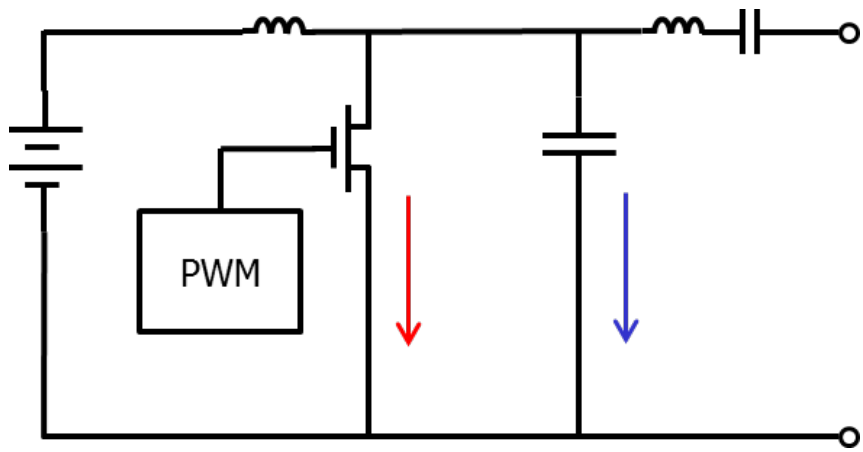

**Figure 5 Waveform of voltage charged by the shunt capacitor in Class-E inverter.**

For Class-E rectifier, it consists of a shunt diode, two shunt capacitors, and an inductor. To demonstrate its operation, assume AC is coming in from the end of inverter due to the series LC resonant circuit. Referring to Figure 3, if the inductor in the rectifier is quite large, a DC will transfer through the inductor. As in the inverter, the sum of current passing through the diode and the shunt capacitor next to the diode is equal to the difference between the sine wave current from inverter and the DC going out through the inductor. As the current sine wave is coming into the rectifier, the shunt capacitor charges when the current level is positive and starts discharging itself when the current level turns negative from positive. At the point where the current wave hits its maximum negative value, the capacitor is fully discharged. As the current wave slope turns positive right after the maximum negative value, the capacitor starts to build negative charge. By building a negative voltage, the diode turns on and thus, the path becomes at ground. Meanwhile, as the current level gets back to positive, the charges are building up in capacitor to produce positive voltage, and thus the diode turns off. In other words, the diode is turned on when the

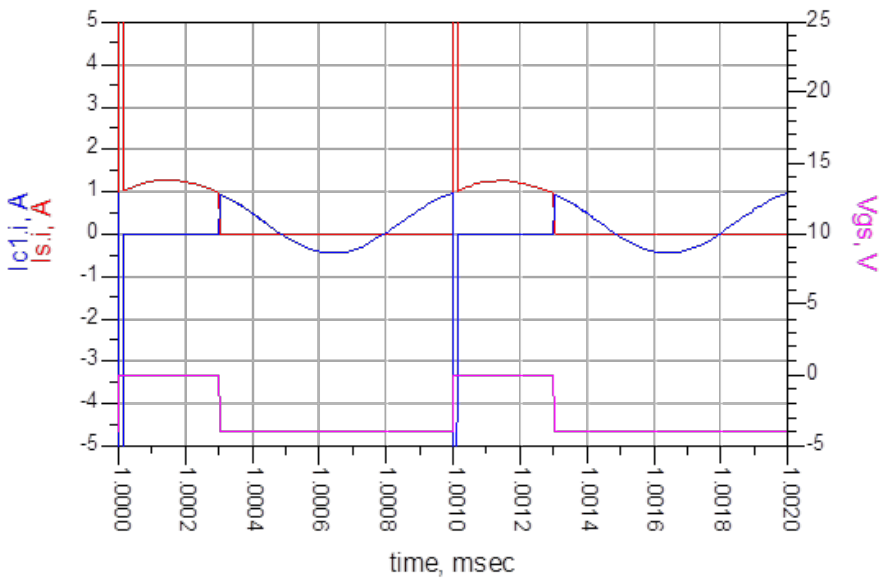
rectifier input voltage is lower than the ground and thus, the path becomes shorted. On the other hand, if the rectifier input voltage is higher than the ground, the diode is turned off. This will result in half sinusoidal voltage swing. The large value of inductor and a shunt capacitor before the load present as a low pass filter together. Thus, the rectifier outputs a DC.

DC-DC Converter is a device that produces variety of DC voltage level as an output from the fixed level of DC power supply. A control signal must be input in order to control the output voltage level as desired. The role of this control signal in the DC-DC Converter is to produce Pulse Width Modulation (PWM) which controls the switches in the Converter. In Class $E^2$ DC-DC Converter, the PWM is the key component that controls the output voltage of the supply modulator.

To illustrate the operation of DC-DC Converter, compare the differences between two different control signals, one with duty cycle of 0.3 and another with 0.5 as shown in Figure 6. Figure 6(a) shows the class E inverter. The red arrow indicates current passing through the switch and blue arrow indicates current passing through the shunt capacitor. As described in the previous section, the sum of these two currents must be equal to the difference between AC current passing through the LC resonator circuit and the DC current from the power supply. In Figure 6(b) and (c), the red and blue color indicates the currents passing through the switch and passing though the capacitor respectively and the pink graph shows the voltage waveform with certain duty cycle at gate of the switch. It is noticeable that during 0.3 duty cycle, the current swing level is less than 2A while 3.5A swing occurs during 0.5 duty cycle. This is because as the time for open switch increases, very low duty cycle in other words, the DC current from the power supply has nowhere to flow; Switch is opened, shunt capacitor is seen as open at DC and capacitor in series LC resonator is also seen as open due to the capacitor at DC. Thus, it reduces current swing level. On the other hand, if we turn on and off the switch with the time close to the conduction angle of 118 degrees of the series LC resonator, the current swing is maximized. Regarding as the conduction angle mentioned, refer to Chapter 3. In general, it is known that the conduction angle of 118 degrees in Class-E Amplifier shows the best efficiency.


PWM

(a)


Ic1,i, A
Is,i, A
Vgs, V
time, msec
5
4
3
2
1
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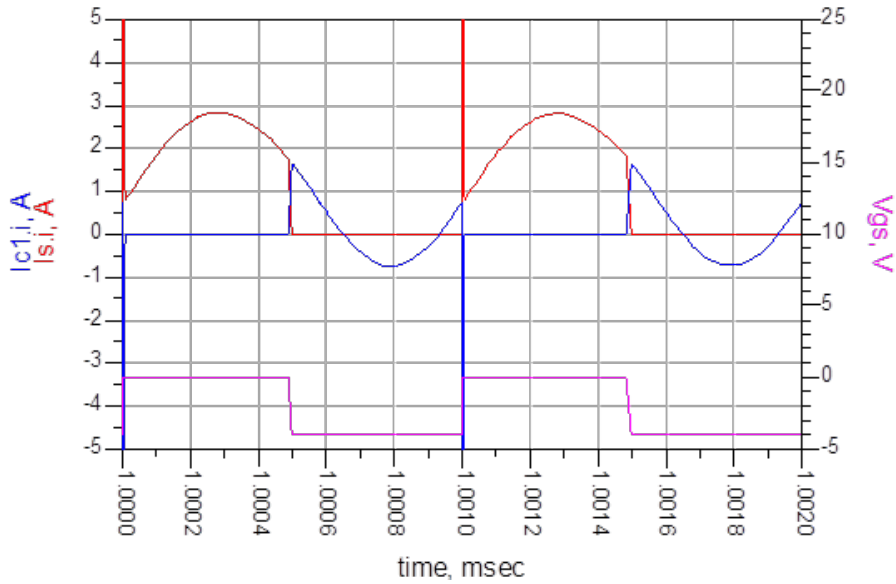
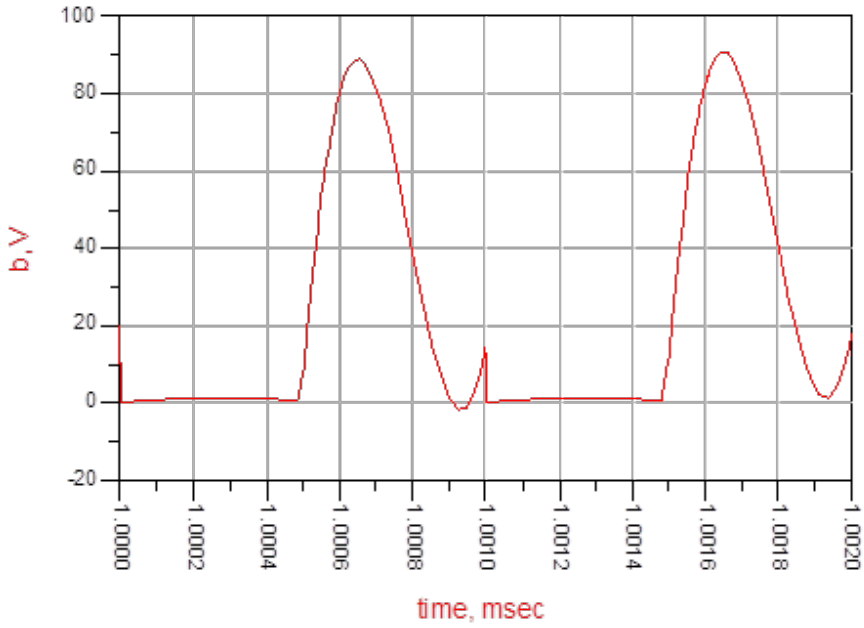
(b)



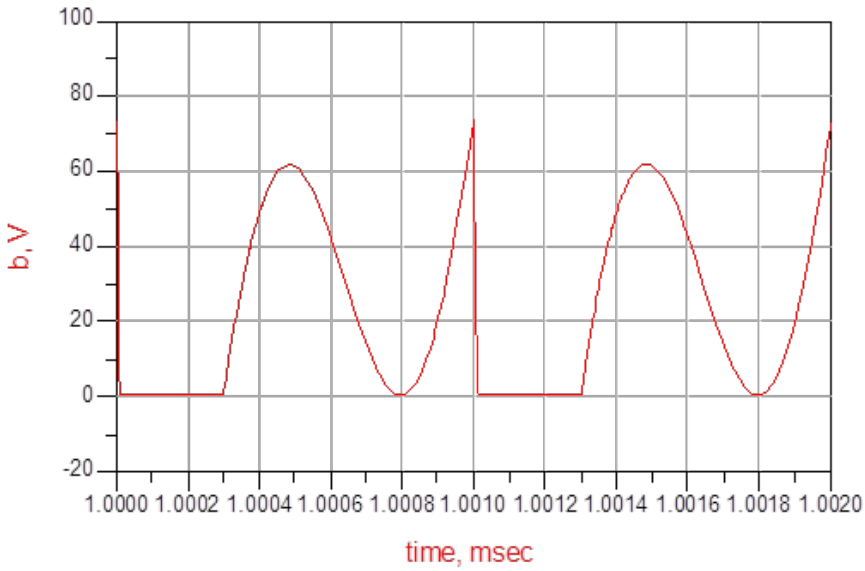

(c)

**Figure 6 (a) The overview of the Class-E inverter. The current waveforms (red and blue) and the voltage waveform (pink) at gate of the inverter switch of the inverter when duty cycle is (b) 0.3 and (c) 0.5.**

When the current swing level is increased, the voltage waveform at the drain of switch becomes as Figure 7. Notice that Figure 7(a) shows greater magnitude of voltage swing than Figure 7(b). Therefore, higher duty cycle constructs bigger wave and thus, bigger power is transferred to the rectifier. The power control in the Class $E^2$ DC-DC converter is done in Class-E inverter. The role of rectifier is to receive the AC power from the inverter and low pass filtering it. Since the rectifier operates independently from the control signal, the analysis of rectifier depending on the control signal is omitted. As a result, PWM is a key component to control DC-DC Converter with its duty cycle.




(a)




(b)

**Figure 7 The drain voltage waveform of the inverter switch when duty cycle is (a) 0.5, and (b) 0.3.**

The further details about Class-E will be covered in Chapter 3. In this thesis, the shunt diode in Class-E rectifier is replaced with a GaN HEMT so that the supply modulator only has components of GaN HEMT and lumped elements. Furthermore, loss from the forward voltage drop of a diode can be eliminated by replacing diode. The newly adopted GaN HEMT rectifier switch will serve the role of shunt diode and its operation and control is described in the following section. The new schematic diagram of the Class $E^2$ DC-DC Converter is illustrated in Figure 8.

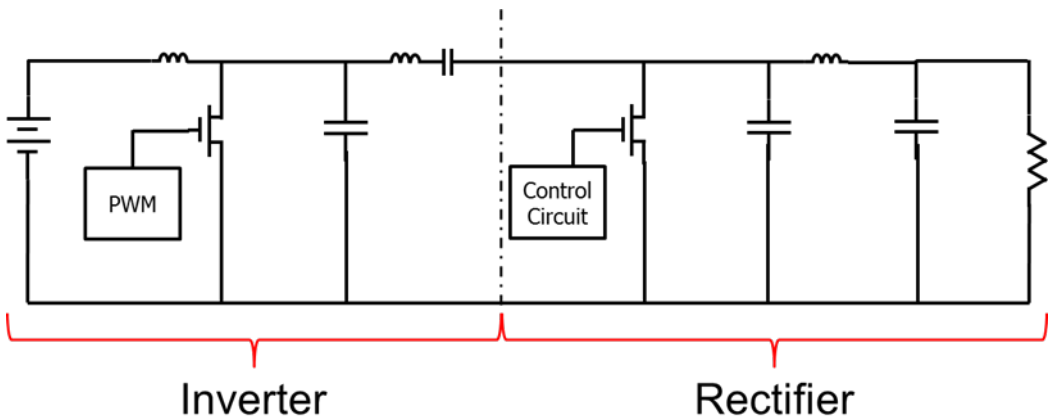



**Figure 8 New schematic diagram of Class $E^2$ DC-DC Converter.**

## 2.3. PWM Controlled Supply Modulator

The control circuits that will be discussed in this section can be divided into two groups; one for inverter controller and another for rectifier controller. Although the idea is basically the same between the two, a few quite differences can be found, such as line connection and the size of transistors.

### 2.3.1. Pulse Width Modulation (Inverter Switch Control)

The inverter is controlled by the Pulse Width Modulation (PWM) signal which is a pulse wave with a fixed frequency but its pulse width can be modulated according to control signal level as desired. The main idea of PWM is described in Figure 9.

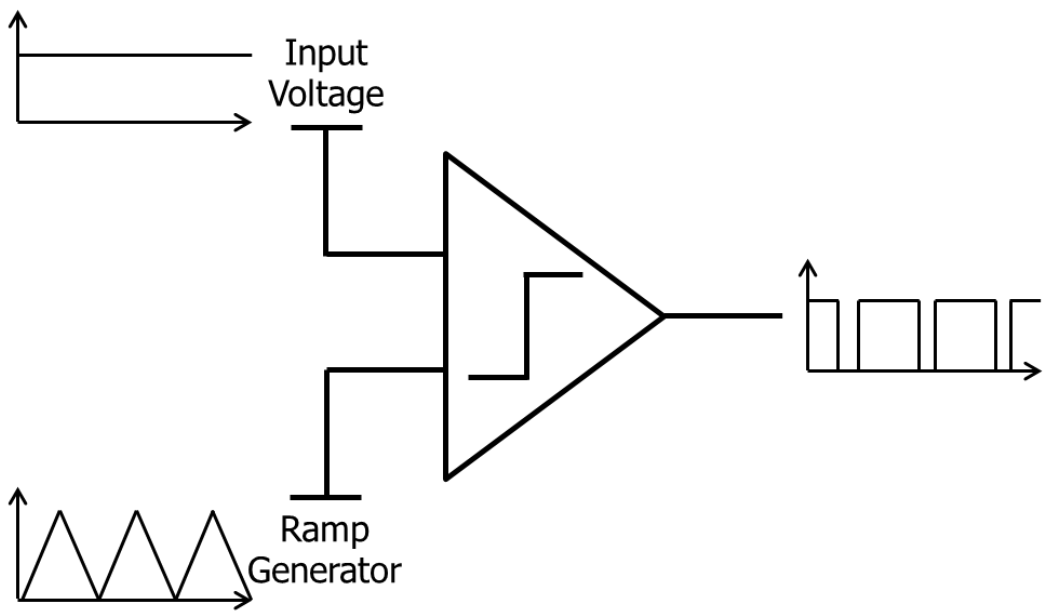



**Figure 9 The operation principle of the PWM controller.**

The PWM consists of two big components; a ramp generator and a comparator. The ramp generator is a triangular wave generator with a desired frequency and the comparator is a logic circuit that compares two input signal and outputs High or Low according to its two inputs. Referring to Figure 8, when the input voltage is higher than the ramp generator voltage level at a certain time, the comparator produces output High. When the input voltage is lower than ramp generator, it outputs Low.

The output High and Low represents the voltage applied as a supply voltage for $V_{dd}$ and $V_{ss}$. Because the ramp generator produces a fixed level of voltage swing with a fixed frequency, the output duty cycle can be adjusted by the input voltage of the comparator. Thus, PWM can be generated with desired pulse width only with the input voltage.

Actually the main part of PWM can be thought as the comparator, but the ramp generator is also important. First of all, the switching frequency of the modulator is decided to the frequency of the ramp generator. While the comparator needs to switch fast and sensitively at the moment the input voltage and ramp voltage cross each other, the ramp generator needs to keep producing constant voltage level swing with constant frequency.

The ramp generator is an oscillator that generates a triangular wave and it is composed of two Operational Amplifiers (OP Amp), three resistors, and a capacitor as shown in Figure 10. The two OP Amps can be in same size, but their duties are quite different. The left side OP Amp in Figure 10 operates as a comparator while the right side OP Amp acts as an inverting integrator. The OP Amp on the left side starts with an unknown state, however, assume the positive input of the OP Amp is slightly higher than the negative input. Because this left OP Amp acts as comparator, it will amplify its difference and outputs High, which would be its supply voltage. This High output will feed input of inverting integrator, the right OP Amp, thru the resistor, $R_1$, and the capacitor, C, will start charging with RC time constant. This will result in decrease of output voltage at a constant rate. The voltage difference between the output of the right OP Amp and the output of the left OP Amp will be divided according to the voltage divider composed of $R_2$ and $R_3$. When the divided voltage becomes low enough to reach the reference voltage, which is the negative input for left OP Amp, the left OP Amp switches its output polarity to Low and thus, the right OP Amp switches its direction to upwards forming the other half of triangular wave. Again, when the voltage difference between two outputs crosses reference voltage, the new cycle of triangular wave begins. The frequency of the ramp generator can be calculated with $R_1$, $R_2$, $R_3$, and C as shown in following equation.

$$f = \frac{1}{4R_1C} \cdot \frac{R_2}{R_3}$$

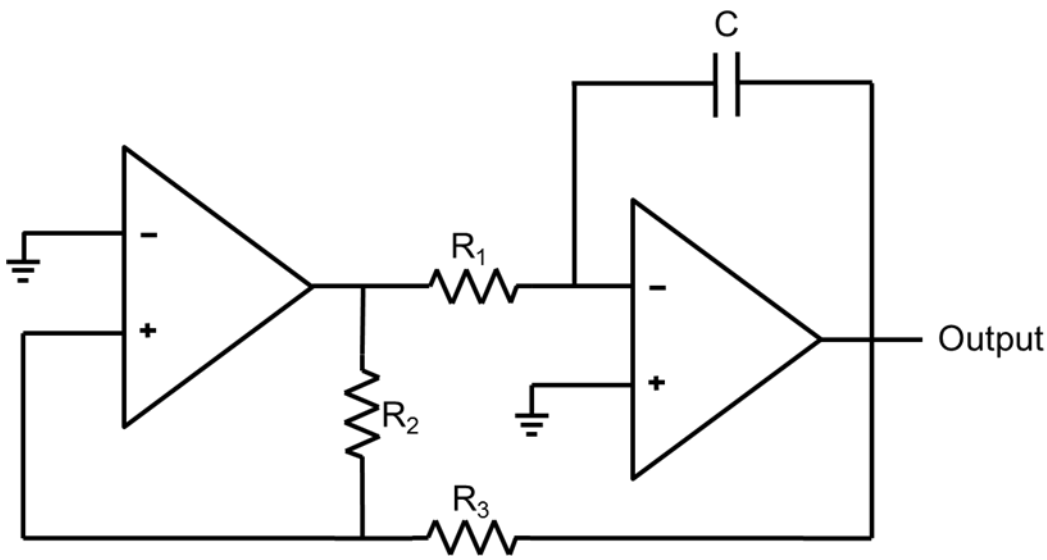



**Figure 10 the schematic of the ramp generator.**

## 2.3.2. Rectifier Switch Control

The role of rectifier switch is to replace diode as described in the previous section. The result of the inverter current swing comes out as sine wave due to the series LC resonator at the end of inverter. The rectifier switch shorts the current when the current level hits the negative maximum and opens when the current level gets back to zero. In order the switch to respond correctly, gate voltage signal should be related to somewhere taking the phase information into account. The rectifier switch cannot be related to any part of DC-DC converter where it belongs since it may change the whole circuit. As a result, the rectifier switch is related to the independent source, ramp generator, which is used to produce PWM and control inverter switch. The ramp

generator is related in terms of phase information of the sine wave current at series LC resonator. However, due to series LC resonator and shunt capacitor located in between inverter switch and rectifier switch, phase delay is inevitable.

To compensate the phase delay a series RC delay is used. But there is a limitation on delay length produced by the RC circuit. Because as the signal pass thru the RC circuit, not only the phase is delayed, but it also reduces voltage swing. If the voltage swing is lower than the input coverage of comparator, the comparator cannot produce output signal properly. Therefore, a hysteresis comparator is adopted, so that partial delay is made with RC circuit and additional delay is produced by the hysteresis comparator. By the mean of producing RC delay with hysteresis comparator, the comparator gives later response than the conventional comparator. In Figure 11(a), it shows the conventional comparator that is used in inverter switch control. When the blue line is higher than the red line, the output gives High and when the blue line is lower than the red line, the Low is the output. Figure 11(b) shows the result when the comparator's two inputs are switched. Because rectifier should operates in opposite way from the inverter switch, it needs to be connected in different way. When the comparator becomes hysteresis, the output result becomes Figure 11(c). The red line needs to hit a certain amount of voltage higher than the blue line in order to outputs High, and the red line needs to hit a certain amount – but not necessarily the same amount as before – lower than the blue line in order to outputs Low. The amount it needs to produce high and low can be determined with the transistor size inside of comparator which will be discussed later.

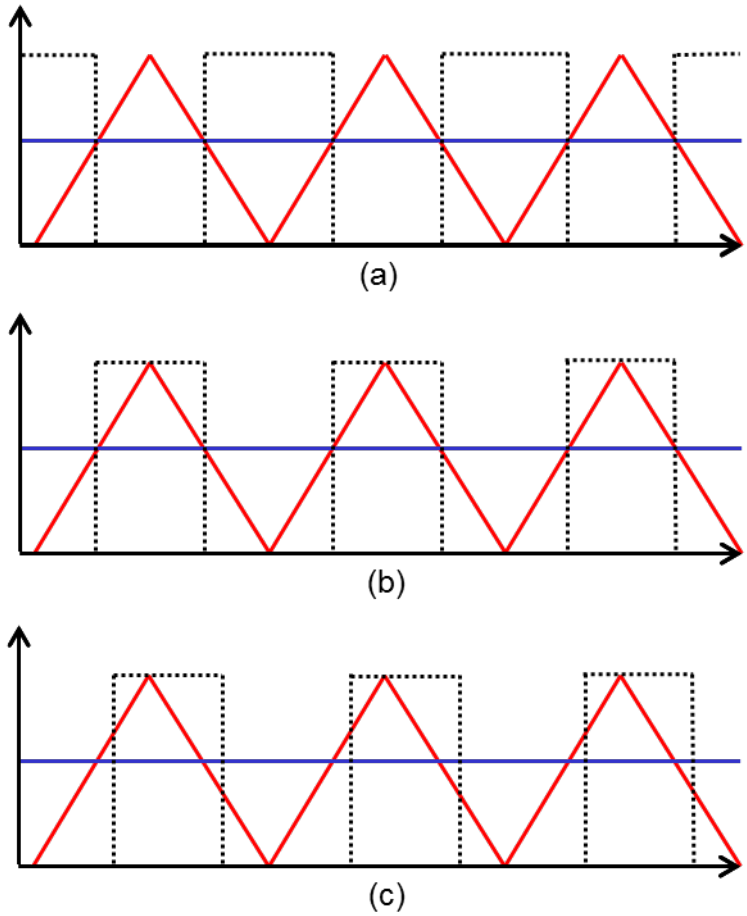



**Figure 11 Voltage waveform of the comparator (a) normal operation. (b) when both input are inverted. (c) with the hysteresis.**

Therefore as depicted in Figure 12, the triangular wave from the ramp generator passes thru a resistor, $R_1$, and a capacitor, C, transferring into hysteresis comparator input. Note that resistor, $R_2$, is very large value, so that the voltage does not get divided. The role of resistor, $R_2$, is to eliminate the floating status of the input, which would be the gate of a transistor. By giving potential to the gate before the drain voltage is applied, transistor explosion can be avoided.

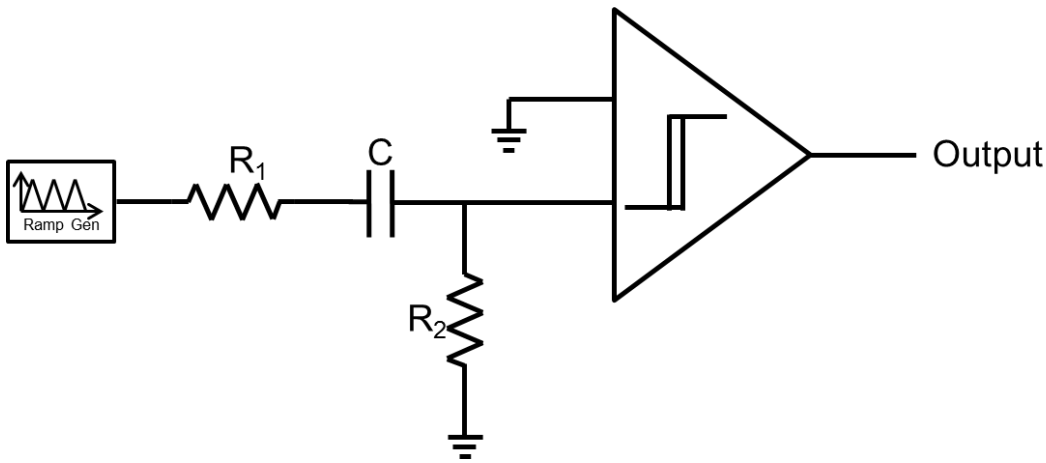



**Figure 12 Rectifier control scheme.**

Until now, the concept of PWM system and the required elements are discussed. Additionally, a schematic diagram for the inverter switch controller and the rectifier switch controller has been reviewed. The detailed portion of designing each element will be discussed in the following section.

## 2.4. CMOS Control Circuit

As described earlier, the proposed Class $E^2$ DC-DC Converter has only shunt switches and thus, the control signal required is only a range of -10V to 2V. Typically the threshold voltage of GaN HEMT is about -3.2V. At -4V of gate voltage, drain-to-source is isolated enough and the channel is turned on completely at +1V of gate voltage which results in demand of 5V operation CMOS control circuit. Note that although the CMOS controller will be biased with -4V and +1V in the measurement, 0V and 5V of power supply is assumed in design section. In this section, the design of 5V operation CMOS control circuit that includes PWM using IBM 0.18um SOI 2.5V RF technology will be discussed.

### 2.4.1. Operational Amplifier

Operational Amplifier (OP Amp) is a key element in designing CMOS controller to produce PWM. The specification of OP Amp varies the limit of switching frequency and the voltage range of triangular wave. Additionally, the comparator is derived from the OP Amp and the variation of the OP Amp is used as voltage regulator. Among the CMOS components designed in this chapter, OP Amp consumes the most current and thus, more attention should be made.

First of all, the most complicated portion is designing OP Amp for ramp generator. It needs to operate with supply voltage of 5V with 5V of wide input common mode range and its phase margin should be larger than 60 degree in order to avoid self-oscillation. Figure 13 shows the basic schematic of an OP Amplifier.

From the schematic, a desired OP Amplifier will be derived. Since the CMOS controller is fabricated using IBM 0.18um SOI 2.5V RF technology, a single transistor cannot endure 5V stress. Therefore each of transistors must be stacked so that each transistor's stress does not exceed 2.5V. The stacked version of OP Amp will become as depicted in Figure 14.

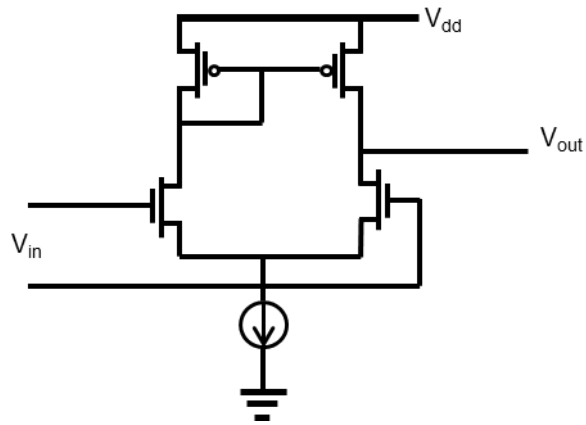



**Figure 13 A basic operational amplifier.**

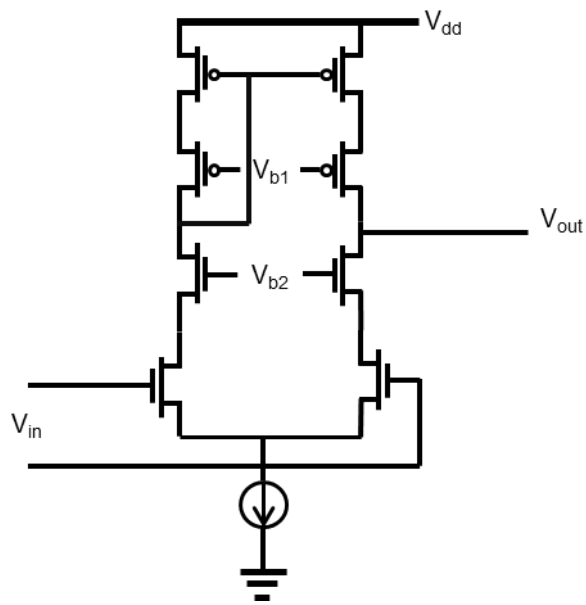



**Figure 14 A cascode operational amplifier to prevent from voltage breakdown.**

An active current mirror load is applied in this amplifier using top two PMOS transistors for single ended output. It should be noted that the gate bias active current mirror is fed by drain node of lower PMOS transistor to bias theses transistor to the edge of the triode region in order to increase the output voltage swing.

After stacking the OP Amp, the next procedure is to increase input common mode range. Because the triangular wave that will produce later will swing 0V to 5V, the input of the OP Amp will be 0V to 5V swing. The gain of the OP Amp should be large enough over 5V range of input voltage, meaning it should have more than 30dB of gain whether its input voltage is 0V or 5V. To make this happen, input folded cascode is applied as shown in Figure 15.

Also note that the input folded cascode is stacked to avoid exceeding breakdown voltage. Although the top two PMOS transistors' gates are fed by the drain voltage of lower PMOS transistor, this OP Amp will outputs a limited range since all transistors are not completely turning on and off – the maximum output voltage swing is limited by the overdrive. To make a rail-to-rail swing at the output, a push-pull stage is added at the output and to control the push-pull stage, it is necessary to have floating current source in the middle of the OP Amp. Therefore the next version of schematic of the OP Amp will be as depicted in Figure 16.

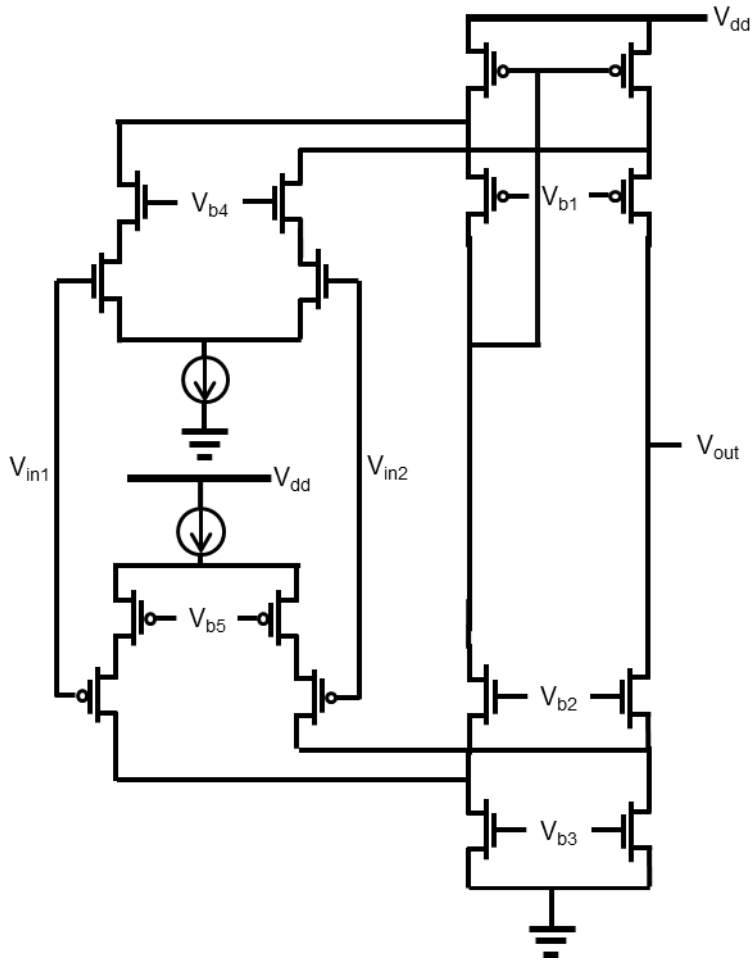



**Figure 15 An input folded cascode operational amplifier to extend the input common mode range.**

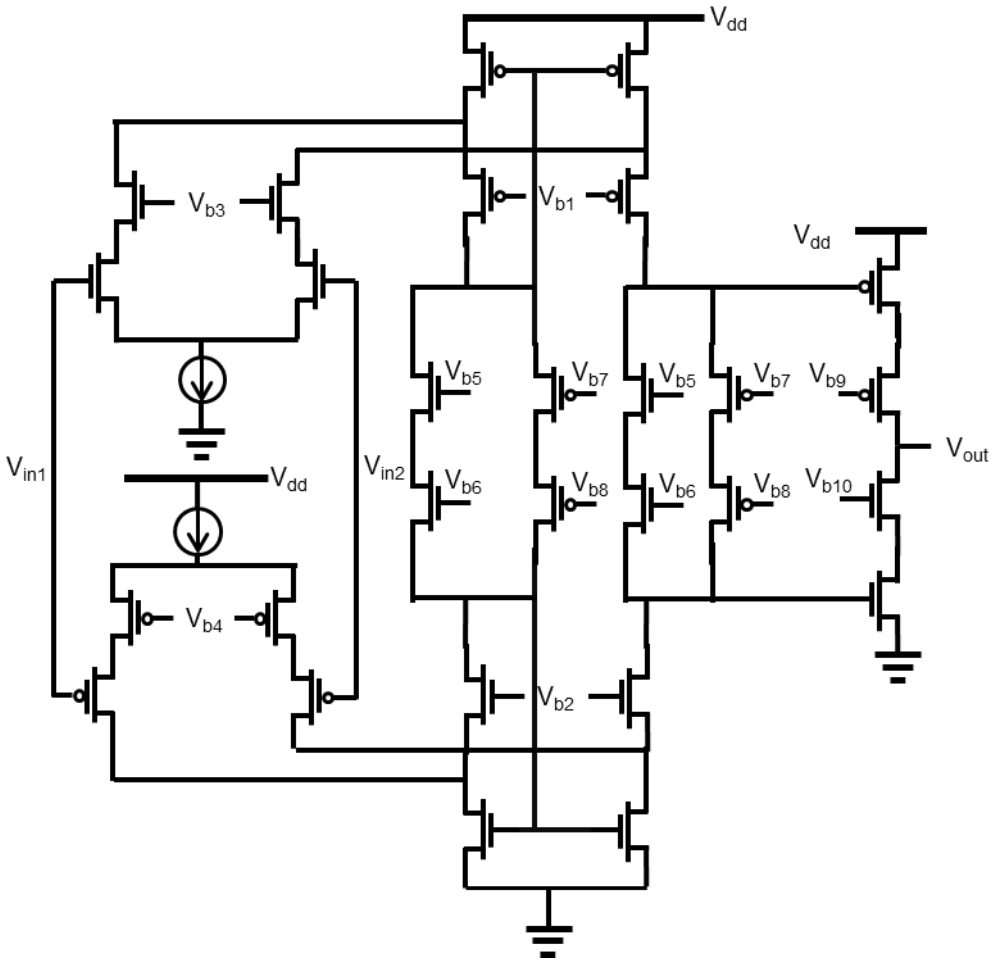



**Figure 16 An input folded cascode operational amplifier with common-source push-pull output stage. The output stage is controlled by floating current sources.**

The final procedure is to obtain wide phase margin. Although the frequency limit of the OP Amp is critical in deciding frequency of ramp generator, or even switching frequency of modulator, phase margin should be obtained as more than 60 degree in order to operate in stable mode. This wide phase margin will also eliminates oscillation of the device. To obtain it, Miller Compensation is adopted at the push pull stage as shown in Figure 17.

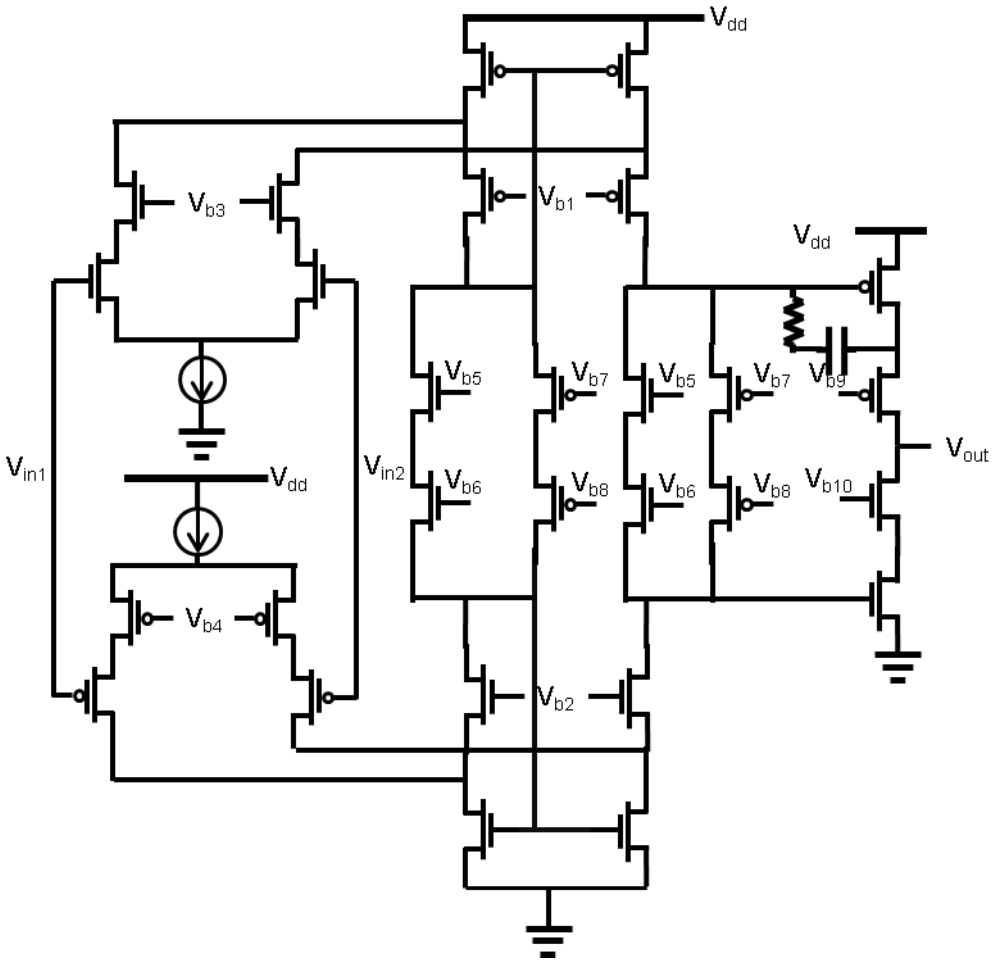
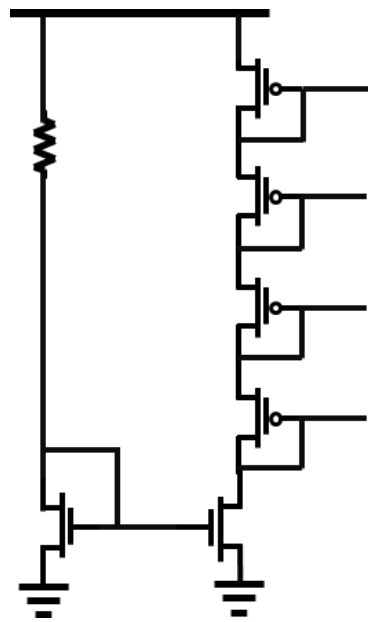
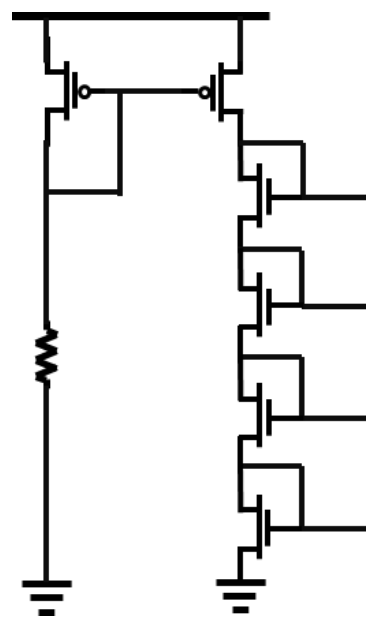



**Figure 17 The complete schematic of the operational amplifier with miller compensation.**

As noticed in the schematic, there are 10 different gate biases. Those biases are feed by current mirror technique. This current mirror technique is a safe way to give an accurate bias without worrying of fabrication error. The two main current mirror schematics are shown in Figure 18. Figure 18(a) shows supply for the PMOS gates and Figure 18(b) works as supply for the NMOS gates. By adjusting the individual transistor sizes, a desired level of voltage can be obtained. In this OP Amp, there are 4 of these current mirrors and each of them feed 2 to 3 biases.



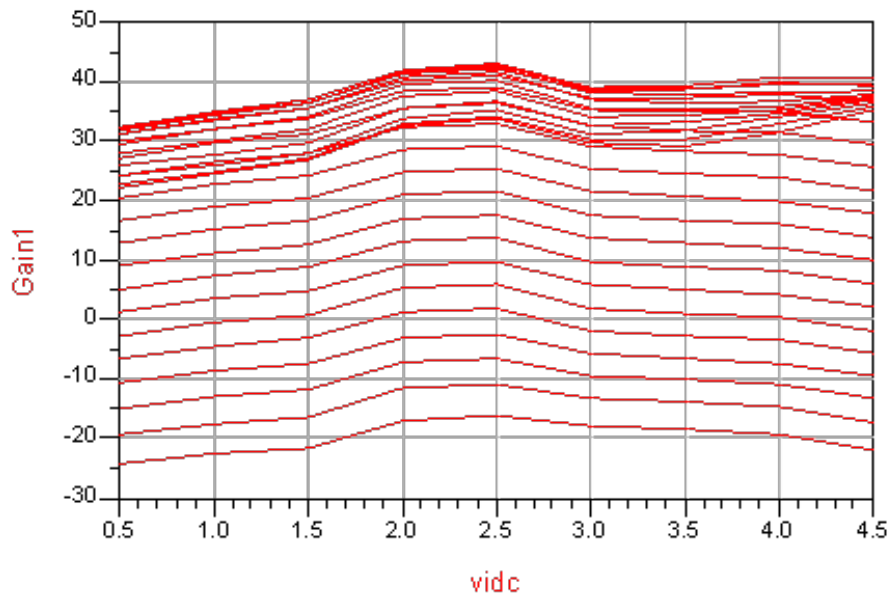
(a)



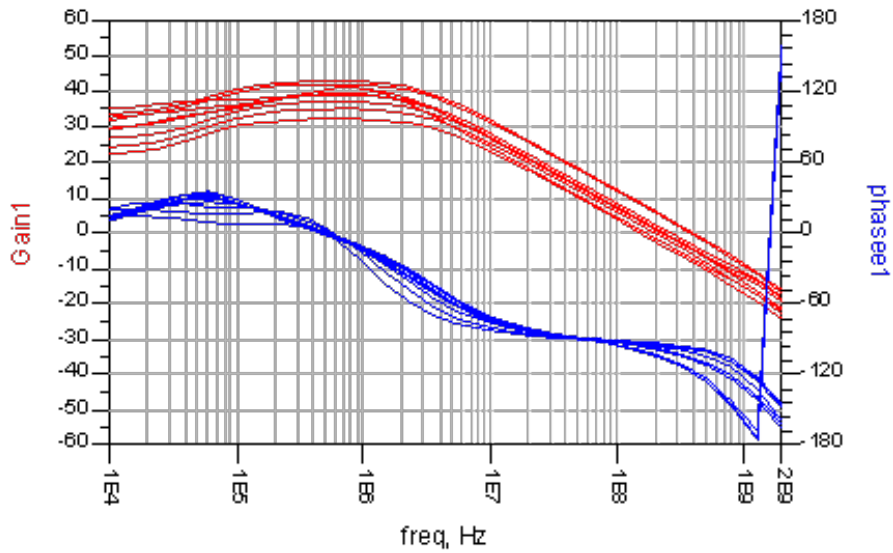
(b)

**Figure 18 Current mirror (a) PMOS feeding, (b) NMOS feeding.**

With the OP Amp designed as the schematic shown in Figure 17, input common mode range with 32~43 dB of gain and more than 60 degrees of phase margin is obtained as shown in Figure 19. By keeping each transistor sizes minimum, the current consumption of the OP Amp is 2.0mA according to ADS2009 Update 1. The simulation results are shown in Figure 19.




(a)




(b)

**Figure 19 Simulation results of the operational amplifier. (a) gain versus input common mode, (b) transfer function.**

## 2.4.2. Comparator

When there are two different signals, a comparator compares the two and depending on which one is higher than another, it outputs high or low. A comparator can be designed as an OP Amp described in the previous section, however, the designed OP Amp in consumes high amount of current. The role of comparator is just to compare and it is expected not to consume mush current. Therefore, a simple structure of comparator is used. As shown in Figure 20, a conventional one-stage comparator is designed.

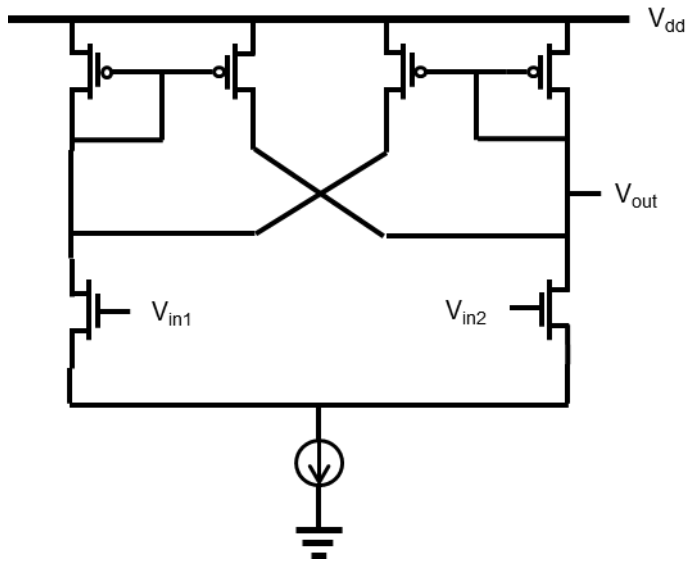



**Figure 20 A conventional one-stage comparator.**

Remembering that in this work, IBM 0.18um SOI 2.5-V RF technology is used and thus, the voltage breakdown of each transistor needs to be considered here again. Therefore, the conventional one-stage comparator is changed to stacked structure shown in Figure 21.

The final circuit diagram is shown in Figure 22. The second stage is added in order to produce output rail-to-rail swing. Note that there are two different output nodes, one as High and another as Low. High output produces a signal ranging from 2.5V to 5V while low output produces a signal ranging from 0V to 2.5V. Although it is not noted in Figure 22, the node between the lower transistor of $V_{out,H}$ and the upper transistor of $V_{out,L}$ can be used as full-swing output node. Again in here, 4 different biases in Figure 22 are fed using current mirror technique described in above.

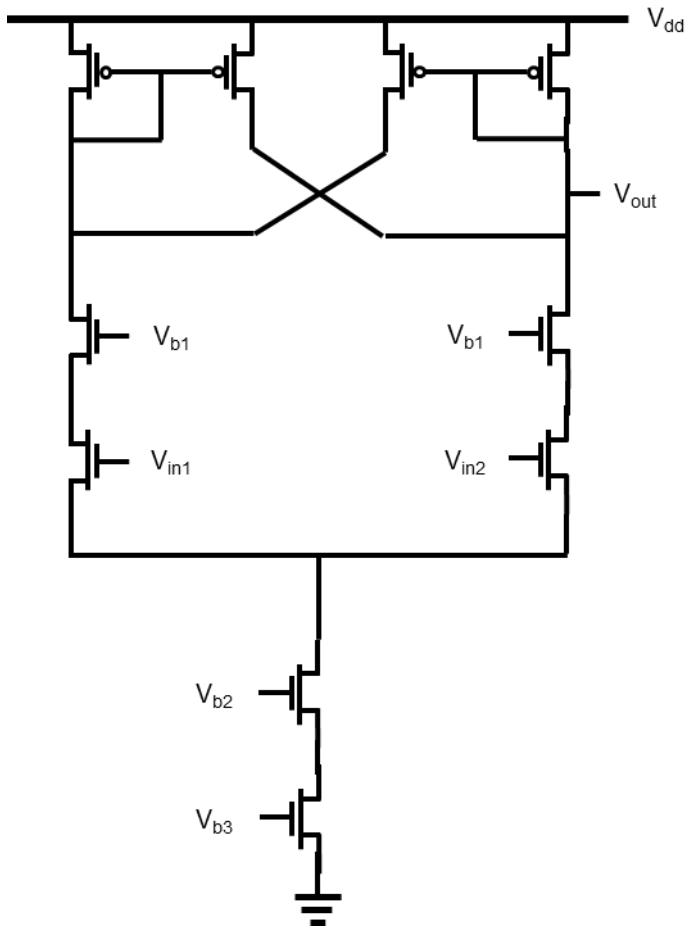



**Figure 21 A stacked one-stage comparator.**

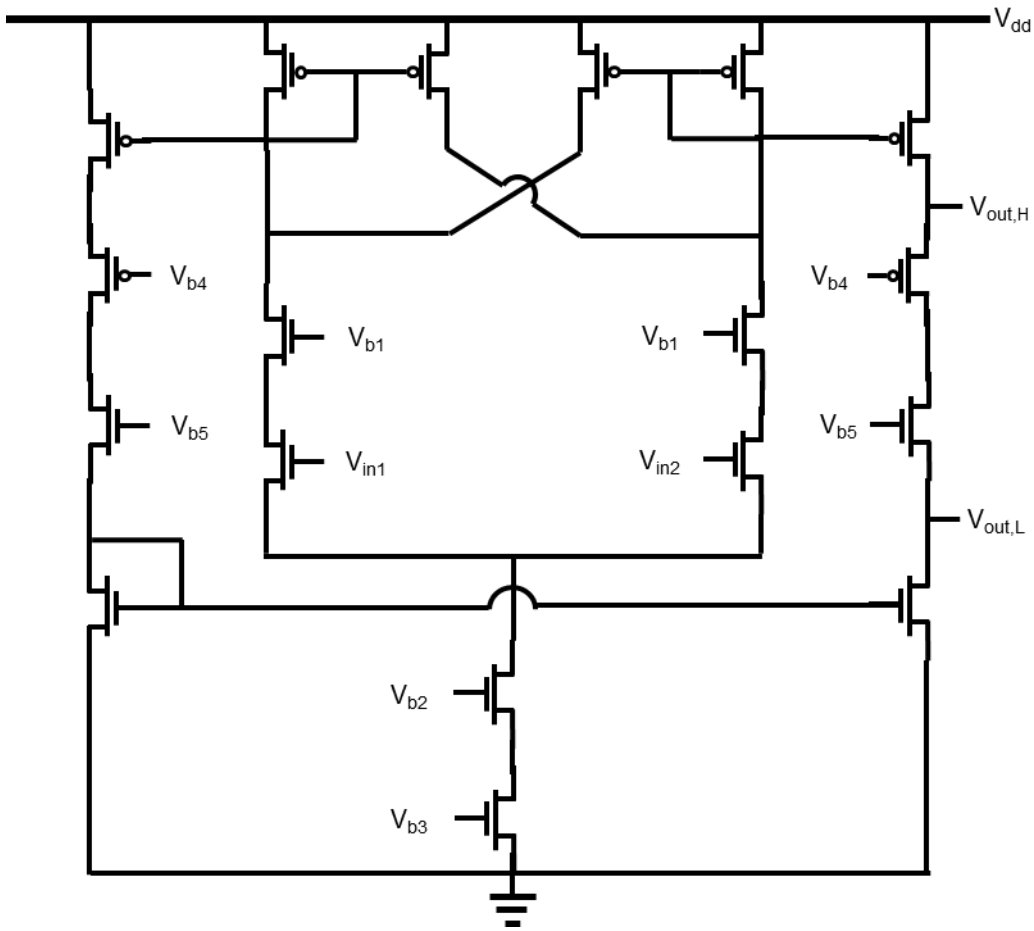
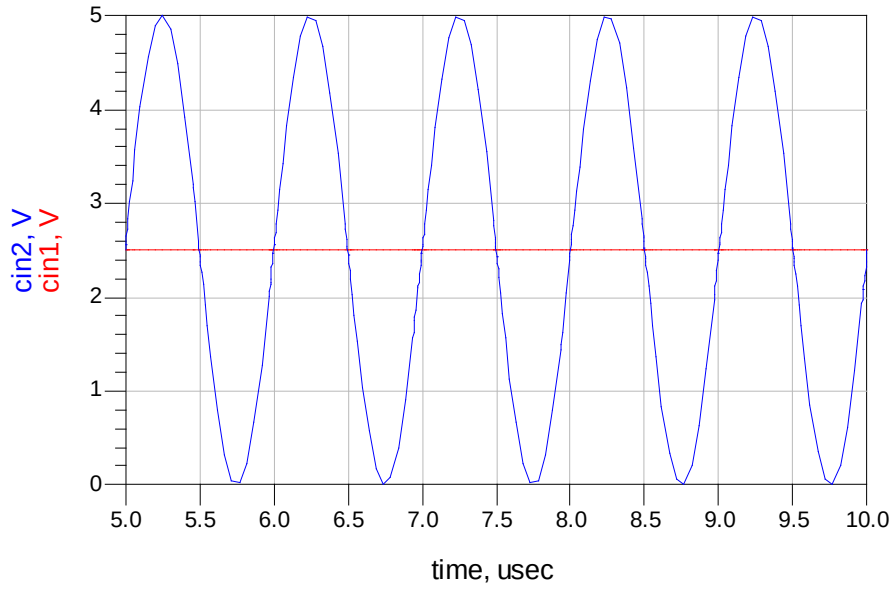
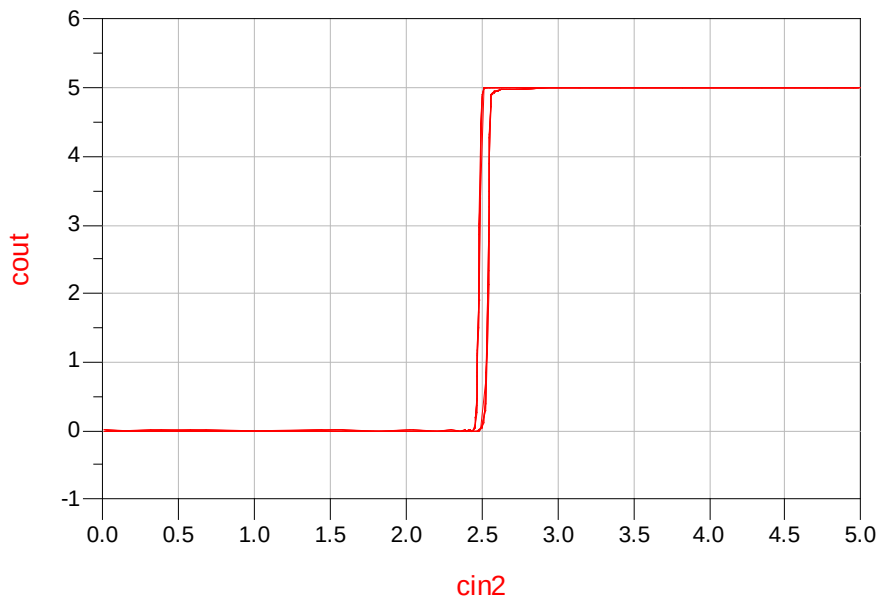



**Figure 22 The complete schematic of the 2-stage stacked comparator**

In order to check if the comparator is correctly designed, a few graphs are checked. Figure 23(a) shows the two input signals, one with red and one with blue. Figure 23(b) shows the output responds depending on the input modulated signal. In this case, the input signal of blue line in Figure 23(a) is used as a modulated signal. Notice that the output voltage of comparator changes rapidly as the modulated signal crosses 2.5V of constant input voltage Figure 24 shows the output voltage at $V_{out,H}$ and $V_{out,L}$, each is indicated as red line and blue line respectively. According to the simulation total current consumption of the comparator is about 0.9mA.




(a)




(b)

**Figure 23 Simulated results of the comparator. (a) input dc voltage with input modulated signal and (b) output voltage vs. input modulated signal showing that the output changes rapidly at the comparing point.**

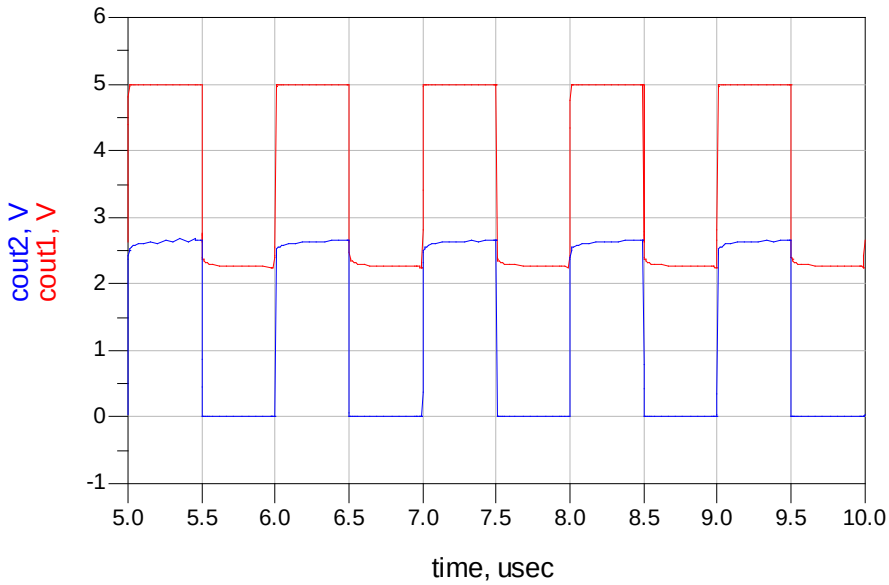



**Figure 24 Output voltage of comparator at two different nodes.**

## 2.4.3. Hysteresis Comparator

While the comparator changes its output status, i.e., high to low or low to high, as soon as one input crosses the another, a hysteresis comparator changes it output when one input crosses the point of the another plus or minus alpha. To help understanding, refer to Figure 25. Assume one input as a reference is 2V (blue line) and another input is a triangular wave (red line) swing from 0V to 4V. A conventional comparator will give output High right after the red line crosses blue line, which is at 2V and outputs Low right after the next cross at 2V. Meanwhile, a hysteresis comparator does not give High output right after the red line crosses blue line, but it gives when the red line crosses about 2.5V. Additionally, when the red line crosses blue line from high to low, the output does not change to low immediately, but when the red line crosses about 1.5V, the output changes to Low. This is the difference between the conventional comparator and the hysteresis comparator. Previously, the

reason for adopting hysteresis comparator is mentioned as it gives the time delay. Strictly speaking, it is not the matter of time, but the comparator responds at the different point from the reference input. If the red line in Figure 25(b) moves from 0 to 2.4, the output will never change since it does not cross 2.5. Additionally, the reference point where the output is changed does not have to be ±0.5 of the reference. It could be any number, i.e., +0.7 and -0.3. This parameter can be adjusted when the circuit is designed. In this work, the hysteresis comparator is designed to have different absolute value of offsets from reference. Since one input will be applied with the voltage swing of 5-V peak-to-peak, the hysteresis comparator can be thought as a time delay component.

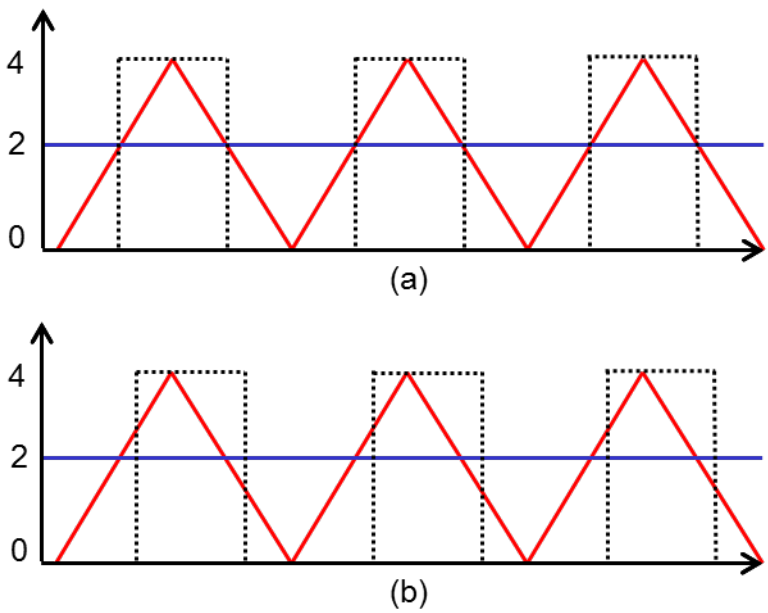



**Figure 25 Difference between (a) a conventional comparator and (b) a hysteresis comparator**

The final schematic of the hysteresis comparator is the same as conventional comparator, but the sizes of transistors are different. In this work, $M_1$, $M_2$, $M_3$, and $M_4$

in Figure 26 are different in gate width from conventional comparator. $M_1$, $M_2$ are tripled in size in order to make hysteresis and $M_3$, $M_4$ are doubled in size in order to endure high voltage stress between gate-to-source and gate-to-drain. All the biases are fed using current mirror technique described in Section 2.4.1.

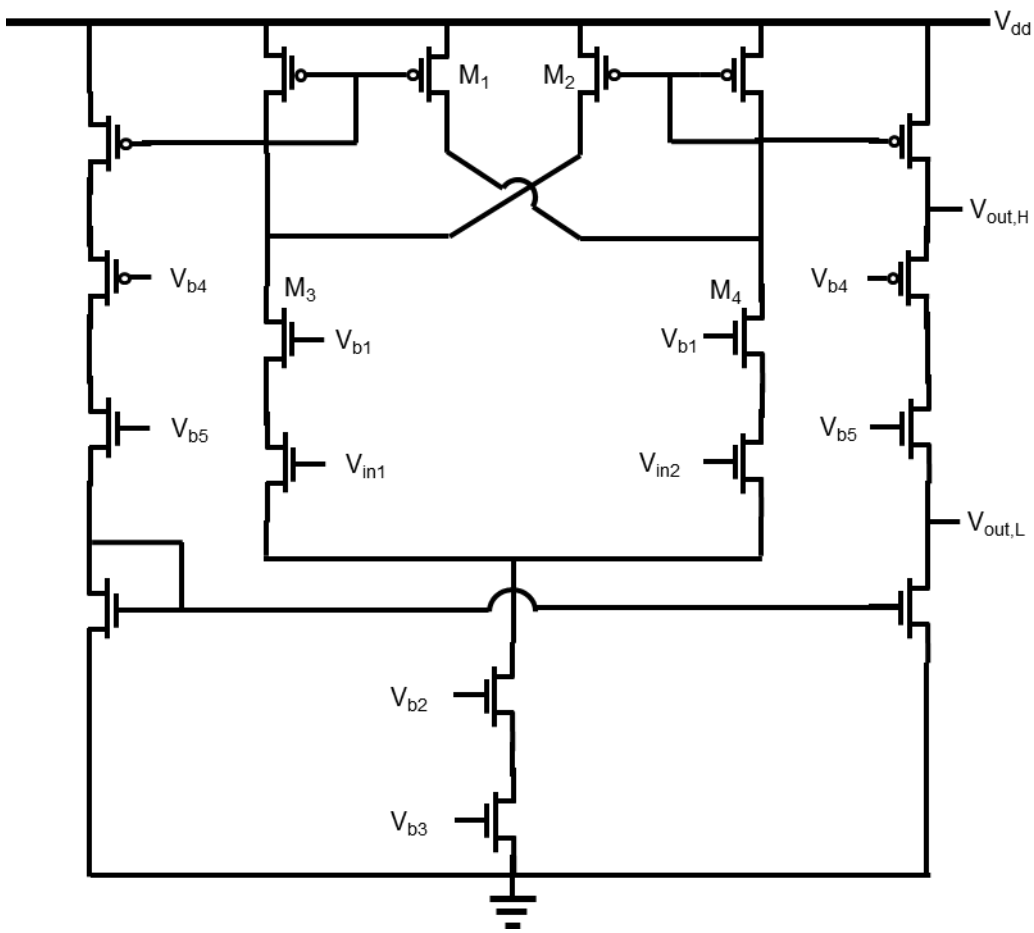



**Figure 26 The complete schematic of hysteresis comparator.**

Simulation results are shown in Figure 27. One of the input voltages is a 5V modulation signal while another is a constant voltage signal of 4V. Since the comparator is designed to be hysteresis, the output changes when the modulation

signal crosses 3.6V and 4.1V, not 4V. The overall current consumption including current mirror bias is 1.3mA.

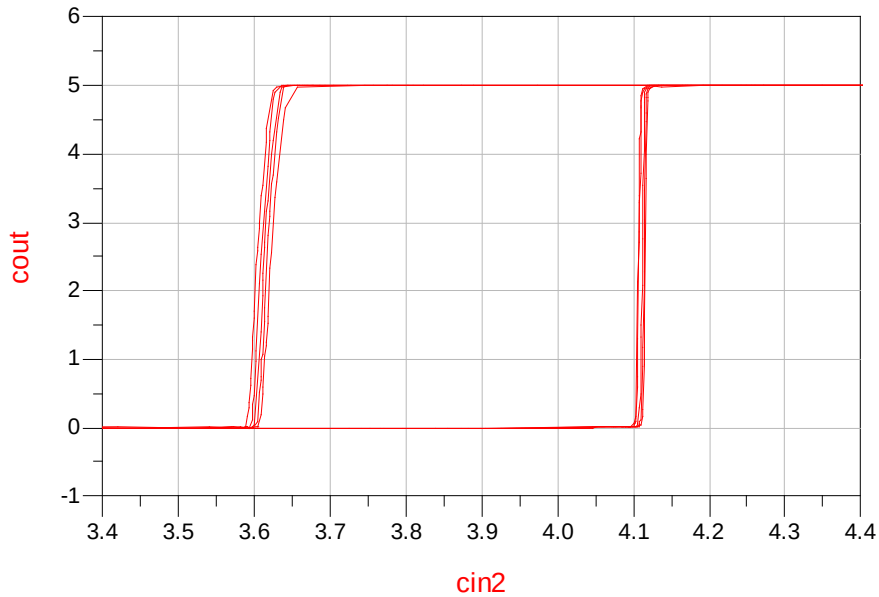



**Figure 27 Simulated result of output voltage vs. input modulated signal showing that the output changes at different reference point when constant input voltage signal of 4V is applied.**

## 2.4.4. Voltage Regulator

Voltage regulator is used to provide a constant level of voltage at a desired node. Instead of applying a direct voltage to the node, it can provide more stable DC voltage. This voltage regulator is used in gate driver, which will be discussed in the next section.

A simple voltage regulator is adopted in this work, that is, a voltage follower using OP Amp as illustrated in Figure 28. The OP Amp designed in Section2.4.1 consumes a lot of current due to many of requirements. Differently, an OP Amp to be

used in here does not require that much. First of all, since the purpose of the voltage regulator is to provide a middle level of voltage between High and Low, only a specific level of input will be applied and thus, it does not need input common mode range. It does not have to have high gain and neither push-pull stage for rail-to-rail swing. Therefore, by eliminating unnecessary things but keeping the stacked structure in order to prevent voltage breakdown, a simple OP Amp is designed as shown in Figure 29.

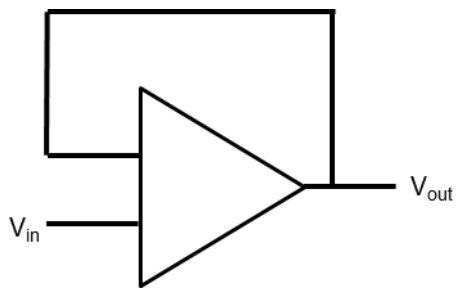



**Figure 28 A voltage regulator using OP Amp.**

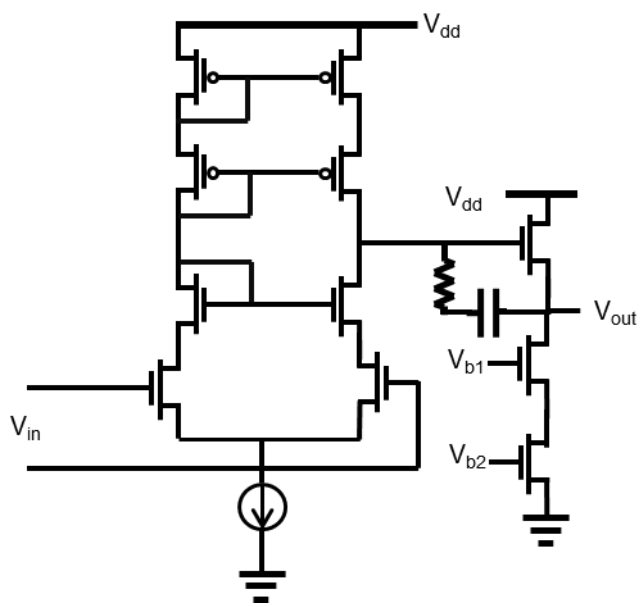
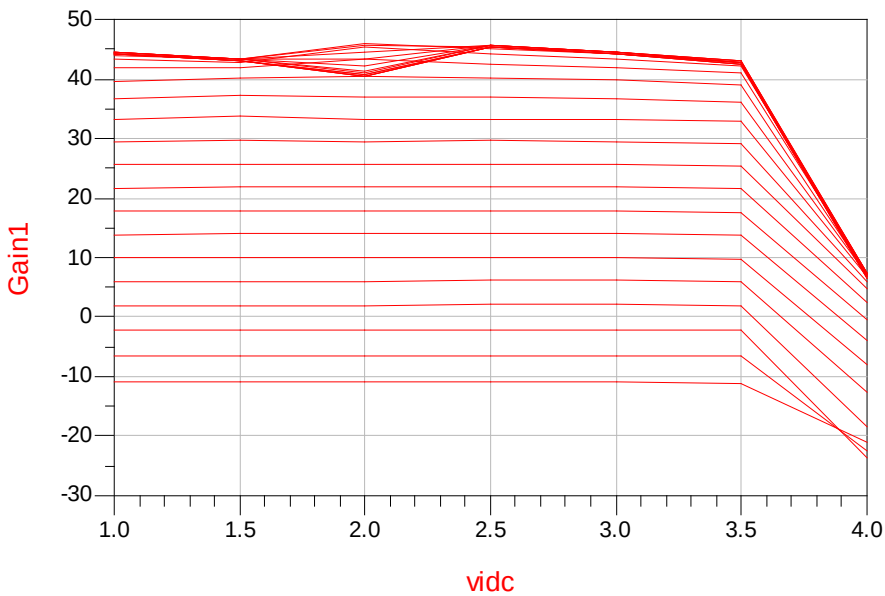
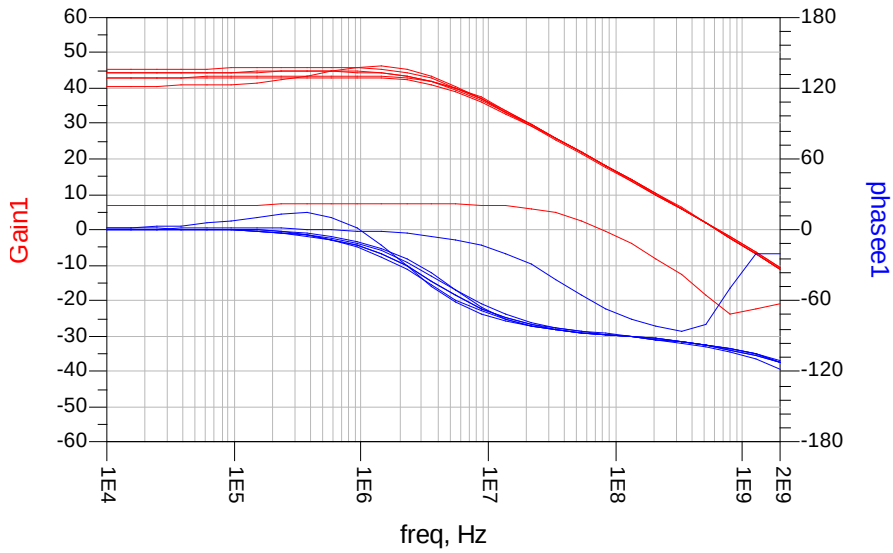



**Figure 29 The complete schematic of simple operational amplifier.**

For stability and to reduce number of biases, active current mirror load is applied. Miller compensation at the output gives higher phase margin and increase stability of the OP Amp. The biases at the last stage are fed by current mirror technique described in Section 2.4.1. The simulation result of this OP Amp is shown in Figure 30. Over 40dB of gain is obtained at 2.5V input voltage according to Figure 30. Referring to Figure 30(b) the phase margin of more than 60 degree is obtained. The striking line in Figure 30(b) is the curve for when the input voltage is 4.0V. At 4.0V of input, the gain is as low as negative value. However, the OP Amp designed in this section will have a constant input voltage of 2.5V and thus, this error in design is neglected. The overall current consumption is 0.43mA.




(a)




(b)

**Figure 30 Simulation results of the operational amplifier. (a) gain versus input common mode, (b) transfer function.**

## 2.4.5. Gate Driver

A most simple part of designing CMOS controller in this work can be a gate driver, however, it could be also considered as the most difficult one since it carries an important role of the CMOS controller.

The GaN HEMT that is going to be used in the supply modulator has an input capacitance of 34pF. Considering an input capacitance of IBM 0.18um SOI 2.5-V RF technology is 0.34fF/um, it is enormously large. In order to drive 34pF of GaN gate, a few stage of gate driver is essential.

An inverter which is composed of a PMOS and a NMOS is shown in Figure 31. The conventional gate driver is a series of inverter chain as illustrated in Figure 32. The inverter in logic circuit gives an output signal opposite to its input. When the

input is Low, the PMOS will turn on and the NMOS will turn off. This will lead the output to High as a supply voltage. In opposite, when the input is High, the PMOS is turned off and the NMOS is on, resulting output voltage to be at ground, Low. In general, the ratio of size of PMOS and NMOS is 3:1. However, the best performing size should be found using simulation.

Usually, digital logic circuit is designed as small as possible in order to operate in fast speed and with low current. However, the output of this small logic circuit cannot drive a large component; which would be the GaN HEMT in this work. That is because the load of the logic circuit is a large capacitor, a RC delay due to the capacitance is inevitable. In order to overcome this issue, an inverter with a little larger size is placed at the end of logic circuit. The inverter should not be as large to make the output signal distorted. Then, the larger inverter than the previous inverter should be placed in the next and repeated. The larger inverter can drive larger capacitive load. Therefore, in order to drive very large capacitive load, a chain of inverter must be used while each inverters have different size, becoming large as they get close to load.

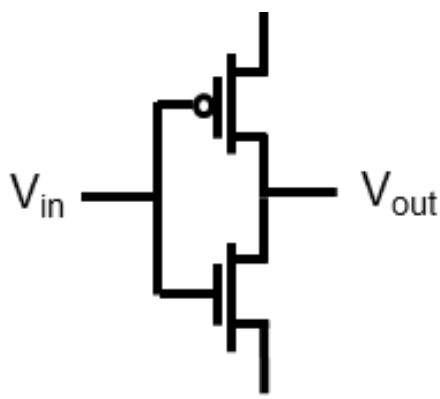



**Figure 31 An inverter composed of a PMOS and a NMOS.**

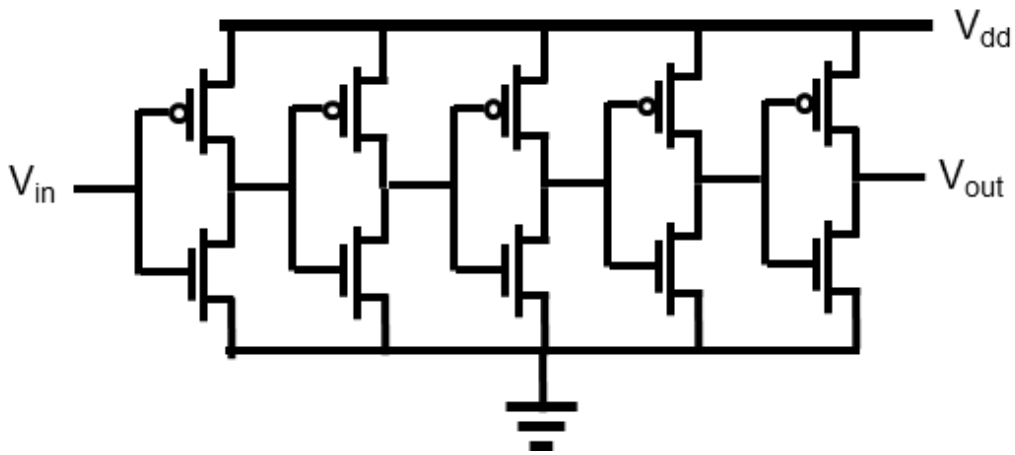



**Figure 32 A conventional gate driver.**

As it is considered in every previous designs, the voltage breakdown should be considered again. In gate driver, instead of simply stacking the transistor, two different voltage signals, each having 2.5V swing will be carried from comparator, or the input of gate driver, then they will be combined together at the end of inverter chain.

In Figure 22 and Figure 26, it is noticeable that the output of the comparator or the hysteresis comparator is not at one node, but two different nodes, $V_{out,H}$ and $V_{out,L}$. High output voltage, $V_{out,H}$, will give 2.5V to 5V pulse swing and $V_{out,L}$ will give 0V to 2.5V swing. Each of these output then will drive two different gate drivers. As shown in Figure 33, a complete schematic of gate driver will consists of two gate drivers with one cascode inverter at the end to combine the signal from two gate drivers. Because the upper gate driver is driving a signal swing of 2.5V to 5V, the source of NMOS should be at 2.5V as a reference voltage. Similarly, the lower gate driver is driving a signal swing of 0V to 2.5V, so that the source of PMOS should be tied to constant voltage of 2.5V. In here, the 2.5V is generated by the voltage regulator discussed in the previous section. This is important because the node for source of NMOS in upper gate driver and the node for source of PMOS in lower gate driver should be united to one node and the voltage at that node should be at stable and constant voltage.

The last stage of the whole gate driver is consisted of two PMOS and two NMOS

with a stacked form of a single inverter as shown in Figure 33. The lower PMOS and the upper NMOS in the last stage is serving their duty of separating the voltage so that each of four transistor are not handling more than 2.5V of voltage breakdown. Upper PMOS is getting signal from the upper gate driver and the lower NMOS is getting signal from the lower gate driver. By turning on and off the two transistors, the last stage of the gate driver drives 34pF of GaN HEMT.

The two different output signals, $V_{out,H}$ and $V_{out,L}$, from the comparator or the hysteresis comparator should be in phase theoretically. However in gate driver, the main issue lies on the shoot-thru current, a large level of current flowing from the supply to the ground during very short time when both PMOS and NMOS are not completely on or off. This effect becomes serious as the size of transistor increases. In other words, the last stage of gate driver is exposed to the shoot current problem and this could lead to a large current consumption. Therefore in purpose, the size of transistors in the second stage of comparator or hysteresis comparator are adjusted in order to generate slightly different phased signal as shown in Figure 34.

Figure 34 shows the signal at the input of gate driver. the red line shows the upper gate driver signal while the blue line shows the lower gate driver signal. According to the figure, it is noticed that the upper gate driver is turned off after the lower gate driver is turned on and the upper gate driver is turned on before the lower gate driver turned off. Remembering that the gate driver designed here is 6-stages, the signal at the input of gate driver will be inverted at the input of the last stage. Thus, the last stage of PMOS will turn on after the NMOS is turned off and vice versa. With a precise control of signal, the total current consumption in gate driver is about 1.2mA.

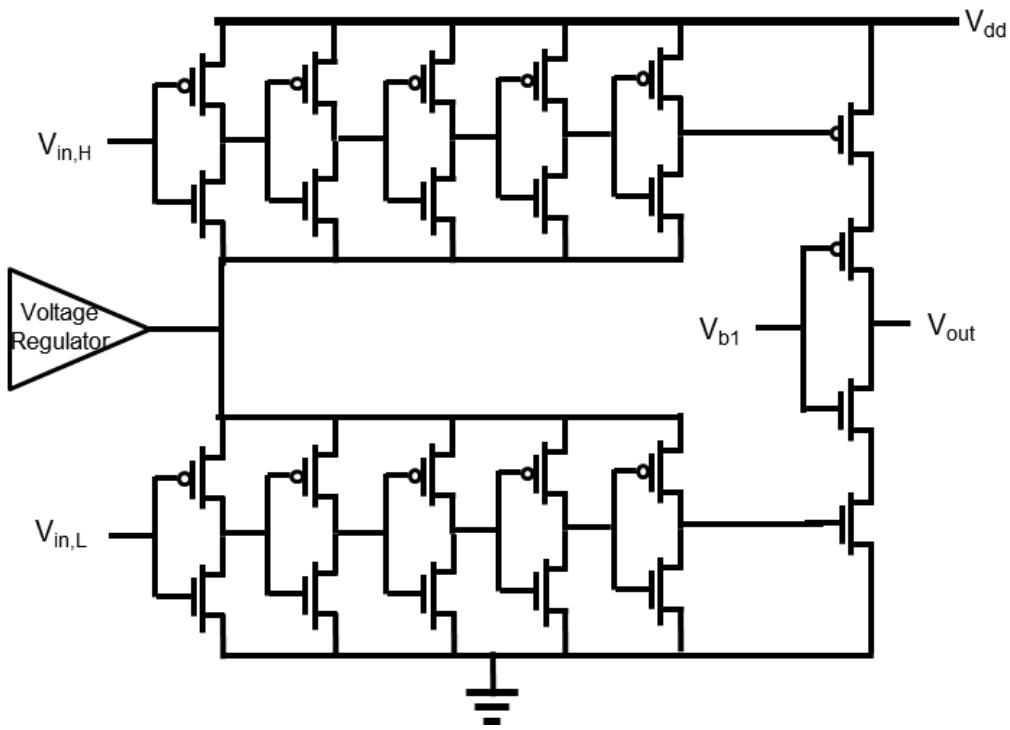



**Figure 33 The complete schematic of gate driver.**

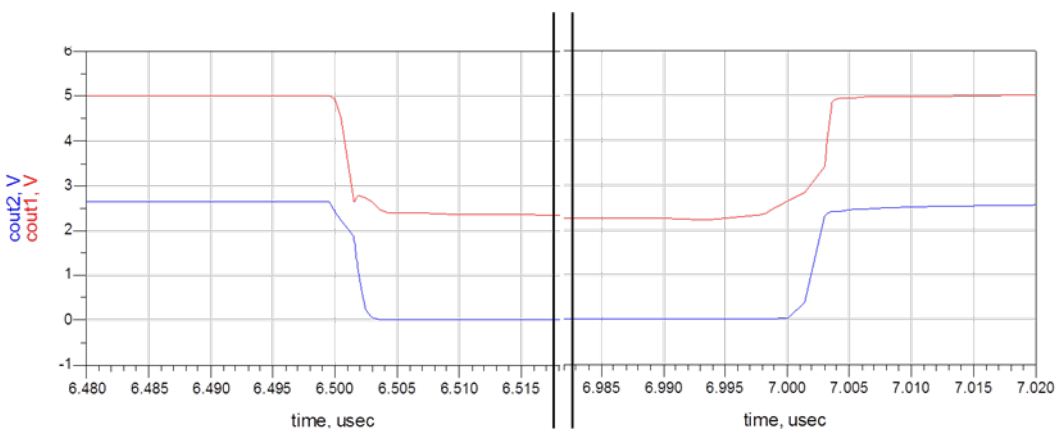



**Figure 34 Input signal of the gate driver.**

### 2.4.6. Layout

Based on the design in previous sections, the layout of the CMOS circuit is shown in Figure 35. The upper part of the chip is for inverter control and the lower part of the chip is for rectifier control. Inverter control circuit is composed of two OP Amps, forming ramp generator, comparator, voltage regulator, and a gate driver. Rectifier control circuit is composed of hysteresis comparator, voltage regulator and a gate driver. Inverter control circuit and rectifier control circuit are quite similar to each other, but the comparator input is alternate to each other and the comparator is working differently, one is conventional and another is hysteresis. More other components were fabricated in the chips, but since they were not used in the final version of a supply modulator, those will not be mentioned in this thesis.

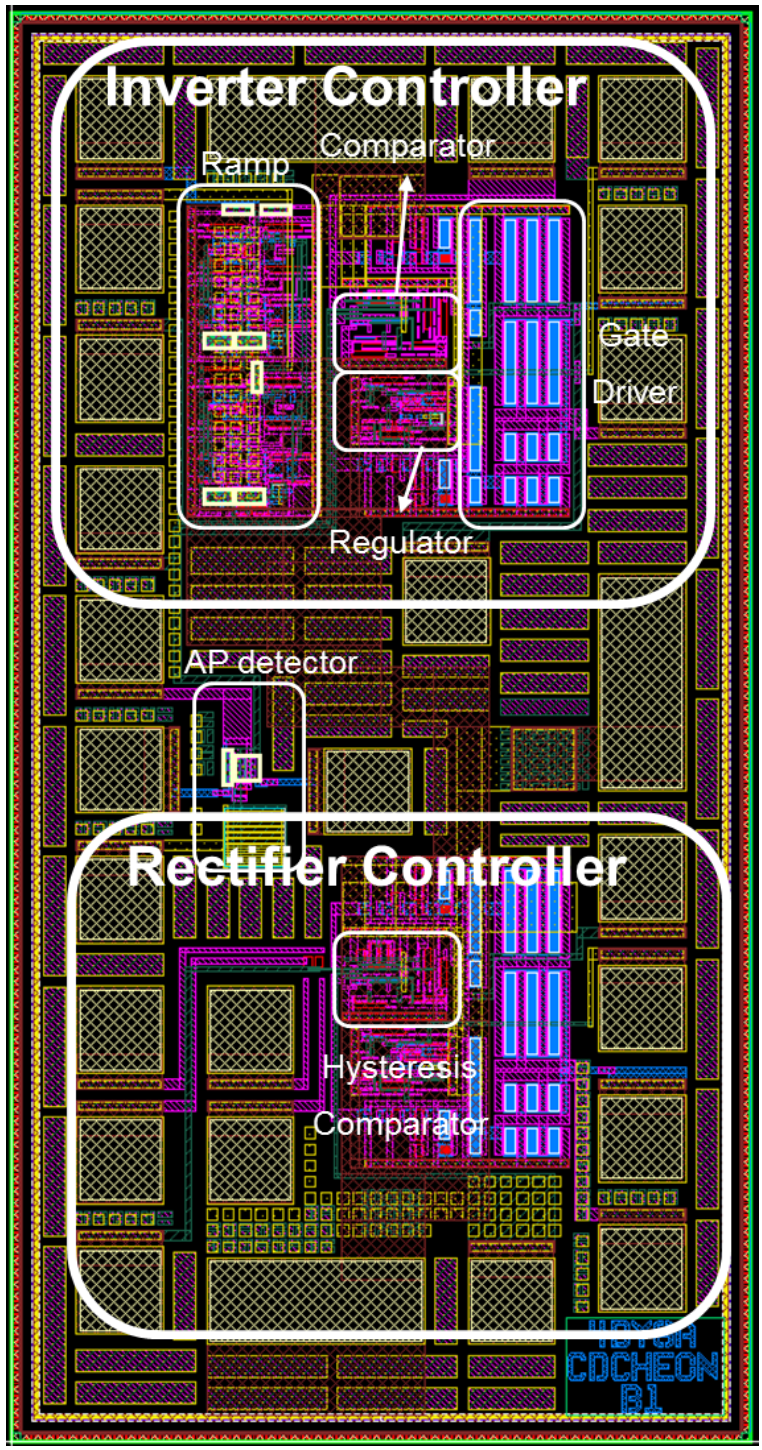



**Figure 35 Layout of the CMOS circuit**

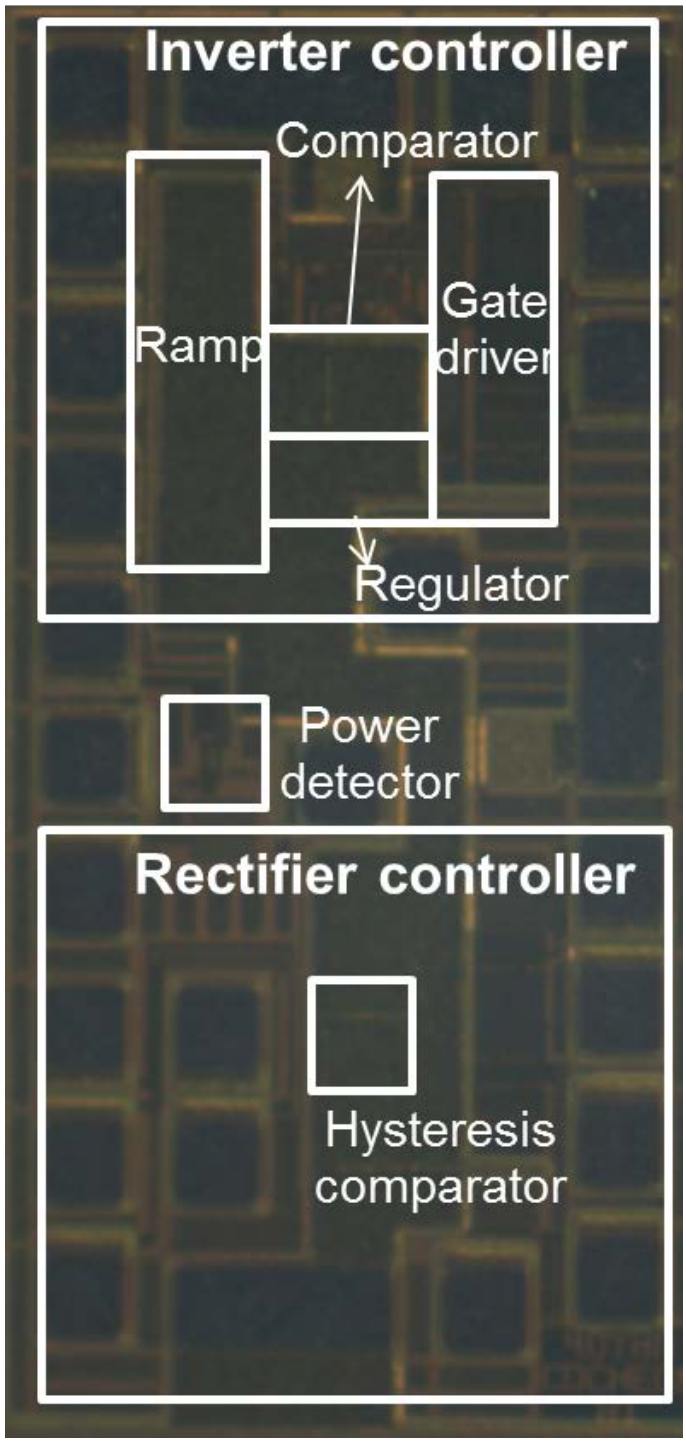



**Figure 36 Photograph of the CMOS circuit**

## 2.5. Measurement: Hybrid Modulator with CMOS and GaN HEMT

### 2.5.1. CMOS Control Circuit Results

CMOS control circuit is fabricated using IBM 0.18um SOI 2.5V RF technology. The fabricated CMOS is working good as it will be shown in the following. Although the CMOS control circuit is designed under the assumption of supply voltage of 5V and the reference voltage at ground, it also worked for -4V as the reference voltage with 1V of supply voltage in both simulation and measurement, perfectly to feed GaN HEMT switch. From now on, it should be noted that the CMOS controller is biased with the supply voltage of 1V and the reference voltage of -4V.

Because it was impossible to locate pads in between each component, detailed analysis of each component cannot be performed. However, the waveform for ramp generator and PWM can be seen with oscilloscope. In Figure 37, the output of the ramp generator is shown. Additionally, to test if PWM is working properly, a random signal is applied to the other side of comparator. The output as a result is as shown in Figure 38.

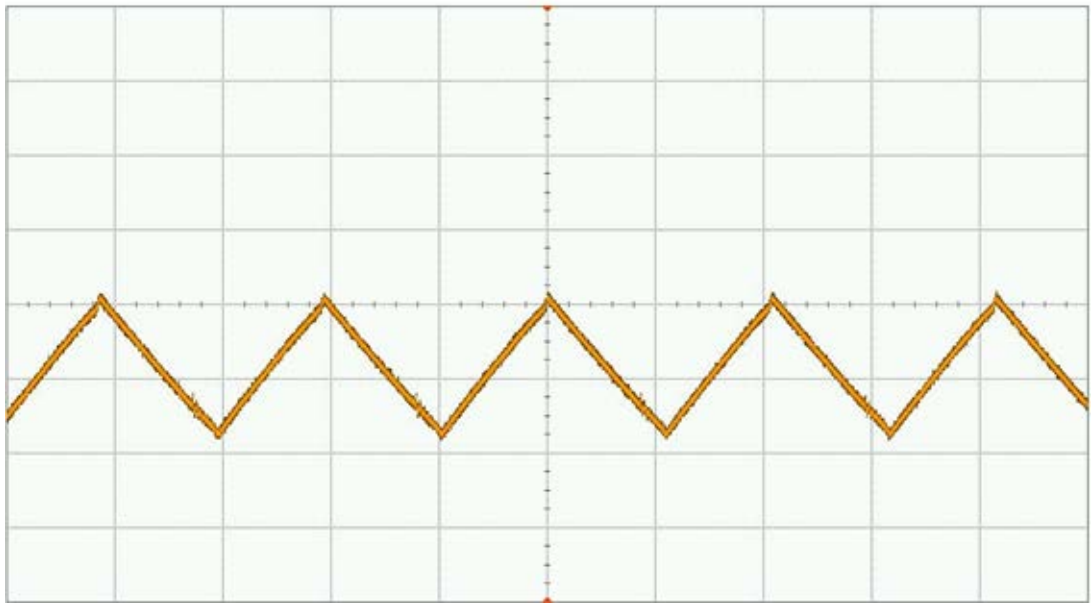


**Figure 37 Ramp Generator Output.**

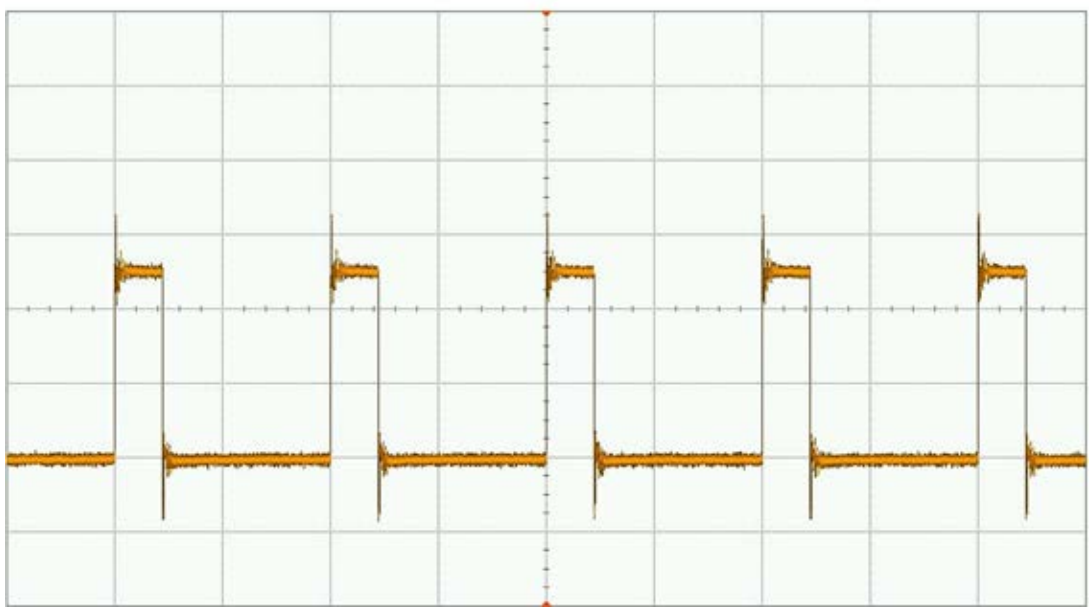


**Figure 38 PWM Output at a certain voltage input.**

After the testing the CMOS die, the overall power consumption of the die is calculated using supply voltage and current. According to the display of the power supplies, it shows 6mA of current flows through the CMOS chip when 5V with ground as the reference is applied. This is a 30mW consuming control circuit. Since the designed supply modulator is handling over 10W, 30mW is smaller than 1/300 of total power. Therefore, the power dissipated by the CMOS control circuit is neglected.

There are only two screen shots due to lack of tuning pads, however, it can be concluded the CMOS design is working properly. The next step is to apply this CMOS to a hybrid GaN HEMT supply modulator.

## 2.5.2. Hybrid Modulator Results

Fabricated CMOS using IBM 0.18um SOI 2.5V RF technology and hybrid GaN HEMT Class $E^2$ DC-DC Converter has been combined to form as a supply modulator. In this thesis, GaN HEMT model CGH60120D from Cree Inc. with 360 um of unit gate width and 28.8 mm of total gate width is used. On resistance of this model is 0.1 ohm and the input capacitance is 34pF. The output capacitance is 7.7pF.

In Figure 39, the schematic for the Class $E^2$ DC-DC Converter is shown again with variable names; $L_s$ is a supply inductor, $C_{pi}$ is a inverter parallel capacitor which is charged and discharged according to current flow and switch status, $L_r$ and $C_r$ are a inductor and a capacitor for the series LC resonator, respectively, $C_{pr}$ is a rectifier parallel capacitor working similarly to the inverter parallel capacitor, $L_{lpf}$ is a low pass filter inductor and $C_{lpf}$ is a low pass filter capacitor. The value of each component are written in the following Table 1. With the value written in Table 1, measurement has been performed. A photograph of the test module is shown as Figure 40. The results of the measurement are shown in Figure 41 and Figure 42.

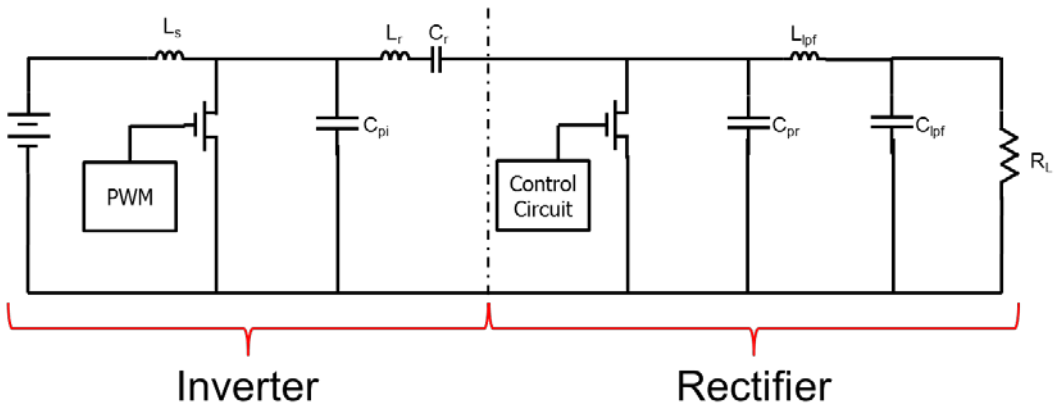



**Figure 39 The schematic for Class E2 DC-DC Converter with variable name.**

**Table 1 Parameters for Class E DC-DC Converter**

| Ls | Cpi | Lr | Cr | Cpr | Llpf | Clpf | RL |
|---|---|---|---|---|---|---|---|
| 220uH | 1.18nF | 20uH | 37.7nF | 1.18nF | 220uH | 0.5uF | 102.5 Ω |

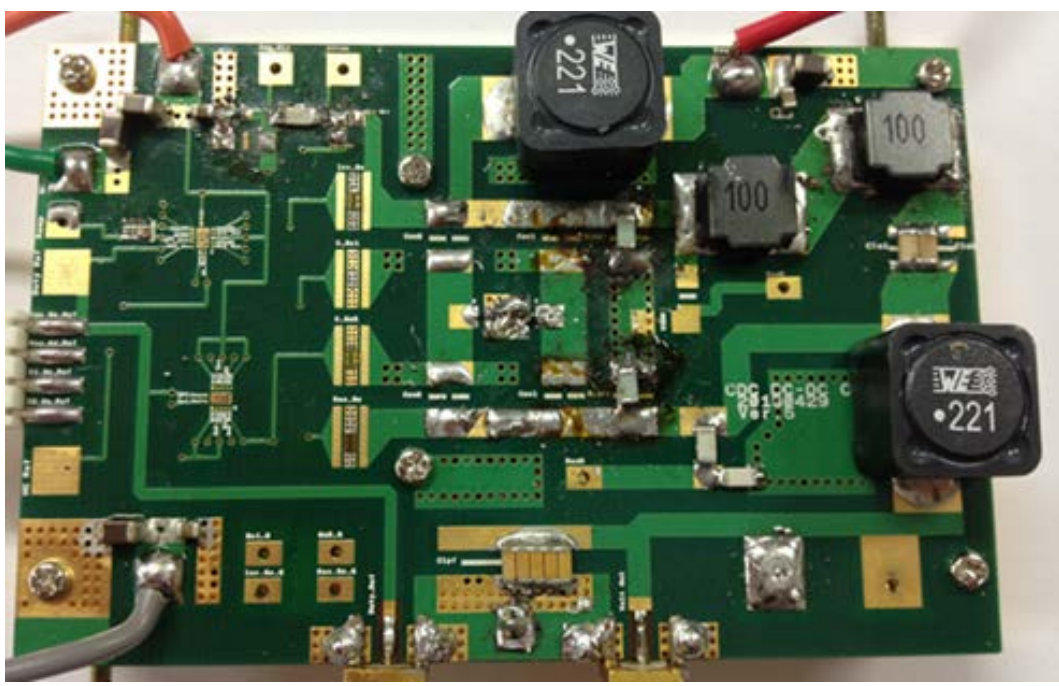



**Figure 40 Photograph of the test module.**

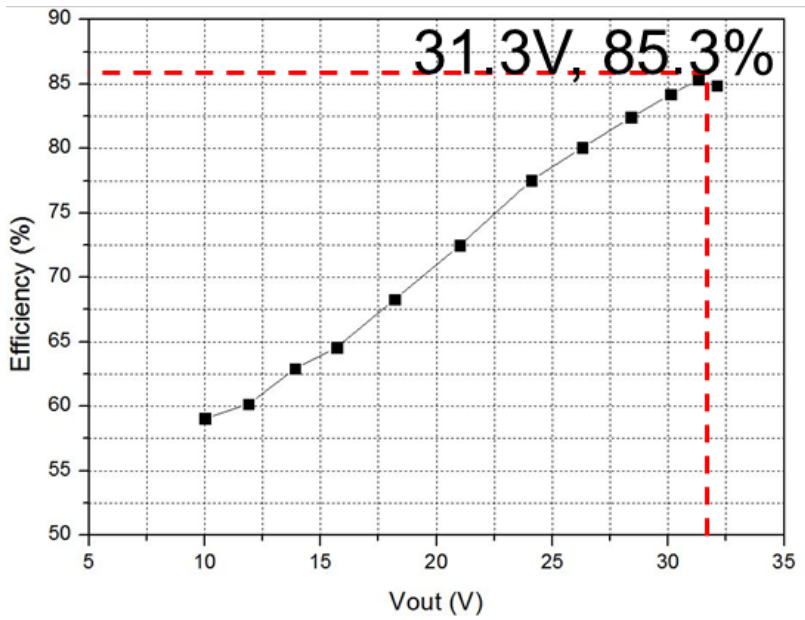



**Figure 41 Efficiency vs. Output Voltage**

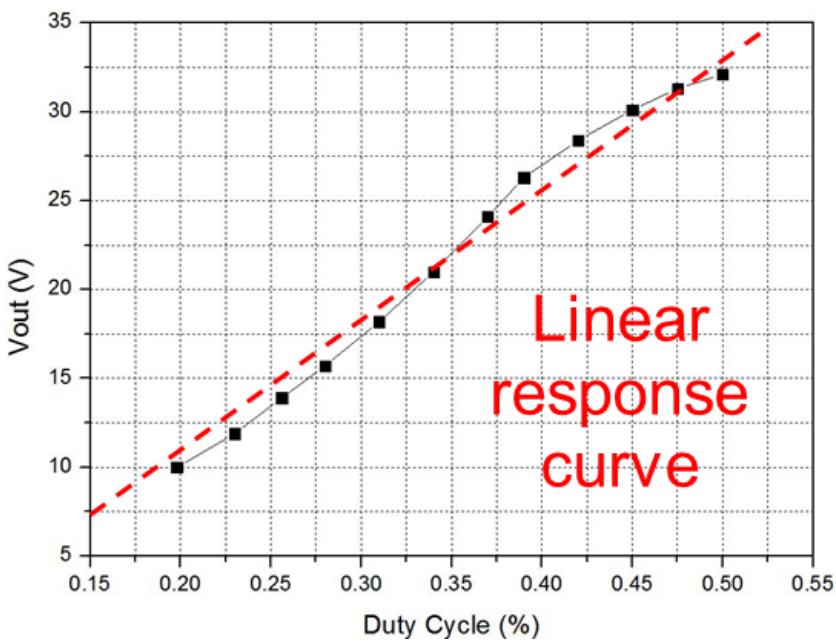



**Figure 42 Output Voltage depending on Duty Cycle.**

According to the Figure 41 and Figure 42, the supply modulator output voltage range is 10V to 32V when the duty cycle is in between 0.2 to 0.5. The peak efficiency of the DC-DC Converter is 85.3% when duty cycle is about 0.475 and 31.3V is outputted. It is well shown that the output voltage decreases when the duty cycle decreases. The efficiency also gets decrease as duty decreases. This is the main problem since the supply modulator is supposed to have constantly high efficiency. However in this work, Class-E inverter is adopted. The conduction angle for inverter becomes smaller from the optimum angle as the duty cycle becomes lower. In other words, the time for the inverter switch being in on-state is decreasing while the off-state is increasing as the duty cycle decreases. This results in increase of time for current to flow into the shunt capacitor in inverter too long that before the capacitor is fully discharged, the inverter switch will turn on. To help understanding, refer to Figure 7. The remaining charges in capacitor than flows through the on-state switch resulting in waste of energy. This is inevitable since the DC-DC converter is controlled by duty cycle. The solution to this problem is proposed and the measurement is performed in Chapter 5.

Table 2 shows the comparison of this work with other published supply modulators. Yet, there are only two of the supply modulators with GaN and the [7] and [8] are published from the same lab. Since there is not enough for references, supply modulators with other technologies are also compared. Refer to [12] the efficiency of the supply modulator in this work has similar performance. Although the difference in switching frequency is big, the peak efficiency of this work is higher than [7] and [8].

**Table 2 Comparison table for supply modulator**

| Ref | $f_{switching}$ | $V_{out}$ | $\eta_{peak}$ | Topology | Technology |
|---|---|---|---|---|---|
| **2010 [9]** | 700 kHz | 3.3 V | 96 % | Buck-Boost | CMOS |
| **2010 [10]** | 2 MHz | 12 V | 91 % | Flyback | LDMOS |
| **2011 [11]** | 2 MHz | 28 V | 70 % | Hybrid switching | LDMOS |
| **2012 [12]** | 5 MHz | 32 V | 84 % | Hybrid switching | LDMOS |
| **2012 [13]** | 5 MHz | 4 V | 91 % | Buck-Boost | CMOS |
| **2012 [14]** | 200 MHz | 2.4 V | 79 % | Buck | BiCMOS |
| **2013 [7]** | 200 MHz | 20 V | 64 % | Buck | **GaN** |
| **2013 [8]** | 200 MHz | 28 V | 73 % | Buck | **GaN** |
| **This work** | **1 MHz** | **32 V** | **85.3 %** | **Class $E^2$** | **GaN** |

## 2.6. Future Work

The strong advantage of Class $E^2$ DC-DC Converter is that it has potential to maintain high efficiency at high switching frequency. In this thesis, 1MHz of low switching frequency is used. One of the purpose of this thesis is to open up the development of supply modulator with GaN HEMT and thus, average power tracking system is chosen instead of envelop tracking system (ET). Because it is to realize the average power tracking system with GaN HEMT, no high switching frequency is essential. There is no modulation signal, but only continuous wave (CW) signal is used as an input power. As a result, 1MHz of low switching frequency is enough to fulfill this thesis.

Upon the success realization of supply modulator in this chapter, the future work is presented in this section using ADS2009 update 1 simulation. The switching frequency of 100MHz, 200MHz, and 400MHz is applied to this Class $E^2$ DC-DC Converter topology in order to handle WCDMA and 16QAM LTE signal. Four different

cases are simulated and their conditions are written in Table 3.

**Table 3 List of cases and its conditions**

| | Modulation Type | Bandwidth | PAPR | Switching Frequency |
|---|---|---|---|---|
| **Case 1** | WCDMA | 3.84 MHz | 9.6 dB | 100 MHz |
| **Case 2** | LTE 16QAM | 10 MHz | 9.42 dB | 200 MHz |
| **Case 3** | LTE 16QAM | 20 MHz | 9.68 dB | 200 MHz |
| **Case 4** | LTE 16QAM | 20 MHz | 9.68 dB | 400 MHz |

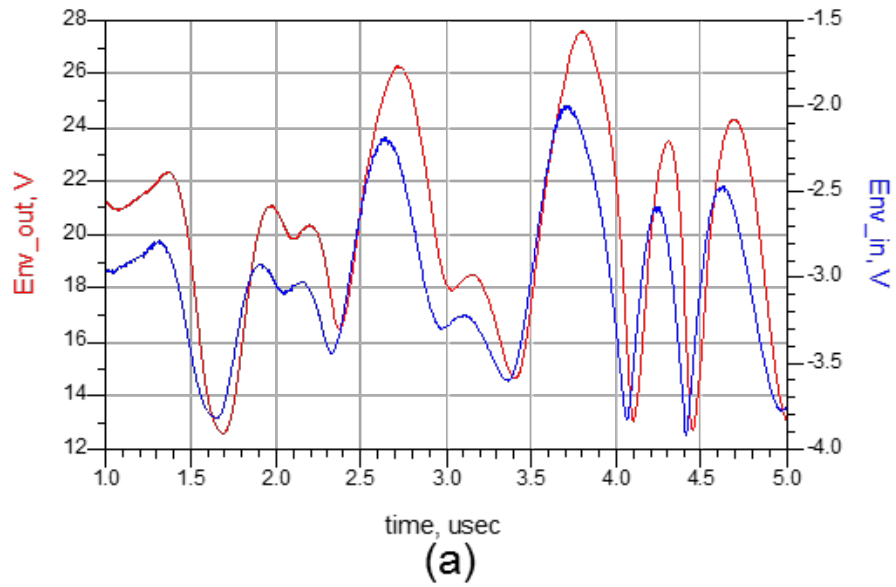
For case 1, envelop signal of WCDMA with bandwidth of 3.84MHz and 9.6dB of peak-to-average power ratio (PAPR) is used. The switching frequency of supply modulator is 100MHz. The resulting waveform with input waveform of envelop is presented in Figure 43. The estimated average efficiency is 78% with average load voltage of 21V. The output voltage ranged from 12V to 28V.

For case 2, 10MHz LTE 16QAM is used which PAPR is 9.42 dB. When 200MHz of switching frequency is used, the supply modulator produces 76% of estimated average efficiency with load voltage of 16.8V. The output voltage ranged from 12V to 27V as shown in Figure 44.

Figure 45 shows the result of case 3, where 20MHz LTE 16QAM with PAPR of 9.68dB is applied as an input signal of supply modulator which having 200MHz of switching frequency. The result shows the estimated efficiency of 79% with 18.8V of load voltage. The output voltage range is 12V to 24V.

The last case is 20MHz LTE 16QAM with 400MHz switching frequency. The estimated average efficiency is 76% while load average voltage is 19.5V. The output voltage range still shows 12V to 25V. This output voltage range can be adjusted by tuning the elements in DC-DC converter. The graphical representation is shown in Figure 46.

The results of the 4 simulations are tabled in Table 4. It should be noted that for all 4 cases, the efficiency does not fall meaning that the increase in switching frequency does not affect efficiency. This is a notable achievement since conventional buck converter or other type of DC-DC converter drops its efficiency as switching frequency increases.



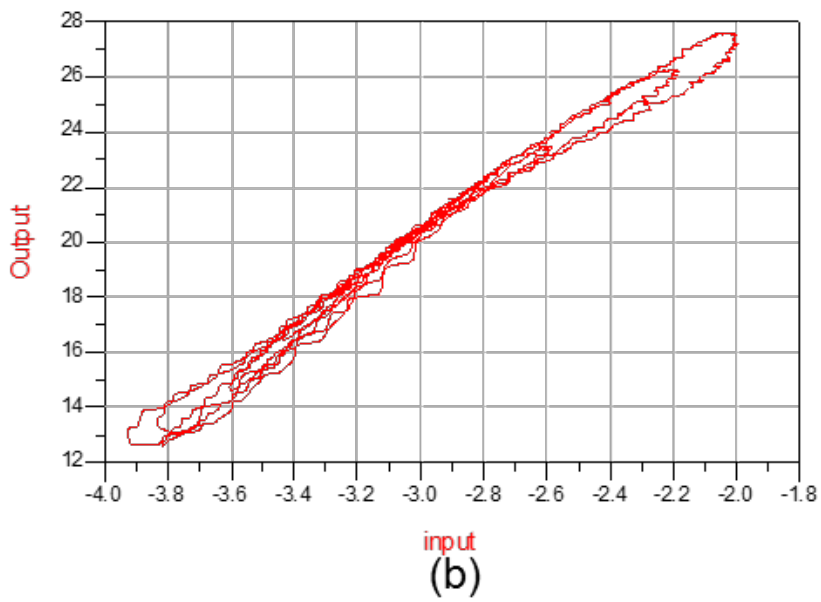




**Figure 43 Case 1 (a) input and output envelop waveform and (b) output voltage according to input level.**

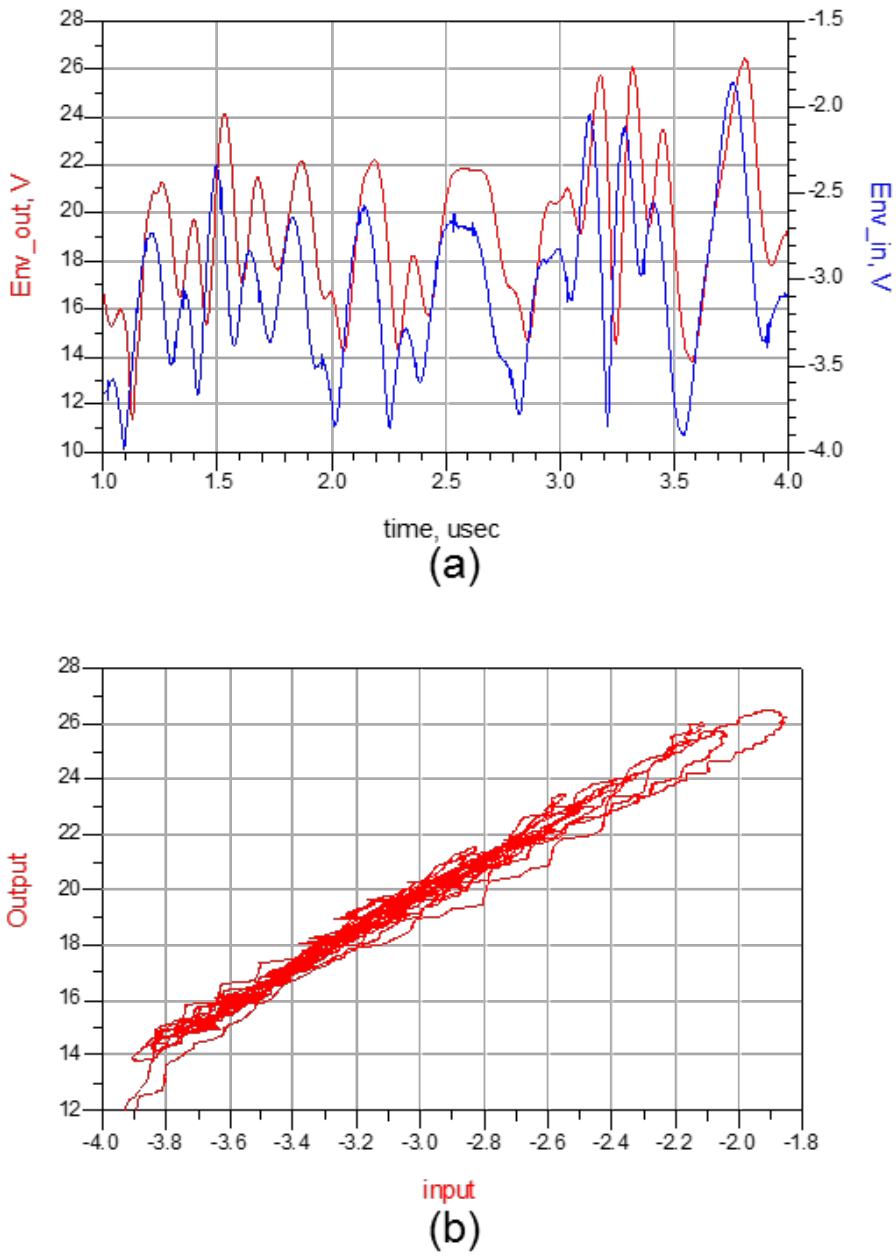
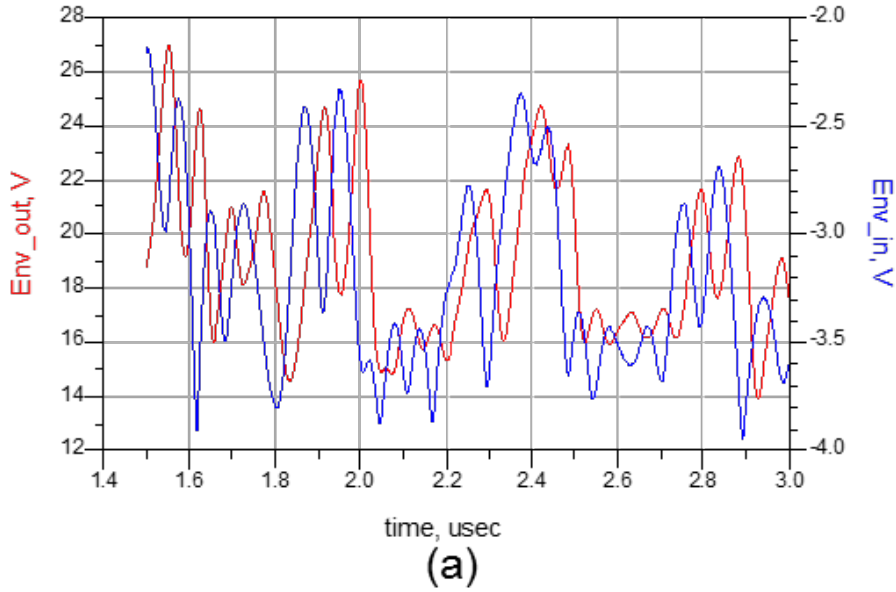



**Figure 44 Case 2 (a) input and output envelop waveform and (b) output voltage according to input level.**



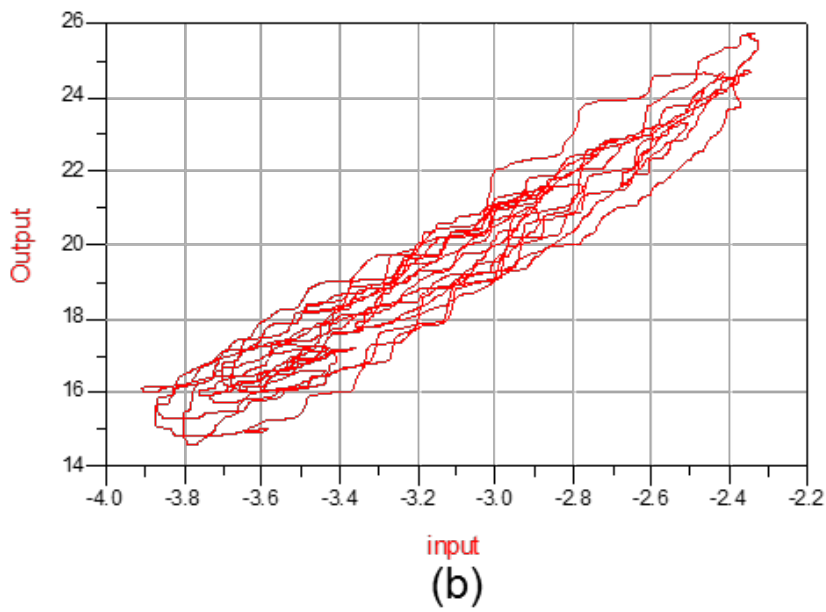




**Figure 45 Case 3 (a) input and output envelop waveform and (b) output voltage according to input level.**

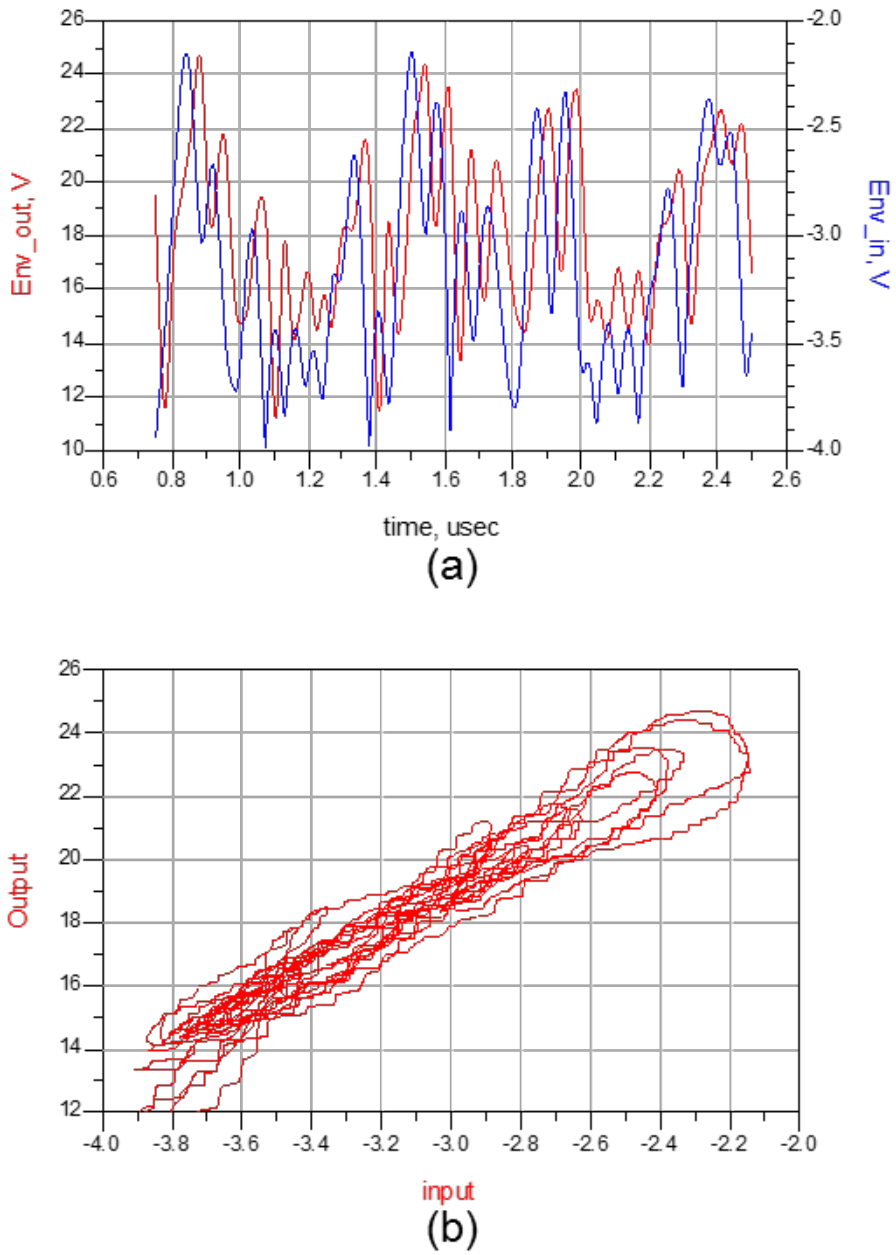



**Figure 46 Case 4 (a) input and output envelop waveform and (b) output voltage according to input level.**

**Table 4 Results of case simulations**

| | Switching Frequency | Estimated Efficiency | Average Load Voltage | Output Voltage Range |
|---|---|---|---|---|
| **Case 1** | 100 MHz | 78 % | 21.0 V | 12 V – 28 V |
| **Case 2** | 200 MHz | 76 | 16.8 | 12 V – 27 V |
| **Case 3** | 200 MHz | 79 | 18.8 | 14 V – 26 V |
| **Case 4** | 400 MHz | 76 | 19.5 | 12 V – 25 V |

Most DC-DC converters produces square wave with switches and convert it to DC power with low pass filter. However, the parasitic capacitance between the drain and source of the power transistor causes a distortion in square wave. This distortion directly relates to the efficiency of the modulator, and the effect of source-to-drain capacitance becomes significant as the switching frequency increases.

On the other hand, the Class $E^2$ DC-DC Converter does not have such problem. It adopts the topology of class-E power amplifier which uses source-to-drain capacitance as a shunt capacitor required in its topology. Therefore, the weakness of the conventional DC-DC converter is now become the essential component in Class $E^2$ DC-DC Converter. Additionally, class-E inverter can handle a few GHz and it has been already proved by the fact that there are countless work on Class-E power amplifiers in GHz range including this thesis in Chapter 3.

The second biggest advantage of this topology is that it does not have linear stage which is a power consumer. Without a linear stage, the Class $E^2$ DC-DC Converter can handle high switching frequency by itself. In conclusion, the Class $E^2$ DC-DC Converter topology has great potentials to be highly efficient at high switching frequency.

## 2.7. Conclusion

Operational principle of Class $E^2$ DC-DC Converter has been discussed and the required CMOS control circuit is mentioned. Each component in CMOS control circuits, including OP Amps for ramp generator, comparator, hysteresis comparator, voltage regulator and gate driver, is designed thoroughly and its normal operation has been checked. With Cree Inc.'s CGH60120D GaN HEMT and working CMOS control circuits, the whole system of Class $E^2$ DC-DC Converter is realized. The measurement result shows the maximum efficiency of 85.3% with 31.3V of output voltage at 0.475 duty cycle. The advantage of the Class $E^2$ DC-DC Converter is discussed and proved its potential of high efficiency at high switching frequency using simulation.

# 3. Power Amplifier

## 3.1. Introduction

A switching mode amplifier provides a very high efficiency while linearity and bandwidth is poor relative to linear amplifier. In the ideal switching amplifier, the active device works as a perfect switch meaning when it is turned on, the current flows from drain to source without a voltage drop and when it is turned off, no currents can flows but voltage drop across the drain and source is formed. With this assumption, there will be no overlap between the current and the voltage across the drain and source at any point. This will result in zero DC power dissipation in the transistor and 100% of efficiency. Although non-ideal characteristics, such as finite on-resistance of active device prevents the amplifier to reach 100% of efficiency in reality, switching amplifier is dominant over linear amplifier in terms of efficiency. In this chapter, the topology for Class-E Power Amplifier, 2-Stage Class-E Power Amplifier design procedure and measurement results will be discussed.

## 3.2. Class E Power Amplifier

The waveform of Class-E inverter has been discussed in Chapter 2. The operation principle of the Class-E Power Amplifier (PA) is almost the same as Class-E inverter designed previously. However in chapter 2, the purpose of Class-E inverter is to produce current sine wave that would transfer to the rectifier and the amplitude of it is determined by PWM. Since it was designed at 1MHz, the values of lumped elements are quite large and thus, parasitic elements of an active device can be ignored. Alternatively, Class-E PA that will discuss here will have frequency of 5.8GHz where all the parasitic components become dominant at harmonics. A close attention to the topology should be made in order to properly design a Class-E PA. Basically, the waveform of Class-E PA is the same as discussed in Chapter 2, so it will not be mentioned in detail here, although, numerical analysis of Class-E PA will be added.

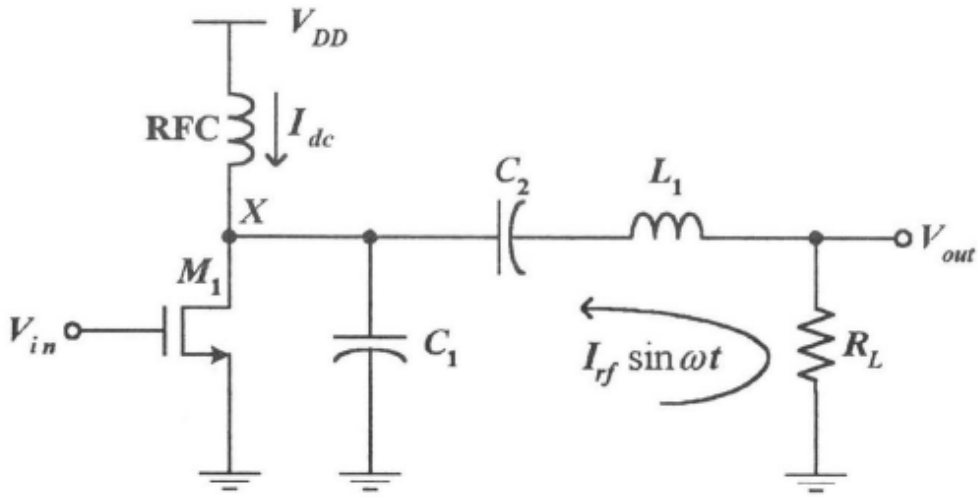



**Figure 47 Basic schematic of Class-E Power Amplifier. [20]**

Figure 47 shows the basic schematic of Class-E PA. It is composed of one active device as a switch, an inductor for DC feed, shunt capacitor, and a series LC resonant circuit for filter that passes fundamental frequency. Because of series LC resonant circuit, it can be seen as a sine wave current source. Figure 48(a) depicts sum of sine wave current and DC current supplied. When the active device in turned on, partial sine wave of current flows through the active device. This is shown in Figure 48(b), plotting the current flow through the active device. Figure 48(c) shows the current flowing into the shunt capacitor. When the current flowing into the capacitor is positive, the voltage is built up across the capacitor while it gets discharged when the current starts flowing in negative way. This is illustrated in Figure 48(d).

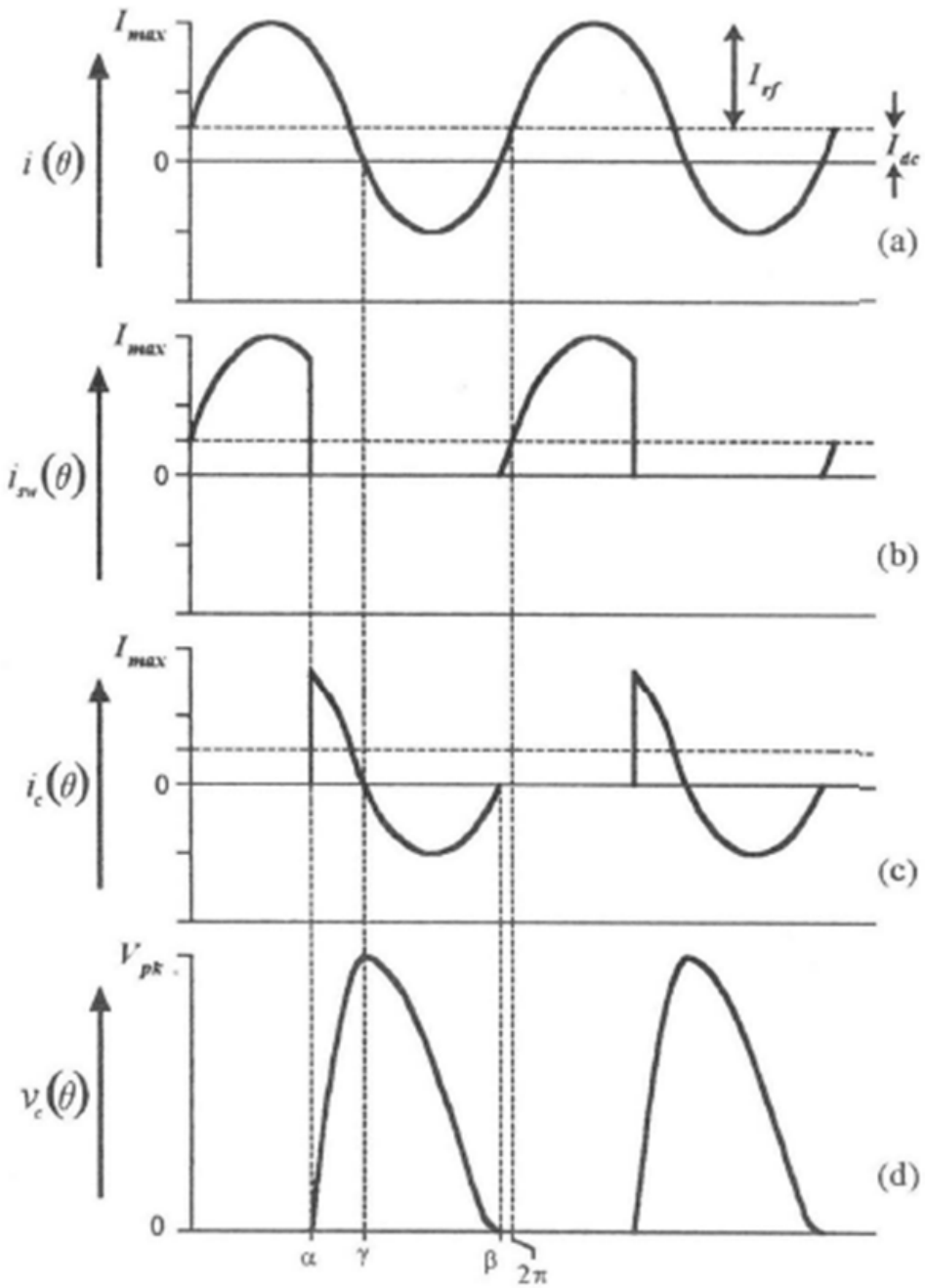



**Figure 48 Voltage and current waveform of the Class-E PA. (a) Summation of the switch current and capacitor current. (b) Current waveform flowing in the transistor. (c) Current waveform flowing in the capacitor. (d) Drain voltage waveform. [20]**

The purpose of numerical analysis is to find the optimized value for shunt capacitor for a given supply voltage and a peak current. Therefore, it is desired to figure out how much DC current is flowing through the active device during its turn on state. The total current, sum of sine wave current and DC current from supply, can be written as,

$$I(\theta) = I_{dc} + I_{rf} \sin\theta$$

To calculate desired shunt capacitance, it is desired to know how much current is flowing into the active device. So from Figure 48(b), the current flowing into the active device is integrated as following, where $\alpha$ is the conduction angle, phase when the switch is turned on, $\beta$ is the phase when the total current level crosses zero from negative to positive, $I_{dc}$ is the current from the supply through the inductor, $I_{rf} \sin\theta$ is the current transferred through the series LC resonator.

$$I_{dc} = \frac{1}{2\pi} \int_{\beta-2\pi}^{\alpha} I_{dc} + I_{rf} \sin\theta \, d\theta$$

From this equation, the relationship between $\alpha$ and $\beta$ can be computed as,

$$\sin\beta = \frac{\cos\beta - \cos\alpha}{\alpha - \beta}$$

meaning that if $\alpha$ is chosen arbitrary, $\beta$ is decided automatically.

DC current, $I_{dc}$, and RF current, $I_{rf}$, is unknown parameter, however, the maximum amplitude of current wave can be defined as $I_{pk} = I_{dc} + I_{rf}$. If the total

current is normalized, the following equation can be made.

$$I(\theta) = I_{dc} \cdot (1 + m\cos(\theta))$$

where

$$m = \frac{I_{rf}}{I_{dc}}$$

As a result, DC current, $I_{dc}$ and RF current, $I_{rf}$, can be calculated as,

$$I_{dc} = \frac{I_{pk}}{1+m}$$

$$I_{rf} = \frac{I_{pk}}{1+1/m}$$

From the current flowing into the active device, current flowing into the shunt capacitor can be also calculated. Although the voltage across the shunt capacitor instantaneously changes, the average of it should be equal to supply voltage. With this fact, the value for shunt capacitor is calculated as follows.

$$V_{dc} = \frac{1}{\omega C_p} I_{pk} v_{dc}(\alpha)$$

## 3.3. Extraction of Parasitic Elements

Since the frequency of 5.8GHz is high enough for the PA to be affected by parasitic elements, modeling of an active device is required. Using "Modelman" program, each of parasitic elements in GaN HEMT CGH60008D from Cree Inc. is

extracted. The most important factor in designing Class-E PA is the shunt capacitor. Thanks to high designing frequency, the parasitic capacitance seen from the drain to source can be used as shunt capacitor in Class-E PA. As the frequency increases, Miller Effect also needs to be considered. Therefore, in this section, capacitances between gate-to-drain and drain-to-source are computed.

Figure 49 shows the extracted drain-to-source capacitance of the CGH60008D depending on drain-to-source voltage at 5.8GHz using "Modelman" program. Each of plots indicates the gate bias level from -3.6V to 0V. As the drain to source voltage decreases, the drain-to-source capacitance shows nonlinearity. However as the drain-to-source voltage increases, the capacitance tends to converge.

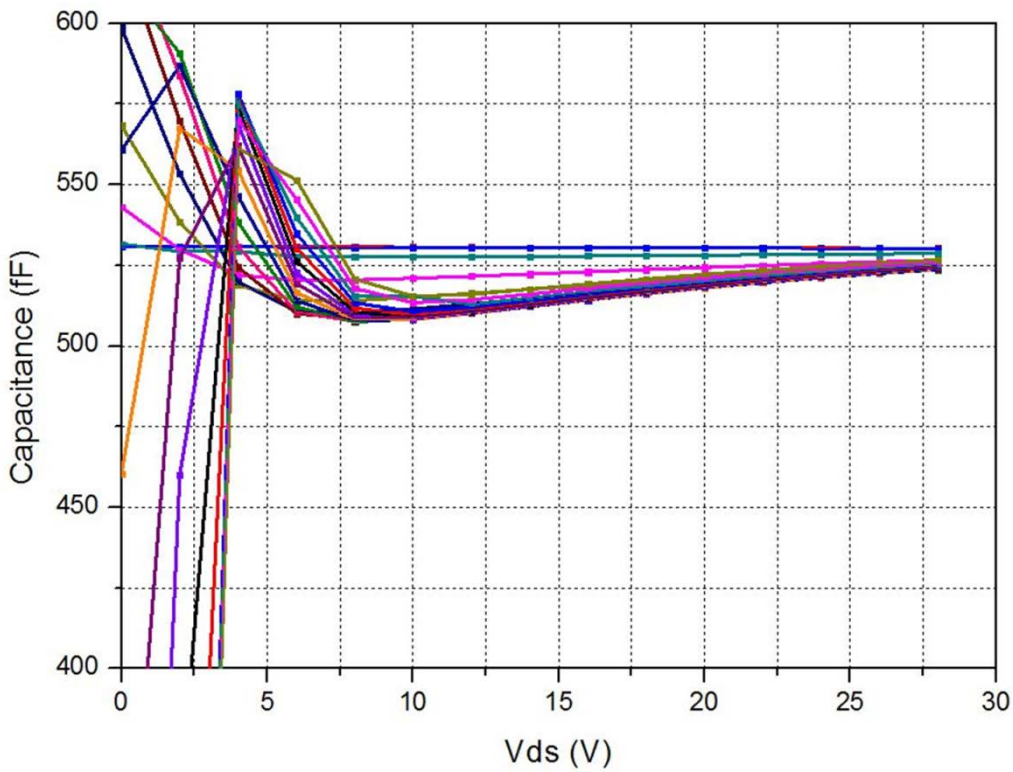



**Figure 49 Extracted drain-to-source capacitance of the CGH60008D by gate bias depending on drain-to-source voltage.**

As the frequency increases, the effect of gate-to-drain capacitance begins to appear. Therefore with the same method, gate-to-drain capacitance is also modeled and depicted in Figure 50. Similar to drain-to-source capacitance, nonlinearity of capacitance is noticeable at low drain-to-source voltage. In designing power amplifier, this nonlinear capacitance cannot be accounted, instead, a fixed value of capacitance needs to be assumed. Before picking the fixed value of capacitance, the total output capacitance seen from the drain node of a transistor must be computed first.

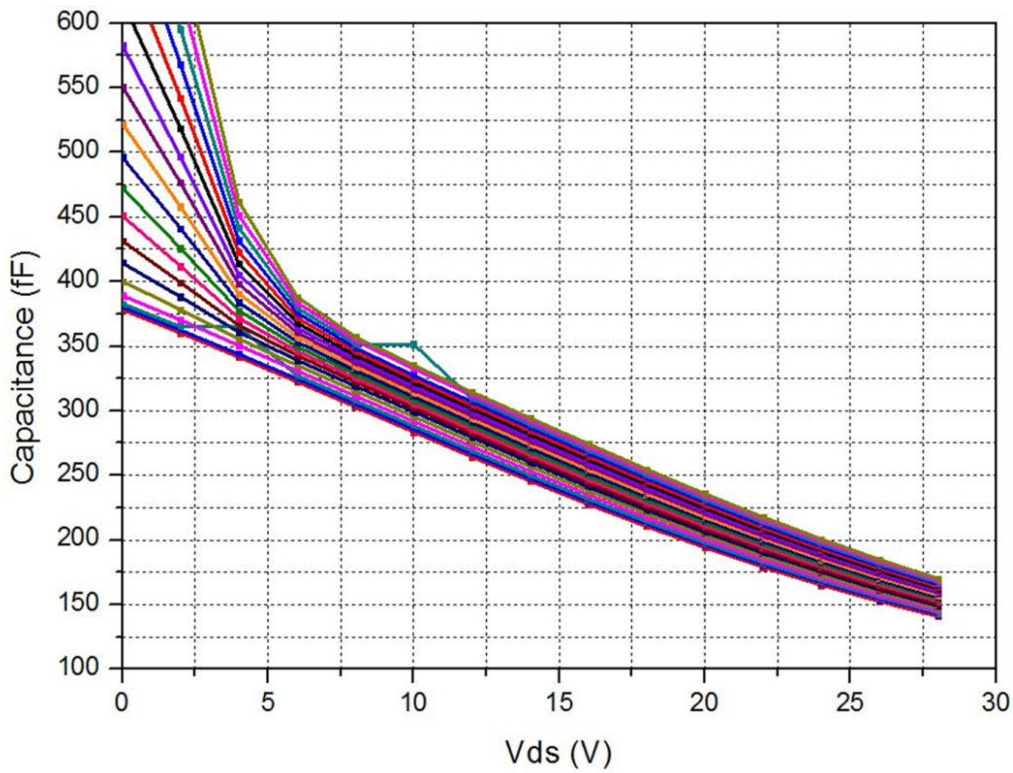



**Figure 50 Extracted gate-to-drain capacitance of the CGH60008D by gate bias depending on drain-to-source voltage.**

To calculate shunt capacitance of an active device, Miller Effect is considered. When there is a series impedance, $Z$, with a gain of $-K$, as illustrated in Figure 51, it can be divided in to two impedance, $Z_{in}$ and $Z_{out}$.

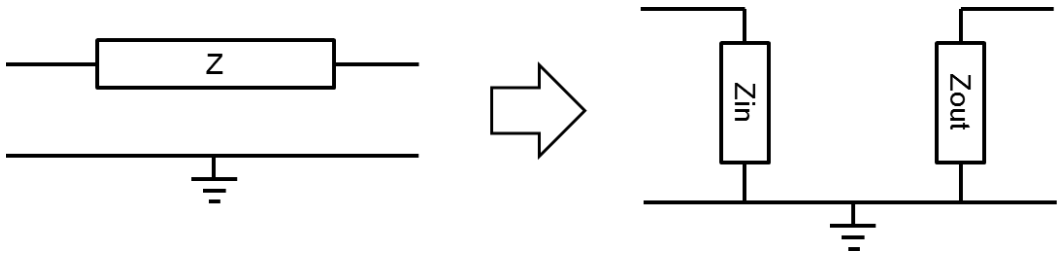



**Figure 51 Graphical representation of the miller effect.**

In this case, Z is the gate to drain capacitance. Then, $Z_{out}$ becomes,

$$Z_{out} = Z/\left(1 - \frac{1}{K}\right)$$

The partial gate-to-drain capacitance, $C_{gd}$, seen from the drain node is then,

$$C_{gd,} = C_{gd} \cdot \left(1 + \frac{1}{A}\right)$$

where $K = -A$, which is a gain.

The gain $A$ of a transistor is equal to $g_m r_o$ and those are extracted from ADS2009 Update 1 with a model provided by Cree.

$$g_m = 0.008$$
$$r_o = 2400$$
$$\therefore A = 19.1$$

The partial gate-to-drain capacitance, $C_{gd}$, seen from the drain node of the CGH60008D GaN HEMT can now be computed. With the result of this Miller Effect, total output capacitance seen from the drain node at every point is calculated and plotted in Figure 52.

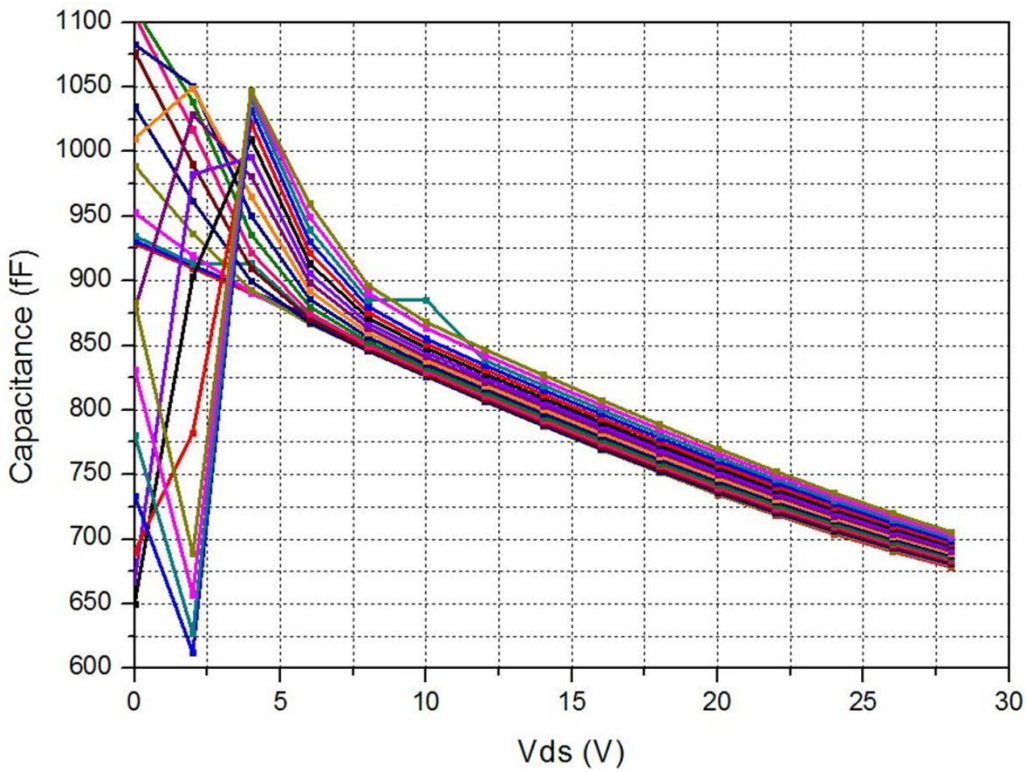



**Figure 52 Calculated total output capacitance of the CGH60008D by gate bias depending on drain-to-source voltage.**

When PA is realized and measured, the drain-to-source voltage swing occurs. This means that the drain-to-source voltage is not at fixed point, but keeps moving high and low. Although the output capacitance is calculated only for valid range of drain-to-source voltage of 5V to 28V, the trend of output capacitance can be assumed.

## 3.4. Two-Stage Class-E Power Amplifier

In this thesis, Two-Stage Class-E PA is designed. Because the transistor CGH60008D is the smallest in product line, both stages are designed with same size of transistor. Instead of making the driver-stage small in size, the supply voltage of driver-stage is reduced to 1/3 of power-stage supply voltage, which would be 10V for driver-stage and 28V for power-stage. Thus, the design parameters must be considered differently.

With the total output capacitance calculated in the previous section, initial calculation for series LC resonant circuit is performed. According to the calculation, the parameters are computed as shown in Table 5.

**Table 5 Parameters for Class-E Operation**

| $V_{dc}$ (V) | $R_L$ (Ω) | $C_p$ (pF) | Freq(MHz) | $L_s$(nH) | $C_s$(pF) | $C_{ITp}$(pF) | $L_{ITs}$(nH) |
|---|---|---|---|---|---|---|---|
| **28** | 10.12 | 0.69 | 5806 | 1.52 | 0.69 | 1.09 | 0.55 |
| **10** | 8.22 | 0.8 | 5809 | 1.44 | 0.68 | 1.24 | 0.51 |

Although $R_L$ is the load impedance, it is necessary to have 50 ohm termination at the end of amplifier. Thus, impedance transformation is required. On the right column, there are $C_{ITp}$ and $L_{ITs}$. $L_{ITs}$ is a series inductor and $C_{ITp}$ is a parallel capacitor, both together make up the impedance transformation 50 ohm to desired load impedance. The values in the Table 5 are only the guiding values for initial design. Using these values, load matching for Class-E operation has been designed with ideal components. With a little bit of tuning, the following load matching S-parameter is obtained as depicted in Figure 53. After some tuning to achieve higher efficiency, the new values for lumped elements are tabled in Table 6. Compare to Table 5, there are not much differences.

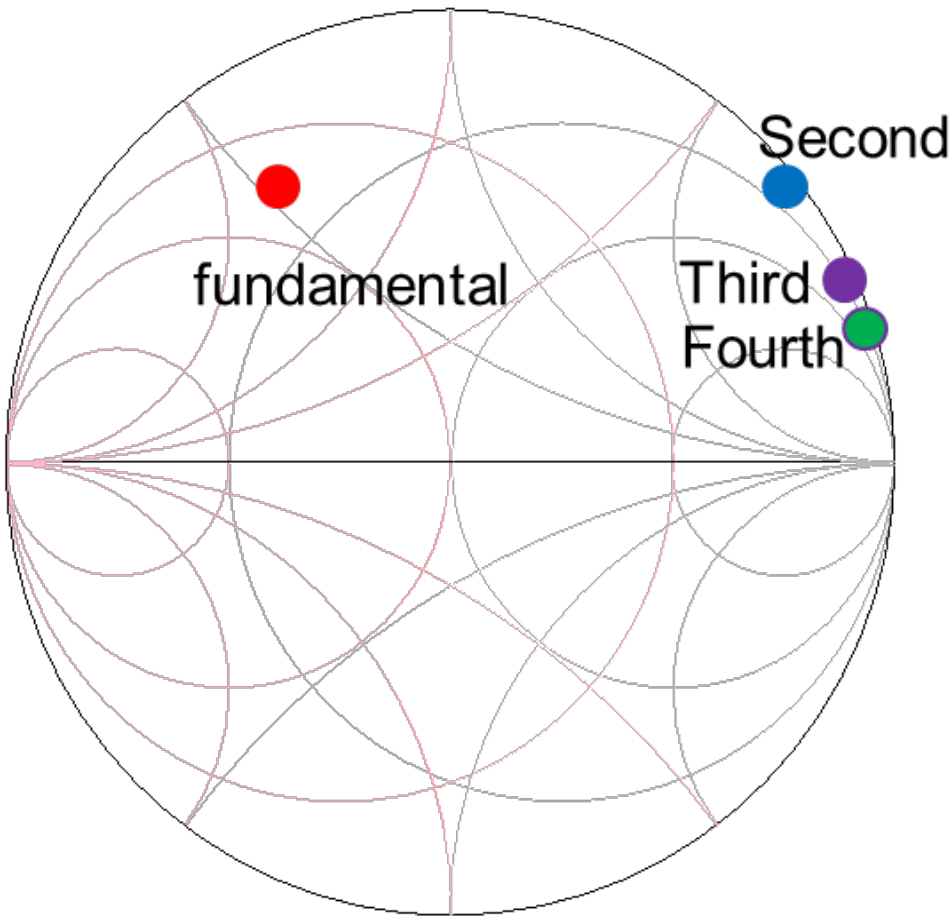



**Figure 53 Fundamental and harmonic load impedances of the Class E amplifier using ideal components.**

**Table 6 Revised parameters for Class E operation**

| $V_{dc}$ (V) | $R_L$ (Ω) | $C_p$ (pF) | Freq(MHz) | $L_s$(nH) | $C_s$(pF) | $C_{ITp}$(pF) | $L_{ITs}$(nH) |
|---|---|---|---|---|---|---|---|
| **28** | - | 0.69 | 5800 | 1.8 | 0.7 | 1.1 | 0.55 |

Note that the fundamental impedance is in its optimal point while second, third, fourth harmonics are gathered in open. This is because class E amplifier uses series LC resonant circuit, so that only fundamental frequency can pass through the series LC resonant circuit while the other harmonics are blocked.

The next step is to change the lumped elements to ideal microstrip lines. Because the PA is designed at high frequency, most of lumped elements cannot be used to realize the matching due to their low self-resonance frequency (SRF). In addition, as the frequency gets higher, the lumped elements shows its parasitic and loss. Therefore, minimum number of lumped elements are kept only for DC block and envelop short while the rest part of matching are done using microstrip lines. The new schematic using microstrip lines for load impedance is shown in Figure 54.

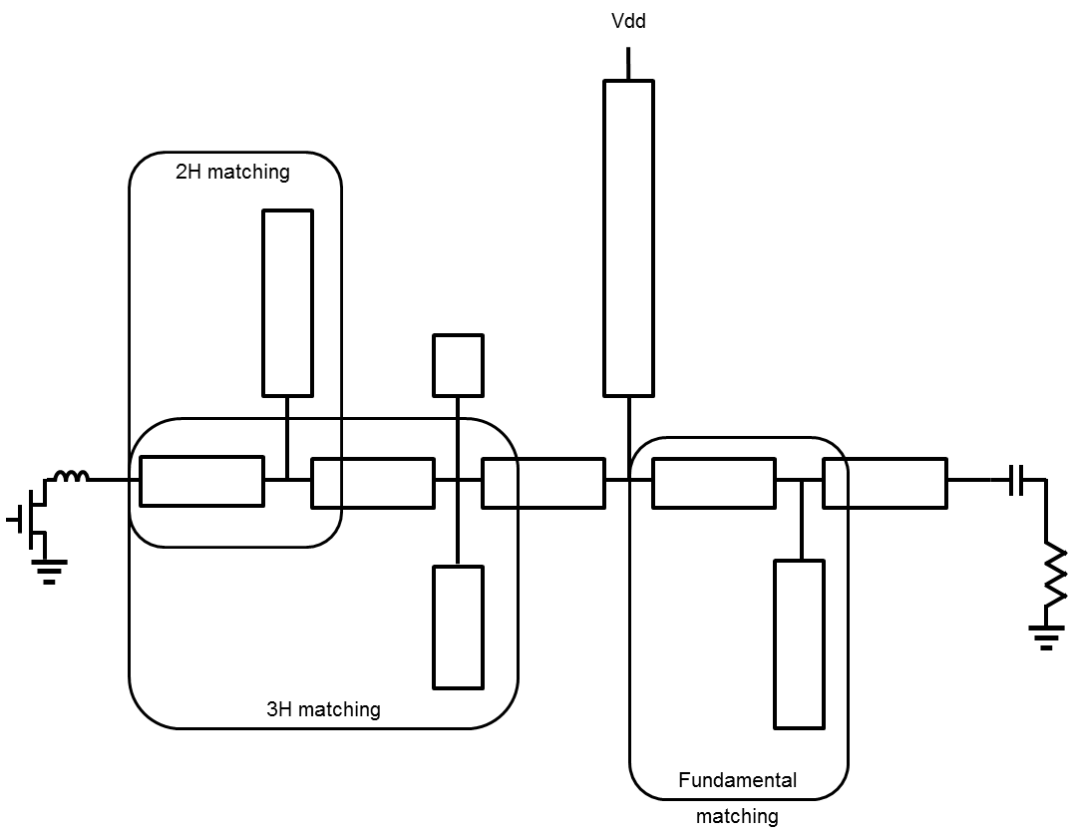



**Figure 54 Transmission line implementation of the load matching network.**

The second harmonic and the third harmonic are sent to open right after the shunt capacitor, which is internally located in the transistor as the output capacitance seen from the drain. The fourth harmonic was sent to pure reactive region, but its real value is not controlled, thus it may not be at open. Through the fundamental matching lines, fundamental impedance is located where it is desired to be. At the end of load matching, DC blocking capacitor takes place which is seen as short at fundamental frequency. The resulting load impedance S-parameter is shown in Figure 55. Although it is little bit changed from the lumped element design, the effect by its change is small enough to ignore.

The second harmonic matching comes the first because sending harmonics to the open is difficult. By obtaining series line and quarter wavelength of second harmonic stub in the first place, the second harmonic does not need to be considered thereafter. Same reason and method is applied to the third harmonic matching. Because the third harmonic affects a lot less on the efficiency of PA than the second harmonic in general, it comes after the second harmonic treatment. After the treatment for the second, the third, and the fourth harmonic, bias line comes in and the fundamental matching is performed with the series line and a shunt stub acting as a series inductor and a shunt capacitor, respectively.

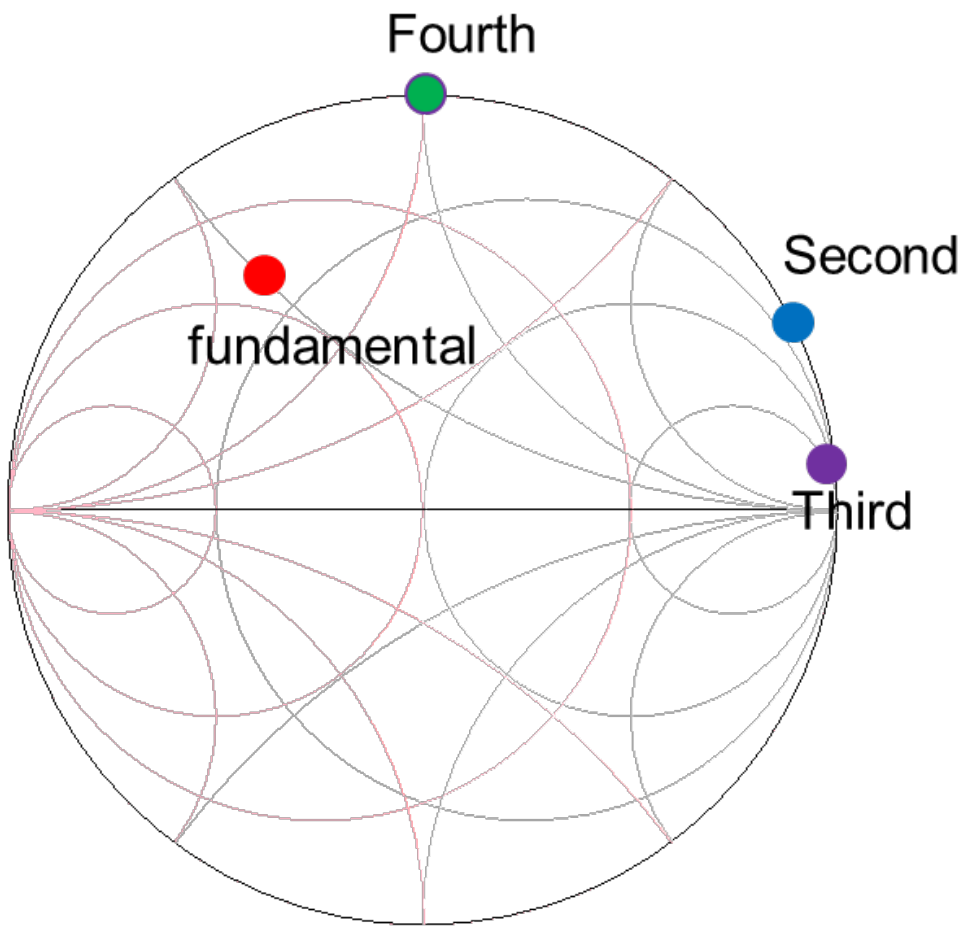



**Figure 55 Fundamental and harmonic load impedance of the designed class E amplifier using transmission line.**

The inter-stage matching is done in similar method. Since the driver-stage will have supply voltage of 10V, the optimum load impedance for the driver-stage is little different from the power-stage. According to Table 5, the optimum load impedance, $R_L$, for driver-stage is little less than the power-stage due to different supply voltage. Under such consideration, inter-stage matching has been performed.

The second harmonic treatment comes the first after the shunt capacitor, the drain-to-source capacitance in driver-stage transistor as shown in Figure 56. The reason is the same as it is in power-stage. In inter-stage however, differently from the

power-stage, no other harmonics are treated. This is because the inter-stage matching is the most sensitive part of the 2-Stage PA system. If there are shunt stubs for the third harmonic and the fourth harmonic, it will be very difficult to control the fundamental load in inter-stage. It will also present as obstacles during the measurement. In addition, the main purpose of the driver-stage is to push high power into the power-stage. Since the third harmonic affects about 5% of efficiency in general for one-stage power amplifier, it is assumed that the third or higher harmonic at the driver-stage level does not affect overall efficiency as much as it is at power-stage.

After the second harmonic treatment, the drain bias line comes in to play followed by a DC blocking capacitor. The DC blocking capacitor is a Murata GJM15 1005 capacitor value of 1.5pF. This is a high Q capacitor and the value is chosen where 5.8GHz is a short. After the DC blocking capacitor, shunt stub acting as a shunt capacitor with series line as a inductor comes in to play for fundamental load matching of driver-stage. The inter-stage matching network seen from the drain of driver-stage is illustrated in Figure 57. Meanwhile, the inter-stage matching should shape the input power coming in to gate of the power-stage. This is done by using the fundamental matching indicated in Figure 56 and the gate bias of the power-stage. Upon the simulation result, the second harmonic impedance looking from the gate of power-stage transistor into the inter-stage matching should be at slightly inductive region from the short ( $0 - j88$ ) as shown in Figure 58. According to theory, in order to maximize the waveform, even harmonic should be blocked in order to add up all the odd harmonic for input shaping. However, it is analyzed that when the second harmonic is sent to short region at the gate of transistor (when looking from the gate of power-stage transistor into inter-stage), the parasitic capacitance inside of the transistor will carry the second harmonic to open region. Therefore, the input shaping is done by placing the second harmonic to about $0 - j88$.

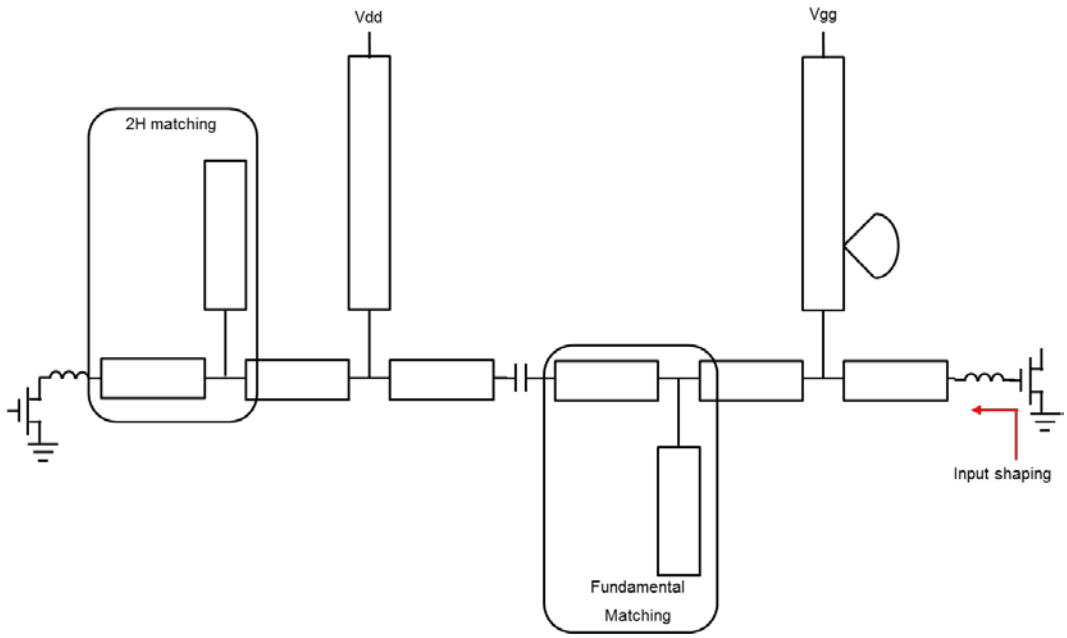



**Figure 56 Schematic diagram of inter-stage matching network.**

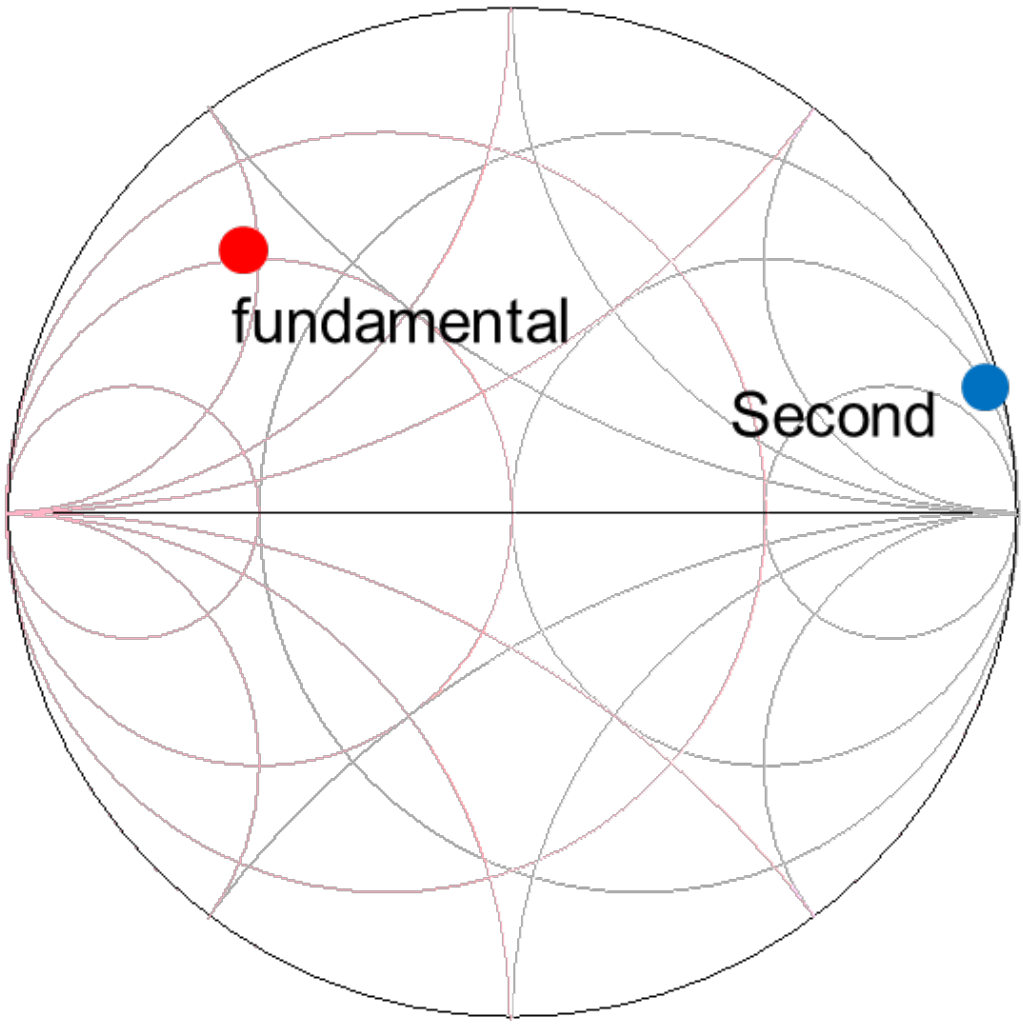



**Figure 57 Inter-stage matching network seen from the drain of driver-stage.**

The radial stub is used in the bias line. This is to make the bias line open at the second harmonic. For the fundamental frequency, a 1.5pF GJM15 capacitor is placed accordingly in order to make the bias line open as well. However, mentioned capacitor cannot short the second harmonic due to its SRF.

Input matching of the power amplifier is done with the same method described in above. The second impedance looking from the gate of driver-stage to the input is

placed to a slightly inductive region from the short in the Smith Chart. The rest of input matching is done by adding a high impedance series line as an inductor and a shunt stub as a shunt capacitor to place the input of power amplifier 50ohm. It should be noted that, when there is no input power, the input matching is not at 50ohm, but it is intended to become 50ohm as the input power increases. The input impedance looking from the outside of the system into the system is changing according to the input power level due to mainly the parasitic of the transistor.

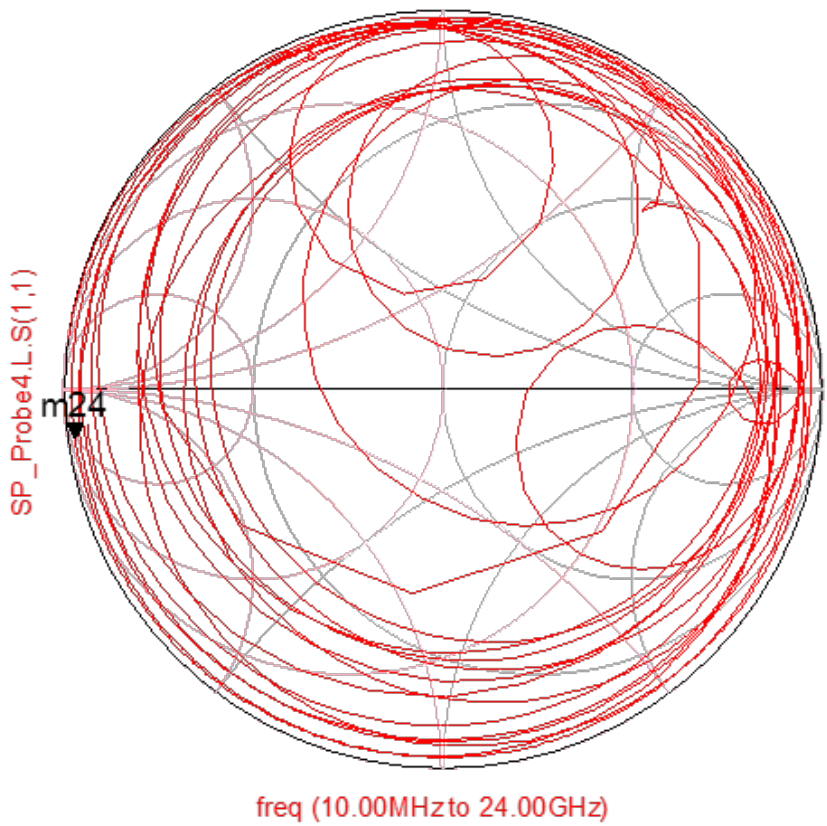



**Figure 58 Second harmonic impedance location when looking from the gate of power-stage transistor into inter-stage.**

The complete final schematic of the designed Class-E 2-Stage PA is shown in Figure 59 and the simulation result is shown in Figure 60. The simulation is performed

under assumption that the microstrip lines are made of perfect conductor and there is no loss tangent. According to Figure 60, PAE of 70% with gain of 22dB is obtained at 37.8dBm output power while the power-stage drain efficiency shows more than 80%.

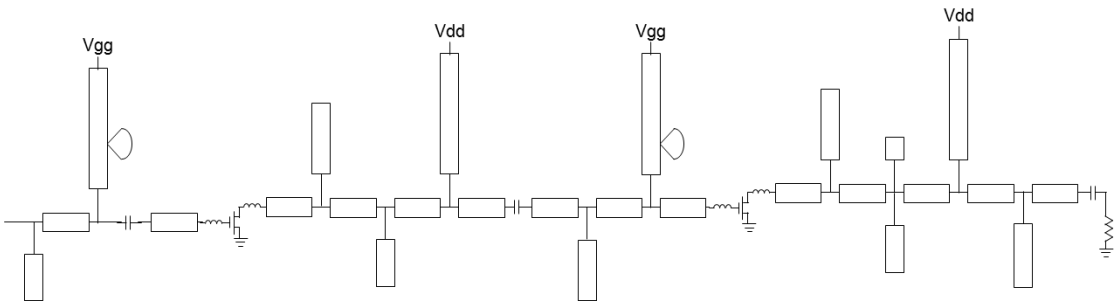



**Figure 59 The final schematic of the designed class E amplifier.**

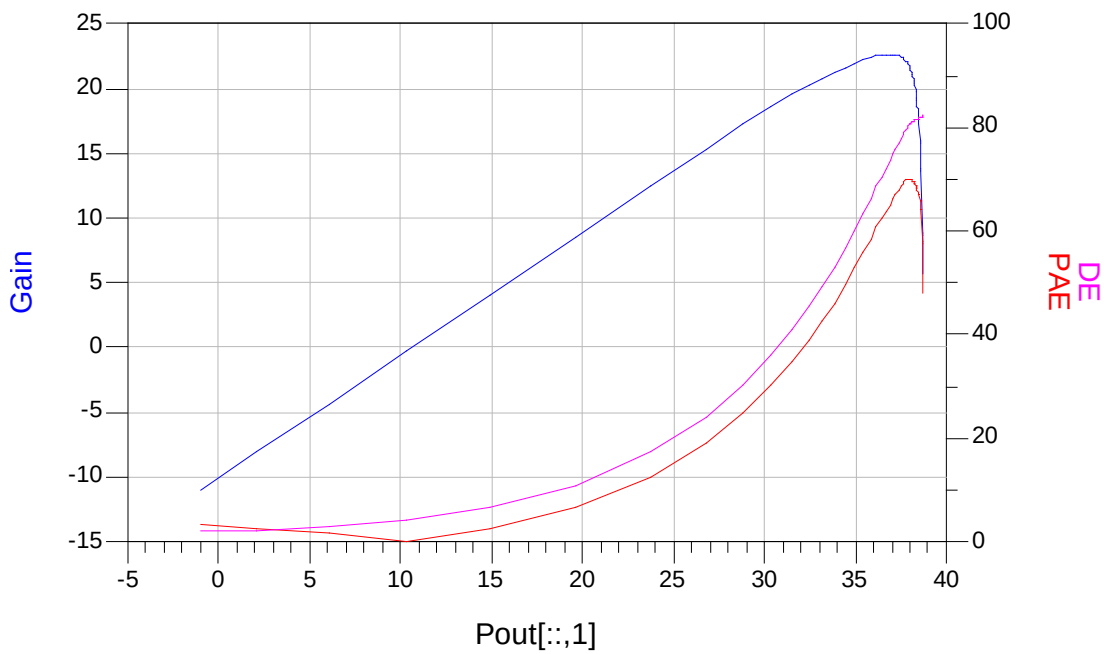



**Figure 60 Simulated performance of the designed class E amplifier.**

Since the Class-E PA is using drain-to-source capacitor as a shunt capacitor, it is unable to check the waveform at the pure transistor level. However, if the drain-to-source capacitor is assumed to be linear, a negative capacitor can be added right next to the drain of transistor then add the positive capacitor with same absolute value again after the current and voltage probe for compensation as shown in Figure 61.

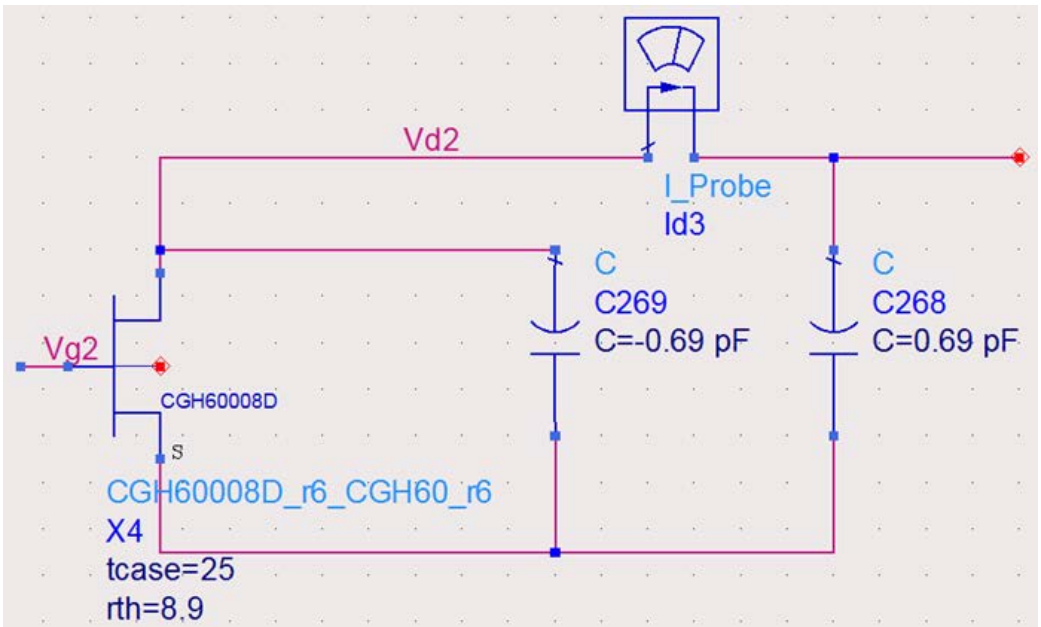



**Figure 61 Schematic of de-embedding linear part of the drain-source capacitance of the transistor.**

The waveform at the drain node after the drain-to-source capacitor is compensated and is shown in Figure 62. Red line indicates the voltage across the transistor while blue line indicates current flow across the transistor. The reason why the current swing goes negative is because the drain-to-source capacitor compensation is not accounted the non-linear capacitance at low drain-to-source voltage. The reason why the voltage does not hit zero is because of knee voltage. From the plot, it is concluded that the current is asymmetric and the overlap between voltage and current is small. Because the falling part of the current wave starts at the

same time the voltage starts rising, with a steep slope, it can be say that the PA designed works in Class-E mode.

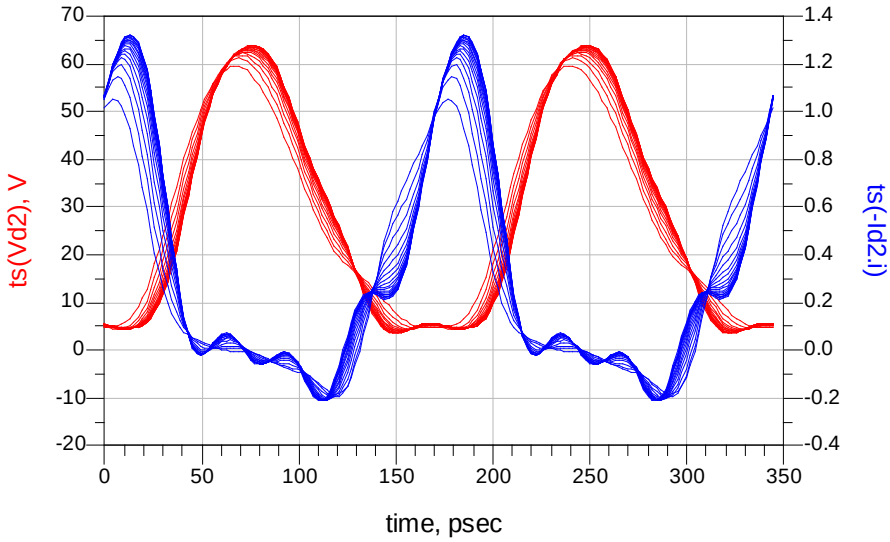



**Figure 62 Simulated drain voltage and current waveform of the class E amplifier.**

When the loss for microstrip lines is added, such as conduction loss and loss tangent, the efficiency falls. The loss information for RT/Duroid 5880 10mil thick substrate is applied; Permittivity is equal to 2.2, Loss Tangent is equal to 0.0004, and conductivity is $5.8 \times 10^7$ Siemens/m for gold cover. The results is shown in Figure 63 as peak PAE of 68.0% with 19.9dB of gain at 37.9dBm of output power. It is noticed that the efficiency and the gain falls by 2% and 2dB, respectively.

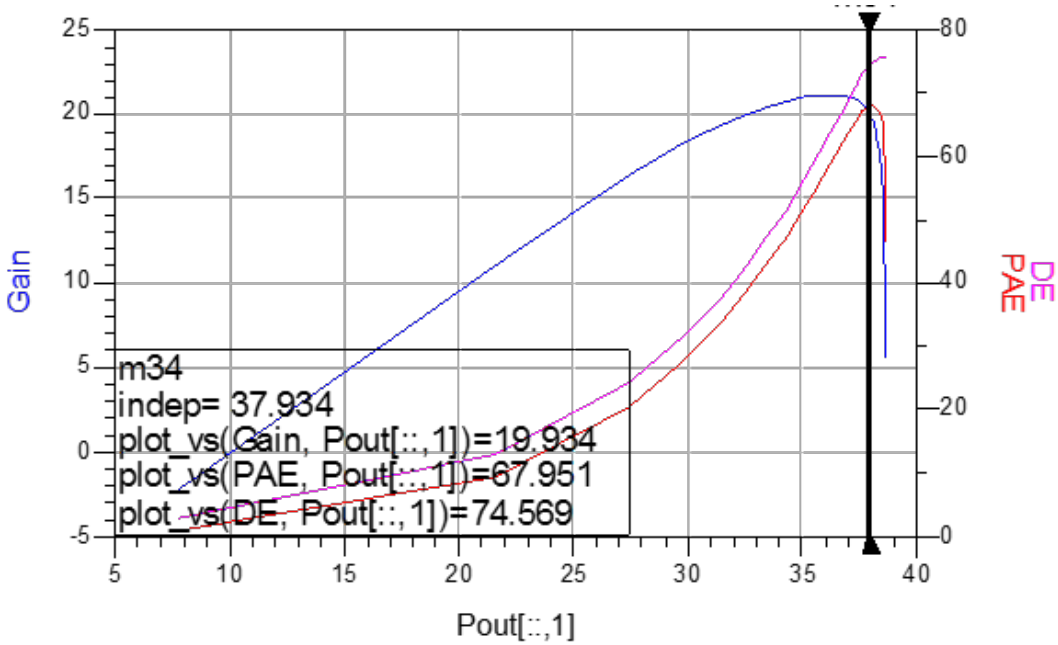



**Figure 63 Simulated performance of the Class-E 2-stage power amplifier. By applying line loss, the efficiency and gain drops 2% and 2dB respectively.**

With designed parameters, EM simulation is performed with ADS2009 Update 1 Momentum. Because the PA operates in high frequency, it is essential to run EM simulation before fabricating Printed Circuit Board (PCB). The same substrate information is used, which is for 10-mil thick RT/Duroid 5880 and the specifications of the following; Permittivity is equal to 2.2, Loss Tangent is equal to 0.0004, and conductivity is $5.8 \times 10^7$ Siemens/m for gold cover. EM simulation is performed from 100MHz to 25GHz with 100MHz sweep. Because the efficiency of PA can be affected by harmonics, up to fourth harmonic should be calculated. Furthermore, dense step is essential, otherwise, the EM simulation gives different results. EM simulated result is shown in Figure 64. According to the Figure 64, the PAE of 67.4% with 18.9dB gain is presented at 37.9dBm of output power. The maximum power stage drain efficiency is 76.2%.

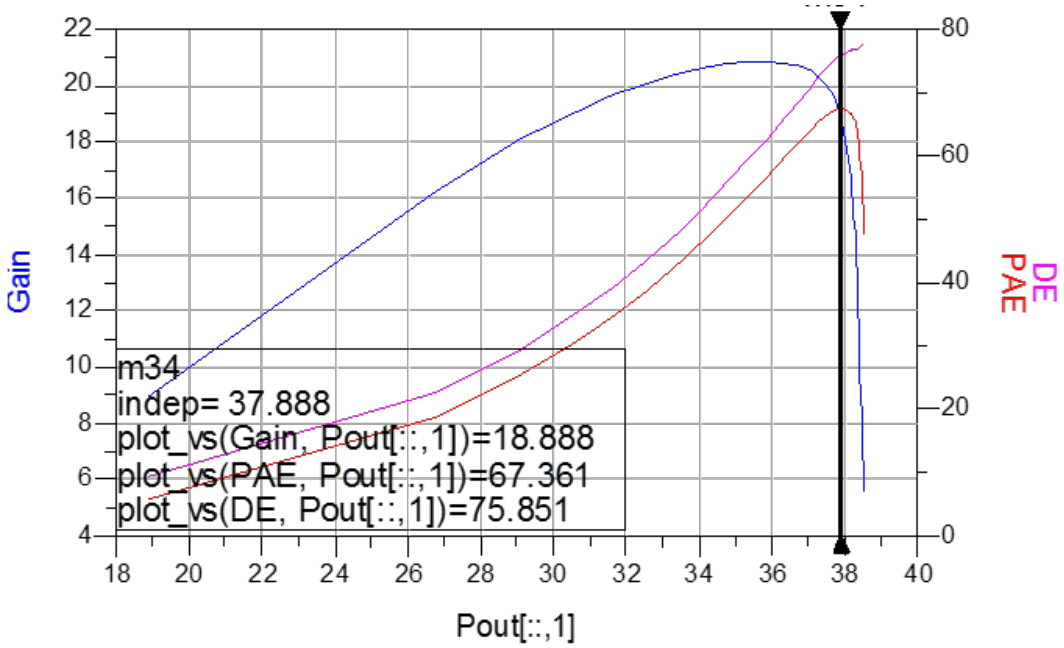



**Figure 64 Simulated performance of the class E 2-stage power amplifier with full-wave simulated line segments.**

## 3.4. Measurement: Class E Two Stage Power Amplifier

The designed 2-Stage Class-E PA from the previous section has been implemented using RT/Duroid 5880 10mil thick substrate. The GaN HEMT used is CGH60008D with gate width of 1.8mm from Cree Inc. The gold plating over the microstrip lines has been done to minimize conductor loss. The substrate information is the following; Permittivity is equal to 2.2, Loss Tangent is equal to 0.0004, and conductivity is $5.8 \times 10^7$ Siemens/m for gold cover. The photograph of the test module is shown in Figure 65. The experimental result of the implemented PA is shown in Figure 66 and Figure 67.

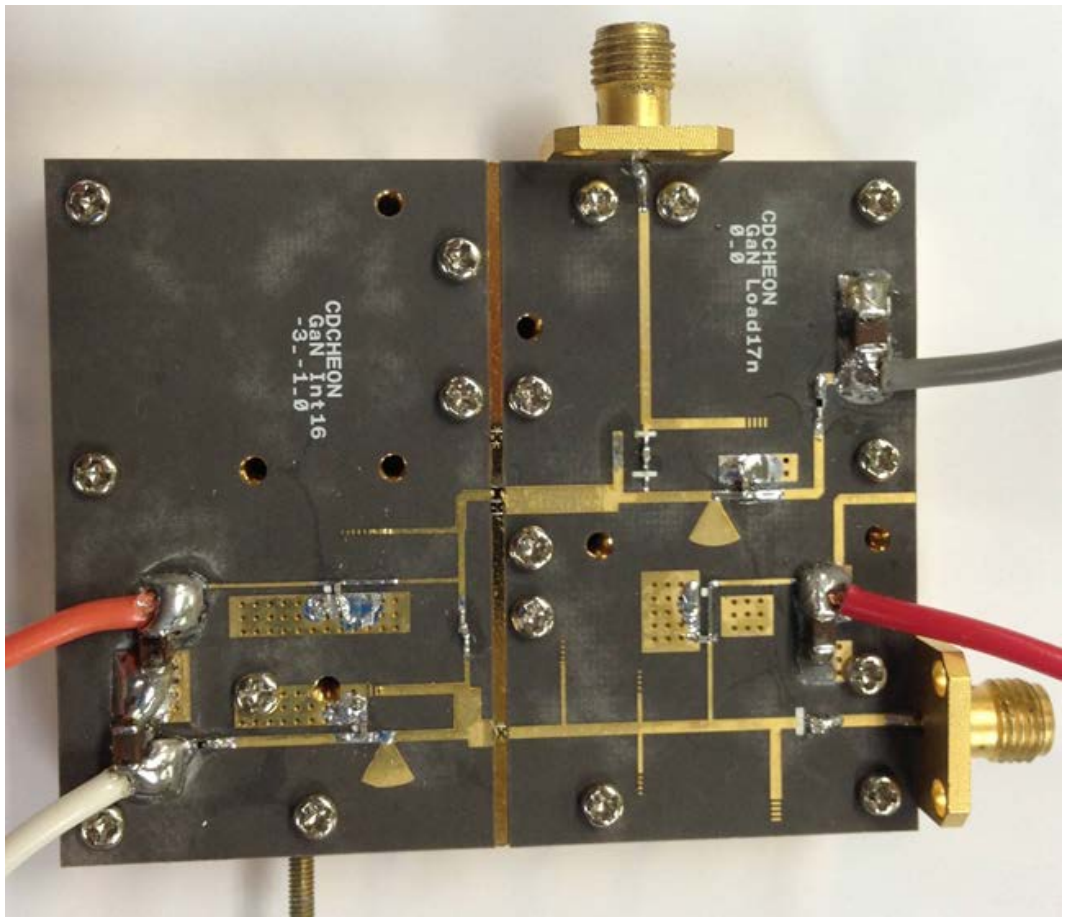



**Figure 65 Photograph of 2-Stage PA.**

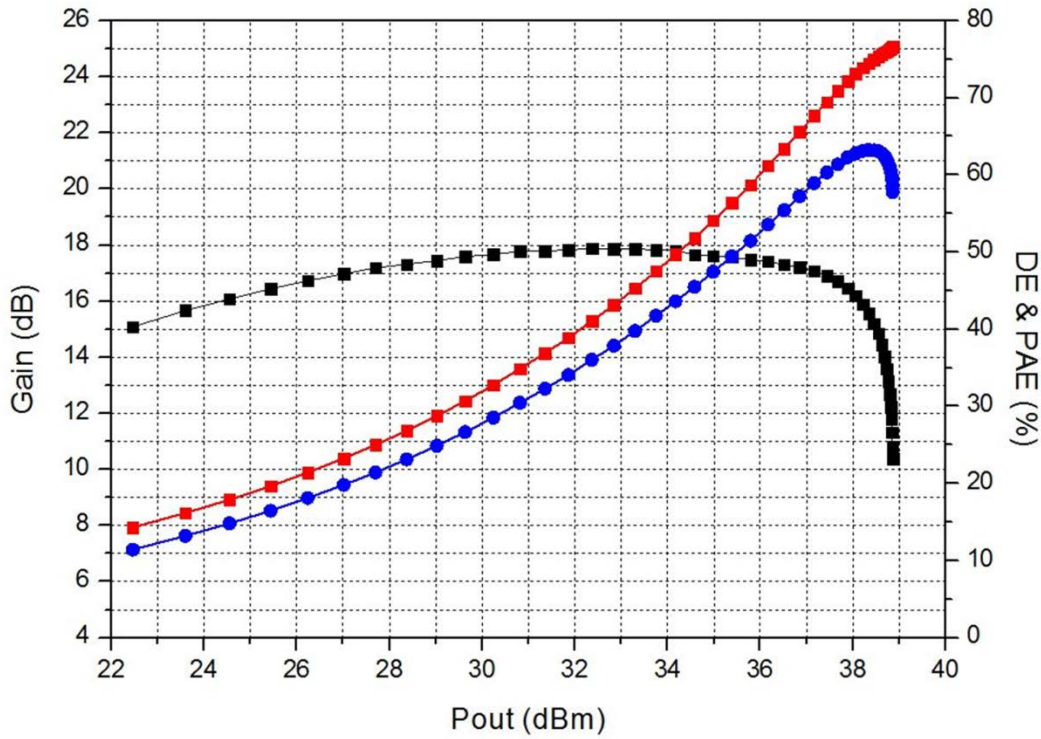



**Figure 66 Implemented 2-stage Class-E Power Amplifier Performance when the drain bias voltage of the power-stage is 28V.**

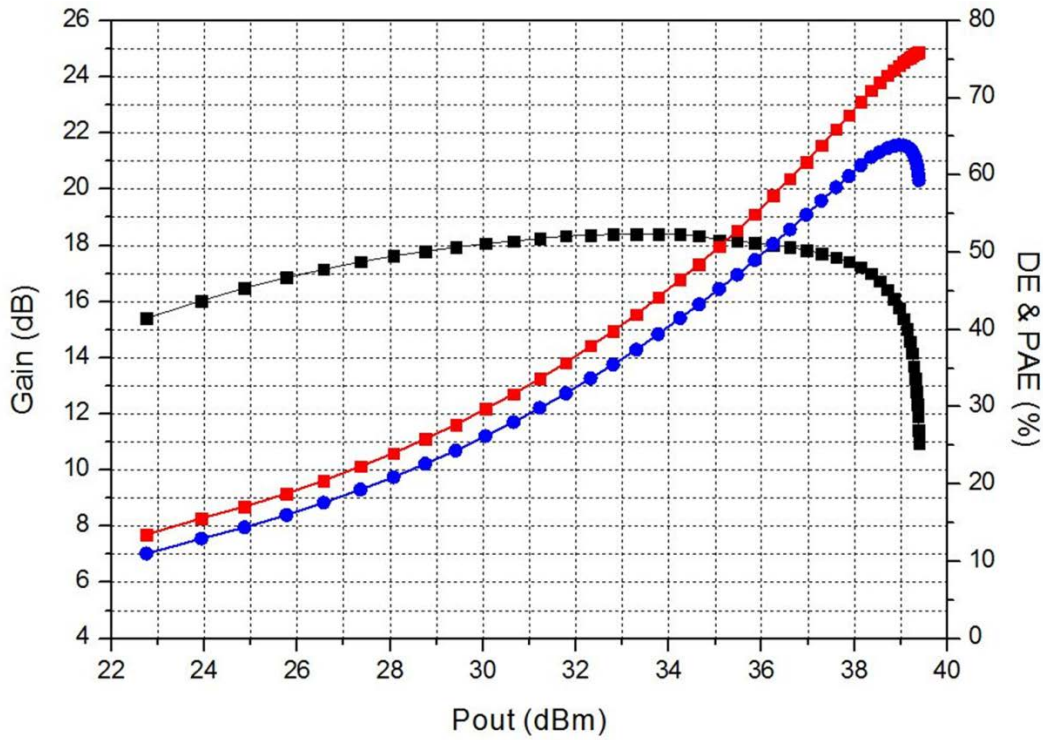



**Figure 67 Implemented 2-stage Class-E Power Amplifier Performance when the drain bias voltage of the power-stage is 30V.**

For Figure 66, the gate bias and the drain bias for the driver-stage are -3.3V and 10V respectively, while the gate bias and the drain bias for the power-stage are -3.8V and 28V respectively. According to the experiment, the maximum PAE of 63.2% is reached at 38.3dBm of output power with gain of 15.6dB. The maximum drain efficiency of the power-stage is higher than 76.6%. When the drain bias of the power-stage is increased to 30, the maximum PAE of 63.9% at 39.0dBm of output power with 15.8dB gain is measured as shown in Figure 67. However, the maximum drain efficiency at the power-stage is little lowered to 76%.

Table 7 shows the comparison chart. Note that all the references are 1-Stage GaN PA while 2-Stage GaN PA is implemented in this thesis. According to the Table 7, this work shows the greater in gain and output powers with higher PAE compare to the others.

**Table 7 Comparison table for power amplifier**

| Ref | Freq. | $P_{out}$ | Gain | $PAE_{peak}$ | Topology | Technology |
|---|---|---|---|---|---|---|
| **2006 [1]** | 5.5 GHz | 35 dBm | 6 dB | 63 % (DE) | $2^{nd}$ harmonic tuned | Hybrid GaN 1-Stage |
| **2007 [2]** | 6.0 GHz | 35 dBm | 6 dB | 45 % | Class E | MMIC GaN 1-Stage |
| **2008 [3]** | 5.6 GHz | 37 dBm | 10 dB | 35 % (DE) | N/A | Hybrid GaN 1-Stage |
| **2009 [4]** | 5.0 GHz | 38 dBm | 7.5 dB | 22 % | N/A | Hybrid GaN 1-Stage |
| **2010 [5]** | 5.7 GHz | 36 dBm | 6 dB | 40 % (DE) | Class AB | Hybrid GaN 1-Stage |
| **2010 [6]** | 5.4 GHz | 36 dBm | 13 dB | 70 % | Class J | Hybrid GaN 1-Stage |
| **This work** | **5.8GHz** | **39 dBm** | **15.8 dB** | **63.9 %** | **Class-E** | **Hybrid GaN 2-Stage** |

## 3.5. Conclusion

The principle of operation for Class-E Power Amplifier is discussed and an important parameter, shunt capacitance next to the drain of transistor is numerically analyzed. Based on the equations derived, basic lumped elements composing Class-E PA are calculated. With the calculated value, simulation is performed with ADS2009 Update 1. After the initial design, the lumped elements are replaced by microstrip lines. Simulation results with loss and without loss are compared. As the last step for simulation, EM simulation has been performed. The final simulation results give PAE of 67.4% with 18.9dB gain at 37.9dBm of output power.

A designed PA is implemented using RT/Duroid 5880 10mil thick substrate with

gold plating and two CGH60008D bare-die GaN HEMTs from Cree Inc. The measurement results show the maximum PAE of 63.2% at 38.3dBm of output power with 15.6dB gain when 28V of supply voltage is applied to the power stage. When 30V is applied to the power-stage of the PA, maximum PAE of 63.9% at 39.0dBm of output power with 15.8dB gain is resulted.

# 4. Average Power Tracking System I

## 4.1. Introduction

The implemented 2-Stage Class-E Power Amplifier (PA) from Chapter 3 is combined with supply modulator realized in Chapter 2. The supply modulator is feeding the power-stage of the PA while the driver-stage runs with constant supply voltage of 10V. Since the PA uses non-linear devices and the supply modulator is an open-loop structure, unpredicted problem may occur. Thus, it is necessary to analyze the PA data in more depth in order to decide at what input power level what input voltage should apply to PWM control circuit in order the supply modulator to supply the desired level of voltage to PA. As the input power level changes the input voltage of PWM control circuit needs to be changed accordingly. In this chapter, expected overall PAE is calculated first to figure out if there is any unpredicted problem. Next, by modulating the supply voltage at the drain of power-stage, increased drain efficiency (DE) for power-stage is obtained.

## 4.2. Expected Overall PAE Calculation

Before combining PA with the supply modulator, expected overall efficiency is calculated in order to decide what supply voltage should be needed for PA in order to produce the best efficiency at certain input power. Using the "Efficiency vs. Output Voltage" data shown in Figure 41, the final efficiency of PA with supply modulator can be predicted. If the efficiency of modulator at a specific output voltage is plotted accordingly to the PA's requiring supply voltage the predicted total efficiency can be graphed as Figure 68. As it is shown in Figure 68, the green line represents efficiency of the supply modulator at the expected output power when 28V is supplied. The red line represents peak Power-Added Efficiency (PAE) when the supply is modulated to

track peak PAE. The blue line represents the overall PAE calculated with PAE of PA and the efficiency of supply modulator.

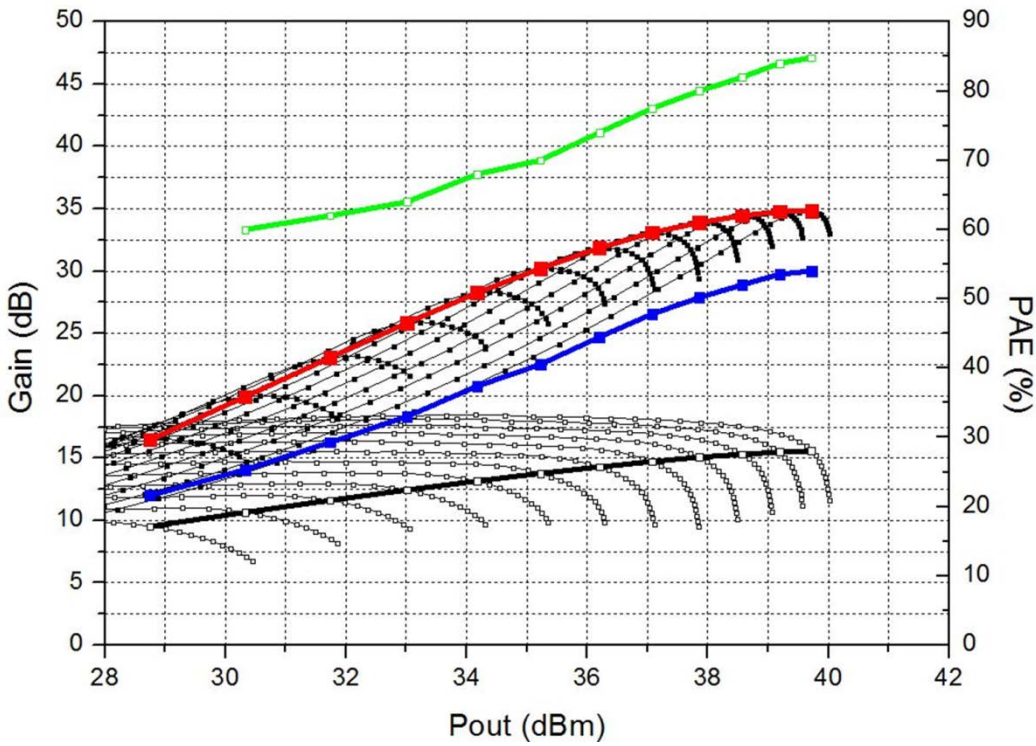



**Figure 68 Expected APT system performance. Each color of line represents Efficiency of supply modulator at expected output power, trajectory of peak PAE of PA for swept supply voltage and the calculated overall PAE from top to bottom.**

From the Figure 68, it is shown that the overall efficiency does not overlap with 28V constant voltage supplied stand-alone power amplifier and thus, the APT system has nothing better than the stand-alone. Although the overall PAE is not improved, the increment in DE at the power-stage level is considered in the next section.

## 4.3. Synchronization of Supply Modulator with Power Amplifier

The power-stage DE of the PA is swept with supply voltage of 10V to 32V by 2V step and plotted as shown in Figure 69. As an initial prediction, when the supply modulator is applied, the efficiency should follow the peak DE if and only if the modulator has 100% of efficiency. Unfortunately, the efficiency of modulator is not perfect. Because the peak efficiency of the supply modulator is 85% according to Chapter 2, the PA with modulator will have maximum efficiency of $85\% \times 75\%$, which is 63.7%. With the same method used in previous section, the "Efficiency vs. Output Voltage" data shown in Figure 41 is brought again to estimate the final power-stage DE of the PA with supply modulator. The predicted total DE can be graphed as blue line in Figure 70.

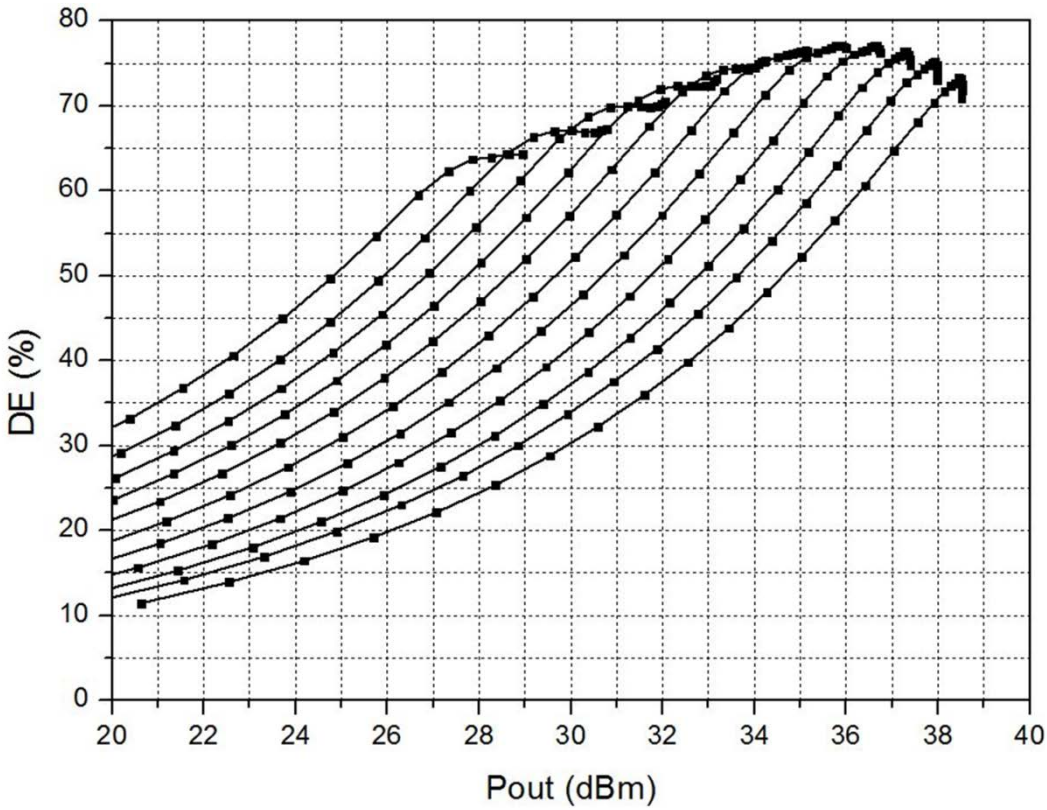



**Figure 69 Measured DE of power-stage of the amplifier.**

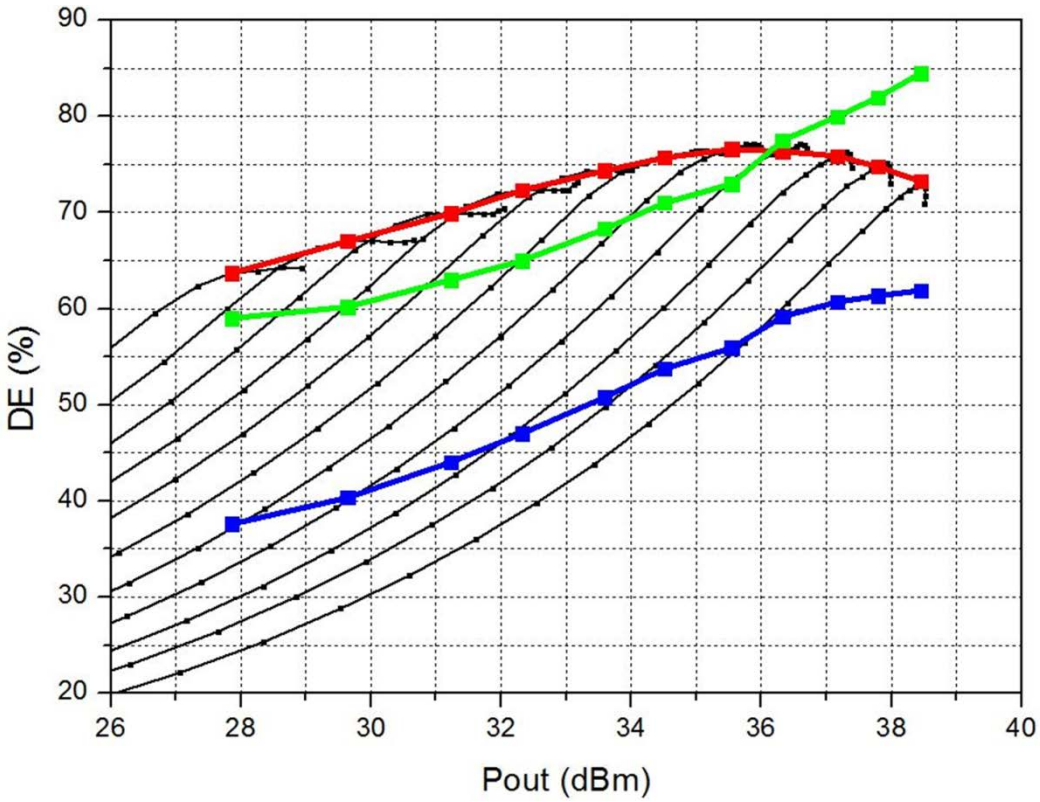



**Figure 70 Predicted power-stage DE when overall system is realized.**

There is an important thing to consider when PA is combined with the supply modulator. When the supply voltage of PA decreases, the load impedance seen from the supply would increases. To help understanding, refer to Figure 71. This is important because the supply modulator is designed with fixed load impedance. When the load impedance of the supply modulator increases the supply modulator produces larger voltage than it is supposed to produce. This will result in no supply modulation to PA even though a smaller power is applied to the PA input. In more details, when small power is applied at gate of PA, small duty cycle will transfer to the supply modulator and the supply modulator would feed small drain voltage to PA. But since the load impedance of modulator is an increase value due to smaller voltage applied, the modulator gives higher voltage again than it is supposed to feed. This will become a loop and eventually, the voltage across the GaN HEMT switchs in

supply modulator exceeds the breakdown. As a result, the drain voltage of PA will not drop nevertheless the input power is decreased.

Such problem arose as a main issue for switching mode supply modulator. This is because the switching mode supply modulator is an open-loop structure, which output is a function of not only the input voltage but the value of load. A typical supply modulator where uses both of a linear stage and a switcher stage does not have such issue since the linear stage produces a feedback and the supply modulator operates as close-loop structure. The output of the close-loop structure is only a function of input voltage and thus, the load of supply modulator does not matter. However it is described in Chapter 1, by having a linear stage the total efficiency of the supply modulator decreases. Therefore there is trade-off.

To solve this problem, the supply modulator should follow the point where the gain is about 60% compressed from its peak. Referring to Figure 72(b), when the supply modulator follows the constant gain at high output power (blue line,) the supply modulator is following the black line in gain graph. The black line graph in Figure 64(a) shows how the load impedance of PA looking down from the supply modulator changes according to its voltage. Meanwhile, if the supply modulator follows the compressed gain line, as shown as red line in Figure 64(b), the load resistance changes a lot less according to Figure 64(a), the red line.

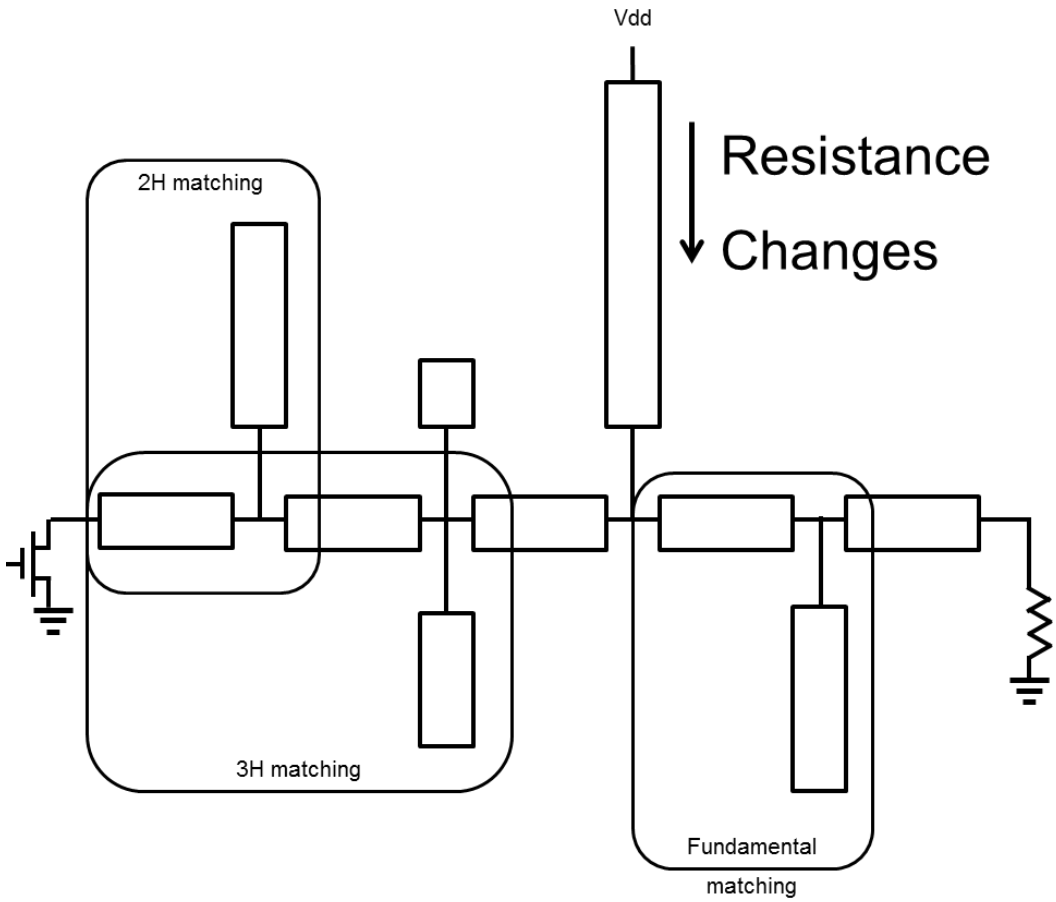
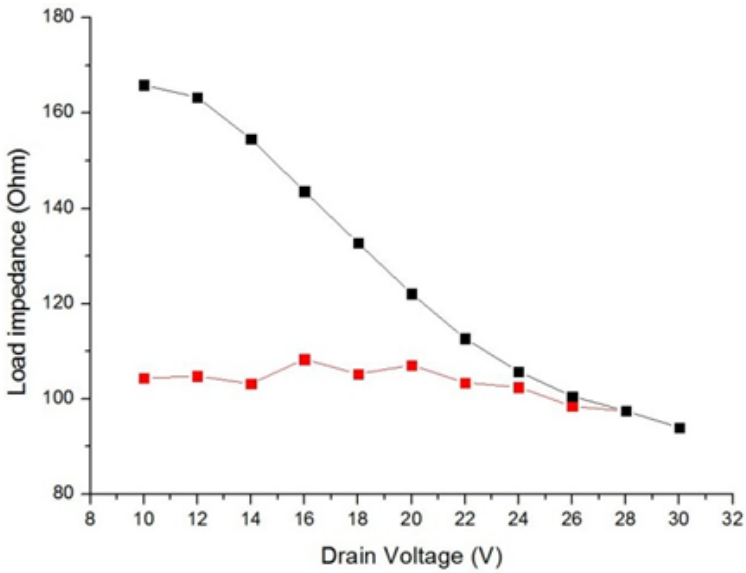
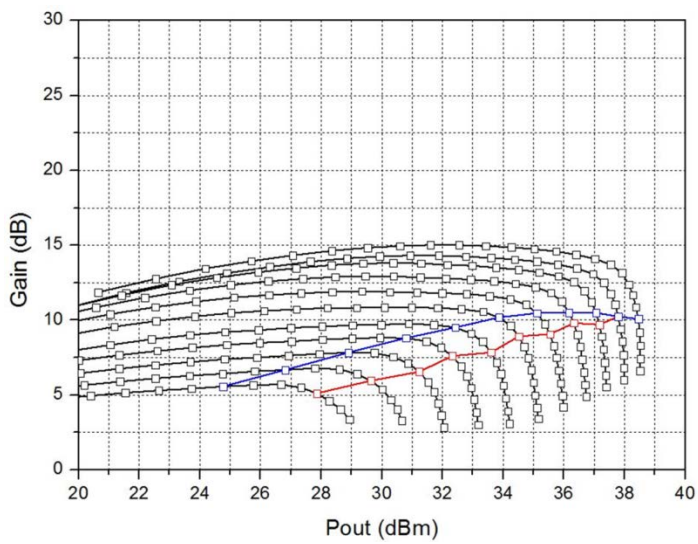



**Figure 71 Concept of the impedance seen at the supply modulator.**




(a)




(b)

**Figure 72 Load impedance modulation effect. (a) Load impedance seen at the supply modulator. The black curve is the case for tracking optimum power-stage DE while the red is compensated curve for maintaining same impedance and (b) corresponding gain curve, blue curve for tracking optimum power-stage DE while red curve for maintaining same impedance.**

Since the supply modulator is designed with 102.5 ohm, variation of load resistance from 95 ohm to 110 ohm does not affect critically. Therefore in this work, supply modulator is synchronized with PA to follow 60% compressed gain line in order to minimize the variation of load impedance.

## 4.3. Measurement: Average Power Tracking Power Amplifier I

The power detector synchronizes the input power of PA with the PWM control circuit in supply modulator. A measurement is performed with Agilent VEE program. When input power is applied, a power sensor reads the real power input to the 2-Stage Class-E PA. (Because GaN PA drives high power, its input power should be large as well. Therefore it is inevitable to use two Driver PAs after the signal generator.) At the same time, the input power through a 20dB coupler is read by a detector. This detector will compute the RMS value of the input power and send appropriate DC voltage to PWM control circuit input. Then, the PWM control circuit decides the duty cycle and the supply modulator decides its output voltage. When this output voltage is applied to the drain of PA, a highly efficient output power is resulted. This output power will be detected by another power sensor and plotted on the Agilent VEE program. As shown in Figure 73, the experimental result follows the estimated power-stage DE line.

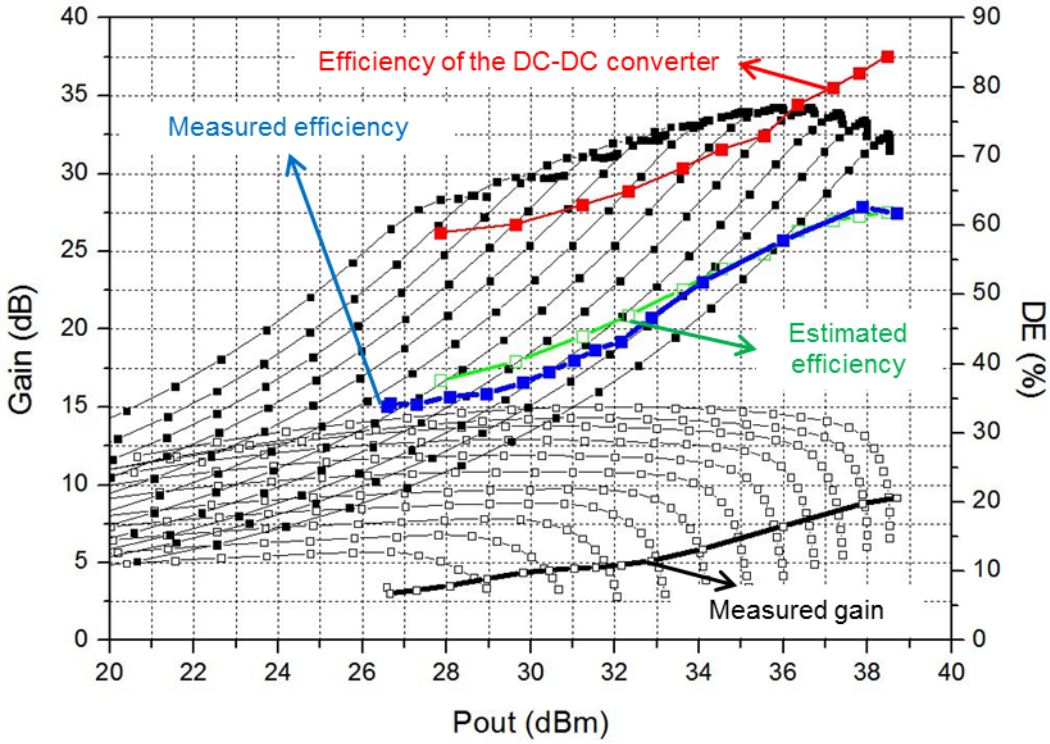



**Figure 73 Measured overall system efficiency of the APT PA.**

Figure 74 shows the magnified version of Figure 73. In Figure 74, the red line is power-stage DE of a stand-alone PA with 28V of supply voltage while the black line is of a stand-alone PA with 30V of supply voltage. Blue line in Figure 74 shows the power-stage DE of the average power tracking (APT) system. The supply modulator used here can boost up to 31V and buck down to 10V with 28V of supply voltage. Although it is typical to compare with stand-alone PA with 28V of supply voltage, 30V supplied stand-alone PA is also compared.

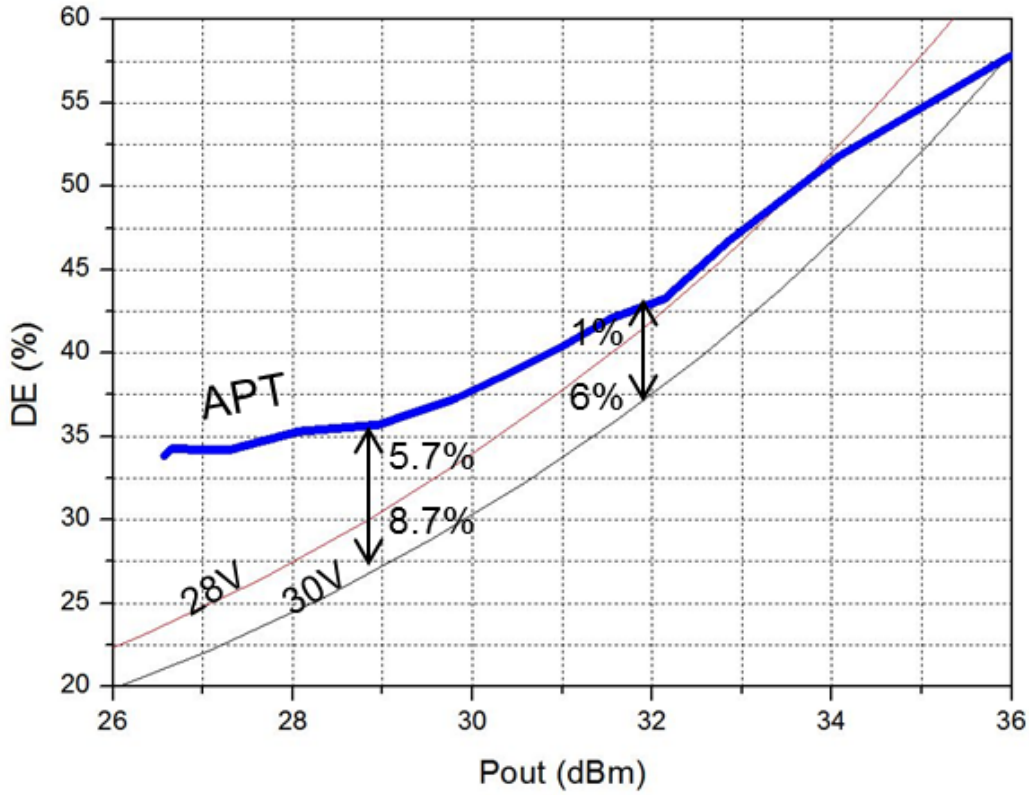



**Figure 74 Magnified version of overall system efficiency of the APT PA.**

As a result, the power-stage peak DE of the APT system combination of the PA and the supply modulator shows 62.6% at 37.9dB output power. At 6dB back-off power, the efficiency increases from 41% by 1% when compared to 28V supplied stand-alone PA. At 9dB Back-off power, its efficiency increases from 30% to 35.7%. Since the supply modulator boosts up to 32-V, the maximum output power is increased to 38.7dBm from 37.9dBm according to Figure 73. Back to Figure 74, increase in efficiency of 6% can be found at 6dB back-off power when the APT system is compared to 30V supplied PA. At 9dB back-off power, total of 8.7% efficiency is increased. The Final data is organized in Table 8.

**Table 8 Overall system efficiency of the APT PA**

| | | Stand-alone PA efficiency (%) | With modulator (%) | Efficiency increased (%) |
|---|---|---|---|---|
| **Compare to 28V** | Peak Efficiency | 75.2 | 62.6 | -12.6 |
| | 6dB Back-off | 41 | 42 | 1 |
| | 9dB Back-off | 30 | 35.7 | 5.7 |
| **Compare to 30V** | Peak Efficiency | 73.3 | 62.6 | -10.7 |
| | 6dB Back-off | 36 | 42 | 6 |
| | 9dB Back-off | 27 | 35.7 | 8.7 |

## 4.4. Conclusion

The PA module implemented in Chapter 3 is combined with the supply modulator implemented in Chapter 2 to realize Average Power Tracking system. Variation in load impedance looking from the supply to the drain of PA is taken into account and the solution is proposed. As a result, power-stage peak DE shows 62.2% at 27.8dBm. At 6dB and 9dB back-off, 1% and 6% of power-stage DE is improved, respectively. The output power is also increased from 37.9dBm to 38.7dBm due to boost characteristic at high duty cycle of the supply modulator. Comparing to a 30V supplied stand-alone PA, 5.7% and 8.7% of power-stage DE is improved for 6dB and 9dB back-off, respectively.

# 5. Average Power Tracking System II

## 5.1. Introduction

As it is stated in Chapter 2, the major problem lies on the Class-$E^2$ DC-DC Converter is the low efficiency at low output voltage. As the duty cycle of the PWM reduces, the conduction angle for the inverter switch becomes smaller than the optimum angle. This causes the switch to be on before the shunt capacitor is fully discharged. The energy stored in the shunt capacitor is then get wasted more and more as the duty cycle of PWM decreases. In this chapter, a new method to control the inverter switch is proposed. Instead of PWM control, Pulse Width and Frequency Modulation (PWFM) is adopted in order to avoid the waste of energy stored in capacitor. The PFWM control for Class-$E^2$ DC-DC Converter has never been introduced. In the next section, the concept of PWFM control will be discussed followed by realization of Average Power Tracking (APT) system using the most efficient PA designed in this thesis.

## 5.2. Concept of PWFM

As it is noticed in Figure 7(b), when the conduction angle is decreased, the voltage charged in the shunt capacitor drops at once before it gets fully discharged. This is because the time of the inverter switch in off-state becomes long as the duty cycle of PWM decreases and the capacitor is in charged state after one-cycle of fully charged and fully discharged. The shunt capacitor in the Class-E inverter is a fixed value. Although the amount of current flowing into the capacitor and out of the capacitor could not be tuned to be exactly the same during the time interval of off-state of the inverter switch, the time required for the capacitor to charge up and discharge fully should be a certain value. Without a modification to the Class-$E^2$ DC-

DC Converter realized in Chapter 2, it can be thought as about 0.5 of duty cycle of 1MHz PWM shows the best time interval for the capacitor value used in this thesis due to its highest efficiency shown in Figure 42. Considering the switching frequency of 1MHz, the best time interval for the shunt capacitor being on-state is 500ns.

In this newly introduced control method, the time for the inverter switch in off-state will be fixed to 500ns no matter what. If the PWM control used in chapter 2 is illustrated as in Figure 75(a), the PWFM control that is going to be used in this chapter will be as illustrated in Figure 75(b). In Figure 75(a), the period is kept the same while the on-state of the switch is changing as it gets below, lowering the duty cycle. In Figure 75(b), the time interval for the off-state of the switch is kept constant while the on-state of the switch is modulated as it gets below. In terms of period, Figure 75(b) is changing its frequency; and of course, duty cycle. Thus, with the constant time interval for the inverter switch to be in off-state, frequency is modulated. This is the PWFM that is introducing here as a proposed method to control Class-$E^2$ DC-DC Converter.

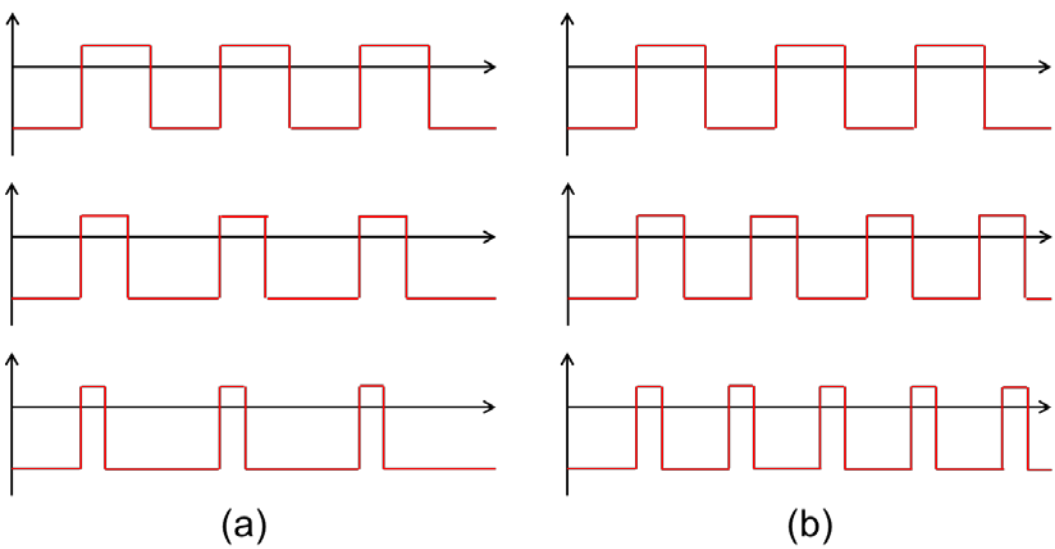



**Figure 75 (a) PWM signal as its duty cycle decreases in downwards and (b) PWFM as it gets higher frequency in downwards.**

## 5.3. Measurement: PWFM Controlled Supply Modulator

The final target of this thesis is to produce the best performance in Power Added Efficiency (PAE). As it will be discussed in the following section, the load impedance seen at the power-stage supply of the 2-stage Class-E PA is about 85ohm. This is different from the previous work, where 102.5ohm is used in Chapter 2 and thus, little modification in values of lumped elements for the Class-$E^2$ DC-DC Converter is made as shown in Table 9. For the variable name, refer to Figure 76.

**Table 9 Parameters for the new Class-$E^2$ DC-DC Converter**

| Ls | Cpi | Lr | Cr | Cpr | Llpf | Clpf | RL |
|---|---|---|---|---|---|---|---|
| 220uH | 0.86nF | 18.2uH | 37.7nF | 0.86nF | 220uH | 2.2uF | 85 Ω |

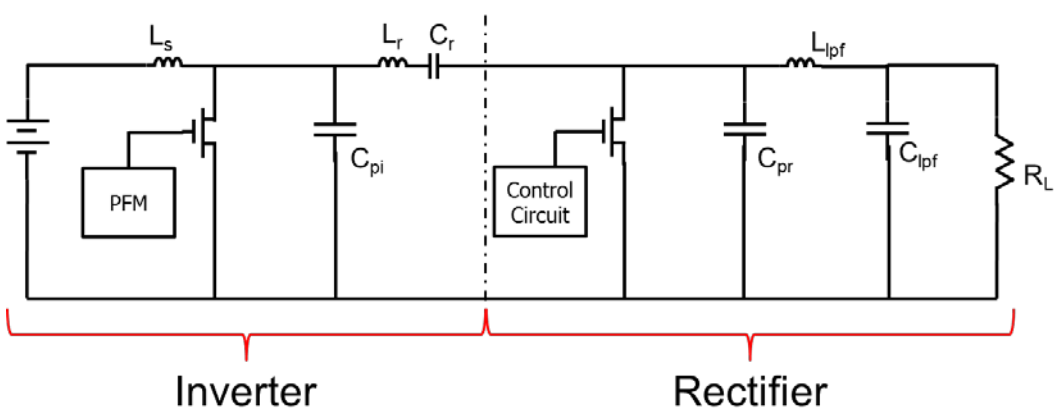



**Figure 76 The schematic for class E2 DC-DC converter with variable name.**

The measurement data of the stand-alone supply modulator is tabled in Table 10. As the frequency increases, the efficiency still tends to decrease, but at 12V of output voltage only about 10% of efficiency decreased from the peak. Figure 77 shows the graphical representation of efficiency depending on output voltage. The red line indicates PWFM controlled supply modulator performance while the black line shows the previously built PWM controlled supply modulator performance. From the graphical analysis, it is noticeable that at 12V of output voltage, about 11% of efficiency increased.

If the variables in Table 9 are tuned, up to 90% of efficiency could be obtained by measurement. However, the peak efficiency is traded-off with the efficiency at low output voltage. As a supply modulator, the flat efficiency over the wide range of output voltage is essential. Therefore in this thesis, peak efficiency of 83% of PWFM controlled supply modulator is used. Figure 78 shows the linear response of the output voltage according to frequency of PWFM input. It shows that by changing the frequency linearly, the output voltage can be changed in linear.

**Table 10 Experiement results for PWFM controlled modulator**

| Period (ns) | Pulse Width (ns) | Freq (MHz) | Vdd (V) | Idd (mA) | Vout (V) | RL (ohm) | Eff (%) |
|---|---|---|---|---|---|---|---|
| **1000** | 500 | 1.00 | 32 | 480 | 32.93 | 85 | 83.06 |
| **950** | 450 | 1.05 | 32 | 432 | 30.95 | 85 | 81.52 |
| **900** | 400 | 1.11 | 32 | 375 | 28.62 | 85 | 80.30 |
| **850** | 350 | 1.18 | 32 | 312 | 25.90 | 85 | 79.05 |
| **800** | 300 | 1.25 | 32 | 244 | 22.75 | 85 | 77.98 |
| **750** | 250 | 1.33 | 32 | 177 | 19.22 | 85 | 76.73 |
| **700** | 200 | 1.43 | 32 | 117 | 15.40 | 85 | 74.52 |
| **650** | 150 | 1.54 | 32 | 69 | 11.49 | 85 | 70.34 |
| **600** | 100 | 1.67 | 32 | 38 | 7.86 | 85 | 59.77 |

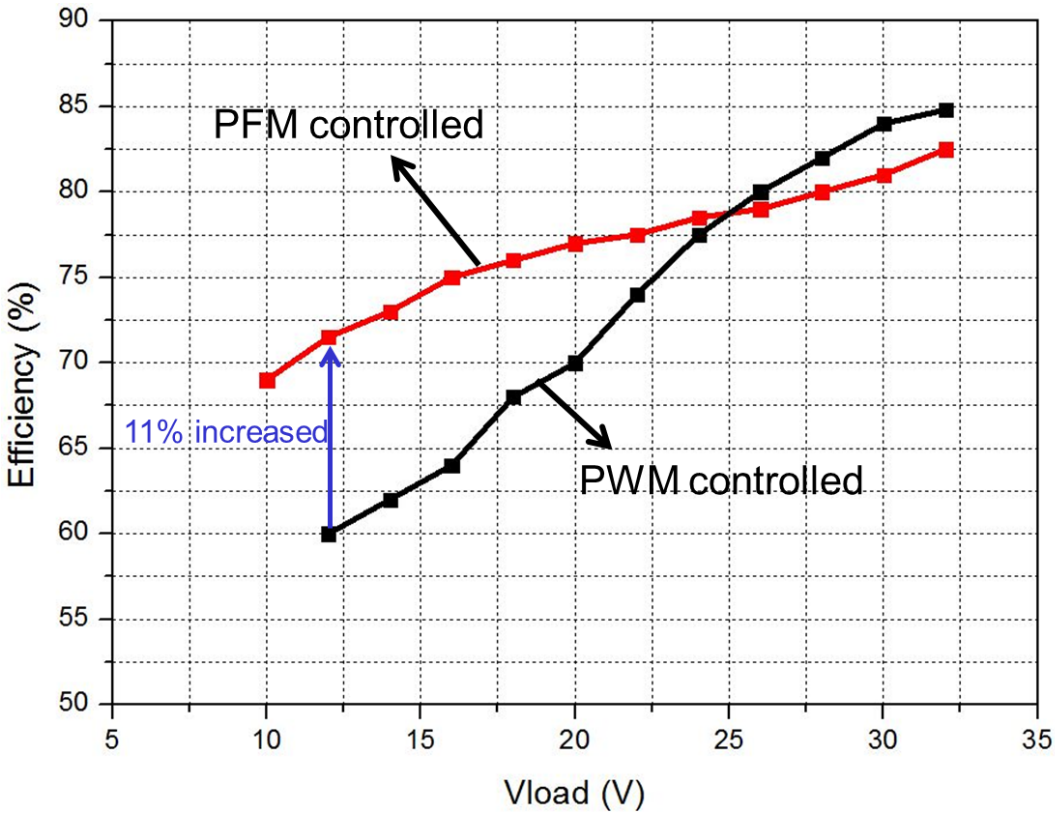



**Figure 77 Efficiency vs. Output Voltage, Red: PWFM controlled and Black: PWM controlled**

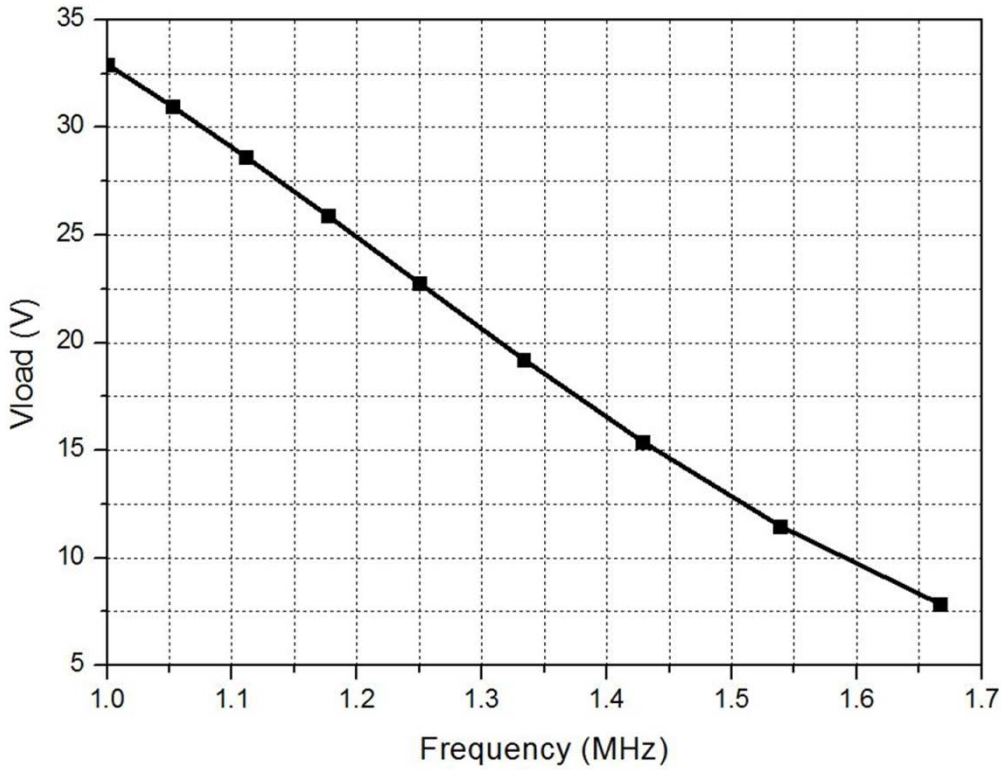



**Figure 78 Linear response of output Voltage vs. Frequency**

## 5.4. Highly Efficient 5.8GHz Power Amplifier

In this section, the 2-Stage Class-E PA designed in Chapter 3 is used without a modification. The supply voltage sweep result of the PA and the load impedance seen from the supply will be discussed again.

The power amplifier implemented in this thesis shows the maximum PAE of 63.9% according to Figure 67. However in this chapter, such high PAE result is difficult to obtain since the result is obtained in condition of very low temperature, just before dewdrops be formed on microstrip lines. If the power amplifier is on for more than a few seconds, the heat from the transistor is inevitable and thus resulting in degradation of performance. Because the temperature of the transistor cannot be kept

constant, from now on, the cooling system of the power amplifier is removed and the measurement will be performed in room temperature of hot summer in Korea.

Supply voltage swept Power-Added Efficiency (PAE) of the PA is plotted in Figure 79. It is swept from 10V to 32V with 2V steps. As it is shown, the PAE decreases rapidly as the output power decreases. This is inevitable since change in supply voltage is applied only to the power-stage of the 2-stage PA. By lowering the supply voltage, the power-stage produces less gain while the driver-stage, which having constant supply voltage of 10V, keeps producing high gain. Then the power consumption in the driver-stage eventually becomes larger relative to the power consumption in the power-stage. This will reduce the overall PAE. This becomes the main issue of the 2-stage power amplifier when average power tracking is applied. In order to make the PAE decrease less, one-stage power amplifier is desired. However, the gain of one-stage power amplifier using the same GaN HEMT model is low; less than 10dB, therefore 2-Stage PA is persisted. Additionally, if the GaN HEMT model is changed to a high-gain transistor, this problem may be solved.

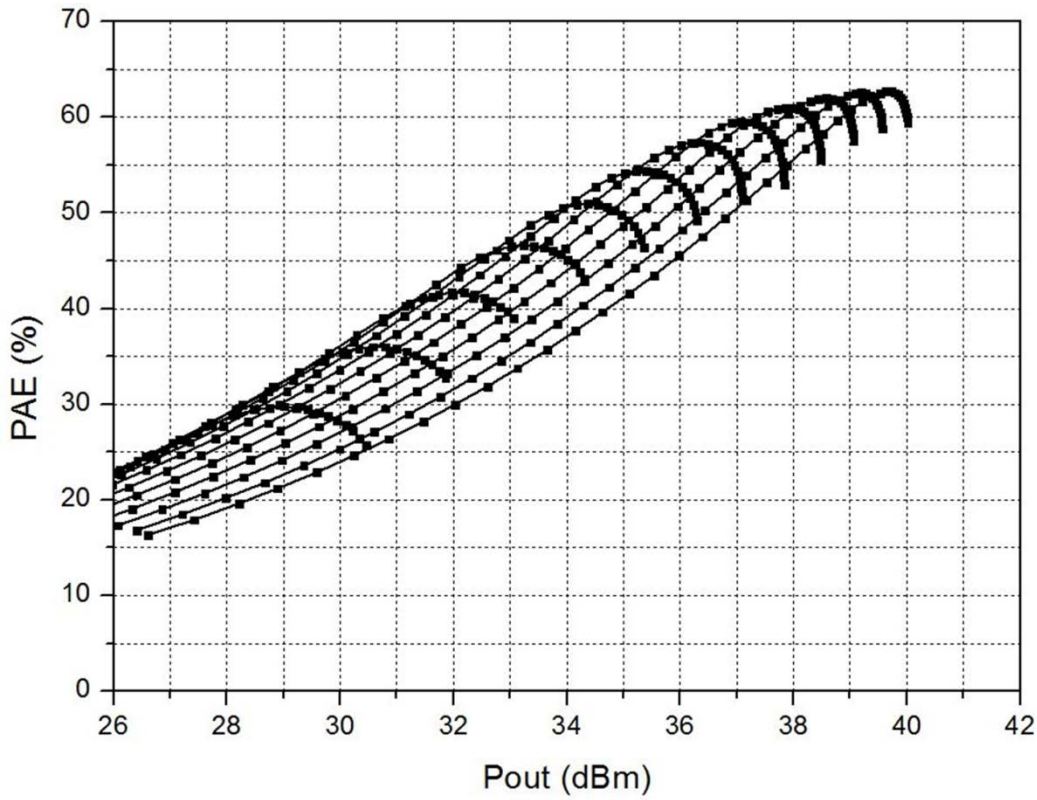



**Figure 79 Measured PAE of the PA.**

The load impedance seen from the supply is illustrated in Figure 80. The concept of load impedance talking in here has been described in previous chapter. According to the Figure 80, the load impedance does not change a lot and thus, the average of impedances at different supply voltage, 85ohm, is assumed as the fixed load impedance. Instead of large variation of load impedance, the reason for small variation of load is because the gain curve is not at constant. It will be found in Figure 85 that the gain curve is not constant. Although, the supply modulator modified in the previous section is appropriate with the load impedance of 85ohm.

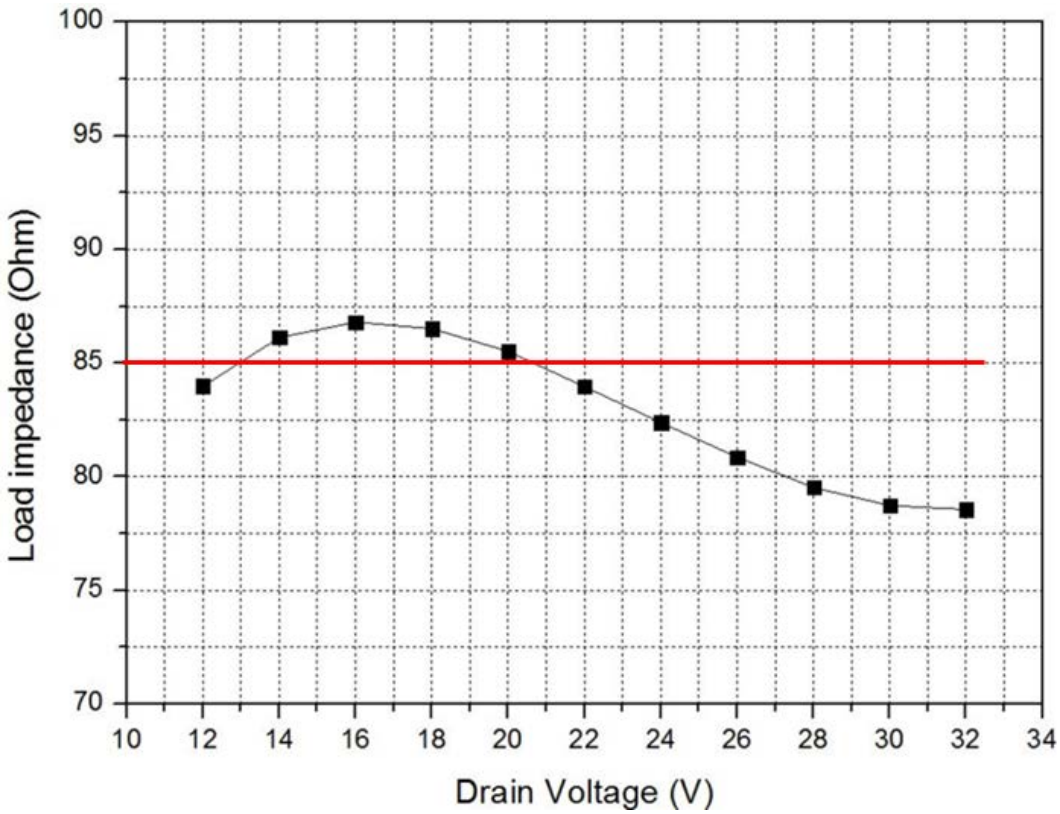



**Figure 80 Load impedance modulation depending on supply voltage of power-stage of the PA.**

Same procedure as described in Chapter 4, the overall PAE of the APT system is calculated. With the supply modulator efficiency and its output voltage data, the expected supply modulator efficiency at output power of the PA is estimated. This result can be found in green line in Figure 81. The peak PAE of the PA is connected and is represented as red line in Figure 81. The product of these two curves, the efficiency curve for the supply modulator and the PA is plotted in blue representing estimated overall PAE of the APT system.

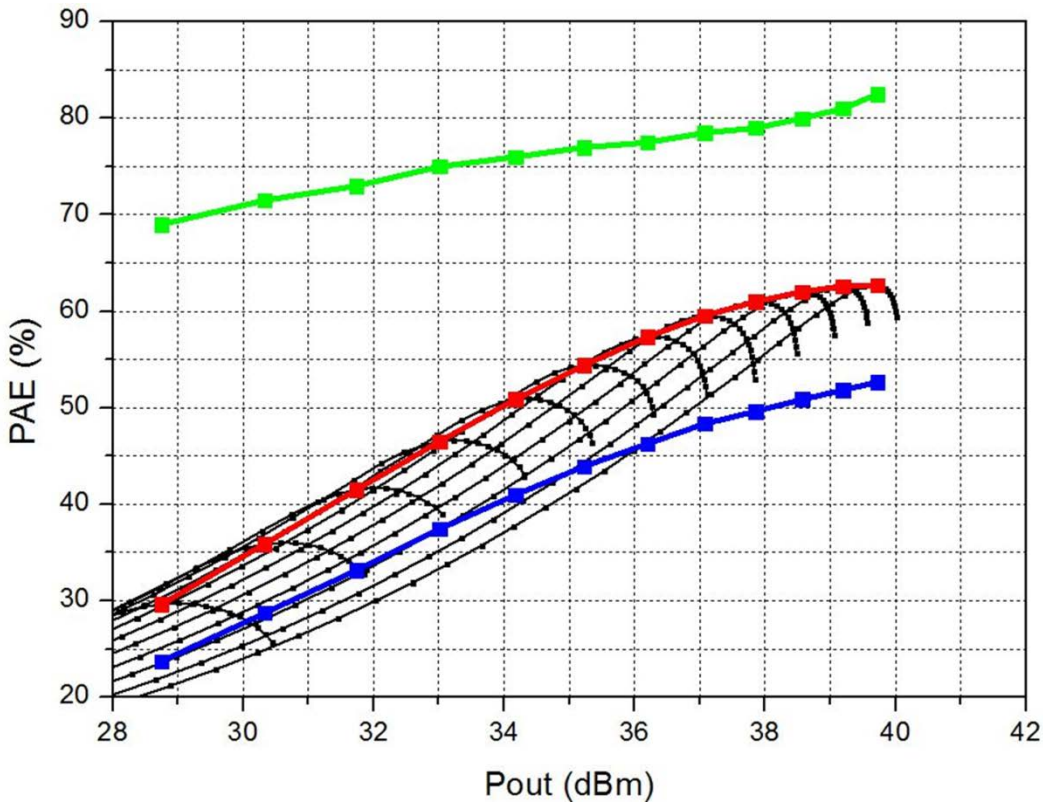



**Figure 81 Expected performance of APT system. Green: expected efficiency of supply modulator, Red: expected PAE of the PA, Blue: the product of the supply modulator efficiency and the PA PAE.**

Instead of PAE, if power-stage DE is plotted, the result becomes as shown in Figure 82. The green curve represents the efficiency of supply modulator while the red curve shows the connection of rational values of power-stage DE at different supply voltage. The blue line shows the calculated power-stage DE when APT system is realized. Note that the blue line here is not a product of two curves. DC supply power for the power-stage is computed first with the output power of the PA, efficiency of supply modulator and DE of the stand-alone PA. Then the new power-stage DE of the APT system is computed.

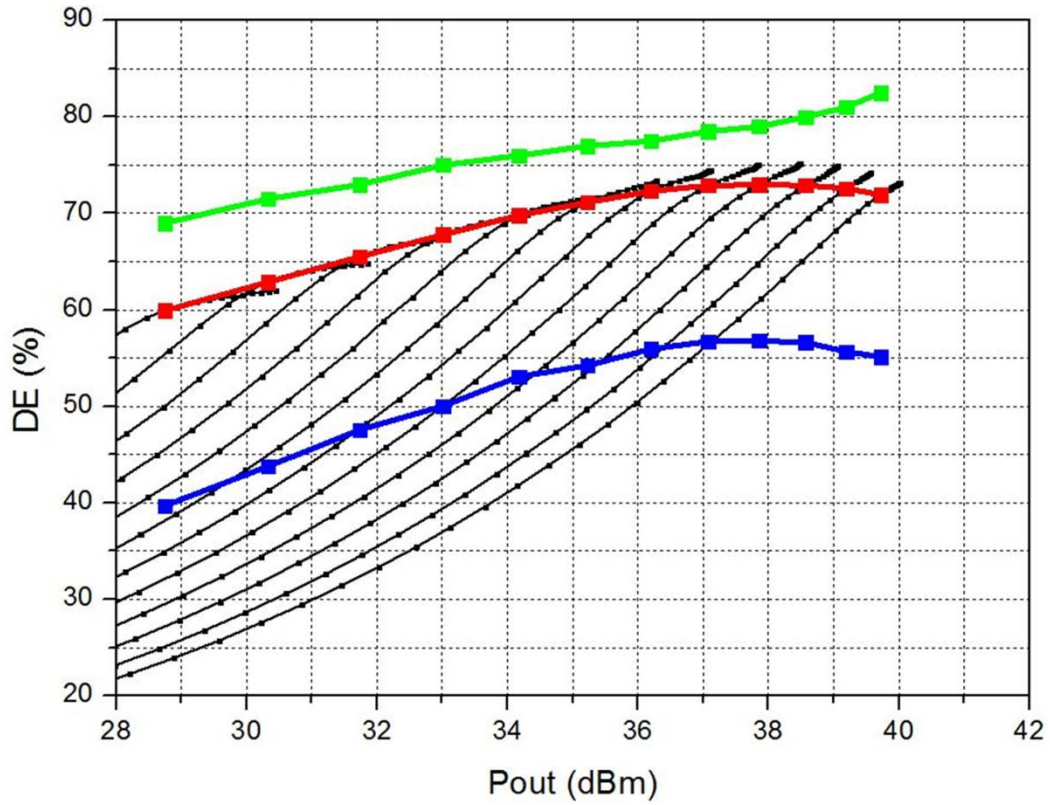



**Figure 82 Expected performance of APT system. Green: expected efficiency of supply modulator, Red: expected DE of the PA, Blue: the calculated power-stage DE when APT system is realized.**

## 5.5. Measurement: Average Power Tracking Power Amplifier II

The whole system of APT system is realized. The gate bias and drain bias for driver-stage of the PA are -3.3V and 10V, respectively and the gate bias for the power-stage is set to -3.8V. In order to prevent exceed amount of current flowing through the inverter switch in supply modulator; the supply voltage of supply modulator should be turned on at the last, even later than the input power applied to the PA.

This is because the load impedance seen at the drain bias of power-stage is changing as a function of input power of the PA. Different from 28V of supply voltage in Chapter 4 measurement, supply voltage of 32V is used in here for the supply modulator, and the GaN HEMT switch in inverter is fed by -4V to 1V swing PWFM signal from the function generator. This is because since the peak PAE curve in Figure 79 tends to drop rapidly as the output power decreases. In order to extend the curve beyond the presented output power, the supply voltage is increased. In the later section, the average power tracking system realized here is compared to the stand-alone power amplifier having 32V of supply voltage.

The result of the average power tracking system experiment is shown in Figure 83 and the magnified version of the PAE increment is shown in Figure 84. The blue line in Figure 83 represents the calculated expected overall PAE while the gold line represents the measured overall PAE. The measured PAE shows good agreement with the calculated curve.

The peak overall PAE is 49.5% at 39.6dBm of output power with gain of 15.6dB. At 6 dB back-off power, 4% of PAE is increased from the stand-alone 32V supplied PA resulting in 39% of PAE. At 9 dB back-off power, 3.5% of PAE is increased resulting in 29%. The finalized result is written in Table 11.

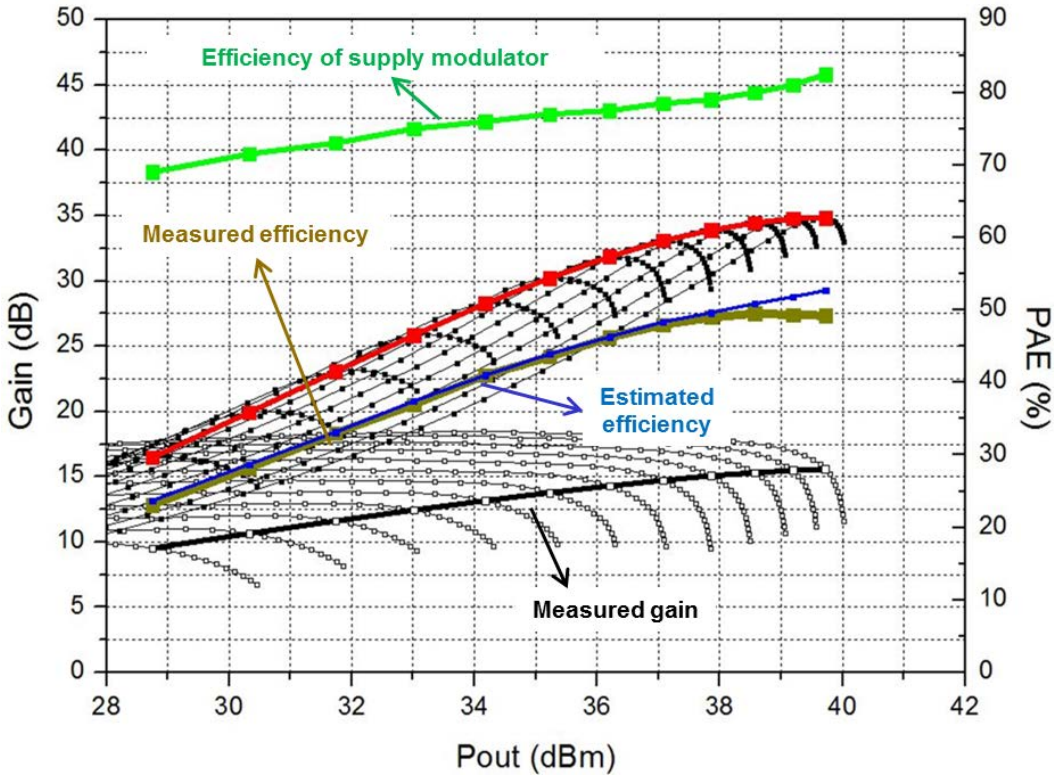



**Figure 83 Measured overall system efficiency of the APT PA.**

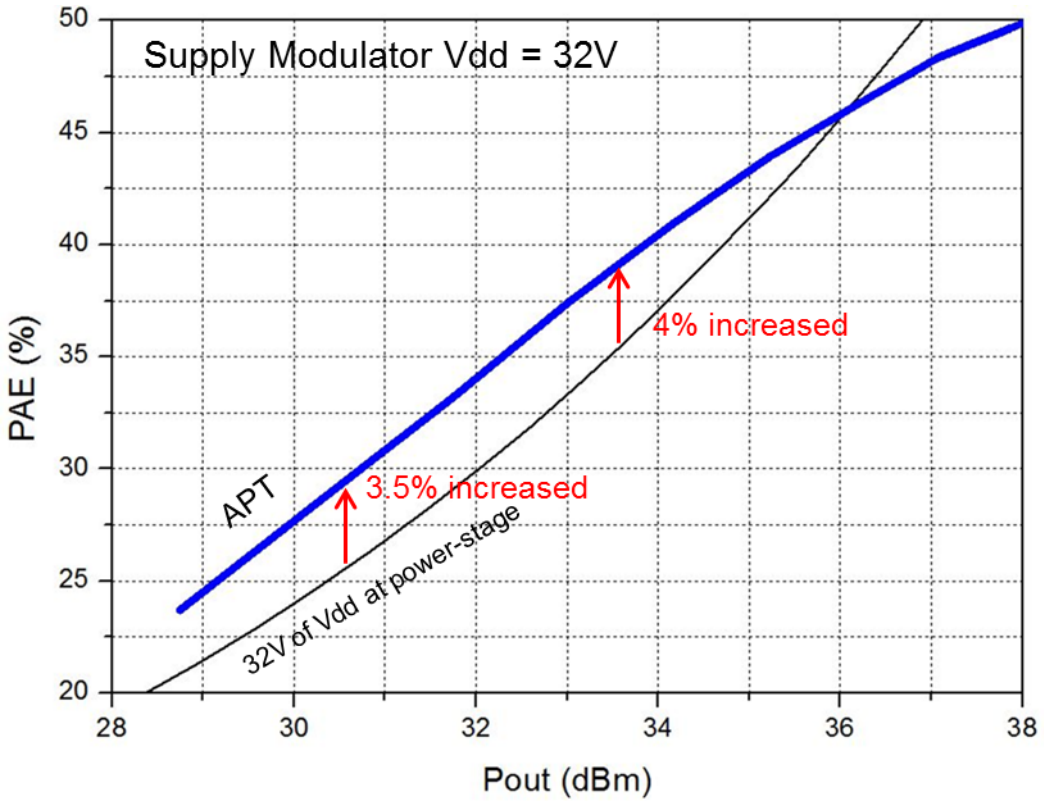



**Figure 84 Magnified version of measured overall system efficiency of the APT PA.**

**Table 11 Overall system efficiency of the APT PA**

| | | Stand-alone PA efficiency (%) | With modulator (%) | Efficiency increased (%) |
|---|---|---|---|---|
| **Compare to 32V** | Peak Efficiency | 62.7 | 49.5 | -13.2 |
| | 6dB Back-off | 35 | 39 | 4 |
| | 9dB Back-off | 25.5 | 29 | 3.5 |

In terms of power-stage DE, the APT system shows striking improvement. According to Figure 85, maximum power-stage DE of 56.8% at 38.0dBm of output power is shown. At 6dB back-off power, 15% of power-stage DE is improved resulting in 48% and 17% is improved at 9dB back-off power resulting in 40% of power-stage

DE.

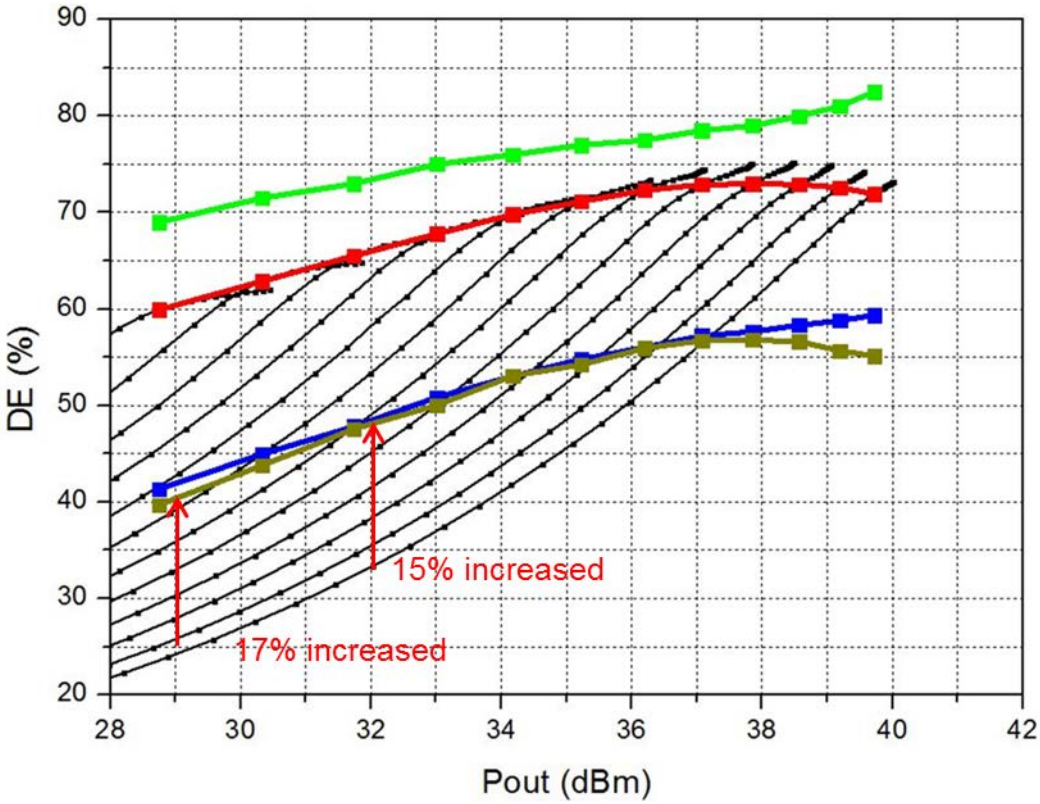



**Figure 85 Measured power-stage DE of the APT PA.**

The Photograph of test station is shown in Figure 86.

Table 12 shows the comparison with the systems of back-off efficiency enhancement. There is no work for average power tracking or envelop tracking in 5.8GHz range, however, many papers regarding Doherty Amplifier are published.

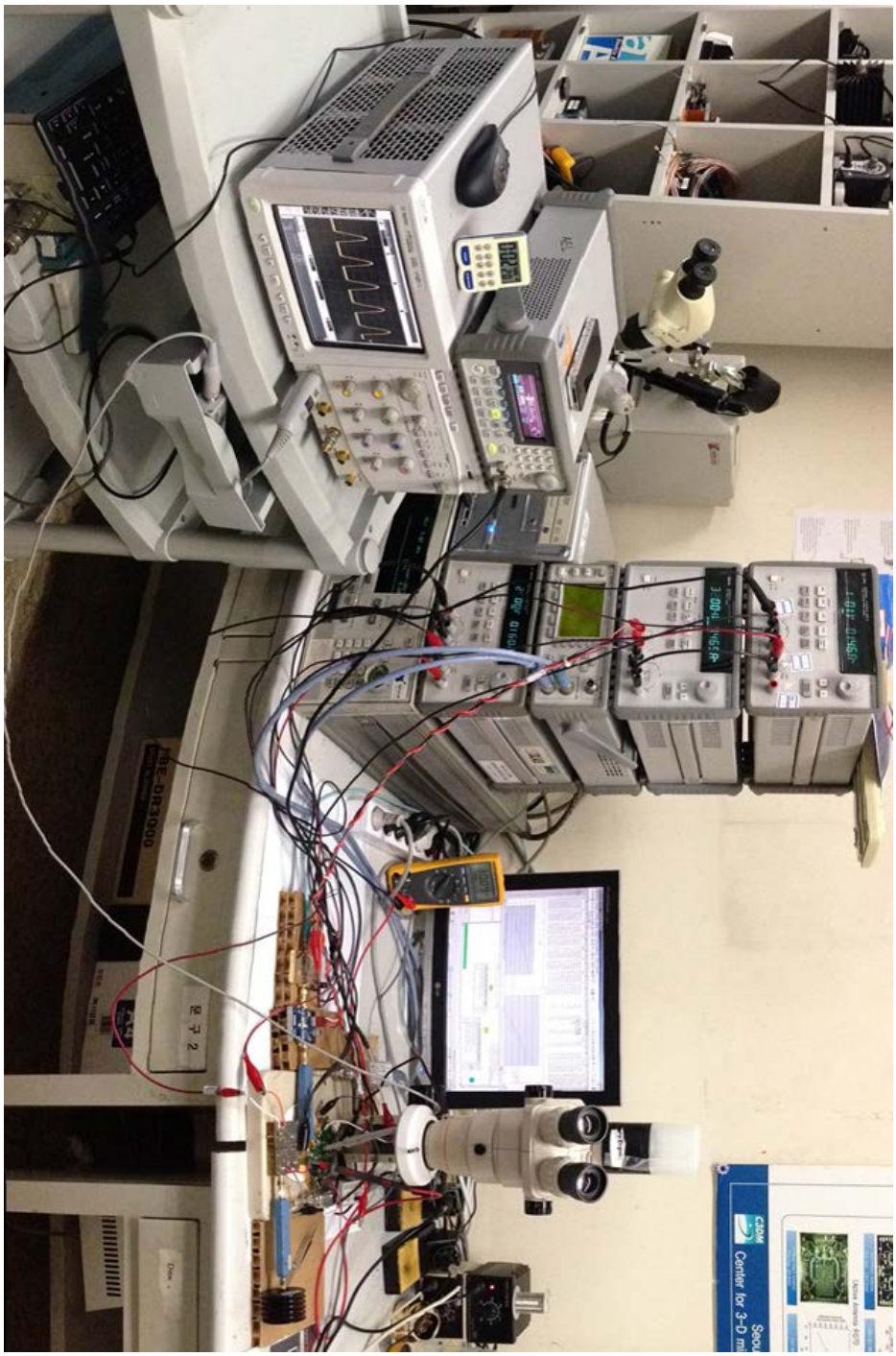


**Figure 86 Photograph of the test station.**

**Table 12 Comparison table for system of back-off efficiency enhancement**

| Ref | Freq. | $P_{out}$ | $PAE_{peak}$ | PAE @ Back-off | Technology |
|---|---|---|---|---|---|
| **2010 [15]** | 5.6 GHz | 34 dBm | 40.5 % | 27 % @ 6 dB | Hybrid GaAs Doherty |
| **2010 [16]** | 9.6 GHz | 30 dBm | 46% (DE) | 32% (DE) @ 6 dB | MMIC GaAs Doherty |
| **2011 [17]** | 5.8 GHz | 41.5 dBm | 63 % (DE) | 49% (DE) @ 6 dB | Hybrid GaN Doherty |
| **2013 [18]** | 7 GHz | 37 dBm | 51 % (DE) | 47 % (DE) @ 7 dB | MMIC GaN Doherty |
| **2013 [19]** | 6.8 GHz | 35 dBm | 42 % | 38 % @ 6 dB | MMIC GaN Doherty |
| **This work** | **5.8 GHz** | **40 dBm** | **49.5 %** | **39 % @ 6 dB** | **Hybrid GaN APT** |
| **This work** | **5.8 GHz** | **40 dBm** | **56.8 % (DE)** | **48 % (DE) @ 6 dB** | **Hybrid GaN APT** |

## 5.6. Conclusion

The new method to control Class $E^2$ DC-DC Converter is proposed. With the Pulse Width and Frequency Modulation (PWFM) signal, the problem of reduction in conduction angle in Class-E inverter is resolved and the efficiency of 11% at low output voltage is increased. With the newly introduced control method, Average Power Tracking (APT) system is realized. With the 2-Stage PA implemented in Chapter 3, the overall peak PAE of 49.5% is resulted when the output power is 39.6dBm. At 6 dB back-off power, 4% of PAE is increased from the stand-alone 32V supplied PA resulting in 39% of PAE. At 9 dB back-off power, 3.5% of PAE is increased from 25.5%. In terms of power-stage DE, maximum of 56.8% DE is shown at 38.0dBm. About 15% of efficiency is increased at 6dB back-off power resulting in 48% and 17% of efficiency is increased at 9dB back-off power resulting in 40% of power-stage DE.

# 6. Conclusion

In near future, the fabrication technology will evolve so that Gallium Nitride and (GaN) CMOS can be fabricated on one wafer. When this technology is developed, the advantage of high efficiency, high voltage breakdown, and high power density GaN and the advantage of fast, small, and cheap CMOS can emerge to serve its role accordingly as a system on chip (SoC). In this thesis, CMOS controlled GaN HEMT Class $E^2$ DC-DC converter is built and applied to highly efficient 2-Stage Class-E Power Amplifier.

Starting from the operational principle of class $E^2$ DC-DC converter, requiring CMOS components to control GaN HEMT supply modulator is discussed and designed. The CMOS components were fabricated using IBM 0.18um SOI 2.5V RF technology. The control circuit has been tested its operation and combined with GaN HEMT switches in the supply modulator. Those GaN HEMT switches serve as controlling DC output power of the supply modulator. The implemented supply modulator shows the maximum efficiency of 85% with 32V output voltage when 0.5 duty cycle is applied.

A 5.8GHz 2-Stage Class-E Power Amplifier (PA) is introduced and its essential parameter and its operations are numerically analyzed. With the computed equation, PA is designed with ideal lumped elements. Because the lumped elements in real world have low SRF and loss, it is required to replace with microstrip line. Taking variety of losses, such as conductor loss and loss tangent, an EM simulation is performed. Based on the EM simulation results, PA is implemented with Cree Inc.'s CGH60008D GaN HEMT. The experimental result shows the maximum power-added-efficiency (PAE) of 63.2% at 38.3dBm of output with 15.6dB gain when 28V of supply voltage is applied to the power-stage and 10V applied to the driver-stage. When 30V is applied to the power-stage of the PA, maximum PAE of 63.9% at 39.0dBm of output power with 15.8dB gain is resulted

By combining supply modulator with GaN HEMT PA, the PAE is not increased at the back-off power. Therefore, only the drain efficiency (DE) of the power-stage in

power amplifier is considered. When the supply modulator is applied to the power-stage only and kept constant voltage of 10V at driver-stage, increment in DE of power-stage can be noticed. At 6-dB back-off, 1% of DE is improved while 6% is increased at 9-dB back-off. Although the supply voltage of modulator is 28V, the maximum output voltage of the supply modulator is 31V. Thus, when comparing APT system power-stage DE to 30V supplied stand-alone PA, 5.7% and 8.7% of DE is improved at 6-dB and 9-dB back-off, respectively.

A new method to control the supply modulator is proposed. With PWFM control, Class $E^2$ DC-DC Converter obtains high efficiency even at the low output voltage. By applying this control method, the overall Average Power Tracking system shows the increment of 4% of PAE at 6dB back-off output power. At 9dBm back-off output power, 3.5% of PAE is increased while the peak efficiency is 49.5% at 39.6dBm of output power. In terms of power-stage DE, 15% and 17% of efficiency is increased at 6dB and 9dB back-off power while 56.8% of peak DE is shown at 38.0dBm.

In order to increase the back-off power efficiency more, a few things need to be corrected. A new power amplifier should be implemented. Due to the problem stated in Chapter 5, the new design should be focused to less decrement in PAE as the supply voltage decreases. This can be done by designing a high efficient and high power single-stage PA with a transistor having high gain. Second, the PWFM controlled supply modulator needs to be more optimized. As it is shown in Chapter 2, Class $E^2$ DC-DC Converter has potential to operate in high frequency with high efficiency. By performing the proposed supply modulator with higher frequency, highly efficient Envelop Tracking (ET) can be realized with promising material, GaN. The realization of PWFM with CMOS circuit is essential since the CMOS consumes much less power relative to the whole system of the GaN supply modulator. Because of the advantage of not having a series switch in Class $E^2$ DC-DC Converter, this advantage can be even stronger with CMOS control circuit for GaN supply modulator.

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# Appendix Notes

# Appendix Notes

# 초록

본 논문에서는 Cree 사의 CGH60 시리즈 GaN HEMT bare die 칩으로 제작된 PA 를 이용한 Average Power Tracking (APT) 시스템이 구현되었다. 전원 변조기의 제어 회로로써 IBM 0.18um SOI 2.5V RF 공정이 사용되었다.

전원 변조기로는 Class $E^2$ DC-DC컨버터가 사용되었다. Class-E 인버터와 Class-E정류기에 필요한 스위치로는 GaN HEMT가 사용되었다. 두 스위치 모두 CMOS회로에서 펄스 폭 변조 (PWM)방식으로 만들어진 펄스로 제어되었다. 공급 전압 28V와 1MHz PWM신호를 사용한 결과 듀티가 0.5 일 때 최대 효율 85%와 31V의 출력 전압을 얻을 수 있었다.

GaN HEMT 를 이용하여 5.8GHz 고효율 2-단 Class-E 전력 증폭기도 제작되었다. 수치해석적으로 초기 디자인이 진행되었으며, lumped 소자들은 모두 마이크로스트립으로 대체되었다. 측정 결과 39dBm 에서 63.9%의 효율을 얻을 수 있었으며 그때의 전력 이득은 15.8dB 였다. Power-단의 드레인 효율은 76%였다.

백오프 구간에서의 효율을 올리기 위해 APT 시스템이 적용되었다. 시스템의 Power-단 드레인 효율은 6dB 백오프 지점에서 1%증가하였으며 9dB 백오프 지점에서 5.7% 증가하였다. 전원 변조기의 최대 출력 전압은 32V 로 부스팅 되기 때문에 최대 출력 전력은 37.9dBm 에서 38.7dBm 으로 증가하였다.

전원 변조기를 제어하기 위해 펄스 폭과 주파수 변조 (PWFM)방식이 PWM 대신 제안되었다. 제안된 전원 변조기는 12V 출력전압일 때 11%의 효율 증가를 보여주었으며 따라서 넓은 출력 전압 영역에서 70%이상의 효율을 보여주었다. 같은 PA 에 APT 를 적용한 결과 39.6dBm 에서 최대 PAE 49.5%를 얻을 수 있었다. 6dB 와 9dB 백오프 지점에서의 효율은 각각 4%와 3.5%씩 증가하였다.

**Keywords:** Average Power Tracking (APT), Class-E Power Amplifier, Class $E^2$ DC-DC converter

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- Clifford DY Cheon