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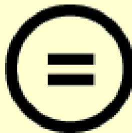

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Direct Cu Deposition on Ru and Co/Ni Alloy Barrier Layer for the Next-generation Cu Damascene Process

차세대 구리 상감 공정을 위한 루테늄 및 코발트/니켈 합금 확산 방지막 상 직접 구리 도금

2016년 2월

서울대학교 대학원

화학생물공학부

김 광 환

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지도교수 김 재 정

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서울대학교 대학원
화학생물공학부
김 광 환

김광환의 공학박사 학위논문을 인준함
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위 원 장 ____________________ (인)

부 위 원 장 ____________________ (인)

위 원 ____________________ (인)

위 원 ____________________ (인)

위 원 ____________________ (인)

ABSTRACT

In semiconductor manufacturing history, the transition of conducting material from Al to Cu was considered one of the most significant changes. Such replacement is accompanied with the introduction of damascene process, which proceeds first by deposition and patterning of the dielectric layer. Then the patterned dielectric is covered with diffusion barrier layer and Cu seed layer. Subsequently, Cu is filled by superfilling techniques, resulting in void-free and seamless filling of trenches and vias with high aspect ratios. Among these steps, the diffusion barrier and Cu seed layer are formed by physical vapor deposition. However, the problem induced by the poor step coverage of the diffusion barrier/Cu seed layer has become serious as trenches are being reduced. Therefore, different deposition methods such as chemical vapor deposition, atomic layer deposition, electroless deposition, and direct electrodeposition are considered as alternatives to physical vapor deposition for the formation of the barrier/seed layer. Specifically, electroless deposition and direct electrodeposition have received much interest due to their various advantages.

In this study, the entire metallization processes were modified for the next-generation interconnect fabrication. On Ta barrier layer, direct Cu electrodeposition was developed using Pd nanoparticles as a Cu nucleation promoter. Pd nanoparticles were synthesized

by a polyol method and loaded onto a pretreated Ta substrate. Through a two-step potentiostatic electrodeposition process in a pyrophosphate-based electrolyte, a continuous Cu seed layer was deposited on the Ta substrate, although the surface showed irregular morphology. The addition of allyl alcohol improved the surface regularity of the Cu seed layer, allowing the conformal Cu seed layer to be formed successfully on the 55 nm patterned Ta substrate. Cu gap-filling was achieved by galvanostatic ED in a sulfate-based electrolyte on the preformed seed layer.

On SiO_2 substrate, electroless deposition of various barrier layers was investigated for all-wet Cu interconnect fabrication. In this study, the entire fabrication process including substrate activation, barrier layer electroless deposition, and direct Cu electrodeposition was modified. The SiO_2 substrate was activated via Pd nanoparticles that were immobilized on the substrate by using a preformed self-assembled monolayer composed of 3-aminopropyl-triethoxysilane. Reduction of barrier layer resistivity was achieved by applying ultrasound during the substrate activation process and by adjusting the composition of the electroless deposition bath. The Cu electrodeposition was performed directly on the electroless barrier layers after performing coulometric oxide reduction, thus improving the adhesion and nucleation density of Cu on the barrier layer. The electrodeposition process was conducted in two steps: Cu nucleation and Cu thin film formation at a high overpotential followed by additional Cu film growth at a low overpotential. As a result, a uniform, smooth Cu film covered the barrier layer. In

addition, bottom-up Cu filling was accomplished on a 120 nm wide, patterned substrate with a 2.5 aspect ratio. Barrier layer performance was evaluated by using a stacked specimen formed by applying the proposed procedure.

On Ru substrate which is considered as next-generation barrier material, Cu growth phenomena were investigated during electroless deposition. Different to the formaldehyde based bath, the use of hydrazine based bath facilitated the observation of Cu growth phenomena during the electroless deposition. The whole surface-catalyzed electroless deposition occurred on Ru, and electrochemical quartz crystal microbalance as well as linear sweep voltammetry studies revealed that Cu covered Ru surface within a few seconds of deposition. Measurement of sheet resistance change confirmed that Cu nucleation on Ru was continuous with forming a film. During the period, Cu film growth was monitored by an atomic force microscope imaging, indicating that Cu was deposited on Ru preferentially, rather than on the deposited Cu at the initial stage of the deposition. The whole surface-catalyzed electroless deposition achieved the 55 nm gap-filling, and this showed the possibility of the practical adoption of electroless deposition as a method for metallization in ultralarge-scale integration.

keywords: Cu, direct electrodeposition, electroless deposition, next-generation barrier layer, all-wet metallization

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TABLE OF CONTENTS

ABSTRACT i

TABLE OF CONTENTS iv

LIST OF TABLES vii

LIST OF FIGURES viii

CHAPTER I. Introduction and overview 1

1.1. The interconnection technology for ULSI 1

1.1.1. The present and issues of interconnection technology 1

1.1.2. The next-generation interconnection technology 4

1.2. Direct Cu deposition 12

1.2.1. Direct Cu ED 12

1.2.2. Cu ELD 13

1.2.3. Direct Cu ELD 15

1.3. All-wet metallization 19

1.3.1. Electroless Co/Ni alloy as a barrier/capping material 19

1.3.2. All-wet metallization 23

1.4. Concepts of the study 29

CHAPTER II. Experimental 31

2.1. Direct ED of Cu on Ta 31

2.1.1. Preparation of Pd NPs 31

2.1.2. Direct ED of Cu on Ta 32

2.2. Direct ED of Cu on Co/Ni alloy 35

2.2.1. Pretreatment of substrate and SAM-Pd activation 35

2.2.2. ELD of Co/Ni alloy films and direct Cu ED 36

2.3. Direct ELD of Cu on Ru 38

2.3.1. Pretreatment of Ru and direct Cu ELD 38

2.3.2. Preparation of Ru electrode and EQCM monitoring 39

2.4. Instrumentation 41

CHAPTER III. Direct ED of Cu on Ta 44

3.1. Seed layer formation by direct Cu ED on blanket Ta substrate 44

3.1.1. Pd NPs loading on blanket Ta substrate 44

3.1.2. Cu seed layer formation by direct Cu ED on Pd NPs-loaded Ta substrate 45

3.2. Trench filling by direct Cu ED on patterned Ta substrate 56

CHAPTER IV. Direct ED of Cu on Co/Ni alloy 62

4.1. ELD of Co/Ni alloy barrier layer 62

4.1.1. Optimization of substrate activation process 62

4.1.2. Optimization of barrier layer ELD 64

4.2. Direct Cu ED on ELD-barrier layer 76

4.3. Barrier layer performance and trench filling 88

4.3.1. Barrier layer performance investigation 88

4.3.2. Trench filling by all-wet metallization process 89

CHAPTER V. Direct ELD of Cu on Ru 97

5.1. Cu growth phenomena on Ru during ELD 97

5.1.1. Preparation of Ru electrode for EQCM monitoring 97

5.1.2. Observation of Cu growth phenomena on Ru during ELD 98

5.1.3. Determination of Cu growth phenomena on Ru during ELD 103

5.2. Trench filling by direct Cu ELD on patterned Ru substrate 117

CHAPTER VI. Conclusions 120

REFERENCES 122

국문초록 133

LIST OF TABLES

Table 2.1. Composition of ELD Bath for the Deposition of NiWP / CoWP / NiCoP...... 37

Table 4.1. Composition and Properties of Each Barrier Layer 67

Table 5.1. Calculated Thickness of Deposited Cu on Ru... 106

LIST OF FIGURES

Figure 1.1. Gate and interconnect delay versus technology generation (edited from ref. [3]).. 7

Figure 1.2. Predictions of ULK roadmap in the ITRS'2005, 2009, and 2011, and the final decisions of ITRS'2013 (edited from ref. [9]). 8

Figure 1.3. Measured narrow Cu line resistivity (blue circles) versus line width. Comparisons are depicted with suggested models considering electron scattering due to surface and grain boundaries (edited from ref. [16]). 9

Figure 1.4. Prediction of low-k materials scaling according to the 2013 edition of ITRS Roadmap. 10

Figure 1.5. Schematic diagram of the damascene process of Cu in ULSI. 11

Figure 1.6. Seam formation after conformal ELD in narrow trench. 17

Figure 1.7. Void-free filling of narrow trench by ELD with organic additives. 18

Figure 1.8. W versus P atomic content for ELD-CoWP (edited from ref. [62,63]). 25

Figure 1.9. W versus P atomic content for ELD-NiWP (edited from ref. [64-71]).......... 26

Figure 1.10. Damascene Cu interconnect EM data comparing undoped Cu with Co alloy capping layer to Si(C)N dielectric capping layer (edited from ref. [59])...... 27

Figure 1.11. Schematic diagram of the "all-wet" metallization process. 28

Figure 2.1. Schematic diagram of the direct Cu ED process on Ta assisted by the Pd NPs.

.... 34

Figure 2.2. Schematic illustration of direct Cu ELD process on Ru substrate................. 40

Figure 2.3. Schematic illustration of method for film adhesion test referring to ASTM D3359.[111] 43

Figure 3.1. (a) TEM image of synthesized Pd NPs on TEM grid and (b) number probability of Pd NPs according to the particle size. 49

Figure 3.2. (a) The mass change during the Pd NPs coating process on QCM electrode and (b) XPS analysis of the Ta substrate after Pd NPs loading..................... 50

Figure 3.3. The AFM surface morphology of Ta substrate (a) before and (b) after the Pd NPs loading. 51

Figure 3.4. FESEM images of Cu deposited on (a, c) blanket Ta and (b, d) Pd NPs-loaded Ta substrates. Inset in (d): AFM image of the specimen. 52

Figure 3.5. (a) LSV on Pd NPs-loaded Ta substrate with the addition of allyl alcohol to the Cu-Pyro bath (scan rate = 10 mV s^{-1}). (b, c) FESEM images of Cu film deposited on Pd NPs-loaded Ta substrate with 0.035 M allyl alcohol. Insets in (c): AFM image of the specimen... 53

Figure 3.6. LSV on Cu deposited on (a) the blanket Ta, (b) the Pd NPs-loaded Ta without allyl alcohol, and (c) the Pd NPs-loaded Ta with 0.035M allyl alcohol. LSV experiments were conducted in Cu-Sul bath (scan rate = 10 mV s^{-1})........... 54

Figure 3.7. LSV on a Cu seed layer prepared on the Pd NPs-loaded Ta by direct ED in

Cu-Pyro bath containing 0.035 M allyl alcohol. LSV experiment was conducted in Cu-Sul bath (scan rate = 10 mV s^{-1}) and the concentration of each additive is specified in the Chapter 2.1.2. 55

Figure 3.8. FESEM images of 55 nm patterned Ta substrate (a, d) before seed layer deposition and after seed layer formation (b, e) without Pd NPs and (c, f) with Pd NPs.. 58

Figure 3.9. FESEM images of Cu seed layer deposited on 55 nm patterned Ta with Pd NPs, according to the allyl alcohol concentration. Allyl alcohol content in Cu-pyro bath was (a, e) 0.0175 M, (b, f) 0.035 M, (c, g) 0.0525 M, and (d, h) 0.07 M. 59

Figure 3.10. (a) Trench opening width after Cu seed layer formation with varying the allyl alcohol concentration in Cu-Pyro bath and (b) TEM image for the Cu seed layer deposited with 0.07 M allyl alcohol (Pt was sputtered before the TEM specimen preparation by FIB). 60

Figure 3.11. TEM analyses of 55 nm patterned trench covered with the Cu seed layer after filling in Cu-Sul bath. The Cu seed layer was prepared by direct ED on the Pd NPs-loaded Ta with 0.07 M allyl alcohol in Cu-Pyro bath. 61

Figure 4.1. FESEM surface analyses of ELD-NiWP layer deposited on (a) Sn-Pd activated and (b) SAM-Pd activated SiO_2 blanket substrate. Picture of the specimen was also taken after ELD (insets). 68

Figure 4.2. The AFM morphology analyses of (a) pristine SiO_2 substrate and the SiO_2 substrate after SAM-Pd activation (b) without and (c) with sonication during the Pd NPs adsorption step. (d) and (e) show FESEM surface and cross-sectional (insets) analyses for a 25 nm thick NiWP film deposited on (b) and (c), respectively. 69

Figure 4.3. The effect of PEG concentrations on (a) the rate of NiWP ELD and (b) resistivity and surface roughness of a 25 nm thick NiWP film. 70

Figure 4.4. Surface and cross-sectional FESEM analyses of CoWP layer deposited with 0.4 M citrate and 0.2 M NaH_2PO_2. 71

Figure 4.5. Effect of citrate and NaH_2PO_2 concentration on the deposition rate of CoWP ELD and resistivity of 25 nm thick CoWP film. 72

Figure 4.6. FESEM surface analyses of $Ni_xCo_{(0.04-x)}P$ film prepared with each deposition condition. 73

Figure 4.7. The deposition rate and resistivity of 25 nm thick Ni_xCo_yP film prepared in each deposition condition. 74

Figure 4.8. XRD analyses of each barrier layer having 25 nm of thickness. 75

Figure 4.9. Results of XPS analyses of NiWP film before (black line) and after (red line) undergoing the coulometric reduction process (slight oxidation occurs during sample transfer). 80

Figure 4.10. Results of LSV on the NiWP layer before (black line) and after (red line)

coulometric reduction (scan rate = 20 mV s^{-1}). 81

Figure 4.11. Pictures of (a) as-prepared NiWP film and (b, c) Cu film electrodeposited (b) without coulometric reduction process or (c) after coulometric process on NiWP film. 82

Figure 4.12. The LSV results on the NiWP layer before (black line) and after (red line) coulometric reduction process. The LSV studies were conducted in 1 M H_2SO_4 electrolyte (Cu ED bath without Cu ion and additives, scan rate = 20 mV s^{-1}). 83

Figure 4.13. Results of LSV on each barrier layer after coulometric reduction (scan rate = 20 mV s^{-1}). 84

Figure 4.14. FESEM surface analyses of 25 nm thick NiWP layers (a) after coulometric reduction, and (b-e) after Cu ED at (b) −0.75 V, (c) −1.0 V, (d) −1.25 V, and (e) −1.5 V vs. SCE. In all cases, the deposition charge density was 10 mC cm^{-2}. 85

Figure 4.15. The effect of deposition potential on the ratio of the sheet resistance after Cu ED (R_S) to the resistance before Cu ED (R_{S0}). The deposition charge density was 10 mC cm^{-2} and the average R_{S0} for the 25 nm thick NiWP layer was 35 Ω $square^{-1}$. 86

Figure 4.16. FESEM surface analyses of a Cu film deposited on a NiWP layer (a) at −1.25 V (vs. SCE) for 200 mC cm^{-2} and (b) at −1.25 V (vs. SCE) for 10 mC

cm^{-2} followed by −0.45 V (vs. SCE) for 190 mC cm^{-2}. The insets present a cross-sectional FESEM images of a 100 nm thick Cu film on a 25 nm thick NiWP layer. 87

Figure 4.17. FESEM surface analyses of 25 nm thick (a) NiWP, (b) CoWP, (c) $Ni_{0.03}Co_{0.01}P$, and (d) $Ni_{0.02}Co_{0.02}P$ formed by ELD on SAM-Pd activated SiO_2 substrate. (a'~d') FESEM surface analyses of 100 nm thick Cu film directly deposited by ED on corresponding (a~d) ELD-barrier layer. 91

Figure 4.18. Change in sheet resistance after thermal treatment (500℃, 30 min in a N_2 atmosphere) of each specimen having different barrier layer. The thickness of each barrier layer was 25 nm and that of the overlaying Cu was 100 nm..... 92

Figure 4.19. XRD analyses of a Cu (100 nm) / NiWP (25 nm) / SiO_2 stacked specimen before (black line) and after (red line) thermal treatment at 500℃ for 30 min in a N_2 atmosphere. 93

Figure 4.20. LSV on the NiWP substrate after 1st step Cu ED with varying the additive combination in Cu ED electrolyte. Inset: LSV on the 30 nm thick Cu film after CRM. The scan rate was 20 mV s^{-1}. 94

Figure 4.21. (a) FESEM image of 120 nm width trench after NiWP barrier layer formation and (b) the evaluation of conformality. 95

Figure 4.22. FESEM images of 120 nm width trench (a) after NiWP ELD and after direct Cu ED on (a) with total charge amount of (b) 150 mC cm^{-2}, (c) 200 mC cm^{-2},

and (d) 300 mC cm^{-2}. 96

Figure 5.1. (a) QCM analysis during the displacement reaction between Cu and Ru ion on Cu electrode. (b, c) FESEM analyses of (b) before and (c) after Ru displacement reaction on Cu electrode. 107

Figure 5.2. E transient as a function of the ELD time both on Ru wafer and electrode. ELD was conducted in a hydrazine based Cu ELD bath. 108

Figure 5.3. The effect of HF treatment on the potential transient during coulometric reduction of Ru surface. 109

Figure 5.4. The EQCM monitoring on Ru electrode in formaldehyde or hydrazine based Cu ELD bath. Changes in (a) potential and (b) mass change rate were simultaneously recorded as a function of time. 110

Figure 5.5. The sheet resistance ratio (R_{S0}/R_S) change of Ru substrate with respect to the deposition time in formaldehyde or hydrazine based Cu ELD bath. 111

Figure 5.6. LSV on Ru and on Cu deposited Ru substrate (scan rate = 20 mV s^{-1})........112

Figure 5.7. AFM morphology analyses of electroless deposited Ru according to the deposition time. 113

Figure 5.8. XRD analyses of blanket Ru and 55 nm Cu prepared by ELD on Ru in hydrazine based Cu ELD bath. 114

Figure 5.9. Electrochemical stripping of ELD-Cu on Ru substrate (scan rate = 20 mV s^{-1}). 115

Figure 5.10. XPS spectra of (a) 3 s, (b) 5 s, and (c) 6 s deposited Ru substrate. 116

Figure 5.11. Dependence of deposition rate of Cu ELD and the resistivity of resultant Cu film on the concentration of DPS in the bath. 118

CHAPTER I. Introduction and overview

1.1. The interconnection technology for ULSI

1.1.1. The present and issues of interconnection technology

An integrated circuit (IC) is a set of electronic circuits on one small plate of semiconductor material. Modern ICs can be made very compact, incorporating up to several billions transistors and other electronic components in an area of about 1 cm^2 in consequence of ultra-large scale integration (ULSI).[1] All transistors and other IC components have to be electrically interconnected to provide the proper functionality. The width of the conducting lines that connect different transistors in a circuit is becoming smaller as the technology advances; it dropped below 100 nm in 2008 and in 2015, the width of the half-pitch for metal 1 of memory and logic ICs reached 24 nm and 32 nm, respectively.[2]

In parallel, the interconnect delay is becoming an increasing limitation of the overall signal propagation delay. The total resistance (R) of the interconnect structure is now a significant factor affecting the chip performance. At the same time, the capacitance (C) between wires is increasing due to the decreasing spacing between the wires. Both

factors significantly increase the RC delay of IC circuits. In the early 1990s, the semiconductor industry found that the concept to improve IC performance by enhancing the speed of individual transistors through scaling should be complemented by an improvement of the interconnect delay. This was possible by making changes to the materials used for both the wires and the insulator (Fig. 1.1).[3] The need to decrease the RC delay, the dynamic power consumption, and the cross-talk noise was the main driving force behind the introduction of new materials to the back-end-of-line (BEOL, the part of the IC manufacturing process where interconnects are made) integration.[4]

Metallic conductivity and resistance to electromigration of bulk copper (Cu) were known to be better than those for aluminum (Al), which was the interconnect material until Cu interconnect was introduced in the late 1990s.[5] Application of an interconnect material with lower resistivity such as Cu decreases the interconnect RC delay, which, in turn, increases the IC speed.[6] The transition to Cu as the conductor was one of the most significant changes in semiconductor manufacturing history. The first working microprocessor using Cu was made by IBM in 1997 and the process was introduced into high volume manufacturing in IBM's facilities in 1998.[5]

Replacement of Al by Cu has an enormous obstacle for the semiconductor industry, because Al is deposited over the entire wafer surface and then patterned by reactive ion etching (RIE).[7] Cu cannot be patterned by traditional RIE because of the very low vapor pressure of the reaction products, and a new process had to be developed. As a result, the

damascene process has emerged as the industry standard.[8] The dielectric layer is deposited and patterned first before the metal deposition. Then the patterned dielectric is filled by superfilling techniques, in which higher deposition rates are achieved at the bottom of the trenches with respect to the sidewalls, resulting in void-free and seamless filling of trenches and vias with high aspect ratios. These processes have played a pivotal role in the success of this technology.

However, the introduction of Cu was not sufficient for the necessary reduction of RC delays. The most straightforward way to reduce the C value is to lower the dielectric constant (k) of dielectric layer. Fig. 1.2 shows the trends in k number, referred to the ITRS roadmaps of three different editions.[9] Despite the ITRS roadmap kept pushing lower-k forward to more advanced node, the real situation had been much more challenging and complicated. According to 2013 edition of the ITRS, ultra-low-k (ULK) materials with dielectric constants still as high as k = 2.5 were integrated in 2012 (Fig. 1.2).[9] The general issue of (porous) low-k materials is that they are generally soft, mechanically weak, and do not adhere well to silicon or metal wires. Furthermore, porous low-k materials do not withstand conventional interconnect processing (e.g. they degrade during the plasma and chemical processing). Several different types of low-k materials have been considered. Initially, organosilicate-based (OSG) ULK materials were rapidly developed, such as XLK, LKD, NCS, etc.; however, they quickly met huge challenges during their integration.[10] Low-k dielectrics based on organic polymers have

low polarizability and, therefore, are able to provide the lowest k values (2.8–3.0) without requiring the introduction of porosity. However, efforts to integrate organic materials into ICs have also not been successful. In addition to poor mechanical and thermal properties, the key problems were related to the relatively high coefficient of thermal expansion (CTE) with respect to other components of ICs.[11]

Additional challenges during the introduction of Cu and low-k dielectrics are related to the high diffusivity of Cu ions.[2] To avoid Cu diffusion into the dielectric, significant efforts were made to develop Cu diffusion barriers. These include conductive barriers isolating the Cu wire and the low-k dielectric in a metallization level and dielectric barriers deposited after chemical mechanical planarization (CMP) and before starting the next metallization level. The major requirements for these barrier layers are their density and amorphous nature and a lack of any chemical groups that can oxidize Cu so that no Cu ions can be formed.[12-15] Therefore, the barriers must be hydrophobic and good barriers against moisture diffusion because penetrated water can oxidize Cu and form Cu ions.

1.1.2. The next-generation interconnection technology

The efforts during the last two decades have made the Cu/low-k technology matured. While Cu was successfully introduced to decrease the interconnect delay, the

development and the selection of both low-k dielectrics and more suitable conductor materials other than Cu are becoming subjects of intensive research, owing to the aggressive scaling of Cu line width and height. Indeed, the Cu resistivity drastically increases below line widths of 20 nm due to pronounced size effects (Fig. 1.3).[16] Nevertheless, Cu remains uncontested conductor in view of conductivity and resistance to electromigration.[17] While the search for new interconnect materials such as carbon nanotubes and graphene is ongoing, there are still no clear alternative materials at this point.[18] Due to the long transition time from research to production, there is a great risk that no novel material will be ready to replace Cu/low-k interconnects at 11nm or even smaller technology nodes.

According to the ITRS, material innovation in combination with traditional scaling will no longer satisfy the performance requirements in the long-term and radically new interconnect paradigms are needed. For example, the integration beyond the 7 nm technology node is currently much less clear and a “red brick wall” (Fig. 1.4) appears in the 2013 edition of the ITRS Roadmap.[2] Therefore, processing as well as architectural solutions, instead of materials solutions, are being suggested.

As already be mentioned in Chapter 1.1, the damascene process is composed of the patterning of a low-k dielectric layer, the deposition of a diffusion barrier/Cu seed layer, Cu gap-filling, and CMP (Fig. 1.5).[19] Among these steps, the diffusion barrier and Cu seed layer are formed by physical vapor deposition (PVD). Generally, metals deposited

by the PVD method show good adhesion with the substrate and superior film properties, such as low resistivity and low surface roughness.[20,21]

However, the problem induced by the poor step coverage of the diffusion barrier/Cu seed layer has become serious as trenches are being reduced. Various papers have reported the difficulties in Cu gap-filling by electrodeposition (ED) due to overhang and defects at the sidewalls of the PVD diffusion barrier/Cu seed layer on narrow trenches.[22-25] Therefore, other deposition methods such as chemical vapor deposition (CVD), atomic layer deposition (ALD), electroless deposition (ELD), and direct ED are considered as alternatives to PVD for the formation of the barrier/seed layer. Specifically, ELD and direct ED have received much interest due to their various advantages, such as their low process cost, short process time, and excellent control of the thickness of the deposited metal.[26]

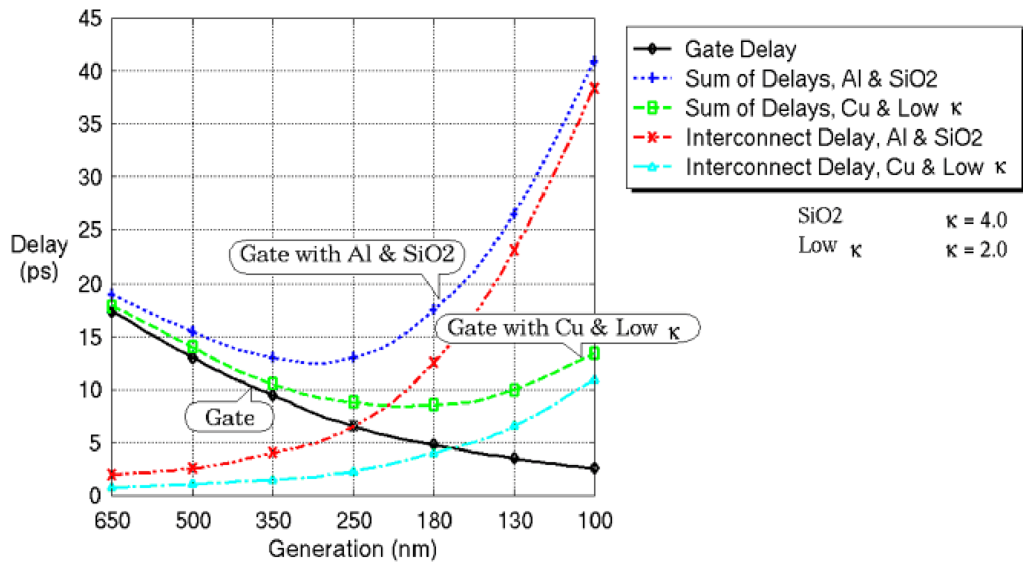
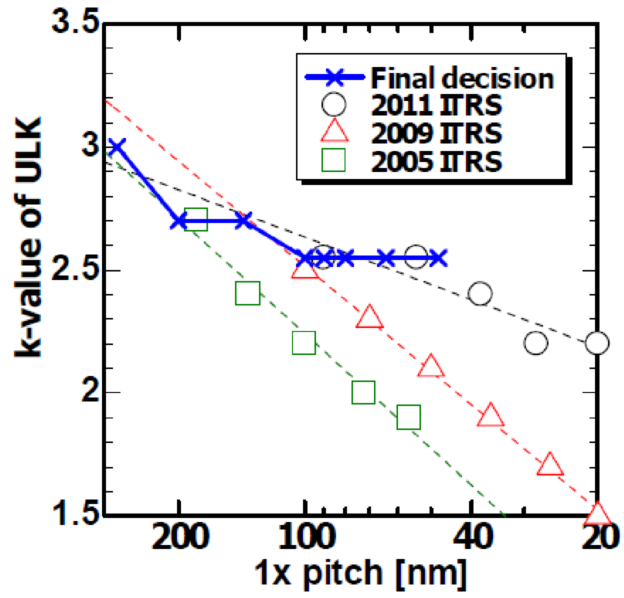


Figure 1.1. Gate and interconnect delay versus technology generation (edited from ref. [3]).



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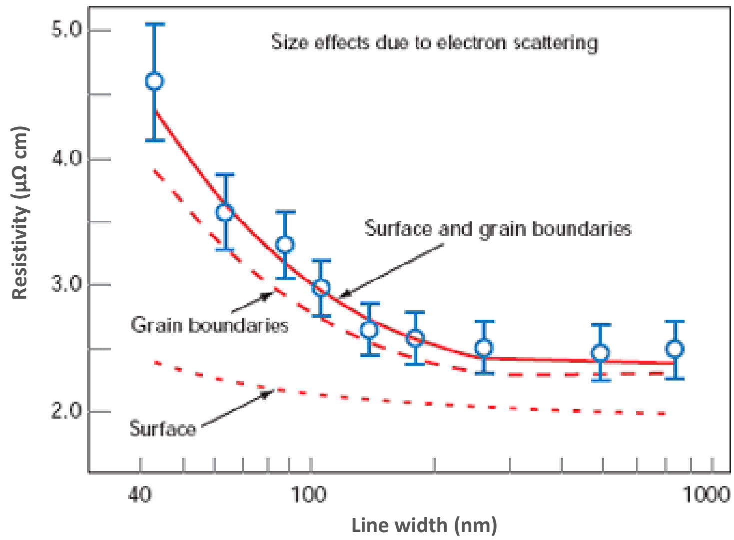


Figure 1.3. Measured narrow Cu line resistivity (blue circles) versus line width. Comparisons are depicted with suggested models considering electron scattering due to surface and grain boundaries (edited from ref. [16]).

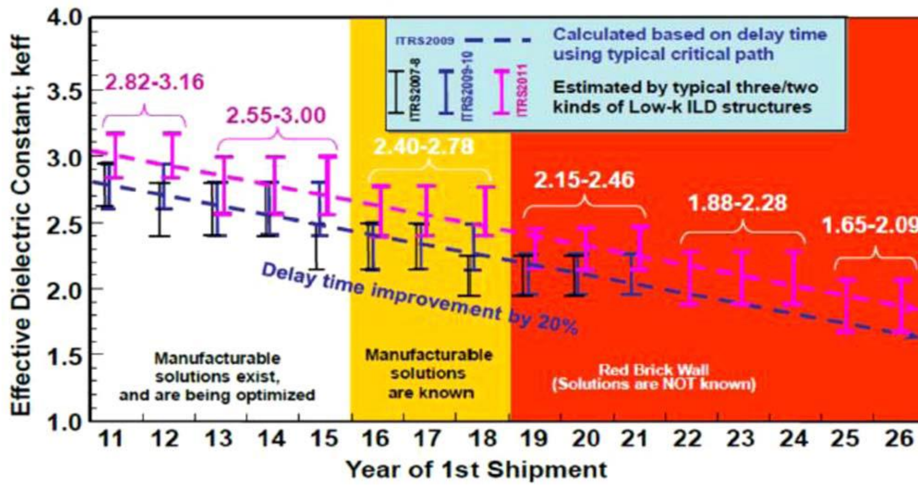


Figure 1.4. Prediction of low-k materials scaling according to the 2013 edition of ITRS Roadmap.

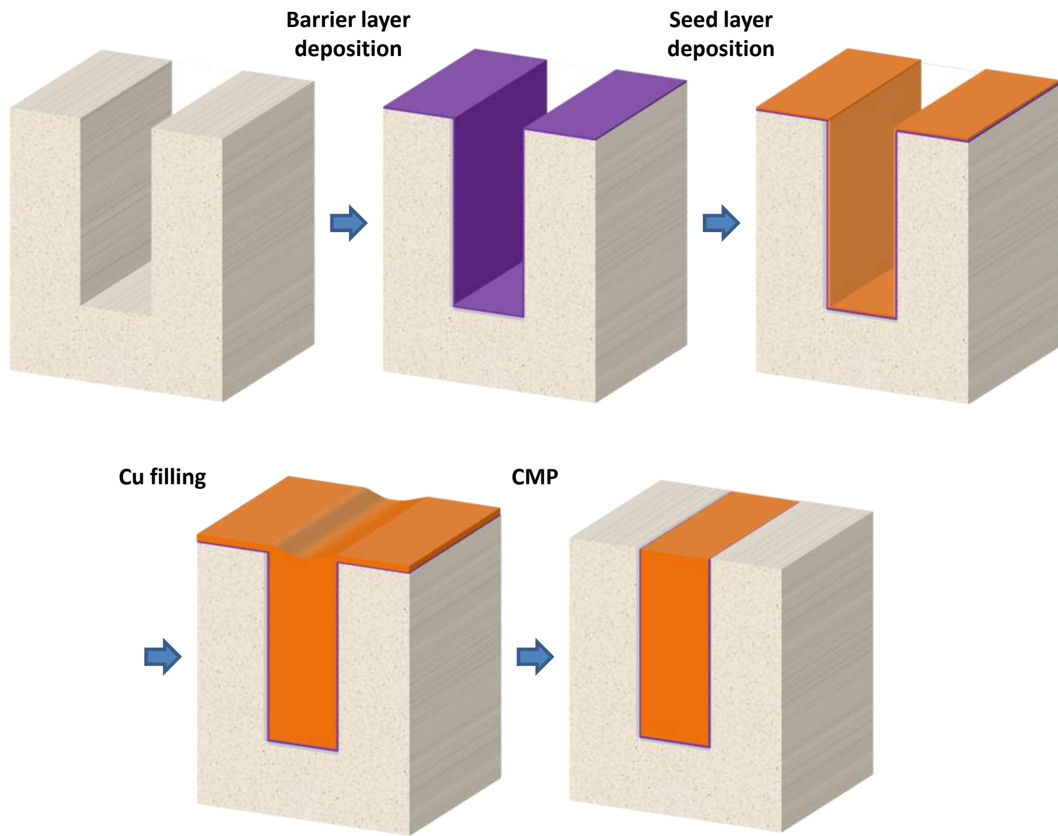


Figure 1.5. Schematic diagram of the damascene process of Cu in ULSI.

1.2. Direct Cu deposition

1.2.1. Direct Cu ED

Direct Cu ED is defined as the ED of Cu without a Cu seed layer on a heterogeneous substrate such as tantalum (Ta), titanium (Ti), iridium (Ir), or ruthenium (Ru). Some papers reported Cu superfilling of sub-micron features as well as seed layer deposition performed by direct ED.[22,27-31] Our previous paper described the direct Cu ED on a TiN/Ti diffusion barrier with the aid of a palladium (Pd) particle which was formed via a displacement reaction.[22] The displaced Pd particle assisted in the formation of a uniform Cu film layer by reducing the charge transfer resistance during the ED process. Thus, defectless superfilling was realized on a 400 nm feature. In addition, studies of direct Cu ED on a Ta-based barrier layer were also published by Kim *et al.* and Starosvetsky *et al.* Kim *et al.* focused on the observation of the growth of Cu films on a TaN substrate after the anodic removal of Ta oxides in a saturated KOH solution.[30] Starosvetsky *et al.* succeeded in the seedless gap-filling of a 300 nm trench which consisted of a TaN/Ta barrier layer after a cathodic pretreatment in a pyrophosphate-based electrolyte.[31]

Although various approaches have been reported by various research groups, it is still challenging by means of direct ED to fill sub-100 nm trenches covered with highly resistive barriers owing to their low conductivity and large charge transfer resistance. The

aforementioned studies applied various strategies, such as native oxide removal or the use of Pd activation: however, the remaining oxides or large Pd particles especially with a wide distribution prohibited the formation of an ultrathin layer and the sub-100 nm feature filling.

1.2.2. Cu ELD

ELD is a well-known method for preparing thin films of metals and their alloys.[32] It is a highly selective method allowing additional patterning of isolated and embedded structures on insulating substrates, e.g. glass, plastic or ceramic. ELD is a relatively low temperature (less than the boiling point of the electrolyte) and low cost process compared to other deposition methods such as PVD or CVD.[33-35] ELD features uniform and normally conformal deposition with low defect density and some unique material properties. In the last few decades, ELD of metals (e.g. copper, gold, nickel, cobalt, palladium, iron, silver, etc.) and their alloys was demonstrated for micro system applications: microelectronics, micro electro mechanics, micro electro optics and microfluidics, micro fuel cells, micro batteries etc. ELD was also demonstrated on nano structures, both artificial and natural.[32,36] The progress in ELD followed the need and the trend for better metallization technologies for complex structures with critical dimensions that had been shrinking continuously in the last few decades.[37-39]

Electroless Cu for ULSI metallization was proven to be competitive to ED. The resistivity of ELD-Cu could be in the range of 2.0-μΩ cm and it was capable of forming deep submicron features.[40] Cu ELD was highly conformal, leading to seam formation at the center of interconnect lines (Fig. 1.6). Void-free filling of high aspect ratio via-holes was reported with the proper choice of additives such as bis-(3-sulfopropyl)-disulfide (SPS) and mercapto alkyl carboxylic acids as accelerators, and poly(ethylene glycol)-poly(propylene glycol) triblock copolymers as inhibitors.[41-43] Void-free electroless Cu deposition in sub-micrometer trenches was obtained in the presence of poly(ethylene glycol) (PEG) as inhibitor as well as accelerating species such as SPS and its derivatives, 3-N,N-dimethylamino-dithiocarbamoyl-1-propanesulfonic acid (DPS) and 2-mercapto-5-benzimidazole-sulfonic acid (MBIS) (Fig. 1.7).[44-48] Nevertheless, ELD of Cu still needs further improvements to combine the highest conductivity and the best seamless trench filling compatible with most inter-level dielectric schemes and the process requirements. For example, the use of formaldehyde as a reducing agent is regulated and might be restricted in a few countries. Therefore, alternative scheme using glyoxylic acid was devised.[49] Typical Cu plating bath operates at high pH (>12.5) and deposition temperature near 70℃ which may be a problem to some polymer based low dielectric insulators. Thus, other solutions working at lower pH and lower temperatures are also possible, although, they usually yield Cu with higher specific resistivity.

1.2.3. Direct Cu ELD

Direct Cu ELD is also defined as the deposition of Cu without a Cu seed layer on a heterogeneous substrate such as Ta, Ti, Ir, or Ru by means of ELD. Recently, Ru has received attention as an alternative seed and barrier layer instead of conventional Cu seed and Ta barrier layer, because of its low resistivity and excellent adhesion, as well as its negligible solubility with Cu.[50-52] As the CVD and ALD of Ru are well-developed, the application of Ru seemed promising in the past few years.[53-55] Unfortunately, however, Ru itself was determined not to be suitable as a barrier layer, since Cu could diffuse through columnar Ru grains.[51,56] Therefore, research on the improvement in the barrier layer property of Ru-alloy (e.g. Ru-Al_2O_3, RuCr) or Ru/barrier layer stack (e.g. Ru/Ta, Ru/TiN) are widely conducted nowadays. In addition, study on the feasibility of direct Cu ED on those layers also takes huge interest.[50,55-57]

On the other hand, the deposition of a Cu film on Ru by ELD has not yet received much attention, although ELD is currently one of the promising technologies for metallization. Despite numerous advantages of ELD as mentioned in Chapter 1.2.2, the necessity of the catalyzing process on conventional barrier layers such as Ta or TiN has limited the practical application of ELD in ULSI.[19,58] The catalyzing process signifies the formation of catalytic particles on the substrate, which act as initial nucleation sites for Cu ELD.[33] The catalytic particle generally causes low-density Cu nucleation, disturbing thin film

formation as well as sub-100 nm feature filling.[19,58] However, the catalyzing process is not required in the case of Ru, because the whole Ru surface is catalytic to ELD, and this facilitates the relatively high-density Cu nucleation.[53] Therefore, the thin film formation and sub-100 nm feature filling by ELD are expected to be feasible on Ru surface. Recently, F. Inoue *et al*. reported the Cu seed layer deposition by ELD directly on ALD-Ru for the TSV filling.[53] However, the detailed understanding over the growth phenomena and feature filling by Cu ELD on Ru is still insufficient.

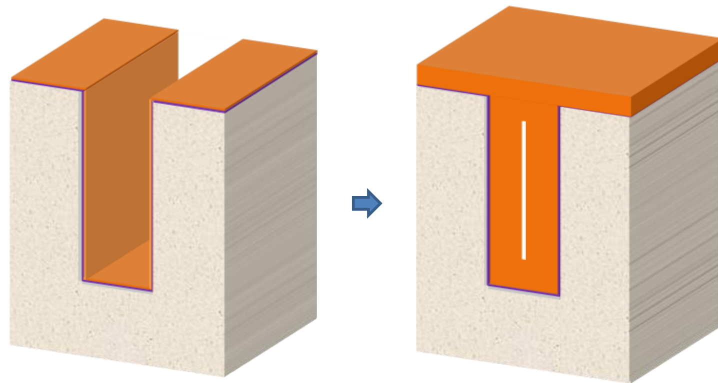


Figure 1.6. Seam formation after conformal ELD in narrow trench.

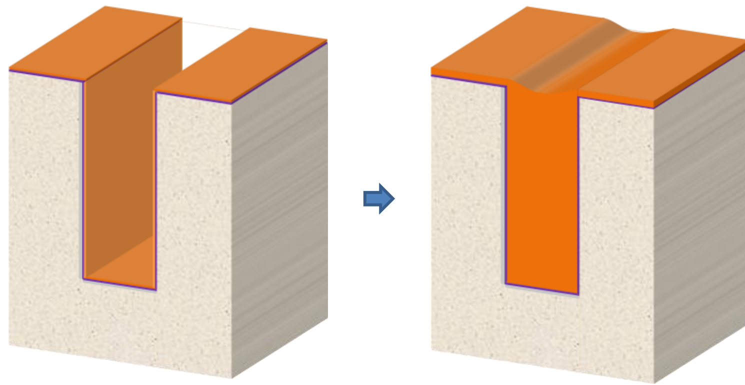


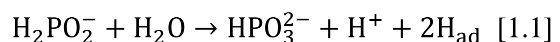
Figure 1.7. Void-free filling of narrow trench by ELD with organic additives.

1.3. All-wet metallization

1.3.1. Electroless Co/Ni alloy as a barrier/capping material

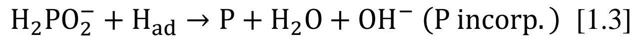
Electroless cobalt (Co) and nickel (Ni) alloys can be excellent barrier and capping materials for Cu and silver (Ag) metallization. Electroless Co and Ni alloys are highly selective, uniform and serve their function even for ultrathin layers (10–20 nm). To deposit electroless Co or Ni films, hypophosphite or di-methyl-amino-borane (DMAB) was used as reducing agents, and as a result of reducing agent oxidation, phosphorous (P) or boron (B) could be incorporated into the deposit. Furthermore, to improve the thermal stability and diffusion properties, refractory metals such as tungsten (W), molybdenum (Mo), or rhenium (Re) can be co-deposited with electroless Co or Ni when water-soluble compounds of refractory metals were introduced into the deposition solutions.[59] For example, W was incorporated into electroless Co film up to 12 at% when tungsten-phosphoric acid was used as a W source in the deposition bath. The incorporation reaction pathways for each constituent are described elsewhere, and for example, the preparation of CoWP or NiWP film in acidic or basic conditions are like below[60,61];

Acidic electrolyte with hypophosphite reducing agent

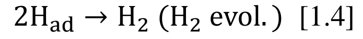


$$H_2PO_2^- + H_2O \rightarrow HPO_3^{2-} + H^+ + 2H_{ad} \quad [1.1]$$

$$Ni^{2+} \text{ or } Co^{2+} + 2H_{ad} \rightarrow Ni \text{ or } Co + 2H^{+} \text{ (Ni or Co dep.)} \quad [1.2]$$

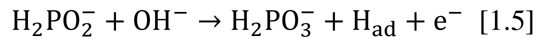


$$H_2PO_2^- + H_{ad} \rightarrow P + H_2O + OH^- \text{ (P incorp.)} \quad [1.3]$$



$$2H_{ad} \rightarrow H_2 \text{ (} H_2 \text{ evol.)} \quad [1.4]$$

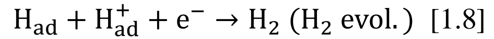
Basic electrolyte with hypophosphite reducing agent



$$H_2PO_2^- + OH^- \rightarrow H_2PO_3^- + H_{ad} + e^- \quad [1.5]$$

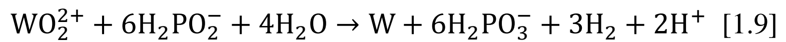
$$Ni^{2+} \text{ or } Co^{2+} + 2e^- \rightarrow Ni \text{ or } Co \text{ (Ni or Co dep.)} \quad [1.6]$$

$$H_2PO_2^- + e^- \rightarrow P + 2OH^- \text{ (P incorp.)} \quad [1.7]$$



$$H_{ad} + H_{ad}^{+} + e^- \rightarrow H_2 \text{ (} H_2 \text{ evol.)} \quad [1.8]$$

W co-deposition



$$WO_2^{2+} + 6H_2PO_2^- + 4H_2O \rightarrow W + 6H_2PO_3^- + 3H_2 + 2H^+ \quad [1.9]$$

Various studies have reported the effect of the concentration of ELD bath constituents on the P and W incorporation amount in CoWP or NiWP films. The results of investigation using several CoWP or NiWP baths are depicted in Fig. 1.8 and 1.9.[62-71] It could be seen from the figures that co-deposition of W clearly influenced on the P content of the deposits: in general, the incorporation of P into the film was impeded by the co-deposition of W, probably due to a competitive consumption of hypophosphite for the incorporation of P and W (reaction [1.3] and [1.7] vs. [1.9]).

Electroless barriers for on-chip metallization are characterized by the following microstructure effects: (a) the so-called "solute effect", P (or B) and W (or Mo, Re) impurities create a "stuffed" boundary, blocking possible Cu diffusion through the grain boundaries; (b) ε-cobalt grains embedded in an amorphous matrix, thus avoiding the high diffusivity paths of the grain boundaries in regular polycrystalline materials.[59] For instance, selectively deposited electroless Ni–P and Co–P, Ni–Co–P films were investigated as the barrier/cladding materials for Cu metallization.[72,73] The former electroless barriers for Cu were effective up to a temperature of 400℃. The introduction of a third alloying element, especially refractory metal, e.g. W, Mo, or Re, improves barrier efficiency. NiB, NiReP and NiWP show ability to serve as a barrier and cladding layers without significant diffusion of Cu into the barrier and no Cu line resistance increases at temperatures up to 400–500℃. Electroless CoWP thin films showed an ability to function as effective barriers/cladding layers for Cu metallization at temperatures up to 550℃.[74] Electroless barrier layers can be formed on PVD or CVD deposited Co (or Ni) seed layers as well as directly on dielectric layers (such as SiO_2). Self-assembled monolayer (SAM) of silane-based compounds followed by treatment in a Pd containing activator was utilized as the adhesion promoter/catalytic layer.

SiN or SiC layer is typically used as the etch stop and passivation layer for Cu. SiN/Cu or SiC/Cu interface is a major electromigration-voiding site. Selective metal capping with electroless metals was proposed as one of the ultimate solutions to this problem.[72-76]

Electroless metal capping/barrier layers such as CoWBP, CoWP, NiMoP also provide barrier properties against Cu and oxygen diffusion so that lower effective interconnect capacitance can be obtained with thinner or even without SiN (SiC) layers which have high-k.[77-79] It was also demonstrated that both the contact resistance and the leakage that could be lower for a stand-alone electroless metal cap compared to a stand-alone SiN cap, presumably due to the damage associated with the SiN deposition. The electromigration median-time-to-failure (EM MTTF) of damascene Cu interconnects with Co capping layer is about ten-times better than that of Cu metallization with Si(C)N dielectric capping layer. The distribution of the EM failures is also tighter on Co capping wafers (Fig. 1.10).[59] The increase of the EM resistance with an electroless capping layer can be explained by the complete passivation of the top interface as fastest diffusion path resulting in increased adhesion and interfacial bonding strength (i.e. metal/metal > metal/Si > metal/oxygen bonding).

Selective electroless Ni process was demonstrated to fill the contact holes to Si while providing low contact resistance and planar surface.[80,81] Selective electroless Co and Ni deposition into through silicon vias (TSV) for 3D interconnects has been also achieved through the mechanical removal of catalysts from the front surface of the wafers or the use of photosensitive TiO_2/catalyst process.[59] It enables selective TSV filling that eliminates the needs for PVD barrier/seed layer and CMP that significantly reduces the 3D packaging cost.

1.3.2. All-wet metallization

As referred in Chapter 1.1, owing to some critical failures of Cu metallization, especially designed barrier and capping layers are used to overcome those difficulties. Since Cu may diffuse via those layers or even react with them causing another kind of failure, the most popular barriers are TaN, TiN, or Ta/TaN bilayer.[82] Alternative barriers are ternary compounds of transition metal films that provide a good Cu diffusion barrier due to its nano-crystalline or amorphous structure, such as Ti–Al–N, Ta–Al–N which have been developed using a reactive PVD or CVD.[83] It is reported that CVD is preferable for fabricating barrier layer, because disadvantageous characteristics of PVD such as poor step coverage have set critical limits on silicon device applications by increasing the aspect ratio of the trenches.

Following those reports, it is evident that the application of ELD has superior advantage due to its simplicity and by having a better step coverage on complex shape substrate. The electroless NiB, CoB, NiW-X or CoW-X (X = P, B), CoSnB films have outstanding thermal stability as a capping layer or barrier layer.[76,84-88] Moreover, the insertion of a SAM, which had been investigated as diffusion barrier, to the formation of these layers is effective to produce conformal and thin film.[89-93]

An interesting approach was integrating all the various wet processes together onto a unified process; a so-called "all-wet" process as described in Fig. 1.11. The proposed

all-wet metallization process includes barrier layer ELD, seed layer formation, and Cu ED. To form a barrier layer by ELD on a dielectric substrate such as SiO_2, most studies have created a SAM prior to ELD in order to immobilize the catalytic particles.[90,94,95] Generally, the use of a SAM improves catalytic nanoparticle coverage as well as adhesion between the electroless deposited film and the substrate, because the alkoxy group in the silane radical makes a strong bond with the SiO_2 surface and the amino or thiol group of the reverse position traps the catalysts. Electroless Co or Ni alloy films are uniformly deposited on the SiO_2 substrate by using 3-aminopropyltriethoxysilane (APTES) as the organosilane molecule.[90,94,95]

A Cu seed layer formation step is essential before undertaking Cu ED on electroless barrier layers, because the conductivity of electroless deposited Co or Ni alloy layers are low. Usually, Cu seed layer formation on an electroless deposited barrier layer is conducted by using Cu ELD and/or by means of a displacement reaction between Cu ions and the barrier material. Subsequently, Cu ED is performed on the seed layer, thus realizing an all-wet metallization process.[90,96] However, Cu seed layer formation through a displacement reaction can lower device reliability by inducing surface damage and pitting on the barrier layer. Therefore, the development of a method for direct Cu ED is highly pursued on electroless deposited Co or Ni alloy barrier layers. It is as well expected that the elimination of the seed layer formation step would enhance the productivity of the device.

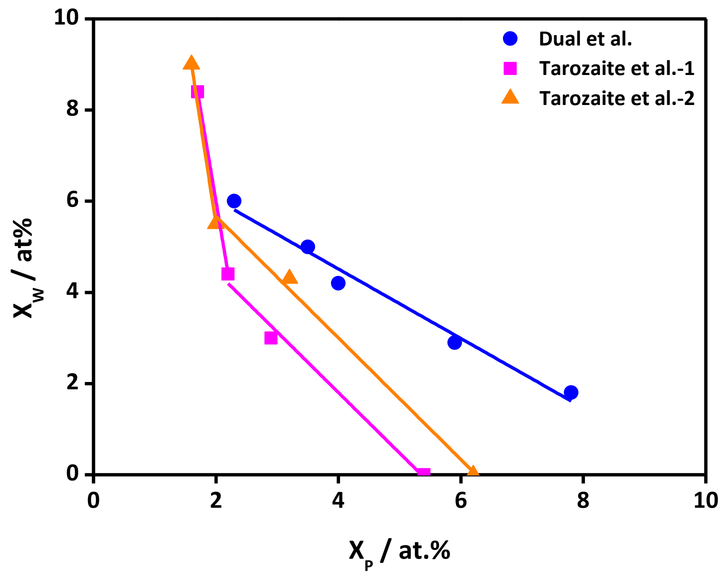


Figure 1.8. W versus P atomic content for ELD-CoWP (edited from ref. [62,63]).

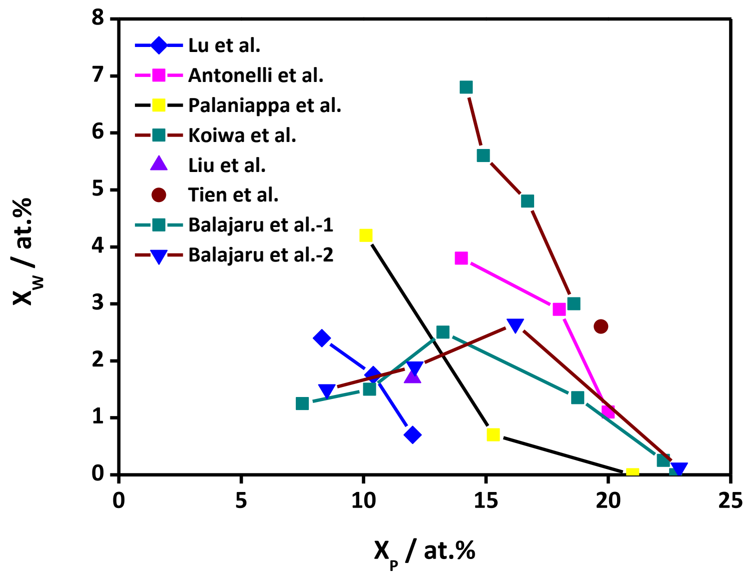


Figure 1.9. W versus P atomic content for ELD-NiWP (edited from ref. [64-71]).

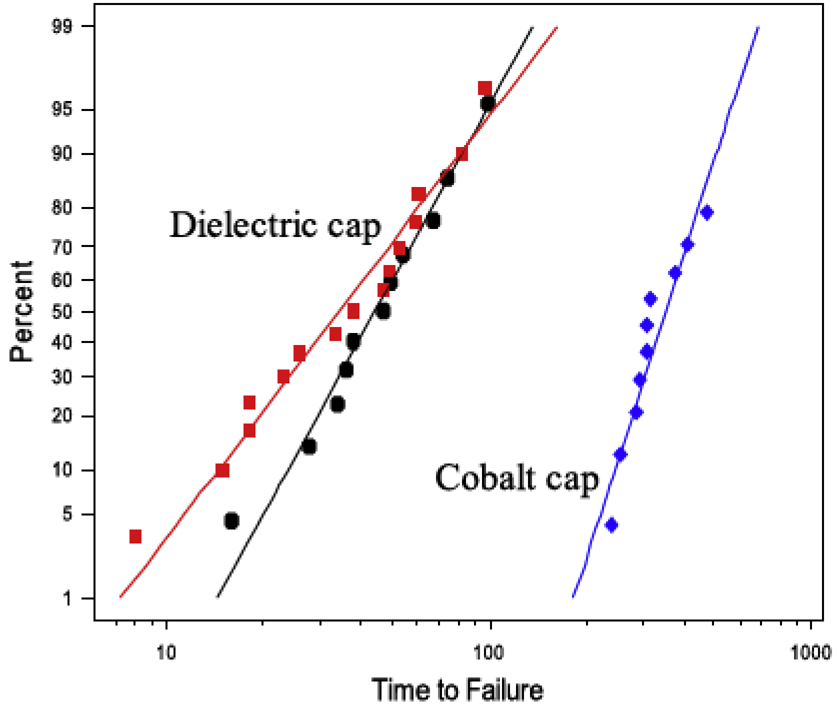


Figure 1.10. Damascene Cu interconnect EM data comparing undoped Cu with Co alloy capping layer to Si(C)N dielectric capping layer (edited from ref. [59]).

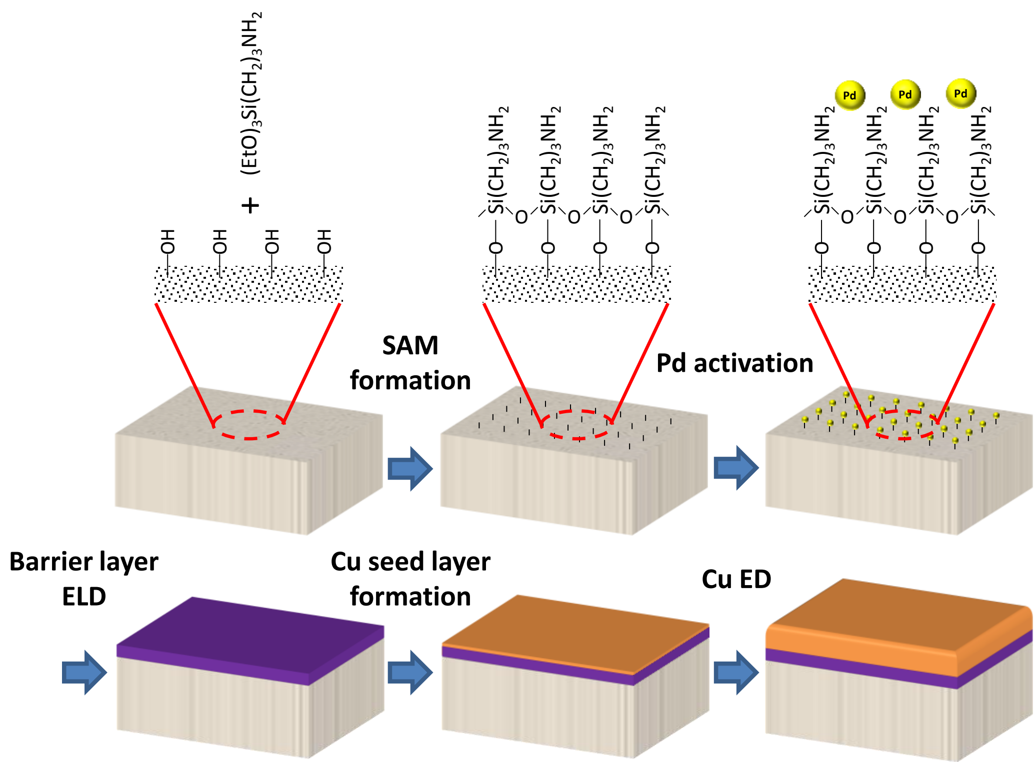


Figure 1.11. Schematic diagram of the “all-wet” metallization process.

1.4. Concepts of the study

In this study, the entire metallization processes were modified for the next-generation interconnect fabrication. On Ta barrier layer, a feasible direct Cu ED was investigated, in an effort to realize sub-100 nm gap-filling by direct Cu ED. Well-defined Pd nanoparticles (NPs) were introduced on a Ta substrate to promote the nucleation of Cu on a highly resistive substrate. Pd NPs ~3 nm in size and the addition of allyl alcohol in the ED bath facilitated the preparation of a uniform Cu seed layer on a blanket Ta substrate. The seed layer formation method was also successfully applied to a 55 nm patterned Ta substrate. After the deposition of the seed layer, gap-filling of the trenches was accomplished.

A method for direct Cu ED on an electroless deposited Co or Ni alloy barrier layer was investigated for all-wet Cu interconnect fabrication. To achieve practicable direct Cu ED, we modified the entire all-wet metallization process. A reduction in electroless deposited Co or Ni alloy films' resistivity was achieved by controlling the activation process and the composition of the ELD bath. To obtain a uniform, smooth Cu film, barrier layer oxide was removed through a coulometric reduction method (CRM) followed by a two-step potentiostatic Cu ED process, leading to a successful bottom-up Cu filling.

On Ru substrate, which is considered as next-generation barrier/seed material, Cu growth phenomena were investigated during direct Cu ELD. Major obstacle that

interferes with the understanding of growth phenomena during ELD is the existence of induction period, which is occasionally reported in ELD when it is conducted in a formaldehyde or a glyoxylic acid based solutions.[34,53,97] Generally, induction period in ELD is originated from the poor catalytic activity of substrate to ELD or from the complex surface reaction such as adsorption of reagents, substrate oxide formation as well as removal.[53,97] Therefore, Cu ELD bath that did not exhibit the induction period on Ru substrate was introduced in this study. By using the solution, the Cu nucleation and film growth on Ru was investigated at the early stage of the ELD. In addition, the feasibility of Cu ELD on Ru, as a practical metallization process, was examined by a gap-filling experiment.

CHAPTER II. Experimental

2.1. Direct ED of Cu on Ta

2.1.1. Preparation of Pd NPs

Pd NPs were synthesized using a microwave-assisted polyol method.[98-100] A solution containing 0.003 M K_2PdCl_6, 0.01 M polyvinylpyrrolidone (PVP, Mw = 40,000 g mol^{-1}), 0.001 M cetyltrimethylammonium bromide (CTAB), and 10 M ethylene glycol (EG) was prepared for the Pd NPs synthesis. The solution was heated in a microwave for 80 s to induce the reduction of Pd ions. After heating, the solution was dispersed in acetone and the centrifugation was conducted at 10000 rpm for 20 min to separate the Pd NPs from the solution. The separated Pd NPs were washed by n-hexane and ethyl alcohol to remove the residual PVP and EG, and then dispersed in ethyl alcohol to make the 0.18 wt% Pd NPs dispersion. The zeta-potential of the synthesized Pd NPs was measured to −53 (±1.9) mV, and this attributed to the excellent dispersing property of the Pd NPs in ethyl alcohol.

2.1.2. Direct ED of Cu on Ta

Fig. 2.1 illustrates a schematic diagram of the direct Cu ED process assisted by the Pd NPs. A blanket or 55 nm patterned SiO_2/Si substrate covered with a Ta barrier layer (7 nm, PVD) was used as the substrate. The substrate was cut to $1.5 \times 1.5\ cm^2$, and the native Ta oxide was removed by immersing the specimen in a solution containing 0.6 M HF and 0.3 M HNO_3 for 10 min (blanket) or 3 min (pattern, the adjustment in the immersion time was inevitable because of a vulnerable Ta barrier layer at the sidewall of the pattern).[101] The process not only removes the native oxide but also improves the hydrophilicity of the Ta surface. After the Ta oxide removal process and a subsequent rinsing step, the Pd NPs were loaded onto substrate by coating 0.1 mL of the dispersion, and dried on hot plate for 15 min at 80℃ to evaporate the ethyl alcohol.

The electrolyte for the deposition of the Cu seed layer consisted of 0.3 M $Cu_2P_2O_7$ and 1.0 M $K_4P_2O_7$ (Cu-Pyro bath).[31,102] The Cu seed layer was formed onto the Pd NPs-loaded Ta substrate by direct Cu ED via two steps: a nucleation step and a film formation step. The deposition potential and charge amount in each case were fixed to −1.5 V (vs. saturated calomel electrode; SCE) and 6 mC cm^{-2}. After the deposition of the seed layer, annealing was conducted at 100℃ for 30 min in a N_2 atmosphere to improve the adhesion of the seed layer.

The electrolyte for additional Cu deposition was comprised of 0.25 M $CuSO_4$ and 1 M

H_2SO_4 (Cu-Sul bath). 88 μM PEG (Mw = 3400 g mol^{-1}), 1 mM NaCl, and 50 μM SPS were added as additives for the trench filling.[103-106] Prior to the gap-filling, the Cu native oxide on the Cu seed layer was removed by dipping the specimen into a solution containing 0.02 M citric acid and 0.03 M KOH for 30 s.[107]

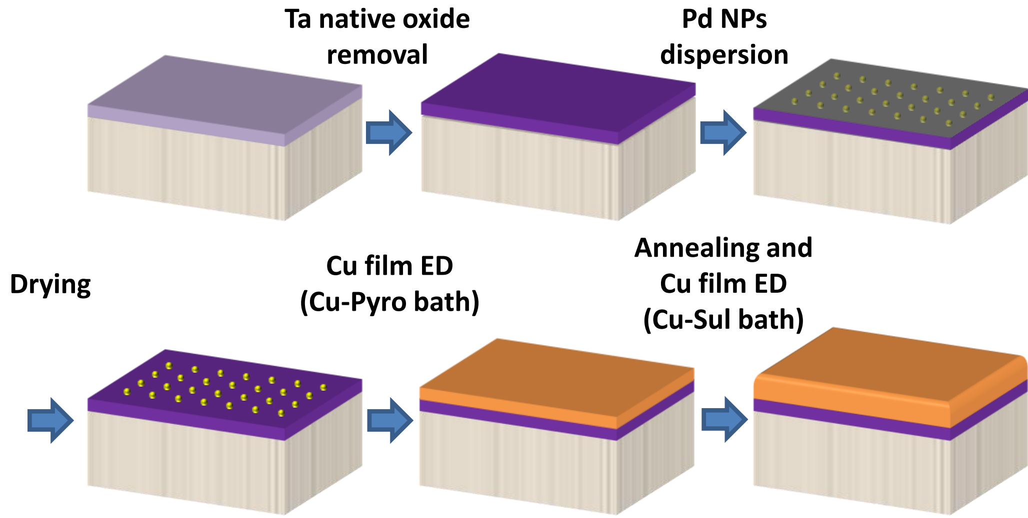


Figure 2.1. Schematic diagram of the direct Cu ED process on Ta assisted by the Pd NPs.

2.2. Direct ED of Cu on Co/Ni alloy

The experimental scheme of direct Cu ED on Co/Ni alloy layer prepared by ELD on SiO_2 dielectric is similar with that depicted in Fig. 1.11 of all-wet metallization. However, the Cu seed layer formation step was omitted by the modification of the entire all-wet metallization process.

2.2.1. Pretreatment of substrate and SAM-Pd activation

Blanket or patterned, 1.5×1.5 cm^2 SiO_2/Si substrate samples were etched with 0.6 M HF solution for 5 s to remove air-born oxide and contaminants.[108,109] After rinsing the etched samples with deionized water, an APTES-SAM was formed on the substrate by immersion in a toluene solution containing 1 wt% APTES for 10 min at 60℃.[94] The SAM-bearing substrate was then dipped in a Pd NPs dispersion for 3 min to induce the adsorption of Pd NPs. The dispersion contained 3 nm average diameter Pd NPs which were synthesized by a polyol method as described in Chapter 2.1.1. Dispersion concentration was adjusted to 0.01 wt% by dilution with ethyl alcohol.

2.2.2. ELD of Co/Ni alloy films and direct Cu ED

After SAM-Pd activation of the samples, ELD of Co or Ni alloy films was performed on the samples. The composition of each ELD bath is presented in Table 2.1. Whereas the pH of Ni alloy ELD bath was set as 5, that of Co alloy ELD bath was adjusted to 10 due to low deposition kinetic of Co ELD in acidic environment.

Before direct Cu ED on electroless Co or Ni alloy layers, the native oxide of the alloy layer was removed by a coulometric reduction process in a 0.01 M H_2SO_4 solution along with 100 μA cm^{-2} of cathodic current for 100 s. The electrolyte for Cu ED contained 0.25 M $CuSO_4$ and 1.00 M H_2SO_4. Conventional additives for bottom-up filling [88 μM PEG (Mw = 3400 g mol^{-1}), 1 mM NaCl, and 50 μM SPS] were added to the electrolyte during trench filling.[103-106]

Table 2.1. Composition of ELD Bath for the Deposition of NiWP / CoWP / NiCoP

	NiWP	**CoWP**	**NiCoP**
citrate	0.08 M	0.07 – 0.4 M	0.07 M
CH_3COO^-	0.06 M	–	–
H_3BO_3	–	1 M	1 M
$NiSO_4$	0.075 M	–	0.03 – 0.01 M
$CoSO_4$	–	0.04 M	0.01 – 0.03 M
Na_2WO_4	0.02 M	0.03 M	–
additive	0 - 5 ppm PEG	1.15 mM ATRA	1.15 mM ATRA
NaH_2PO_2	0.25 M	0.05 – 0.3 M	0.05 M
pH	5	10	10
temp.	90°C	90°C	90°C

2.3. Direct ELD of Cu on Ru

2.3.1. Pretreatment of Ru and direct Cu ELD

The experimental scheme of direct Cu ELD on Ru covered specimen is illustrated in Fig. 2.2. Cu ELD was performed on a 1.5×1.5 cm^2 coupon Si wafer covered with ALD-Ru (30 nm on blanket and 7 nm on patterned substrate). Prior to ELD, all substrates were immersed in 0.6 M HF solution for 3 min to remove the native oxide layer on the surface.[52] Subsequent to pretreatment, each substrate was dipped into the Cu ELD solution consisting of 4 mM $CuSO_4$, 8 mM ethylenediaminetetraacetic acid (EDTA), and 12 mM p-HCHO (para-formaldehyde) or NH_2NH_2. The solution pH was adjusted by KOH to 12.8, and the temperature was maintained at 70°C using a thermostat.

The effect of HF application on Ru substrate was examined by coulometric reduction method (CRM). The CRM was conducted in 0.01 M H_2SO_4 electrolyte with the cathodic current density of 100 μA cm^{-2}.[110] In addition, the formation and the deposition amount of Cu films were determined by linear sweep voltammetry (LSV) which was conducted in a 0.05 M tetramethylammonium hydroxide (TMAH) containing solution.

2.3.2. Preparation of Ru electrode and EQCM monitoring

To investigate the surface state and mass change during Cu ELD, electrochemical quartz crystal microbalance (EQCM) monitoring was introduced. A Ru electrode was prepared by Ru displacement reaction on the Cu-coated AT-cut crystal QCM electrode (QA-A9M-Cu(M), mirror finish, Seiko EG&G model, A = 0.196 cm^2). The displacement of Cu to Ru was performed in a solution consisting of 0.5 mM $RuCl_3$ and 0.1 M $HClO_4$, for 30 s at 70°C. Before the displacement, native Cu oxide was removed by cathodic polarization in 0.1 M H_2SO_4 solution at 5 mA cm^{-2} for 5 min.[97] The prepared Ru electrode was dipped into the Cu ELD solution after the oxide removal.

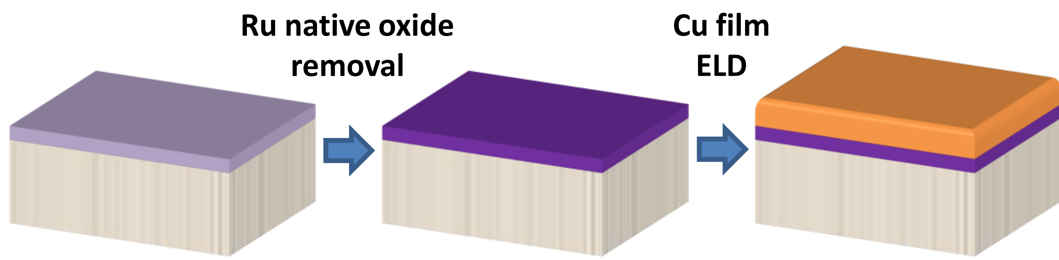


Figure 2.2. Schematic illustration of direct Cu ELD process on Ru substrate.

2.4. Instrumentation

Solutions were agitated during mixing and temperature adjustment. However, solutions were quiescent during the pretreatment, activation, and deposition steps. In all electrochemical experiments, including LSV, CRM, and ED, specimen was loaded onto a laboratory-made electrochemical cell that exposed 1 cm^2 of the sample surface. SCE and platinum (Pt) wire were used as reference and counter electrodes, respectively. A potentiostat (PAR 2273, EG&G) was used for the ED process and the electrochemical analysis. On the other hand, the potential and mass change during the EQCM observation were simultaneously recorded by potentiostat (263A, EG&G) and QCM (QCA917, EG&G).

A field emission scanning electron microscope (FESEM; S-4800, Hitachi), a transmission electron microscope (TEM; JEM-2100F, JEOL), and an atomic force microscope (AFM; 5100 AFM, Agilent Technologies) were utilized for the microscopic observations. A focused ion beam (FIB; Quanta 3D FEG, FEI) was used to prepare the specimen for the TEM analysis. In addition, an X-ray photoelectron spectroscope (XPS; AXIS-His, Kratos) and an Auger electron spectroscopy (AES; PHI 670, Perkin-Elmer) were used for the spectroscopic analyses.

Sheet resistance (R_S) of the specimen was measured by using a 4-point probe (CMT-SP 2000N, Advanced Instrument Technology). Film resistivity was calculated based on the

film thickness and R_S, assuming that major path for current flow is along the film surface. An X-ray diffractometer (XRD; D8-Advance, Bruker Miller) was used to characterize film crystallinity.

Film adhesion of the specimen was assessed by the tape test method proposed in ASTM D3359.[111] For testing per ASTM D3359, the specimen surface was divided into 2×2 mm^2 squares by using sharp cutting tool. The area of the film that detached after tape removal was used to calculate the percentage of area removed (PAR) value (Fig. 2.3).

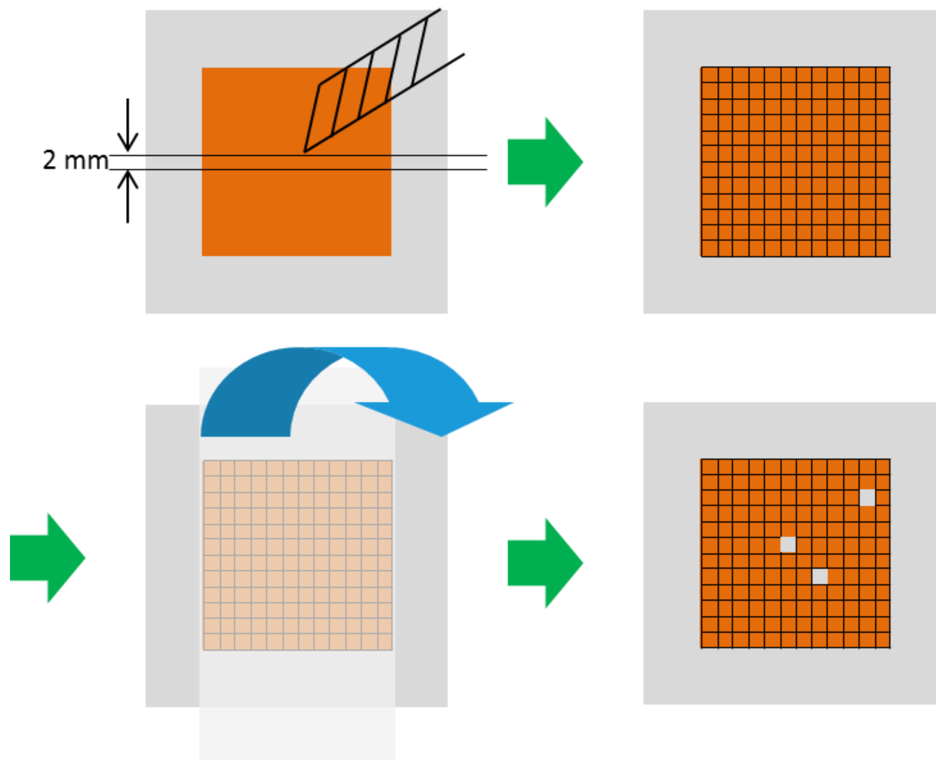


Figure 2.3. Schematic illustration of method for film adhesion test referring to ASTM D3359.[111]

CHAPTER III. Direct ED of Cu on Ta

3.1. Seed layer formation by direct Cu ED on blanket Ta substrate

3.1.1. Pd NPs loading on blanket Ta substrate

The synthesized Pd NPs that would act as a promoter for Cu nucleation were analyzed by TEM. The TEM observation was conducted after sampling and drying the Pd NPs dispersion on TEM grid (Formvar Grid 100mesh, Cu). As shown in Fig. 3.1a and b, the synthesized Pd NPs had a uniform size distribution with average size of 3.0 (±0.4) nm.

The amount of Pd NPs loaded on the substrate following the method described in Chapter 2.1.2 was measured by QCM by coating the QCM electrode with Pd NPs dispersion. The frequency change according to the drying time was measured, and the mass change was calculated based on it. As depicted in Fig. 3.2a, initial fluctuation of the mass change was observed after the Pd NPs loading (50 s) and abrupt decrease of the mass occurred after the complete evaporation of ethyl alcohol (430 s). By the calculation, the fixing amount of Pd NPs was determined to 1.8 μg cm^{-2}. Moreover, distinct Pd-related peaks were identified by XPS analysis after the Pd NPs loading onto Ta substrate. As can be seen in Fig. 3.2b, there existed peaks related to Pd and PdO (The PdO seemed

to be formed during the drying process by the oxidation of Pd).

The distribution of Pd NPs on Ta substrate after loading was evaluated by comparing the surface morphology measured by AFM. As depicted in Fig. 3.3a and b, the surface morphology was rarely changed except the slight increase in the surface roughness, indicating that no severe aggregation of Pd NPs occurred on the surface. Therefore, it could be expected that the Pd NPs were quite uniformly distributed over the Ta substrate after loading. The improved hydrophilicity of Ta surface after pretreatment seemed to facilitate the uniform wetting of the Pd NPs dispersion during the coating process.

3.1.2. Cu seed layer formation by direct Cu ED on Pd NPs-loaded Ta substrate

After removing the ethyl alcohol by drying, the deposition of the Cu seed layer on the highly resistive Ta barrier was performed using a basic Cu-Pryo bath. Generally, the use of basic electrolyte gives higher nucleation density on highly resistive substrate during the ED, which facilitates the formation of the continuous Cu seed layer.[112-114] As already be mentioned in Chapter 2.1.2, The Cu seed layer formation step was composed of two potentiostatic ED steps; a nucleation step and a film formation step. After performing the ED process, Cu film was exclusively formed on Pd NPs-loaded Ta as shown in Fig. 3.4. It was presumed that, during the nucleation step, the Cu nuclei were primarily developed on the loaded Pd NPs because the Pd NPs promoted the electron transfer. During the film

formation step, Cu film formation was completed via the coalescence between the Cu nuclei. Consequently, 18 (±4.8) nm of Cu film was deposited on the Ta substrate, as depicted in Fig. 3.4b.

However, the seed layer showed an irregular thickness with a root mean square roughness (R_{rms}) value of 10.7 nm, as shown in Fig. 3.4d. The non-uniform thickness distribution should be originated from the preferential growth of the deposited Cu during the film formation step. Cu nuclei which developed on Pd NPs during the nucleation step would prompt the Cu ion reduction even more than Ta or Pd NPs. Cu film deposition with a rough surface morphology would not be avoidable in the event of non-uniform growth.

In order to solve the surface roughness problem, allyl alcohol, which has been applied as a leveler during the deposition of a Cu-Zn alloy in a pyrophosphate-based electrolyte, was adopted.[102] Despite the lack of information, it was reported by Senna *et al.* that allyl alcohol suppressed the Cu deposition by forming a stable complex with Cu ion, and improved the surface uniformity during the Cu-Zn alloy deposition process. Similarly in this study, the addition of allyl alcohol clearly suppressed the kinetics of Cu deposition as depicted in Fig. 3.5a. Consequently, the uniformity of the Cu seed layer was significantly improved by the addition of 0.035 M allyl alcohol into the Cu-Pyro bath (Fig. 3.5b and c). Owing to the brightening effect of the allyl alcohol, the thickness of the Cu seed layer decreased to 12 (±1.2) nm and the R_{rms} value was reduced to 2.5 nm.

The adhesion of the Cu seed layer was tested via the tape test method. The adhesion of the Cu seed layer was markedly affected by the thermal treatment at 100℃ for 30 min in a N_2 atmosphere, decreasing PAR value from 19.4% to 6.7%. The improvement also had a positive influence on the subsequent Cu ED. Without the thermal treatment, peeling-off of Cu deposit was observed when a 100 nm thick Cu film was electrodeposited on the seed layer. On the other hand, the film remained intact on the thermally-treated Cu seed layer showing the PAR value of 12.5%. Therefore, the thermal treatment was performed after the seed layer formation in all cases.

Subsequent to the seed layer formation, LSV in a Cu-Sul bath was conducted on the seed layer. As depicted in Fig. 3.6, the Cu deposit formed on the blanket Ta gave the lowest current density, and the on-set potential for the Cu reduction ($\eta_{red, Cu}$) was −0.5 V (vs. SCE). This occurred because the Cu film was not completely formed on the bare Ta substrate. In contrast, $\eta_{red, Cu}$ was positively shifted to 0.0 V (vs. SCE) on the Cu seed layers deposited on the Pd NPs-loaded Ta substrates. At the same time, the current density was high on the Cu seed layers in all of the potential ranges investigated. Despite the similar $\eta_{red, Cu}$ value, a higher current density was observed on the Cu seed layer deposited without allyl alcohol compared to that deposited with 0.035 M allyl alcohol, as expected given that ally alcohol reduced the surface roughness.

In addition, the effect of the additives, an accelerator and a suppressor, all of which are essential for trench filling in a Cu-Sul bath, was tested on a Cu seed layer by LSV. A seed

layer deposited on the Pd NPs-loaded Ta with 0.035 M allyl alcohol was used to test the additive effect. In Fig. 3.7, the additives worked well on the seed layer, as on a conventional Cu electrode.[104-106] That is, a combination of PEG and Cl^- suppressed the reduction of the Cu ions, and the addition of the SPS accelerated the Cu ion reduction on the seed layer, as usual.

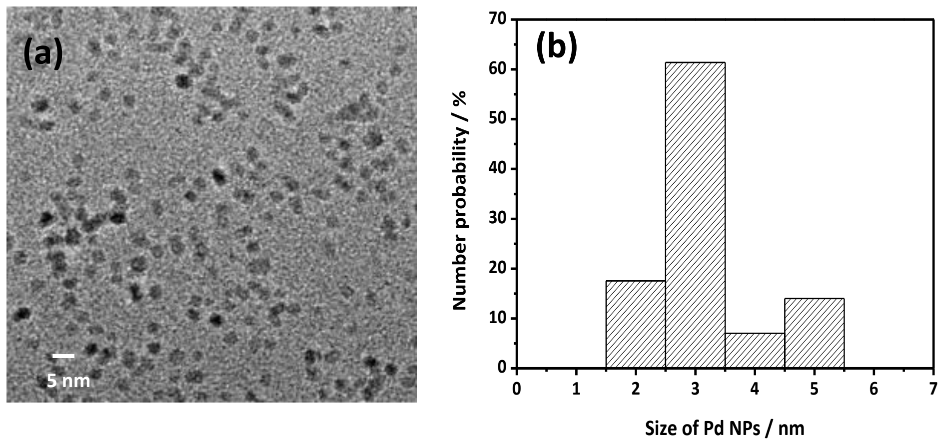


Figure 3.1. (a) TEM image of synthesized Pd NPs on TEM grid and (b) number probability of Pd NPs according to the particle size.

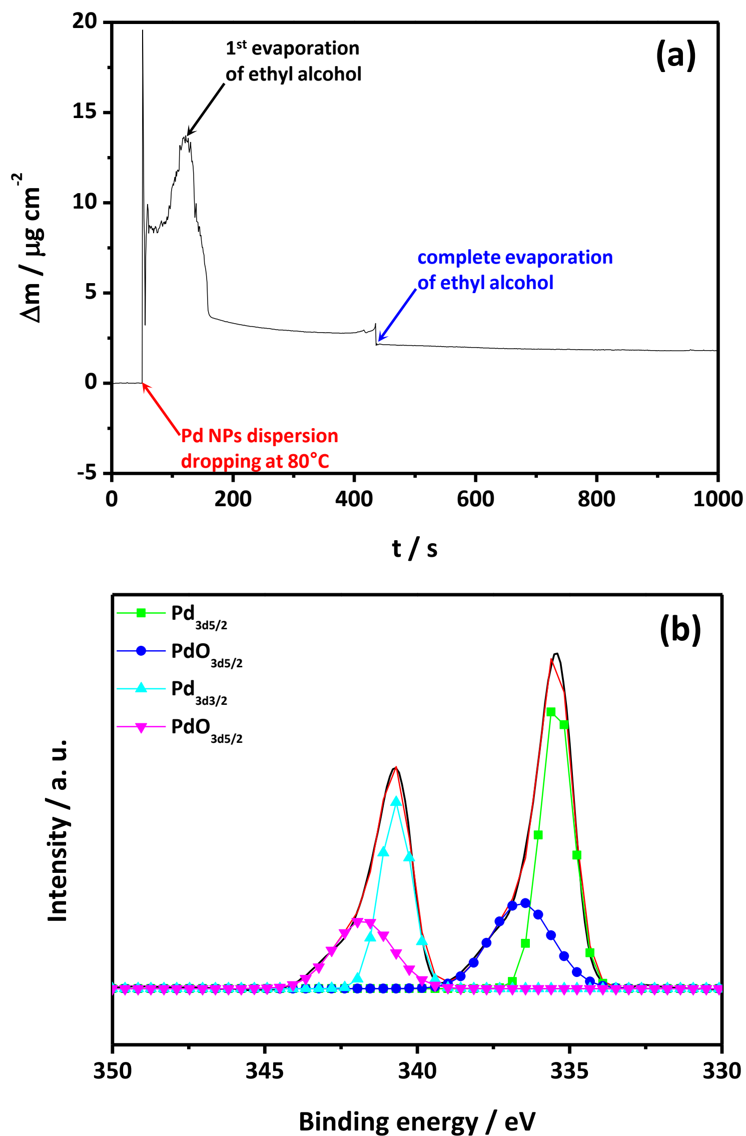


Figure 3.2. (a) The mass change during the Pd NPs coating process on QCM electrode and (b) XPS analysis of the Ta substrate after Pd NPs loading.

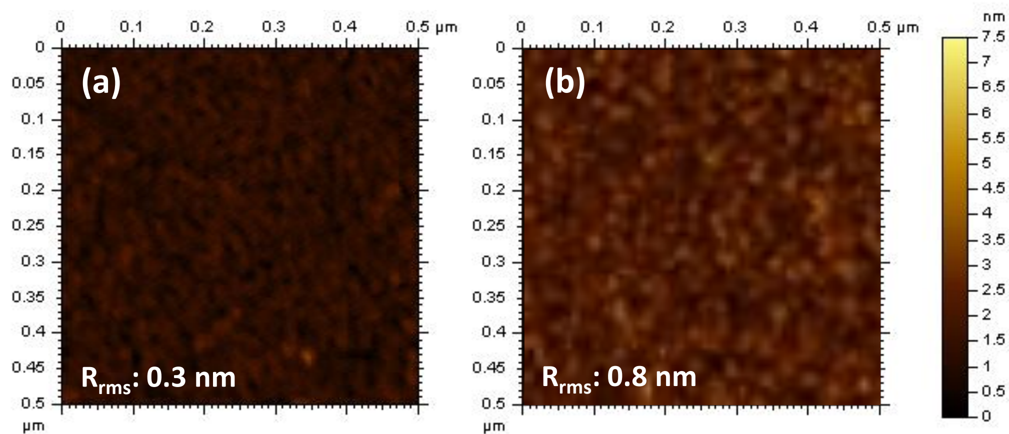


Figure 3.3. The AFM surface morphology of Ta substrate (a) before and (b) after the Pd NPs loading.

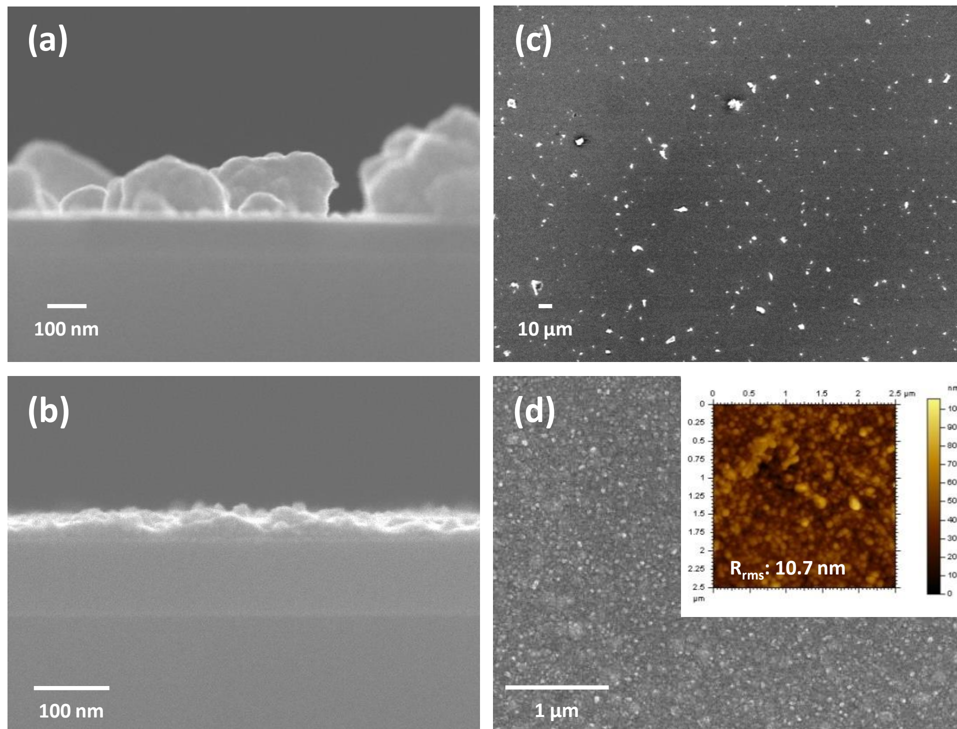
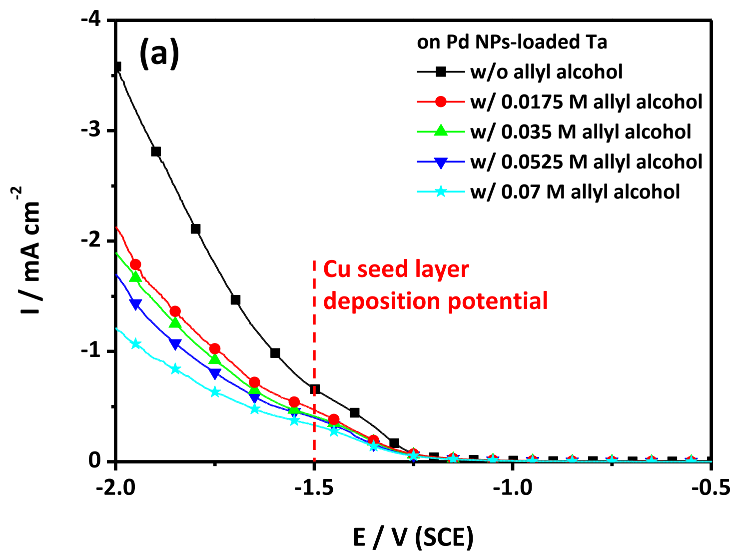


Figure 3.4. FESEM images of Cu deposited on (a, c) blanket Ta and (b, d) Pd NPs-loaded Ta substrates. Inset in (d): AFM image of the specimen.



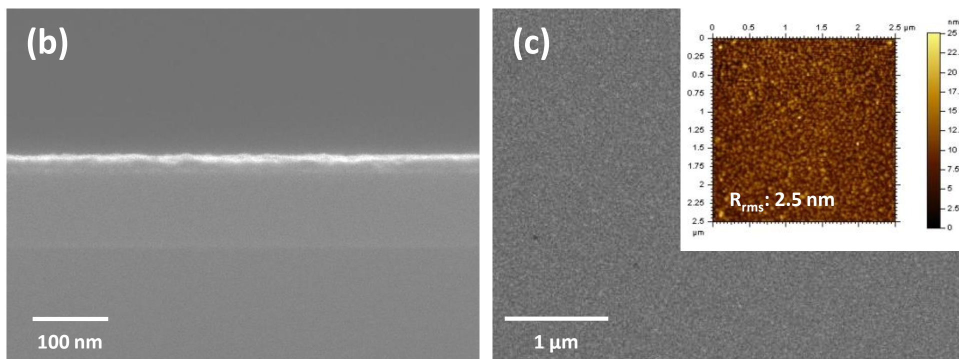


Figure 3.5. (a) LSV on Pd NPs-loaded Ta substrate with the addition of allyl alcohol to the Cu-Pyro bath (scan rate = 10 mV s^{-1}). (b, c) FESEM images of Cu film deposited on Pd NPs-loaded Ta substrate with 0.035 M allyl alcohol. Insets in (c): AFM image of the specimen.

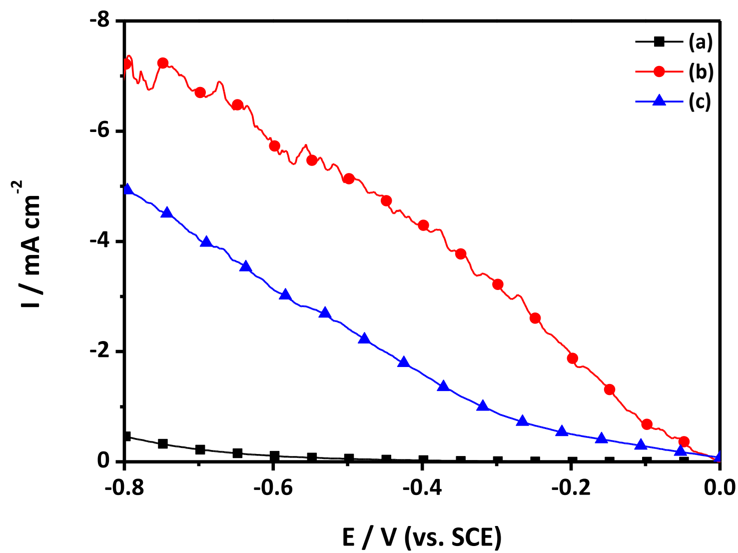


Figure 3.6. LSV on Cu deposited on (a) the blanket Ta, (b) the Pd NPs-loaded Ta without allyl alcohol, and (c) the Pd NPs-loaded Ta with 0.035M allyl alcohol. LSV experiments were conducted in Cu-Sul bath (scan rate = 10 mV s^{-1}).

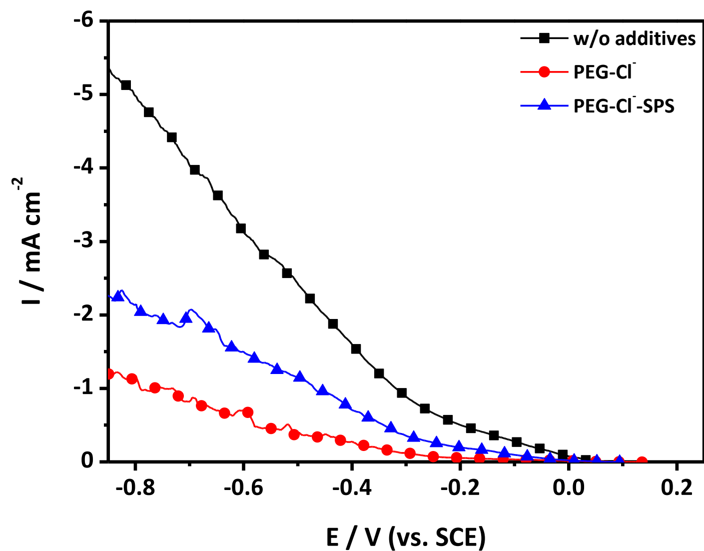


Figure 3.7. LSV on a Cu seed layer prepared on the Pd NPs-loaded Ta by direct ED in Cu-Pyro bath containing 0.035 M allyl alcohol. LSV experiment was conducted in Cu-Sul bath (scan rate = 10 mV s^{-1}) and the concentration of each additive is specified in the Chapter 2.1.2.

3.2. Trench filling by direct Cu ED on patterned Ta substrate

Direct Cu ED was also applied to a 55 nm patterned Ta substrate to form a seed layer and to fill the trench. Fig. 3.8a and d present the 55 nm patterned substrate covered with 7 nm of a Ta barrier layer. As was expected, only irregular Cu islands were observed on the rib of the trench after the seed layer formation steps when Pd NPs were not loaded (Fig. 3.8b and e). In contrast, a Cu seed layer was deposited on the bottom, side, and top of the trench of the Pd NPs-loaded Ta substrate, as depicted in Fig. 3.8c and f, although the uniformity of the seed layer was poor. Therefore, allyl alcohol was used again during the seed layer formation process on the trench.

The effect of the allyl alcohol content on the uniformity of the seed layer was investigated by FESEM images, as depicted in Fig. 3.9. These images show that the uniformity of the seed layer was gradually improved with increase in the concentration of allyl alcohol. To compare the seed layer uniformity quantitatively, the trench opening after the formation of the seed layer was measured, as shown in Fig. 3.10a. Finally, when 0.07 M of allyl alcohol was added, the width of the trench opening approached to that of a Ta substrate, which was sufficient to be applied for the trench filling step. Based on the TEM image in Fig. 3.10b, the thickness of the seed layer was measured as 5.1 (±0.3, bottom) nm, 4.3 (±0.3, side) nm, and 5.5 (±0.6, top) nm, indicating the formation of a conformal seed layer.

The brightening effect was not observed on the patterned substrate with 0.035 M allyl alcohol, which was sufficient concentration on the blanket substrate. It indicated that the surface concentration of allyl alcohol would change with the surface area of the substrate at the same bulk concentration. Therefore, the increased allyl alcohol concentration (0.07 M) was required for obtaining the smooth deposit on the patterned substrate, due to the large surface area of the patterned substrate compared to that of the blanket substrate.

Galvanostatic ED was carried out to fill the trench covered with the seed layer. A Cu-Sul bath was used in combination with PEG-Cl^{-}-SPS as additives for the filling. The applied cathodic current was set to 5 mA cm^{-2} and the deposition process was stopped when the accumulated charge amount exceeded 300 mC cm^{-2}. TEM observation result after cutting by a FIB is illustrated in Fig. 3.11. Without any defects or voids, a 55 nm patterned substrate was successfully filled.

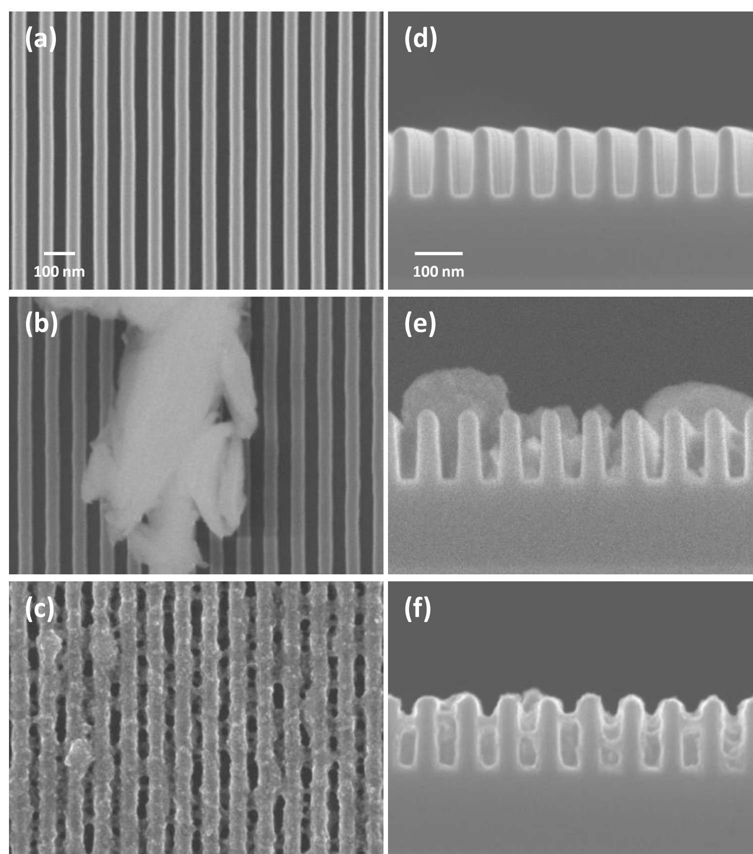


Figure 3.8. FESEM images of 55 nm patterned Ta substrate (a, d) before seed layer deposition and after seed layer formation (b, e) without Pd NPs and (c, f) with Pd NPs.

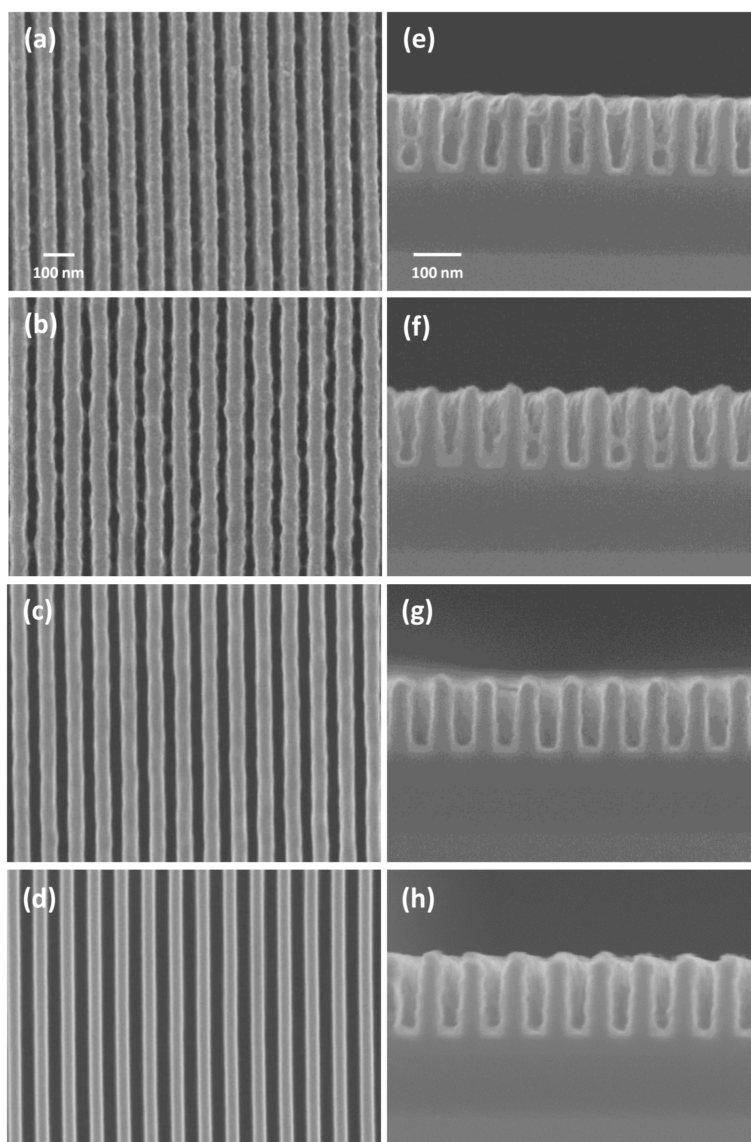


Figure 3.9. FESEM images of Cu seed layer deposited on 55 nm patterned Ta with Pd NPs, according to the allyl alcohol concentration. Allyl alcohol content in Cu-pyro bath was (a, e) 0.0175 M, (b, f) 0.035 M, (c, g) 0.0525 M, and (d, h) 0.07 M.

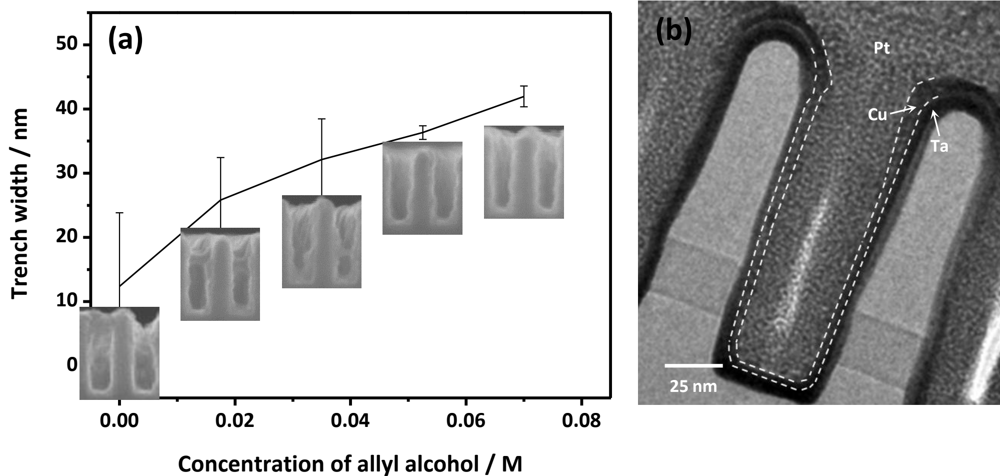


Figure 3.10. (a) Trench opening width after Cu seed layer formation with varying the allyl alcohol concentration in Cu-Pyro bath and (b) TEM image for the Cu seed layer deposited with 0.07 M allyl alcohol (Pt was sputtered before the TEM specimen preparation by FIB).

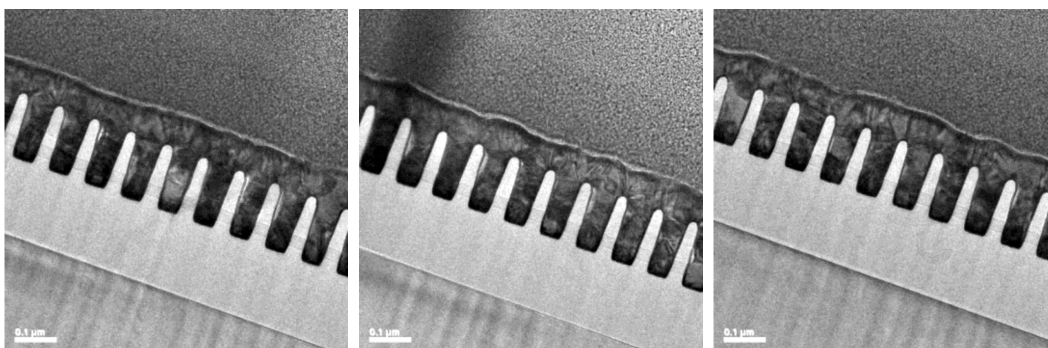


Figure 3.11. TEM analyses of 55 nm patterned trench covered with the Cu seed layer after filling in Cu-Sul bath. The Cu seed layer was prepared by direct ED on the Pd NPs-loaded Ta with 0.07 M allyl alcohol in Cu-Pyro bath.

CHAPTER IV. Direct ED of Cu on Co/Ni alloy

4.1. ELD of Co/Ni alloy barrier layer

4.1.1. Optimization of substrate activation process

The effectiveness of a SAM-Pd activation process on the subsequent ELD procedure was examined by comparing with ELD of NiWP on a SiO_2 substrate activated via conventional Sn-Pd activation process. Conventional Sn-Pd activation process is sequentially carried out by adsorption of colloidal Sn particles on the substrate, followed by covering metallic Pd through displacement reaction between Sn and Pd ions. Then the substrate is "activated" for a subsequent ELD process as Pd can catalyze the ELD. The merit of introducing colloidal Sn particles is that they adsorb well on various substrates and activate substrates including non-conductive material. Nevertheless, ELD of NiWP on Sn-Pd activated SiO_2 substrate induced non-uniform deposit formation as shown in Fig. 4.1a. Thus it was inevitable to introduce SAM on SiO_2 substrate for the activation because the result should be originated from poor adsorption strength of Sn-Pd particles on SiO_2. Consequently by using SAM-Pd activated SiO_2 substrate, we could obtain uniform NiWP film by ELD as shown in Fig. 4.1b.

The SAM-Pd activation process on SiO_2 substrate was optimized by observing surface morphology after activation process and by measuring the resistivity of electroless NiWP film formed on it. Surface morphologies of the pristine SiO_2 and SAM-Pd activated SiO_2 substrates were examined to determine the state of Pd adsorption. The Pd NPs were uniformly distributed on the activated substrate (Fig. 4.2b), but some agglomerated particles were observed. After ELD of NiWP layer on the activated substrate, there were areas with large clusters and non-uniform NiWP growth (Fig. 4.2d), which appeared to occur in areas that previously were covered with agglomerates of Pd NPs. The resultant resistivity of the 25 nm thick NiWP film was 205 (±19.5) μΩ cm; a high value due to the presence of large clusters that induce severe electron-surface scattering. Because such a high resistivity is inappropriate for direct Cu ED, the SAM-Pd activation process was modified by applying mild sonication during Pd NPs adsorption. As shown in Fig. 4.2c, application of ultrasound (40 kHz, 70 W) during Pd NPs adsorption prevented Pd agglomeration on the surface. The ultrasound-treated surface had a 0.91 nm R_{rms} value, lower than the 1.15 nm R_{rms} for the surface prepared without sonication. Consequently, when a 25 nm thick NiWP film was prepared, the film surface was devoid of large clusters as depicted in Fig. 4.2e, and the resultant resistivity of the film was 125 (±4.6) μΩ cm. The surface R_{rms} of the NiWP film was 2.68 nm, 32% smaller than the surface R_{rms} measured on the surface of Fig. 4.2d (3.96 nm).

4.1.2. Optimization of barrier layer ELD

ELD of Co/Ni alloy barrier layer was performed on the SAM-Pd activated SiO_2 substrate. Although the activation process was optimized in previous chapter, the resistivity of a deposited NiWP film was still high for conducting the direct Cu ED on it. Therefore, further reduction in the resistivity of a NiWP film should be preceded.

To achieve a further reduction in the resistivity of a NiWP film, PEG (Mw = 3400 g mol^{-1}) was introduced to the NiWP ELD bath. The addition of PEG can alter the ELD rate by affecting adsorption on active deposition sites. In addition, because PEG can act as a defoamer, the improvement in surface roughness and film ductility was also anticipated via fast desorption of evolved H_2 during ELD.[115] Fig. 4.3a shows that the rate of NiWP ELD decreased as the concentration of PEG increased; however, there was no further decrease in deposition rate beyond a 1 ppm PEG addition. To determine the effect of the decrease in deposition rate, 25 nm thick NiWP layers were prepared at each of the tested PEG concentrations. As expected, suppression of the deposition rate through the addition of PEG was associated with a reduction in resistivity and surface roughness of the NiWP film as in Fig. 4.3b. The addition of between 1 and 5 ppm of PEG induced reductions in resistivity and surface R_{rms} of NiWP film to 89 (± 4.0) μΩ cm and 1.44 nm, respectively.

Subsequently, CoWP and NiCoP layers were also prepared by ELD on SAM-Pd

activated SiO_2 substrate. In case of CoWP layer ELD, however, the resistivity of 25 nm thick CoWP layer deposited with reference condition showed an extremely high value as presented in Fig. 4.4. Therefore, the improvement in the resistivity of CoWP layer was attempted by the variations in the concentration of complexing agent (citrate) and reducing agent (NaH_2PO_2) of ELD bath.

Fig. 4.5 shows the deposition rate of CoWP ELD and resistivity of 25 nm thick CoWP film prepared in various deposition conditions. It was found from the investigation that a reducing agent, rather than a complexing agent, played a key role in controlling the resistivity of the film. As can be seen in Fig. 4.5b, reduction in the concentration of NaH_2PO_2 considerably improved the conductivity of CoWP film, not influencing the rate of ELD. Hence, it was suspected that surplused electrons produced from the the oxidation reaction of abundant $H_2PO_2^-$ (reaction [1.5]) should consumed to further reduce $H_2PO_2^-$ (reaction [1.7]), increasing incorporation amount of P in the CoWP film. Increased P contents in the film at high $H_2PO_2^-$ concentration condition seemed to result in extremely resistive CoWP layer. Consequently, minimum resistivity of 25 nm thick CoWP layer was obtained as 101 (± 6.9) μΩ cm.

Three kinds of NiCoP layers were prepared by varying the concentration of Ni and Co precursor in the bath which had similar composition with the ELD bath for CoWP. Surface morphology, deposition rate, and film resistivity analyses were conducted after forming $Ni_xCo_{(0.04-x)}P$ films having 25 nm of thickness (notation of each film followed

the mole concentration of metal source in the bath). The results in Fig. 4.6 and Fig. 4.7 represent that decrease in Ni/Co source ratio induced rather smooth but higly resistive film formation. Due to poor catalytic activity of Co toward the oxidation reaction of $H_2PO_2^-$, deposition rate became slow as the amount of Co source increased.[116]

The composition and resistivity of each barrier layer are summerized in Table 4.1. For all cases, the incorporation amount of P or W and the resistivity were nearly 10% and 100 μΩ cm, respectively, which were feasible for making "stuffed" barrier layer and for performing direct Cu ED on it. The amorphous nature of each barrier layer was confrimed by XRD analyses results in Fig. 4.8. Thus the direct Cu ED was performed on prepared barrier layer. Details are discussed in the proceeding chapter.

Table 4.1. Composition and Properties of Each Barrier Layer

	NiWP	**CoWP**	**$Ni_{0.03}Co_{0.01}P$**	**$Ni_{0.02}Co_{0.02}P$**
Ni	81.7%		55.3%	43.1%
Co		81.9%	29.7%	45.3%
P	11.4%	4.4%	10.8%	8.3%
W	3.5%	5.8%		
Resistivity / μΩ cm	89 (±4.0)	101 (±6.9)	98 (±8.8)	107 (±19.9)
Adhesion (PAR value)	3.45%	7.90%	6.67%	6.45%

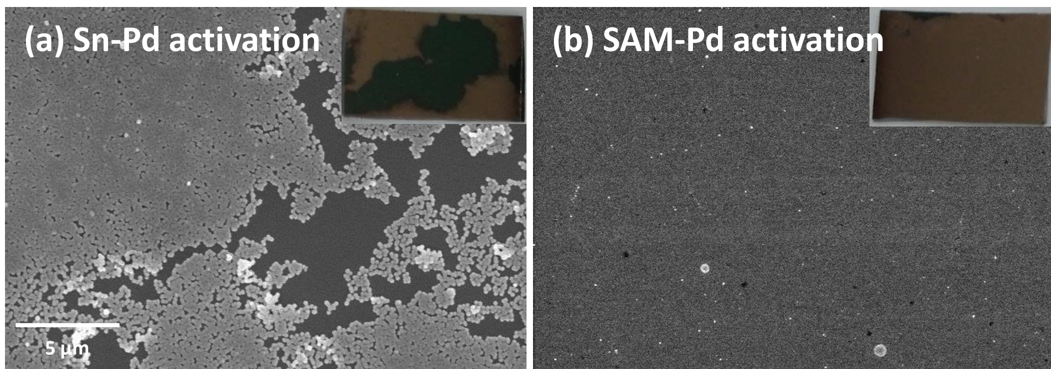


Figure 4.1. FESEM surface analyses of ELD-NiWP layer deposited on (a) Sn-Pd activated and (b) SAM-Pd activated SiO_2 blanket substrate. Picture of the specimen was also taken after ELD (insets).

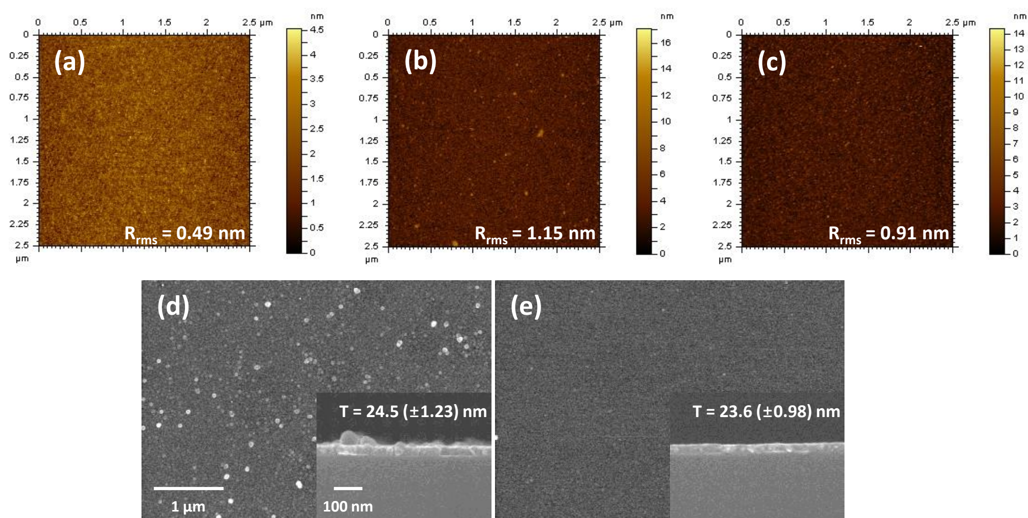


Figure 4.2. The AFM morphology analyses of (a) pristine SiO_2 substrate and the SiO_2 substrate after SAM-Pd activation (b) without and (c) with sonication during the Pd NPs adsorption step. (d) and (e) show FESEM surface and cross-sectional (insets) analyses for a 25 nm thick NiWP film deposited on (b) and (c), respectively.

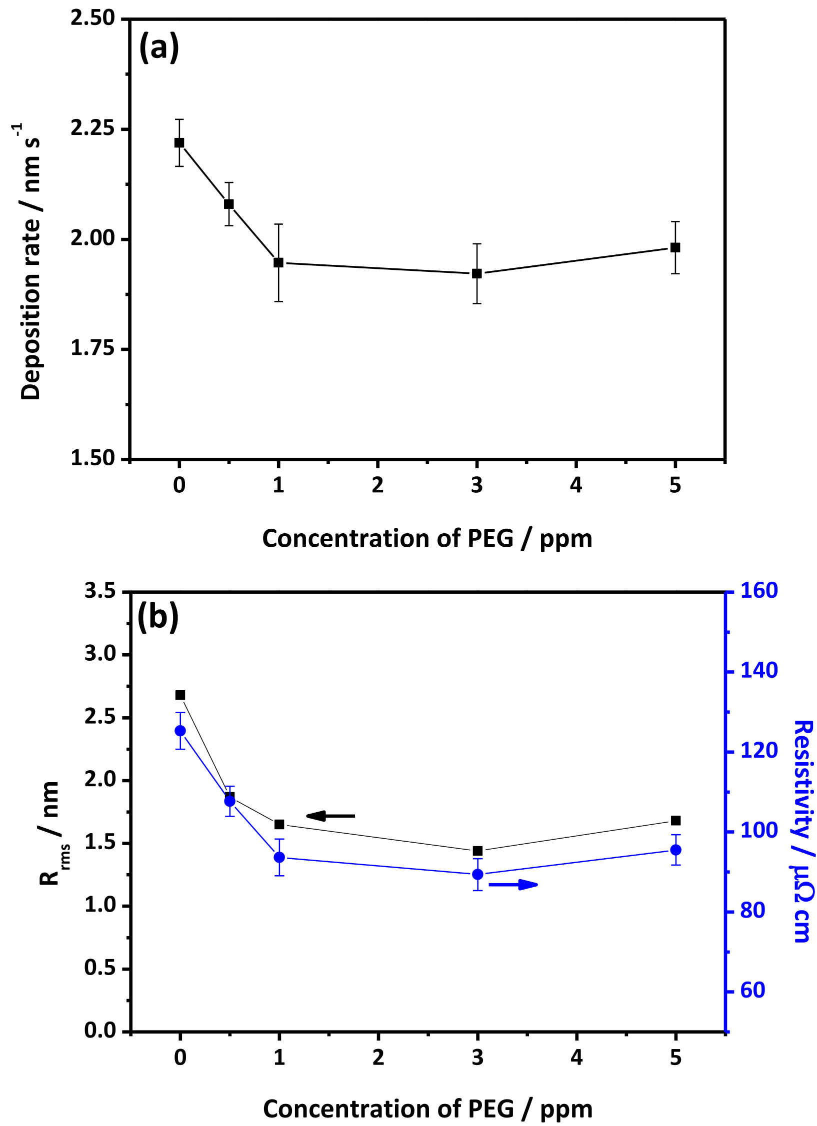


Figure 4.3. The effect of PEG concentrations on (a) the rate of NiWP ELD and (b) resistivity and surface roughness of a 25 nm thick NiWP film.

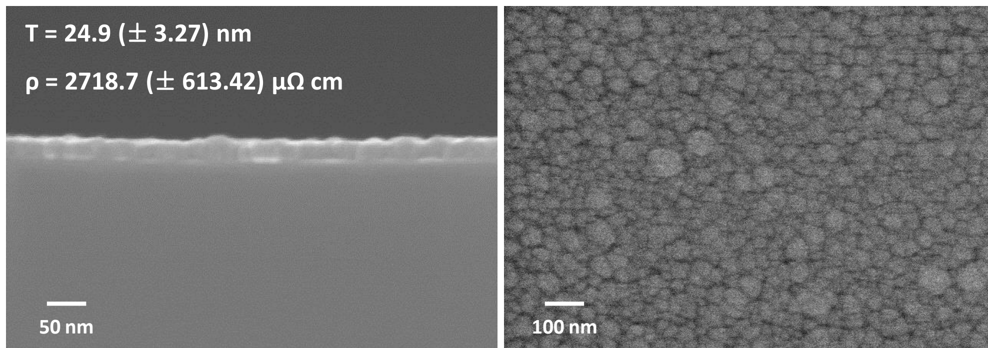


Figure 4.4. Surface and cross-sectional FESEM analyses of CoWP layer deposited with 0.4 M citrate and 0.2 M NaH_2PO_2.

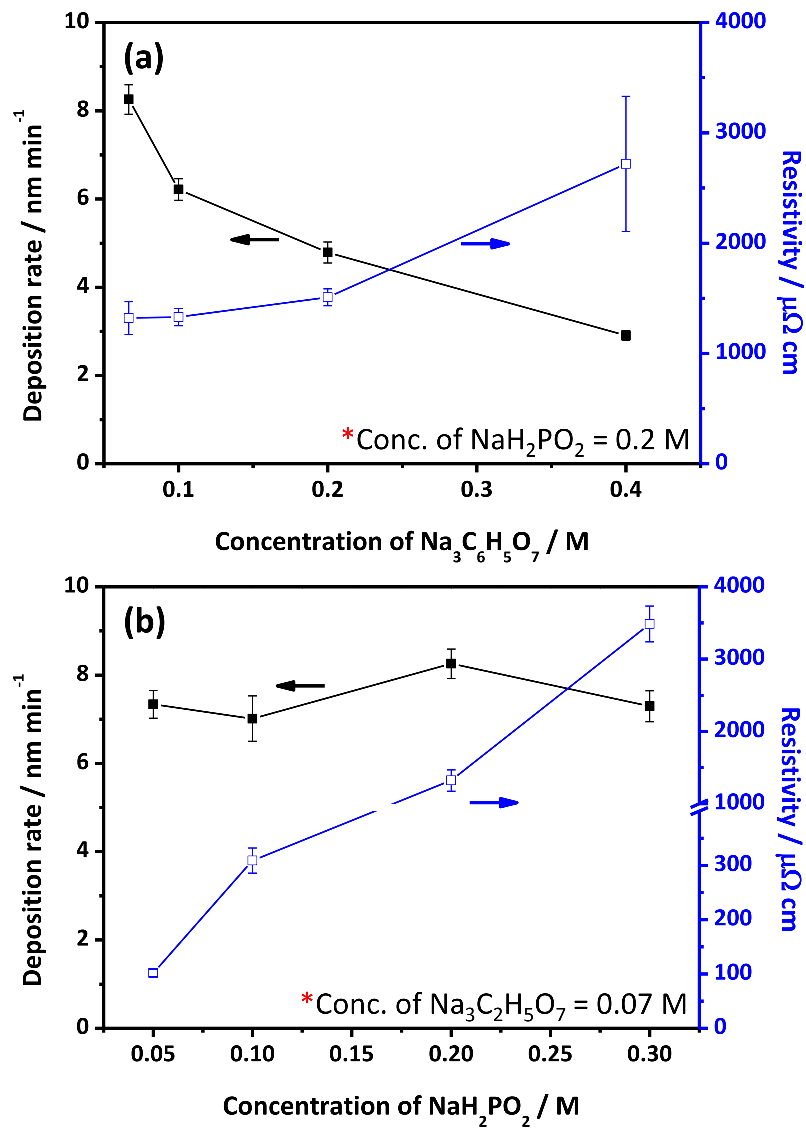


Figure 4.5. Effect of citrate and NaH_2PO_2 concentration on the deposition rate of CoWP ELD and resistivity of 25 nm thick CoWP film.

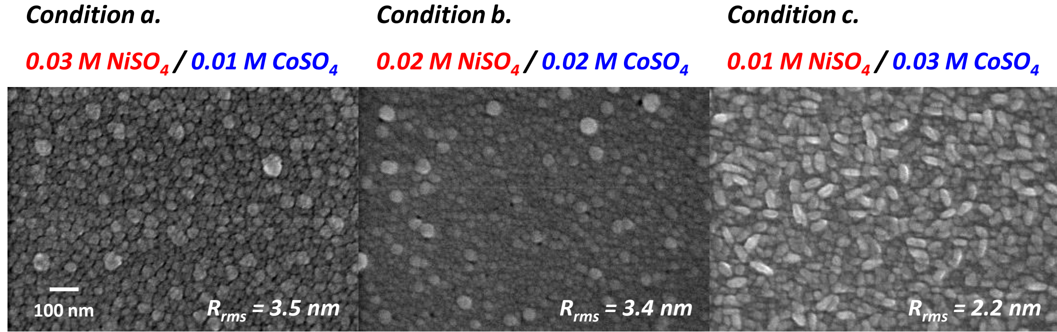


Figure 4.6. FESEM surface analyses of $Ni_xCo_{(0.04-x)}P$ film prepared with each deposition condition.

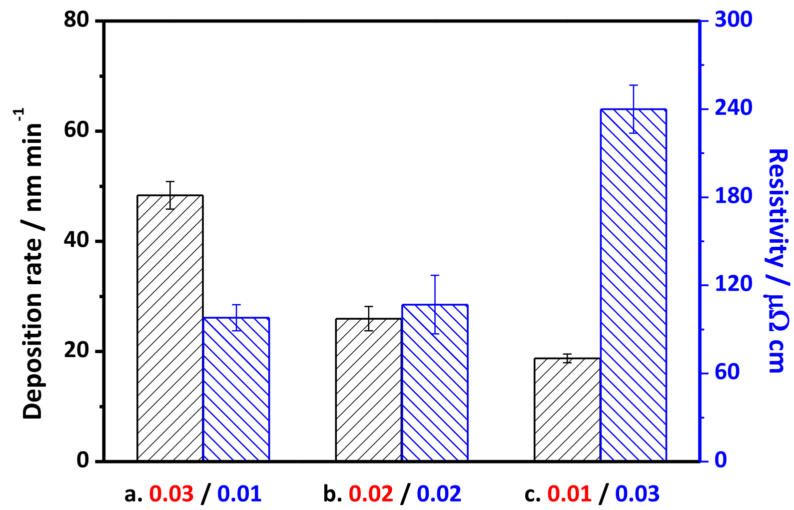


Figure 4.7. The deposition rate and resistivity of 25 nm thick Ni_xCo_yP film prepared in each deposition condition.

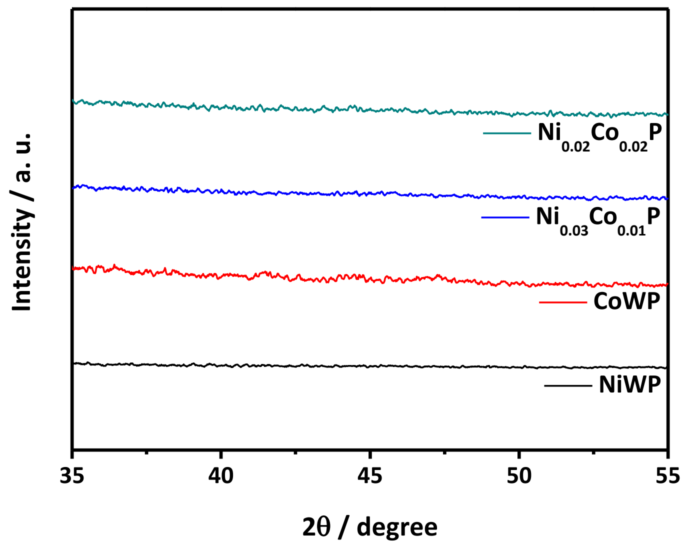


Figure 4.8. XRD analyses of each barrier layer having 25 nm of thickness.

4.2. Direct Cu ED on ELD-barrier layer

Direct Cu ED was carried out on 25 nm thick ELD-barrier layers having ~100 μΩ cm of resistivity, which were prepared following the descriptions in previous chapter. As a representative, the procedure of direct Cu ED was investigated on a NiWP film having 89 μΩ cm of the resistivity.

Before performing Cu ED, the NiWP layer underwent coulometric reduction to reduce the native oxide on the surface. Fig. 4.9 presents XPS results for Ni_{2p}, an abundant component in a NiWP layer. Compared to the untreated (as-prepared) NiWP layer, the coulometrically treated layer had less NiO on the surface. The results indicate that surface oxide can be successfully removed by applying a coulometric reduction treatment.

Oxide removal by coulometric reduction affected two aspects of the NiWP layer: (1) alteration of the electrochemical activity of the NiWP layer for Cu ion reduction and (2) alteration of the adhesion between the NiWP and Cu layers. To investigate those effects, the polarization behavior of Cu ion reduction on the NiWP layer was assessed by performing LSV in the Cu ED electrolyte. The electrolyte contained 0.25 M $CuSO_4$ and 1.00 M H_2SO_4, as described in the experimental section. As shown in Fig. 4.10, the voltammograms for the as-prepared and coulometrically treated NiWP layers can be divided into four regions: Region 1, Cu nuclei formation and coalescence on the NiWP layer; region 2, Cu growth on the deposited Cu layer; region 3, mass transfer limited Cu

deposition; and region 4, Cu deposition with H_2 evolution. The positive shift in the end-potential of region 1 indicates that Cu nucleation and film formation were more favorable on the coulometrically treated NiWP layer than on the as-prepared layer. In addition, tape test results indicated that adhesion between the Cu and NiWP layers was remarkably improved on the coulometrically treated NiWP layer (e.g., Cu deposit detachment occurred during ED on the as-prepared samples as in Fig. 4.11).

One characteristic behavior detected in the LSV results was the occurrence of a large current density in region 1 of Fig. 4.10. Within the late portion of region 1, the current density was larger than that in the initial portion of region 2. According to the previous report of A. Królikowski *et al.*, the reduction of residual oxygen occur at low overpotential when polarization of NiP alloy was conducted in H_2SO_4 electrolyte and this effect was pronounced for amorphous NiP.[117] Likewise, as depicted in Fig. 4.12, the reduction of residual oxygen occurred at low overpotential when the coulometrically reduced NiWP layer was investigated by the LSV. However, when current density was simply compared, it seemed that current related to the residual oxygen reduction on NiWP was not sole rationale for enhanced current density in region 1. For example, increased current density at −0.3 V (vs. SCE) in Fig. 4.10 was 6.2 mA cm^{-2}, whereas that in Fig. 4.12 was merely 3.8 mA cm^{-2}. Therefore, it could be explained that the enhanced current density in region 1 of Fig. 4.10 is related to the addition of current associated with Cu ion reduction and dissolved oxygen reduction on the NiWP layer. The abrupt

decline in current density at the boundary of region 1 and 2 may be related to the cessation of the oxygen reduction reaction due to the film surface changing from NiWP (with Cu clusters) to Cu.

Very similar polarization curves were obtained when CoWP, $Ni_{0.03}Co_{0.01}P$, and $Ni_{0.02}Co_{0.02}P$ were investigated as depicted in Fig. 4.13. The results of regions 1 and 2 shown in Fig. 4.10 and 4.13 indicate that barrier material (e.g. Co and/or Ni) is exposed to the Cu ED electrolyte until the Cu has fully covered the barrier layer. Under the circumstances, a displacement reaction between Cu ions and Co and/or Ni metal could not be avoided because the reaction is thermodynamically favorable. To prevent further displacement, it is important to promote the complete coverage of the barrier layer by Cu before attempting to increase the thickness of the Cu film.

Fig. 4.14 illustrates the effect of deposition potential on the surface morphology of the Cu deposited on the coulometrically treated NiWP layer. In the ED process, the nucleation density is exponentially proportional to the applied overpotential.[118,119] Fig. 4.14b and c thus show that some nuclei were sparsely formed on the NiWP layer when the applied potential was low; however, a uniform, smooth Cu film was obtained when the applied potential was −1.25 V (vs. SCE) as in Fig. 4.14d. Furthermore, the conductance of the Cu electrodeposited specimens increased with an increase in applied potential, as reflected by the difference in R_S before and after Cu ED (R_S/R_{S0} = 0.13 (±0.011); Fig. 4.15). However, an increase in deposition potential to −1.5 V (vs. SCE)

resulted in a rough Cu deposit with voids (Fig. 4.14e), which is due to the vigorous H_2 evolution that occurs at that higher potential. Based on these results, a −1.25 V (vs. SCE) of deposition potential was considered optimal for direct Cu ED on the coulometrically treated NiWP layer.

To investigate the Cu film properties further, a 100 nm thick Cu film was formed by increasing the deposition charge during Cu ED. However, continued deposition at −1.25 V (vs. SCE) produced a rough Cu film as in Fig. 4.16a due to vigorous H_2 evolution during Cu deposition. Numerous vacancies were present on the film, and the resistivity of the film was 9.3 (±1.06) μΩ cm. To avoid the problems associated with H_2 evolution, a two-step deposition process was introduced. In the first step, a high overpotential of −1.25 V (vs. SCE) was applied for 10 mC cm^{-2} to induce quick formation of a thin Cu film. In the second step, a low overpotential of −0.45 V (vs. SCE) was applied for 190 mC cm^{-2} to increase film thickness. This two-step process resulted in growth of a uniform 100 nm thick Cu layer with a resistivity of 3.4 (±0.28) μΩ cm.

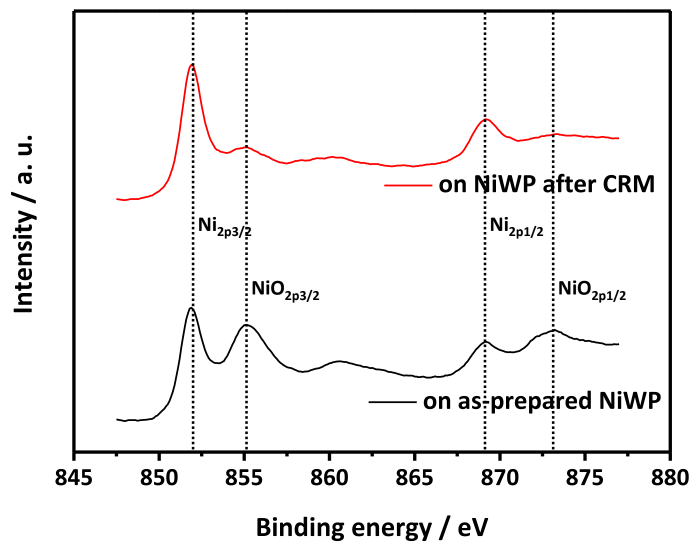


Figure 4.9. Results of XPS analyses of NiWP film before (black line) and after (red line) undergoing the coulometric reduction process (slight oxidation occurs during sample transfer).

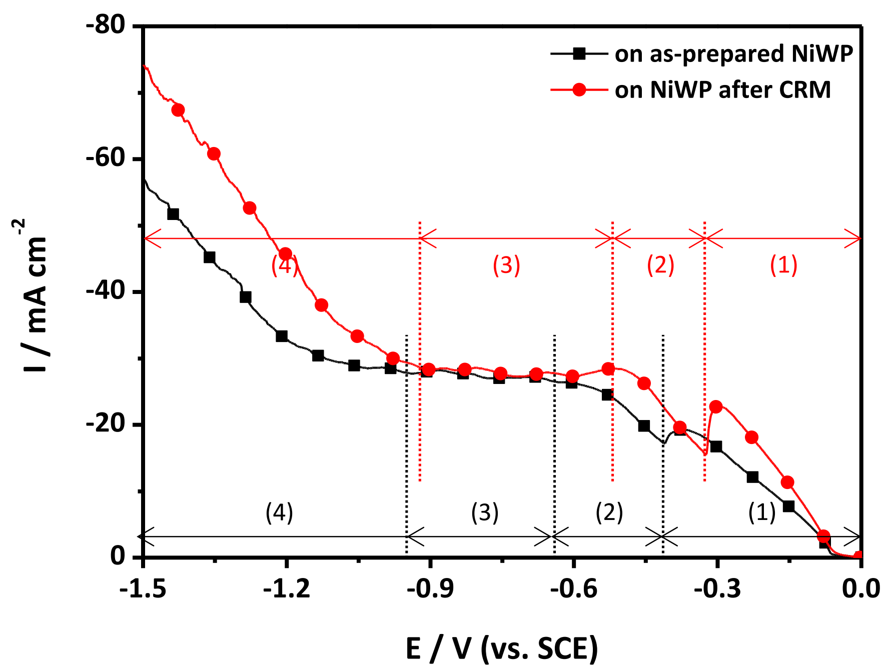


Figure 4.10. Results of LSV on the NiWP layer before (black line) and after (red line) coulometric reduction (scan rate = 20 mV s^{-1}).

Figure 4.11. Pictures of (a) as-prepared NiWP film and (b, c) Cu film electrodeposited (b) without coulometric reduction process or (c) after coulometric process on NiWP film.

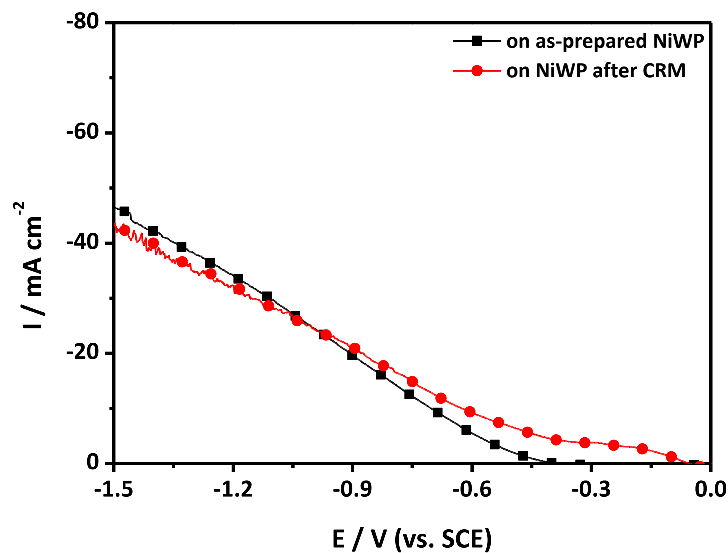


Figure 4.12. The LSV results on the NiWP layer before (black line) and after (red line) coulometric reduction process. The LSV studies were conducted in 1 M H_2SO_4 electrolyte (Cu ED bath without Cu ion and additives, scan rate = 20 mV s^{-1}).

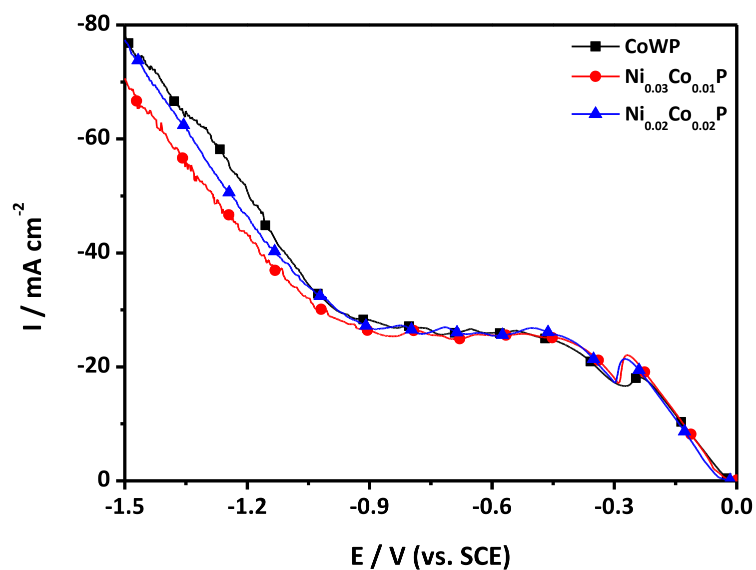


Figure 4.13. Results of LSV on each barrier layer after coulometric reduction (scan rate = 20 mV s^{-1}).

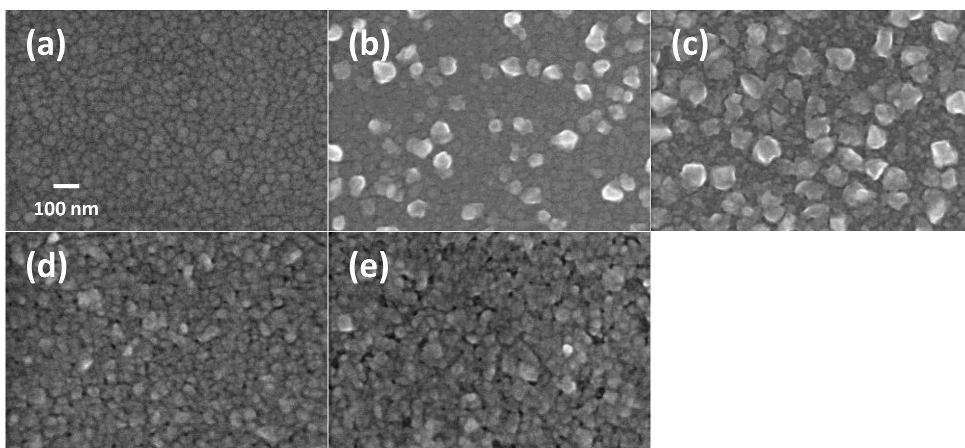


Figure 4.14. FESEM surface analyses of 25 nm thick NiWP layers (a) after coulometric reduction, and (b-e) after Cu ED at (b) −0.75 V, (c) −1.0 V, (d) −1.25 V, and (e) −1.5 V vs. SCE. In all cases, the deposition charge density was 10 mC cm^{-2}.

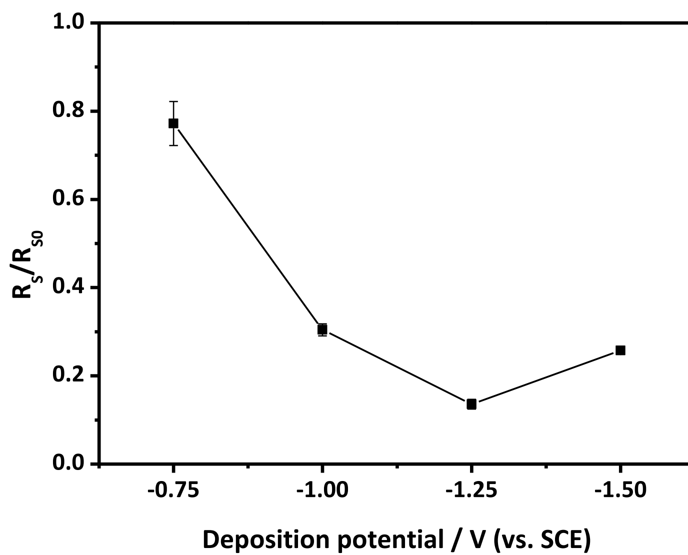


Figure 4.15. The effect of deposition potential on the ratio of the sheet resistance after Cu ED (R_S) to the resistance before Cu ED (R_{S0}). The deposition charge density was 10 mC cm^{-2} and the average R_{S0} for the 25 nm thick NiWP layer was 35 Ω $square^{-1}$.

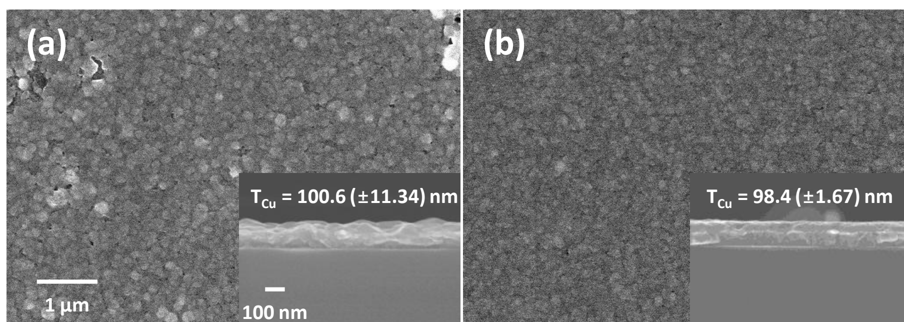


Figure 4.16. FESEM surface analyses of a Cu film deposited on a NiWP layer (a) at −1.25 V (vs. SCE) for 200 mC cm^{-2} and (b) at −1.25 V (vs. SCE) for 10 mC cm^{-2} followed by −0.45 V (vs. SCE) for 190 mC cm^{-2}. The insets present a cross-sectional FESEM images of a 100 nm thick Cu film on a 25 nm thick NiWP layer.

4.3. Barrier layer performance and trench filling

4.3.1. Barrier layer performance investigation

The performance of each electroless barrier layer was investigated using Cu (100 nm, ED) / barrier layer (25 nm, ELD) / SiO_2 stacked blanket specimens. The surface analyses of each barrier layer and Cu film on it are summarized in Fig. 4.17. As can be seen in Fig. 4.17, a uniform, smooth 100 nm thick Cu film was formed on each 25 nm thick barrier layer, following the procedure described in previous chapter.

The specimen was annealed at 500℃ for 30 min in a N_2 atmosphere and the change in R_S was measured to evaluate the barrier layer performance (Fig. 4.18). Unfortunately, R_S increased after the thermal treatment when CoWP or CoNiP was tested, which implied those barrier layers did not properly prohibit the diffusion of Cu. The failure was remarkable when the barrier layer did not contain W, assuring the importance of refractory metal incorporation on the diffusion barrier property improvement.[59-61] On the contrary, the R_S of the specimen decreased by approximately 13% after annealing when NiWP was applied as barrier layer. Improvement in conductivity should be originated from the grain growth and stress relaxation during the thermal treatment.[120] A noticeable increment in diffraction peaks in annealed specimen supports the explanation (Fig. 4.19). More importantly, no peak related to silicide formation was observed, which indicated

that electroless deposited NiWP layer could successfully inhibit inter-diffusion between Cu and Si.[55,121] Therefore, NiWP layer was selected for a subsequent trench filling experiment on a patterned SiO_2 substrate.

4.3.2. Trench filling by all-wet metallization process

Fig. 4.20 shows current-potential curves for Cu deposition in the presence of organic additives for bottom-up Cu filling. As additives would affect Cu growth stage considerably more than the Cu nucleation stage, LSV was performed on the NiWP specimen after the 1st step Cu ED. As can be seen in Fig. 4.20, the tested specimen showed polarization behavior similar to that of the Cu substrate (Fig. 4.20, inset). Furthermore, the combination of additives induced general polarization behavior as on a Cu substrate before the mass transfer limiting region: the addition of PEG-Cl^- suppressed the deposition of Cu, whereas the addition of SPS to PEG-Cl^- accelerated Cu deposition.[104-106] Thus it was expected that the organic additives should act in a manner similar to that on a Cu substrate during gap-filling on a patterned NiWP specimen.

A 120 nm wide, patterned SiO_2 substrate with a 2.5 aspect ratio was prepared for the trench filling experiment. As depicted in Fig. 4.21a, a 25 nm thick NiWP layer was conformally formed along the top, sides, and bottom of each trench. The degree of conformality was evaluated by comparing the thickness ratio. The thickness ratios of

side/bottom and top/bottom was measured as 0.99 (±0.089) and 1.06 (±0.11), respectively, implying excellent conformality of ELD for forming barrier layer.

Subsequently, trench filling was conducted by using the two-step, direct Cu ED process. The deposition conditions were −1.25 V (vs. SCE) for 10 mC cm^{-2} in the first step and −0.45 V (vs. SCE) with a variety of charge amounts in the second step. As the total charge during deposition increased, bottom-up Cu filling was observed as in Fig. 4.22.

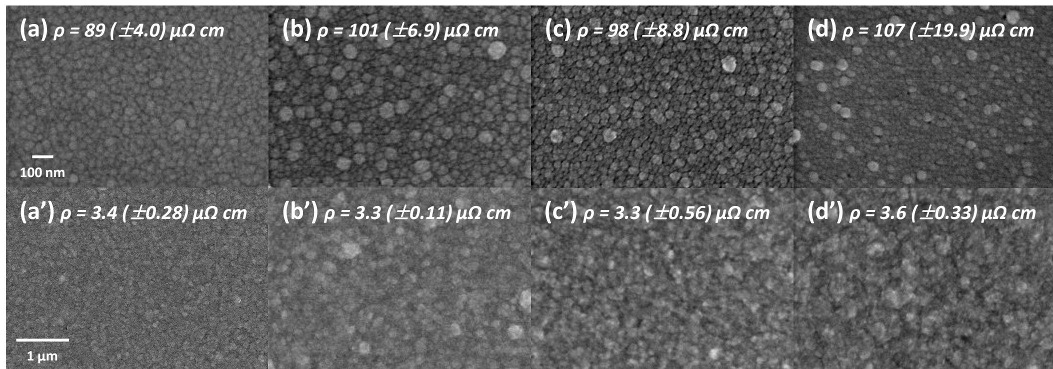


Figure 4.17. FESEM surface analyses of 25 nm thick (a) NiWP, (b) CoWP, (c) $Ni_{0.03}Co_{0.01}P$, and (d) $Ni_{0.02}Co_{0.02}P$ formed by ELD on SAM-Pd activated SiO_2 substrate. (a’~d’) FESEM surface analyses of 100 nm thick Cu film directly deposited by ED on corresponding (a~d) ELD-barrier layer.

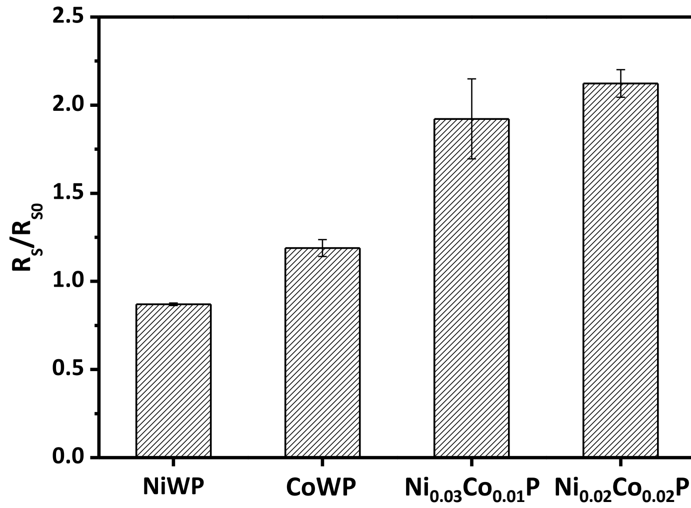


Figure 4.18. Change in sheet resistance after thermal treatment (500℃, 30 min in a N_2 atmosphere) of each specimen having different barrier layer. The thickness of each barrier layer was 25 nm and that of the overlaying Cu was 100 nm.

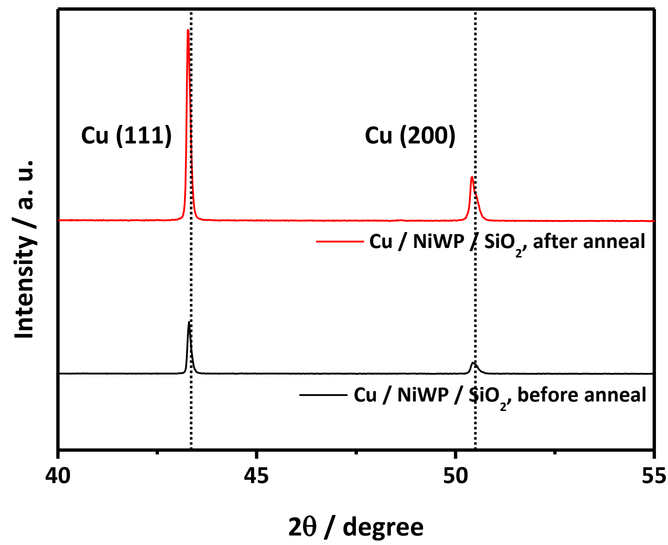


Figure 4.19. XRD analyses of a Cu (100 nm) / NiWP (25 nm) / SiO_2 stacked specimen before (black line) and after (red line) thermal treatment at 500℃ for 30 min in a N_2 atmosphere.

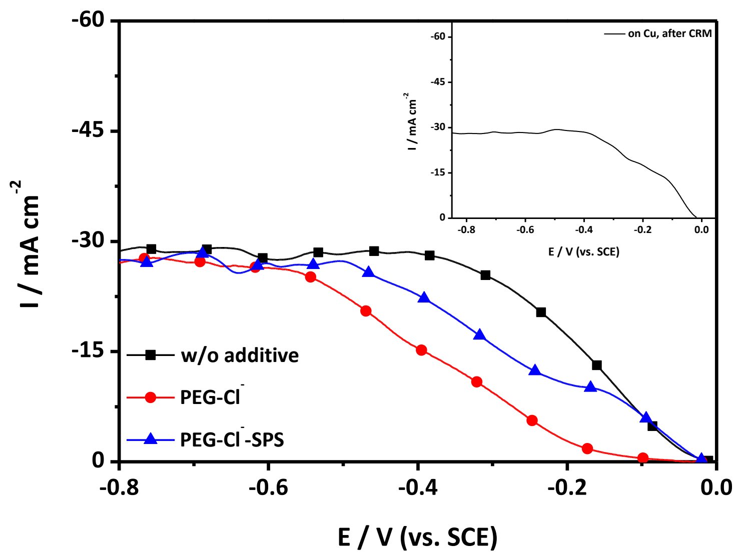


Figure 4.20. LSV on the NiWP substrate after 1st step Cu ED with varying the additive combination in Cu ED electrolyte. Inset: LSV on the 30 nm thick Cu film after CRM. The scan rate was 20 mV s^{-1}.

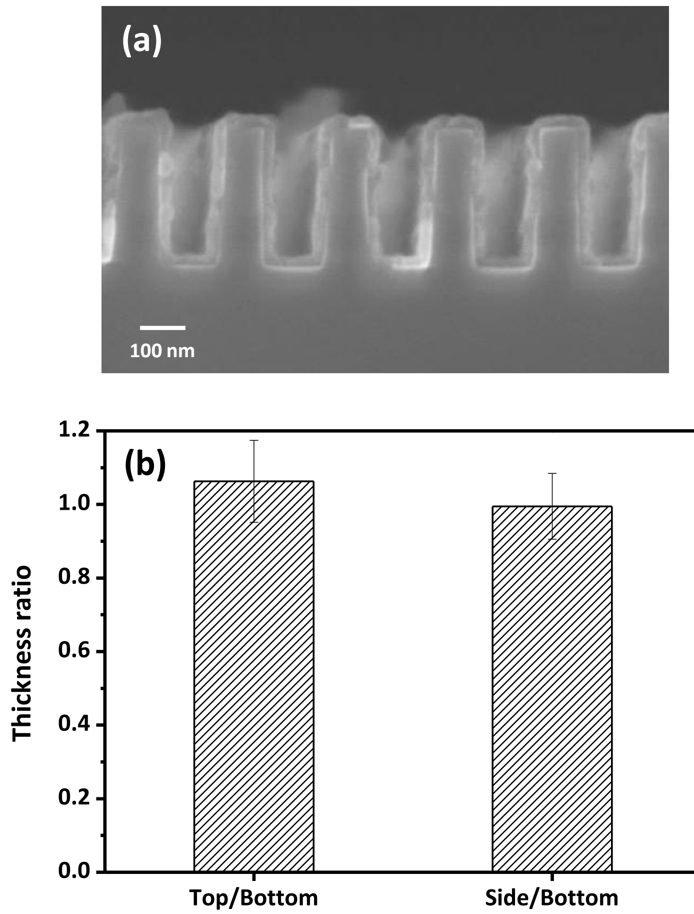


Figure 4.21. (a) FESEM image of 120 nm width trench after NiWP barrier layer formation and (b) the evaluation of conformality.

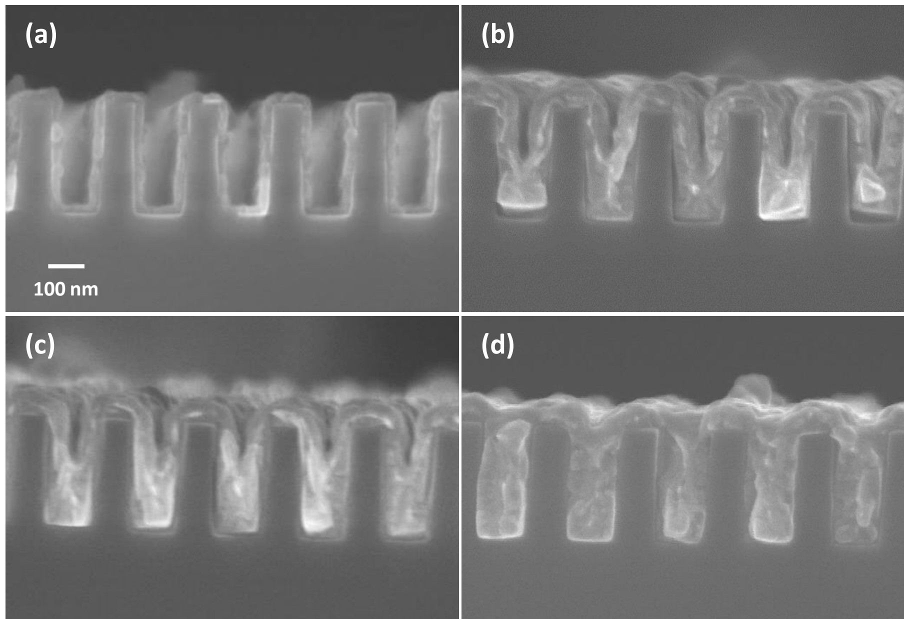


Figure 4.22. FESEM images of 120 nm width trench (a) after NiWP ELD and after direct Cu ED on (a) with total charge amount of (b) 150 mC cm^{-2}, (c) 200 mC cm^{-2}, and (d) 300 mC cm^{-2}.

CHAPTER V. Direct ELD of Cu on Ru

5.1. Cu growth phenomena on Ru during ELD

5.1.1. Preparation of Ru electrode for EQCM monitoring

It would be best to use ALD-Ru covered QCM electrode for the EQCM monitoring. Unfortunately, however, commercial QCM electrode covered with ALD-Ru was not available. Therefore, we fabricated the Ru QCM electrode (Ru electrode) for the EQCM observation by the galvanic replacement reaction on Cu QCM electrode (Cu electrode).

The thickness and surface morphology of fabricated Ru electrode was analyzed. The displaced thickness was simply determined by QCM analysis as in Fig. 5.1a. Considering the stoichiometry of displacement reaction, surface area of electrode, areal density of Cu, thickness of Cu monolayer, and lattice parameter of Cu (fcc) and Ru (hcp), the dissolved Cu layer was 11.03 nm and the deposited Ru layer was 8.70 nm. In addition, Fig. 5.1c implied that Ru was continuously formed after the displacement reaction on the Cu electrode with distinguishable change in surface morphology.

The validity of the fabricated Ru electrode with Ru wafer was examined by comparing potential (E) transient during ELD. As can be seen in Fig. 5.2, the E transient was quite

similar between the two samples. Although many factors such as surface roughness should be different between Ru wafer and electrode, the use of Ru electrode was quite useful for the real-time investigation of Cu ELD using EQCM.

5.1.2. Observation of Cu growth phenomena on Ru during ELD

Prior to the growth phenomena observation, the effect of HF application on the reduction of Ru surface oxide was evaluated by the CRM, because the amount of remaining surface oxide is proportional to the charge applied before the potential plateau reached during the CRM.[110] Corresponding to such a perspective, the results depicted in Fig. 5.3 indicated that the Ru surface oxide was partially removed after the HF treatment. Nevertheless, the HF treatment and subsequent rinsing steps were significant processes to assure the identical surface state, even though the treatment could not eliminate the entire Ru surface oxide.

Formaldehyde based (HCHO-bath) and hydrazine based (NH_2NH_2-bath) Cu ELD solutions were compared to investigate the Cu growth phenomena on Ru during ELD. For the interpretation of ELD, various studies used a mixed potential theory. The mixed potential theory assumes that the potential and current during ELD can be derived by superimposing the polarization curve obtained from each half reaction of ELD: metal ion reduction and the oxidation of reducing agent.[116,122] However, it is generally accepted that

the mixed potential method could not reflect the interdependence of the two half reactions and real-time change in the surface state.[53,97,122] Furthermore, shift in mixed potential occasionally observed when the scan rate for the polarization differed, due to the irreversibility of ELD and the forced potential. Therefore, EQCM method that simultaneously records the E and mass change (Δm) during ELD was introduced in this study.

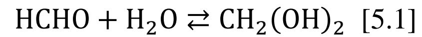
The EQCM monitoring by using prepared Ru electrode was conducted in either HCHO-bath or NH_2NH_2-bath. As described in Fig. 5.4, in the case of EQCM monitoring in HCHO-bath, the E negatively shifted during 20 s and maintained at −0.75 V (vs. SCE). At the same time, mass change rate (r: $d(\Delta m)/dt$) increased during initial 20 s and kept 0.017 μg s^{-1} until the end of the monitoring. On the other hand, E positively shifted right after the dipping of the Ru electrode into the NH_2NH_2-bath (Fig. 5.4a). Simultaneously, fast decline in the r was shown at the initial stage of monitoring as depicted in Fig. 5.4b. Then after 5 to 7 seconds of the immersion, E and r maintained at −0.68 V (vs. SCE) and 0.016 μg s^{-1}, respectively.

Obvious difference was also observed when R_S change was measured after ELD in each bath using Ru wafer. Fig. 5.5 represents the R_S ratio before and after ELD (R_{S0}/R_S, proportional to the conductance of the specimen) according to the deposition time. As shown in Fig. 5.5, R_{S0}/R_S fluctuated in the early stage and started to increase after 20 s of deposition when HCHO-bath was used. On the contrary, R_{S0}/R_S noticeably increased at

the beginning of the deposition when NH_2NH_2-bath was investigated.

Negative shift in E, increase in r, and fluctuation in R_{S0}/R_S occurred at the initial stage of ELD when HCHO-bath was studied. Those phenomena would be related with the induction period, which is frequently reported in ELD.[34,53,97] Meanwhile, NH_2NH_2-bath did not exhibit the general phenomena relevant to the induction period. The difference in initial phase would be closely associated with the oxidation mechanism of formaldehyde and hydrazine on metal catalyst (M)[123];

Oxidation of formaldehyde:



$$\mathrm{HCHO + H_2O \rightleftarrows CH_2(OH)_2} \quad [5.1]$$

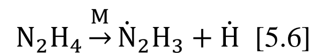
$$\mathrm{CH_2(OH)_2 + OH^- \rightleftarrows CH_2OHO^- + H_2O} \quad [5.2]$$

$$\mathrm{CH_2OHO^- \xrightarrow{M} \dot{C}HOHO^- + \dot{H}} \quad [5.3]$$

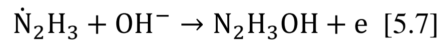
$$\mathrm{\dot{C}HOHO^- + OH^- \rightarrow CH(OH)_2O^- + e} \quad [5.4]$$

$$\mathrm{CH(OH)_2O^- \rightarrow HCOO^- + H_2O} \quad [5.5]$$

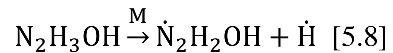
Oxidation of hydrazine:



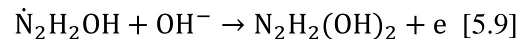
$$\mathrm{N_2H_4 \xrightarrow{M} \dot{N}_2H_3 + \dot{H}} \quad [5.6]$$



$$\mathrm{\dot{N}_2H_3 + OH^- \rightarrow N_2H_3OH + e} \quad [5.7]$$



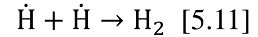
$$\mathrm{N_2H_3OH \xrightarrow{M} \dot{N}_2H_2OH + \dot{H}} \quad [5.8]$$



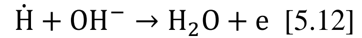
$$\mathrm{\dot{N}_2H_2OH + OH^- \rightarrow N_2H_2(OH)_2 + e} \quad [5.9]$$

$$\mathrm{N_2H_2(OH)_2 \rightarrow N_2 + 2H_2O} \quad [5.10]$$

The hydrogen atoms can either be oxidized or be desorbed as a gas;



$$\dot{H} + \dot{H} \rightarrow H_2 \quad [5.11]$$



$$\dot{H} + OH^- \rightarrow H_2O + e \quad [5.12]$$

In general, the dehydrogenation step (reaction [5.3], [5.6] and [5.8]) considerably affects to the catalytic nature of the electroless processes.[97,123] As clarified in the oxidation mechanism, however, formaldehyde should be converted to methylene glycol anion (CH_2OHO^-, reaction [5.1] and [5.2]) before the adsorption and dehydrogenation on metal catalyst (reaction [5.3]). On the other hand, hydrazine forms atomic hydrogen directly on metal catalyst after adsorption (reaction [5.6] and [5.8]). In addition, platinum group metals which are known as better catalysts toward the oxidation of hydrazine than that of formaldehyde should assist the prompt oxidation of hydrazine minimizing the induction period.[116] Consequently, it is reasonable to assume that the synergetic effect of aforementioned two factors would induce the distinction in the initial stages of Cu ELD on Ru surface when two baths were investigated.

As the induction period prohibits the precise observation of growth phenomena at the initial stage, it was determined that the NH_2NH_2-bath was more appropriate for this study. The growth phenomena investigation could be started from the EQCM monitoring and R_{S0}/R_S change those were used for the bath examination. From Fig. 5.4, it was expected that the sharp change in E at the initial stage in NH_2NH_2-bath was attributed to the transition of the surface from Ru to Cu. Therefore, the high r during that period indicated the favorable deposition of Cu on Ru. In accordance with these considerations, Fig. 5.5

suggested that Cu nucleated on Ru continuously, forming a film.

The formation of Cu film on Ru was also confirmed by the LSV experiment in 0.05 M TMAH electrolyte. The LSV experiment was conducted on Ru and on Cu deposited Ru substrates which were prepared by using NH_2NH_2-bath. The scanning was performed from −1200 to 0 mV (vs. SCE) and the scan rate was 20 mV s^{-1}. As depicted in Fig. 5.6, an oxidation peak was observed around −900 mV (vs. SCE) on blanket Ru substrate, whereas on Cu deposited Ru substrates, that peak disappeared. As the displacement from Ru to Cu should be excluded due to the higher standard reduction potential of Ru than Cu, it could be concluded that conductive ELD-Cu film fully covered the Ru at the early stage of the deposition (below 3 s).

The deposition process on Ru was further observed by AFM, and Fig. 5.7 shows the surface morphology change at the initial stages of ELD when the deposition was conducted in NH_2NH_2-bath. As can be seen in Fig. 5.7a to c, before 5 s, the surface morphology of each specimen was similar to that of blanket Ru. It seemed that thick and columnar Ru grain induced large R_{rms} value. The surface morphology changed, however, with decrease in the R_{rms} value between 5 s and 6 s of deposition. After 6 s, the island-like deposits emerged, showing distinctly different surface morphology with blanket Ru, as in Fig. 5.7d and e. Decrease in R_{rms} value would be related with the high density Cu nucleation. Therefore, it was presumed that Cu film grew on Ru showing indistinguishable surface morphology before the moment of the surface morphology

transition. As the deposition time increased, Cu growth seemed to follow the 3 dimensional (3D) island formation.

5.1.3. Determination of Cu growth phenomena on Ru during ELD

Usually, the metal growth mode on a heterogeneous substrate is determined by the binding energy (E) and crystal misfit (δ) between substrate and deposited metal. In the case of Cu growth on Ru, there are many reports that Cu can be underpotentially electrodeposited on Ru, and these are decisive evidences of the strong E between Ru and Cu ($E_{\text{Ru-Cu}}$).[124,125] Based on the calculation by deposition potential shift, K.R. Zavadil *et al.* reported that underpotentially deposited Cu on Ru was more stable than bulk deposited Cu on Cu, with a Gibbs energy difference of 35 kJ mol^{-1}.[125] The strong $E_{\text{Ru-Cu}}$ makes it possible to assume that the Cu can grow preferentially not on the deposited Cu but on Ru at the early stage of ELD.

δ between Ru and Cu ($\delta_{\text{Ru-Cu}}$) is calculated by using the nearest interatomic distances, with the equation expressed as

$$\delta_{\text{Ru-Cu}} = {(d_{Cu} - d_{Ru})}/{d_{Ru}} \quad [5.13]$$

where d_{Cu} and d_{Ru} are the nearest interatomic distances of deposited Cu and Ru substrate, respectively.[126] X-ray diffractometer spectra was recorded on the Ru substrate covered with 55 nm thick ELD-Cu film as in Fig. 5.8, and d values of the strongest peaks of each

metal in the spectra were selected for the calculation (JCPDS file No. 04-0836 for Cu and No. 06-0663 for Ru). As a result of calculation, $\delta_{Ru\text{-}Cu}$ has relatively large value of ca. 24%.[127] Therefore, these theoretical contemplation of strong $E_{Ru\text{-}Cu}$ and large $\delta_{Ru\text{-}Cu}$ support the assumption that early stage Cu nucleation on Ru during ELD would follow or be similar to Stranski-Krastanov growth mode (c.f. layer-by-layer growth occurred with strong E and nearly zero δ values).[128]

The surface morphology changed between 5 s and 6 s of deposition. To measure the estimated value of growth mode transition thickness, an electrochemical method was used for the stripping of Cu deposited in NH_2NH_2-bath. Fig. 5.9 shows the electrochemical stripping of ELD-Cu by LSV with scanning from open circuit potential to 350 mV (vs. SCE), again in 0.05 M TMAH solution. On Cu deposited Ru substrates, two anodic peaks were identified as an oxidation of Cu surface (p_1) and a stripping of whole ELD-Cu (p_2), respectively.[129] Whereas p_1 gave similar value, an increase in p_2 was observed due to the increase in the amount of Cu deposited over time. The calculated thickness values around the transition time are listed in Table 5.1. The calculation was carried out by peak area integration through −70 to 330 mV (vs. SCE), the stripping region, assuming that the Cu existed as a compact layer. The areal density and charge density of stripping the monolayer Cu used in the calculation were 1.58×10^{15} atoms cm^{-2} and 500 $\mu C\ cm^{-2}$, respectively.[130,131] Charge consumed on the surface oxidation was subtracted. The thickness was also calculated by QCM measurement in Fig. 5.4b and

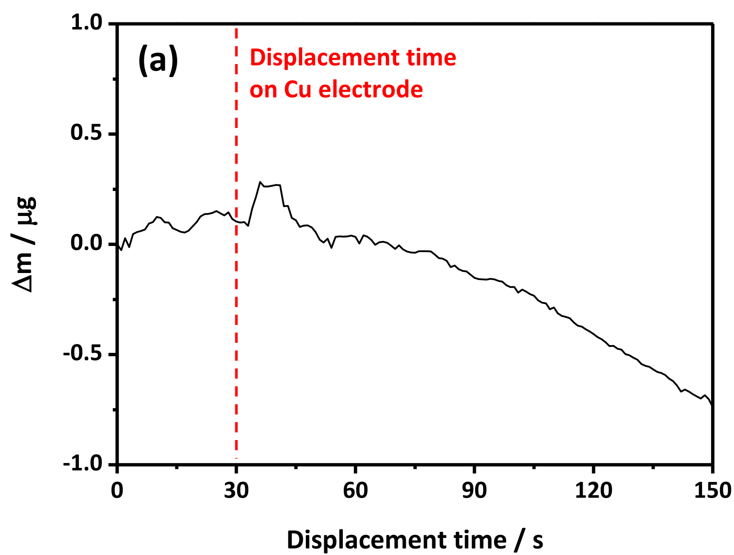
XPS analyses in Fig. 5.10. In XPS analysis, thickness was calculated using the equation as below;

$$d = \lambda_{AL} \cos\theta \ln\left[1 + \frac{(I_{Cu}/s_{Cu})}{(I_{Ru}/s_{Ru})}\right] \quad [5.14]$$

where λ_{AL} is electron attenuation length in the Cu overlayer (0.809 nm), θ denotes emission angle (53°), *I* signifies XPS signal intensity, and *s* implies elemental sensitivity factor (*s* for Cu $2p_{3/2}$ = 16.73 and for Ru $3d_{5/2}$ = 7.39).[132] By the calculation, the critical thickness where growth mode changes was determined to be 8 to 9 Å (around 3-4 monolayers, 5 s), regardless of the calculation with (electrochemical stripping and QCM) or without (XPS) applying the bulk material properties. Through the results in Fig. 5.4 to 5.7 and Table 5.1, it can be suggested that the layer-by-layer growth of Cu on Ru formed a conductive Cu layer even at the very early stage of ELD, until ca. 8 to 9 Å, and the growth mode changed to 3D islands formation as the film became thicker.

Table 5.1. Calculated Thickness of Deposited Cu on Ru

Cu ELD time / s	Thickness of Cu by electrochemical stripping / Å	Thickness of Cu by QCM / Å	Thickness of Cu by XPS / Å
3	7.90	4.93	5.76
5	8.98	8.02	8.17
6	10.15	9.65	9.30



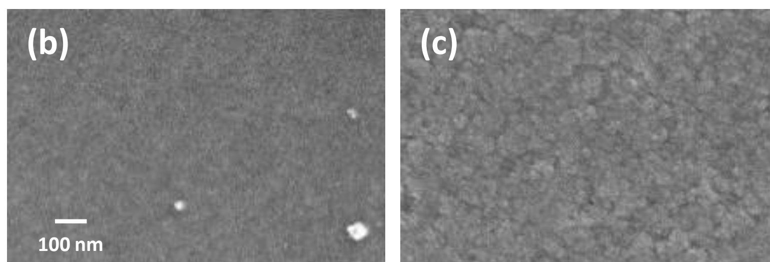


Figure 5.1. (a) QCM analysis during the displacement reaction between Cu and Ru ion on Cu electrode. (b, c) FESEM analyses of (b) before and (c) after Ru displacement reaction on Cu electrode.

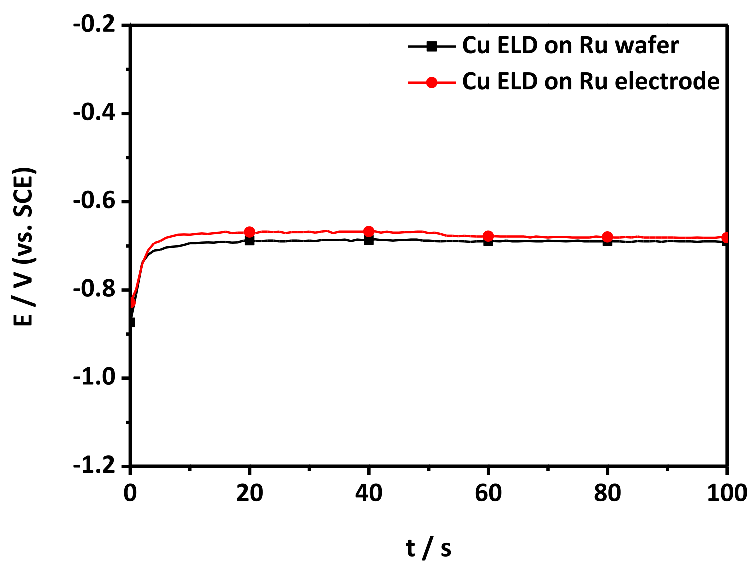


Figure 5.2. E transient as a function of the ELD time both on Ru wafer and electrode. ELD was conducted in a hydrazine based Cu ELD bath.

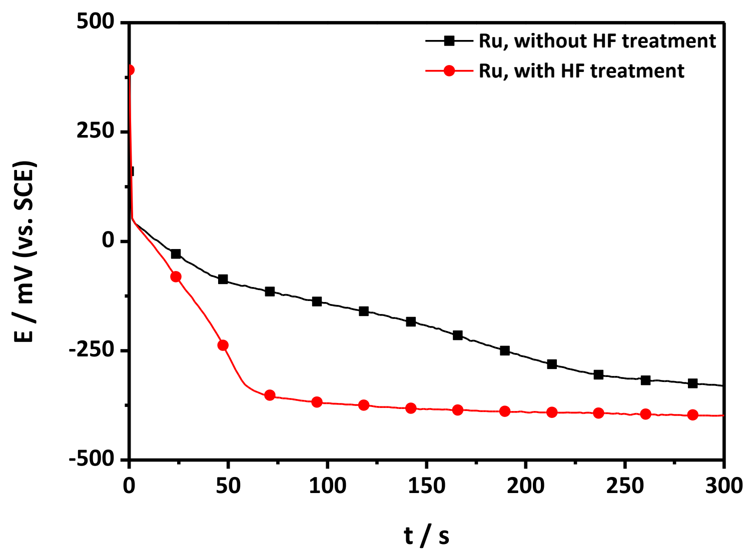


Figure 5.3. The effect of HF treatment on the potential transient during coulometric reduction of Ru surface.

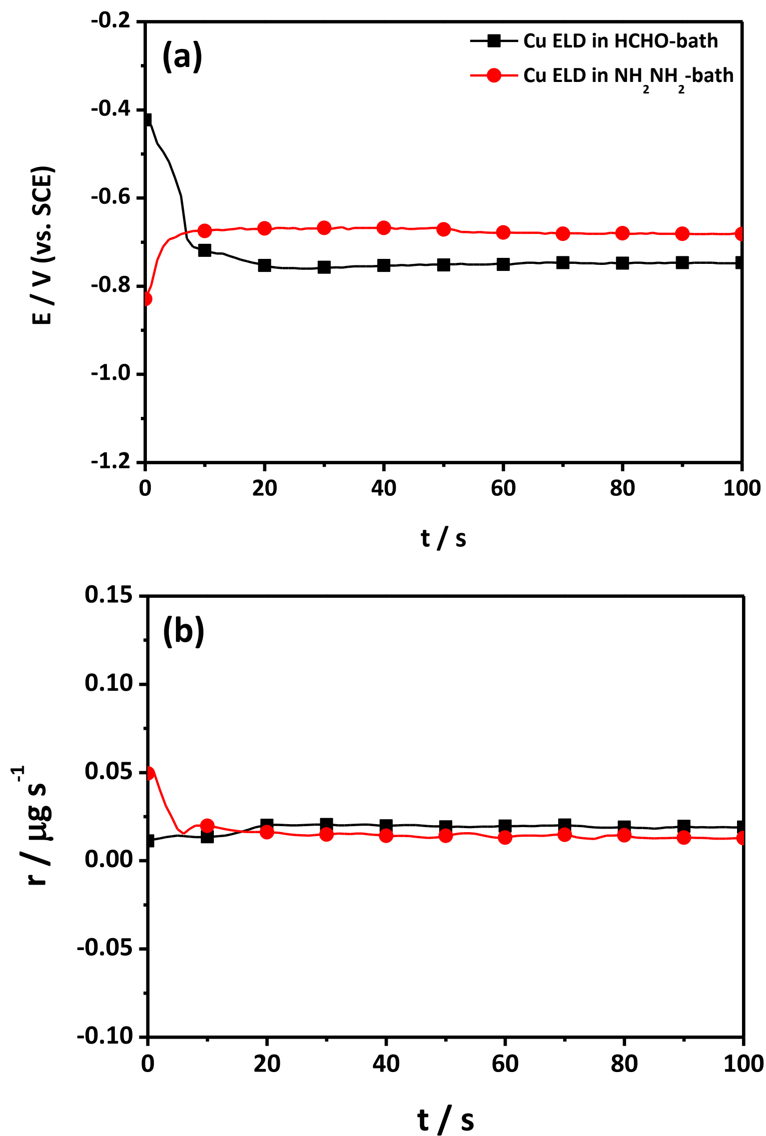


Figure 5.4. The EQCM monitoring on Ru electrode in formaldehyde or hydrazine based Cu ELD bath. Changes in (a) potential and (b) mass change rate were simultaneously recorded as a function of time.

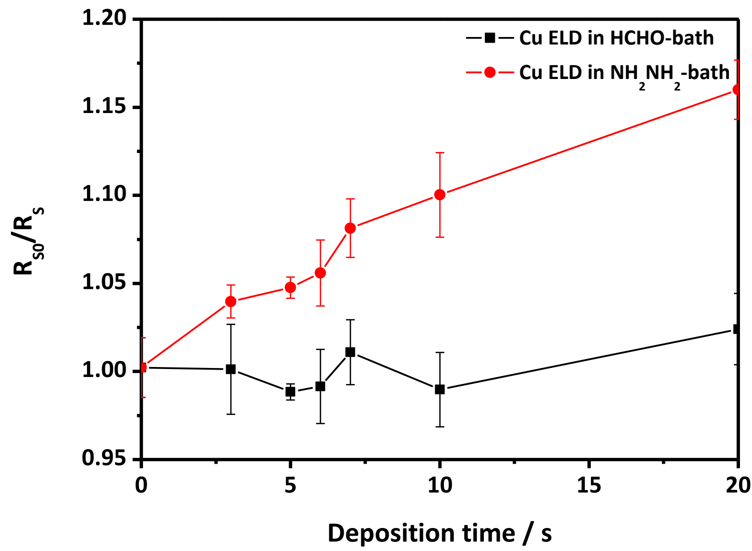


Figure 5.5. The sheet resistance ratio (R_{S0}/R_S) change of Ru substrate with respect to the deposition time in formaldehyde or hydrazine based Cu ELD bath.

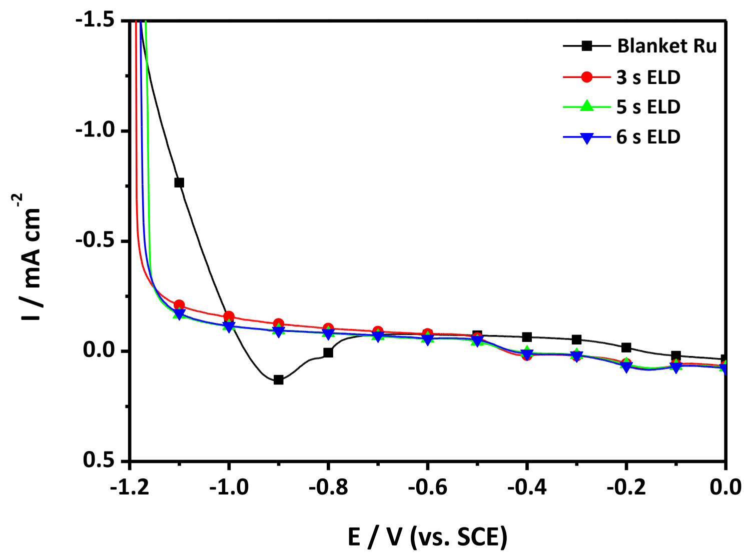


Figure 5.6. LSV on Ru and on Cu deposited Ru substrate (scan rate = 20 mV s^{-1}).

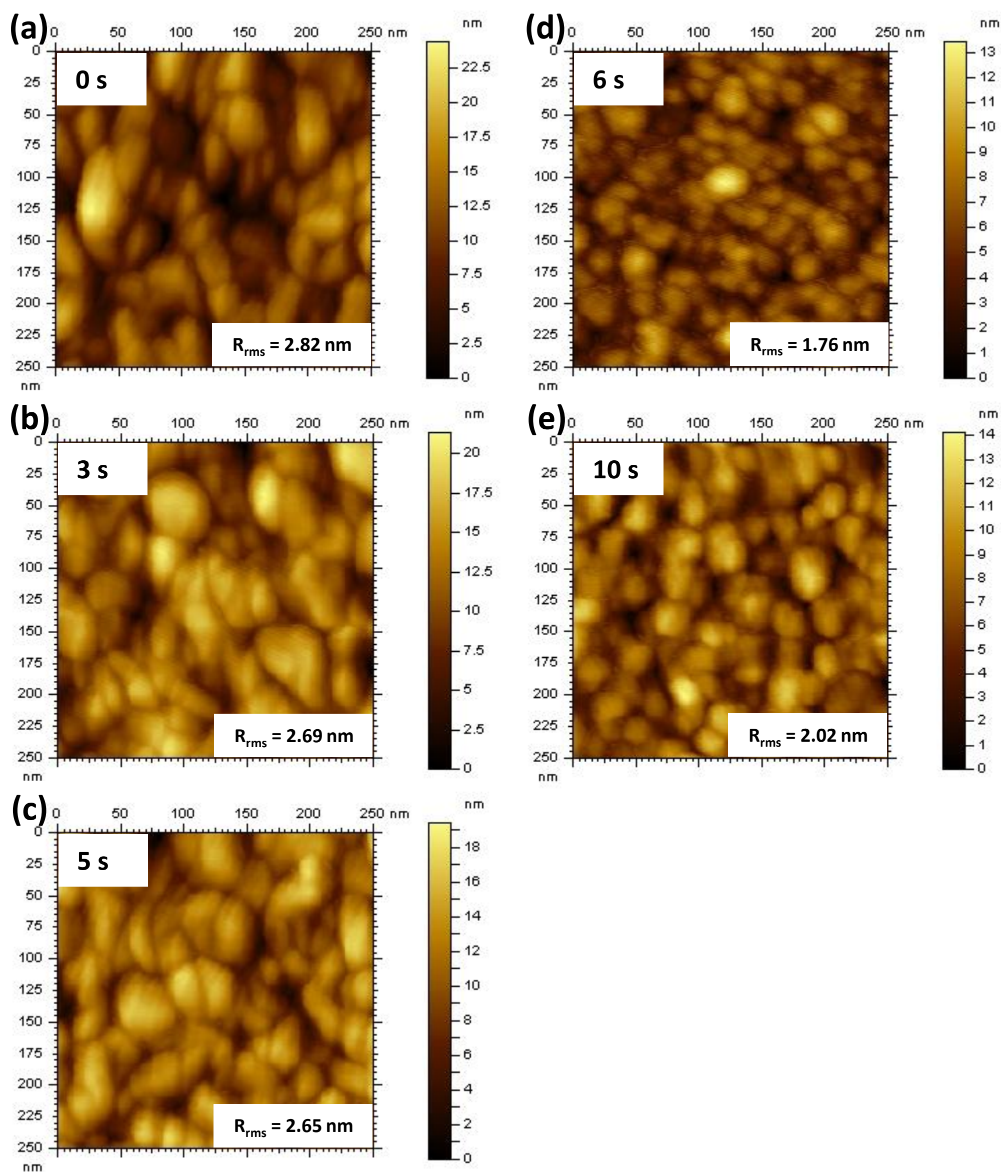


Figure 5.7. AFM morphology analyses of electroless deposited Ru according to the deposition time.

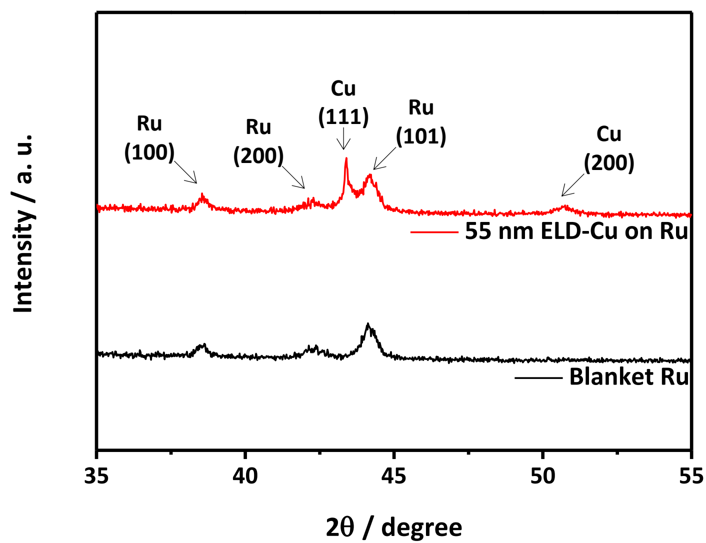


Figure 5.8. XRD analyses of blanket Ru and 55 nm Cu prepared by ELD on Ru in hydrazine based Cu ELD bath.

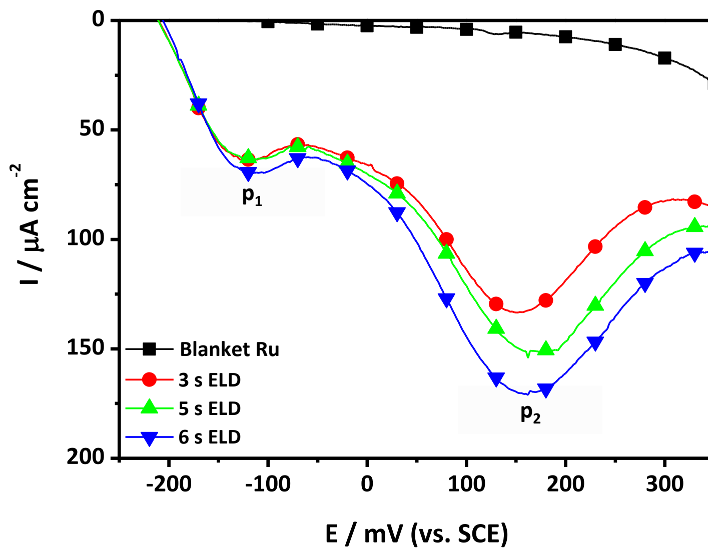


Figure 5.9. Electrochemical stripping of ELD-Cu on Ru substrate (scan rate = 20 mV s^{-1}).

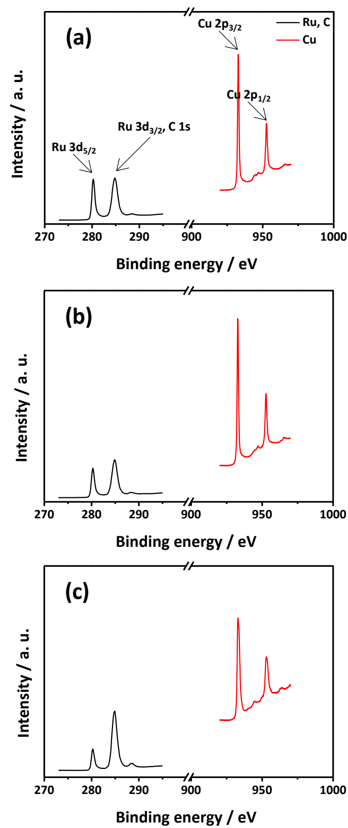


Figure 5.10. XPS spectra of (a) 3 s, (b) 5 s, and (c) 6 s deposited Ru substrate.

5.2. Trench filling by direct Cu ELD on patterned Ru substrate

The feasibility of Cu ELD on Ru as practical application for ULSI metallization was examined by gap-filling experiment. DPS and 2,2'-dipyridyl, used for the gap-filling by Cu ELD on Cu seed layer, were selected to induce the bottom-up filling.[34] Similar to the previous report, the acceleration and suppression effect according to the DPS concentration was also observed during Cu ELD on Ru substrate as in Fig. 5.11. It seemed that the Ru substrate did not much affect to the role of the additives, as the Ru surface rapidly covered by Cu. Consequently, by adding 4 mg L^{-1} of DPS and 75 mg L^{-1} of 2,2'-dipyridyl to NH_2NH_2-bath, void-free trench filling was successfully achieved as in Fig. 5.12a. High nucleation density of Cu on the whole Ru surface was advantageous for gap-filling the narrow trench. However, the thermal treatment induced the intermittent appearance of small voids near the bottom of the trenches (Fig. 5.12b). The evolution of voids would be attributed to the increased surface roughness by applying additives for the gap-filling, and the incorporated oxygen during the Cu ELD.[53,133] It is believed that the formation of voids after annealing should be resolved by the process optimization before scaling up of such a process toward the wafer level.

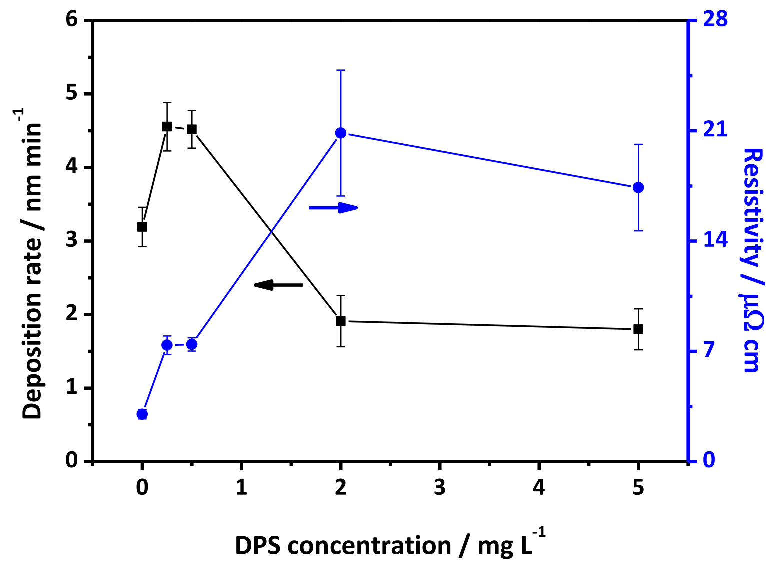


Figure 5.11. Dependence of deposition rate of Cu ELD and the resistivity of resultant Cu film on the concentration of DPS in the bath.

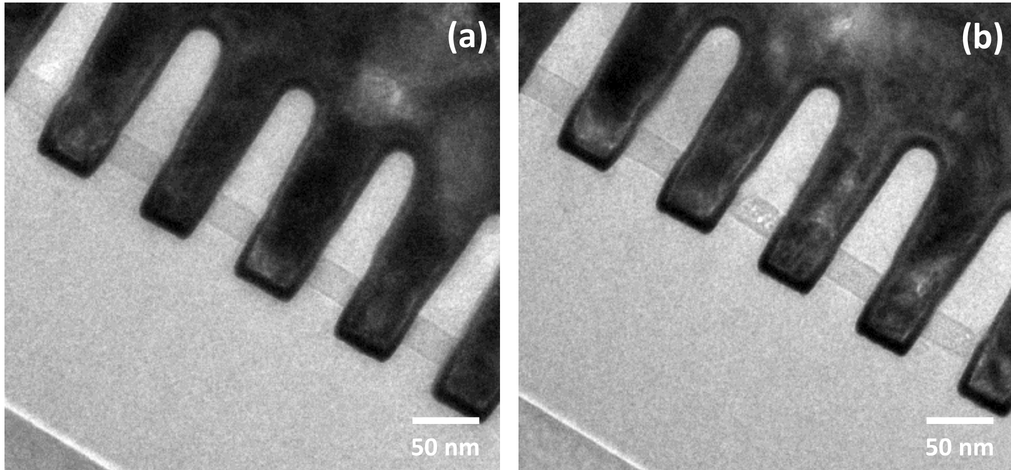


Figure 5.12. TEM cross-sectional analyses of 55 nm trenches (a) after filling by Cu ELD on patterned Ru substrate (deposition time = 40 min) and (b) after annealing of (a) at 250°C for 30 min in a N_2 atmosphere.

CHAPTER VI. Conclusions

In this study, the entire metallization processes were modified for the next-generation interconnect fabrication. On conventional Ta substrate, direct Cu ED was conducted to prepare a thin Cu seed layer by an assistance of Pd NPs. With the aid of Pd NPs as a Cu nucleation promoter, a continuous 18 (±4.8) nm Cu seed layer with an R_{rms} value of 10.7 nm was deposited on a Ta substrate after two-step potentiostatic ED process in a Cu-Pyro bath. The addition of allyl alcohol improved the uniformity of the seed layer with a reduction in the thickness to 12 (±1.2) nm and with a reduced R_{rms} value of 2.5 nm. Using allyl alcohol, a 5 nm thick Cu seed layer was also conformally formed on a 55 nm patterned Ta substrate. After the formation of the seed layer, trench filling was also realized via galvanostatic ED in a Cu-Sul bath.

ELD of various barrier layers on a SiO_2 substrate was investigated for all-wet Cu metallization. In this study, the entire fabrication process including substrate activation, barrier layer ELD, and direct Cu ED was modified. The SiO_2 substrate was activated via Pd NPs that were immobilized on the substrate by APTES-SAM. Reduction of barrier layer resistivity was achieved by applying ultrasound during the substrate activation process and by adjusting the composition of the ELD bath. The Cu ED was performed directly on the ELD layers after performing CRM, thus improving the adhesion and nucleation density of Cu on the barrier layer. The ED process was conducted in two steps:

Cu nucleation and Cu thin film formation at a high overpotential followed by additional Cu film growth at a low overpotential. As a result, a uniform, smooth Cu film covered the barrier layer. In addition, bottom-up Cu filling was accomplished on a 120 nm wide, patterned substrate with a 2.5 aspect ratio. Barrier layer performance, evaluated by using a Cu (100 nm) / electroless barrier layer (25 nm) / SiO_2 stacked blanket specimens prepared by applying the proposed method. Only the test with NiWP barrier layer was within acceptable limits, implying the importance of refractory metal incorporation on the diffusion barrier property improvement.

On Ru substrate which is considered as next-generation barrier material, Cu growth phenomena were investigated during ELD in a hydrazine based solution. Whereas the induction time was measured to be 20 s in the case of formaldehyde, hydrazine did not show the induction period on Ru, which facilitated the Cu growth phenomena observation. When the hydrazine based solution was applied, whole surface catalyzed Cu ELD occurred on Ru at the beginning of the deposition, with a distinct transition in growth mode. Before the moment of transition, the layer-by-layer growth of Cu on Ru formed a continuous film with negligible surface morphology change until ca. 8 to 9 Å. It was followed by a 3D island formation with high density Cu clusters. Considering these results, it was reasonable to assume that the Cu growth on Ru resembled Stranski-Krastanov growth, due to the strong binding energy and large lattice mismatch between Cu and Ru. Moreover, the feasibility of Cu ELD on Ru as a practical metallization process was examined by successful gap-filling inside the 55 nm trench.

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국문초록

반도체 제조공정의 발전 과정 중 전도체로서 알루미늄을 구리로 대체한 것은 가장 중요한 변화 중 하나로 여겨진다. 이 변화 과정 중 다마신 공정이라는 공정이 도입되었는데, 다마신 공정의 특징은 트렌치나 비아가 될 부분에 먼저 절연층을 형성하고 패터닝 하는 것이 선행된다는 데 있다. 이후 패턴이 형성된 절연층은 확산방지막과 구리 씨앗층으로 도포되고, 이 위에 초등각 전착 기술을 이용해 트렌치나 비아 내부에 공동 없이 구리를 채우게 된다. 이 과정 중, 확산방지막과 구리 씨앗층은 현재 물리기상증착 방법을 통해 형성되고 있다. 그러나 트렌치의 폭이 점차 감소함에 따라 물리기상증착 방법으로 형성된 확산방지막과 씨앗층의 부실한 단차도포성으로 인해 여러 문제들이 발생하고 있다. 따라서 물리기상증착을 대체할 수 있는 도금 방법으로써 화학기상증착, 원자층증착, 무전해도금, 직접 전해도금 등에 대한 연구가 활발히 진행되고 있고, 이 중 특히 무전해도금과 직접 전해도금은 습식공정이 가지는 여러 이점 때문에 더욱 주목 받고 있다.

본 연구에서는 차세대 반도체 제조공정을 위한 금속화 공정에 관련한 전반적인 개선을 시도하였다. 먼저 기존 확산방지막으로 이용되는 탄탈륨 기판 위에서는 팔라듐 나노콜로이드를 구리 핵형성 촉진제로 이용한 구리 직접 전해도금 방법을 개발하였다. 팔라듐 나노콜로이드는 폴리올 방법으로 형성되어 산화막이 제거된 탄탈륨 확산방지막 위에 물리흡착방법으로 도포되었고, 이후 피로인산염 기반의 전해액 내에서 두 단계 정전압 도금방법을 이용해 탄탈륨

기판 위에 구리 씨앗층을 형성하였다. 그러나 이러한 방법으로 형성된 구리 씨앗층은 표면이 매우 불균일하여 후속 초등각 전착을 위한 전해도금 시 공동 발생을 야기할 수 있는 문제가 존재하였다. 따라서 전해액에 알릴 알코올을 첨가하여 직접 전해도금을 실시하였고, 그 결과 55 nm의 패턴이 형성되어 탄탈륨 확산방지막이 도포되어 있는 기판에 우수한 단차도포성을 갖는 구리 씨앗층을 형성할 수 있었다. 이후 황산 기반의 전해액에서 정전류 도금 방법으로 위 패턴의 초등각 전착을 성공적으로 달성하였다.

다음으로 가장 일반적으로 이용되는 절연체인 이산화규소 기판 위에서 다양한 확산방지막을 무전해도금 방법으로 형성함으로써 금속화 공정을 실시하는 일괄습식공정에 대한 연구를 진행하였다. 이 연구에서는 표면 전처리, 확산방지막 무전해도금, 그리고 구리 직접 전해도금에 이르는 모든 금속화 공정을 개선하였다. 먼저 이산화규소 기판에 3-아미노프로필트리에톡시실란의 자가조립단분자막을 형성하고 팔라듐 나노콜로이드를 흡착시킴으로써 기판을 활성화 하였다. 팔라듐 나노콜로이드 흡착 과정 중에 초음파를 인가하는 것과 더불어 무전해도금 용액의 조성을 조절함으로써 무전해도금을 통해 형성되는 확산방지막의 비저항을 개선할 수 있었다. 이 위에 구리 직접 전해도금을 수행하기 앞서 전해식 환원방법을 실시함으로써 후속 구리 직접 전해도금 시 구리의 핵형성과 구리 막과 확산방지막 사이의 접착력을 증가시킬 수 있었다. 구리 직접 전해도금은 높은 과전압을 인가하여 얇은 구리막을 형성한 후 낮은 과전압을 인가하여 구리 박막을 성장시키는 두 단계로 구성되었다. 그 결과 균일하고 표면 거칠기가 낮은 구리 박막을 확산방지막 위에 직접 형성할

수 있었고, 120 nm의 너비에 2.5의 종횡비를 가지는 패턴이 형성된 이산화규소 기판을 본 연구에서 개발한 일괄습식공정으로 채울 수 있었다. 또한 확산방지막 특성도 이 방법으로 준비된 기판을 이용해 실시할 수 있었고, 실제 극초대형 집적회로 제조공정에의 이용 가능성을 확인하였다.

끝으로 차세대 확산방지막으로 주목 받고 있는 루테늄 기판 위에서는 무전해도금 과정 중 구리의 성장 메커니즘을 규명해 보았다. 포름알데히드 기반의 도금 용액과 달리 하이드라진 기반의 도금 용액을 이용한 경우, 무전해 도금 초기에 잠복기를 보이지 않아 성장 메커니즘 규명에 더 유리하였다. 루테늄의 경우 그 자체로써 표면 전체에서 무전해도금을 촉진하였고, 개회로전압 측정과 수정진동자저울을 통한 도금과정 모니터링 및 선형전위주사 실험을 실시한 결과 무전해도금을 통해 구리가 루테늄 표면을 수초 내로 도포함을 확인할 수 있었다. 도금 전·후 면저항 변화를 측정한 결과 도포된 구리는 연속적인 막을 형성하는 것으로 밝혀졌고, 이 과정을 원자간력현미경으로 관찰한 결과 도금 초반에 구리는 기 형성된 구리보다 루테늄 위에 더 우선적으로 성장하는 것으로 확인되었다. 이와 같이 표면 전체에서 촉진된 무전해도금을 통해 55 nm의 패턴 내 초등각 전착도 성공적으로 수행하여 본 공정이 극초대형 집적회로 제조공정에 이용 가능함을 확인하였다.

주요어: 구리, 직접 전해도금, 무전해도금, 차세대 확산방지막, 일괄습식공정
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