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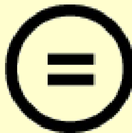

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工學博士學位論文

Improvement of Breakdown Characteristics in AlGaN/GaN Power HEMTs

電力用 AlGaN/GaN 高 電子 移動度 트랜지스터의
內壓 特性 向上

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金 榮 實

Abstract

Improvement of Breakdown Characteristics in AlGaN/GaN Power HEMT

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Gallium Nitride (GaN) based high electron mobility transistor (HEMT) or heterostructure field effect transistor (HFET) are promising device for high-power switches which has to operate in electrically and environmentally harsh condition. The devices benefits from the material properties GaN offers: high critical field, high carrier mobility and a high saturation velocity of carriers.

The breakdown voltage in AlGaN/GaN HEMTs is known to be triggered by gate leakage caused by the concentration of the electrical field at the drain-side edge of the gate electrode. The influence of gate leakage on blocking characteristics is alleviated by reducing the peak intensity of the electric field at the drain–side of the gate. There are two methods to reduce the peak intensity of the electric field: one is to decease the probability of tunneling of electrons into device active area the other is to

relieve the crowding of electric field at the drain-side edge of gate.

Nickel has been used as a gate electrode of the AlGaN/GaN HEMTs to form the Schottky contact due to its relatively high work function (5.15 eV). In this work, nickel oxide (NiO_x) was inserted as the interfacial layer between main gate (Ni) and AlGaN barrier layer for improve the reliability of the AlGaN/GaN HEMTs. NiO_x film was formed through the thermal oxidation in furnace. Material property of NiO_x film depended on the two main factors: oxidation temperature, density of the film controlled by deposition rate. Only the NiO_x film oxidized proper temperature range from 400℃ to 500℃ gave a favorable effect on the device performance. The NiO_x film with high atomic density exhibited resistive switching characteristics, which can be used for GaN based memory device. Experiments to verify the effect of NiO_x on reverse blocking operation were carried out. At the high temperature reverse bias (HTRB) test, it was found that work function of the NiO_x was maintained. Moreover, it played an important role to improve the stable blocking operation. The result of electroluminescence (EL) analysis was consistent with the results obtained from HTRB test. Leakage current of the AlGaN/GaN HEMTs with NiO_X interfacial layer measured at 200℃ was lower than that of the conventional device by 3 orders of magnitude. The breakdown voltage of the proposed device was up to 1.5 kV (1480 V).

In recent years, improvements of the overall device performance were achieved by adopting metal-insulator-semiconductor (MIS) or metal-oxide-semiconductor (MOS) structure. At the gate region, by insulating gate electrode by means of a dielectric layer, electron injection is suppressed effectively. In this work, improvement of the blocking

capability and reliability of AlGaN/GaN MIS-HEMTs employing atomic-layer-deposited (ALD) Al_2O_3 material was confirmed by experimental results. Mechanism responsible for the leakage current of the proposed device was investigated. Measured Leakage current of the fabricated MIS-HEMT was reduced to the range from sub pA (fA) to few pA. At the HTRB test, MIS-HEMT exhibited proved its thermal stability. Although drain leakage current (I_{DSS}) was increased in proportion to the operational temperature, the leakage current of the proposed device was still lower than that of conventional device by 2 orders of magnitude. Breakdown voltage of the proposed device was up to 2 kV.

Key words: AlGaN, GaN, High electron mobility transistor (HEMT), Metal oxide semiconductor (MOS), Schottky Barrier Diode (SBD), Leakage current, Breakdown, Electric field concentration, Gate dielectric, ALD, Al_2O_3

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Chapter 1

1. Introduction

1.1 Status quo of GaN power device

Recently, the development of the electric power and the wireless telecommunication industry makes the need of the high power, high frequency transistors increased steadily. The demands such as more power, (higher frequency bands) better linearity, reliability and excellent power efficiency are driving the development of the power (RF) semiconductors capable of satisfying all these specifications at a reasonable price.

Over the past few decades, many device researchers have developed many competing semiconductor devices and technologies to establish the high power, high frequency, high efficiency power systems in many commercial as well as military applications.

Power semiconductor devices play a crucial role in the regulation and distribution of power energy. By some estimates, more and more power utilized in the world flows through at least one power device. In general,

power device is the semiconductor switches used in power processing to control the electric power, transferred from the power supply through the distribution system shown in Fig.1.1, to the many kinds of load used for home applications (white goods) and PCU (power control unit) for industrial high voltage equipment [1]. As the vehicle have become high-tech, automotive electronics equipped in the manufacturing process have increased drastically. These electronic modules are controlled by smart power chip where many discrete power devices are integrated (Fig. 1.2). In recent years, hybrid vehicles (HVs) have emerged as an alternative for the next generation transport. Even now, it is evolving into its ultimate form of electric vehicle (EVs) according to technical road map (Fig. 1.3). In electric vehicles, high performance power supply of drive electronics is an essential component that impact the overall system of is based on high performance (Fig. 1.4). The performance of the power supply depends on the highly reliable power discrete devices that compose the power supply. This technical transition in automobile makes automotive field an emerging market for power semiconductor with the higher growth potential than existing market. Consequently, power semiconductor is indeed as well as in name inevitable element in the overall macro and microelectronics.

After the invention of the transistor in 1947, there are many semiconductor materials such as Si, Ge, SiGe, GaAs, InP, SiC, GaN and so on. And there are still countless efforts for the invention of semiconductor materials with material properties which outperforms that of the existing materials. Among the several semiconductors, silicon has long been in the dominant position of semiconductor material for the various devices.

Almost 90% of the commercial semiconductor product, unexceptionally in power semiconductor device, is made of the silicon. The broad use of silicon is due to the competitive advantages compared with other materials such as the abundant amount, ease of doping process and the existence of good and stable insulator [2]. Si-based devices using most common structure including LDMOS (lateral double diffused metal-oxide-semiconductor), VMOS (vertical channel MOS), Super-junction MOS, MCT (MOS controlled thyristor), IGBT (insulated gate bipolar transistor) have established a well-reputed position in the high-voltage power devices [3]. In the high speed devices, Si LDMOS was covering about 90% of high power RF applications in the 2GHz frequency range; the remaining 10% market share was addressed by GaAs technology such as GaAs high electron mobility transistors (HEMTs), hetero bipolar transistor (HBTs) [4].

However, even though many advantage of the silicon, silicon technology has matured to the extent that intrinsic material parameters limit the performance of devices. To sustain high breakdown voltage, Si-based device should have an extra epi layer capable of depletion region. Thick epi layer means inevitably long drift region of the device, which is unfavorable in the perspective of the power loss due to its high on-resistance ($R_{on\text{-}sp}$). In the frequency range of interest (2-20 GHz), Si-based high speed devices are also inherently limited by material parameter such as inversion layer mobility and saturation velocity. Further improvement in the speed of the Si-based device is based on the decreasing dimension of the gate into nanoscale through the development of better lithographic tools and from using Si based alloy such as Si-Ge [5].

The necessity to realize the faster and electrically robust devices to sustain higher breakdown voltage than ever has been one of the strong motivations for the development of the three terminal devices to satisfy aforementioned features by exploiting novel properties of the III-V semiconductors. During the last two decades, researchers and developers have made tremendous progress in Gallium Nitride (GaN) for a vast spectrum of applications. Development of advanced epitaxial growth technique such as metal-organic chemical vapor deposition (MOCVD) and molecular beam epitaxy (MBE) have been the basis for many GaN-based devices with highly improved or novel properties. In the field of optoelectronics, one of the main application field, light emitting diode (LED) utilizing GaN has broaden the boundary of the light spectrum covered so far by commercial LED product to blue and ultra violet area. When it comes to other applications, albeit small portion in the whole applications, broad range of applications such as attenuator, mixer (oscillator) even memory and logic circuits have been realized by means of GaN-based devices [Fig.1.5]. But switching devices for high power and high speed is what attracts the most interest [6].

GaN has been the material of choice for the power switch that handles high power and operates faster under harsh ambient condition. When it comes to GaN-based transistors, heterostructure with nitride-based binary or ternary compound (AlGaN, AlN, InGaN) has received a lot of interest. GaN-based HEMTs is field effective transistor (FET) which is a voltage controlled unipolar device. The control electrode is capacitively coupled to the active region of the device, the channel carriers are spatially separated by another heterogeneous wide bandgap layer. Due to

its material properties suitable for the both high power and high speed operation (specific physical features will be explained next chapter), it has emerged as a very promising, long-term contender to other viable technologies for solid-state high power, high frequency device. Many research groups are intensively working on AlGaN/GaN HEMTs to hold the dominant position in various technologies from Epi-growth to design of the device structure.

The AlGaN/GaN HEMTs, representative of the nitride electronics, have evolved rapidly form the first demonstration in 1993 to today's high performance commercialized devices. This tremendous evolution been made on the development of the epi-growth technique. From the embryonic stage, the Epi-growth technology of planar AlGaN/GaN heterostructure has been led by MOCVD (metal organic chemical vapor deposition) rather than MBE (molecular beam epitaxy) method. In the academia, professor Umesh Mishra and his research group at UCSB (University of California Santa Barbara) have the relatively unique position of being very strong in material growth of nitride semiconductors, in device processing and understanding of devices properties from the early stage of the gallium nitride (GaN) field. In the initial stage of the material growth and their applications to AlGaN/GaN HEMTs, two substrates have dominated: sapphire and SiC. Sapphire is the traditional substrate for MOCVD of GaN, and it is responsibly cheap at ~100$ per 2 inch wafer. The drawback of sapphire substrate is its low thermal conductivity, which makes it difficult to dissipate heat generated during high current operation. The alternative substrate, SiC, was for long not suitable for RF devices, due to the electrical conductivity in the

substrate. In 1999 the first semi-insulating SiC substrates became available, and SiC has since become the leading substrate for high-power devices, due to this high thermal conductivity. High cost is the major drawback for SiC: currently semi-insulating 4H-SiC retails for ~4000$ per 2inch wafer, which is about 40 times the cost of sapphire [7]. The high cost of the epi-wafer due to substrate has been a hurdle to the development of the growth technique and their applications to HEMTs. Therefore many research groups made ceaseless efforts to minimize the cost of producing epi-wafer. As a part of the effort, they started to use Si as a substrate on which GaN is grown even though large lattice mismatch between Si and GaN. Lots of experiment on GaN grown on Si substrate has been carried out to this day. As the yield of the process goes up, the potential of cost-reduction becomes great. The price competitiveness of the Si-based epitaxial technique and performance advantage of the GaN-on-Si devices made many global GaN manufacturers emerge on the GaN market.

GaN technology is evaluated not mature yet for implementation within consumer-like business in power semiconductor industry (discrete, module and IC's) by some research institutions analyzing and forecasting technical progress and surveying market trend such as Yole Développment (Lyon, France). However, albeit obstacles such as expensive material cost and inherent factors to limit device performance, GaN technology recently moved beyond the university-level development phase into the commercialization stage by providing customers with capabilities that may be out of reach of present semiconductor materials.

Industry confidence in GaN technology has increased with more semiconductor companies announcing GaN development project.

It is the development of the material growth of gallium nitride that brings many companies into business area. GaN grown on Si should take a dominant position, thanks to many advantages favorable to the commercialization: its cost competitiveness, the availability of 6 inch (150mm) wafers, even up to 8 inch, with thickness of epi layer over 7μm under qualification and compatibility to Si process for back-end process. The well-reputed wafer producing companies such as AZZURO (German), EpiGaN (Belgium), NTT-AT (Japan) currently supplies 150mm GaN-on-Si epitaxial wafer [Fig. 1.6] [8]. The most of them have a capacity to develop 200mm GaN wafer within 2012 and also have a plan to commercialize according to customer demand. IMEC, Belgium's giant semiconductor research center, announced Au-free CMOS-compatible AlGaN/GaN HEMT device processed on 200 mm Si substrates in 2011 [Fig. 1.7]. One of the challenges working with GaN-on-Silicon is apparently wafer bow, and to manage this they used thicker 1.15 mm wafer, which gave an acceptable less than 50 micron bow [9]. In general, power device makers usually buy polished silicon wafers, conduct the epitaxy (or buy Si epi-wafers), then process the devices. This model is roughly the same for SiC technology. New GaN producers, however, may not integrate metal organic chemical vapor deposition (MOCVD) GaN epitaxy, instead buying GaN epi wafers and processing them in existing CMOS lines. Alternatively, new entrants could fully integrate the GaN process, from the bare silicon, GaN epi, and front-end fabrication.

In 2012, the GaN power semiconductor market is relatively small with only two major device suppliers. However, now many entrants have appeared in GaN market; existing silicon-based electronics suppliers developing GaN technologies and LED makers diversifying capability to make power electronics. In 2013, now many player in the GaN market such as International Rectifier (IR), Efficient Power Conversion (EPC), Transphrom in United states and AZZURO (German), MicroGaN (German) , EpiGaN (Belgium) in Europe and NTT Advanced Technology (NTT-AT), Furukawa electronics, Fujitsu, NEC, Panasonic, Sanken Toshiba, Powdec in Japan and other many small-medium size companies are ramping to production [table 1.1][10].

Among them, some component suppliers have begun to offer GaN products used in the power management chip since 2005. At that time, it was customized product rather than off-the-shelf. However, some pioneers showed there was a trend to globalize the GaN manufacturing industry with the lapse of time. One of main two vendors in early stage of GaN market, International Rectifier Corp. (El Segundo, Calif.) have already released the prototype of GaN product `GaNpowIR™′ in 2008 and the first GaN commercial product `ip2010′ which is a high frequency, switching power stage solution consist of GaN power transistor die and a silicon controller ASIC die for step-down buck application according to its GaN technology Point-of-Load (POL) [Fig. 1.8] [11]. And the other, Efficient Power Conversion Corp. (El Segundo, Calif.) introduced its first enhancement-mode GaN on silicon FETs (eGaN) produced in high-volume using standard silicon manufacturing facilities. Its commercial products EPC series named as EPC1001, EPC1010, EPC1015 is in the progress of

evolution to the limit of GaN [12]. Transphorm, a gallium nitride power start-up and the first company to achieve JEDEC qualification for its GaN-on-Si devices, announced its first fully-qualified commercial GaN HEMT devices whose blocking voltage and specific on-resistance (R_{DS-ON}) is 600 V and 310 mΩ respectively, at the end of 2012. And next year, at the 2013 ARPA-E Energy Innovation Summit, Transphorm announced the world's first GaN-based high power converter which is 4.5 kW PV (photo voltaic) power converter powered by 600 V GaN half-bridge module with its costumer-partner Yaskawa Electric. This is a milestone in adoption of GaN technology in power conversion [13]. In Japan, Fujitsu Semiconductor announced that it has achieved high output power of 2.5 kW in server power-supply units equipped with GaN power devices on Si at Nov. 2012 and will start volume production of the GaN power devices by the second of 2013 [14]. Sanken is also known as a player in commercial GaN product. In Korea, Samsung Electronics, well-known for its memory business, jumped into the GaN power device market on the basis of its material growth technology accumulated in GaN LED business and advanced semiconductor-processing technology few years ago. At the International Symposium on Power Semiconductor Devices and IC's (ISPSD) 2012, it exhibited for the first time its enhancement-mode GaN HEMTs device by employing a 70nm-thick p-GaN layer selectively grown under gate electrode for normally-off operation. The information Samsung released about their GaN HEMT device was quite impressive. The threshold voltage of the device was 3 V, specific on-resistance ($A{\cdot}R_{ON}$) was as low as 2.9 mΩ-cm^2, breakdown voltage of the device was 1.6 kV and the Figure of Merit (FOM) was calculated to be 921 mV/Ω-cm^2, which

was the highest value reported so far for the E-mode GaN device according to their claim [15]. However, its GaN technology is far from the commercialization, with being on R&D stage now.

GaN technology is maturing and now offers transistor, diode and even ICs compatible with power electronics expectations, at least in the 0~600 V range. $16.6 billion market size is envisioned [16]. As shown in Fig. 1.8, many global players of the GaN power electronics (including epi growth, discrete, module) have already released their fully-qualified products on the power device market. Almost commercial GaN products currently on the market are targeting in the low to medium voltage sector. Devices in this sector should satisfy such specifications as few-ampere (A) current handling capability and ~600 V blocking voltage range, which has been the operational domain of the Si power MOSFET. Considering the GaN current state-of-the art, promising application range where commercial GaN products with blocking voltage range ~600 V can be used is from the power supply for IT electronics, home appliance to non-customer product such as PV inverter for solar sector, UPS, RF power station and motors control etc [17]. For GaN technology, it is still far from entering into the medium to high voltage applications used in power system of the Train, Avionic, and electric vehicles (EVs) due to its immaturity and limiting factors. Si IGBT account for $1.6 billion in this sector in this market. In the high voltage sector up to 1.2 kV, many leading research groups, academia and industries are working on, however, commercial devices with V_{BR} over 600 V is not available yet [Fig. 1.9]. Although the market size of the current GaN device is a small share of the silicon dominated power electronics, it is envisioned that GaN technology will encroach on

the power semiconductor market in the near future.

Due to the great effort of many global GaN companies to improve the GaN technology, GaN technology hold its place in the global power semiconductor market with broadening the scope of applications and diversifying industrial categories. According to IMS report issued in 2010, it is predicted that application segment and its market size of GaN device will undergo a change by some factors such as global renewable energy policy and needs of specific industry. The reality of the GaN market in 2013 corresponds to its prediction more or less [Fig. 1.10].

The market for power devices implemented in gallium nitride was less than $2.5 million in 2011, according to market research firm Yole Développement (Lyon, France). However, there was a great deal of R&D activity and Yole saw the power GaN market growing to nearly $12 million at the end of 2012 and $500 million in 2016. The company makes this prediction in its report entitled Power GaN-2012 edition.

2013 should be a turnaround year for GaN power electronics devices, according to analysts. That year should see a switch from qualification to production ramp-up for several companies to enter the GaN power electronics devices. As a result, the GaN device market could reach $50 million. In 2014, most of these new GaN power electronics companies will ramp up their production capacity. By 2015, the availability and adoption of fully-qualified GaN devices with at least 600 V breakdown capability will spur growth of the market and open doors to non-consumer applications by the which time, up from only two this year, the number of companies involved in GaN power electronics should grow from 12 to 15.

These companies should be sharing consumption of more than 100,000 6-inch epi-wafers [18].

Beyond 2015 the qualification of GaN device for the electric vehicles (EVs/HEVs) sector would allow the GaN device business to approach $1 billion and may exceed $1 billion in annual value by 2019. The forecasted revenue for GaN power semiconductors is $1.75 billion by end of 2022 (after 9 years) at an explosive Compound Annual Growth Rate (CAGR) of 63.78% from 2012 to 2022. The phenomenal growth rate of approximately 60 to 80% year-on-year is expected to continue for the following years. Apart from power semiconductors, GaN is predominantly used in optosemiconductors, for LEDs and laser diodes. The total GaN semiconductors (including both, power and optosemiconductors) market revenue is expected to reach $2.6 billion by 2022 according to Philippe Roussel, power electronics business unit manager at Yole [Fig.1.11] [19].

Table 1-1 Main manufacturers of GaN epi-wafer and related applications (devices) [Source: Power GaN report, Yole Développment, Feb. 2012]

Company	GaN epiwafer	GaN device
AZZURRO (GE)	X	
BeMiTec (GE)		FL
Dowa Electronics Materials (J)	X	
EPC (US)		X
EpiGaN (B)	X	
Furukawa (J)	X	X
GaN Systems (CA)		FL
International Rectifier (US)	X	X
MicroGaN (GE)		X
NTT (J)	X	
OnChip Power (US)		FL
Panasonic (J)	X	X
Powdec (J)	X	X
Sanken (J)	X	X
Sumitomo SEI (J)	X	X
Toshiba (J)	X	X
Transphorm Inc. (US)	X	X

FL: Fab-less business model. Design only

Power GaN pure-players

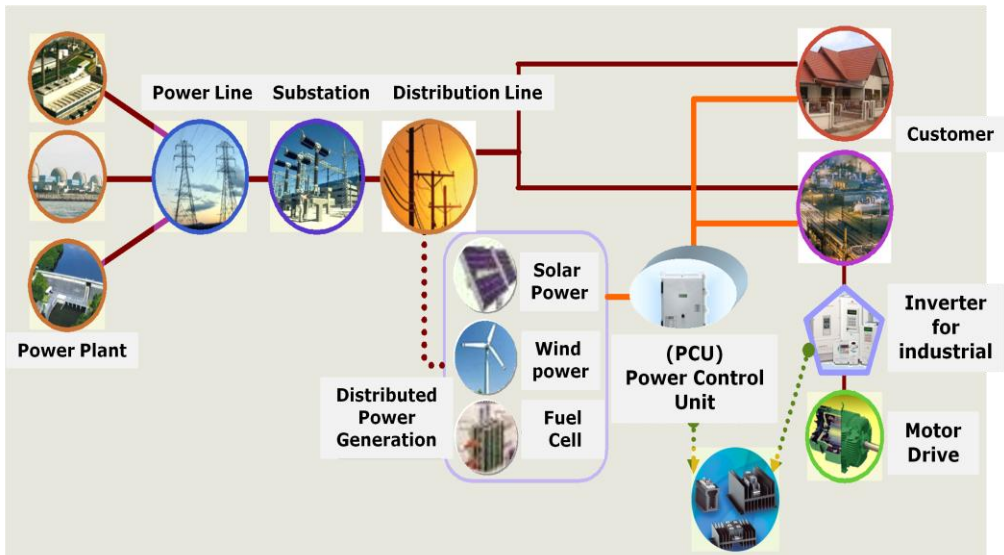


Figure 1.1 Schematic diagrams illustrating generation and distribution of the electric power.

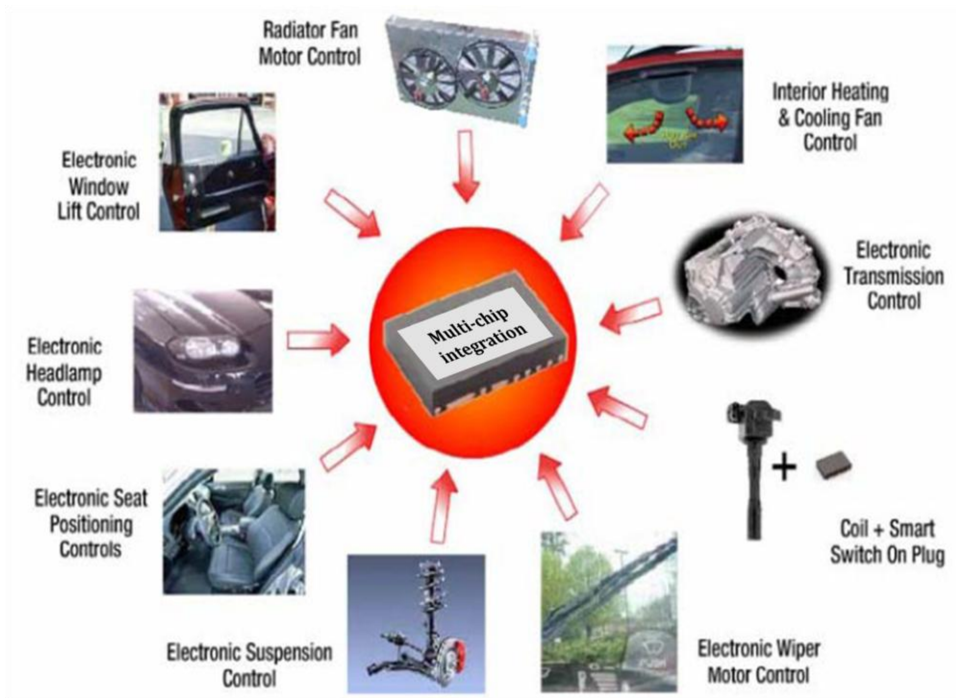


Figure 1.2 Electric parts of the automobile controlled by power manage chip.

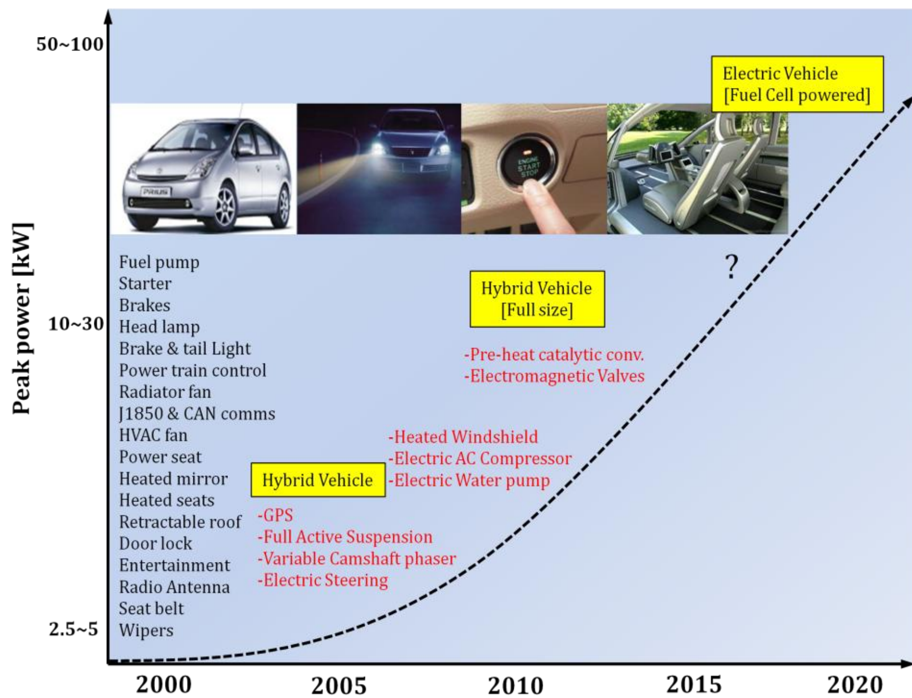


Figure 1.3 Development of the electronic components equipped to automobile.

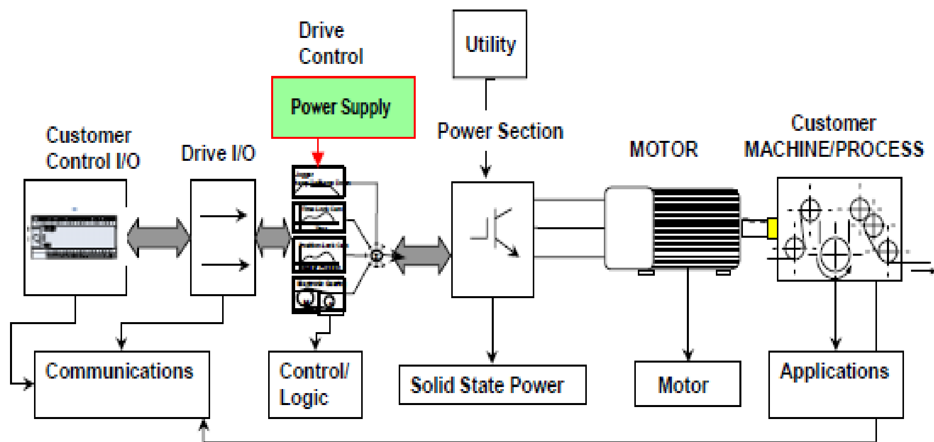


Figure 1.4 Schematic describing the components of typical motor drive system of the electrical vehicle.

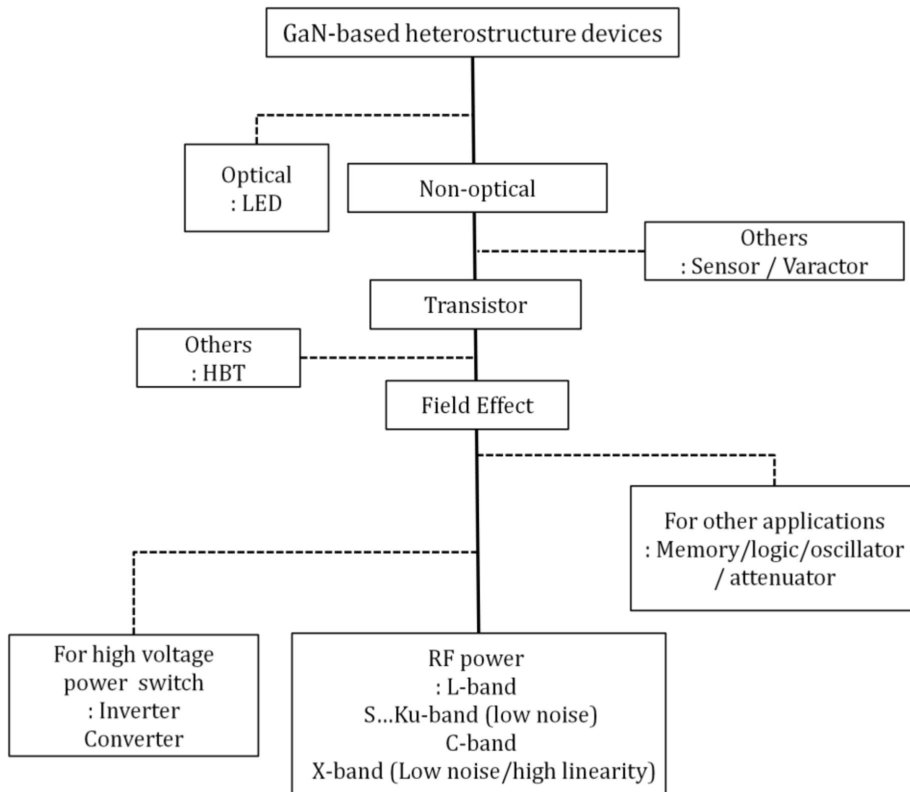


Figure 1.5 Taxonomy of GaN-based heterostructure devices [3].

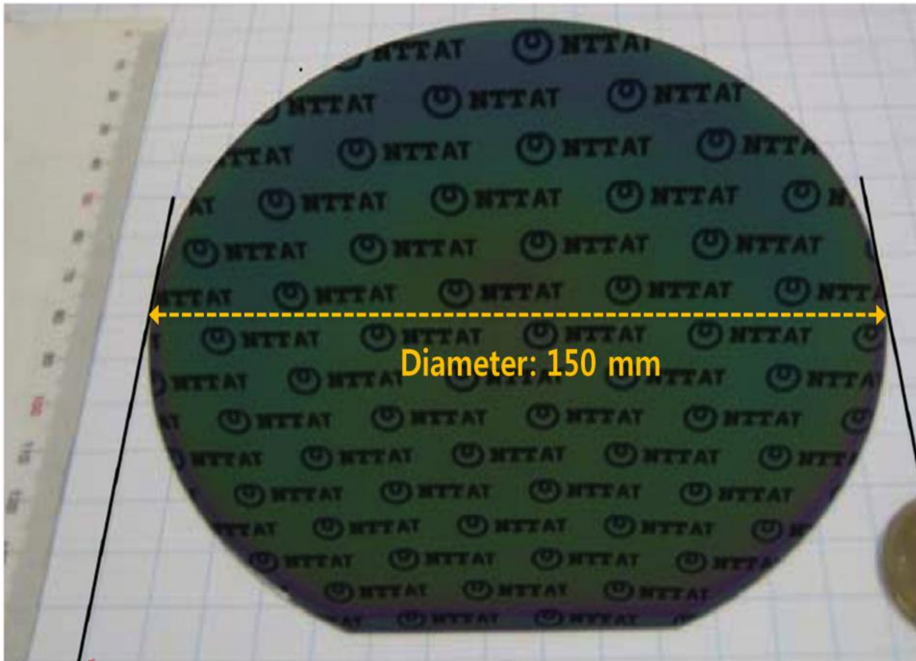


Figure 1.6 6-inch GaN-on-Silicon wafers with an AlGaN/GaN HEMT epitaxial structure. [Source: NTT-AT]

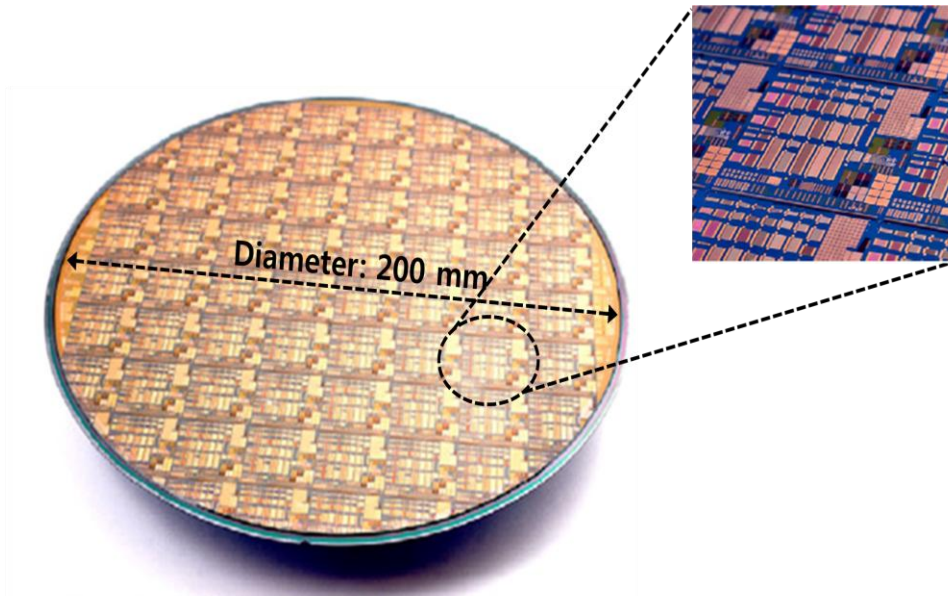
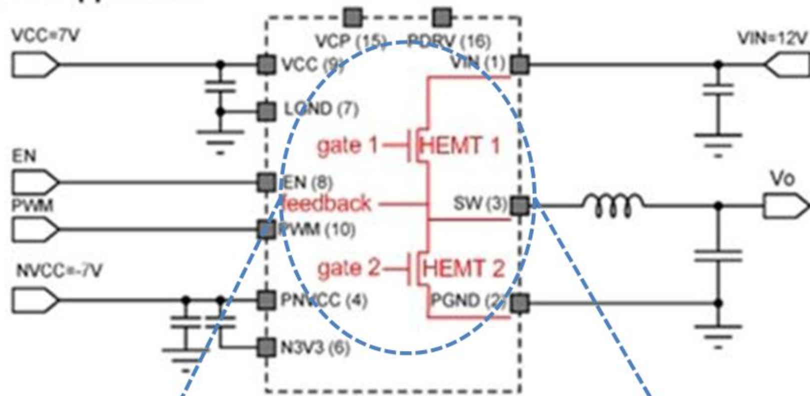


Figure 1.7 IMEC's Au-free CMOS-compatible AlGaN/GaN HEMTs processed on 200 mm Si substrates and die.



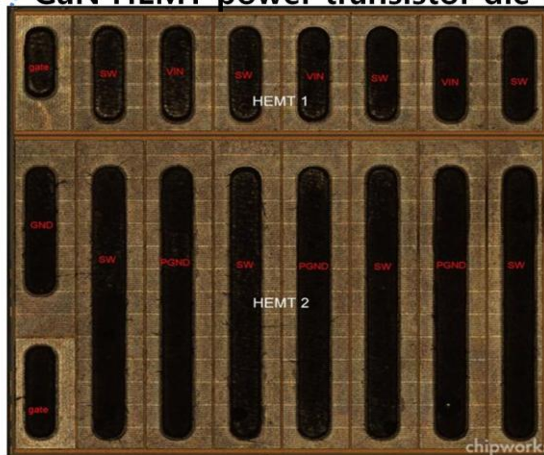


Figure 1.8 Simplified Schematic of iP2010 application (commercial product of International Rectifier) and photograph of GaN HEMT power transistor die.

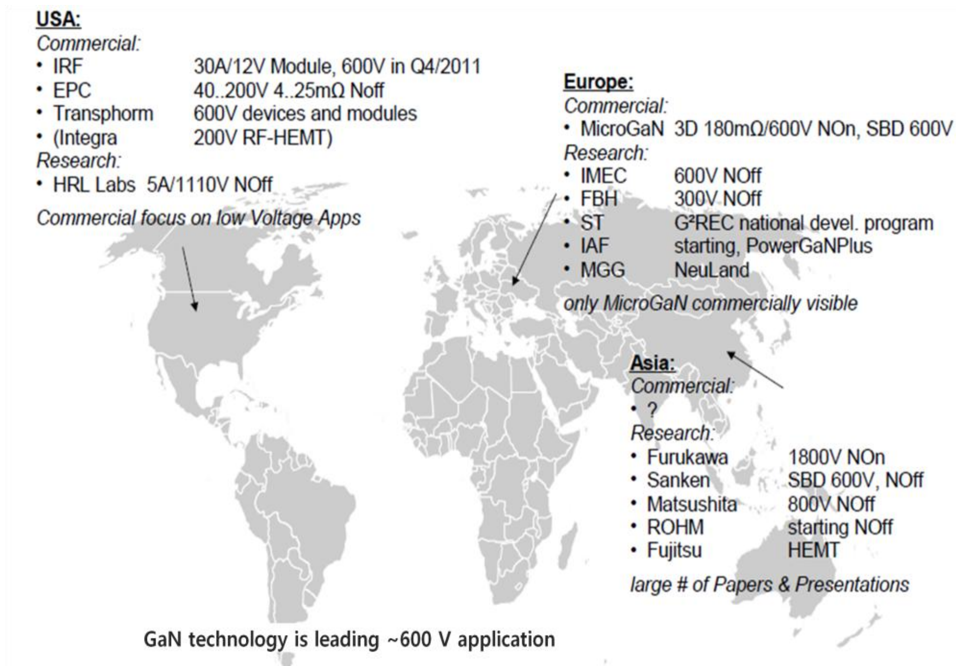
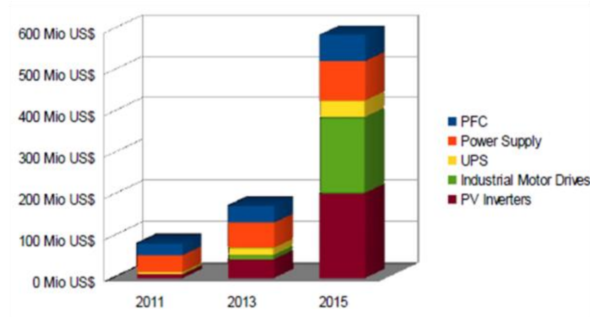


Figure 1.9 Geographical positioning of the global players of GaN power electronics and its commercial products.

Figure 1.10 Fields of applications for GaN power devices and target applications of commercial GaN products.



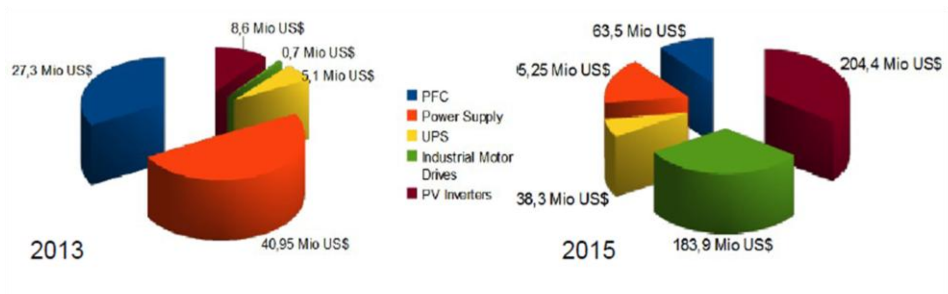


Figure 1.11 Application segments of the GaN-based devices.

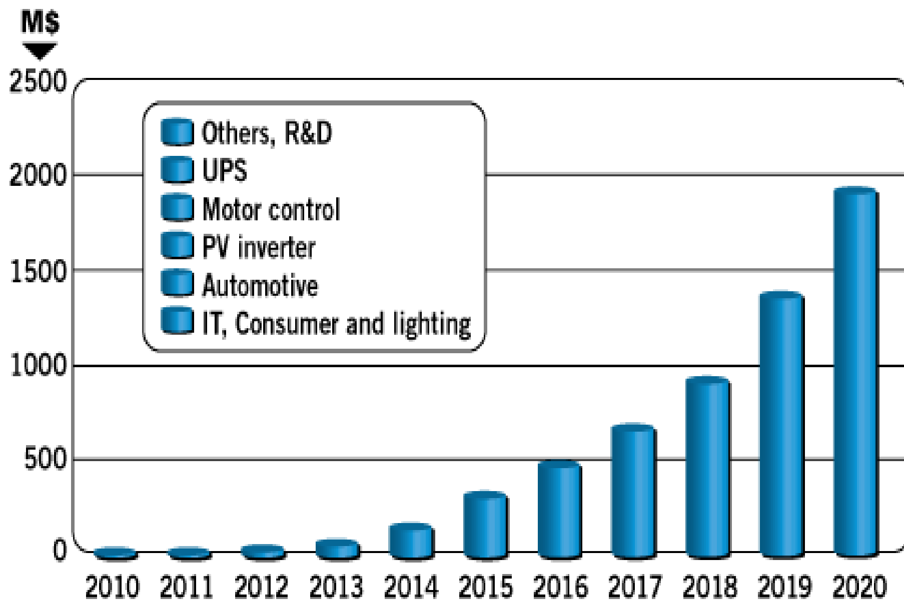


Figure 1.12 GaN device market size and list of applications sectors. [Source: Yole Power GaN report, March 2102]

1.2 Research Background

The power electronics industry has dealt with conversion and motion, and thus requires lighter, smaller, cheaper and more efficient systems. It is well recognized that the improvements in the system performance in terms of efficiency, size, and weight are driven by enhancements made in semiconductor device characteristics. The ideal semiconductor device required for such an efficient system should realize the low on-resistance, fast switching speed, high breakdown voltage and wide safe-operation-area (SOA). Power devices used in systems can be broadly classified into two categories: power rectifier and power switches.

Up to date, power discrete market including semiconductor devices, modules and ICs has been dominated by silicon for a long time due to the advantages silicon technology had: abundance of the material; easy doping; existence of stable insulator [20]. Silicon technology, however, are approaching the theoretical limit of performance (Fig. 1. 13) [21]. There have been efforts to push beyond limits of Si by novel devices structures like such as RESULF (reduced surface field), Superjunction MOSFET [22-23]. However, it looks tough to overcome the inherent limits by introducing new device structure. For instance, in order to minimize the power loss in the Si power MOSFET, there should be a trial to reduce the on-resistance by increasing the device die size. In the light of high-frequency operation, increased die size causes the input capacitance to increase. This results in corresponding increase in switching losses, which offsets the reduction of conduction losses achieved by the decrease

in the on-resistance. Consequently, it is necessary to reduce the specific on-resistance ($R_{ON\text{-}SP}$, on-resistance per unit area, usually, square centimeter) with keeping the same die size.

At the same time, wide bandgap semiconductors, particularly SiC and GaN emerged as a new candidate for power device because they offer many potential advantages over silicon devices in the areas of switching, operation temperature and blocking voltage. These potential advantages arise from the fundamental physical properties of the material. Unique material properties such as wide bandgap, lower intrinsic carrier density, higher breakdown (critical) field, higher saturation velocity and higher junction temperature guarantees many features favorable to high power operation when the device is made by these materials. The comparison of key electronic properties for the semiconductors is shown in table 1-2 [24].

GaN has saturated electron velocities (V_{sat}) of 2.5×10^7 cm/s and a energy band gap of 3.4 eV that leads to a critical breakdown filed (E_C) of 3.5 MV/cm, as well as stability at high temperature. In addition, heterostructure with another nitride compounds (AlGaN, AlN) which have the wider band gap than GaN allows very high density electron channel (n_s of 1×10^{13}) near the interface and high electron mobility (μ_n: 1500~ 2000 cm^2/Vs) in channel. A high $n_s\cdot\mu_n$ product results in low on-resistance (R_{ON}).

Recently, these potentials that wide bandgap materials have are getting closer to reality because of significant improvement in epi-growth and

process technology for SiC and GaN. SiC switches with blocking voltage of kilo-volts and current density of 1 kA/cm^2 have been demonstrated. GaN HEMTs have moved to the stage of commercialization from the phase of research in academia. Diamond is also expected to be next-generation semiconductor device for high power applications due to its superior material properties to that of gallium nitride. However, diamond has drawbacks such as difficulty of doping and high activation energy. These problems should be resolved to join the ranks of materials for next-generation power devices [25].

To compare objectively theoretical limit of semiconductors from the material property point of view, various figure of merits (FOMs) have been proposed. The figure-of-merit is the most widely used criteria, combined with common material parameters, to evaluate the performance of device which specific material is made by. In 1965, Johnson introduced the figure of merit,

$$\text{Johnson's figure of merit (FOM)} = \left(E_C \cdot V_{sat} / \pi\right)^2$$

, which was the power-frequency product [26]. E_c and V_{sat} are the critical field and saturation velocity. The critical field and saturation velocity limit the performance of typical devices in the Johnson's FOM.

The devices for high power switch need a minimum breakdown voltage which is as twice as the operation voltage at least in order to operate with reliability. The drain to gate voltage ratio (V_{DS}/V_{GS}) should be high to reduce the power loss consumed by the driver. The on-resistance of the switch ought to be as low as possible to reduce the conduction losses

during on-state of the switch. Under the assumption that power losses are only responsible to conduction losses, Baliga introduced another figure of merit, called Baliga's figure of merit (BFOM), for vertical power field effect transistors in 1982.

$$\text{Baliga's FOM} = V_{BR}^2 / R_{on} \sim \varepsilon \cdot \mu \cdot E_C^3$$

Where μ is the mobility and E_C is the critical field.

The switching losses generated during the turn-on and turn-off time should be as low as possible. This is important for switching operation at higher frequencies. The loss in power conversion system is mainly attributed to these two losses (conduction and switching losses). The conduction losses can be reduced to some degree by decreasing device area or die size. However, increased device area results in increase in capacitance and increase in switching losses. Consequently, at a given switching frequency, total loss can be minimized by choosing the optimum device area. For any given device area, the switching losses increase proportionally to switching frequency. The correlation between parameters to determine power losses of the switching device is led to high frequency figure of merit [27-28].

$$P_{loss(Min)} \sim \sqrt{f} / (\sqrt{\mu} \cdot E_C)$$

Various figures of merit of wide bandgap semiconductor materials are summarized in table 1-3 [29] and in Fig.1.14. From the table and figures, advantage of GaN and AlGaN/GaN heterostructure over SiC is clearly illustrated.

For a complete understanding of the advantages of the GaN in terms of device, Actual Si-based vertical power devices such as IGBT are illustrated as an example (Fig 1. 15). Under the assumption of one-sided abrupt junction, breakdown voltage (V_{BR}) of the IGBT is roughly equal to one half of the product of two factors: critical field; width of depletion region. If the IGBT is made of GaN, the width of depletion region required to sustain the same blocking voltage will be reduced by one-tenth due to its high critical field. Thickness of epi layer can be reduced according to the reduced depletion region. From a commercialization perspective, GaN-based vertical power device has great price competitiveness. It can be also demonstrated through the equation for breakdown voltage represented as

$$V_{BR} = \frac{1}{2} W_D \cdot E_C = \frac{\varepsilon \cdot E_C^2}{2q \cdot N_D}, \text{ where } W_D = \sqrt{\frac{2\varepsilon}{q \cdot N_D}}, \quad E_C = \sqrt{\frac{2q \cdot N_D \cdot V_{BR}}{\varepsilon}}$$

Where ε is the dielectric constant of the semiconductor and E_C is the critical electric field. In this equation, breakdown voltage increase in proportion to the square of critical field.

In case of vertical power device, thickness of the drift region should be increased in order to blocking high reverse bias voltage. Therefore, the portion of epi layer to total on-resistance is increased as breakdown voltage increases. The portion of epi-layer in the device having breakdown voltage over 500 V takes up approximately 80 % of the total on-resistance as shown in Fig. 1.16. From this correlation, it is expected that GaN-based vertical device has a lower on-resistance due to the

reduced epi-layer than that of Si-based device.

Based on vertical structure with a uniform doping profile, the on-resistance of device is represented as

$$R_{ON=SP} = \rho \cdot W_D = \frac{4V_{BR}^2}{\varepsilon \cdot \mu \cdot E_C^3}$$

Where ε, μ and E_C are dielectric constant, electro mobility and critical electric field respectively. In order to achieve high breakdown voltage, doping level of the drift region should be reduced to expand the depletion length. This, in turn, will increase the on resistance and power losses. However, for the same breakdown voltage, on-resistance of GaN-based device can be lowered by few orders of magnitude than that of Si due to its high critical field. In terms of process, it means that GaN vertical device can have the higher doped drift layer than that of Si device. As shown in Fig.1.17, for given the same breakdown voltage, GaN can be doped with higher doping density which is three orders of magnitude higher than that of Si theoretically. If GaN vertical device with the same volume as that of Si device, it will exhibit the higher breakdown voltage and lower on-resistance than that of Si device. In other words, GaN-based vertical device can achieve the same breakdown voltage and on-resistance with small device volume due to the thinner and higher doped drift region than that of Si device as shown in Fig. 1. 18.

Due to its wide bandgap property, GaN has very low intrinsic carrier concentration that results in negligible junction leakage current up to 400℃. The operating temperature is only limited by the extrinsic

material property such as reliability of the passivation layer, thermal stability of Schottky metal etc. This allows GaN-based device to operate at high temperature without excessive leakage or thermal runaway phenomenon. The necessity of the cooling system is lessened. For instance, thermal withstanding capability of the GaN HEMT based converters is expected to be slightly over 250℃. Highly efficient converters will simplify the heat-sinking requirement, resulting in a great reduction in the size and weight of equipment. Consequently, the overall system becomes compact and light [Fig. 1.18]

The AlGaN/GaN high electron mobility transistor (HEMT) is a kind of the hetero field effect transistor (HFET) consists of peculiar electron channel, 2 dimensional electron gas (2DEG) at the hetero interface. Two ohmic contacts called drain and source electrode give access to the channel. To control the transistor, a gate electrode is placed on top of the AlGaN barrier (or GaN capping layer), which is located between source and drain electrode. Gate electrode is capacitively coupled to the active region of the device. The location of the gate electrode depends on the purpose of the device. In case of the high power switches, gate is generally located closer to sources rather than drain electrode to sustain high voltage which stems from inductive load of the system (or module). In case of the devices for RF operation, the length of the control electrode matters rather than location for good performance.

By applying a bias between gate and source (V_{GS}), the conductivity of the channel (2DEG) is modified and drain current (I_D) can be controlled under the same drain-source voltage (V_{DS}). When the electron channel is

fully opened by V_{GS}, the output current of the device is determined by V_{DS} and $I_{D.}$

The input characteristic of the HEMT is determined by internal diode which consists of gate electrode of the HEMT and AlGaN barrier. Ideally, the no current (I_G) flows through the Schottky contact. However, in actual devices, it cannot be neglected. Together with V_{GS}, it decides the performance of the internal diode which control overall HEMTs.

Table 1-2 Material properties of semiconductors [24]

		Si	AlN	GaN	SiC		Diamond
					4H	6H	
Bandgap at 300 K (eV)		1.12 Indirect	6.1 Indirect	3.44 Direct	3.25 Indirect	2.86 Indirect	5.46-5.60 Indirect
Bulk mobility at 300 K (cm^2/Vs)	μ_e electron	1400	1100	900[1)] 2000[2)]	700	330-400	2200
	μ_h Hole	450	400	10	NA	75	1800
n_i [intrinsic carrier] density (cm^{-3})		1.5×10^{10}	$\sim10^{-31}$	1.9×10^{-10}	8.2×10^{-9}	8.2×10^{-9}	$\sim1.6\times10^{-27}$
v_{sat} [Saturation velocity] (10^7 cm/s)		1	1.8	2.5	2	2	3
E_C [Critical field] (10^6 V/cm)		0.3	11.7	3.5	3.2	2.4	7
Thermal conductivity (W/cmK)		1.3	2.5	1.1	4	5	6-20

Table 1-3. Normalized figure of merit of wide bandgap semiconductors [29]

Material	Si	4H-SIC	GaN	AlN	Diamond
BM ($\varepsilon_r \mu E_C^3$)	1	130	650	31700	4110
BHM (μE_c^2)	1	22.9	77.8	1100	470
JM ($E_c v_{sat}/2\pi$)	1	180	760	5120	2540
KM $\theta_k(v_{sat}/\varepsilon_r)^{1/2}$	1	4.61	1.6	21	32.1

*BM: Baliga's figure of merit for power switching

BHM: Baliga's high frequency FOM

KM: Keyes's figure of merit considering thermal limitation.

JM: Johnson's figure of merit for high frequency devices

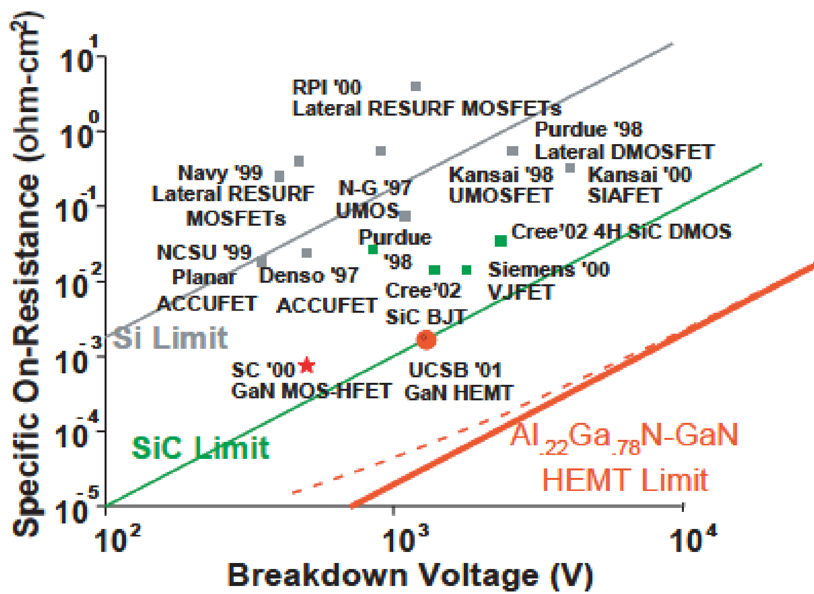


Figure 1.13 Theoretical limits of the figure of merit (FOM) for silicon, silicon-carbide and gallium nitride [21].

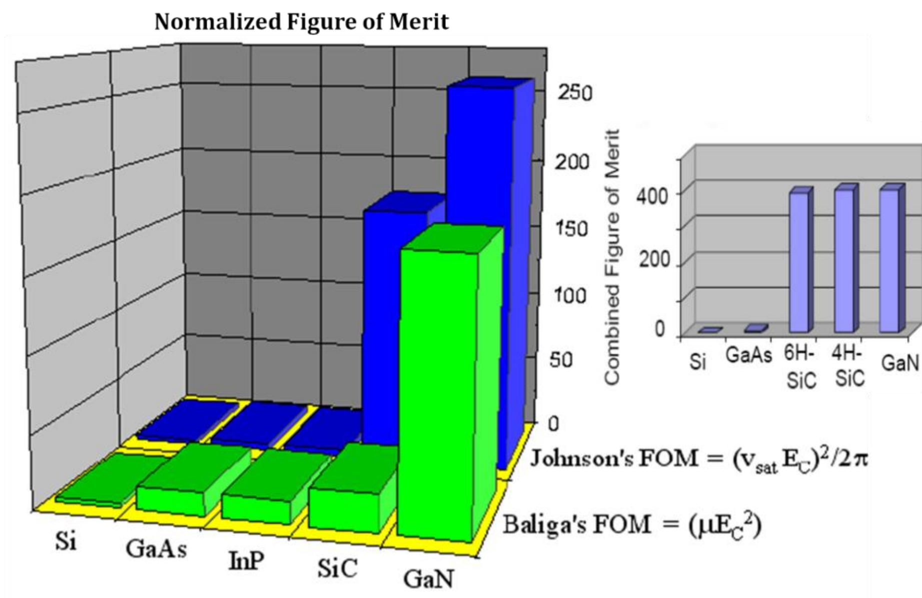


Figure 1.14 Baliga's and Johnson's figure of merit (FOM) for various semiconductor materials.

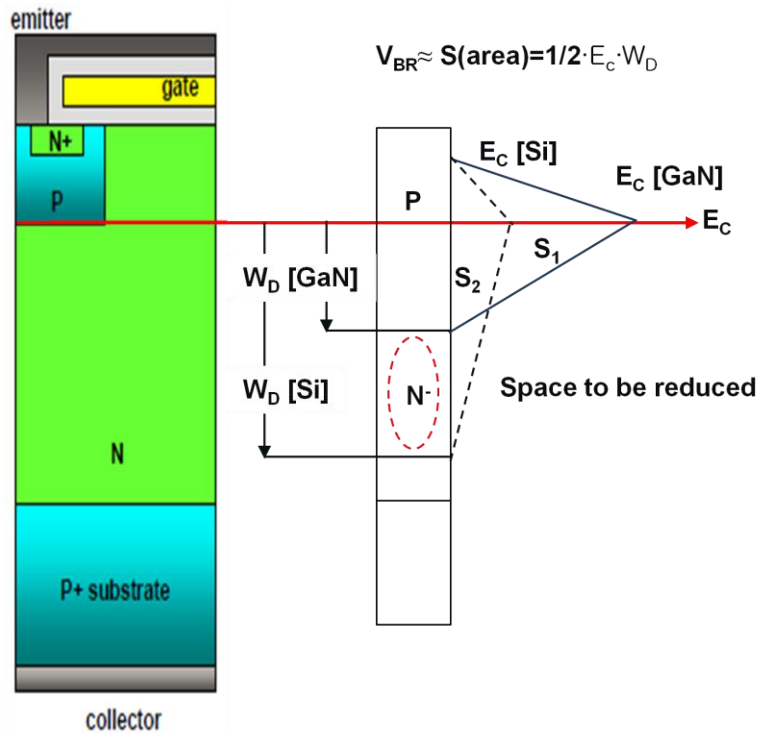


Figure 1.15 Schematic diagram describing the distribution of electric field and depletion region of Si IGBT under reverse bias condition.

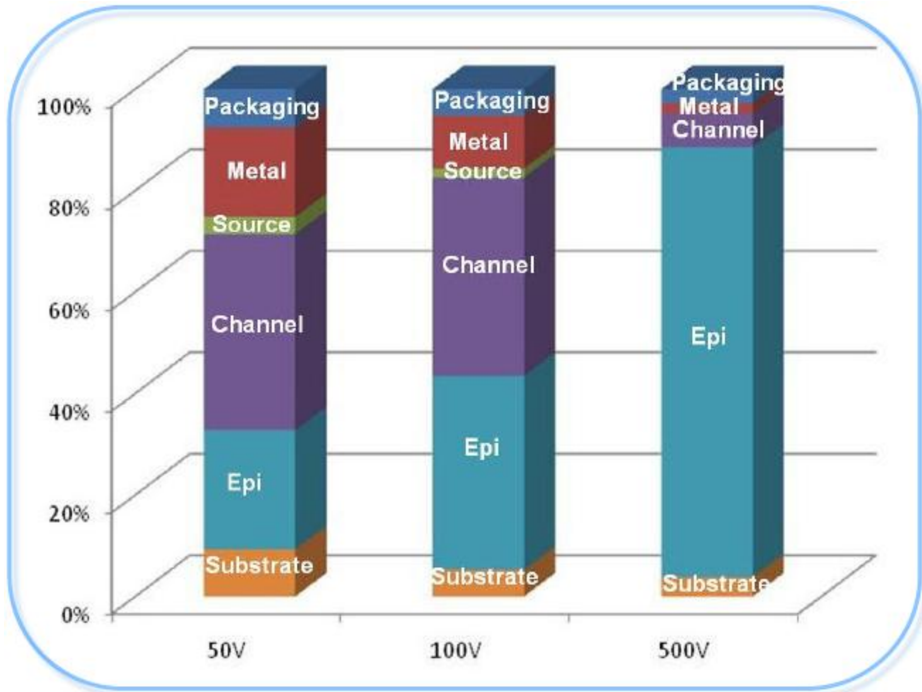


Figure 1.16 Portion that each part of the power device occupies to the total on-resistance according to breakdown voltage.

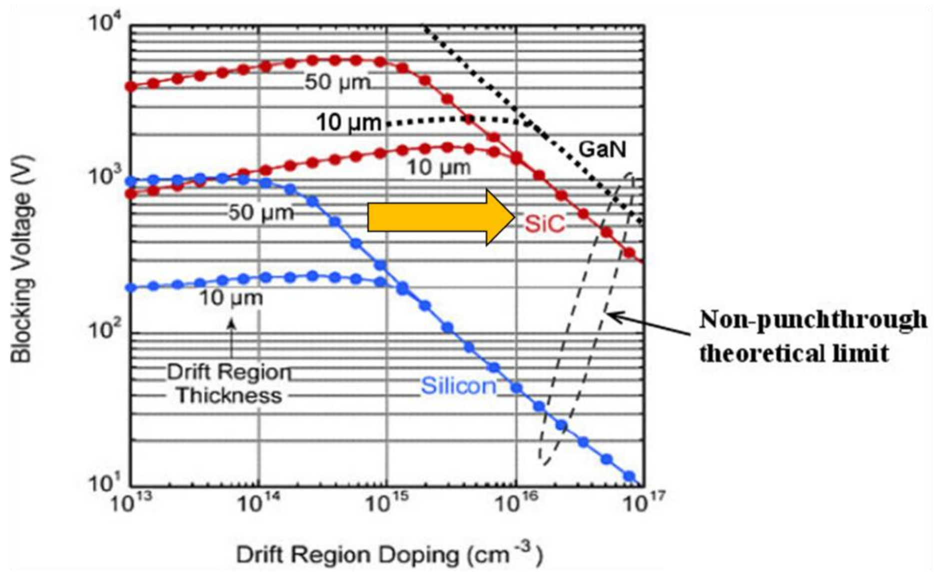


Figure 1.17 Theoretical limit of the doping level in the drift region of vertical device according to the required breakdown voltage.

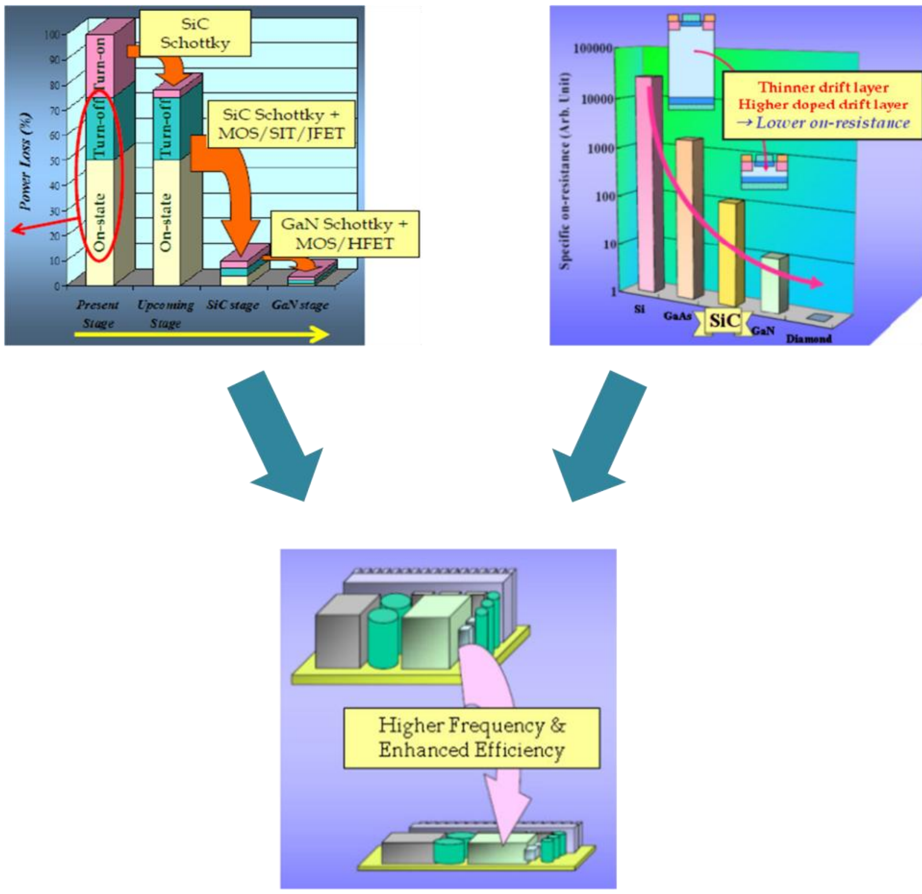


Figure 1.18 Schematic diagrams describing the simplification and lightening of the power system based on a GaN based discrete.

1.3 Organization

Devices for high power switches are required to handle high current with low conduction loss during on-state and sustain high blocking voltage with low leakage current during off-state for the reliability of the systems. Many research groups working on high power switches have focused on technologies to improve the blocking capability of the device without any cost of forward characteristics. Various techniques, called termination method, to enhance the blocking characteristics of the device have been reported. In this dissertation, various methods to improve the blocking characteristics are proposed. The feasibility of the method is verified through the experiment results.

Chapter 2 includes overall review of AlGaN/GaN HEMTs. Fundamentals of the AlGaN/GaN HEMTs are covered in many points of view. Polarization phenomenon responsible for the electron channel, called 2 dimensional electron gases (2DEG), and the advantages from this peculiar channel system are investigated. Then, fabrication processes such Ohmic contact and Schottky contact formation and its basic mechanism are covered. Finally, Factors that limit the performance of the AlGaN/GaN HEMTs is discussed briefly. Traps on the surface and in the bulk have been the issue which caused non-idealities in the device performance. In this chapter, Non-idealities related to traps and solutions which have been reported by many research groups is introduced. Finally failure mechanism is also reviewed.

Chapter 3 focuses on a reliability of the AlGaN/GaN HEMTs employing nickel oxide film used as the interracial layer. First the material properties of nickel oxide film according to oxidation temperature and atomic density of the film are characterized. Nickel oxide film with high atomic density exhibits resistive switching characteristics. This unique phenomenon demonstrates the possibility that GaN based device can be used as memory device. Memory action is confirmed through the fabricated AlGaN/GaN HEMTs using nickel oxide film with switching properties. In case of the nickel oxide film with normal density, the effect of the nickel oxide film on the operation in blocking mode is investigated. Through a HTRB test, thermal stability of the proposed device is verified. SIMS analysis and data obtained from the gate-diode characteristic is used to demonstrate the mechanism of the stable blocking characteristics of the proposed device. Finally, experiments on fluorinated nickel oxide interfacial layer are introduced. AlGaN/GaN HEMTs using fluorinated nickel oxide interfacial layer shows an improved current capability. The mechanism of the increased current capability and the role of the implanted fluorine ions are analyzed in terms of the polarization.

Chapter 4 is about AlGaN/GaN MOS-HEMT employing ALD Al_2O_3 gate dielectric. At first, advantage of AlGaN/GaN HEMTs having MOS structure is structure is introduced. Then, overall device performance of the MOS-HEMT is demonstrated. Trap density extracted from the subthreshold swing (SS) and hysteresis of the C-V curve of MOS-HEMTs give an account for the condition of interface between ALD Al_2O_3 and AlGaN barrier layer. From leakage current and pulsed I-V characteristics, passivation effect of the ALD Al_2O_3 dielectric is demonstrated. HTRB test and accelerated

stress experiments give an explanation for the electrical ruggedness of the ALD Al_2O_3 film.

Finally, conclusions are summarized in chapter 5.

Chapter 2

2. Review of AlGaN/GaN HEMTs

2.1 Principle of AlGaN/GaN HEMTs

AlGaN/GaN high electron mobility transistor (HEMT) is a three terminal device with similar structure of MOSFET. In the structure, instead of oxide layer, the AlGaN ternary compound with wide band gap of 4.3 eV in used to separate the gate electrode from the channel. The conductivity of the device depends on the electron channel of high density at the hetero-interface. Because electron channel is located underneath the AlGaN barrier and distributed within 2~3 nm-thick region from the barrier layer, it is called 2 dimensional electron gas (2DEG). In the following, the formation process will be explained and characterized by means of carrier concentration, mobility, and velocity.

Each of two semiconductor layer, AlGaN, GaN have a different energy band gap (E_g). Because the lower edge of the conduction bands (CBM) is different from each other, neither are the upper edge of the valence band. During the alignment of the energy band, there is the band offset due to

the difference of the electron affinity (χ) of the two semiconductors according to Anderson's electron affinity rule [30].

$$\Delta E_C = \chi_{AlGaN} - \chi_{GaN} \text{ , } \Delta E_V = E_g^{AlGaN} - E_g^{GaN} - \Delta Ec$$

Band offset of the conduction band between AlGaN with al mole fraction of 30 % and GaN is reported to be 0.42 eV [31]. For a more complete understanding of alignment between two nitride material, assuming that two material are brought into intimate contact, Fermi level (E_F) of each material is different and is pinned at the bulk side of the material. Since Fermi level of each materials need to be in thermodynamic equilibrium, energy band of two nitride materials bends with each Fermi levels being aligned. The energy band of GaN bends down ward with making triangular potential well at the hetero interface. Free electrons is confined or accumulated in this potential well with forming 2DEG (Fig. 2.2).

This explanation is essentially consistent with a theory suggested by researcher such as Freeman, Schwierz and Ambacher in the perspective of charge neutrality. In the theory, due to the spontaneous polarization of the Ⅲ-nitride material (spontaneous and piezoelectric polarization will be explained in the next section), electric field exists in both semiconductors (GaN, AlGaN). The magnitude of the polarization field of AlGaN layer is larger than that of GaN. Additionally, AlGaN is under tensile stress due to its smaller in-plane lattice constant (a_0) than that of GaN. Consequently, extra field induced by piezoelectric polarization is added to the inherent field caused by spontaneous polarization. The formation of 2DEG is considered as a process to compensate the surplus polarization

field of the AlGaN layer. Namely 2DEG in the GaN top layer is a result of sheet charge induced to compensate the discontinuity in polarization at the hetero interface for ensuring the local charge neutrality.

Fig. 2.3 illustrates the simulated energy band configuration for the different bias conditions. In the HEMT operation, the magnitude of the concentration of 2DEG is controlled by the gate voltage (V_G). With V_G increasing more negative, the conduction band at the interface lifts above the Fermi level with weaker bending of band. This means that fewer states in the potential well are occupied. Consequently 2DEG is depleted until the channel is pinch-off.

The control of 2DEG concentration in AlGaN/GaN HEMTS is achieved by changing the Al mole fraction of the $Al_XGa_{1-X}N$ barrier. It has been found that increase of the Al content cause the density of 2DEG (n_s) increase approximately linearly at a rate (dn_s/dx) of $5.45\times10^{13}cm^{-2}$ (Fig. 2.4) [31-32].

In the AlGaN/GaN heterostructure, intentional doping process in the AlGaN barrier or GaN layer to form 2DEG is not necessary. In contrast to the AlGaN/GaN heterostructure, AlGaAs/GaAs system needs doping process to form the channel. The main advantage of 2DEG in AlGaN/GaN system is to exploit the electron channel of high density without suffering the mobility degradation caused by many factors. At room temperature, the maximum electron mobility is limited by polar phonon scattering. At low sheet carrier density, ionized impurities and piezoacoustic scattering degrade the mobility. For high density, these scattering processes are screened by electrons in the channel, which explains the increase in

mobility. At very high carrier density, the average distance of the 2DEG to the AlGaN/GaN interface is reduced. In this case, electron mobility is influenced by interface quality. It means that the mobility can be decreased significantly due to the interface roughness scattering [33].

For the use of the 2DEG as conductive channel in actual devices such as transistors, it is required to characterize the electronic transport with ease. If as electric field parallel to the 2DEG is applied, carriers in the channel will be accelerated and will reach a saturation velocity (υ_{sat}) depending on scattering processes. In general, the dependence of υ to *E* (field) can be expressed as

$$v = \mu(E, n_S, T) \cdot E$$

Where μ is the mobility of electrons, which itself is strongly dependent on electric field, the sheet carrier density (n_s), temperature (T) and scattering centers Fig. 2.5 illustrates the correlation between velocity or mobility and these parameters. For low electric fields, velocity increased linearly in proportion to electric field. For high field, υ reaches its maximum value (υ_{max}), and for higher field, υ saturates and becomes independent on electric field. In the case of low electric field, mobility of the electron (μ_0) depends on temperature (T) and sheet carrier density (n_s) [34].

The comprehensive knowledge of υ_{sat}, n_s, and μ is helpful to evaluate DC, RF, and power measurement of the device based on 2DEG channel system. For instance, current density (j_{2DEG}) of the electron channel in the linear and in the saturation regime can be expressed in term of υ and n_s as

$j_{2DEG}=q \cdot n_s \cdot \mu_0 \cdot E$ or $j_{2DEG}=q \cdot n_s \cdot \upsilon_{sat}$. For excellent RF performance of the device, μ_0 and υ_{max} should be high. With regard to the power performance, a high n_s is important parameters to decide the current capacity. Additionally, the high breakdown field (E_c) of device material and high thermal conductivity (θ_k) of the substrate is important to achieve stable performance.

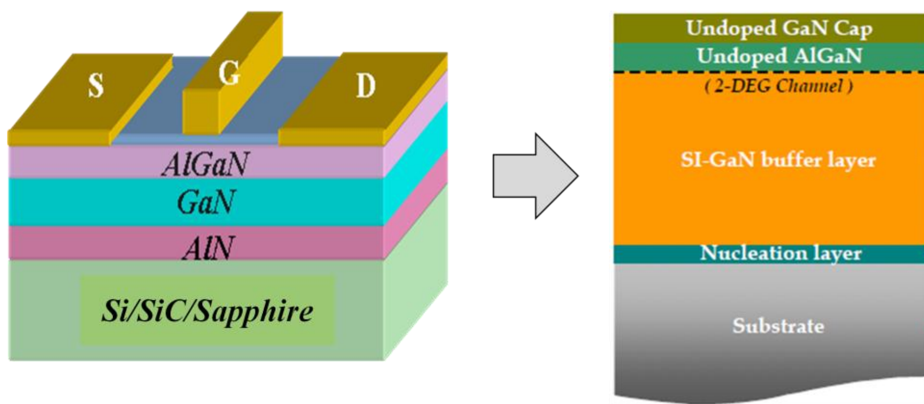


Figure 2.1 Schematics shows standard structure of AlGaN/GaN HEMTs.

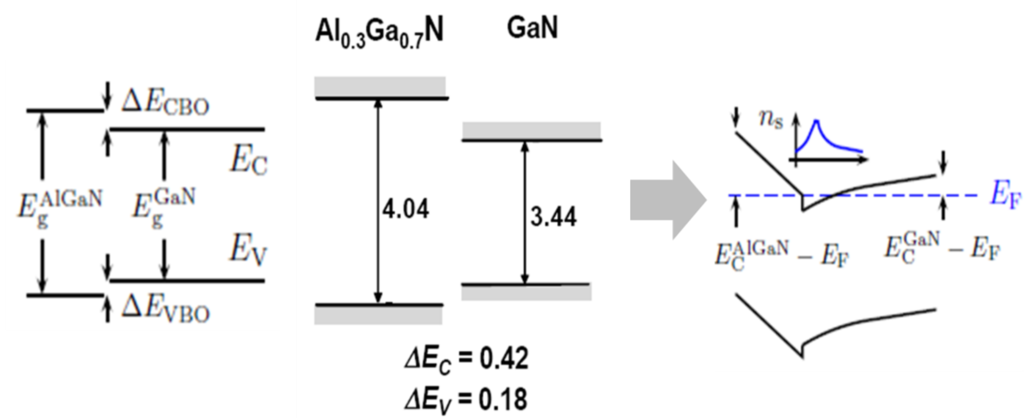


Figure 2.2 Schematic diagram describing band offset of in conduction band and valence band of the AlGaN/GaN structure and its alignment [30]. [ΔE_C for $Al_{0.3}Ga_{0.7}N$/GaN heterostructure: 0.42 eV reported by Schwierz et al.]

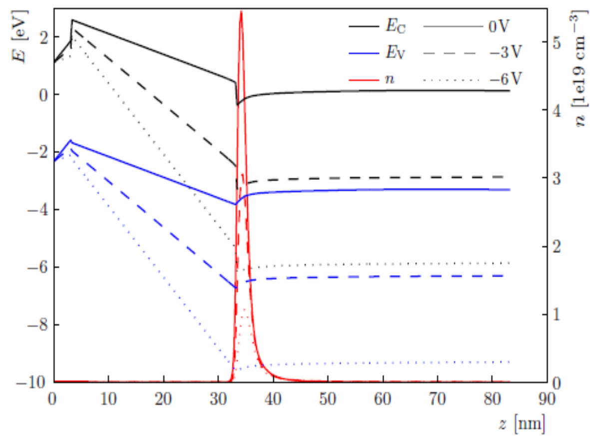
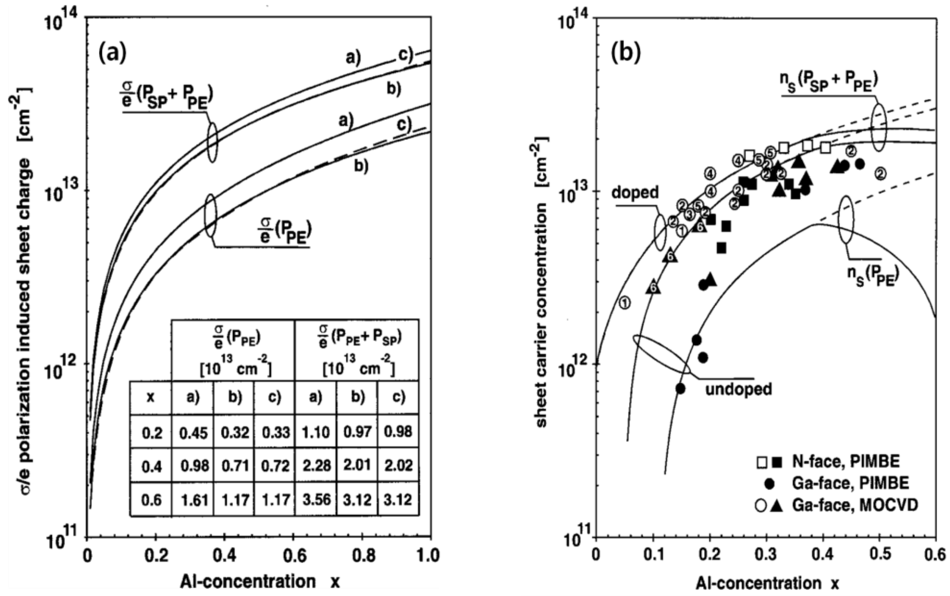


Figure 2.3 Simulated energy band diagram and charge carrier distribution of GaN/AlGaN/GaN structure according to different bias conditions.



x	$\frac{\sigma}{e}(P_{PE})$ [10^{13} cm^{-2}] a)	b)	c)	$\frac{\sigma}{e}(P_{PE}+P_{SP})$ [10^{13} cm^{-2}] a)	b)	c)
0.2	0.45	0.32	0.33	1.10	0.97	0.98
0.4	0.98	0.71	0.72	2.28	2.01	2.02
0.6	1.61	1.17	1.17	3.56	3.12	3.12

Figure 2.4 (a) Piezoelectric (P_{PE}) and total polarization (P_{SP}+P_{PE}) induced sheet charge of AlGaN/GaN heterostructure according to Al alloy composition. (b) Calculated maximum sheet carrier concentrations $n_s(P_{SP}+P_{PE})$ for pseudomorphic (dashed line) and partially relaxed [solid line] Ga-face $Al_XGa_{1-X}N$/GaN HEMTs. Black symbols are the sheet carrier concentrations determined by Hall-effect measurement at T=300 K.

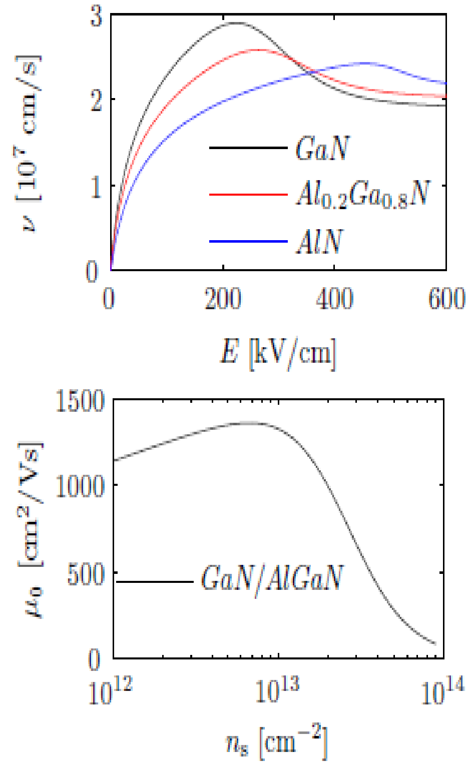


Figure 2.5 Carrier velocity (υ) and low-field mobility (μ_0) in GaN-based devices. (a) The carrier velocity as a function of electric field (E). (b) Low field mobility (μ_0) as a function of sheet carrier concentration (n_s) at room temperature.

2.2 Structure and Polarization

The group Ⅲ-nitrides such as AlN, GaN, and InN can be classified into three crystal structure: wurzite, zinc-blende, and rock –salt. Among them, wurzite structure is thermodynamically stable phase which consist of two interpenetrating hexagonal close packed lattices, which can be shifted with respect to each other ideally by $3/8 \cdot c_o$ [35]. c_o is the height of the hexagonal lattice cell. The chemical bond of Ⅲ-nitride compound such as GaN is covalent.

The unit cell of the wurzite lattice is hexagonal with a basis of four atoms. There is no symmetry in this lattice structure along the c-axis or [0001] direction, which is the direction expressed by a vector pointing from a Ga to the nearest neighbor N atom. The lack of symmetry indicates that an atom in the position on a close packed plane with specific coordinate (x, y, z), is not invariant to the position (-x, -y, -z) since inversion result in replacement of group Ⅲ atoms by nitrogen atoms and vice versa. As a result, all atoms on the same plane at each side are the same. Consequently, wurzite GaN crystals have two distinct faces, commonly known as Ga-face and N-face.

Figure 2.6 illustrates the atomic arrangement in Ga-face and N-face GaN crystal with the parameters to define the wurzite lattice such as a_0 (basal hexagon) and c_0 (height of the hexagonal lattice cell) and its surface morphology. In an ideal wurzite crystal the c_0/a_0 ratio equals 1.633 [36].

Table 2-1 shows an overview of these lattice parameters of wurzite Ⅲ-nitride at 300 K. From table 2-1, it is clear that GaN is closest to the ideal

wurzite structure. The non-ideality represented as c_0/a_0 ratio is important factor to determine the strength of polarization in Ⅲ-nitrides.

Nitrogen is the smallest and the most electronegative in group Ⅴ-element. Ⅲ-nitride covalent bonds have the stronger ionicity than other Ⅲ-Ⅴ covalent bonds. This ionicity results in a macroscopic polarization if the crystal lacks structural symmetry.

The wurzite Ⅲ-nitride also has no symmetry along the [0001] (c-axis) direction. The combination of the strong iconicity of Ⅲ-nitride bond with the non-symmetry in crystal lattice results in a strong macroscopic polarization along the [0001] direction. Because this polarization occurs in the equilibrium lattice of Ⅲ-nitride without any mechanical stain, it is called spontaneous polarization [37]. As the lattice non-ideality increases, c_0/a_0 ratio deviates from 1.633 of the ideal lattice, the spontaneous polarization (P_{SP}) increases as shown in table 2-1.

If the ideality of Ⅲ-nitride lattices is changed by external force, there will be large changes in the polarization of the crystal. If the mechanical stress is applied to the Ⅲ-nitride lattice, the lattice parameters (a_0, c_0) of the crystal will be changed to accommodate the stress. This makes the polarization strength changed. This additional polarization in strained Ⅲ-nitride is piezoelectric polarization [37].

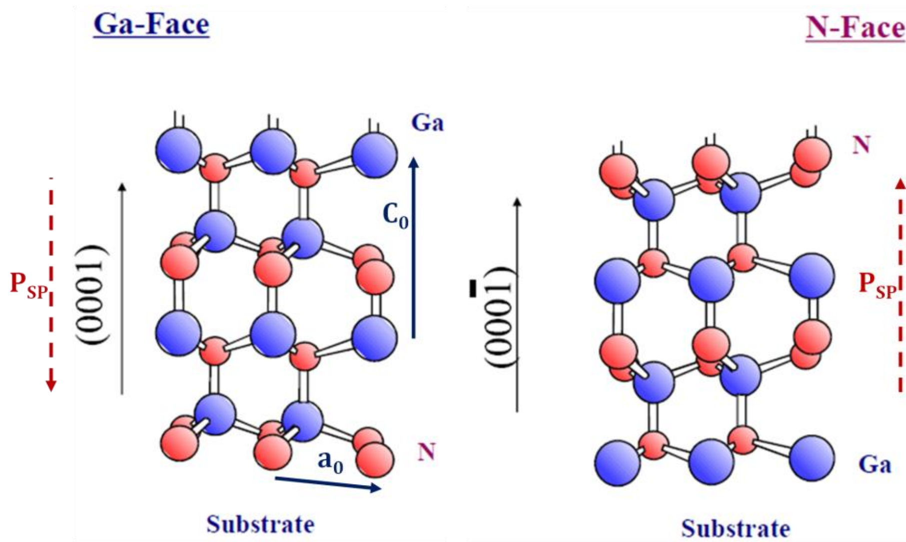
Piezoelectric polarization in the nitride crystal changes according to direction of mechanical stress. The value of piezoelectric polarization in Ⅲ-nitride is negative for layer under tensile stress ($a>a_0$) and positive for

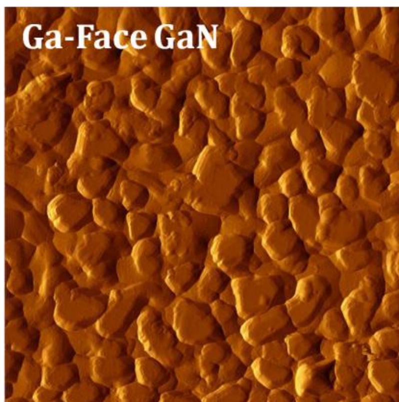
layers under compressive stress ($a<a_0$). As spontaneous polarization in Ⅲ-nitride is always negative. If Ⅲ-nitride is under biaxial compressive stress, in-plane lattice constant a_0 will decrease and vertical lattice constant c_0 will increase. As C_0/a_0 ratio will approach to the ideal ratio of 1.633, spontaneous polarization will decrease. Total polarization of the crystal will decrease because piezoelectric polarization and spontaneous polarization are anti parallel to each other. On the contrary, If biaxial tensile stress is applied to the Ⅲ-nitride, total polarization will increase because piezoelectric polarization and spontaneous polarization are parallel [38].

Figure 2.7 illustrates the direction of the spontaneous and piezoelectric polarization vectors, polarization-induced interface charge, and 2DEG in the pseudomorphic GaN/AlGaN/GaN heterostructure with Ga-face polarity according to mechanical strain (tensile and compressive stress). Piezoelectric polarization will not be generated in the GaN buffer because the lattice mismatch effect between GaN and substrate is alleviated by defects or dislocations in the bottom of GaN buffer. Piezoelectric polarization in GaN buffer can be ignored [39].

Table 2-1 Lattice parameters of wurzite Ⅲ-nitride at 300 K [36]

Parameter	Ideal	AlN	InN	GaN
a_0 (Å)	-	3.112	3.548	3.189
c_0(Å)	-	4.982	5.760	5.185
c_0/a_0(experimental)	-	1.601	1.6116	1.6259
c_0/a_0(calculated)	1.633	1.619	1.6270	1.6336
P_{SP}	-	-0.081	-0.032	-0.029





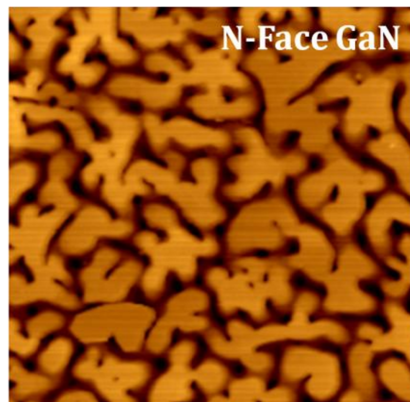
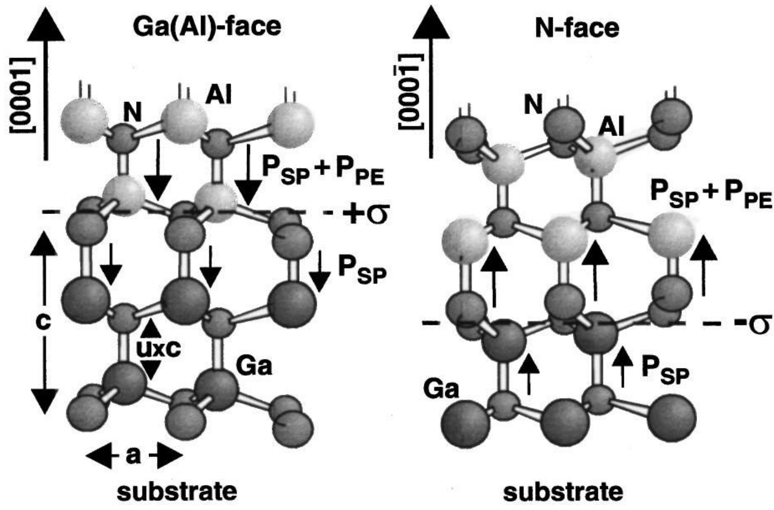
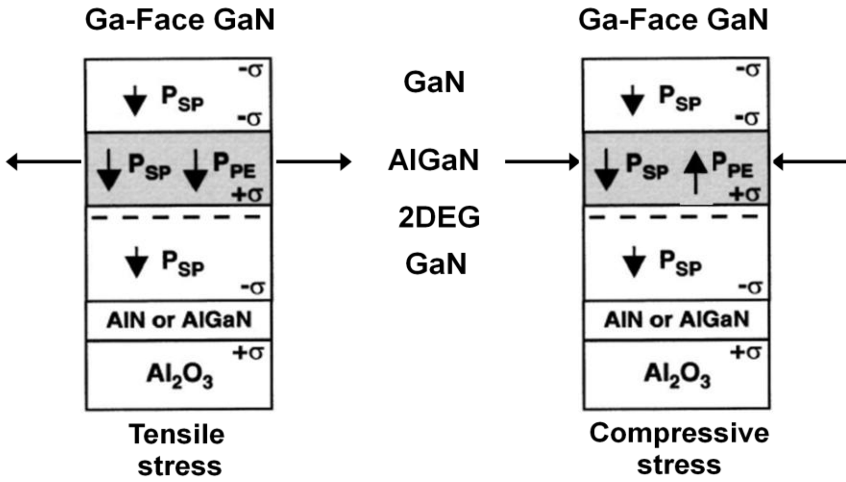


Figure 2.6 Directions of spontaneous polarization in the N-face/Ga-face GaN wurtzite structure and surface morphology of Ga/N-Face GaN.



(a)



(b)

Figure 2.7 Diagram describes (a) crystal structure, polarization-induced sheet charge, P_{SP} and P_{PE} of AlN/GaN heterostructure. (b) P_{SP} and P_{PE} in GaN/AlGaN/GaN heterostructure according to mechanical strain [O.Ambecher].

2.3 Device fabrication

2.3.1 Pre-treatment

The surfaced of the GaN and ALGaN is unique and quite different from other common semiconductor materials, even other Ⅲ-Ⅴ semiconductor materials. Condition of the surface of the GaN or AlGaN is important not only for fabrication process and but for proper device operation. In the fabrication process, clean surface guarantees a stable photo-resist adhesion which leads to accurate pattern for etching and deposition. Even though solvent cleaning and chemical treatment by common acids or bases do not lead to improvement in performance, surface treatment with these solutions results in relatively intimate metal-semiconductor contacts by removing oxide layer and various contaminants on the surface of GaN or AlGaN. It can be the foundation to fabricate the device which functions normally.

Contamination or oxide on the surface results in abnormal device performance. In the atmosphere, the surface of the GaN and AlGaN layer is covered with native oxide or organic (or inorganic) contaminant. The organic contaminant can be removed by organic solvent such as acetone, methanol, isopropyl alcohol or oxygen plasma. In case of inorganic contaminants, NH_4OH, $(NH_4)_2S$ and NaOH are suggested to use. Commonly used acids such as HCl and HF are found to remove the oxide layer effectively. In general both acids are reported to be effective in removing almost all contaminants. Especially, HCl-based solution is more

effective in removing oxides with leaving less oxygen residue. HF is more effective in removing contamination related to carbon and hydrocarbon [40].

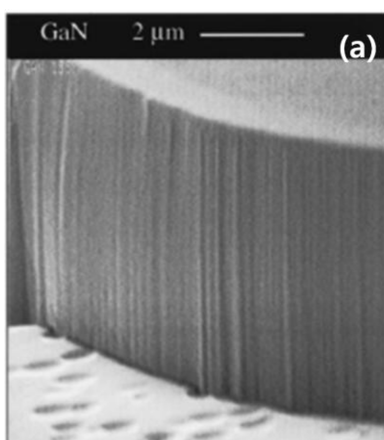
2.3.2 Isolation

In practice, the transistor will be fabricated in parallel with any other transistors on the same wafer or piece of wafer. Insulation of the device is required to allow each device to operate independently without any interference from other device. Especially, in case of AlGaN/GaN HEMTs which is normally-on due to an inherent, high density electron channel (2DEG), electrical isolation is mandatory regardless of its sequence and methods.

The process of the isolation of the AlGaN/GaN HEMTs is to eliminate the electron channel (2DEG) formed in heterostructure. Various methods to isolate the AlGaN/GaN HEMTs have been reported. Isolation by forming thick thermal oxide (Ga_2O_3) through thermal oxidation at the temperature of 900℃ has been proposed by Masato [41]. However, it can cause the thermal damages such as loss of nitrogen and thermal decomposition, which deteriorate the device performance. The junction isolation, which has been used in Si-based CMOS process, cannot be implemented due to the difficulty of doping of p-type material. The most widely used method is to take away the AlGaN barrier in between the regions designed to fabricate devices. Without an AlGaN layer, electron channel will not form and thus a current cannot flow between devices. The effective way is to remove the AlGaN layer through the dry etching because GaN (AlGaN) is chemically stable [42]. Fig 2.8 shows the SEM image of the etched GaN profile. The morphology of the cleared etched GaN looks like a mesa. So,

device isolation using dry etching method is called mesa isolation. Mesa isolation is usually performed by dry etching due to the anisotropic and smooth etching profile [43]. The inductively coupled plasma reactive ion etching (ICP-RIE) is used to mesa isolation rather than electron cyclotron resonance (ECR). The sequence of mesa isolation is different from each other. It is usually performed before Ohmic contact formation. Some groups, however, performs mesa isolation after Ohmic contact in order to prevent ohmic metal from being deposited on the etched mesa side wall, because Ohmic metal deposited on the mesa wall or the gate feed run over the mesa wall can be the source of parasitic leakage current.

Finally, implantation using nitrogen (N^+), argon (Ar^+), helium (He^+) ion, and proton (H_+) etc have been known as isolation method [44-46]. Principle of the implant isolation is based on the Mott transition: conductivity of semiconductor implanted with high dose of ions change entirely. Namely, implant isolation insulates each device by making periphery of the device highly resistive.



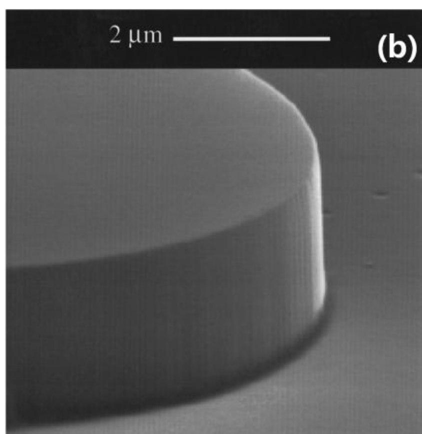


Figure 2.8 SEM micrographs of GaN etched in (a) Cl_2-based ICP plasma (b) BCl_3/Cl_2-based ICP plasma.

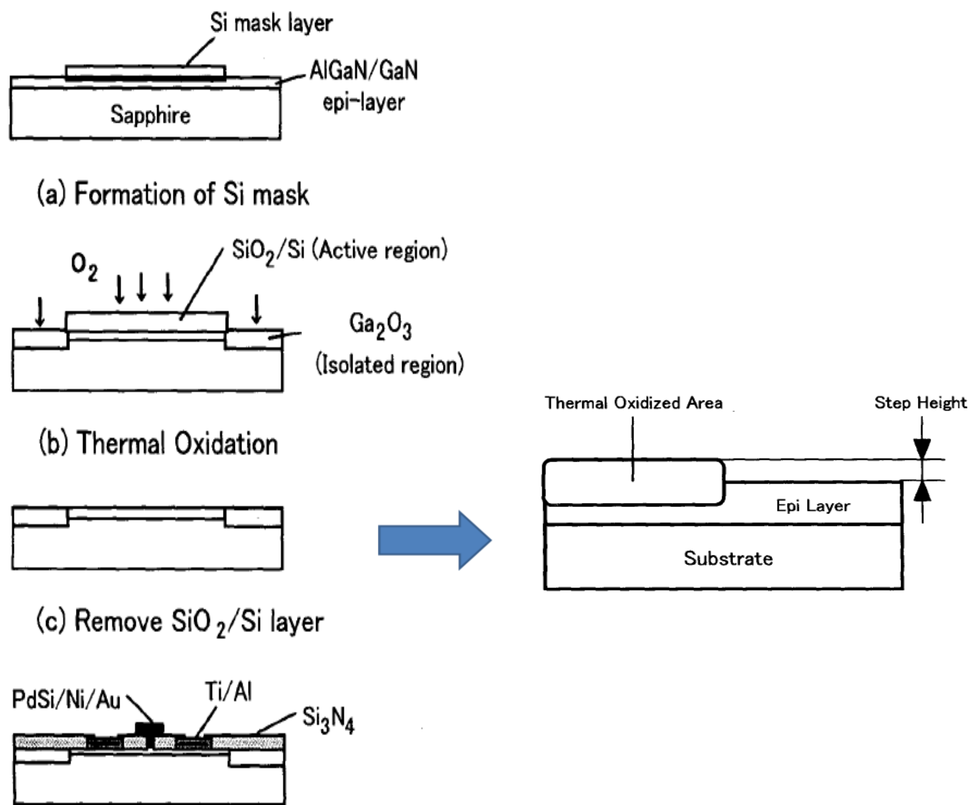


Figure 2.9 Schematics describing a process sequence for the Selective oxidation process.

2.3.3 Ohmic and Schottky contacts

Ohmic contacts on the AlGaN/GaN HEMTs are based on Ti/Al metallization schemes. The most widely used metal stacks are the Ti/Al/Ti/Au, Ti/Al/Ni/Au. Each of the metal layers in this scheme has its own specific role.

Titanium, the first metal of the stack in all case, is thought to be multi-functional layer. Key role of Ti layer in formation of Ohmic contact is to create nitrogen vacancies (V_N) by reacting with nitrogen atoms in the AlGaN barrier layer. As a result of reaction, TiN is formed at the interface between Ti and AlGaN layer. This process make the surface of the barrier highly doped, which allows electrons to tunnel through the electrical thin potential barrier as shown in Fig. 2.10 [47-49]. Moreover, Ti serves as an adhesion layer to offer mechanical stability [50].

Aluminum is expected to react with Ti to form an Al_3Ti layer, which prevents the underlying Ti layer from being oxidized and to serve as a diffusion barrier layer for the metal on top of Al as shown in Fig. 2.11 [50-52]. One of the most important reasons for piling metals on top of the Al is to inhibit metals layers from spreading out. In general, Ohmic contacts are annealed at high temperature over 800 ℃ which is much higher than the melting point of Al (about 660℃). If no metals are put on top of Al, the footprint of the contact cannot remain originally defined.

The Ni layer should prevent Au from diffusing into the Al layer because,

when Au reacts with Al, they can form a highly resistive layer. Au overlayer is usually added to improve the conductivity of the metal stack.

It is certain that several reactions take places at different temperatures. To get reproducible Ohmic contact formation, it is important to accurately control both the temperature and time variations. Rapid Thermal annealing (RTA) is the most suitable technique to satisfy these requirements.

Schottky contacts are in charge of blocking characteristics of the HEMT devices. The potential barrier height between metal and AlGaN barrier is a crucial parameter to control the electron current across the interface and depletion region formed in heterostructure. Barrier height is simply defined as the difference between the minima of the conduction band and the Fermi-level of the metal or the difference between metal work function and electron affinity of semiconductor (Fig. 2.12) [53]. It has been reported that there is a variation in barrier height for the same metal deposited on the AlGaN layer with the same Al more fraction. This spreading is attributed to many factors: different defects present in the semiconductor material; the surface cleanliness and roughness; local stoichiometry variation etc. To achieve large Schottky barrier height (SBH) at metal-semiconductor contact for highly rectifying contacts, gate metals with large work function such as Pt, Au, and Ni have been used. Work function of various metals is shown in table 2-2 [54]. Nickel, widely used for Schottky contact due to its large work function, gives barrier height of about 0.66~1 eV.

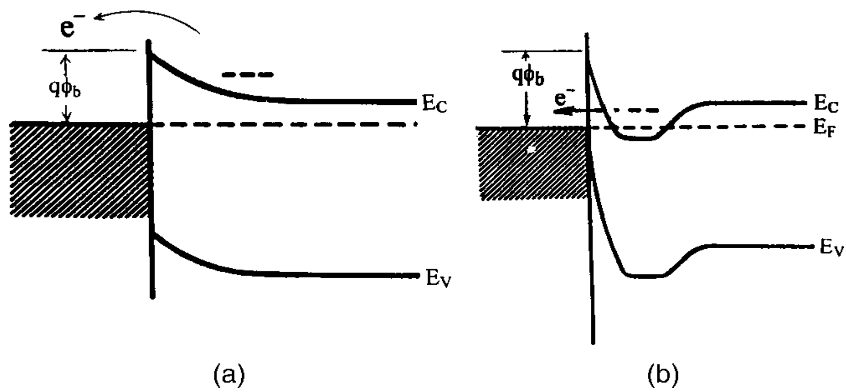
Besides the method of increasing the barrier height employing metals

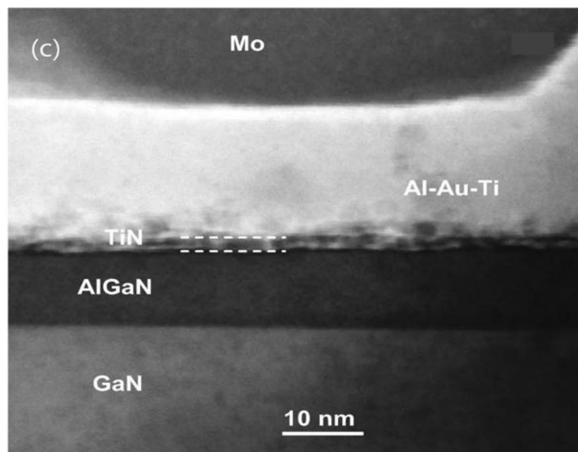
with large work function, another method to get high barrier height is polarization engineering. In GaN/AlGaN/GaN heterostructure, GaN layer added atop the basic AlGaN/GaN HEMTs allows negative polarization charge at top of the AlGaN barrier to be involved in the Schottky barrier structure. It strengthens polarization field, which is unfavorable for the tunneling of electron at the interface between GaN cap layer and AlGaN barrier layer. Thereby barrier height between metal and GaN/AlGaN/GaN heterostructure is increased (Fig. 2.13).

Thermal stability of Schottky contacts is another important issue for device operation because almost metals used for Schottky contact has low thermal budget. Namely, most of them are melt at the temperature over 600℃. For instance, the temperature of 400℃ and 575 ℃ is a thermal limits for Au and Pt, respectively [55].

Table 2-2 Work function of metal for Schottky contact [54]

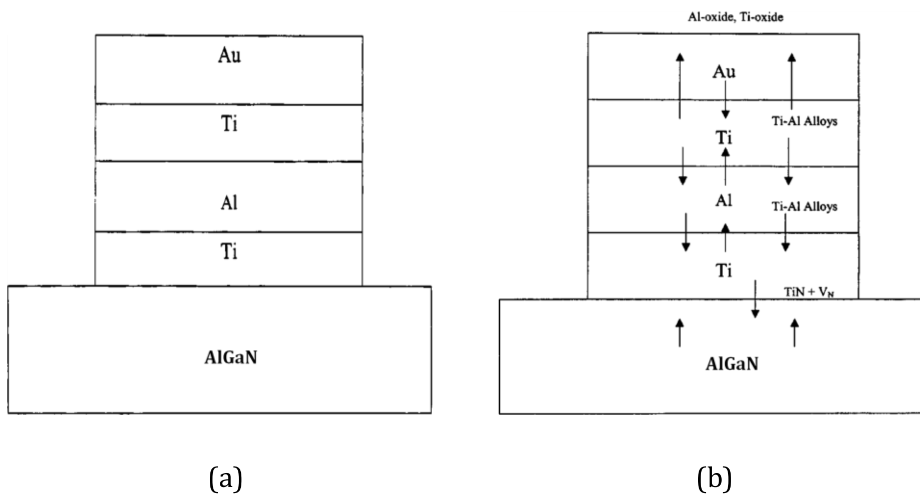
Metal	Work function [eV]
Pt	5.65
Au	5.10
Ni	5.15
Pd	5.12
Ir	5.46
Mo	4.60





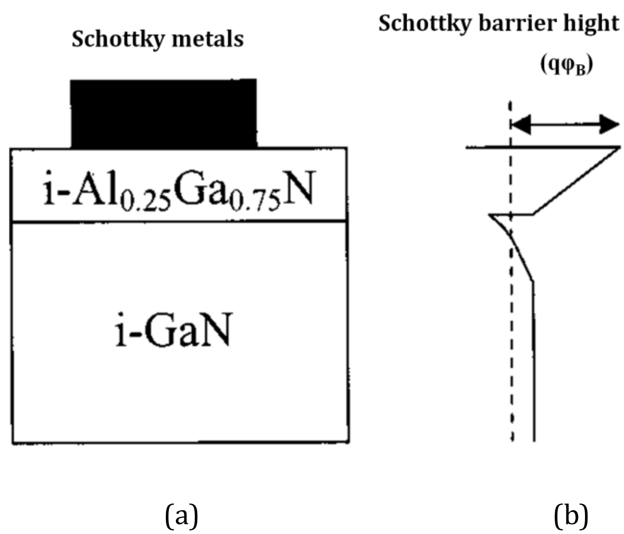
(c)

Figure 2.10 Schematic energy band diagram for the metal-semiconductor interface showing the band bending to the presence of nitrogen vacancies (V_N) (a) CB and VB without band bending and (b) CB and VB with band bending due to the presence of nitrogen vacancies (V_N) (c) Magnified micrograph showing interfacial region between metal stack and semiconductor [47].



(a) (b)

Figure 2.11 (a) Schematic structure of the Ti/Al/Ti/Au-AlGaN Ohmic contact, (b) schematic diagram describing direction by arrows outward and inward diffusion of Al, Ti, Au, and N of AlGaN and the reaction products obtained as a result of various reactions. thus interaction of Ohmic metal stack [50-52].



(a) (b)

Figure 2.12 (a) Schematic diagram describing a typical gate structure of AlGaN/GaN HEMTs (b) Conduction band energy diagram [53-54].

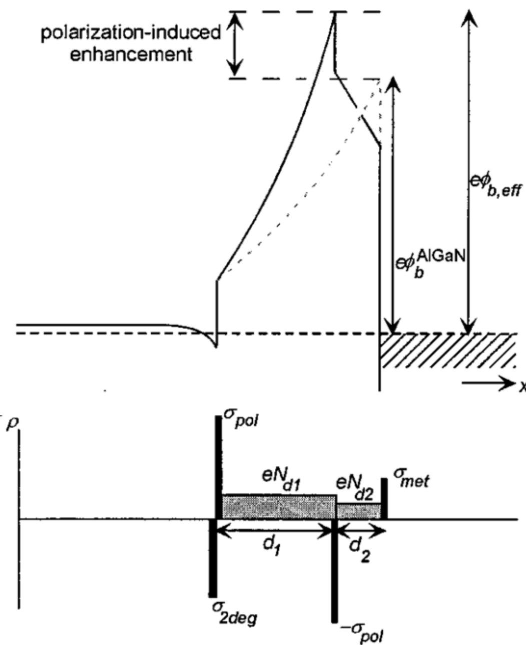


Figure 2.13 Schematic energy band diagram and charge distribution for the GaN/AlGaN/GaN Heterostructure. [The negative polarization charge at the upper AlGaN/GaN interface leads to a large enhancement in effective barrier height]

2.4 Substrate used to AlGaN/GaN HEMTs

In all field effect transistors (FETs), gate electrode serves to modulate the current through a bias-dependent depletion of the channel region. The current is pinch-off, when the channel is fully depleted by gate bias. For complete pinch-off operation, It is required that the conductivity between source and drain contacts should be eliminated. In case of standard Si MOSFETs, the base layer is of the opposite conductivity type to the source and drain implanted regions. This forms a reverse biased pn junction under pinch-off condition. For HEMTs, however, this option is not available. For RF and high power operation, a conductive base layer or substrate is not desirable in terms of power losses and breakdown voltage. The base layer or substrate makes a contribution in blocking current for complete off-state.

Through the development of AlGaN/GaN HEMTs, two substrates have dominated: sapphire (Al_2O_3) and SiC. Sapphire is the traditional substrate for MOCVD of GaN. Large lattice mismatch with GaN resulted in high dislocation density of 10^{10} /cm^2 in the epitaxial film. Because thermal expansion coefficient of sapphire is larger than that of GaN, compressive strain induced on cooling down. It is known that compressive strain of 0.7 Gpa remains on sapphire film of 1~3 μm thick at room temperature. [56]. Sapphire is electrically insulating but has a poor thermal conductivity which limits the power handling capability of the devices.

The alternative substrate, SiC, has been not used for RF and power devices due to electrical conductivity in the substrate. In 1999 the first semi-insulating SiC substrates became available. Even though small lattice mismatch of 3 %, it is still large enough to result in high dislocation densities on the order of 10^{9}-10^{10}/cm^{2}, which is similar to that of GaN film grown on sapphire. Reason for this is the roughness of the SiC substrate (1 nm RMS compared to 0.1 nm for sapphire) and damages introduced during the polishing process. Different pre-treatment such as wet etching or annealing is required to alleviate these effects. Because the thermal coefficient of SiC is smaller than those of GaN, SiC film is usually under tensile strain. One advantage of SiC is its high thermal conductivity. This makes SiC an excellent choice for high power devices. However, high cost is the major drawback of the SiC substrate.

The reasons for making a great effort on Si substrate are obvious. Si substrate is cheap, available in very large size and has a high degree of crystal perfection. Growth problem such as large lattice mismatch and thermal mismatch was overcome by technical breakthrough such as supuerlattice structure and strain releasing layer (SRL). Due to its moderate thermal conductivity of 1.5 W/cm·K, the problem of poor thermal conductivity of GaN is mitigated by the Si substrate, when it is grown on.

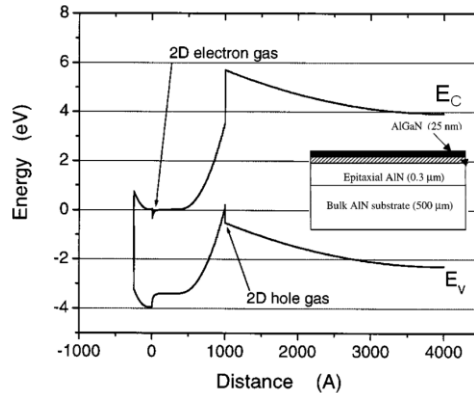
Among all the substrates substrate, AlN is the best match to GaN. Its lattice constant matches not only at room temperature but also at growth temperature of GaN. Epitaxial layer of GaN grown on bulk AlN substrates have shown low dislocation density on the order of 10^{4}-10^{5}/cm^{2}, which is

four orders of magnitude lower than GaN layer grown on SiC. At the same time, bulk AlN substrates have superior thermal conductivity of ~3 W/cm·K which is comparable to that of semi-insulating 4H-SiC (~3.9 W/cm·K) [57]. The AlGaN/GaN HFET grown on bulk AlN substrate exhibits DC and RF characteristics comparable to HFET grown on SiC. Measured drain current is over 400 mA/mm and measured cut-off frequency (f_T) is ~ 5 GHz. The results indicate that AlGaN/GaN HFET grown on AlN have potential to yield more reliable and longer lifetime device due to much smaller dislocation density (Fig.2.14) [58]. Physical properties of the substrates used in GaN epi growth is summarized in table 2-3 [59].

Si is emerging as the most suitable choice for commercial product due to its low cost and large size availability. However, it is reported the device fabricated on Si (111) have the disadvantage that electrical breakdown occurs vertically through the Si substrates. This is because of the critical electric field of Si (E_C: 0.3 MV/cm) is ten times lower than that of GaN (E_C: 3.5 MV/cm). It is indicated that Si substrate can be a leakage path in the high-voltage blocking mode. This can be a serious drawback when it is used for very high voltage application. Consequently, the removal of Si substrate is proposed by P. Srivastava et al. for the enhancement of breakdown voltage [60]. Fig. 2.15 illustrates the layer-transfer process for selective removal of Si substrate and measured breakdown voltages. After substrate removal, breakdown voltage of DHFET and buffer breakdown is increased significantly while device with Si substrate exhibits the saturated breakdown voltage.

Table 2-3 Physical properties of substrates used in AlGaN/GaN heterostructure [58]

Substrate	AlN	GaN	Al_2O_3	SiC	Si
Thermal conductivity [W/cm·K]	3.3	1.3	0.5	3- 3.8	1-1.5
Lattice mismatch [%]	-2.4	-	-16	+3.5	-17
Resistivity	high	high	high	high	mediate
Cost	High	high	low	high	low
Wafer size [inch]	small	small	6	3	12



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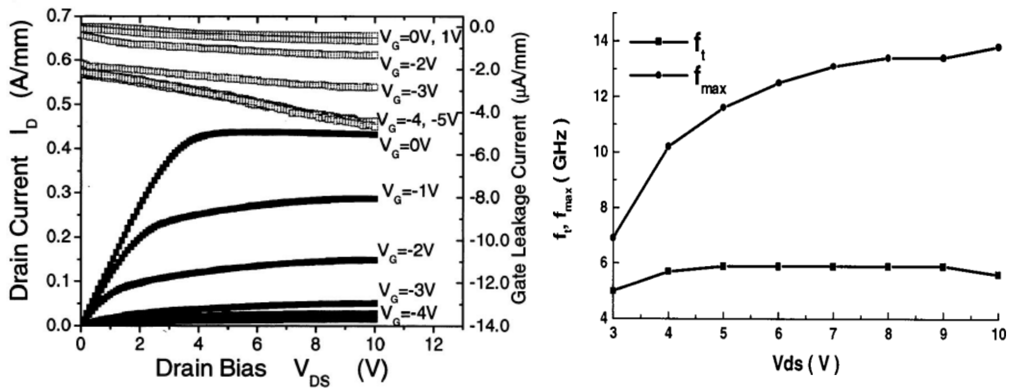
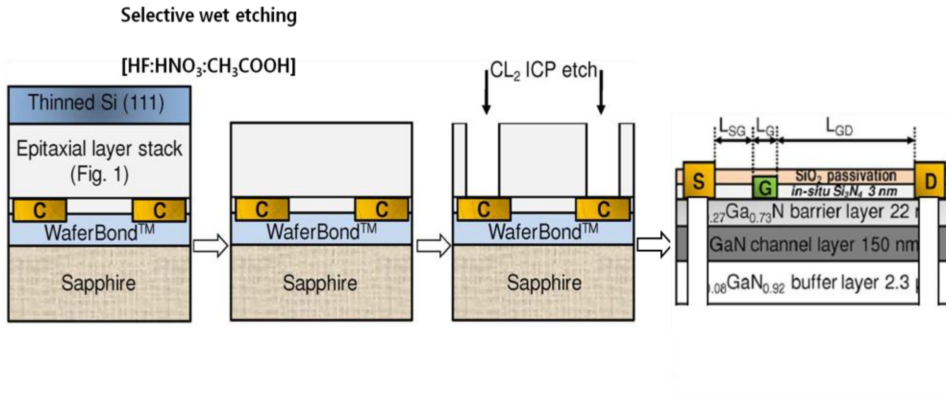


(b)

Figure 2.14 (a) Energy band diagram of AlGaN/GaN/AlN Heterostructure, (b) DC output current and f_T and f_{MAX} of AlGaN/GaN HFET on bulk AlN [59].



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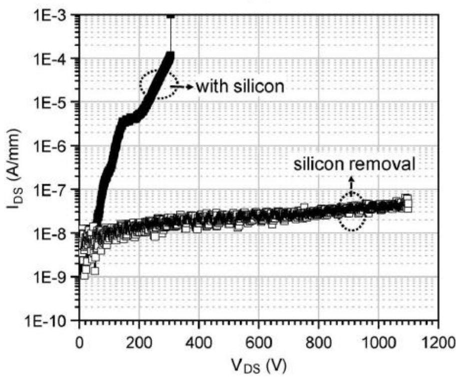
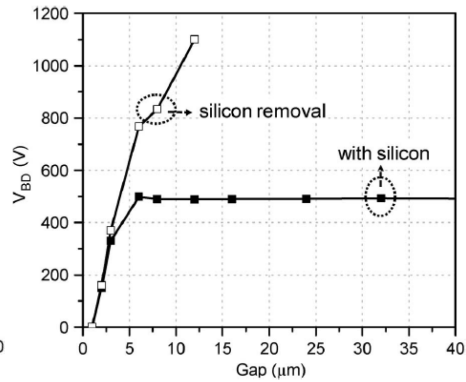




(a) (c)

Figure 2.15 (a) Processing steps for Silicon removal and layer transfer (b) Measured breakdown voltage of the DHFET (c) Buffer breakdown voltage as a function of the isolated gap between two ohmic contacts [60].

2.5 Factors limiting the HEMT performance

2.5.1 Current collapse

The problem of current collapse in GaN HEMTs has been variously referred to as dispersion (DC to RF dispersion), current slump and current collapse. It is one of the most important problems that degrade the device for high power switches.

In general, current collapse is the phenomenon where the measured output power at microwave frequencies is considerably smaller than that obtained DC operation. To explain the lower output power at RF operation, $I_{DS\,MAX}$ is expected to be reduced or V_{KNEE} be increased from the DC values. Fig. 2.16 shows measured DC and pulsed I-V characteristic with typical dispersion phenomenon [61]. As can be seen from Fig. 2.16, there is a considerable reduction of the drain current, together with an increase in knee voltage, when it is measured under the drain current. It is known that the current collapse is attributed by deep level states in the bulk or by the surface states on the surface. Because deep level states are generally located few eV below conduction band or few eV above the valence bands, electrons in the CB of VB can be caught easily. It is required more energy (thermal or electrical) and more time for electrons to be free from deep level states. The charge states of these deep levels do not respond to the high frequency signal applied to the devices. It is required to minimize the bulk trap densities in order to improve power performance of GaN HEMT but do not eliminate the problem of current

collapse. When the HEMT is under large drain bias in the off-state, the surface of the AlGaN barrier become negatively charged. It is understood by a postulation that donor-like surface states on the barrier layer accept electrons injected from gate to become negatively charged. These charged states act as the negatively biased gate with introducing vertical depletion in the device. These charged states are also responsible to the dispersion. It is reported that the trapping of carriers take place in the AlGaN barrier or the surface of the device and not the buffer. [62]

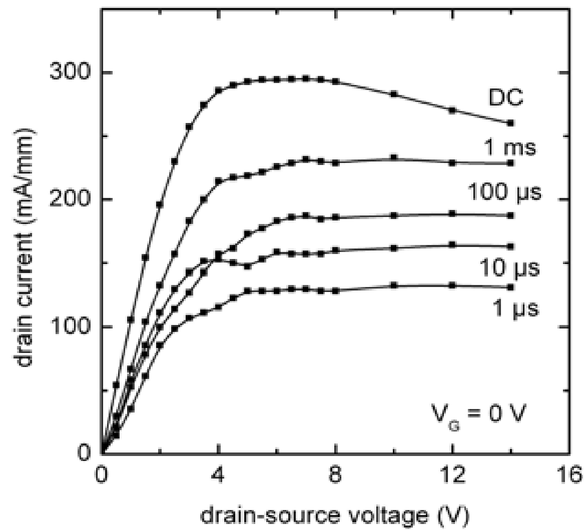


Figure 2.16 Typical DC and pulsed I-V characteristics of the AlGaN/GaN HEMT [61].

2.5.2 Leakage current

GaN has emerged as a promising material for high power applications. However, GaN-based later device such as metal-semiconductor field-effect transistor (MESFET) and high electron mobility transistor (HEMT) suffer from high leakage current which deteriorates the reliability and efficiency of the devices. Especially, gate leakage current prohibits GaN HEMTs from approaching their potential. For the low noise and improved reliability, AlGaN/GaN HEMTs should suppress the leakage current passing throughout all parts of the device.

Prior to focusing on the suppression of leakage current, understanding of where the leakage current occurs and flows is required. It is well-known that the gate leakage current on the active area is dominant factor which is related to many degradation phenomena in the blocking mode. However, in the AlGaN/GaN HEMT, there are many routes where electrons pass through under high reverse bias condition. Fig. 2.17 illustrates all the possible leakage paths of the AlGaN/GaN HEMTs are as follows

Active region (the surface of the access region between source and drain)

Mesa side wall (an inclined plane of the mesa morphology)

Peripheral region (etched GaN region surrounding active region)

Buffer region (GaN buffer region between substrate and AlGaN barrier)

Until recent days, except gate leakage current on the active area, the effect

of the leakage current through each path on the blocking characteristics of the device has not been investigated.

However, experimental results showing that other leakage components as well as gate leakage have an effect on the device performance are reported by some research groups [63-65]. For instance, after silicon was adopted as the substrate of the GaN-based heterostructure, GaN-buffer leakage component due to the screw dislocations is of interest to many device engineers. As referred to in section 2.4, it is often reported that AlGaN/GaN HEMT grown on Si substrate suffers from premature device failure due to the large buffer leakage current and breakdown occurring at the GaN buffer or Si substrate. Considering dominant degradation factors are different from each device according to its epitaxial structure and fabrication process, it is required to investigate the effect of other leakage components on the device performance and take these factors into account in the analysis of device degradation.

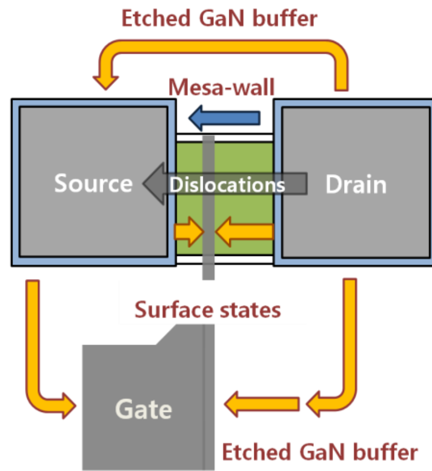
The active area of AlGaN/GaN HEMT is generally defined by dry etching. It is indicated that periphery of AlGaN/GaN is exposed to plasma damages during isolation process and is full of defects and surface states of high density. Because gate electrode is deposited across both the active area (gate finger) and etched peripheral region including mesa wall (gate feed), it is strongly expected that parasitic leakage current takes place. Fig. 2.18 shows a measured gate leakage current of the AlGaN/GaN HEMT. The intercept of Y-axis could be interpreted as the parasitic leakage current originated from etched peripheral region including mesa side-wall. The parasitic leakage current represented as Y-intercept in Fig. 2.18 increases

in proportion to operating temperature. This reflects that high operating temperature gives thermal energy enough for hopping conduction to electrons in the etched peripheral region. Consequently, at high operating temperature, parasitic leakage current is increased. At the operating temperature of 200℃, parasitic leakage current (4.45 μA) is larger than the leakage current measured under the V_{DG} of 100 V at 50 ℃ (3.38 μA). From this, it is suggested that the portion of the parasitic leakage component is not negligible at high operating temperature.

Figure 2.19 (a) show the test structure to distinguish the buffer leakage component (vertical) from surface leakage component (lateral) [66]. Bulk leakage is three orders of magnitude higher than surface leakage current. Even though there is a deviation in the reduction of surface leakage current due to the quality of SiN_X passivation layer, bulk leakage current remains similar regardless of passivation. Even though it seems that buffer leakage current is a little high, this experimental result is a concrete example to show that leakage current through the buffer region can be the main factors to deteriorate the blocking characteristics of the device.

From measured gate leakage current, it is verified that peripheral leakage current makes a contribution to the total gate leakage current to some degree. In experiment carried out by Chuan Xu et al (Fig. 2.20) [67], the portion of the each leakage component to the total gate leakage current is investigated in detail. From the experimental results, it is found that leakage current through the AlGaN or etched GaN surface is quite low. Especially, leakage current through the peripheral GaN region is as low as

few decade pA (10^{-11}~10^{-10}). This is similar to the measured leakage current (4.225×10^{-10}A) through the etched GaN region of the fabricated device (Fig. 2. 21). Leakage current (~10^{-8}) originated from mesa side wall was higher than other leakage component. From this, it was verified that most of the leakage current originated from the peripheral GaN region consisted of the leakage passing through the mesa side-wall.



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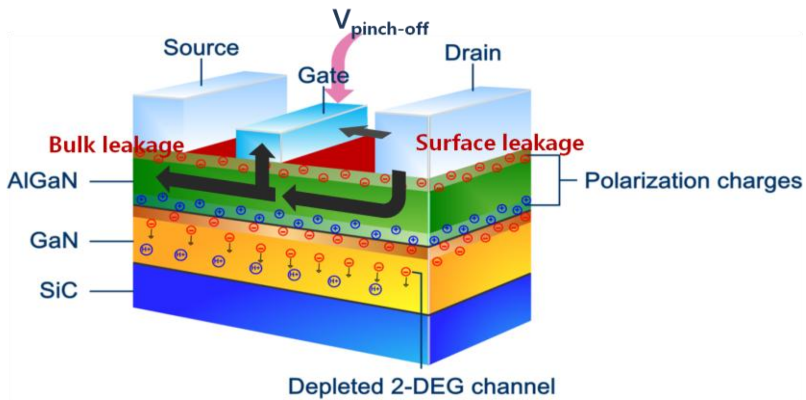


(b)

Figure 2.17 Schematic diagrams illustrating all the possible leakage path of AlGaN/GaN HEMTs in (a) 2-D (b) 3-D view.

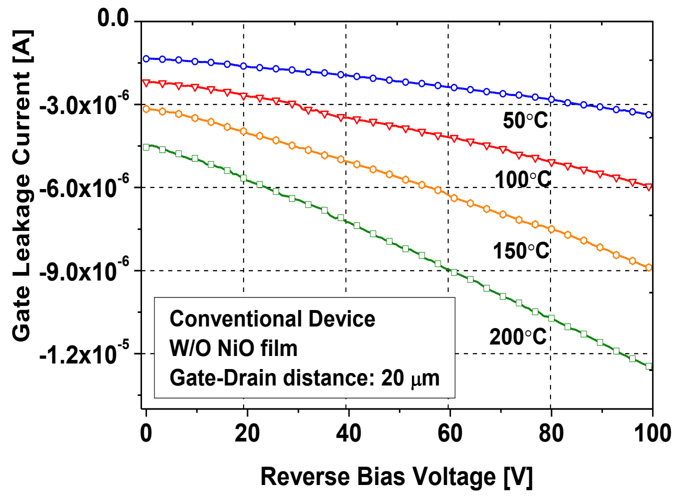
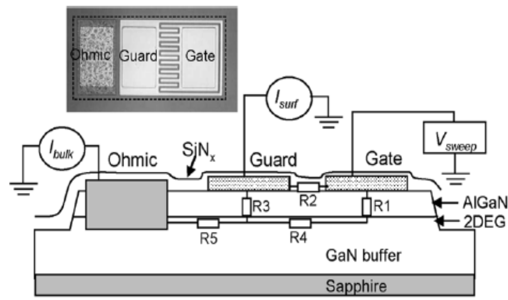


Figure 2.18 Gate leakage current of conventional AlGaN/GaN HEMTs according to various operating temperatures.



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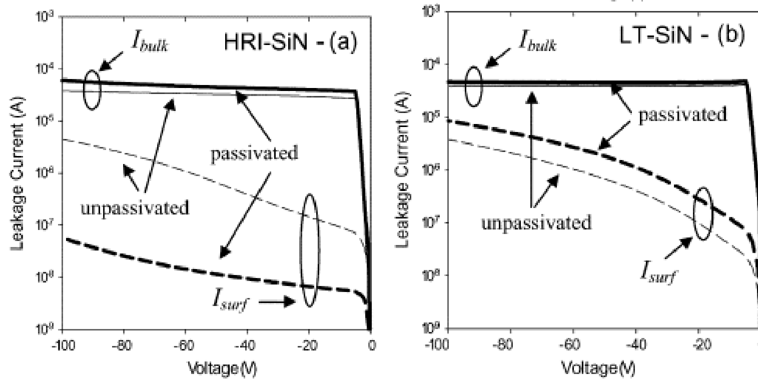
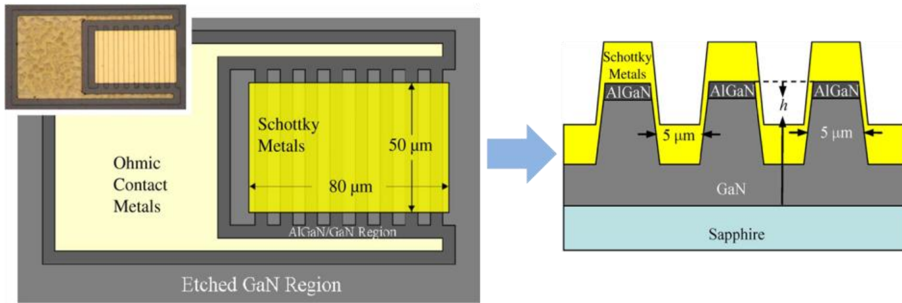


(b)

Figure 2.19 (a) Test structure used to isolate the surface and buffer leakage component. (b) I-V characteristics before (thin line) and after (thick line) passivation [66].



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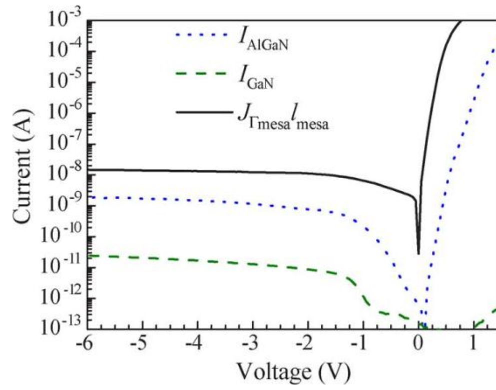
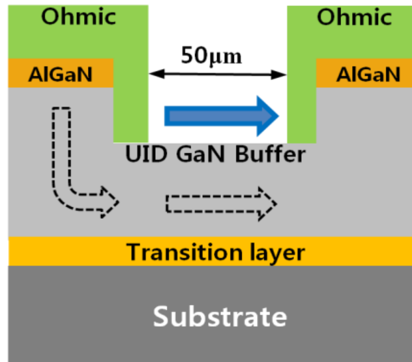


(b)

Figure 2.20 (a) Cross section and top view of ridge-furrow test structure. (b) I-V characteristics of the three leakage components [67].



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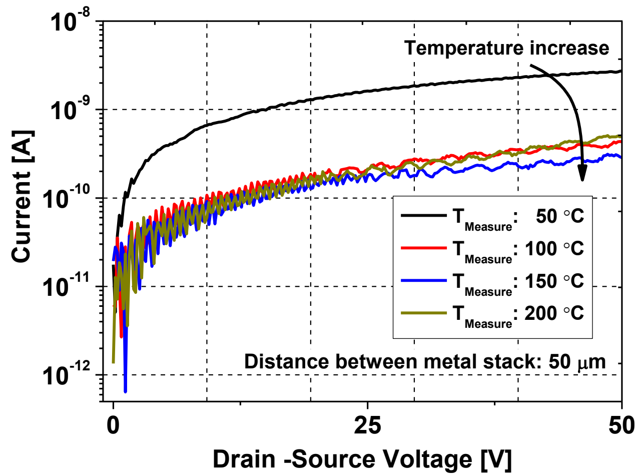


Figure 2.21 (a) Schematic for test pattern to measure the peripheral leakage current (b) Measured peripheral leakage current at various operating temperatures.

2.5.3 Breakdown mechanism and Failure

For power devices, breakdown voltage along with maximum drain current is the most important parameters to estimate the performance of the device. In the power devices with lateral geometry, avalanche breakdown between gate and drain is generally believed to be the mechanism of the breakdown.

Breakdown phenomenon in GaN HEMT is initiated by the operation under off-state where the pinch-off bias is applied to the gate and the drain is positively biased. In the reveres blocking mode, high drain-gate voltage (V_{DG}) is dumped into the drift region between gate and drain electrode. Most of electric field is concentrated on the depletion region formed below the gate electrode accompanying peak of electric field at the drain-side of the gate electrode. Under high-electric-field condition, electrons will inject into the surface of semiconductor (AlGaN barrier or GaN capping layer) due to the poor reliability of the gate. Many trap states distributed on the surface is filled with injected electrons. Carriers in the channel are vertically depleted to keep the system of the heterostructure electrically neutral. As the applied voltage is increased, more electrons are injected into barrier layer and they are trapped by these states. Surface charge resulting from electron trapping moves from the drain-side gate edge towards drain inducing extra depletion region with small contour. This side-gating effect (or virtual gate effect) not only shortens effective drift region between gate and drain but also gives rise to intense local electric field at the end of extra depletion region, which gives rise to

impact ionization and avalanche breakdown in GaN buffer at relatively low reverse bias voltage (Fig. 2.22). This surface charges result in many non-idealities in the forward operation as well.

The drain bias generates a constant electric field (E_X) in the lateral direction (toward drain electrode). Considering the net polarization which is equal to the difference in polarization between AlGaN and GaN, The polarization field E_P in AlGaN layer is as high as several MV/cm and enough to be taken account in the analysis of field distribution. Therefore, total electric field in the depletion region is a combination of lateral component of E_X ($=dV_{DG}/dL_{GD}$) and vertical component of E_P. Total field is expressed as $E_{total}^2=E_X^2+E_p^2$. If the gate-drain drift region is fully depleted by the reverse bias (V_{DG}), the V_{DG} is considered as breakdown voltage (V_{BR}). Then E_{total} is equal to critical electric field of GaN. It is still controversial which component of the E_{total} is dominant (Fig. 2.23).

In the actual power devices, there are two types of degradation. The one is degradation which is reversible. This means that device can operated normally without any degradation after reasonable time to recover its original performance. This is generally attributed to the electron trapping or hot-electron. The other one is permanent irreversible degradation which is called device failure. There are many factors to give arise device failure.

As referred to earlier, in the AlGaN/GaN heterostructure, piezoelectric polarization is based on the mechanism in which the mechanical stress changes into electric field. Under high bias condition, however, mechanical stress occurs due to the electric field, which is called inverse-

piezoelectric phenomenon. If very high voltage is applied to the device in the blocking mode, substantial mechanical strain is applied to the device. As a result, pit-like defect is formed at local region nearby the drain-side gate edge where electric field is concentrated as shown in Fig. 2.24 [68]. Once it is formed on the AlGaN barrier layer, it remains permanently regardless of recovery time. Moreover, the defect evolves into crack, as the frequency of being exposed to high bias condition increases.

Breakdown is one of the irreversible degradations. In general, breakdown leads to the device failure. After an occurrence of breakdown, it is hard for the device to operate as before because all parameters to determine the performance such as on-resistance, output current and leakage current deteriorates severely. If breakdown is accompanied with physical destruction, the device becomes impaired. Most frequently observed physical destruction during breakdown is the burn-out or blow-up of electrode [69]. Fig. 2.25 illustrates microscope image of the AlGaN/GaN HEMT after breakdown. Breakdown event leads to the destruction of HEMT with burn-out or blow-up of the electrode over the channel area. From the wreckage of metal and the trace of migrated metal, the point where the breakdown occurs or leakage path in the active region can be conjectured. As shown in Fig. 2.25, drain and gate metal is destroyed after breakdown. It is the evidence to verify the fact that large lateral electric field exists between gate and drain rather than other active area.

Another event to cause the permanent degradation is buffer breakdown. GaN HEMT grown on Si substrate has dislocations over $10^{10}/cm^2$ due to the large lattice mismatch and thermal coefficient mismatch. It was found

that a screw (vertical) component of the dislocation in GaN buffer is the primary source of the buffer leakage and the density of screw dislocation is strongly associated with the buffer breakdown [70]. Consequently, GaN-on-Si device is more vulnerable to buffer breakdown than that grown on other substrates. Buffer breakdown is also destructive event with the loss of active region including GaN buffer. As shown in Fig. 2. 26, wreckage of buffer breakdown looks like a crater with diameter of few micrometers.

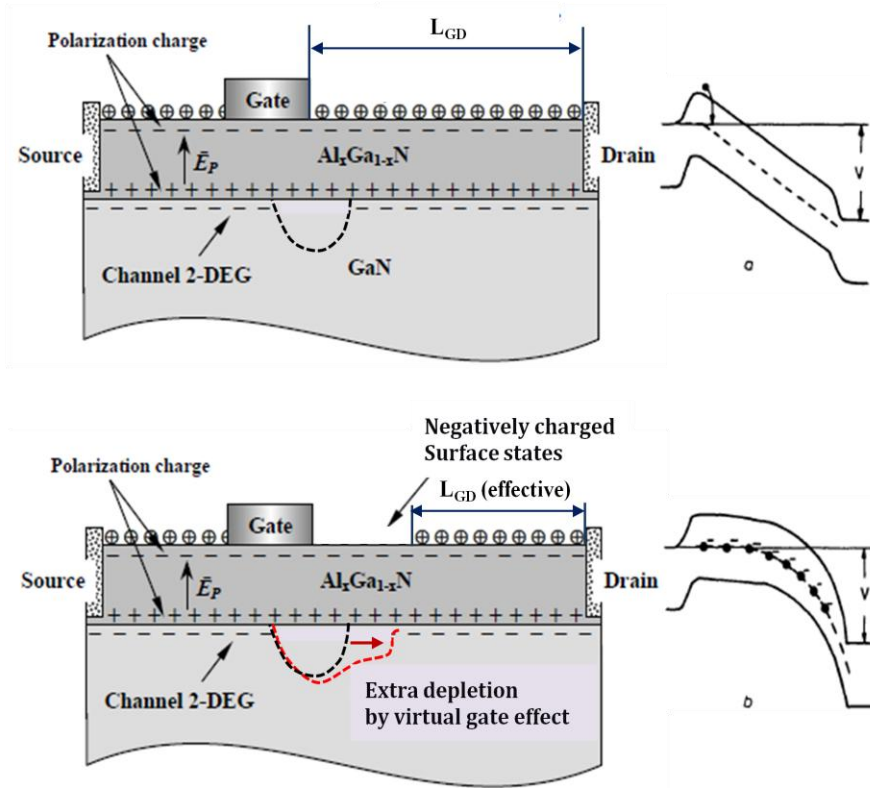
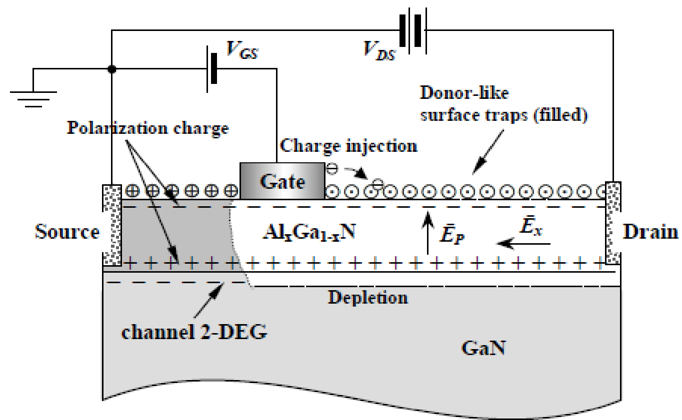


Figure 2.22 Schematic diagrams describing side-gating effect (virtual gate effect) [right] and energy band diagram and field distribution [left].



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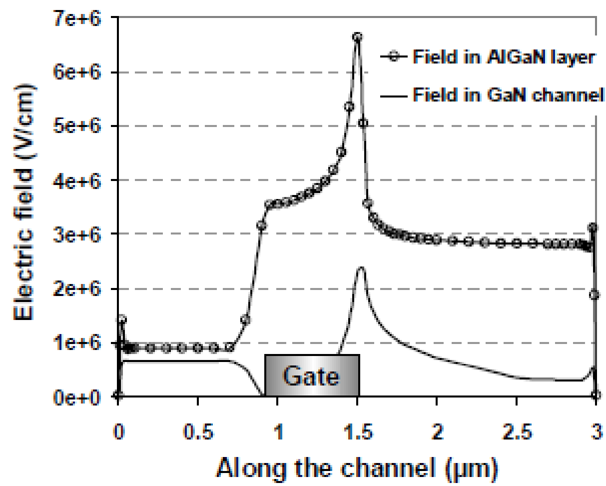


(b)

Figure 2.23 Schematic diagram describing distribution of (a) depletion region, electric field, (b) electric field of the AlGaN/GaN HEMT under off-state (pinch-off and positive drain bias).

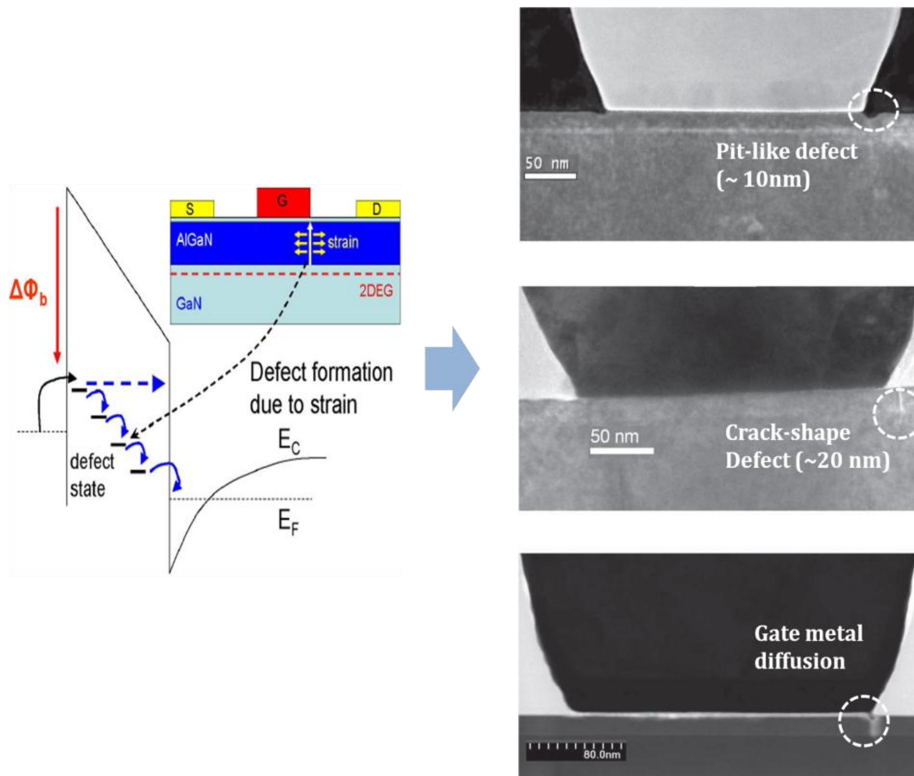
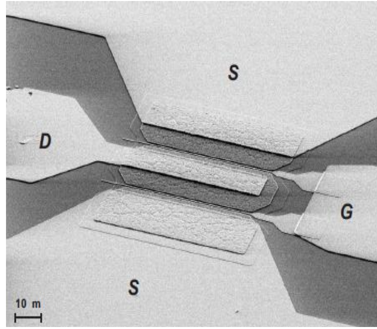
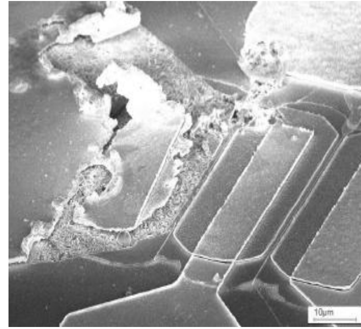


Figure 2.24 Schematic diagram describing the inverse-piezoelectric polarization and microscopic images describing the evolution of pit-like defect due to inverse piezoelectric phenomenon [68].





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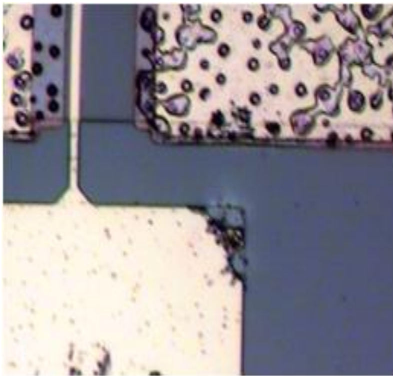
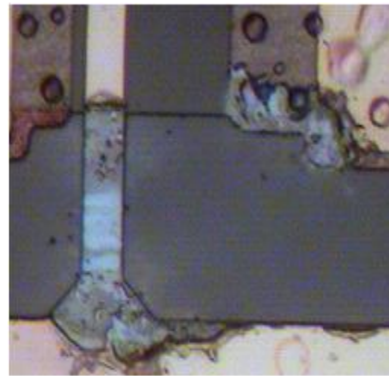




(b)

Figure 2.25 Microscope images of the AlGaN/GaN HEMT after destructive off-state breakdown (a) blow-up of source electrode [69] (b) burn-out between gate and drain electrode.

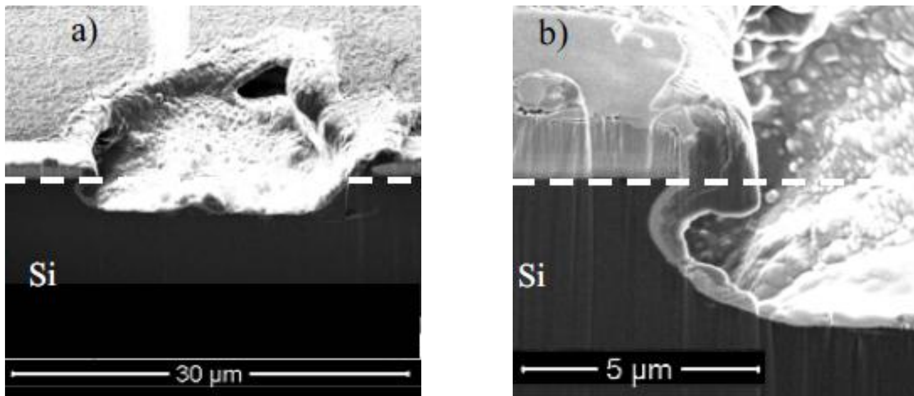
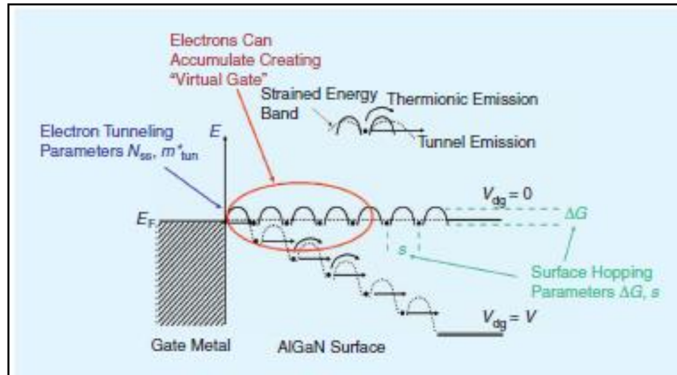


Figure 2.26 Images by Focused Ion Beam: (a) buffer breakdown of AlGaN/GaN HEMTs with deep mesa etching (b) magnification of the left image [70].

2.5.4 Technologies for high breakdown

GaN has emerged as the most suitable candidate for high power device due to its superior material properties such as large bandgap and high electron velocity. However, the performance of the AlGaN/GaN HEMT is still far from the theoretical limit that GaN can approach. Factors that limit the performance of GaN device are primarily gate leakage current and trap-related degradation. Especially, in terms of the blocking capability, gate leakage is the culprit to lower the breakdown voltage of ALGaN/GaN HEMT. As referred to previous section, gate leakage is originated from the electrons which are injected into the surface traps by the large electric field concentrated at the drain-side edge of gate (Fig. 2.27) [71]. In this section, various technologies to improve the blocking capability are introduced.



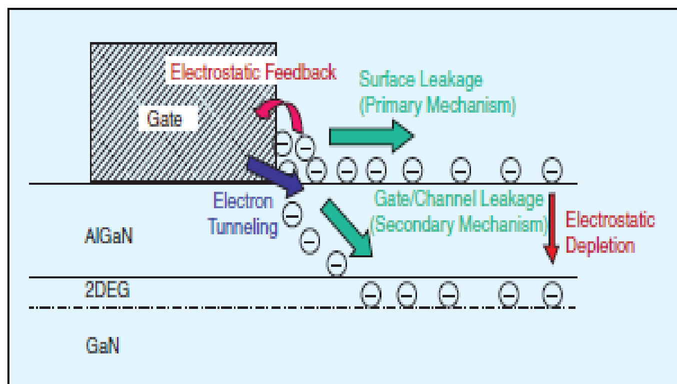


Figure 2.27 Schematic diagram describing electron injection and corresponding results: surface leakage current; virtual gate effect [71].

2.5.4.1 HEMT with Field plate

The breakdown is due to an avalanche that occurs at the drain-side edge of the gate in the blocking mode. It is generally accepted that the extending depletion region toward drain is the most effective way to achieve a high breakdown voltage in the device with planar geometry [72]. MESFET with field plate is typically realized by forming Γ-shape overlapping gate (Fig. 2.28). In the field-plate device, the depletion is extended along the drift region. At the end of the field plate, the second electric field peak is introduced with reducing the first peak at the gate edge. As a result, the breakdown voltage of the device is increased. To achieve the high breakdown voltage, optimum process for the parameters related to the geometry such as the length of field plate (L_{fp}) and thickness of the dielectric (t).

Various types of field plate structures have been reported. Field plate can be applied on the source and drain electrode as well as gate electrode. The HEMT with source field plate, drain field plate and multiple filed plates are shown in Fig. 2. 29. [72-75]. AlGaN/GaN HEMT with multiple field plate and slanted field plate exhibited high breakdown voltage of 900 V and 1900 V respectively (Fig. 2.30) [76-77]. According to Panasonic corp., AlGaN/GaN HEMT with dual field plate (gate and source) on poly AlN dielectric showed a linear dependency of breakdown voltage on gate-drain length (L_{GD}) and achieved the highest breakdown voltage of 10400 V at the L_{GD} of 125μm (Fig. 2. 31) [78]. Recently, HRL has announced that

normally-off AlGaN/GaN HEMT of high performance by employing multiple field plate. It is reported that the packaged device exhibited breakdown voltage of 1200 v and maximum drain current of 2 A with the threshold voltage of 0.64.

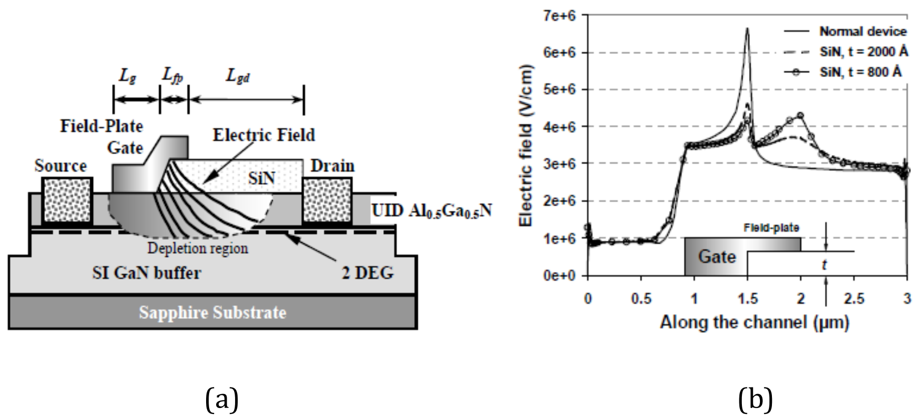
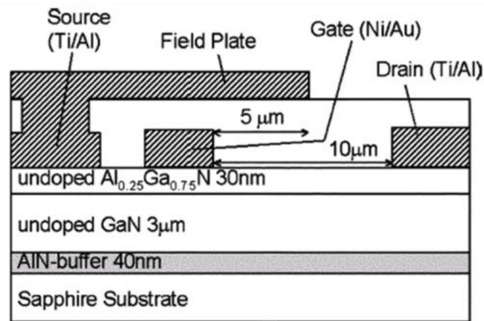


Figure 2.28 (a) Structure of the AlGaN/GaN HEMT with field plate, (b) comparison of electric field for the HEMT with field plate and normal HEMT, (c) Microscope image of HEMT with field plate.



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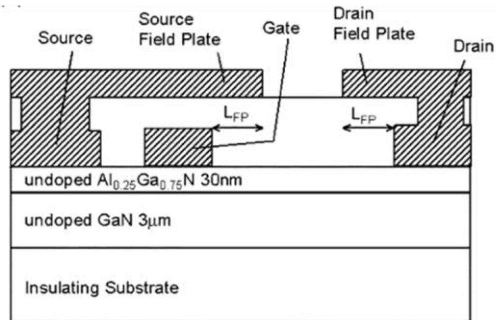
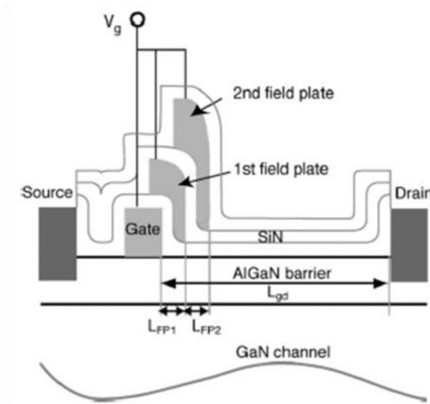
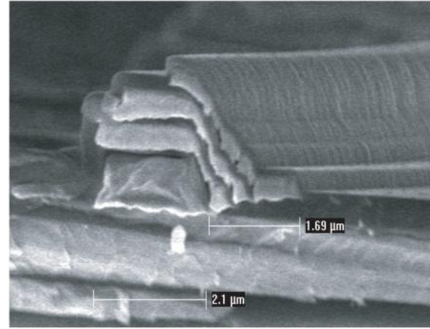


(b)

Figure 2.29 Device structure of HEMT with (a) source field plate (b) dual field plate (source and drain).





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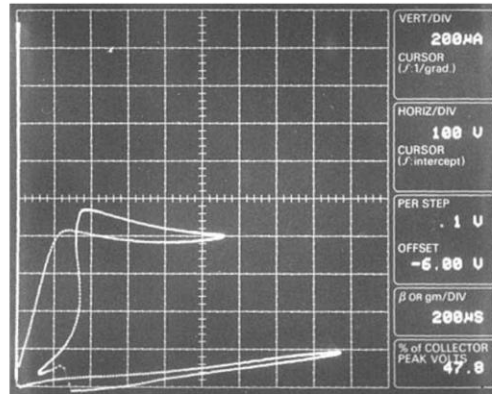
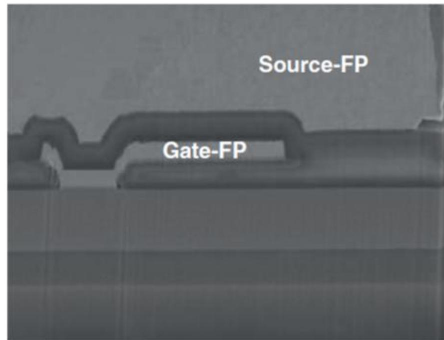


(b)

Figure 2.30 (a) Device structure of AlGaN/GaN HEMT with multiple field plate and microscope image of the fabricated device (b) measured breakdown of the AlGaN/GaN HEMT with multiple field plate.



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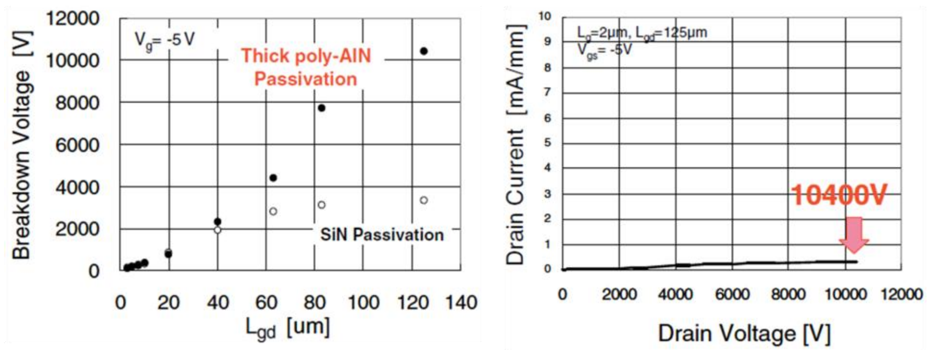


(b)

Figure 2.31 (a) Microscope image of AlGaN/GaN HEMT with dual field plate (b) dependency of breakdown voltage (V_{BR}) on gate-drain length (L_{GD}).

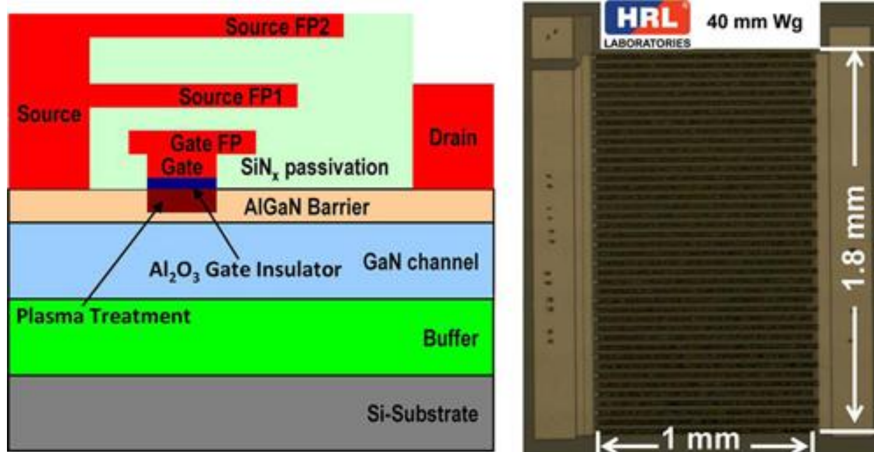


Figure 2.32 Schematic of AlGaN/GaN HEMT with multiple field plate and microscope image of the fabricated device.

2.5.4.2 HEMT with passivation

AlGaN/GaN HEMT devices suffer from degradation at both high voltage and high frequency operation. Surface passivation of these devices with silicon nitride has been reported to reduce current collapse and microwave power degradation for AlGaN/GaN HEMTs [79]. The spectrum of insulator is wide. SiO_2, Si_3N_4, AlN, MgO, ZrO_2 have been studied by many research groups [80-85]. The most widely used dielectric materials are SiO_2 and Si_3N_4. In terms of gate leakage current, reported results are still controversial. Gate leakage is reported to increase [86] and also to decrease [87] after Si_3N_4 passivation. It is well-known that Si_3N_4 passivation eliminates the current dispersion of GaN HEMT and improves the output power density of microwave HEMT. Thus Si_3N_4 is applied to passivation or gate dielectric of high voltage GaN HEMT to reduce the dispersion, but it also increase the gate leakage and hence resulted in low breakdown voltage. The SiO_2 passivated HEMT suffers from large dispersion due to its slow switching speed. However, the gate leakage of the SiO_2 passivated device is much lower than the Si_3N_4 passivated one.

To combine the advantage of low dispersion from Si_3N_4 passivation and low leakage current from SiO_2 passivation, double layer passivation or double layer gate dielectric have been tried (Fig 2.34) [88]. As a result both the low dispersion and high breakdown voltage over 1000 V was achieved.

It is generally accepted that electron-trapping is caused by high drain-

source voltage (V_{DS}) during device operation (forward/reverse). The charged surface states due to the electron trapping moves from gate edge to drain with causing strong local electric field. Assuming a large amount of states on the device surface, electrons injected into the surface are swept easily by the local electric field resulted from charged surface states. It is a kind of process with positive feedback. The more electrons are trapped by the surface states, the stronger local electric field is induced. The strong local electric field reduces the surface potential of the region where the charged surface states are positioned as shown in Fig. 2. 33. This event is accelerated during the reverse blocking operation. It gives rise of breakdown at the surface of the device when the local electric field is over the critical electric field (E_C) of the semiconductor (AlGaN). In order to avoid the surface breakdown, encapsulation of the surface states through the passivation process is required. In the passivated device, electron trapping as well as electron injection is suppressed by insulator. Consequently, premature breakdown is prevented and blocking capability of the device is improved.

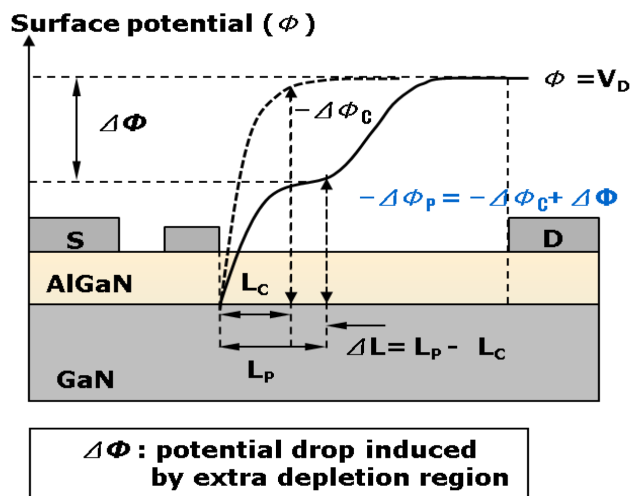


Figure 2.33 Schematic diagrams describing distribution of the surface potential of the AlGaN/GaN HEMT in the blocking mode.

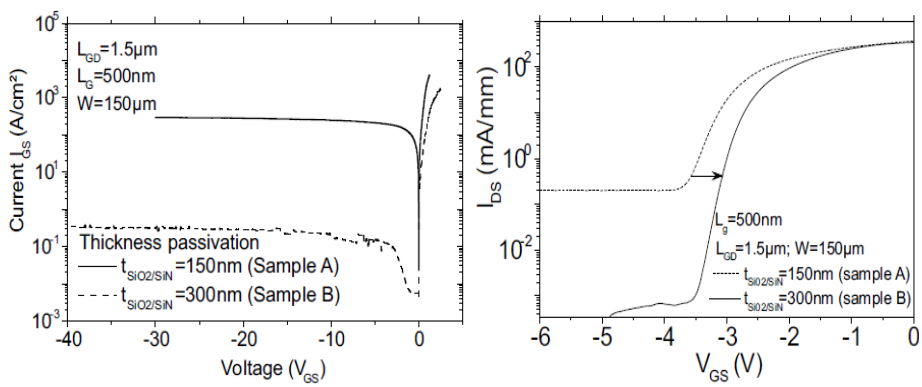


Figure 2.34 I-V characteristics of AlGaN/GaN HEMTs with SiO_2/Si_3N_4 double layer passivation.

Chapter 3

3. AlGaN/GaN HEMT Employing NiO_X Interfacial Layer

3.1 Overview

In this work, properties of the AlGaN/GaN heterostructure on sapphire substrate (Al_2O_3) and the characteristics the fabricated device employing nickel oxide as an interfacial layer were presented. After the HEMTs were realized except gate formation, optimization in the process condition of the nickel oxide interfacial layer was performed. The investigations on the device performance were a subject of the later part of this chapter (in chapter 3.4). Device operation in the blocking mode such as leakage current and breakdown of the device was explained with plausible mechanisms to explain these phenomena. The investigation toward the effect of the nickel oxide on the blocking capability was based on the experimental results. Not only simple electrical measurements but also measurement under various operation temperatures was carried out to evaluate the robustness of the proposed devices in the harsh condition.

EL (Electroluminescence) analysis was used to investigate the effect of the nickel oxide layer on the reverse operation as well. To illuminate the mechanisms of how devices with nickel oxide interfacial layer achieve the stable blocking characteristics, SIMS (Secondary ion mass spectroscopy) analysis was carried out.

3.2 AlGaN/GaN HEMTs on SiC Substrate

3.2.1 Advantage of SiC substrate

AlGaN/GaN HEMTs used in this work were grown on SiC substrate by MOCVD (Metal Organic Chemical Vapor Deposition) technique. Through the development of AlGaN/GaN HEMTs, two substrates: sapphire (Al_2O_3) and SiC, have dominated. Sapphire was the traditional substrate for MOCVD of GaN due to its moderate price. Despite its competitive price, sapphire substrate had a few drawbacks. It was known that a large number of threading dislocations existed in the GaN film on sapphire substrate due to large lattice mismatch (~14%) between GaN and Sapphire. The density of the threading dislocations for GaN on sapphire substrate was reported to be up to 1×10^{11}. Threading dislocations were associated with electronic states called traps within the band gap [89]. Keller observed an inverse correlation between electron Hall mobility and dislocation density [90]. The result of Weimann and Ng indicated that dislocation scattering must be considered in the mobility analysis, when the density of threading dislocation was over 10^8 [91-92]. It was shown that the dislocation related scattering was dominant below a certain electron concentration. As noted above, dislocations of high density had an adverse effect on carrier transport of the device with degradation in forward characteristics.

Because the AlGaN/GaN HEMT is the device with lateral structure, semi-insulating material beneath the device structure is required to intact

lateral conduction in forward operation and sharp pinch-off in reverse operation. For the semi-insulating buffer layer, it was required to reduce the background carrier concentration in GaN buffer. However, it was reported that even un-doped GaN grown by MOCVD on sapphire substrate typically exhibited n-type conductivity presumably due to unintentional doping by oxygen impurities [93]. It was known that oxygen impurities rather than nitrogen vacancy were the major source of residual electrons [94]. During the initial stage of GaN growth on sapphire, oxygen comes from the impurities in the ambient gases during wafer loading or from the out-diffusion from the sapphire substrate [95-96]. As reported, substrate itself can be a source of oxygen, which results in a highly oxygen doped region near the sapphire interface [97-98]. It was unfavorable to the carrier confinement in the device with lateral structure in terms of the carrier transport in the forward operation and leakage current in the reverse operation. In addition, devices especially for power-critical applications should take account of problems related to the heat from device during operation. Thermal conductivity of the sapphire is 15 times lower than that of sapphire. R. Gaska et al. showed that temperature rise for HEMTs on sapphire substrate can be 10 times higher in comparison with that of the HEMTs on SiC substrate [99]. Consequently, SiC substrate has been used as an alternative after semi-insulating SiC substrate was available. SiC has since then held a firm position of substrate for high power devices due to its high thermal conductivity (3.8 W/cm·K) and small lattice mismatch to GaN (3.5 %) contrary to sapphire.

3.2.2 Properties of HEMTs on SiC substrate

AlGaN/GaN heterostructure were grown by MOCVD method. AlGaN/GaN heterostructure used in this work was grown on SiC substrate. Transition layer, often called as SRL (Strain Release layer), was grown in the first to relive a mechanical stress caused by large lattice mismatch. Then, a series of the constituent layers of the HEMTs were grown followed the transition layer. Hall measurement was carried out to investigate the quality of the AlGaN/GaN heterostructure on SiC substrate. Hall measurement is a method commonly used for characterization of semiconductor. It provides information about the key parameters to majority type concentration and mobility. It is generally accepted that channel conductivity of HEMT (MESFET) was investigated using this method.

For the Hall-effect measurements, three test patterns were co-fabricated per one die (diced piece). The Hall structures, similar to windmill, consisted of an isolated mesa island. The whole area of test patterns was 1.5 mm×1.5 mm^2. Each test pattern had four Ti/Al/Ni/Au (20/80/20/100 nm) based contacts (area 496 × 496 μm^2) placed at the each vane of the pattern. Electrical contact to 2DEG was achieved by the annealing at 880℃ for 30 sec in the N_2 ambient. Measurement was performed at the room temperature (300 K). Measured value of carrier concentration (n_s) of the 2DEG and mobility of the heterostructure on SiC substrate were summarized in the table 3-1. The balanced value of carrier concentration and electron mobility of the heterostructure on SiC

substrate was 9.63×10^{12} cm^{-2} and 1.47×10^{3} $cm^{2}/V \cdot s$ respectively. Electron mobility (μ_n) was in a correct inverse proportion to carrier concentration (in table 3-1, test pattern #3), electron mobility extracted in the test pattern with high concentration over 13 orders of magnitude ($>10^{13}$) was slightly decreased due to the scattering of channel carriers. A high $\mu_n \cdot n_s$ product of the heterostructure guaranteed a high conductivity and low on-resistance (R_{ON}) in the access region of the device. It was reflected in a parameter of sheet resistances (R_{sq}) of the hall test pattern.

Table 3-1 Measured Hall parameters of the heterostructure grown on SiC substrate

Hall parameters (at 300 K)	SiC substrate			
	#1	#2	#3	Aver.
n_s [cm^{-2}]	7.15×10^{12}	7.24×10^{12}	1.45×10^{13}	9.63×10^{12}
μ_n [$cm^2/V\cdot s$]	1.8×10^{3}	1.79×10^{3}	8.23×10^{2}	1.47×10^{3}
R_{sq} [$\Omega/\square$]	485	482	524	497

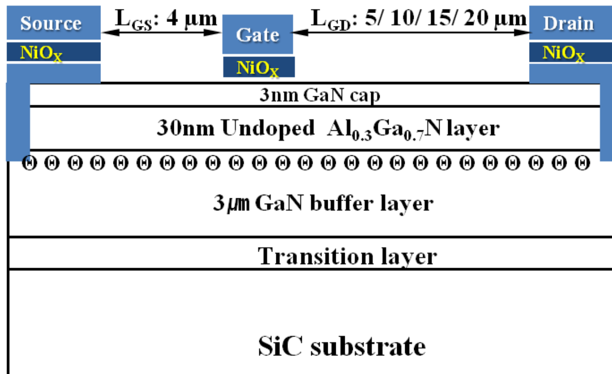
3.3 Device fabrication

Device used in this experiment are fabricated using AlGaN/GaN heterostructure with Al composition of 30% was grown by MOCVD on SiC substrate. Epitaxial structure began with transition layer, which released mechanical strain between Si substrate and GaN buffer. Even though lattice mismatch between SiC and GaN was relatively low (14 %) [100], an insertion of transition layer reduced the dislocations due to mechanical strain. Then GaN buffer layer was grown on transition layer. The total thickness of the GaN buffer was about 3 μm. Electron channel (2DEG) with the density of the late twelve orders of magnitude (9.63×10^{12} cm^{-2}) was formed at hetero interface between GaN buffer and unintentional doped AlGaN barrier. The thickness of AlGaN barrier layer was 30 nm. The hetero structure was topped with a 3 nm-thick GaN capping layer for the protection of the device. Cross-section of the AlGaN/GaN HEMT used in the experiment was illustrated in Fig. 3. 1.

The fabrication process stated with device isolation. Each transistor was electrically isolated through the inductively coupled plasma (ICP) etching process using Cl_2-based gas mixture. Depth of the etched region was about 140 nm. After mesa isolation process, pre-treatment with chemical solutions using diluted acid solution (HCl: H_2O_2: DI=1:1:6 in volume ratio, for 5min) and diluted alkaline solution (NH_4OH: DI=1:5 in volume ratio for 5 min) was carried out at room temperature to remove possible oxide formed during ICP etching. Hydrophobic property was shown at the surface of the active region after pre-treatment. Then photolithograph

was performed to define the foot-print of the ohmic contact (Source/Drain) metals. After defining window for source and drain electrode, surface treatment using BOE (HF: NH_4F =1:10 in volume ratio for 30 sec) was carried out again for the clean surface. Ti/Al/Ni/Au (20/80/20/100 nm) based Ohmic contacts were deposited by e-gun evaporation then annealed at 880℃ in N_2 ambient for 30 sec. 20nm-thick Ni thin film was g-gun evaporated with the deposition rate of 3 ~4 Å/sec. Atomic density of the deposited Ni film was 8.9 g/cc (cm^3). Thermal oxidation was carried out for the formation of the NiO_X interfacial layer using the furnace at various oxidation temperatures in the oxygen ambient with flow rate of 4.5 SLPM (standard liters per minute). Properties of the NiO_X film were dependent on the conditions where the NiO_X film was formed. Specific explanation on the various properties of the NiO_x film was the subject of the next chapter.

The final step of the process was to form Ni/Au gate contact by e-gun evaporation. Gate lengths of the device were 3 or 5 μm. Widths of the gate electrode were 50 /100 μm. Various gate-drain spacing (L_{GD}) from 5 to 20 μm was employed to investigate the dependency of breakdown voltage on the L_{GD}.



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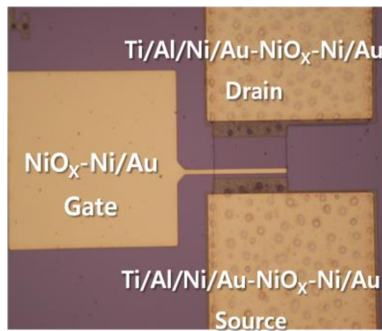


(b)

Figure 3.1 (a) Schematic describing epitaxial structure (b) Microscopic image of the fabricated AlGaN/GaN HEMTs employing NiO_x interfacial layer.

3.4 Properties of the nickel oxide film

Among the many candidates for the gate electrode metals (in table 2-2), nickel (Ni) has been a choice of many research groups for the Schottky contact. Nickel has been used as a gate electrode in the AlGaN/GaN HEMTs due to its high work function (5.15 eV) which is essential to establish a high barrier height to AlGaN/GaN structure.

Nickel oxide (NiO_X) film has been used in various categories of the electronic devices due to its diverse material properties such as transparency, resistive switching, high work function (≥ 5.15 eV). It is well-known that NiO_X layer is a transparent conducting electrode (TCE) and used as a constituent layer of the transparent electrode stack in the thin film transistors (TFTs), and solar cell [101-103]. Memory device employing resistive switching property of the NiO_X film has been a subject of the active research [104-107]. It has been generally accepted that NiO_X was a p-type material and used as p-type layer of the hetero junction in rare instance [108-110]. In case of the GaN related devices, NiO_X was used as an ohmic metal to p-type GaN (Mg-doped GaN), especially GaN based LED devices [111-112]. Recently, Application of NiO_X in the GaN-based power devices has been reported. N. Ganeko et al. realized the enhancement-mode AlGaN/GaN HEMTs with threshold voltage of 0.8 V by employing a NiO_X gate electrode in the recessed AlGaN/GaN HEMTs as a complementary method to shift the V_{TH} more positive direction [113]. Some groups have tried to utilize the NiO_X film as a gate dielectric material. R. Lo Nigro demonstrated GaN and SiC devices on which

crystalline NiO_X film was grown by metal organic chemical vapor deposition (MOCVD) method. Fabricated MIS diode with NiO_X film showed clear diode characteristics [114]. C. S. Oh et al. fabricated the MOS-HEMTs using NiO_X film formed by thermal oxidation of Ni films at 600 ℃ for 5 min. Fabricated device showed a typical characteristics of the AlGaN/GaN HEMTs with MOS structure such as the negative shift of the threshold voltage (from -5 V to -5.9 V) and reduction of the gate leakage current by four orders of magnitude [115]. However, there was no evidence to prove the insulation property of the NiO_X film thermally oxidized at the same oxidation temperature (600 ℃).

3.4.1 Resistive switching property of the NiO_X

In our work, properties of the NiO_X film were dependent on two process parameters: oxidation temperature and atomic density. Thermal oxidation process increased the resistivity of the NiO_X film. Except for inflection point at the 550 ℃, the resistivity of the NiO_X film was saturated over specific oxidation temperature of 300℃ (shown in Fig. 3. 2). At the temperature of 600 ℃, resistivity of the NiO_X was even lower than that of the NiO_X film oxidized at 500 ℃, which conflicted with results that R. Lo Nigo and C. S. Oh demonstrated. The effect of the resistivity of the NiO_X film on the device performance will be explained in chapter 3.5 (Device performance).

On the contrary to the NiO_X film made up of Ni e-gun evaporated with deposition rate of 2~3 Å/sec, NiO_X film with high atomic density (from Ni film e-gun evaporated with deposition rate of 0.1 Å/sec) exhibited a resistive switching property. To confirm the resistive switching characteristic of the NiO_X film of high atomic density, test structure was co-fabricated in the same die (diced piece of the epi-wafer with the same heterostructure). Test structure was composed of two electrodes on the NiO_X film (Schottky contact) and one electrode to AlGaN/GaN Heterostructure (Ohmic contact) as shown in Fig. 3.3. Bias applied to the test structure was as follows: Ground at Ohmic (drain) electrode and -10 V at G1 electrode. When the bias was applied to G1, horizontal current flowing NiO_X was detected by electrode G2 and vertical current flowing though routes other than NiO_X was detected by Ohmic electrode. Resistive

switching of the NiO_X film was confirmed by the drastic change of leakage current of the test structure.

Figure 3.4 (a) showed the I-V characteristics of the test structure on which NiO_X film was deposited under various oxidation temperature. Resistive switching characteristic was characterized by the leakage current passing through the NiO_X film and barrier layer of the heterostructure. Resistive switching characteristic become obscure as oxidation temperature increased. Test structure with NiO_X film oxidized at the temperature in the range from 400~450 ℃ showed a definite switching characteristics. The criterion to evaluate the switching characteristic was the ratio of the resistance extracted from the leakage current in the Set (Low resistance state, LRS) and Reset (High resistance state, HRS) operation. Measured leakage current through the NiO_X film and 13.752 mA and total leakage current detected at the drain electrode was 13.864 mA as shown in Fig 3.4 (b). It reflected that the most the leakage current of the test structure consisted of a surface leakage component (leakage current through the NiO_X film), which indicated that thermally oxidized NiO_X film was not an insulator and barrier layer of the heterostructure including GaN capping layer suppressed the electron injection effectively.

Figure 3.5 showed I-V characteristics of the test structure employing NiO_X film thermally oxidized at 400 ~ 450℃. Curves shown in Fig 3.5. were quite similar to the typical current-voltage characteristics that vertical MIM (metal-insulator-metal) diode exhibited during set and reset operation as shown in Fig. 3.6 [108-109]. In Fig. 3.5 (a), measured current

in the LRS and HRS were 1.386×10^{-2} A and 6.5×10^{-7} A respectively. Extracted resistances from two regimes were 46.88 Ω and 1.23×10^{7} Ω respectively. A ratio of the resistance in the HRS to LRS was about five orders of magnitude (2.63×10^{5}). The ratio (R_{HRS}/R_{LRS}) calculated from Fig. 3. 5 (b) was about four orders of magnitude (8.45×10^{4}). The difference in resistance between HRS and LRS or the ratio of resistance in HRS to LRS was directly led to a memory window of the device with MIM structure.

However, in case of the AlGaN/GaN HEMTs employing patterned NiO_X film below the main gate, contrary to vertical MIM diode, NiO_x film does not act as a channel in which electrons flew. Consequently, such a wide memory window (4 ~5 orders of magnitude) cannot be observed in the I-V curve of the HEMTs with NiO_X film of high atomic density. NiO_X film between semiconductor and main gate acted as an embedded potentiometer due to its resistive switching property. When the gate bias was over a threshold voltage where resistive switching occurs (from LRS to HRS), actual bias applied to semiconductor was smaller than its original value due to voltage drop across the NiO_X film with high resistance. While the gate bias was below the threshold voltage, nearly original gate bias was applied to semiconductor. The difference in the actual bias applied to semiconductor directly led to the difference in drain current as shown in Fig. 3. 7. Memory window was defined as disparity in drain current at the threshold voltage (0.8 V). Measured memory window of the AlGaN/GaN HEMTs with NiO_X with high atomic density was 180 mA/mm (I_{DS} in 'Set'= 484 mA/mm, I_{DS} in 'Reset'= 304 mA/mm).

The plausible mechanism of the resistive switching observed in the NiO_X

film is based on the hypothesis related to Ni filaments. Under high electric field, Ni atoms in the grain boundary are assembled into conducting filaments (Ni filaments) in the NiO_X film. The cluster of percolating Ni filaments acts as a path for current in the film. A conductivity of the NiO_X film is fully dependent on the density of conducting filaments. Low resistance state of the NiO_X film is attributed to the conducting Ni filament of high density. As shown in Fig. 3. 8 (b) [-], yellow lines in the TEM image indicates the Ni filaments in the NiO_X films. However, over the critical electric field, Ni filaments are disrupted simultaneously. This event causes the resistance of the NiO_X film increased drastically. Device with NiO_X film in this bias range do the reset operation.

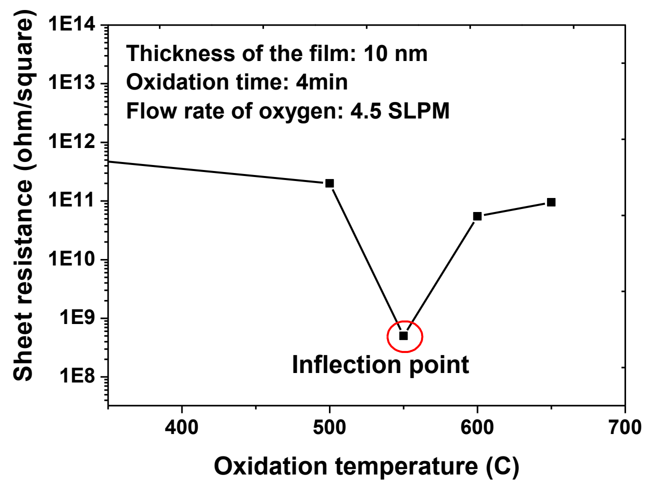


Figure 3.2 Sheet resistivity of the nickel oxide film as a function of oxidation temperature.

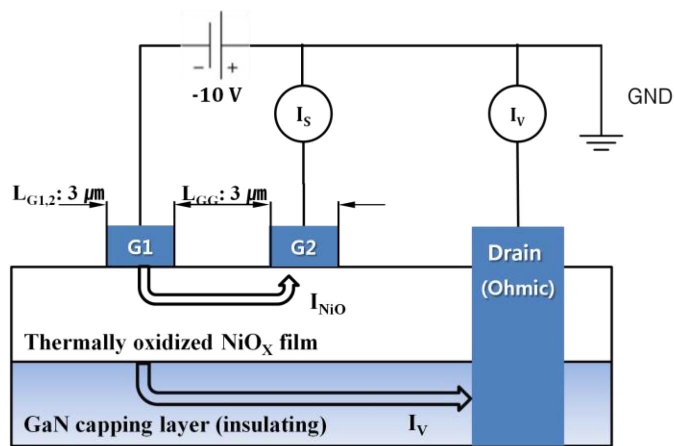
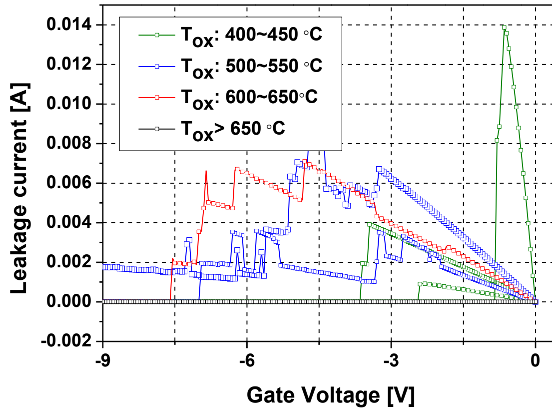


Figure 3.3 Schematic diagram describing test structure to measure resistive switching characteristics of the NiO_x film.



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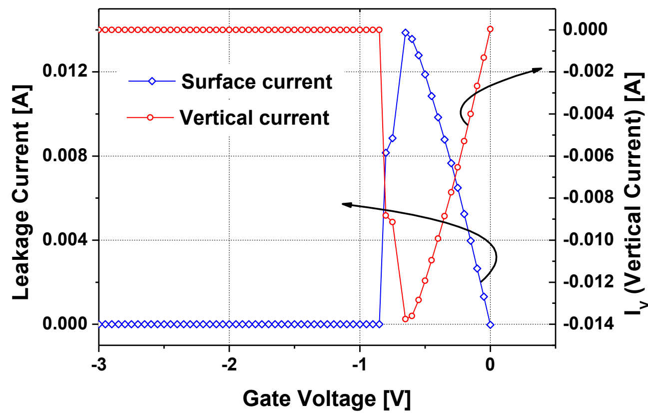

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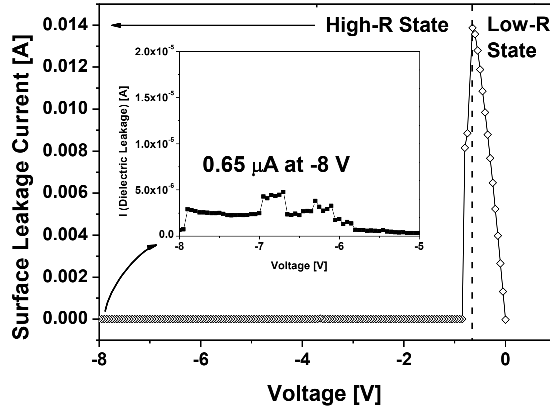
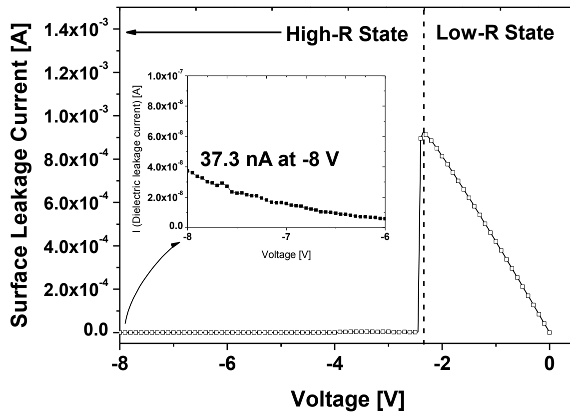
Figure 3.4 Resistive switching characteristics of the nickel oxide film (a) total current (b) classification of the current into $I_{VERTICAL}$ and $I_{HORIZONTAL}$.

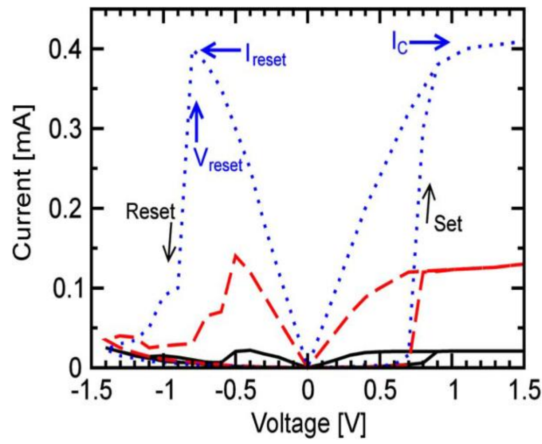


(a)



(b)

Figure 3.5 Transition of the resistivity of NiO_X film oxidized at 400~ 500 ℃ from low resistivity (LR) to High resistivity (HR).



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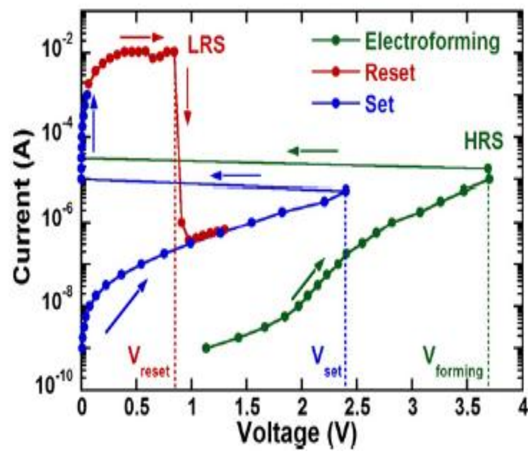


(b)

Figure 3.6 Typical current-voltage characteristics measured during set and reset operation ((a) [104], (b) [105])

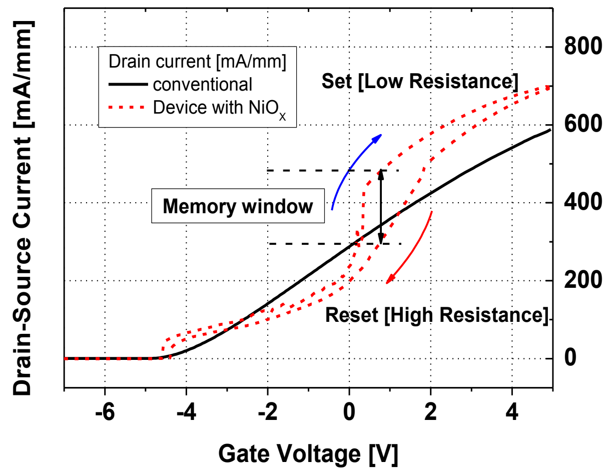
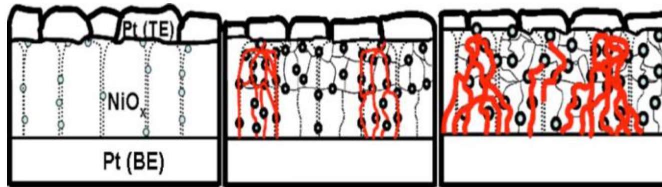
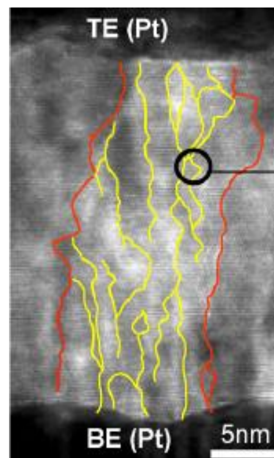


Figure 3.7 Current-voltage (I-V) characteristics of the AlGaN/GaN HEMTs employing a NiO_X film with resistive switching property below the main gate (Ni/Au). [Memory window: ΔI_{DS}= 180 mA/mm at V_{GS}= 0.8 V]



(a)



(b)

Figure 3.8 (a) Schematic diagram explaining mechanism for resistive switching of the NiO_X film [107], (b) TEM image describing the formation of the NiO_X filament cluster [106].

3.5 Device performance

3.5.1 Forward characteristics

3.5.1.1 Threshold voltage

Figure 3.9 (a) shows the transfer characteristics of the fabricated AlGaN/GaN HEMTs employing NiO_X interfacial layer. Threshold voltage (V_{TH}) of the device was defined by a constant current method (at the gate voltage (V_{GS}) where the drain current was 1mA/mm). Threshold voltage of the proposed device was increased as oxidation temperature of the Ni film was increased. Threshold voltage of the AlGaN/GaN HEMTs with NiO_x film oxidized at 500℃ was -4.45 V, which was shifted by 0.3 V toward positive direction from -4.75 V (V_{TH} of the conventional device) (Fig. 3.10). It was an evidence to prove the upward shift of the energy band, which could be confirmed again in the extracted barrier height of the proposed device later. Modification of the energy-band structure was attributed to stoichiometry change of the surface of the heterostructure. In case of the HEMTs, gate is capacitively coupled to channel of the device. Insertion of the dielectric layer between heterostructure and gate electrode reduces gate-source capacitance (C_{GS}). Under the assumption of the same gate-source capacitance (C_{GS}), more gate bias is required to induce or pinch off the channel, i.e. more gate bias for the same drain current, more negative bias for the pinch off the channel. In that sense, NiO_X film inserted between main gate and heterostructure was proved not to be a dielectric material again..

3.5.1.2 Transfer characteristics

Transfer characteristics of the proposed device showed a dependency on the oxidation temperature under the condition of fixed gate-drain spacing (L_{GD}) of 10 μm (shown in Fig. 3.9 (a)). As oxidation temperature increased, maximum drain current of the device decreased. Drain current of the device was measured at the V_{GS} of 2 V and V_{DS} of 10 V. Measured drain current of the conventional device was 588.4 mA/mm, while those of the proposed device with NiO_X film oxidized at 400 ℃ and 500 ℃ were 540.4 and 442.5 mA/mm. Comparing with drain current of the conventional device, drain current of the proposed device with NiO_X film was reduced by 8.15 and 24.8 % respectively. The reduction of the drain current in the transfer characteristics was attributed to the reduced actual bias applied to heterostructure. As referred in previous chapter 4.4, resistivity of the NiO_X film was higher than that of the Ni film. When it was inserted below the main gate (Ni/Au), the series resistance of the gate metal stack was increased (Fig. 3.9 (b)). It reduced actual gate bias which controlled the channel.

A simple and rough approximation for the drain current (I_{DS}) can be expressed as $I_{DS} = W_G \cdot q \cdot n_s \cdot v$ where n_s is the carrier concentration of the channel (2DEG). It is a function of the gate voltage, strictly actual gate voltage applied to heterostructure. Assuming a condition of the fixed gate-source capacitance, carrier concentration (n_s) is a function of V_{GS} for the whole bias range in the forward operation as follows:

$$n_s = \frac{C_{GS}}{q \cdot L_G \cdot W_G}(V_{GS} - V_{TH})$$

In conventional HEMTs with Ni/Au gate, series resistance of the gate metal stack as small as it could be neglected. However, in the expression for the carrier concentration of the HEMTs with NiO_x film, series resistance of the metal stack was too large to be neglected and included in the expression as a form of voltage drop across the NiO_X film.

$$n_s = \frac{C_{GS}}{q \cdot L_G \cdot W_G}(V_{GS} - V_{DROP} - V_{TH})$$

Comparing with the device with Ni/Au gate, actual voltage applied to semiconductor of the device with NiO_X film was much lower than the voltage applied to gate electrode. Consequently, in the AlGaN/GaN HEMTs with NiO_X film, the channel carrier induced by the same gate voltage was lower than that of the conventional HEMTs. It was reflected in a lower drain current in the transfer characteristics.

The degradation of the transconductance also could be explained in the same extend. In general, transconductance is the one of the representative indices to show the gate controllability. Intrinsic transconductance (g_m) can be obtained by differentiating the drain current with respect to the gate voltage (V_{GS}) source and expressed as follows [116]:

$$g_m = \frac{C_{GS}}{L_G} \cdot \left(1 - \left(1 + 2 \cdot \frac{V_{GS} - V_{TH}}{V_C}\right)^{-\frac{1}{2}}\right) \cdot v_{sat} \text{ where } V_C = L_G \cdot E_C$$

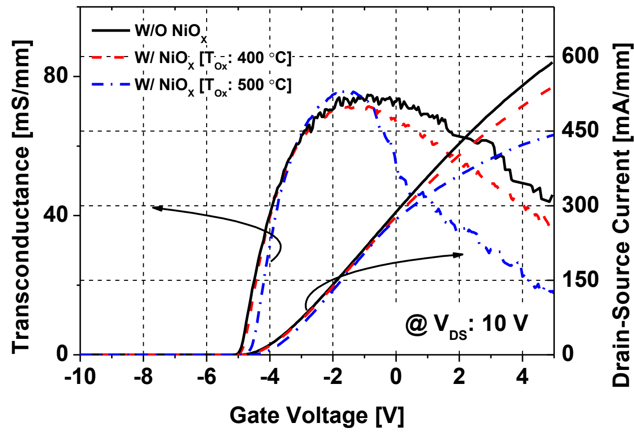
Because the NiO_X film was not a dielectric material, C_{GS} remained nearly constant. Presuming that other parameters were fixed, the only variable to impact on the g_m was gate voltage. Along with the carrier concentration (n_s), transconductance also was a function of the gate voltage. In the above expression, V_{GS} should be substituted by V_{GS}-V_{DROP}. Lower transconductance than that of the conventional device was expected. Maximum transconductance of the devices obtained at the gate voltage of -2 V was similar irrespective of NiO_X film. Measured $g_{m\,MAX}$ of the device with NiO_X film oxidized at 400 and 500 ℃ were 72.5 and 73.5 mS/mm respectively and that of the conventional device was 74.7 mS/mm. However, as the gate voltage increased, disparity was increased. At the V_{GS} of 1 V, g_m of the conventional device was 69.2 ms/mm while that of the proposed device with NiO_X oxidized at 400 and 500 ℃ were 60.8 and 44.8 mS/mm respectively. It was thought that the voltage drop across the NiO_X was increased in proportional to gate voltage, which degraded channel control capability.

Off-state drain leakage current of the MOS-HEMT was measured under the pinch-off bias condition where V_{GS} was -8 V, V_{DS} was 5 V. Off-currents of the device with NiO_X film was lower than that of the conventional one. Off-currents of the device with NiO_x oxidized at 500 ℃ were 5 orders of magnitude lower than that of the conventional HEMT. Measured off-current of the device with NiO_X oxidized at 400 and 500 ℃ were 12.6 nA

(25.2 nA/mm)and 66.5 pA (133 pA/mm), while that of the conventional HEMT with the same device geometry was 7.12 μA (14.2 μA/mm) (Fig. 3.11 (a)). Low off-state drain leakage current reduced the off-state loss during switching operation of the device and increased the power efficiency in the system level. Low off-state leakage current of the proposed device was attributed to the leakage suppression effect of NiO_X interfacial layer. The mechanism of the leakage suppression of the NiO_x interfacial layer was investigated later with various experimental results. The substantially reduced drain leakage current resulted in an excellent on/off current ratio. The on/off current ratio (I_{ON}/I_{OFF}) of the proposed device (with NiO_X film oxidized at 500 ℃) was more than 8 orders of magnitude (3.32×10^8), while that of the conventional one was about 3 orders of magnitude ($4.12\times\times10^3$) as shown in Fig. 3.11. (b). It is well known that the devices with high on/off ratio have some features favorable for a stable forward operation such as low noise figure, and large gate voltage swing. Proposed device with the NiO_X interfacial layer was superior to the conventional one in that respect.

Table 3-2 Transfer characteristics of the AlGaN/GaN HEMTs with NiO_X interfacial layer

Oxidation Temperature	V_{TH} [V]	I_{DS} [mA/mm]	$g_{m\ MAX}$ [mS/mm]	I_{OFF} [A]	On/Off Ratio [I_{ON}/I_{OFF}]
Conv.	-4.75	588.4	74.7	7.12 μA	4.13E3
400℃	-4.70	540.4	72.5	12.6 nA	2.28E6
500℃	-4.45	442.5	73.7	66.5 pA	3.32E8



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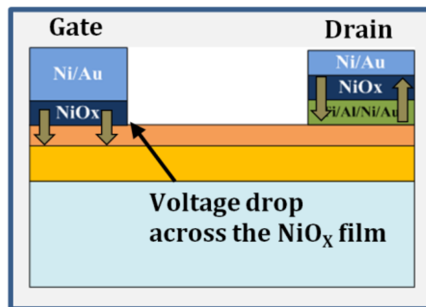


(b)

Figure 3.9 (a) Transfer characteristics, (b) Schematic diagram describing electrode structure (Gate and Drain) of the fabricated AlGaN/GaN HEMTs employing NiO_X interfacial layer. [Green arrows indicates the direction of the diffusion of the metal components]

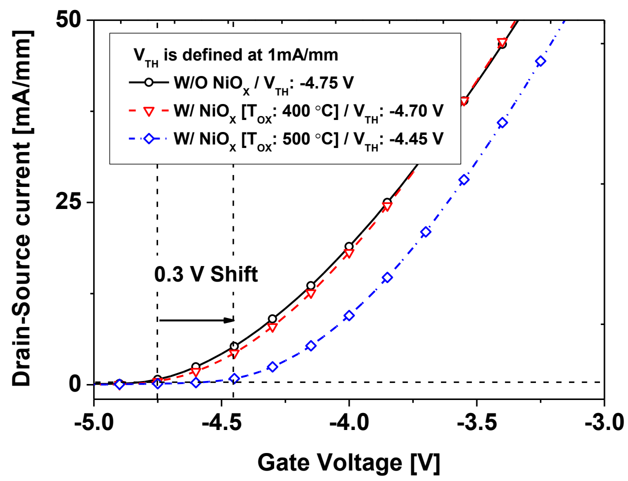
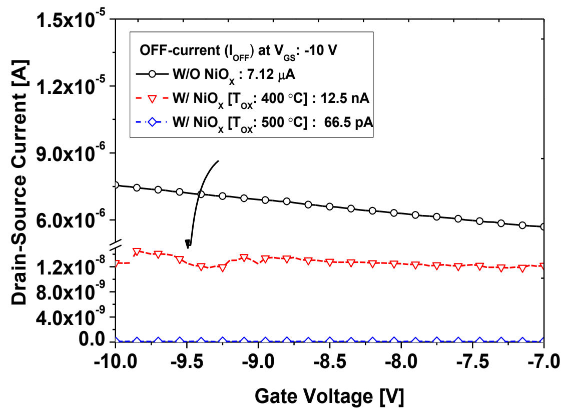


Figure 3.10 Threshold Voltage of the fabricated AlGaN/GaN HEMTs employing NiO_X interfacial layer.



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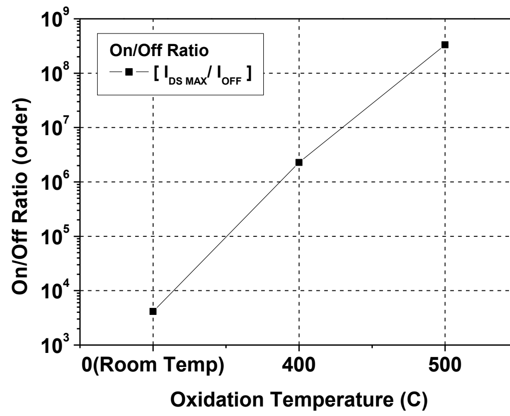


(b)

Figure 3.11 (a) Measured off-current, (b) On/Off ratio of the fabricated AlGaN/GaN HEMTs employing NiO_X interfacial layer.

3.5.1.3 Output characteristics

The critical parameter to estimate the DC output characteristics of the HEMT is the drain current. It can be controlled mainly by the drain-source voltages (V_{DS}) and gate-source voltage (V_{GS}).

Figure 3.12 shows the measured DC output current. DC output characteristic was measured up to drain-source voltage (V_{DS}) of 10 V with various gate-source voltages (V_{GS}). V_{GS} applied to device ware increased from -4 V to 2 V with the ramping rate of 2 V/step. Device geometry, especially gate-drain spacing (L_{GD}), was fixed to figure out the effect of the NiO_X more clearly. From the nearly flat I-V curves, it was suggested that all device, irrespective of NiO_X film, did not experience the current collapse caused by self-heating.

Device parameters from the output characteristics were summarized and compared with parameters from transfer characteristics in the table 3-3. The maximum drain current the AlGaN/GaN HEMT with NiO_X film (oxidized at 500 ℃, L_{GD}= 10 μm) at V_{GS} of 2 V was 415.2 mA/mm, which was similar to that of the conventional one (417.6 mA/mm). Drain current of the conventional device from output characteristics was 424.7 mA/mm and that from transfer characteristics were similar to each other (417.6 mA/mm). In contrast, maximum drain current of the device with NiO_X oxidized at 500 ℃ from output characteristics (415.2 mA/mm) was 13 % higher than that from transfer characteristics (360.8 mA/mm). To the best of my knowledge, the reason for the disparity between

measured drain currents obtained from two measurement method was vague. Despite a similar saturation drain current, the slope of the I_{DS} in the linear region was less steep than that of the conventional one. It indicated that the on-resistance of the proposed device was lower than that of the conventional one. On-resistance was extracted from the slope of the I_{DS} in the linear region at the V_{DS} of 2 V. Numerical expression for the on-resistance calculated from the equation for DC drain current in the linear region as follows:

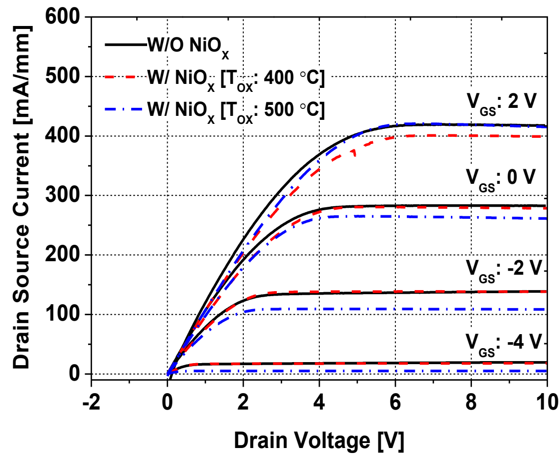
$$\frac{1}{R_{ON}} = \frac{\mu_0}{L_G} \cdot \left(\frac{C_{GS}}{L_G}(V_{GS} - V_{TH}) - \frac{V_{DS}}{2L_G} \right) - \frac{I_{DS}}{V_C}$$

$$I_{DS} = \frac{C_{GS}}{L_G}\left[(V_{GS} - V_{TH}) \cdot \mu_0 \cdot \frac{V_{DS}}{L_G} - \mu_0 \cdot \frac{{V_{DS}}^2}{2L_G} \right] \cdot \left(1 + \frac{V_{DS}}{V_C} \right)^{-1} \text{for linear region}$$

High R_{ON} of the proposed device was due to the insertion of the NiO_X interfacial layer. Increased series resistance of gate metal stack due to the NiO_X film reduced not only V_{GS}-V_{TH} term but also I_{DS} with increasing R_{ON} as indicated by expression for R_{ON}.

Table 3-3 Parameters describing DC output characteristics of the AlGaN/GaN HEMTs with NiO_X interfacial layer (comparison with transfer characteristics)

Oxidation Temperature	I_{DS} [Transfer] V_{GS}: 2 /V_{DS}: 10 V	I_{DS} [DC output] V_{GS}: 2 /V_{DS}: 10 V	R_{ON} [Ω-mm]	$R_{ON\text{-}SP}$ [mΩ-cm^2]
Conv.	424.7 mA/mm	417.6 mA/mm	8.85	4.425
400℃	401.6 mA/mm	402 mA/mm	9.85	4.925
500℃	360.8 mA/mm	415.2 mA/mm	9.66 Ω	4.33



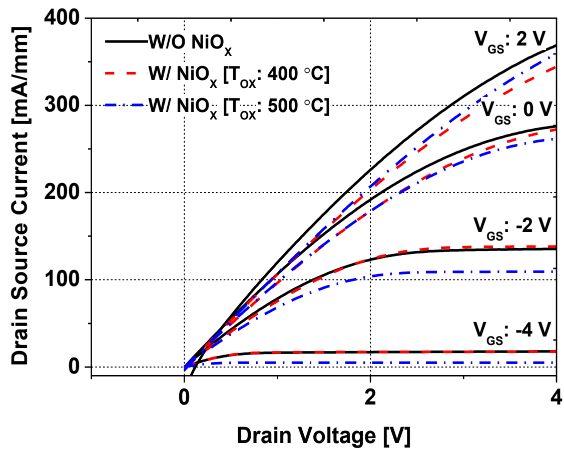


Figure 3.12 Current-voltage (I-V) characteristics of the fabricated AlGaN/GaN HEMT with NiO_X interfacial layer.

3.5.2 Reverse blocking characteristics

3.5.2.1 Leakage current

It is well-known that the leakage current and breakdown voltage of power device are the most critical factors that limit the performance of high power application. The leakage current and premature breakdown deteriorates the blocking capability of the device by causing power loss during off-state operation. When the device is under high reverse bias condition, electron injection from the gate into the semiconductor is mainly attributed to the high field intensity at the gate [117]. To suppress the leakage current, various methods such as passivation and edge termination have been proposed. In this work, the insertion of the NiO_X interfacial layer was proposed as a method to improve the reverse blocking capability of the device by suppressing leakage current and increasing breakdown voltage.

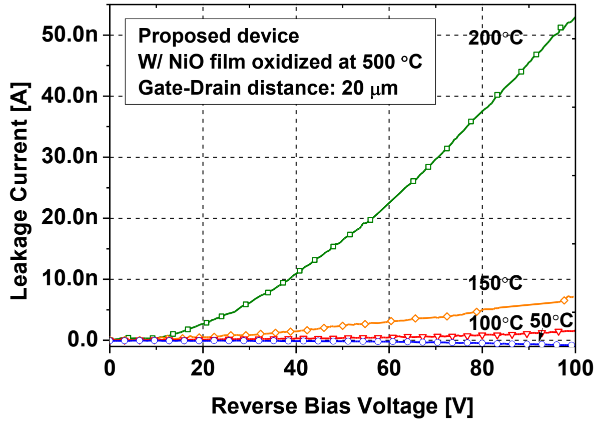
Fig. 3.13 illustrates the leakage current of the device with NiO_X interfacial layer. The leakage current was measured under the reverse bias condition where the gate and drain voltage were -7 V, 100 V respectively under various operation temperatures. Leakage current of conventional devices was increased as the drain bias was increased while that of the proposed device remained at a low level regardless of drain bias. The measured leakage current of conventional device at room temperature was 80 μA/mm (4 μA) while that of proposed device (oxidized at 500 ℃) was 1.66 nA/mm (83.3 pA). The leakage current measured at 200 ℃ was 300

μA/mm (15 μA) and 105.8 nA/mm (52.9 nA), respectively. The leakage current of the proposed device was reduced by four orders of magnitude at room temperature. However, at 200 ℃, reduced by three orders of magnitude. In the high temperature reverse bias (HTRB) test, the noticeable difference in temperature-dependent leakage characteristics between conventional and proposed device was observed. Parameters describing HTRB characteristic of the proposed device was summarized at the table 3-4.

The contribution of the gate leakage current to the total leakage current (I_G/I_{DSS}) is one of the criteria to evaluate the physical, electrical robustness of the gate contact and determine which leakage component is dominant factor. As shown in Fig. 3. 14 (b), the ratio of the conventional device was kept similar (0.83) regardless of the operation temperature. This indicated that Ni-based gate contact was vulnerable to the high temperature and electron injection was not blocked effectively by the Ni-based Schottky junction. On the other hand, the ratio of the proposed device was decreased as the operation temperature was increased. The portion of the gate leakage current of the proposed device was decreased from the 0.99 to 0.11. It suggested that the blocking characteristic of the NiO_X film was less sensitive to the temperature variation than that of the Ni film. And electron injection was effectively blocked regardless of the operation temperature. Consequently, gate leakage current was suppressed effectively while other components were increased in proportion to the operation temperature.

Table 3-4 Measured gate leakage current and its portion of the AlGaN/GaN HEMT with NiO_X film oxidized at 500℃

	Gate-drain spacing [μm]			
	5	10	15	20
I_{DSS}	1.025 nA	846 pA	630 pA	629 pA
I_G	832 pA	676 pA	466 pA	426 pA
Ratio (I_G/I_{DSS})	81.17 %	79.9 %	73.9 %	67.73 %



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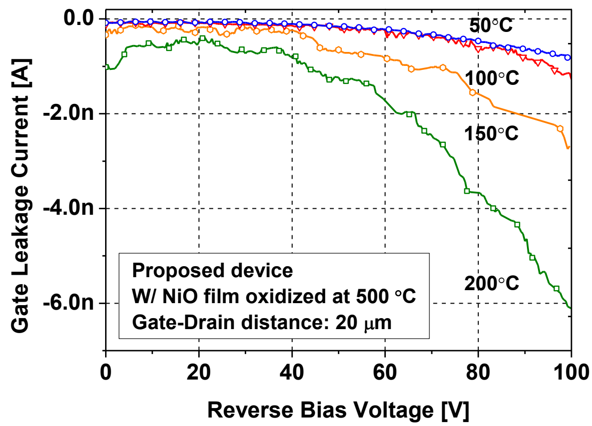
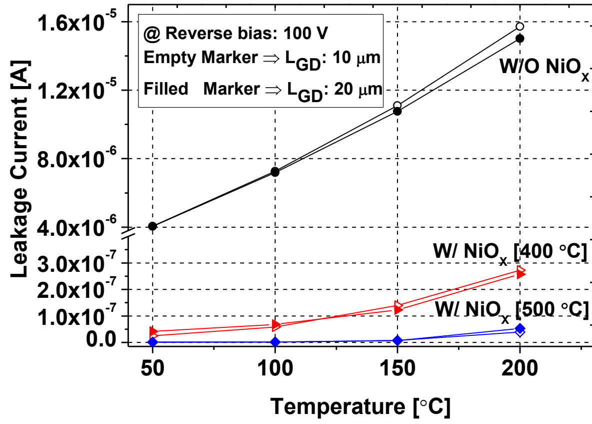


(b)

Figure 3.13 Leakage current in the active region of the AlGaN/GaN HEMT with NiO_X interfacial layer oxidized at 500℃.



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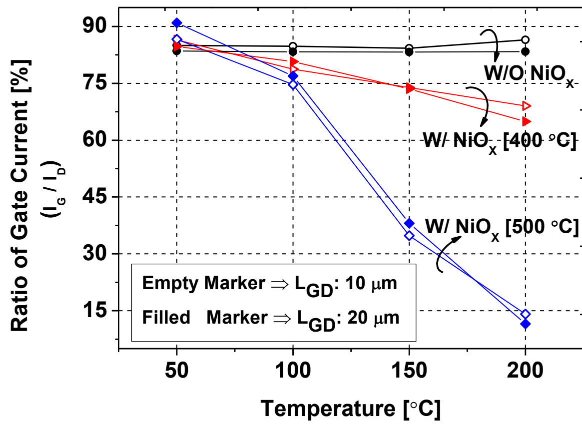


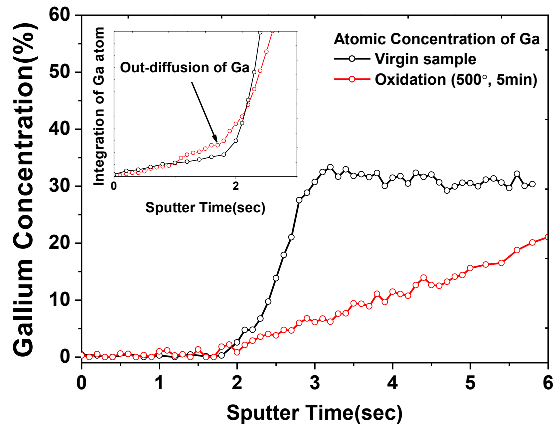
(b)

Figure 3.14 (a) Drain-source leakage current (I_{DSS}), (b) Portion of the gate leakage current of the proposed device at various operating temperatures.

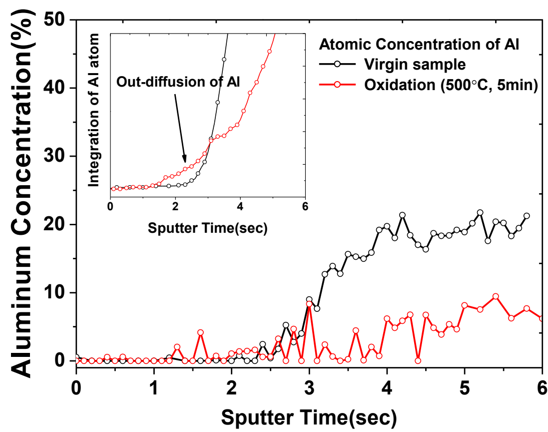
3.5.2.2 Interface characteristics

Auger electron spectroscopy (AES) and time of flight secondary ion mass spectrometry (TOF SIMS) analysis was carried out on the test sample to investigate the stoichiometric change at the surface of the heterostructure during the oxidation. The sample was an AlGaN/GaN heterostructure on which a 10 nm-thick Ni film was deposited. Fig. 3.15 shows the AES data for specific group-Ⅲ atoms of the sample before and after the 500℃ oxidation. At the as-deposited condition, the concentrations of Ga and Al indicated the boundary of the constituents of the heterostructure clearly. When the sample was oxidized at 500 ℃, the concentrations of the Al and Ga atoms were drastically reduced compared with those of the as-deposited sample. The concentration of the group-Ⅲ atoms was increased at the boundary of the layer roughly defined by the AES data of the as-deposited sample. It was confirmed by the insets in Fig. 3.15 which were the curves showing the amount of group-Ⅲ atoms by integrating the concentration. This suggested that group-Ⅲ atoms were out diffused during oxidation. Another AES analysis for Ni and O atoms (not be shown) indicated that, before the oxidation, the deposited nickel and oxygen atoms were relatively intact without any interaction with each other. After the oxidation, the depth profile of the Ni atoms coincided with that of O atoms. This was evidence of the formation of nickel oxide. During the oxidation, metallic Ni in the GaN cap and AlGaN layer was absorbed and changed into NiO_X, and the formed NiO_X was thought to penetrate to the depth of about 20 nm based on the sputtering time. Considering the

thickness of the GaN capping layer, nickel oxide was diffused to a depth of 17 nm of the AlGaN barrier layer. The oxygen and nickel that diffused into the surface of the diode formed various group-Ⅲ oxides and Ni-Ⅲ(-O) compounds as well as NiO_X. From the SIMS profile of GaO and AlO (in Fig. 3. 16) outdiffusion of the group-Ⅲ atoms was verified. After oxidation, more Ni-Ⅲ(-O) compounds were found in the surface of the diode. The loss of the group-Ⅲ atoms through outdiffusion and the formation of the group-Ⅲ oxide or Ni-Ⅲ(-O) compound left group-Ⅲ related vacancies in the GaN cap and AlGaN layer. Since group-Ⅲ related vacancies acted as a triply charged acceptor with a shallow level, the net electron concentration was decreased [118-119]. The Fermi levels of the GaN cap and AlGaN layer were shifted toward the valence band edge. As shown in Fig. 3.17, the shift of the Fermi level and the compensation of the electron by group-Ⅲ related vacancies made the energy band of the GaN cap and AlGaN layer shift upward. This resulted in an electrically thick Schottky barrier height (SBH) with increased barrier height.

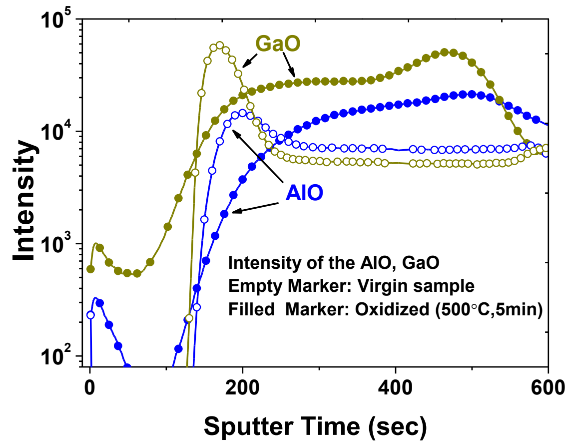


(a)



(b)

Figure 3.15 Auger Electron Spectroscopic (AES) analysis of (a) Ga, (b) Al atoms of the surface of the AlGaN/GaN HEMT with NiO_X interfacial layer.



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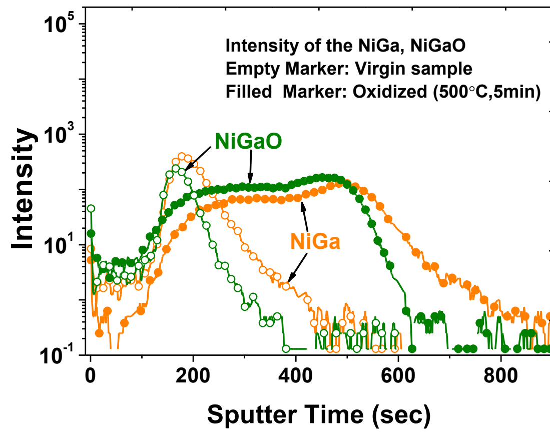


(b)

Figure 3.16 Secondary ion mass spectroscopy (SIMS) analysis of the surface of the AlGaN/GaN HEMT with NiO_X interfacial layer.

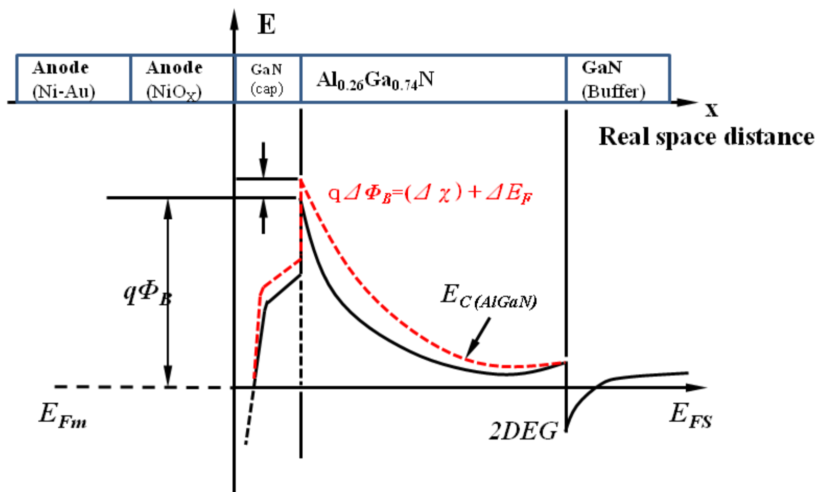


Figure 3.17 Schematic diagram describing energy band structure of gate contact (Ni-Au/NiO_X/GaN/AlGaN) of the AlGaN/GaN HEMT with NiO_X interfacial layer.

3.5.2.3 I-V characteristics of the gate diode

Figure 3.18 shows the temperature-dependent forward and reverse current-voltage characteristics of the gate diode of the HEMT employing a NiO_X-Ni/Au gate. The applied voltage for the forward operation of the diode was 5 V. To evaluate the effect of the NiO_X-based Schottky contact on the forward operation of the diode, the specific on-resistance ($AR_{DS\,(ON)}$) was extracted from the slope of the current curve The $AR_{DS\,(ON)}$ value of the conventional diode was 5.75 Ω cm^2, while that of the proposed diode was 6.093 Ω cm^2. The increase in the specific on-resistance was attributed to the series resistance of the NiO_X-Ni/Au gate stack which was induced by the NiO_X interfacial layer.

However, forward current of the gate diode was comparable to that of the conventional one. The measured forward current of the conventional diode was 87.08 μA/mm while that of the proposed one was 82.64 μA/mm. Degradation caused by the NiO_X film was only 5% of the total diode current (4.44 μA/mm).

The blocking capability of the diode was improved by insertion of the NiO_X interfacial layer. The leakage current of the proposed device was reduced by three orders of magnitude. At room temperature, the leakage current of the conventional diode measured at applied bias of -5 V was 0.263 μA (5.26 μA/mm), while that of the proposed diode was 236 pA (4.72 nA/mm). The leakage currents of both devices increased in proportion to the operating temperature. The leakage current of the

conventional diode measured at 200℃ was 0.824 uA (1.748 uA/mm), while that of the diode with NiO_X-Ni/Au was 368 pA (7.36 nA/mm). The normalized leakage currents ($I_{leak\ (200C)}/I_{leak\ (RT)}$) of the conventional and proposed diodes, measured at 200℃, with respect to the leakage current measured at room temperature, were 3.132 and 1.562 respectively.

Barrier height of the (NiO_X-Ni/Au)-GaN/$Al_{0.3}Ga_{0.7}N$/GaN was extracted from the I-V characteristics. The diode current can be given by the thermionic emission (TE) model and is expressed as

$$I = I_S \exp(\frac{qV}{nkT})\left[1 - \exp(\frac{-qV}{kT})\right]$$

Where n is the ideality factor, and I_S means the saturation current obtained at the applied voltage of 0 V during the voltage sweeping from -5 to 3 V and was given by

$$I_S = AA^*T^2 \exp(\frac{-q\Phi_B}{kT})$$

Where A is the rectifier contact area, $A^*(=4\pi qk^2m^*/h^3)$ is the effective Richardson constant (34.06 $A/cm^2 \cdot k^2$ for $Al_{0.3}Ga_{0.7}N$) [120], T is the temperature in Kelvin, k is the Boltzmann constant, q is the electronic charge, and Φ_B is the barrier height. Extracted barrier height was summarized at the table 3-6. The barrier height of the gate diode employing NiO_X-Ni/Au was 0.81 eV at room temperature (278 K) and 0.75 eV at 200℃ (473 K) respectively while that of the conventional one was 0.75 eV at room temperature (278 K) and 0.66 eV at 200℃ (473 K).

From this experimental result, it was proved that Schottky contact formed between the surface of heterostructure and NiO_X-Ni/Au was not only highly rectifying but also thermally stable than that of the conventional one.

Table 3-5 Barrier height extracted from the gate diode I-V characteristics of AlGaN/GaN HEMT with NiO_X interfacial layer at various operating temperatures

Operating Temperature	Conventional Ni-GaN contact	Proposed NiO_X-GaN contact
Room temp.	0.75 eV	0.81 eV
200℃	0.66 eV	0.75 eV
Variation	- 12 %	-7.4 %

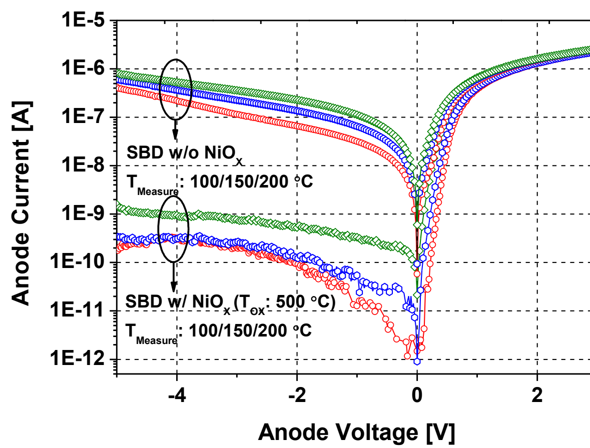


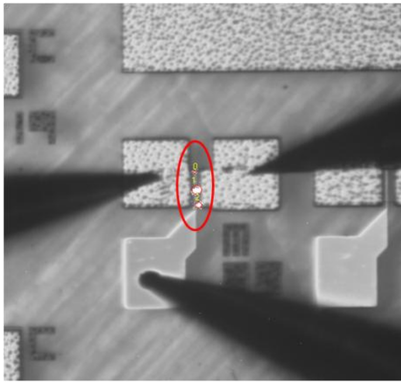
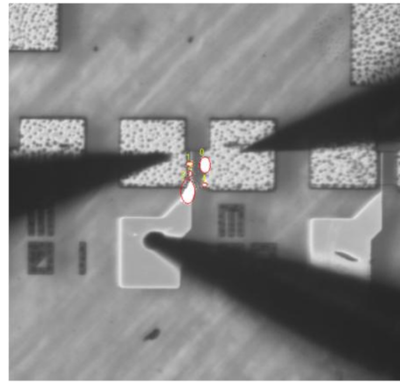
Figure 3.18 Gate diode I-V characteristics of the AlGaN/GaN HEMT with NiO_X interfacial layer at the various operating temperatures.

3.5.2.4 Electroluminescence analysis

Electroluminescence analysis has been used to detect the spot where light emission takes place due to the hot electrons caused by impact ionization or current crowding phenomena [121-123]. Many research groups focusing on the reliability of GaN-based device have made use of EL analysis to detect the spot in which impact ionization took place or electric field was concentrated.

Figure 3.19 illustrated a result of the EL analysis. Electroluminescence images were obtained by applying specific bias to the target device for some duration time (1 min) to analyze the light emission by signal processing. Then, processed signal image of electroluminescence was expressed by white spot and overlapped on the microscopic image of the target device. Because device experienced applied bias for some duration time, the effect of the specific bias condition on the device could be investigated without any destructive analysis. In this work, high reverse bias used in the measurement of breakdown voltage was applied to target device for 1 min to check the spot where electron collision due to the surge of electrons (by impact ionization) or thermal runaway took place. As shown in Fig. 3. 19 (a), in conventional device, white circle was detected on gate-side drain edge, gate feed and gate. These local regions were typical places where severe field concentration was expected. On contrary, in the proposed device, white circle at the gate was not observed. It meant that NiO_X interfacial layer inserted between gate and heterostructure suppressed the injection of electrons into the surface of

the heterostructure effectively. It was another evidence to indicate that improved blocking characteristics of the proposed device was ascribed to the high rectifying contact formed by NiO_X interfacial layer.

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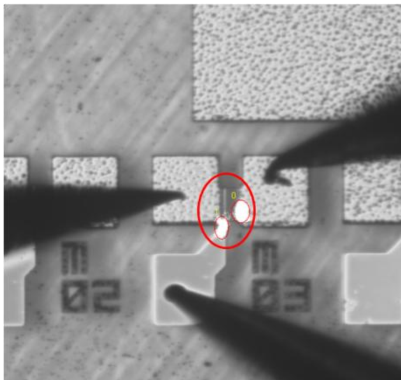
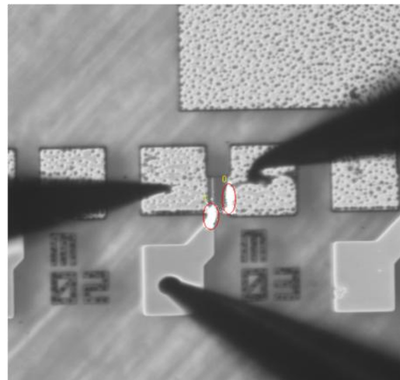



(b)

Figure 3.19 Microscopic image of the Electroluminescence (EL) analysis of the (a) conventional HEMT (b) HEMT with NiO_X interfacial layer. (White circles on the microscopic image indicated the spot where impact ionization occurred).

3.5.2.5 Breakdown characteristics

An enhancement of breakdown voltage in AlGaN/GaN HEMT using NiO_X interfacial layer was investigated. It has already been explained that the high potential barrier induced at the interface between the surface of the heterostructure and NiO_X interfacial layer prevented electrons from injecting into semiconductor which led to the reduction of the gate leakage current. Reduced gate leakage suppressed or postponed the degradation or destructive process caused by high leakage current in blocking mode such as surface hopping, impact ionization and punch through etc., which shifts the reverse bias voltage (drain voltage) where breakdown occurred to the higher value.

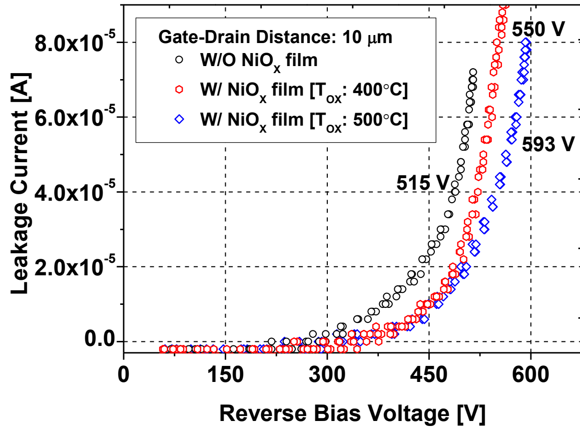
The off-state breakdown of the MOS-HEMT with two gate-drain spacing (L_{GD}) of 10/20 μm was shown in Fig. 3. 20 The breakdown voltage of the device was measured at the sub-threshold gate bias ($V_{GS} < V_{TH}$). During the measurement, the devices were immersed in Fluorinert liquid (3M™ FC-3283) to avoid air breakdown. The drain bias increased with keeping the device in off-state and the current was logged until breakdown was identified. The breakdown voltage (V_{BR}) was defined as the drain voltage at which the leakage current exceeded 1mA/mm. All parameters describing breakdown characteristics of the MOS-HEMT was summarized and compared with conventional device.

Fabricated device with 10μm gate-drain spacing exhibited a soft breakdown characteristic irrespective of NiO_X interfacial layer. Measured V_{BR} of the proposed device with L_{GD} of 10 m was 593 V which was similar

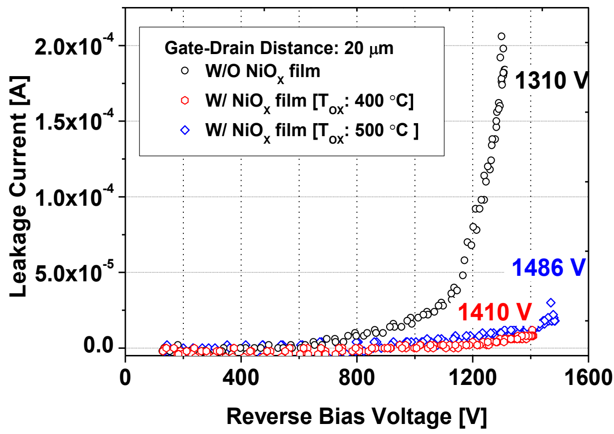
to that of the conventional one (515 V). The leakage currents of both devices at the V_{BR} were over 70 μA/mm. Noticeable improvement in blocking capability was observed in the proposed device with 20 μm gate-drain spacing. Breakdown voltage of the proposed device with L_{GD} of 20 μm was about 1.5 kV which was 29 % higher than that of the conventional one (1310 V). An increment in the value of V_{BR} was not high. AlGaN/GaN HEMT with NiO_X interfacial layer suppressed leakage current effectively during measurement of the V_{BR}. Leakage current of proposed device at V_{BR} was 18 μA/mm which was as low as 9 % of the leakage current of the conventional device (206 μA/mm). Hard breakdown characteristic of the proposed device with L_{GD} of 20 μm was based on the suppression of the drain leakage current, especially gate leakage current. The suppression of the gate leakage current was ascribed to highly rectifying contact formed by NiO_X interfacial layer.

Table 3-6 Parameters describing breakdown characteristics of the AlGaN/GaN HEMT with NiO_X interfacial layer

Geometry (L_G/L_{GD})	V_{BR} [V]	Variation in V_{BR}	Leakage @ V_{BR}	Variation in Leakage
Conv. (3/10 μm)	515	-	72 μA/mm	-
Prop.(3/10 μm)	593	15 %	80 μA/mm	+11 %
Conv. (3/20 μm)	1310	-	206 μA/mm	-
Prop.(3/20 μm)	1486	28.7 %	18 μA/mm	-91 %



(a)



(b)

Figure 3.20 Breakdown characteristics of the fabricated AlGaN/GaN HEMT with NiO_X interfacial layer (gate-drain spacing (L_{GD}) were 10 and 20 μm).

3.6 Summary

We have proposed and fabricated the AlGaN/GaN HEMTs with NiO_X interfacial layer. It was demonstrated that the NiO_X interfacial layer effectively suppressed the premature breakdown and improve the reliability of the gate contact in the high temperature reverse bias operation. As a result, the AlGaN/GaN HEMTs with NiO_X interfacial layer exhibited stable blocking characteristics and increased breakdown voltage when compared to the devices without any interfacial layer. Consequently, AlGaN/GaN HEMTs with NiO_X interfacial layer is highly desirable in order to achieve the stable and robust reverse blocking characteristics.

Chapter 4

4. AlGaN/GaN MOS-HEMT with ALD Al_2O_3 gate dielectric

4.1 AlGaN/GaN HEMT on Si Substrate

The AlGaN/GaN HEMTs heterostructure used in this experiment was prepared on Si substrate. As previously referred, devices grown on Si substrate can be cost-competitive and alternative to those grown on sapphire and SiC substrate. However, epitaxial process of GaN on Si is known to be very difficult due to high lattice mismatch. Properties of the AlGaN/GaN HEMTs on Si were described at first in this section. Then the brief explanation on the MOS structure and importance of the gate dielectric was followed by the next section. The investigations on the device performance were a subject of the next part of this chapter. The forward operation of the device was characterized by means of the DC and pulse method. Device operation in the blocking mode such as leakage current and breakdown of the device was explained with plausible mechanisms to explain these phenomena.

AlGaN/GaN heterostructure were grown by MOCVD method. AlGaN/GaN heterostructure used in this work was grown on (111)-oriented p–type low resistivity silicon substrate with the thickness of 1000 μm in error range of ±25 μm. The resistivity of the substrate was at the lower level than 0.03 Ω·cm ($\rho < 0.03$ Ω·cm). Transition layer, often called as SRL (Strain Release layer), was grown in the first to relive a mechanical stress stemming from the large lattice mismatch. Then a series of layers on which GaN buffer was grown followed the transition layer. Hall measurement was carried out to investigate the quality of the AlGaN/GaN heterostructure on Si substrate. Hall measurement is a method commonly used for characterization of semiconductor. It provides information about the key parameters to majority type concentration and mobility. It is generally accepted that channel conductivity of HEMT (MESFET) was investigated using this method. The Hall-Effect measurement is based on the measurement of an induced voltage of the sample in magnetic field fluxes oriented perpendicular to sample surface [124].

To characterize heterostructure by hall measurements, Hall structure was integrated in the mask for HEMT fabrication. Three test patterns were co-fabricated per one die (diced piece). The Hall structures consisted of an isolated mesa island. The area of test patterns was 1.5 mm×1.5 mm^2. Each test pattern had four Ti/Al/Ni/Au (20/80/20/100 nm) based contacts (area 496 × 496 μm^2) placed at the edge of the sample. The contour of each pattern was similar to the windmill. Annealing at 880℃ for 30 sec in the N_2 ambient (the same annealing condition for Ohmic contact formation) achieved an electrical contact to 2DEG. This design of the test pattern has the advantage that mobility as well as carrier concentration

are measured on the same pattern near the actual device. Measurement was performed at the room temperature (300 K).

Measured value of carrier concentration (n_s) of the 2DEG and mobility of the heterostructure on Si substrate and on sapphire were compared in the table 4-1. Balanced value of the carrier concentration of sample grown on Si was 1.417×10^{13} cm^{-2}. It was 47 % higher than that of the sample gown on SiC. The balanced n_s of the sample grown on SiC substrate was 9.63×10^{12} cm^{-2}. The mobility for both samples grown on Si and SiC substrate were 1.32×10^{2} $cm^2/V\cdot s$ and 1.47×10^{2} $cm^2/V\cdot s$ respectively. Mobility of the sample on Si was 10 % lower than that of the sample on SiC contrary to the sheet carrier concentration (n_s). Although electron mobility is not in a correct inverse proportion to carrier concentration, electron mobility was decreased to some degree due to the channel carriers with high concentration over 13 orders of magnitude ($>10^{13}$). It is known that a high $\mu_n\cdot n_s$ product of the device results in low on-resistances(R_{ON}) of the device. The balanced $\mu_n\cdot n_s$ product of the sample on Si substrate was higher than that of the sample on SiC substrate. It is suggested that balanced sheet resistance of the sample on Si was lower than that of the sample on SiC.

Table 4-1 Measured Hall parameters of the heterostructure grown on Si and SiC substrate

Hall parameters (at 300 K)	Silicon substrate			
	#1	#2	#3	Aver.
n_s [cm^{-2}]	1.38×10^{13}	1.54×10^{13}	1.33×10^{13}	1.417×10^{13}
μ_n [$cm^2/V\cdot s$]	1.17×10^{3}	1.09×10^{3}	1.23×10^{3}	1.163×10^{3}
R_{sq} [Ω/☐]	387	372	382	380
	SiC substrate			
	#1	#2	#3	Aver.
n_s [cm^{-2}]	7.15×10^{12}	7.24×10^{12}	1.45×10^{13}	9.63×10^{12}
μ_n [$cm^2/V\cdot s$]	1.8×10^{3}	1.79×10^{3}	8.23×10^{2}	1.47×10^{3}
R_{sq} [Ω/☐]	485	482	524	497

4.2 Atomic-Layer-Deposited Al_2O_3 dielectric

The Metal-Oxide-Semiconductor field effect transistor (MOSFET) is a three-terminal device which uses a metal gate to control a conducting channel that carrier flow through from a source to drain. Many advantage of the MOSFET is based on utilization of the insulating layer (oxide) between gate and semiconductor layer. The insulation of the gate reduces the gate leakage. Passivation mediates the problems related to the surface states such as dispersion. The performance of the MOSFET (or MOSHEMT) is greatly dependent on the quality of the gate dielectric.

For a material to be a gate dielectric in the MOSFET (MOSHEMT), few factors should be considered: higher dielectric constant than semiconductor, wide band gap, thermal stability, lattice constant and thermal expansion coefficient similar to that of the underlying substrate etc. From a general perspective view, Atomic layer deposited (ALD) Al_2O_3 is the material of choice for dielectric film of MOSFET (or MISFET) due to many advantages originating from the combination of the way of film deposition and inherent material properties. ALD Al_2O_3 almost satisfies the aforementioned requirements. In this section, characteristic of the ALD Al_2O_3 is explained by according to each prerequisites of the gate dielectric material.

Atomic-layer-deposition (ALD) is the one of the most widely used methods to deposit the gate dielectric on the device due to the many features favorable to device. Compare with other methods such as ICP

(inductively coupled plasma), CVD (chemical vapor deposition), It is reported that ALD method causes the low plasma damages. It is the most distinguishable feature of ALD method. Additionally, ALD method is well-known for its nano-scalability, conformability and uniformity [125-126].

High power switches are frequently exposed to the high temperature due to its high current operation. Under high operating temperature, power device should remain reliability. It means that insulator deposited on the surface of the semiconductor is required to tolerate the high operating temperature without any problems. High operating temperature with high power device makes thermal stability a necessity for the dielectric. In general, the crystallinity of the ALD Al_2O_3 used as gate dielectric is amorphous. Amorphous Al_2O_3 film is suitable for gate dielectric. the crystalline phase of the ALD Al_2O_3 is remained up to 800 ℃. It is quite high temperature which cannot be reached by normal device operation. It is reflected that ALD Al_2O_3 has a sufficient thermal stability to be used as gate dielectric.

Dielectric constant (ε_r) or permittivity of the insulator should be higher than that of the semiconductor. The main drive of the high-k research is the demands for the future Si-based transistors. Since the scaling–down of the SiO_2 gate dielectric has reached its technological limits, novel material which can substitute the SiO_2 is in a state of urgent necessity. That is the reason to spur the research on the high–k material as an insulator with a dielectric constant. In the field of GaN-based devices, dielectric constant of the GaN and AlGaN is about 9~9.5 and 8.8 respectively. It is desirable that high-k dielectric materials be used in GaN-

based device. A higher dielectric constant than the semiconductor is in favor of the device operation in terms of two aspects. In general, device with MOS (or MIS) structure undergoes the negative shift of the threshold voltage due to the insertion of insulating film between gate and semiconductor as following equation.

$$V_{th(MOS)} = V_{Schottky} \cdot (1 + C_S / C_i)$$

It can lead to the degradation of gate controllability. To lessen the degradation of gate controllability, dielectric material with higher dielectric constant than semiconductor should be used. High power device are exposed to the high gate bias (V_{GS}) condition in the even forward operation for high current handling. The higher dielectric constant than semiconductor prevents the formation of high electric field across the dielectric film according to the following equation.

$$D = \varepsilon_i E_i = \varepsilon_S E_{S,} \quad E_i = \varepsilon_s \cdot E_S / \varepsilon_i$$

High electric field across the dielectric film can gives rise to dielectric breakdown. This can lead to premature breakdown with formation of the leakage path. It can degrade the forward characteristics by reducing drain-source current. Dielectric constant of

The band gap of a dielectric material is an indicator for the insulating property of a gate dielectric. More reasonable approach to estimate the insulating property is to look at the relative alignment of the each energy band (conduction and valence) of the two adjacent materials. ΔE_C (band-offset of the conduction band) is defined as the energy difference

between the lower conduction band edge of the two material. There are several ways the energy bands can align each other. Among them, two configurations are of interest: the straddling and staggered lineups. Staggered lineup indicates the large offsets in only either the conductor or the valence band, which is beneficial to unipolar device [127]. Straddle lineup is the configuration where small energy band gap is laid on wide energy bandgap with band offset in both bands (Fig. 4.1) [128]. Alignment between Al_2O_3 and AlGaN barrier can be depicted as straddling lineup. The lower ΔE_C is the higher leakage current flow through various mechanism such as Schottky emission or Frenkel-Poole emission etc. A larger bandgap gives rise to the large band offset between dielectric film and semiconductor. Especially large band offset in conduction band (ΔE_C) with respect to semiconductor play a important role to prohibit the leaking of the electrons from the channel and moving into the barrier layer. In general, ΔE_C, ΔE_V should be higher than 1 eV to achieve the sufficient insulation property [129]. Figure 4.2 (a) and (b) illustrate the results for various dielectrics on GaN and AlGaN with Al mole fraction of 30%. According to Fig. 4.2, ΔE_C of SiO_2 between GaN is about 2.56 eV, which suggests that SiO_2 is suitable for the gate insulator of GaN based device. In this respect, as an insulator, SiO_2 outperforms Si_3N_4 and HfO_2. Hafnium dioxide, one of the gate dielectric widely used in Si technology, has a band offset of 1.14 eV with GaN and 0.58 eV with AlGaN. Band offset of Al_2O_3 with GaN is 2.18 eV and 1.55 eV with AlGaN, which is high enough to suppress the leakage through the dielectric layer.

In case of the MOSHEMT for high power device, physical and electrical

ruggedness of the dielectric can be the critical factor to determine the reliability of the device. In general, the ruggedness of the dielectric is evaluated by the breakdown field (E_C) of the dielectric. Insulator with low critical electric field is vulnerable to dielectric breakdown at relatively low reverse bias voltage. Once it occurs, large leakage current flow through the dielectric film of the device independently of the blocking capability of the transistor. So the device with MOS (or MIS) structure should be based on the dielectric with high critical field. The higher breakdown field of the dielectric film is, the more charge carriers flow freely regardless of the gate bias voltage in the forward operation and more reverse bias voltage is sustained without failure of the device. The critical field of Al_2O_3 is in the range from 10~30 MV/cm, which is sufficient to sustain high reverse bias, dumped into device.

Table 4-2 Dielectric constant (ε_r) and energy gap (E_g) of various dielectric materials

Gate dielectrics	Dielectric constant (ε_r)	Energy gap (E_g)
SiO_2	3.9	8.0
Si_3N_4	7.0~7.6	5.1
ZrO_2	15~30	7.8
HfO_2	45~150	5.65
Al_2O_3	8.8~9	9
Ta_2O_3	15~25	4.2

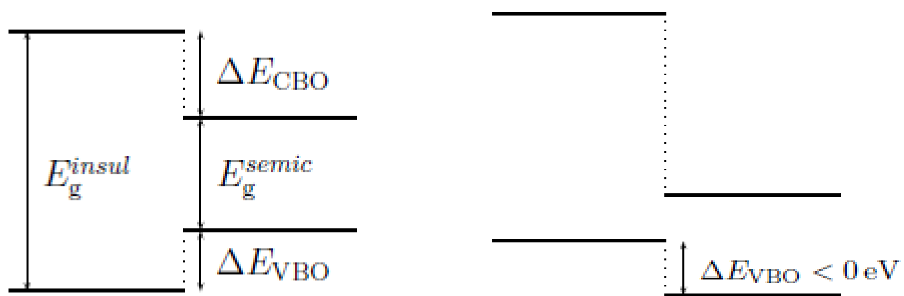
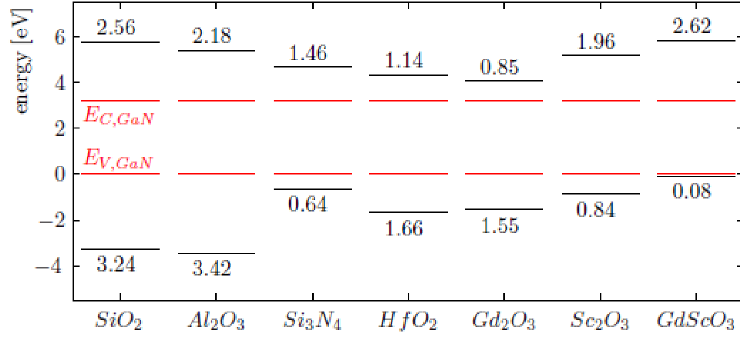


Figure 4.1 Types of band lineups. The energy band either aligns in a straddling (a) or in a staggered (b) lineup [128].



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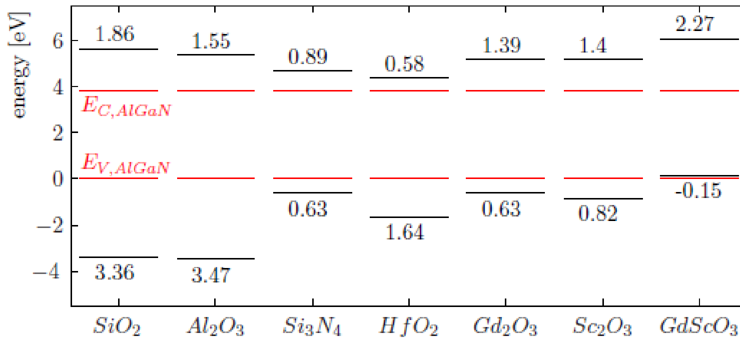


(b)

Figure 4.2 Band offsets between various oxide and (a) GaN and (b) $Al_{0.3}Ga_{0.7}N$. [Black line stands for the bandgap of the oxide, red one stands for bandgap of the AlGaN or GaN]

4.3 Device fabrication

AlGaN/GaN heterostructure used in this experiment are slightly different from the one used in the previous experiment in terms of substrate. AlGaN/GaN heterostructure with Al composition of 26% was grown by MOCVD on Si substrate. The epitaxial structure was grown on p-type low resistivity Si substrate. Resistivity of the substrate was about 0.03 Ω·cm. Epitaxial structure began with transition layer, which released mechanical strain originating from mismatch in lattice constant between Si substrate and GaN buffer. As a result, an insertion of transition layer reduced the dislocations due to mechanical strain. Then C-doped GaN buffer layer was followed, which makes contribution to minimize the drain-source leakage current through the GaN buffer region. The total thickness of the GaN buffer incorporating *i*-GaN was 4 μm. Electron channel of high density was formed between GaN buffer and 30 nm-thick unintentionally doped (UID) AlGaN barrier layer. The structure was completed with a 3 nm-thick GaN capping layer for the purpose of protection. Epitaxial structure for AlGaN/GaN HEMT used in the experiment was illustrated in Fig. 4. 3.

The fabrication process stated with device isolation. Each transistor was defined by inductive coupled plasma (ICP) etching process with Cl_2-based gas mixture. Depth of the etched region was about 150 nm. After isolation process, pre-treatment with diluted acid solution (HCl: H_2O_2: DI=1:1:6 in volume ratio, for 5min) was performed for the clean surface. Then Al_2O_3 dielectric film was deposited. The sequence of the deposition Al_2O_3 was

carried out prior to electrode-formation process. The effect of the pre-passivation process will be explained later. Al_2O_3 film was deposited through plasma enhanced atomic-layer-deposition (PEALD) method. Precursors used in ALD process were tetra-methyl-aluminum (TMA, $AlCH_3$) and O_2 plasma. Deposition was carried out at the temperature of 450 ℃ and pressure of 790 mT. As shown in Fig. 4. 4, actual thickness of the Al_2O_3 film confirmed by transmission electron microscope (TEM) was 103 Å. For the adhesion and cure of damages, Al_2O_3 deposited heterostructure was annealed at 300 ℃ in the N_2 ambient for 5 min.

For the window for source and drain electrode, wet etching using diluted acid solution (HF: NH_4F=1:6 in volume ratio) was carried out. Then Ti/Al/Ni/Au (20/80/20/100 nm) based Ohmic contacts were formed by e-gun evaporation then annealed at 880℃ in N_2 ambient for 30 sec. The final step of the process was to form Ni/Au based gate contact by e-gun evaporation. Standard lift-off method based on photolithography was used to define the footprint for metal electrode. Device has the with various gate lengths (L_G: 3/5 μm) and gate-drain spacing (L_{GD}: 5/10/15/20 μm) was fabricated to investigate the dependency of breakdown voltage on the device geometry. Widths of the gate electrode were 50 /100 μm.

To extract the useful parameters from the Ti/Al/Ni/Au based contact made to the AlGaN/GaN device, I-V measurement was carried out on the co-fabricated test structure for Transfer Length Method (TLM) on the same die on which actual device was fabricated. The TLM measurement was performed just after the rapid thermal annealing of ohmic contact

and prior to the gate electrode deposition. The current and voltage were measured on pads with varying spacing and the resistance. The transfer length indicates that how far current under the ohmic contact will flow laterally. So measured current was a function of the pad spacing. In general, contact resistance can be defined at the resistance which is extracted from the exact current flowing through the ohmic contacts such as source and drain. As the distance between two pads approaches zero, contact resistance (R_C) can be extracted.

Figure 4.5 shows a microscopic image of fabricated TLM pattern and the measured TLM current. Current was measured in the voltage range from – 5 V to 5 V at the room temperature. Contact resistance can be calculated from the value of Y-intercept interpolated in the resistance curve (as a function of spacing). Generally, Y-intercept of the curve is considered as the two times of the contact resistance and can be expressed as following equation

Y-intercept=$2\times R_C/W$, R_C/W (normalized) = Y-intercept/2

So the extracted contact resistance (R_C) of the AlGaN/GaN MOS-HEMT was 1.75 Ω-cm.

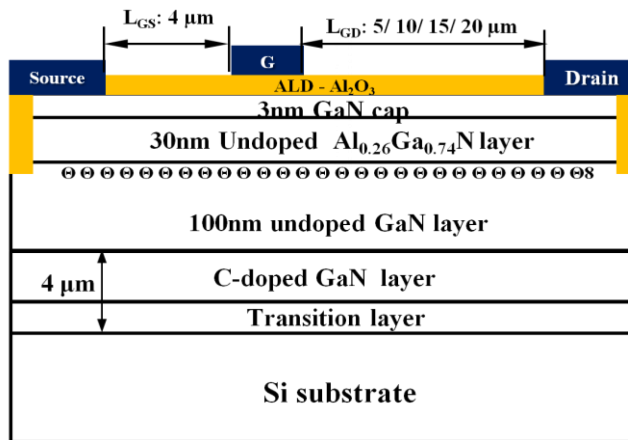
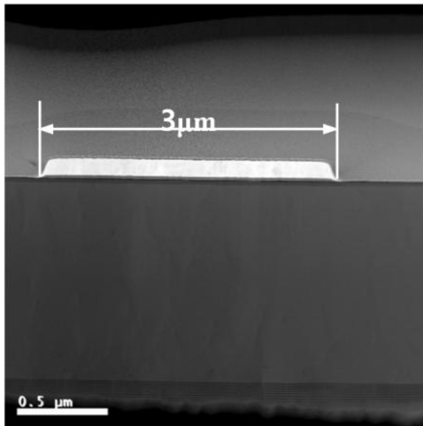
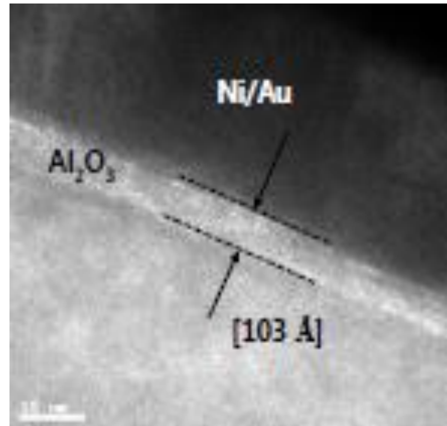


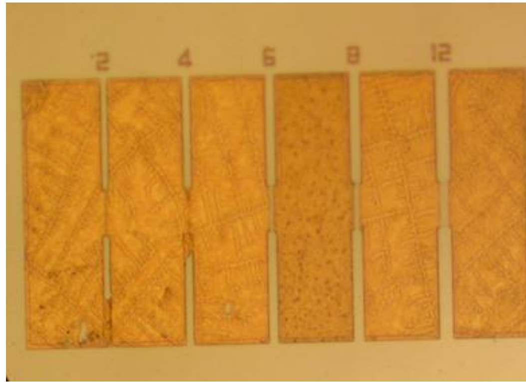
Figure 4.3 Schematic describing epitaxial structure of the fabricated AlGaN/GaN MOS-HEMT.



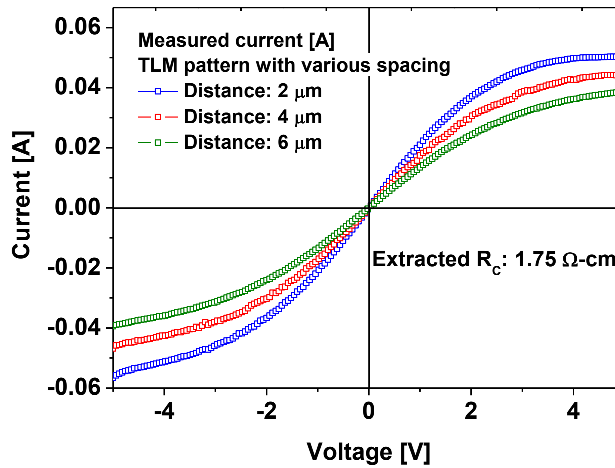


(a) (b)

Figure 4.4 TEM images of (a) gate region (b) below the gate region of the fabricated AlGaN/GaN MOS-HEMT.



(a)



(b)

Figure 4.5 (a) Microscopic image (b) Current plot of fabricated test structure for Transfer Length Method (TLM) with various spacing.

4.4 Device performance

4.4.1 Forward characteristics

4.4.1.1 Threshold voltage

Figure 4.6 illustrates the transfer characteristics of the fabricated AlGaN/GaN MOS-HEMT. Threshold voltage (V_{TH}) of the device was defined at the gate voltage (V_{GS}) where the drain current was 1mA/mm (i.e. defined by constant current method). Threshold voltage of the fabricated MOS-HEMT was negatively shifted from -6.06 V to -7.2 V. it was simply attributed to the increased gate-to-channel separation.

Because, in the MOS-HEMT, the gate is capacitively coupled to channel, it can be explained in terms of the variation of the gate-source capacitance (C_{GS}). Under the assumption of the same gate-source capacitance, C_{GS} is the parameter to change the carrier density of the channel (n_s) by changing gate-source voltage as following equation.

$$q\Delta n_s = C_{GS} \cdot \Delta V_{GS}, \qquad \text{under the same } C_{GS}$$

Based on this, the smaller C_{GS} value of the MOS-HEMT (C_{GS}(MOS-HEMT)< C_{GS}(HEMT)) should take the higher V_{GS} in order to deplete the channel carrier than that of the HEMT should. (｜V_{TH} (MOS-HEMT)｜> ｜V_{TH} (HEMT)｜). An alternative way to explain the higher threshold voltage of the MOSHEMT is through the energy band structure as shown in Fig 4. 7. When the gate-source voltage smaller than the threshold voltage is

applied to HEMT, conduction band is bent upward with lifting potential well above the Fermi-level as shown in Fig .4. 7. This is the mechanism to deplete the 2DEG by means of a gate-source voltage. In the case of MOS-HEMT, some portion of the applied V_{GS} is dropped by a dielectric layer, thus the effective gate-source bias to control the channel is smaller than that of HEMT. In other words, actual gate-source voltage in the MOS-HEMT is not sufficient to deplete the channel completely.

The voltage drop across the Al_2O_3 layer can be extracted from each portion of the gate-source voltage divided by a series of capacitance at the gate region. It can be expressed as follows.

$$V_{Effective} = V_{GS} \cdot \left(C_{Dielectric} / (C_{Barrier} + C_{Dielectric})\right)$$

Where, AlGaN (ε_r= 8.8, d_{AlGaN}= 30 nm), GaN (ε_r= 9.5, d_{GaN}= 3 nm) and Al_2O_3 layer (ε_r= 9, d_{Al2O3}= 10 nm)

For the barrier represented as a series connection of the AlGaN layer and GaN capping layer, according to this expression, the ratio of $V_{Effective}/V_{GS}$ is approximately 0.77. It was suggested that approximately 23 % of the gate-source voltage was dropped across the Al_2O_3 layer and only 77 % of the gate-source voltage was involved to control the channel. Considering that extra gate-source voltage corresponding to 23 % of the V_{TH} of the HEMT was required to deplete the channel of the MOS-HEMT completely, required V_{GS} for depletion of MOS-HEMT is about -7.45 V. The measured threshold voltage of the MOS-HEMT was -7.2 V. It reflected that the approximation of the voltage drop by the dielectric layer was nearly consistent with the actual threshold voltage of the MOS-HEMT. The

deviation of 0.25 V between calculation and measured value might be attributed the inaccuracy in the thickness of the barrier layer. (GaN, AlGaN)

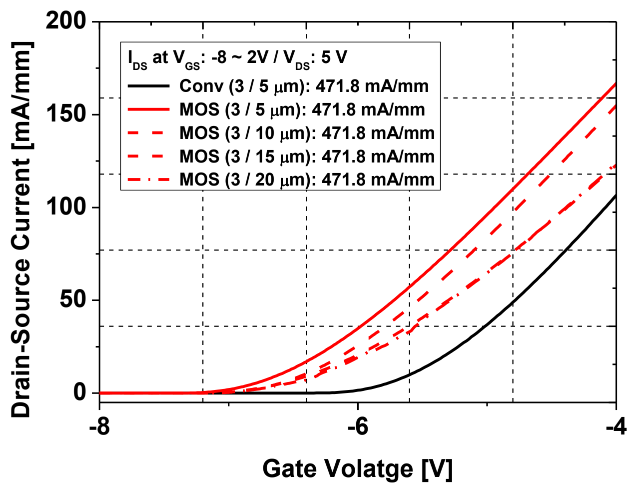


Figure 4.6 Transfer characteristics of the fabricated AlGaN/GaN MOS-HEMT.

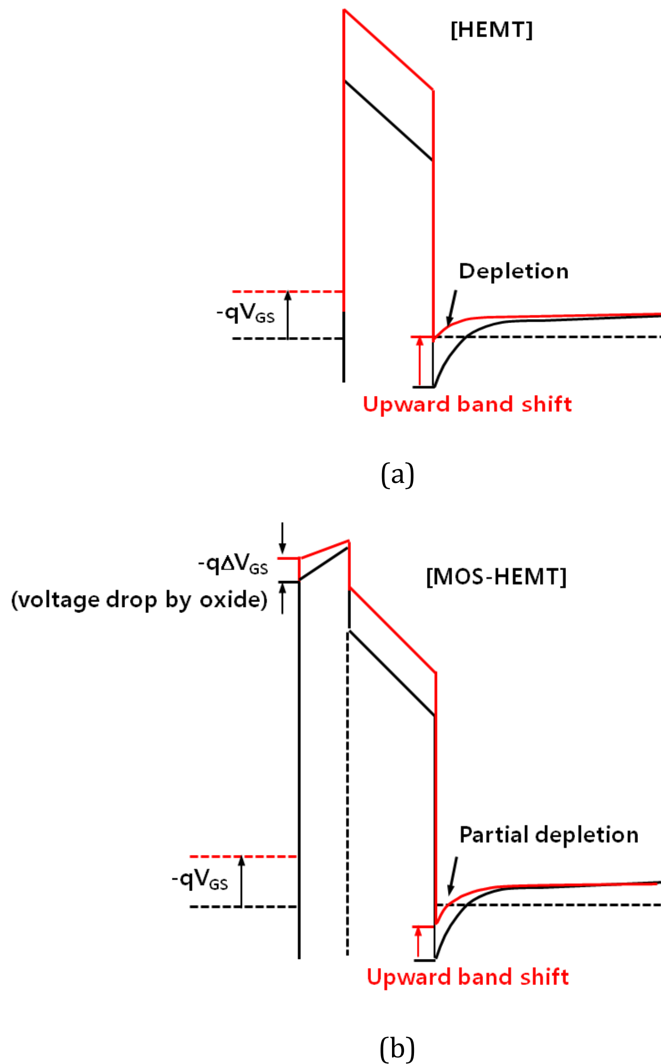


Figure 4.7 Schematic diagrams to illustrate the differences in energy band of (a) HEMT (b) MOS-HEMT under the same gate-source voltage (V_{GS}). The V_{GS} sufficient to deplete the 2DEG of the HEMT is not sufficient to make the MOS-HEMT off-state.

4.4.1.2 Subthreshold swing

The sub-threshold swing (SS) is criterion to evaluate some features of the device. One which can be estimated from sub-threshold swing is the gate controllability. In case of the MIS-HEMT (or MOS-HEMT), It is hard for gate-source voltage to control the channel effectively due to few obstacles. Voltage drop across the dielectric layer reduces the effective voltage to turn on or off the channel. It has an influence on the agility of the device operation to some degree. It is generally accepted that small value of sub-threshold swing indicates a good gate control of the device.

Beside the off-state leakage current, the characteristic of the buffer layer can be estimated by sub-threshold swing. In general, due to the Debye tail in charge distribution, an abrupt turn-off of the device is impossible. In case of the AlGaN/GaN heterostructure, electron channel is induced at the GaN buffer 2~3 nm below the hetero-interface. Channel is apt to be influenced by the condition of the buffer layer: dislocation (threading, screw type); ionized impurities; roughness of the hetero-interface etc.

Sub-threshold swing represents how fast the drain current is cut off by the applied gate voltage in the threshold realm. The drain current in the sub-threshold regime is expressed as following.

$$I_d \propto \exp\left(-n\frac{V_{GS}}{KT/q}\right), \qquad \text{where } n = 1 + \frac{C_{it} + C_{Barrirer}}{C_{Oxide}}$$

Where n is the ideality factor.

Sub-threshold swing is expressed as a reciprocal of the sub-threshold slope. Consequently it is defined as

$$SS = \frac{1}{\text{subthreshold slope}} = \frac{dV_{GS}}{d(\log I_d)} = n\left(\frac{KT}{q}\ln 10\right) = 60(T/300)\cdot n$$

From the equation of sub-threshold swing, interface trap density (D_{it}) can be extracted as following

$$D_{it} = \frac{C_{it}}{q} = \frac{C_{Oxide}}{q^2}\left(\frac{q\cdot SS}{KT\cdot \ln(10)} - 1\right) - \frac{C_{Barrier}}{q^2}$$

Sub-threshold swing was extracted from the linear region of the transfer curve. Extracted sub-threshold swing of the MOS-HEMT was 146.8 mV/dec, while that of the HEMT was 208 mV/dec. Capacitance of the Al_2O_3 layer was 7.96×10^{-7} F/cm^2 (ε_r= 9, d_{Al2O3}= 103Å). Calculated interface trap density 3.64×10^{12}cm^{-2}·eV^{-1}. Comparing with the D_{it} reported by other leading research groups (0.6×10^{12}cm^{-2}·eV^{-1}. MIT [130]), it was thought to be the moderate value. Even though the distance between gate electrode and channel was increased due to the insertion of the Al_2O_3 dielectric, MOS-HEMT exhibited small sub-threshold swing. As shown in Fig. 4. 8, drain current of the MOS-HEMT was increased more steeply than that of HEMT in the sub-threshold regime.

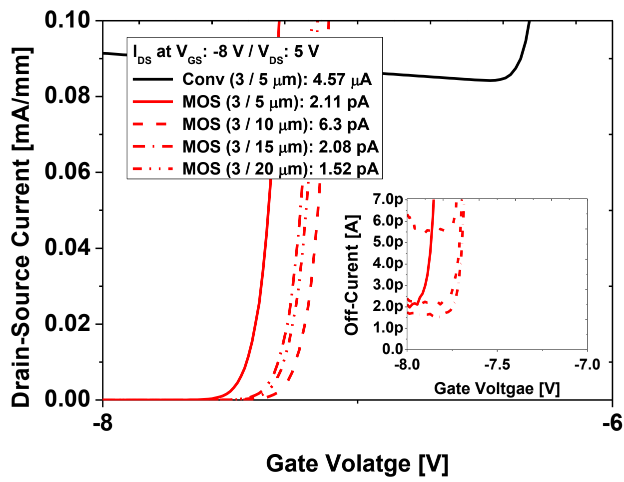


Figure 4.8 Sub-threshold characteristic of the fabricated MOS-HEMT.

4.4.1.3 C-V Measurement

Capacitance-voltage measurement of Schottky diode provides the characteristic of heterostructure with electron channel. Quantities as concentration of 2DEG can be estimated. The integration of the charge under C-V curve implies total sheet charge density of 2DEG.

In case of the MOS_HEMT (or MIS-HEMT), however, more important parameter can be inferred from the capacitance –voltage characteristics. The distortion in C-V curves is caused by two factors: interface trap; (fixed) oxide charge. As shown in Fig. 4. 9, the stretch-out from the ideal curve indicates that device has a large density of interface trap. The parallel shift of the measured C-V curve from the ideal one, represented by hysteresis, is caused by charge trapping in the gate oxide.

Figure 4.10 (a) illustrates the C-V_G characteristics of the fabricated AlGaN/GaN MOS-HEMT. Measurement of the capacitance was performed with the frequency of 1MHz at the room temperature. It was the typical C-V plot of the MOS-HEMT (or MIS-HEMT). Integration of the C-V_G plot as a function of the gate voltage indicates total charge (Q). Integration of capacitance yielded the dependence of n_s on gate voltage as shown in Fig 4.10. (b). Considering that Q is expressed as $Q=q\cdot L_G\cdot W_G\cdot n_s$, carrier density of 2DEG (n_s) can be calculated from the integral form of the total charge (Q) as following equation:

$$n_s = \frac{1}{q \cdot L_G \cdot W_G} \int C dV_G$$

Where q, L_G and W_G denotes the elementary charge, gate length and the gate width respectively. Calculated n_s of the MOS-HEMT was 2.6×10^{13} cm^{-2}. It was slightly smaller than that of the conventional HEMT (3.18×10^{13} cm^{-2}). Maeda et al. has reported that n_s was increased by around 58 % in Al_2O_3/AlGaN/GaN MOS structure using the electron cyclotron resonance (ECR) deposition [131]. However, no obvious increase in n_s was observed in our work. Considering that the deviation in sheet carrier density between two samples was 18 %, it was concluded that insertion of the Al_2O_3 dielectric film had little influence on the channel of the device.

During the sweep of gate bias, the slope of the C-V_G curve of the gate-drain diode was steeper than that of C-V_G curve of conventional HEMT, realizing good C-V behavior close to the ideal curve. Comparing with curve of the conventional HEMT, slope of the MOS-HEMT was kept similar to that of HEMT. It reflected that density of the interface trap was not large to have an effect on the slope of the C-V curve. it was thought to be due to the surface treatment using HCl-based acid solution (HCl: H_2O_2: Di=1:1:6 volume ratio).

In addition, capacitance of the device was changed into depletion mode drastically without any tail as shown in an inset of the fig. 4.10 (a) (magnified C-V_G curve of the MOS-HEMT). This was consistent with the small sub-threshold swing and quite low off-current observed in the transfer characteristics of the MOS-HEMT. Both samples (MOS-HEMT and HEMT) showed deep depletion in the negative bias region which is a

characteristics feature of wide bandgap semiconductor [132]. The zero bias capacitance was in good agreement with the capacitance of series connection of 10 nm-Al_2O_3 layer and barrier layer which was consist of 3 nm-GaN and 30 nm-AlGaN. Measured capacitance of the Al_2O_3 layer was 7.97×10^{-7} F/cm^{-2} and capacitance of the barrier was 2.38×10^{-7} F/cm^{-2}. The calculated total capacitance of a series connection of two components was 1.83×10^{-7} F/cm^{-2}. The measured capacitance of the MOS-HEMT at zero bias was 1.77×10^{-7} F/cm^{-2}. The actual capacitance measure at zero gate bias was in agreement with calculated value with the disparity of 3.8 %.

In the normalized C-V_G curve (Fig. 4. 11), hysteresis of the MOS-HEMT was investigated. The hysteresis during double sweep was due to the charge trapping effect in the gate oxide (MOS-HEMT) or AlGaN barrier layer (HEMT), which can be expressed as

$$Q_{Eff} = C_{OX} \cdot \Delta V_G \text{ or } C_{Barrier} \cdot \Delta V_G$$

Gate voltage was swept from -10 V to 0 V. Then, it was swept backward to -10 V. The positive shift of the gate voltage (ΔV_G) was observed in both curves (MOS-HEMT and conventional HEMT). Hysteresis of the HEMT was 43.9 mV, which might be attributed to electron injection into AlGaN barrier layer, because surface treatment was carried out to both samples in order to remove the Ga_2O_3 on the GaN capping layer. The value of the ΔV_G was 35.1 mV. Although it was slightly smaller than that of the HEMT, the difference between two samples could be considered as the deviation among transistors fabricated on the same heterostructure. Because both

samples were fabricated in the piece of the same AlGaN/GaN heterostructure, hysteresis observed in the C-V of the MOS_HEMT was due to the electron injection into AlGaN barrier in the same way as done in conventional HEMT. Consequently, similar hysteresis was exhibited. Measured hysteresis (ΔV_G) of the MOS-HEMT corresponded to negatively charged oxide charge with the density of 1.75×10^{11} cm^{-2}. This experimental result reflected that almost no electron injection took place in the Al_2O_3 dielectric layer.

The sharp transition from the deep depletion to accumulation and the smaller hysteresis of the C-V curve of the MOS-HEMT indicated that fabricated MOS-HEMT had a relatively low density of the interface trap and deposited Al_2O_3 dielectric film was good quality almost no electron injection took place in the Al_2O_3 layer.

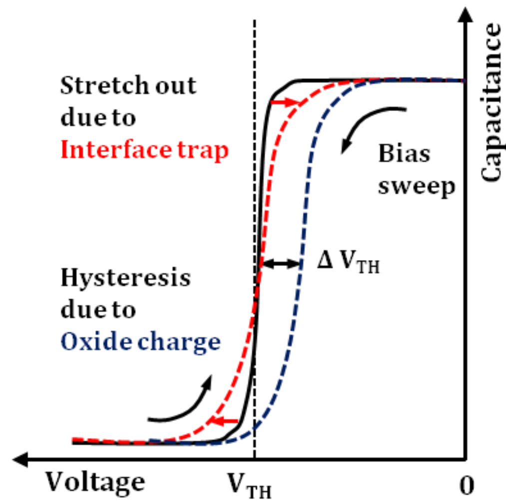
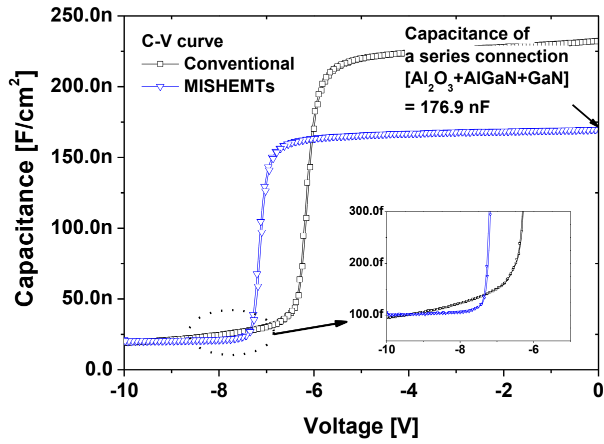
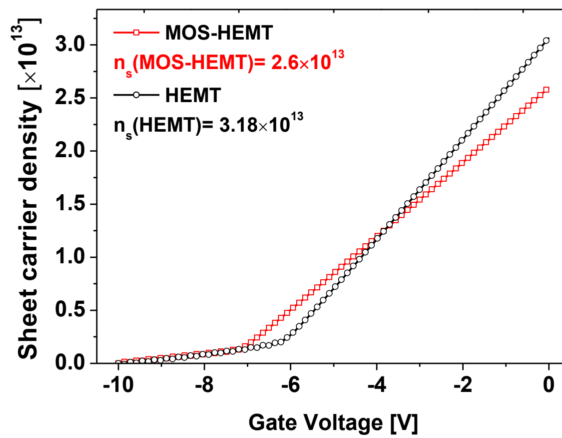


Figure 4.9 Schematic describing the abnormalities in the C-V characteristic, which is represented by stretch-out and hysteresis.



(a)



(b)

Figure 4.10 Capacitance-voltage characteristics of (a) the fabricated MOS-HEMTs and (b) calculated sheet carrier density (n_s) of the MOS-HEMT as a function of gate voltage.

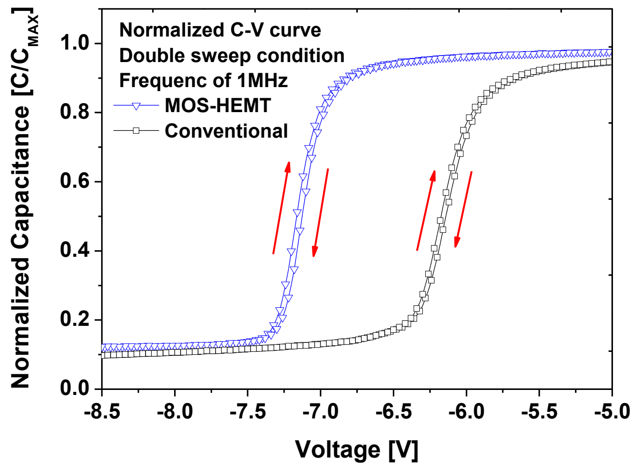


Figure 4.11 Normalized capacitance-voltage characteristics of the MOS-HEMT to compare the hysteresis in the curve.

4.4.1.3 Transfer characteristics

Off-state drain leakage current of the MOS-HEMT was measured under the pinch-off bias condition where V_{GS} was -8 V, V_{DS} was 5 V. Measured off-currents of the MOS-HEMT remained at extremely low level. All the Off-currents were distributed in the range from sub pA to few pA. Off-currents of the MOS-HEMT were 6 orders of magnitude lower than that of the conventional HEMT. Measured off-current of the MOS-HEMT with L_{GD} of 5 μm and L_G of 3 μm was 1.518 pA (30.36 pA/mm), while that of the conventional HEMT with the same device geometry was 4.57 μA (91.4 μA/mm). For the reliable comparison, another control sample, which was MOS-HEMT employing ALD SiO_2 layer as a gate dielectric, was fabricated. Fig. 4.13 showed the off-current of MOS-HEMT with ALD SiO_2 dielectric. SiO_2-based MOS-HEMT was slightly higher than that of the MOS-HEMT with ALD Al_2O_3. However, it was as low as few pA level. Measured value of the SiO_2-based MOS-HEMT with L_{GD} of 5 μm and L_G of 3 μm was 4. 2 pA (84 pA/mm).

Transfer characteristics of the MOS-HEMT exhibited a dependency on the gate-drain spacing. As shown in the table 4-3 and Fig. 4.12, maximum drain current of the MOS-HEMT, measured at the V_{GS} of 2 V and V_{DS} of 5 V, was decreased in reverse proportion to gate-drain distance (L_{GD}). Drain current of the device with L_{GD} of 5 μm was 466.8 mA/mm while that of the device with L_{GD} of 20 μm was 387.2 mA/mm. it was due to the influence of the access resistance of the drift region. The access resistance of the drift region was inherent bulk resistance leading up to active

channel. Consequently, gate-drain distance increased, access resistance was increased. This reduced the drain current of the device as shown in Fig. 4.14.

Off-current of the MOS-HEMT was kept low level regardless of the gate-drain spacing. It was due to the insulation of the gate electrode by Al_2O_3 dielectric film. With reduced sub-threshold swing, extremely low drain leakage current (off-current, ~ few pA) made the high on/off ratio of the device was over 9 orders of magnitude (up to 10 orders of magnitude) as shown in table 4-3. The device with high on/off ratio over 9 orders of magnitude can have some advantages in the device performance such as low noise figure, large gate swing and better linearity [133].

Table 4-3 Transfer characteristics of the MOS-HEMT with various gate-drain spacing (L_{GD})

L_{GD} [μm]	Drain current [mA/mm]	Off-current (un-normalized)	On/Off Ratio [I_{ON}/I_{OFF}]
Conv. (5)	471.77	91.4 μA/mm (4.57 μA)	5.16E3
5	466.8	42.2 pA/mm (1.98 pA)	1.179E10
10	466.8	109.2 pA/mm (5.46 pA)	4.27E9
15	406.4	48 pA/mm (2.08 pA)	9.77E9
20	387.2	35 pA/mm (1.52 pA)	1.27E10

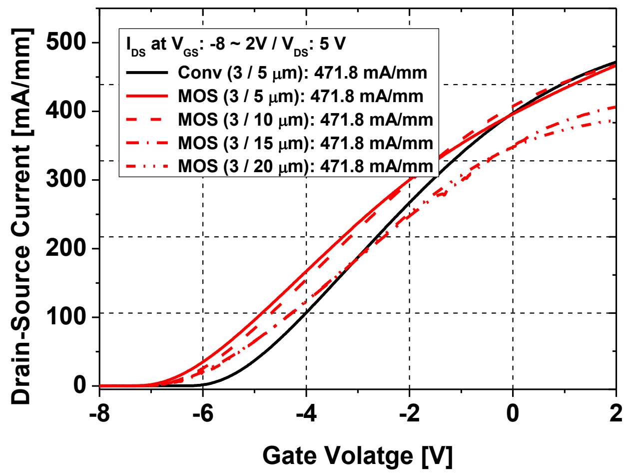
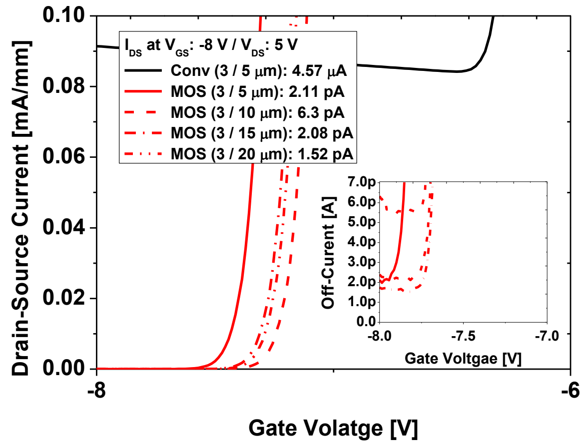
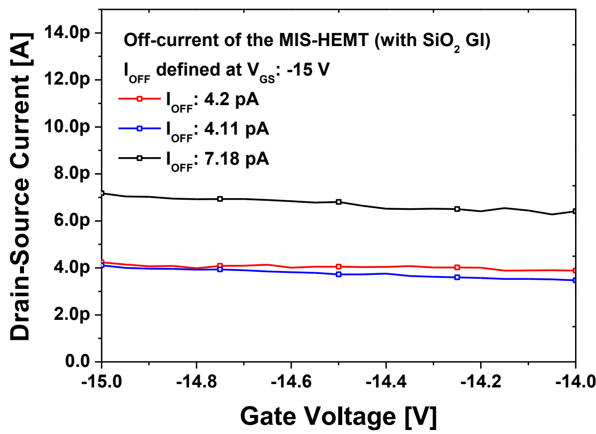


Figure 4.12 Transfer characteristics of the fabricated MOS-HEMT.



(a)



(b)

Figure 4.13 Measured off-current of the MOS-HEMT employing (a) ALD Al_2O_3 gate dielectric, (b) ALD SiO_2 gate dielectric.

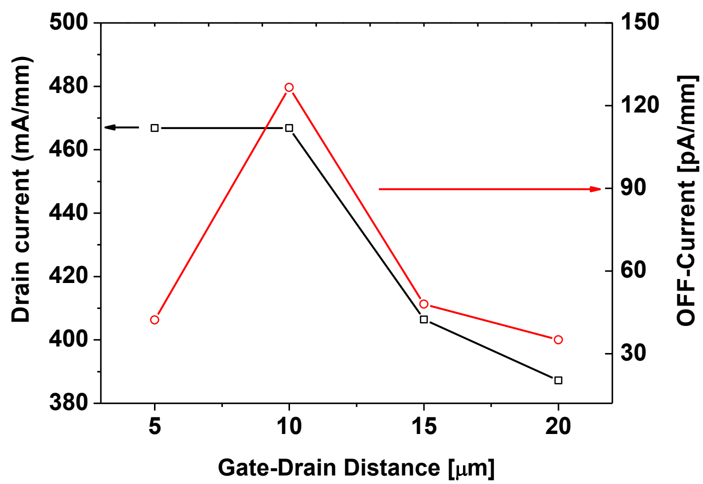


Figure 4.14 Dependency of the transfer characteristic of the MOS-HEMT on the gate-drain spacing (L_{GD}).

4.4.1.4 Output characteristics

The critical parameter to estimate the DC output characteristics of the HEMT is the drain current. It can be controlled mainly by the drain-source voltages (V_{DS}) and gate-source voltage (V_{GS}). Drain current also depends on many other parameters. In case of MOS-HEMTs, some of them are under influence of the gate dielectric layer.

Simply, drain current (I_{DS}) can be expressed as general equation for the current as $I_{DS} = W_G \cdot q \cdot n_S \cdot v$, Where W_G is the gate width, n_s is the concentration of 2DEG, and v is the velocity of the charge carrier in the channel. Without any applied bias (V_{GS}), charge ($Q = q \cdot L_G \cdot W_G \cdot n_s$) stored in 2DEG is determined by the material and structural parameters of the layer system and 2DEG formation mechanism. However, when the gate-source bias (V_{GS}) is applied, the carrier concentration is a function of the gate-source voltage. Assuming that C_{GS} is constant regardless of other external factors, concentration of 2DEG (n_s) is a linear function of V_{GS}:

$$n_s(V_{GS}) = \frac{C_{GS}}{q \cdot L_G \cdot W_G}(V_{GS} - V_{TH}) \quad \text{for } V_{TH} \le V_{GS} \le 0\,V$$

When it comes to v (electron velocity), in the linear region, v is in a linear function of the electric field (E) and expressed as a product form with low field mobility of carrier (μ_0), i.e. $v = \mu_0 \cdot E$. Assuming that drain–source voltage is uniform along the 2DEG, electric field (E) can be calculated from the V_{DS}, i.e. $E = V_{DS}/L_G$ [134]. In the saturation region, carriers in

2DEG have reached the saturation velocity (v_{sat}), so $v = v_{sat}$. Reflection of these two velocity conditions and the dependency of n_s on V_{GS} in the equation for drain-source current (I_{DS}) yields two simple expressions for DC output characteristics as following:

$$I_{DS} = \frac{C_{GS}}{L_{GS}}(V_{GS} - V_{TH}) \cdot \mu_0 \cdot \frac{V_{DS}}{L_G}$$

$$I_{DS} = q \cdot \frac{W_G}{L_G} \cdot n_s \cdot \mu_0 \frac{V_{DS}}{L_G} \qquad \text{for linear region}$$

$$I_{DS} = \frac{C_{GS}}{L_{GS}}(V_{GS} - V_{TH}) \cdot v_{sat}$$

$$I_{DS} = q \cdot W_G \cdot n_s \cdot v_{sat} \qquad \text{for saturation region}$$

Compare to simple model presented above, Das et al. has suggested more advanced model [135]. In his model, sheet carrier concentration (n_s) not only depends on the difference between gate-source voltage and threshold voltage (V_{GS}-V_{TH}), but also on the potential ($V(x)$) originating from of drain-source voltage, which is added to total bias applied to the semiconductor below the gate electrode. Then sheet carrier concentration (n_s) can be expressed as

$$n_s(x) = \frac{C_{GS}}{q \cdot L_G \cdot W_G}(V_{GS} - V_{TH} - V(x))$$

With respect to the carrier velocity (v), non-linear relationship including critical electric field (E_C) was introduced. When electric field approaches to E_C, carrier velocity attain a half of the saturation velocity represented as $v_{sat} = \mu_0 \cdot E_C$ by the following equation:

$$v = \frac{\mu_0 \cdot E}{1 + E/E_C}$$

Taking these modified parameters into account, conventional two expressions for DC characteristics were changed into complex equations describing the drain current of the device more accurately:

$$I_{DS} = \frac{C_{GS}}{L_G}\left[(V_{GS} - V_{TH}) \cdot \mu_0 \cdot \frac{V_{DS}}{L_G} - \mu_0 \cdot \frac{V_{DS}^{\ 2}}{2L_G}\right] \cdot \left(1 + \frac{V_{DS}}{V_C}\right)^{-1} \text{ for linear region}$$

$$I_{DS} = \frac{C_{GS}}{L_G}(V_{GS} - V_{TH} - V_{DS_sat}) \cdot v_{sat} \qquad \text{for saturation region}$$

Figure 4.15 shows the measured DC output current. DC output characteristic was measured up to drain-source voltage (V_{DS}) of 10 V with various gate-source voltages (V_{GS}). V_{GS} applied to device ware increased from -7 V to 2 V with the ramping rate of 3 V/step. The maximum drain saturation current (I_{DSS}) of the AlGaN/GaN MOS-HEMT with L_{GD} of 5 μm at V_{GS} of 2 V was 539.3 mA/mm, which was slightly higher than that of the conventional HEMT with the same device geometry (535.6 mA/mm). Other device parameters from output DC characteristics were summarized at the table 4-4.

In the previous section (5.3.1.4, C-V measurement), sheet carrier concentration of the MOS-HEMT (n_s=2.59×10^{13} cm^{-2}) was 18 % lower than that of the conventional HEMT (n_s=3.18×10^{13} cm^{-2}). As shown in the expressions for drain current (whether simple or advanced) regardless of the operation regime, drain current is essentially in proportion to

concentration of 2DEG. Consequently, albeit 18 % lower carrier concentration of MOS-HEMT, other factors of MOS-HEMT excluding carrier concentration made a contribution to higher drain current than that of conventional HEMT. It was expected that high drain current of MOS-HEMT was attributed to two factors. The first one was the passivation effect of the Al_2O_3 dielectric layer. Although no evidence was observed in this work that Al_2O_3 dielectric made a contribution to increase the density of sheet carriers, it was confirmed that dielectric layer prevented the resistance of the access region of the device from being increased.

It was generally accepted that some key parameters of the HEMTs were susceptible to the electrical condition of surface states. Donor-like surface states with E_D (energy level of donor-like state) distributed on the surface was positively charged, when they were empty (due to the modulation doping in AlGaN barrier) [136]. If empty surface states were occupied by electrons from many sources, occupied donor-like states become electrically neutral and reduce the channel electrons induced at the hetero-interface due to the charge neutrality of the whole heterostructure. Consequently, resistance of the local region where depletion due to occupied surface states takes place increases. It is too large to be neglected once it occurs. This parasitic resistance in the access region (exposed active region between electrodes, denoted as R_S and R_D in Fig. 4. 16) has an adverse effect on the transportation of the carriers passing through the active region, which leads to the degradation of the forward characteristic of the device. Especially, parasitic source resistance (R_S) has a major impact on the output of the HEMT. The higher parasitic source

resistance, the lower saturation drain current ($I_{DS\ sat}$), the less steep the slope of I_{DS} in the linear regime.

In case of the MOS-HEMT, the slope of I_{DS} in the linear regime was steeper than that of the conventional one with the same gate-drain spacing (L_{GD}) (in Fig. 4. 15 (b)). It was the evidence to show that an occurrence of the parasitic source resistance was suppressed by the Al_2O_3 dielectric layer. Slope of the I_{DS} was expressed as on-resistance (R_{ON}) extracted at the V_{DS} of 2 V. On-resistance of MOS-HEMT was 9.22 Ω-mm while that of the conventional one was 9.59 Ω-mm. This indicated that drain current of the MOS-HEMT increased more steeply than conventional device did. The saturation drain current was of the MOS-HEMT was higher than that of the conventional one. Measured $I_{DS\ sat}$ of MOS-HEMT was 539.3 mA/mm while that of the conventional one was 535.6 mA/mm. The difference in drain current decreased at the $V_{D\ sat}$ of the MOS-HEMT was higher than the difference at the V_{DS} of 10 V. The negative slope of the I_{DS} in the saturation regime was thought to be attributed to the current collapse caused by channel-heating (self-heating) [137]. Conventional device without dielectric layer got an advantage on the heat-dissipation. No current collapse due to self heating was observed in I_{DS} of the conventional device. On contrary, MOS-HEMT with Al_2O_3 layer experience current collapse due to self-heating at the drain voltage over $V_{DS\ sat}$. As referred at the chapter 4.2.1, current collapse observed in the DC output characteristic of the MOS-HEMT was due to the poor thermal conductivity of the Al_2O_3 film.

The other factor to make a contribution to the higher drain current of the

MOS-HEMT was field effect mobility of the channel carrier. In general, electron mobility (μ_0) of the AlGaN/GaN heterostructure was reported to be up to 2000 $cm^2/V \cdot s$ (in usual 1700~1900 $cm^2/V \cdot s$). Measured electron mobility of the heterostructure used in this work was in the range from 1123 to 1170 $cm^2/V \cdot s$ (table 1.2). It was generally accepted that such a high electron mobility was due to the separation of channel carriers from ionized impurities. However, electron mobility measured through the fabricated HEMT under a high electric field was much lower than electron mobility (μ_0) measured through the Hall pattern.

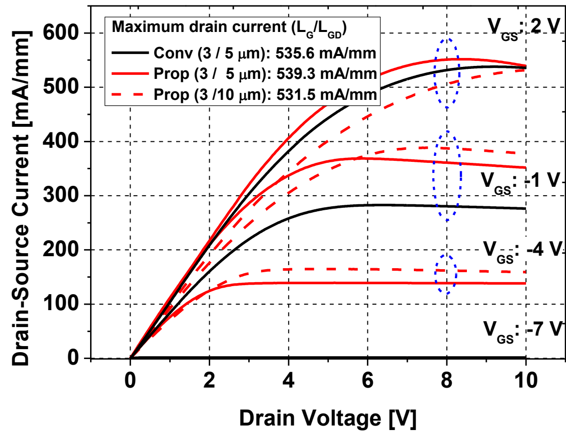
Low field-effect mobility (μ_{FE}) was attributed to the scattering cause by a variety of scattering centers. When the carriers were swept toward one direction by a high electric field, carriers of high density in the channel could be a scatter. Electrons trapped by the surface states distributed on the active region of the device also could interfere with the carrier transport. It was reported that even though they were spatially apart from the channel due to the barrier layer, coulomb scattering caused by trapped electrons of high density was strong enough to decrease the mobility of the channel carrier [138-139]. Roughness of the hetero-interface between AlGaN barrier and GaN buffer was also reported to have a major impact on the carrier transport of the HEMT. Dislocations of large density in the GaN buffer also could be an important scattering center. The core of the dislocations had dangling bonds that introduced electric states, which made dislocations a line of charge. Such charged dislocations scattered electrons involved in conduction. However, the latter were factors impossible to be improved because it was formed

during epi-growth process.

Figure 4.17 showed a measured field-effect mobility of the AlGaN/GaN MOS-HEMT in the saturation regime (V_{DS}>V_{GS}-V_{TH}). Field-effect mobility of the conventional device decreased and saturated as the drain voltage increased while that of the MOS-HEMT increased as drain bias increased. At the drain voltage of the 10 V, field-effect mobility of the MOS-HEMT was 289 $cm^2/V{\cdot}s$ which was 9.5 % higher than that of the conventional one (263 $cm^2/V{\cdot}s$). High field-effect mobility of the MOS-HEMT was achieved by the MOS structure employing ALD Al_2O_3 dielectric layer. Al_2O_3 layer deposited on the active region electrically encapsulate the surface states so that fewer electrons were trapped in the surface state. It was led to the reduction in the density of remote scattering center. By this mechanism, high field-effect mobility of the MOS-HEMT was achieved. As indicated in the expression for DC output characteristics, drain current of the device was directly proportional to field-effect mobility. Consequently, high field-effect mobility and high saturation velocity of the MOS-HEMT made a significant contribution to high drain current.

Table 4-4 Parameters describing DC output characteristics

Device (L_G/L_{GD})	Drain current V_G:2V / V_D:10 V	R_{ON} [Ω-mm]	R_{ON-SP} [mΩ-cm^2]	Field Effect Mobility V_G:2V / V_D:10 V
HEMT (3/5 μm)	535.6 mA/mm	9.59	4.79	263 cm^2/V·s
MOS (3/5 μm)	539.3 mA/mm	9.22	4.61	289 cm^2/V·s
MOS (3/10 μm)	531.5 mA/mm	10.5	5.25	-



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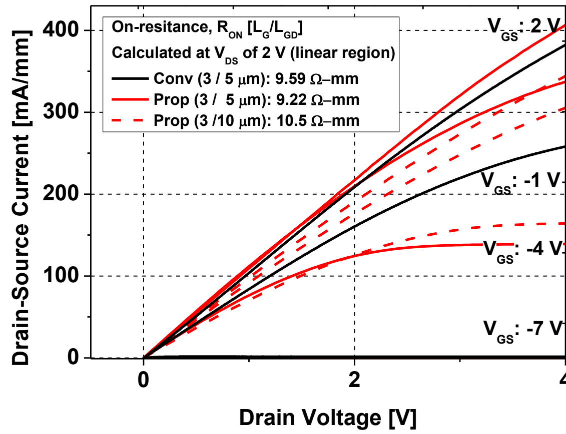


(b)

Figure 4.15 (a) I-V characteristic of the fabricated AlGaN/GaN MOS-HEMT, (b) on-resistance extracted at V_{DS} of 2 V.

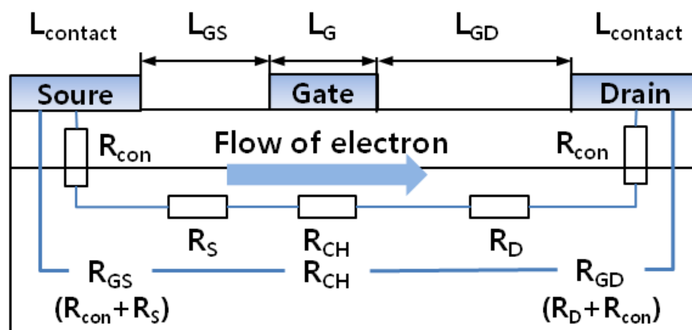


Figure 4.16 Schematic diagram describing the effect of surface states in the access region. The access regions L_{GS} and L_{GD} contribute parasitic resistance R_S and R_D. Slope of I_{DS} in the linear regime and saturation current ($I_{DS\,sat}$) mainly depends on the R_{GS}.

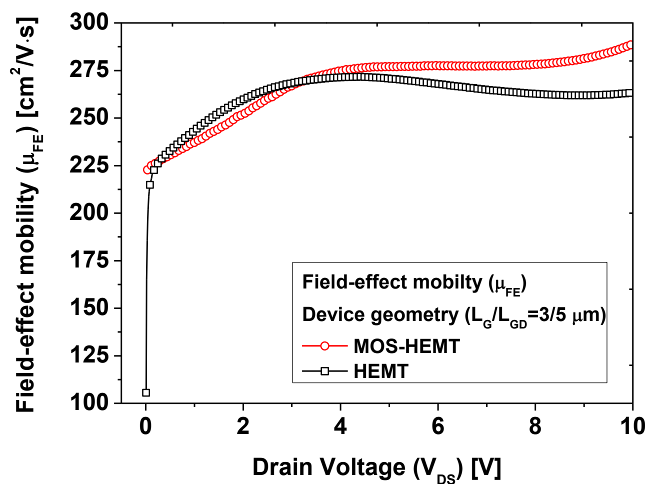


Figure 4.17 Measured field-effect mobility (μ_{FE}) of the fabricated AlGaN/GaN MOS-HEMT.

4.4.1.5 Pulsed I-V characteristics

The pulsed I-V measurement is an effective tool to detect the effects caused by electric states (traps) and indentify the passivation mechanisms that alleviate the trap-related effects without the use of the complicated impedance-matching circuits [140]. In addition, it minimizes the burn-in degradation and the reduction of mobility due to poor thermal dissipation (low heat removal rate) [141].

This method is generally used to investigate the DC/RF dispersion, which is represented as the reduction of the drain current (I_{DS}) under operation with higher frequency compared to DC operation. Characterization of the pulsed I-V characteristic was performed by applying a pulse type gate-source voltage and drain-source voltage. Both pulse signals were synchronized. Figure 4.18 illustrate condition of the pulses for this work. The gate pulse was changed from pinch-off voltage (-9 V) to four values (-7, -4, -1, 2 V) while drain pulse was increased from 0 V to 10 V with ramping rate of 40 mV/step. Period and width of all pulses were 5 μs and 1ms respectively.

Pulsed I-V characteristic of the AlGaN/GaN MOS-HEMT is shown in Fig. 4.19. Results from pulsed I-V measurement were summarized at the table 4-5. DC output currents ($I_{DS\,(DC)}$) were lower than pulsed output current ($I_{DS\,(Pulse)}$). Drain current from pulsed I-V measurement was 658 mA/mm which was 22 % higher than the DC drain current (539.3 mA/mm). The ratio of the drain current from pulsed I-V measurement to that from DC

measurement ($I_{DS\,(Pulse)}/I_{DS\,(DC)}$) is an index to quantify the current collapse phenomena. $I_{DS\,(Pulse)}/I_{DS\,(DC)}$ of the fabricated AlGaN/GaN MOS-HEMT was over unity. It indicated that in the pulsed output characteristic of the MOS-HEMT with operating frequency of 1 kHz, degradation resulted from trap-related effect was not observed. It was thought that pre-passivation of the device using ALD Al_2O_3 dielectric made a significant role to suppress the electron trapping, which prevented the degradation caused by trap-related effect. Negative slope caused by self-heating in DC output characteristic was not observed in pulsed I-V characteristics. It was ascribed to the mitigation of self-heating effect due to the pulse biasing.

Table 4-5 Parameters describing pulsed I-V characteristics

Device (L_G/L_{GD})	I_{DS} (DC) V_{GS}:2 / V_{DS}:10 V	I_{DS} (Pulsed) V_{GS}:2 / V_{DS}:10 V	$I_{DS\,(DC)}/\ I_{DS\,(Pulse)}$
MOS (3/5 μm)	539.3 mA/mm	658 mA/mm	Over unity
MOS (3/10 μm)	531.5 mA/mm	624 mA/mm	Over unity

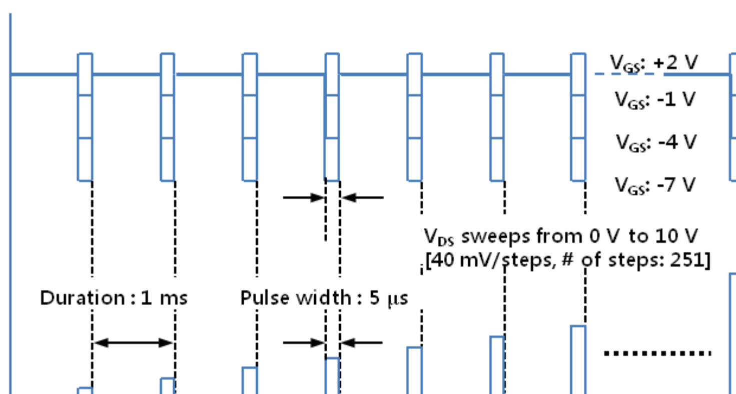


Figure 4.18 Schematic of the bias pulse sequence to be applied to gate and drain electrodes of the device.

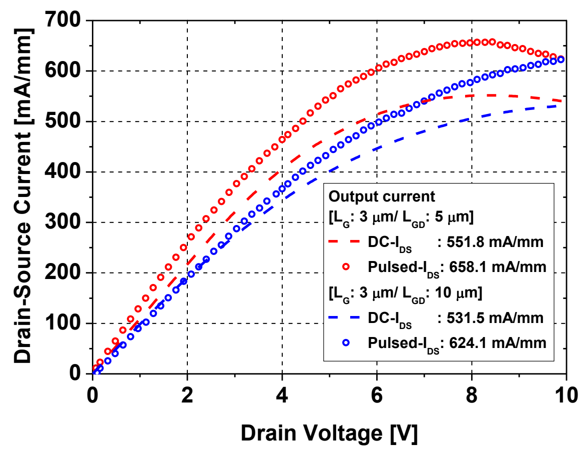


Figure 4.19 Pulsed I-V measurement of the fabricated AlGaN/GaN MOS-HEMTs with gate length of 3 μm and gate-drain spacing of 5/10 μm.

4.4.2 Reverse blocking characteristics

4.4.2.1 Leakage current

GaN-based devices have been considered as a prime candidate for high power devices due to its excellent material properties. However, GaN-based devices such as GaN metal-semiconductor field-effect transistor (MESFET) and AlGaN/GaN HEMT device suffer from high leakage current which prevents the device from approaching their full capability for high power level. As referred to in the chapter 2.5.2 (Leakage current), there are many leakage components classified according to their path (leakage path). Their contributions to total leakage current are also different. Leakage current of the device can be largely categorized as leakage current in the active region and that in the peripheral region. It is known that part of gate electrode (gate feed) and part of ohmic electrodes are deposited on the etched peripheral region including mesa wall. It is supposed that parasitic leakage current flow though the peripheral region. However, its contribution to total leakage current is not significant. In addition, as the operating temperature increased, portion of the peripheral leakage current to total leakage current decreased due to its negative temperature coefficient (Fig. 2.21).

Fig. 4.20 showed a leakage current in the peripheral region of the conventional and MOS-HEMT. Test patterns for the measurement of peripheral leakage current were co-fabricated in the same pie. Test pattern consisted of two isolated islands on which ohmic contact was

formed and distance between them was 20 μm. Peripheral leakage current was measured at the bias of 100 V. Measure peripheral leakage current of the MOS-HEMT was in the range from 1.798 pA/mm to 2.13 pA/mm which was 6 orders of magnitude lower than that of the conventional HEMT (16.2 ~ 19 μA/mm). It was a noticeable result to indicate the passivation effect of the ALD Al_2O_3 dielectric. In general, peripheral region is exposed to the plasma damages due to isolation process and full of defects and surface states of high density. These surface states can be the path for leakage current. However, in the MOS-HEMT, surface states in the peripheral region were buried by pre-passivated ALD Al_2O_3 layer. Carrier transport along the passivated surface was suppressed with reducing peripheral leakage current.

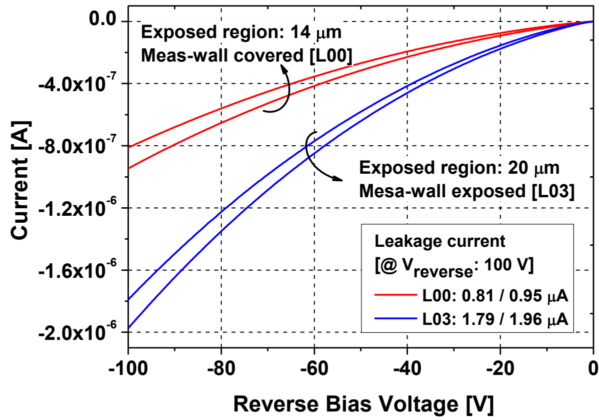
Most critical factor to determine the blocking characteristic and the power efficiency in the off-state was leakage current in the active region. The MOS-HEMTs fabricated through the passivation-first process suppressed drain leakage current and sustained the higher breakdown voltage in the blocking mode. Pre-deposited Al_2O_3 dielectric layer not only protected the device from the possible physical damages during fabrication process but also prevented permeation of the oxygen into the surface of the semiconductor which caused off-state degradation [142-143]. The gate electrode deposited on the Al_2O_3 dielectric was physically and electrically separated from the source of the leakage current sources on the active region. The isolation of the gate electrode by ALD-Al_2O_3 suppressed the gate leakage current effectively. Fig. 4.21 shows the measured leakage current of the fabricated MOS-HEMTs with ALD Al_2O_3 dielectric. Leakage current was measured under the reverse bias

condition where the gate and drain voltage were -10 V, 100 V respectively.

The measured drain leakage current of the conventional HEMTs with L_{GD} of 20 μm was 80 μA/mm (4 μA) while that of the MOS-HEMTs with the same L_{GD} was 0.2 nA/mm (10.4 pA). The drain leakage current was decreased as gate-drain distance (L_{GD}) increased. The leakage suppression effect in the gate leakage current was more obvious. Gate leakage current was reduced by 6-orders of magnitude. The gate leakage of the conventional HEMTs with L_{GD} 15 μm was 69 μA/mm (3.45 μA) while that of the MOSHEMTs with the same L_{GD} was 17.6 pA/mm (0.88 pA). The portion of the gate leakage current to the total leakage current (I_G/I_{DSS}) is one of the important criteria to evaluate the electrical robustness of the MOS-gate structure. As shown in Fig. 4.22, the ratio of the conventional HEMTs was kept similar (~ 0.84) regardless of the device geometry. This indicated that conventional Ni gate contact was vulnerable to the electron injection and, subsequently, blocking capability of the device was degraded by the poor rectifying Ni-based Schottky contact. In case of the MOS-HEMT using dielectric material of poor insulation property, it is hard for the device with the dielectric to reach its intrinsic or potential blocking capability due to the dielectric breakdown (shown in Fig. 4.23). Current runaway in insulator affected by impact ionization inside insulator can cause the premature breakdown of the device. It means that breakdown of the device is mainly dependent on the ruggedness of the dielectric film, irrespective of the blocking capability of the HEMT itself.

On the other hand, the portion of the gate leakage current of the MOS-

HEMTs device was around 0.1. It suggested that, at the gate region, the blocking capability of the MOS-HEMT was more electrically robust than that of the conventional HEMTs and less sensitive to the electron injection due to the insertion of Al_2O_3 film.



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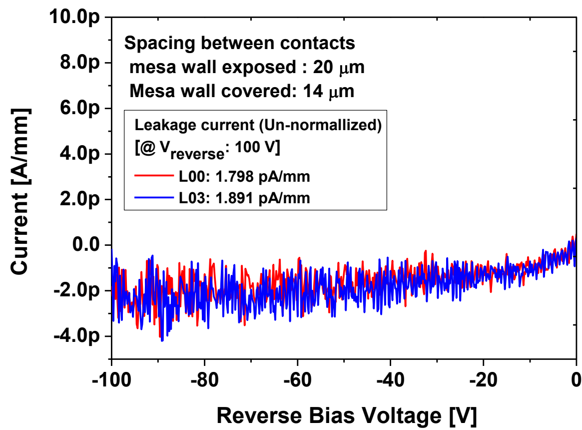
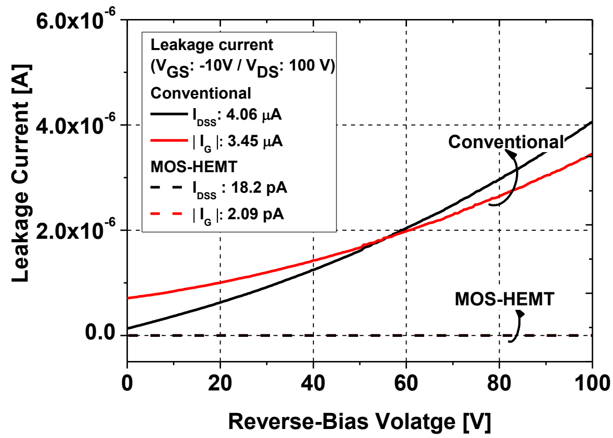


(b)

Figure 4.20 Leakage current flowing through the peripheral region of the (a) conventional device, (b) MOS-HEMT.



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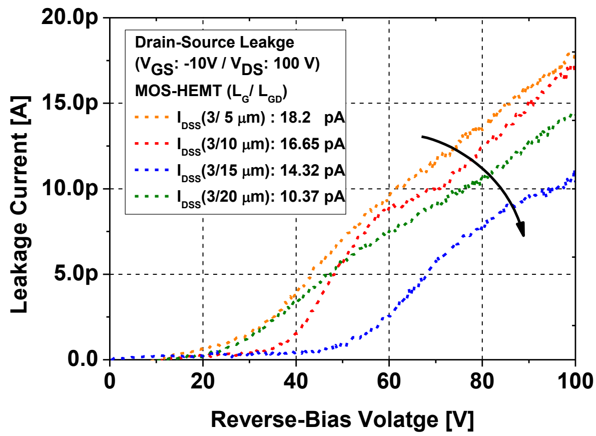

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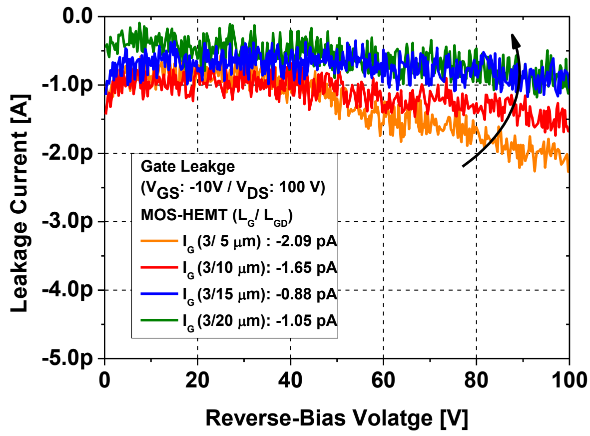
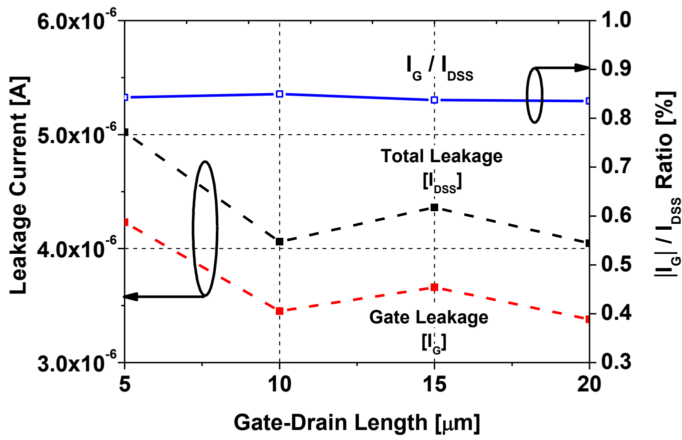


(c)

Figure 4.21 Measured drain-source leakage current (I_{DSS}) of the (a) conventional HEMT, (b) drain-source leakage current (I_{DSS}), (c) gate leakage current (I_G) of the fabricated MOS-HEMT with various gate-drain spacing (L_{GD}: 5, 10, 15, 20 μm).



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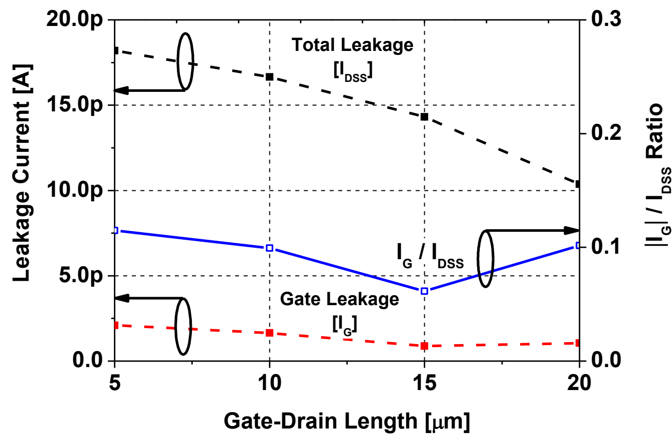
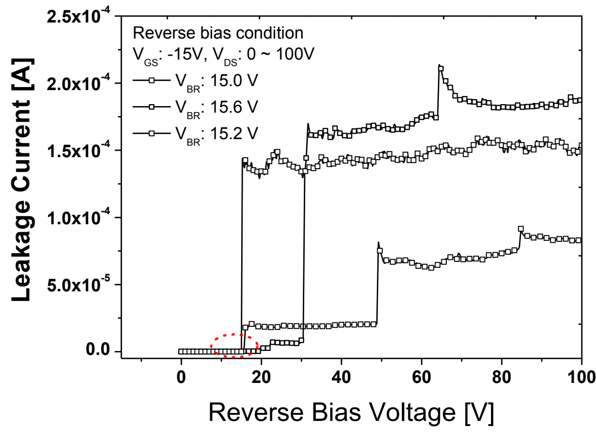


(b)

Figure 4.22 Portion of the gate leakage current (I_G/I_{DSS}) of the fabricated MOS-HEMT with various gate-drain spacing (L_{GD}: 5, 10, 15, 20 μm).



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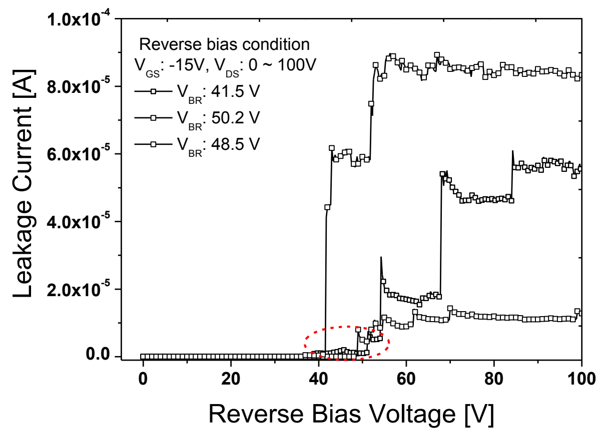


(b)

Figure 4.23 Blocking characteristics of the MOS-HEMT employing ALD SiO_2 dielectric.

4.4.2.2 I-V characteristics of the gate diode

The gate diode characteristics of the fabricated MOS-HEMTs were much improved compared to conventional HEMT and other MOS-HEMT employing ALD SiO_2 dielectric. The MOS-HEMT employing ALD Al_2O_3 showed a superior leakage-suppression capability in both directions (forward and reverse) to that of other devices. The forward and reverse characteristics of the MOS-HEMT using ALD Al_2O_3 dielectric was shown in Fig. 4.24 and 4.25. Parameters describing gate diode I-V characteristic was summarized at the table 4-6.

All I-V curves obtained from gate diode was asymmetric more or less. It was a matter of degrees. It was ascribed to the asymmetric potential barrier height at the interface. Namely, there was a considerable difference between the barrier seen by electrons in the metal (reverse direction) and that seen by electrons in the semiconductor (forward direction). In case of the devices for high power and high voltage operation, it is required that gate diode should suppress the leakage current in both direction equally. To do so, I-V characteristics of gate diode should be symmetric to some degree with allowing low leakage diode current.

It was noticeable that the difference in the leakage current between conventional and MOS-HEMT employing ALD Al_2O_3 was remarkable in both direction. The applied voltage for the forward operation of the gate diode was 5 V. Measured forward and reverse diode current of the

conventional HEMT were 5.8 mA and 0.142 μA while that of the MOS-diode were 2.61 nA and 0.825 pA respectively which was lower 6 orders of magnitude. In case of the MOS-HEMT using ALD SiO_2, reverse diode current (1.6 nA) was 2 orders of magnitude lower than that of the conventional HEMT but it was much larger than that of the MOS-HEMT with ALD Al_2O_3. In addition, forward diode current of the MOS-HEMT using ALD SiO_2 was in mA order. Aforementioned, asymmetric diode characteristic of the device for high power operation was not desirable. From experimental results, insulation property of the ALD SiO_2 dielectric layer poor and the devices of MOS structure using this dielectric film have a risk of the occurrence of dielectric breakdown.

Barrier height of the MOS-HEMT was extracted from the diode I-V characteristics. The diode current can be given by the thermionic emission (TE) model and is expressed as

$$I = I_S \exp(\frac{qV}{nkT})\left[1 - \exp(\frac{-qV}{kT})\right],$$

Where n is the ideality factor, and I_S means the saturation current obtained at the applied voltage of 0 V during the voltage sweeping from -5 to 5 V and was given by

$$I_S = AA^*T^2 \exp(\frac{-q\Phi_B}{kT}),$$

Where A is the rectifier contact area, $A^*(=4\pi qk^2m^*/h^3)$ is the effective Richardson constant (34.06 $A/cm^2 \cdot k^2$ for $Al_{0.3}Ga_{0.7}N$), T is the temperature in Kelvin, k is the Boltzman constant, q is the electronic charge, and Φ_B is

the barrier height. Extracted barrier height was also summarized at the table 4-6. The balanced barrier height of the MOS diode employing ALD Al_2O_3 layer was about 9.33 eV at room temperature while that of the conventional gate diode and MOS diode with ALD SiO_2 were 0.845 and 0.918 eV respectively. From this experimental result, it was proved that MOS-diode employing ALD Al_2O_3 dielectric was more suitable to be used as a gate structure of the power device than others in that term of the leakage current and symmetry of the diode characteristics.

The mechanisms of the gate leakage current were analyzed by using the equations for various carrier transport models in insulating films. It was found that three transport mechanisms were involved in the gate leakage current of the MOS-HEMT (Frenkel-Poole emission, Schottky emission, Fowler Nordheim tunneling). Fig. 4.26 and 4.27 shows the Frenkel-Poole fitting of the conventional and MOS-diode. I-V characteristics of the conventional diode showed straight line in the equation for ln(I/V) versus $V^{1/2}$ in both direction. It indicated that diode leakage current of the conventional diode in both directions was based on Frenkel-Poole emission. It could be interpreted into that carrier transport of the conventional diode was based on trap-assisted tunneling. On contrary, MOS-diode did not show the fitness to the Frenkel-Poole emission mechanism. It could be interpreted that ALD Al_2O_3 dielectric layer of the MOS-diode prevented carrier transport through the traps distributed on the surface by insulating the surface of the semiconductor.

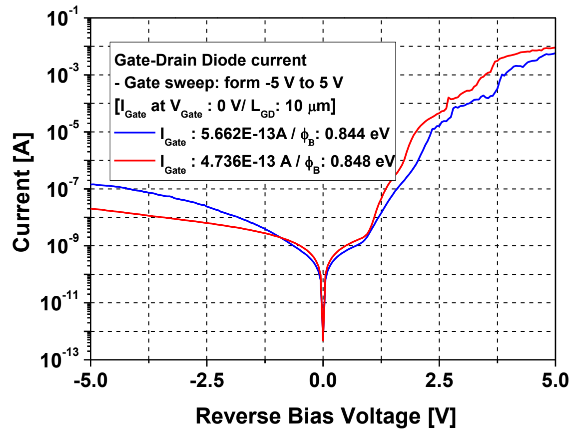
Fig. 4.28 and 4.29 illustrates the Fowler-Nordheim tunneling fitting of the conventional and MOS-diode. Both the devices (conventional and MOS-

diode) showed a fitness to FN tunneling. As shown in Figures, MOS-diode experienced FN tunneling at the higher voltage than conventional diode did. It meant that the mechanism responsible for the diode leakage current was FN tunneling and Al_2O_3 dielectric just postponed the point at which tunneling occurred.

Fig. 4.30 illustrates the Schottky emission fitting of the conventional and MOS-diode. Only the I-V characteristics of the conventional diode showed straight line in the equation for $\ln(I/T^2)$ versus $V^{1/2}$. I-V characteristics of the conventional diode showed a wide straight line in the whole bias range. It meant that the dominant mechanism for the diode leakage current was Schottky emission. In case of the MOS-diode, it was hard to occur the Schottky emission process at room temperature due to high offset of the conduction band formed by Al_2O_3 dielectric. However, I-V characteristics of the MOS-diode at the high temperature showed the fitness to the Schottky emission. It will be explained at the next section.

Table 4-6 Parameters describing gate diode I-V characteristics of the fabricated MOS-HEMT

L_{GD}: 10 μm	Diode current [A]			
	V_G: -5 V	V_G: 0 V	V_G: 5 V	Φ_B
Conventional	0.142 μA	5.66E-13 A	5.84 mA	0.844
	0.022 μA	4,74E-13 A	9.19 mA	0.848
MIS-HEMT with SiO_2	1.6 nA	9.66E-14	1.76 mA	0.889
	2.77 nA	1.0E-14	2.16 mA	0.948
MIS-HEMT with Al_2O_3	0.825 pA	1.94E-14	2.61 nA	0.931
	0.474 pA	1.77E-14	3.44 nA	0.934



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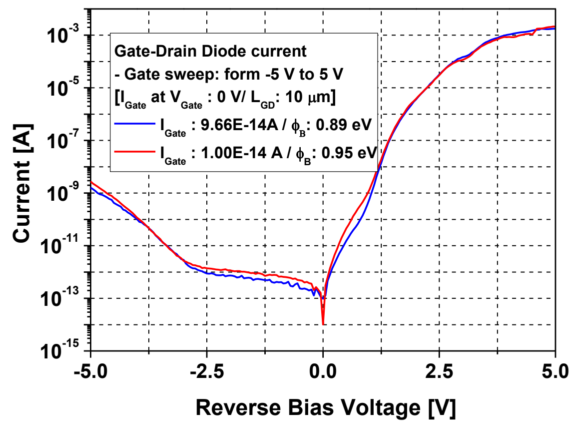
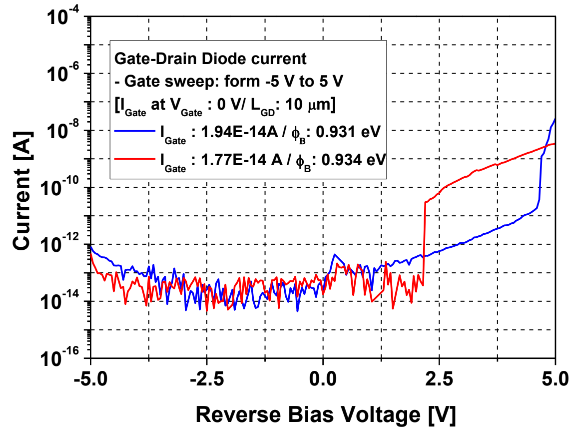
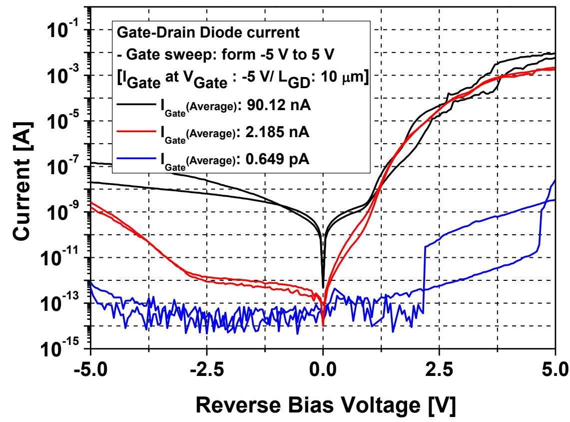


(b)

Figure 4.24 Gate diode I-V characteristics of the (a) conventional HEMT, (b) MOS-HEMT employing ALD SiO_2.

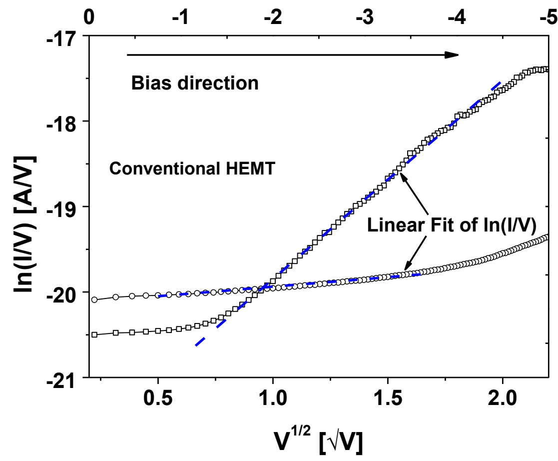


(a)



(b)

Figure 4.25 Gate diode I-V characteristics of the (a) MOS-HEMT employing ALD Al_2O_3 dielectric, (b) Comparison.



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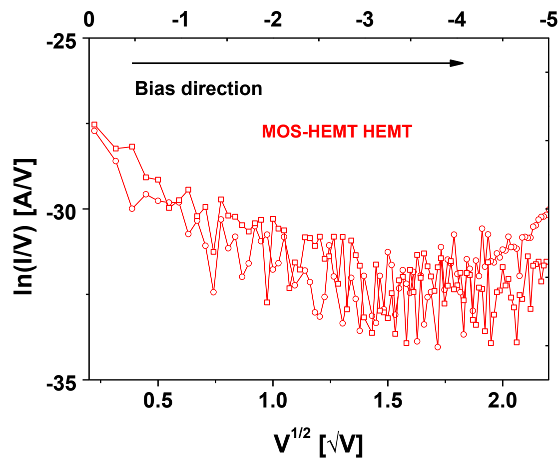


(b)

Figure 4.26 Poole-Frenkel fitting of the (a) conventional HEMT, (b) MOS-HEMT in the negative bias region. Poole-Frenkel emission is indicated by the straight line in the plot of ln(I/V) versus $V^{1/2}$.

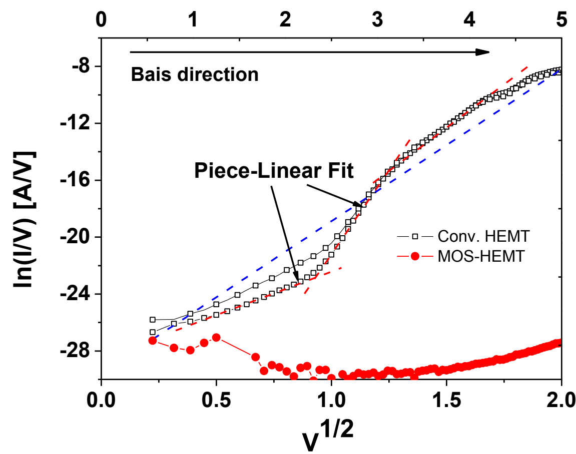
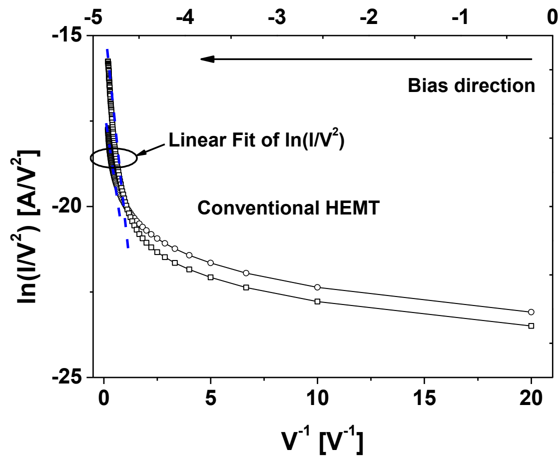


Figure 4.27 Poole-Frenkel fitting of the HEMT in the positive bias region. Poole–Frenkel emission is indicated by the straight line in the plot of ln(I/V) versus $V^{1/2}$.



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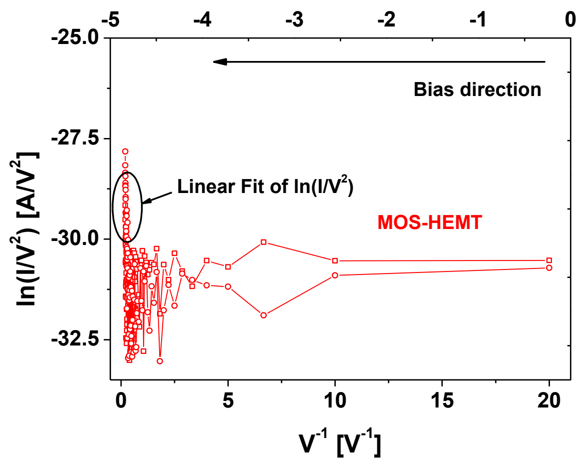


(b)

Figure 4.28 Fowler-Nordheim tunneling fitting of the (a) conventional HEMT, (b) MOS-HEMT in the negative bias region. FN tunneling is indicated by the straight line in the plot of $\ln(I/V^2)$ versus V^{-1}.

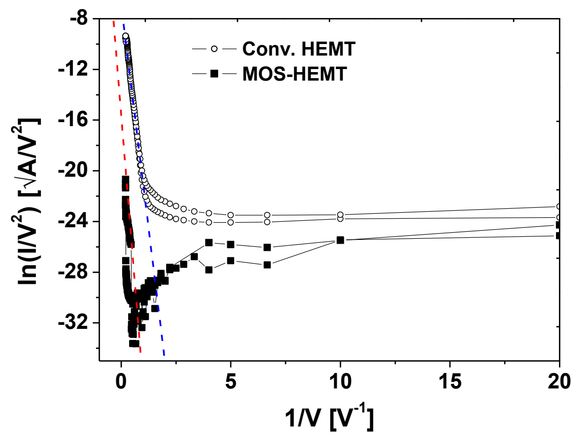
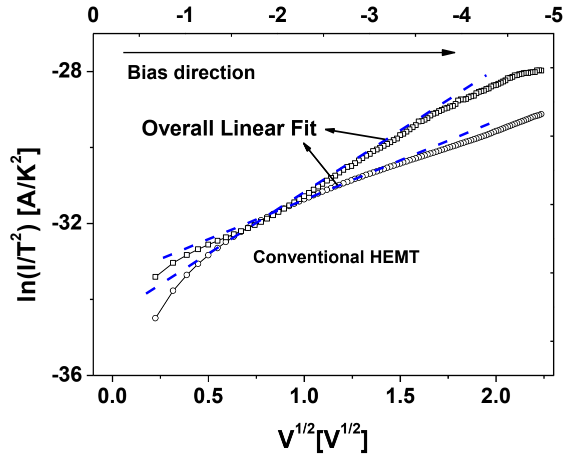
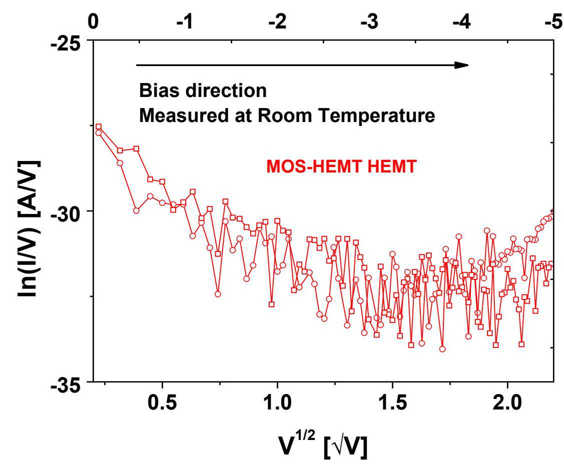


Figure 4.29 Fowler-Nordheim tunneling fitting of the HEMT in the positive bias region. FN tunneling is indicated by the straight line in the plot of $\ln(I/V^2)$ versus V^{-1}.



(a)



(b)

Figure 4.30 Schottky Emission fitting of the (a) conventional, (b) MOS-HEMT HEMT in the negative bias region. Schottky emission is indicated by the straight line in the plot of ln(I/V) versus $V^{1/2}$.

4.4.2.3 Electrical ruggedness of the MOS-HEMT

Ruggedness is the Key feature to decide the reliability of the device for high power of high voltage operation. In general, power devices are frequently exposed to harsh condition where other devices cannot survive (high temperature and high reverse voltage). Lifetime acceleration test based on various stress conditions is performed on power devices to investigate the ruggedness of the power device.

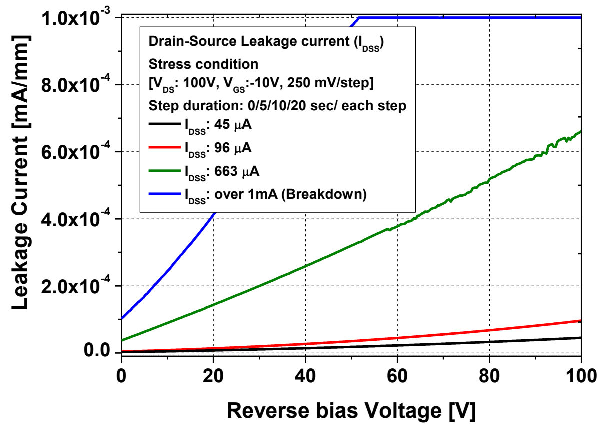
In this work, simple acceleration test was carried out to the fabricated MOS-HEMT by applying drain bias step stress with various step duration time. High temperature reverse bias (HTRB) test was also performed on MOS-HEMT. Fig. 4.31 and 4.32 shows the leakage current of the conventional and MOS-HEMT during acceleration test. As the step duration time was increased, leakage current of the conventional device was increased rapidly so that after 3 times of repetitions, leakage current was reached preset current level (1mA/mm). It indicated that conventional device was vulnerable to the continuous electrical stress and prone to be degraded rapidly by stress condition. However, the MOS-HEMT was sustained stress condition with effectively suppressing a leakage current. Measured drain-source leakage current after the 3 times of repetitions was 12.3 pA. At the end of the 4th stress, breakdown hard breakdown took place. It meant that MOS-HEMT employing ALD Al_2O_3 dielectric have more stable reliability than that of the conventional one.

Figure 4.33 shows the Arrhenius plot from the leakage current of the

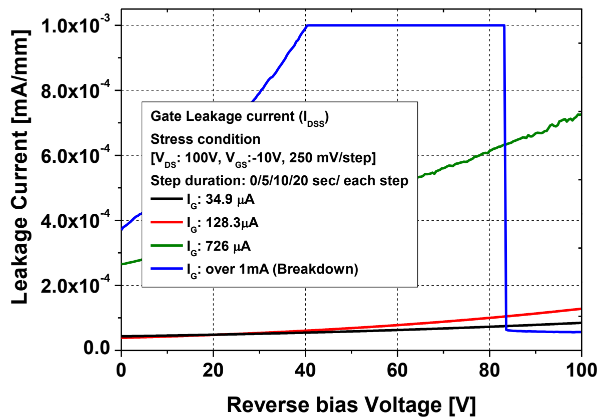
MOS-HEMT during HTRB test. HTRB test was performed at the condition where reverse drain voltage of 100 V at high operating temperature up to 200 ℃. Even though the leakage current of the MOS-HEMT was 2 orders of magnitude lower than that of the conventional one, leakage current of the MOS-HEMT was increased more rapidly than that of conventional devices. It was attributed to the poor heat removal of the MOS-HEMT. Thermal conductivity of the Al_2O_3 dielectric is so low that the heat gained from operating temperature and generated from device operation was not dissipated quickly. The internal heat gives electrons a high thermal energy enough to surmount the potential barrier formed by Al_2O_3 at the interface of the MOS-HEMT. This resulted in the rapid increase in the leakage current of the MOS-HEMT. It was confirmed by the diode I-V characteristics of the MOS-HEMT.

Fig. 4.34 illustrates the Schottky emission fitting of the conventional and MOS-diode at room temperature. As explained at the previous section, Only the I-V characteristics of the conventional diode showed straight line in the equation for $\ln(I/T^2)$ versus $V^{1/2}$. It was confirmed that the dominant mechanism for the diode leakage current was Schottky emission and the MOS-diode was not based on the Schottky emission process at room temperature. However, Fig. 4.35 shows Schottky emission fitting of the MOS-diode at the operating temperature of 200 ℃. On the contrary to the I-V characteristics at the room temperature, Diode I-V of the MOS-HEMT exhibited a straight line after the bias below -3 V. It meant that the rapid increase in the leakage current of the MOS-HEMT was attributed to the occurrence of the Schottky emission of the electrons

of high thermal energy.

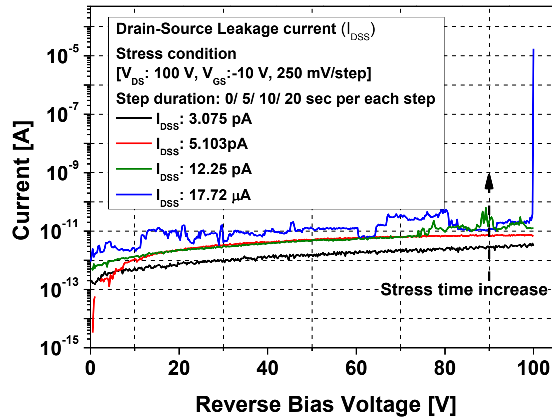


(a)



(b)

Figure 4.31 Measured (a) drain leakage current, (b) gate leakage current of the conventional HEMT during drain bias step stress with various step duration times (0,5,10,20 sec/step).



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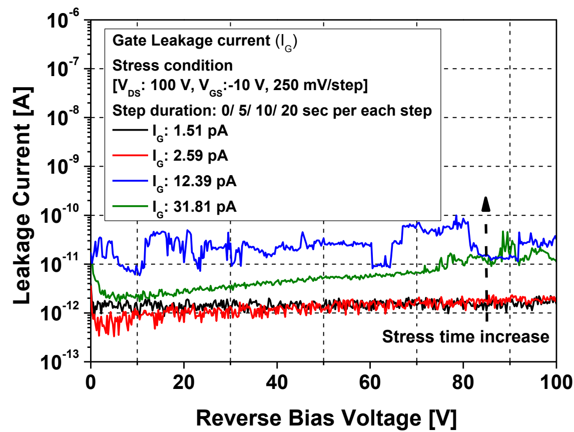


(b)

Figure 4.32 Measured (a) drain leakage current, (b) gate leakage current of the MOS-HEMT during drain bias step stress with various step duration times (0,5,10,20 sec/step).

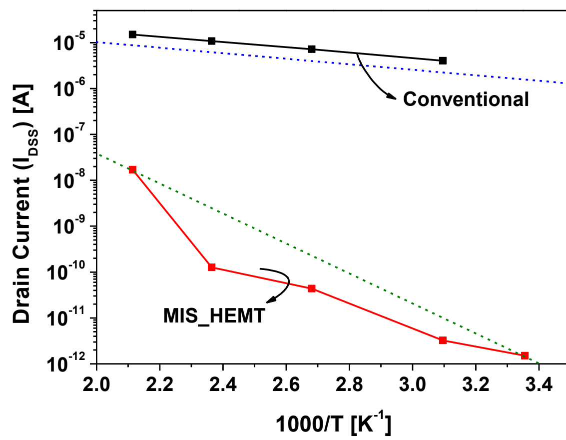


Figure 4.33 Arrhenius plot of the measured drain-source leakage current of the fabricated AlGaN/GaN MOS-HEMT during high temperature reverse bias (HTRB) test.

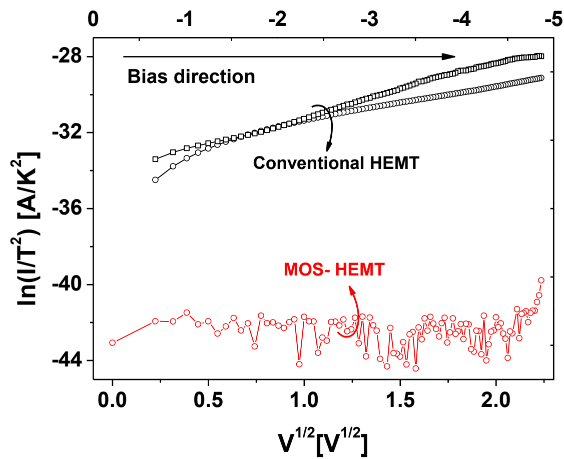
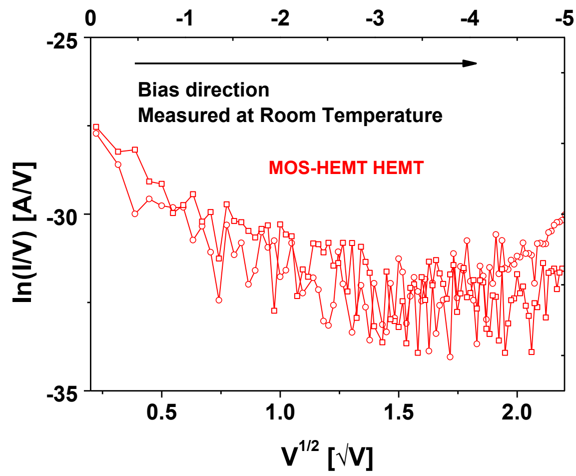


Figure 4.34 Schottky emission fitting in the negative region of the conventional and MOS-HEMT at the room temperature (300 K).



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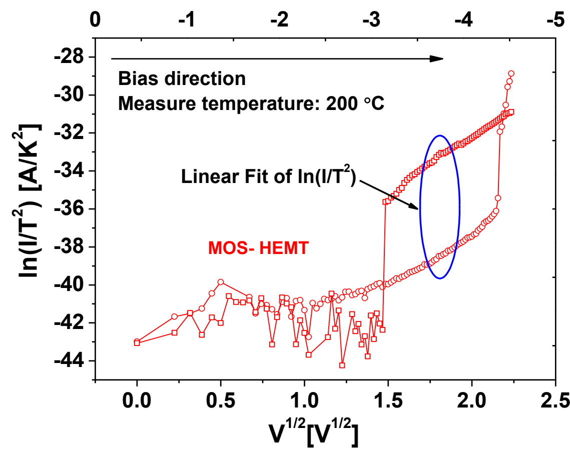


(b)

Figure 4.35 Schottky emission fitting in the negative region of the MOS-HEMT at the (a) room temperature (300 K), (b) 200 ℃ (473 K).

4.4.2.4 Breakdown characteristics

A good device for power application should allow as large current as possible in on-state and high reverse bias and negligible leakage current in off-state to obtain the maximum output power and stable blocking characteristics. In class-A operation, the maximum output power is deiced by the maximum output current ($I_{DS\,MAX}$), the knee voltage (V_{KNEE}), and breakdown voltage (V_{BR}):

$$P_{MAX} = \frac{I_{DS_MAX}(V_{BR} - V_{KNEE})}{8}$$

Especially, for the GaN-based power device which is susceptible to high leakage current, a robust blocking capability is required. Breakdown voltage (V_{BR}) of the device plays a significant role to achieve a system of high efficiency and high reliability.

The breakdown voltage of the device was measured at the sub-threshold gate bias ($V_{GS} < V_{TH}$). During the measurement, the devices were immersed in Fluorinert liquid (3M™ FC-3283) to avoid air breakdown. The air surrounding the devices during the breakdown measurement could be a medium in which short circuit path between two electrodes (gate and drain) formed beyond a certain drain voltage. When the path between two electrodes is formed through the air under high reverse bias, the flash was seen in the air suspected to be a short circuit path in a moment. It is one of the parasitic elements that trigger the breakdown before the device reaches the intrinsic breakdown.

The drain bias increased with keeping the device in off-state and the current was logged until breakdown was identified. The breakdown voltage (V_{BR}) was defined as the drain voltage at which the leakage current exceeded the predefined current value. Preset current value was 1mA/mm which was considered as the current three orders of magnitude lower than the general maximum output current of the device. Leakage current higher than 1mA/mm may result in the severe degradation in device performance and destructive process in the device. Therefore it was considered to be the critical current value at which device breakdown started.

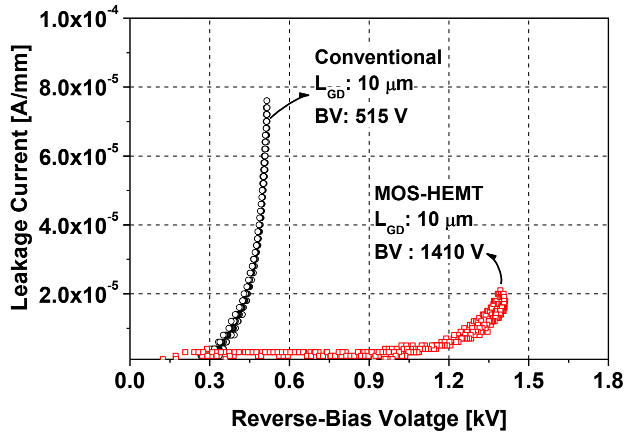
The off-state breakdown of the MOS-HEMT with two gate-drain spacing (L_{GD}) of 10/20 μm was shown in Fig. 4.36. Fabricated AlGaN/GaN MOS-HEMT exhibited a hard breakdown characteristic. On contrary, conventional device showed a soft breakdown characteristic. All parameters describing breakdown characteristics of the MOS-HEMT was summarized and compared with conventional device at the table 4-7. Measured V_{BR} of the MOS-HEMT with L_{GD} of 10 m was 1410 V which was more than two times than that of the conventional one (515 V). The leakage current recorded at the V_{BR} was a criterion to evaluate the blocking capability of the device. Measured leakage current of the MOS-HEMT at V_{BR} was 76 μA/mm while that of the conventional device was 21 μA/mm. It reflected that that blocking capability of the MOS-HEMT employing ALD Al_2O_3 dielectric was superior to that of the conventional one.

The breakdown voltage of the MOS-HEMT with L_{GD} of 20 μm was up to 2

kV (due to the limit of the power compliance in the curve tracer, Tektronix 370A). Actual V_{BR} was supposed to be over 2 kV. The V_{BR} of the conventional one with the same L_{GD} was 1310 V. As the gate-drain spacing was increased, blocking characteristics of the MOS-HEMT was more robust (shown in Fig. 4.36. (b)). It was confirmed by the leakage current. Leakage current of the MOS-HEMT measured at V_{BR} was 6 μA/mm which was about 3 % of the leakage current of the conventional device (206 μA/mm). Figure of merit (FOM) of the MOS-HEMT was increased as gate-drain spacing (L_{DG}) increased. FOM of the MOS-HEMT with of gate-drain spacing of 5 μm was 251 MW/cm^2, FOM of the MOS-HEMT with 20-μm gate-drain spacing was 815 MW/cm^2 (Fig. 4.37). Such a stable blocking characteristics of the AlGaN/GaN MOS-HEMT was ascribed to the passivation effect of the ALD Al_2O_3 dielectric layer.

Table 4-7 Parameters describing breakdown characteristics of the fabricated AlGaN/GaN MOS-HEMT

Geometry (L_G/L_{GD})	V_{BR} [V]	Variation in V_{BR}	Leakage @ V_{BR}	Variation in Leakage
HEMT (3/10 μm)	515	-	76 μA/mm	-
MOS-HEMT (3/10 μm)	1410	174 %	21 μA/mm	-72 %
HEMT (3/20 μm)	1310	-	206 μA/mm	-
MOS-HEMT (3/20 μm)	2000	72.7 %	6 μA/mm	-97 %



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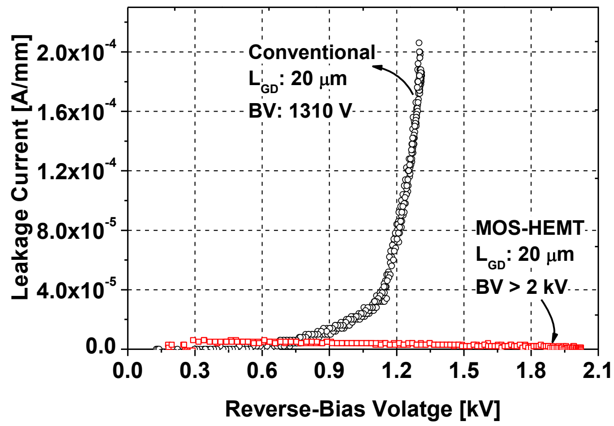

(b)

Figure 4.36 Breakdown characteristics of the fabricated AlGaN/GaN MOS-HEMT with gate-drain spacing (L_{GD}) of 10 μm and 20 μm.

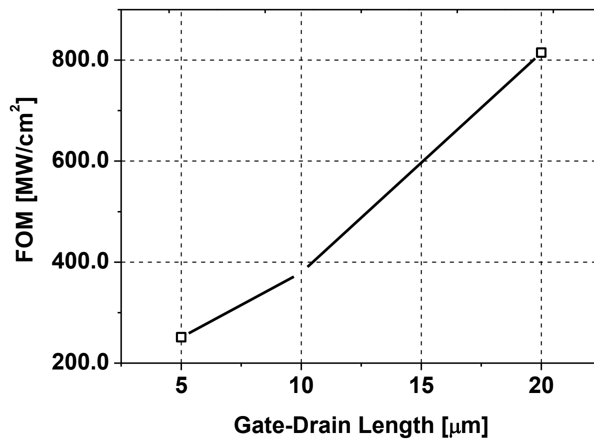

Figure 4.37 Figure of Merit (FOM) of the fabricated AlGaN/GaN MOS-HEMT as a function of the gate-drain spacing (L_{GD}).

4.5 Summary

We have proposed and fabricated the AlGaN/GaN MOS-HEMTs with ALD Al_2O_3 dielectric through passivation-first process. The pre-deposited 10-nm-thick ALD Al_2O_3 gate dielectric acted both passivation layer and gate dielectric for MOS structure. It was found that ALD Al_2O_3 played an important role to achieve the stable blocking capability by protecting device surface from the possible process damages and suppressing the gate leakage current. As a result, Al_2O_3/AlGaN/GaN MOS-HEMTs with L_{GD} of 20 μm exhibited a low gate leakage current of 20.1 pA/mm (1.05 pA) and high the breakdown voltage of 2 kV. In addition, albeit low carrier concentration, the the maximum drain current (539.3 mA/mm) similar to that of the conventional one (535.8 mA/mm), was obtained due to the passivation effect of the Al_2O_3 dielectric. This improvement in forward and reverse operation made the MOS-HEMTs employing ALD Al_2O_3 gate insulator more promising for high power device.

Chapter 5

5. Conclusion.

Gallium Nitride (GaN) based high electron mobility transistor (HEMT) or heterostructure field effect transistor (HFET) are promising device for high-power switches which has to operate in electrically and environmentally harsh condition. The devices benefits from the material properties GaN offers: high critical field, high carrier mobility and a high saturation velocity of carriers.

The breakdown voltage in AlGaN/GaN HEMTs is known to be triggered by gate leakage caused by the concentration of the electrical field at the drain-side edge of the gate electrode. The influence of gate leakage on blocking characteristics is alleviated by reducing the peak intensity of the electric field at the drain–side of the gate. There are two methods to reduce the peak intensity of the electric field: one is to decease the probability of tunneling of electrons into device active area the other is to relieve the crowding of electric field at the drain-side edge of gate.

Nickel has been used as a gate electrode of the AlGaN/GaN HEMTs to form the Schottky contact due to its relatively high work function (5.15 eV). In this work, nickel oxide (NiO_X) was inserted as the interfacial layer

between main gate (Ni) and AlGaN barrier layer for improve the reliability of the AlGaN/GaN HEMTs. NiO_X film was formed through the thermal oxidation in furnace. Material property of NiO_X film depended on the two main factors: oxidation temperature, density of the film controlled by deposition rate. Only the NiO_X film oxidized proper temperature range from 400 ℃ to 500 ℃ gave a favorable effect on the device performance. The NiO_X film with high atomic density exhibited resistive switching characteristics, which can be used for GaN based memory device. Experiment to verify the effect of NiO_X on reverse blocking operation were carried out . At the high temperature reverse bias (HTRB) test, it was found that work function of the NiO_X was maintained. Moreover, it played an important role to improve the stable blocking operation. The result of electro luminescence (EL) analysis was consistent with the results obtained from HTRB test. Leakage current of the AlGaN/GaN HEMTs with NiO_X interfacial layer measured at 200 ℃ was lower than that of the conventional device by 3 orders of magnitude. Breakdown voltage of the proposed device was up to 1.5 kV (1480 V).

In recent years, improvements of the overall device performance were achieved by adopting metal-insulator-semiconductor (MIS) or metal-oxide-semiconductor (MOS) structure. At the gate region, by insulating gate electrode by means of a dielectric layer, electron injection is suppressed effectively. In this work, improvement of the blocking capability and reliability of AlGaN/GaN MIS-HEMTs employing atomic-layer-deposited (ALD) Al_2O_3 dielectric was confirmed by experimental results. Mechanism responsible for the leakage current of the proposed

device was investigated. Measured Leakage current of the fabricated MIS-HEMT was reduced to the range from sub pA (fA) to few pA. At the HTRB test, MIS-HEMT exhibited proved its thermal stability. Although drain leakage current (I_{DSS}) was increased in proportion to the operational temperature, the leakage current of the proposed device remained lower leakage current than that of conventional device by 2 orders of magnitude. Breakdown voltage of the fabricated AlGaN/GaN MOS-HEMT employing ALD Al_2O_3 dielectric was up to 2 kV.

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초 록

최근 들어 고 효율 전력에너지 산업에 대한 관심이 증가됨에 따라 전력 반도체에 대한 관심도 증가하고 있다. 기존 실리콘기반의 전력 반도체는 물성적인 한계로 인해 기술적인 한계에 도달해 있다. 이에 따른 대안으로 우수한 물성을 장점으로 한 Ⅲ−Ⅴ화합물 반도체 물질 특히, 질화갈륨(GaN)을 기반으로 한 전력반도체 소자가 실리콘 전력반도체를 대체할 차세대 반도체 물질로 주목 받고 있다. 질화갈륨 기반의 전력 반도체는 전력의 송배전, 가정용 가전부터 산업용 중장비 및 차세대 전기자동차의 동력계통까지 다양한 분야에 사용되며 점차 그 사용영역이 넓어지고 있으며, 반도체 분야의 선진 연구그룹부터 기존 실리콘 전력반도체 제조업체, 질화갈륨을 이용한 LED 기업까지 질화갈륨 전력 반도체 분야에 대한 활발한 연구가 수행되고 있다.

질화갈륨을 이용한 이종접합구조의 고 이동도 트랜지스터 (AlGaN/GaN HEMT)는 낮은 진성 수송자 생성율에서 비롯한 접합의 열 안정성과 높은 임계 전계를 바탕으로 한 높은 항복전압 그리고 이종접합 계면에 형성되는 고 농도의 전자채널 및 형성 메커니즘에 기인한 높은 전자 이동도 및 전자 포화 속도 등 여러 우수한 물질적 특성을 지니고 있어 낮은 온 저항 및 고속 동작 그리고 안정적인 고온동작 이 구현 가능하여 차세대 전력 반도체 물질로 각광받고 있으며 HEMT 소자를 이용한 전력 반도체 소자에 대한 많은 연구가 이루어지고 있다.

전력용 AlGaN/GaN HEMT 소자는 우수한 대 전류 구동능력과 더불어 낮은 누설전류 및 높은 항복전압으로 대표되는 우수한 역방향 차단특성을

가져야 한다. HEMT 소자의 차단특성을 저하시키는 요인으로는 에피 성장 과정에서 발생하는 수평 수직방향의 각종 결함, 표면 준위에 의한 가상 게이트 효과, 표면누설 전류 그리고 soft breakdown 현상 그리고 드레인 방향 게이트 전극에서의 전계 집중에 의한 누설전류 증가와 역 방향 압전분극 현상까지 다양한 열화 요인이 존재한다.

본 논문은 이러한 여러 요인들에 의한 누설전류를 억제하고 항복전압 특성을 개선하기 위해 다양한 소자의 구조 및 공정방법을 제안하고 제작된 소자들의 전기적 특성을 측정을 통해 제안된 소자의 역방향 차단특성의 향상 여부를 검증하였다.

산화니켈 계면막은 기존 게이트 전극으로 사용되는 니켈을 박막형태로 증착 한 뒤 고온의 산소분위기에서 열 산화 과정을 통해 형성하였으며, 산화니켈 계면막 위로 다시 기존의 니켈전극을 증착하여 산화니켈 계면막이 적용된 소자를 제작한 후, 소자의 전기적 특성이 측정되었다. 소자의 누설전류는 상온에서 수십 μA 에서 수 nA 로 3 order 정도 감소하였다. 산화니켈 계면막에 의한 누설전류의 억제효과는 고온 역 방향 측정 (HTRB test)에서 더 분명하게 나타났다.

기존소자의 게이트 누설전류는 동작온도에 비례하여 증가하여 전체 누설전류(I_{DSS})에서 게이트 누설전류가 차지하는 비율(I_G/I_{DSS})이 상온에서의 값과 유사한 0.80~ 0.85 수준을 나타냈지만 산화니켈 계면막이 적용된 소자의 경우, 200℃에서 측정된 전제누설전류의 값도 수백 nA 로 낮은 수준을 유지하였으며 게이트 누설전류의 비율은 0.15~0.19 정도로 감소하여 기존소자에 비해 상대적으로 매우 안정적인 누설전류 억제효과를 가지고 있음을 확인하였다. 이러한 누설전류의 억제효과는 EL(electro luminescence)를 통해서도 검증할 수 있었다.

측정을 위한 고전압의 역방향 바이어스 인가 시, 기존소자의 경우 전계집중에 의해 게이트전극의 feed 부분이나 드레인 전극의 말단 부위 그리고 소자의 active 영역에서도 EL peak 을 확인할 수 있었지만 산화니켈 계면막이 적용된 소자의 경우 active 영역에서의 EL peak 을 확인할 수 없었다. 이는 산화니켈 계면막이 게이트 누설전류를 효과적으로 억제하고 있음을 나타내는 실험적 근거이다. 산화니켈 계면막에 의한 소자의 차단특성 개선은 항복전압 특성의 개선을 통해서도 확인할 수 있었다. 산화니켈이 제안된 소자의 항복전압은 1.4 kV 로 기존소자에 비해 항복 전압값도 증가하였으며 항복직전까지 누설전류를 억제하는 hard breakdown 현상을 나타내었다. 이러한 위 실험결과를 통해 산화니켈 계면막이 적용된 소자가 전기적으로 그리고 열적으로 안정적인 차단특성을 가지며 이러한 차단특성의 향상에 있어서 산화니켈 계면막이 큰 역할을 하는 것을 여러 실험 결과를 통해 확인할 수 있었다.

AlGaN/GaN HEMT 의 차단특성 개선을 위해 PEALD 방법으로 증착된 Al_2O_3 게이트 절연막이 적용된 MOS 구조의 HEMT 가 제안되었다. ALD 증착 방법은 증착과정에서 발생되는 소자의 표면 손상이 적어 이종접합구조의 2DEG 손상이 적으며, 막의 정확한 두께 조절이 가능하고, 증착 된 막의 특성이 우수한 장점을 갖는다. 본 실험에서는 mesa isolation 직 후 게이트 절연막을 형성하는 pre-passivation 방식을 통해, 추후 공정과정에서 발생할 수 있는 표면손상을 억제하였다. 제작된 MOS-HEMT 소자는 기존소자에 비해 낮은 2DEG 농도를 나타냈지만 게이트 절연막에 의한 표면 passivation 효과로 인해 표면준위의 전하포획이 억제되어 기생 source 저항 및 remote coulomb 산란효과의 감소에 의해 전계 이동도가 증가하여 기존 소자에 비해 채널전자의 농도가 작음에도 불구하고 유사한 전류값을 나타내었다. 또한 pulsed I-V 특성에서는

전류축약 현상 없이 DC 전류 대비 증가된 pulse 전류 값을 나타내었다. (I_{PULSE}/I_{DC}>1) 이는 게이트 절연막에 의한 passivation 이 소자의 순방향 특성을 개선시키는 실험적 근거이다. 역방향 동작에서도 ALD Al_2O_3 가 적용된 MOS-HEMT 는 우수한 차단특성을 나타내었다. 상온에서 측정된 누설 전류값은 수 pA 로 기존소자 대비 6 order 가 감소하였으며 고온 역방향 측정에서도 MOS-HEMT 는 우수한 누설전류 억제효과를 나타내었다. 다양한 누설전류 model 을 통한 MOS-HEMT 의 누설전류 분석결과 MOS-HEMT 는 상온에서 Fowler-Nordheim tunneling 메커니즘에 의한 누설전류가 형성되고 고온 동작에서는 FN tunneling 보다는 Schottky emission (Thermionic Field Emission)에 의해 누설전류가 증가함을 확인하였다. 항복전압 역시 1.9 kV 가 넘는 우수한 항복전압 특성을 획득하였다.

주요어: AlGaN, GaN, 고 이동도 트랜지스터, ALD, 산화니켈, Al_2O3, passivation, 항복전압, 누설전류

학 번: 2010-30214

감사의 글

2007년 연구실에 석사과정으로 입학한 후, 6년이 훌쩍 지나 이제 정들었던 연구실을 떠날 때가 코앞으로 다가왔습니다. 돌이켜 생각해보면 연구실을 처음 방문했을 때의 생경한 모습이 아직도 기억에 생생한데 벌써 졸업을 앞두고 있다는 사실에 새삼 시간이 참 빠르게 지나고 있음을 느낍니다, 지난 석 · 박사 과정을 돌이켜보면 이 기간은 정말 많은 것들을 배우고 느끼며 경험할 수 있는 소중한 시간이었습니다. 연구라는 새로운 분야로의 입문, 선후배들과의 연구실 생활 그리고 선배들로부터의 유익한 조언 이 모든 것들이 연구뿐만 아니라 저 개인적인 성숙을 할 수 있는 밑거름이 되지 않았나 하는 생각을 해봅니다. 졸업을 앞두고 지난 6년간의 결과물들을 정리하는 이 시점에서 저에게 큰 힘이 되어주셨던 주위의 많은 분들에게 이 글을 통하여 감사함을 표하고자 합니다.

먼저 여러모로 부족했던 저를 제자로 받아주시고 항상 저를 자식과 같이 생각하며 이해해주시고 지지해주셨던 한민구 교수님께 깊은 감사와 큰 존경의 마음을 전하고자 합니다. 교수님께서 보여주신 학문에 대한 열정과 예리한 통찰력은 제게 무한한 가르침이자 기반이 되었습니다. 또한 연구 이외에도 주셨던 많은 인생과 처세에 관한 주옥 같은 조언들 역시 앞으로 마음에 깊이 새기고 살아가겠습니다.

부족했던 저의학위 논문을 심사해 주시며 귀중한 조언과 가르침을 주셨던 윤의준 교수님, 이종호 교수님, 김동명 교수님, 김용상 교수님께 진심으로 감사를 드립니다.

6년이라는 긴 시간 동안 저와 함께 연구실 생활을 하면서 많은 즐거움과 힘든 일들을 함께 공유했던 많은 선후배들에게도 고마운 마음을 전하고

자 합니다. 비록 많은 시간을 함께 하지는 못 했지만 입학 후, 연구에 대한 많은 조언과 도움을 주셨던 한상면, 지인환, 신희선, 박중현, 김창연, 이원규, 선배님들께 감사 드리며, 계시는 곳에서 앞으로도 승승장구 하시길 기원하겠습니다. 특히, 연구와 실험 전반에 걸쳐 초석을 다질 수 있도록 많은 도움을 주었던 최영환 선배, 그리고 입학부터 꼼꼼하게 연구실 생활을 챙겨 주었던 동갑내기 규헌, 지용 선배에게 진심으로 감사 드립니다. 그리고 볼 때 마다 늘 따뜻하게 저를 대해 주셨던 상근이형, 조용하지만 카리스마 넘치는 영훈이형, 차도남처럼 보이지만 마음은 따뜻한 선재, 연구실에서 성실함의 표본이었던 성환이 그리고 항상 주변사람들을 유쾌하게 만들어 주는 우철이 형에게도 감사의 말을 전하고자 합니다. 또한 한 학기 선배로 다양한 관심사와 즐거움을 공유했던 다재 다능한 동원이와 매사에 반듯한 승희 언제나 엄청난 학구열을 보여주었던 동기 태준이 형 그리고 매사에 긍적적인 마인드와 특유의 유머로 주변 사람들을 유쾌하게 만들었던 한 학기 후배 정수가 있어서 연구실 생활이 더욱더 즐거웠습니다.

언제나 다정다감하시고 늘 좋은 말씀을 해주셨던 빈이 형 그리고 촌철살인의 말솜씨를 가진 영욱이 형 그리고 운동과 연구 두 분야를 종횡무진 하셨던 승환이 형에게도 감사의 말씀을 전하며 회사에도 뛰어난 재능을 바탕으로 모두 좋은 결과 얻으시길 기원합니다.

그리고 연구실의 궂은 일과 더불어 부족한 선배를 물심양면으로 도와주느라 고생했던 많은 후배님들께도 큰 감사의 마음을 전합니다. 이제 외국에서 학업을 계속 이어나가게 될 오균과 우진에게는 건투를 빌며 그곳에서도 좋은 결실을 이루길 바랍니다. 연구실의 홍일점으로 뛰어난 능력과 겸손함을 겸비한 수연이, 무한한 잠재능력을 가졌지만 안타깝게도 아직 발현되지 않고 있는 선범이 홀로 대전에서 애쓰고 있는 서글서글한 민기에게도 고마운 마음을 전합니다. 싹싹했던 연구실 술 상무 종석이와 연구실 최고 미남 용진이에게는 곧 있을 결혼에 대한 축하의 마음을 전합니다. 회사에

서 휴일도 없이 고생하는 용욱이와 이제 막 회사 생활을 시작한 문규와 승민이는 회사에서도 인정받는 훌륭한 신입사원이 될 것을 믿어 의심치 않습니다. 지금 와서 생각해보면 선배로써 해준 것 없이 받기만 한 것 같아 미안한 마음입니다. 그리고 다양한 연구실의 행정 업무를 오랫동안 담당하며 고생하셨던 유지씨와 지혜씨께도 감사의 말씀을 전합니다..

연구활동을 하면서 여러 도움을 주고 받으며 알게 된 많은 분들께도 감사의 마음을 전합니다. 같이 과제를 하며 알게 된 김형준 교수님 연구실의 정현이형, 창현씨, 도현씨 그리고 바쁜 와중에도 공정에 도움을 주셨던 경북대 김동석씨께 다시 한번 감사 드리며 남은 박사기간 좋은 결과를 얻기를 바랍니다. 그리고 많은 도움 주셨던 나노소자 특화팹센터의 김신근, 이근우 연구원님께도 감사의 마음을 전합니다.

부족한 저를 위해 헌신을 마다하지 않으신 아버지 어머니께 이 자리를 빌어 존경과 깊은 감사의 마음을 전합니다. 두 분께서 주신 사랑과 격려가 제가 지금까지 살아오면서 어려운 일들을 잘 감당해 낼 수 있었던 가장 큰 원동력이라 생각합니다. 이제 3살 1살배기 두 아들과 사투를 벌이면서도 곁에서 못난 신랑을 물심양면으로 내조했던 사랑하는 아내 혜선에게도 감사의 마음을 전하며 더 큰 신뢰와 사랑으로 아끼며 앞으로의 인생을 함께할 것을 약속합니다.

하나뿐인 동생 지영이와 매제 현민이에게는 그간 많이 챙겨주지 못해서 미안하고, 조카 규연 규서는 앞으로 엄마 아빠 말을 잘 듣는 예쁘고 훌륭한 숙녀로 자라길 바랍니다. 또한 멀리서 응원해 주시는 처제와 동서에게 고마운 마음을 전합니다. 그리고 예쁜 조카 윤아는 멋진 가수가 되기를 이모부가 응원합니다. 또한 항상 큰 관심으로 응원해 주시는 장인 장모님께도 깊은 감사 드립니다.

돌이켜보니, 저는 많은 분들로부터 지지와 사랑을 받으며 살아온 것 같습니다. 모든 분들께 다시 한번 감사의 마음을 전합니다. 아직도 많이 부족

한 지식과 인격으로 '학교'라는 울타리를 넘어서서 경쟁과 책임의식이 더욱 요구되는 사회로 나가야 하는 시점이라 두려움이 앞서기도 하지만 앞으로 내딛는 인생의 매 순간순간 최선을 다하며 살아갈 것임을 스스로에게 다짐하며 이 글을 마칩니다.