공학박사학위논문

HA 컨버터를 응용한 AC-DC 및 DC-AC 전력 변환

H-bridge Converter with Additional Switch Legs and its Application to AC-DC and DC-AC Conversions

2013년 2월

서울대학교 대학원

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For the Ascent of Man

Abstract

This dissertation proposes a new topology *H-bridge converter with additional switch legs (HA converter)*. The proposed topology has simple circuit structure with expandability and flexibility. With six semiconductor devices and single inductor, the topology is capable of operating as buck, boost, and buck-boost converter. Theoretically, it demonstrates low common mode current and electromagnetic interference (EMI) by solidly connecting grounds of input and output terminals. The proposed topology is advantageous not only in grid-connected power conversion application but also in stand-alone power system such as electric vehicle, because these systems include large parasitic capacitances and are prone to high common mode EMI due to the wide mechanical structure of the conductor.

Among many offspring circuits of the HA converter, a boost-buck-boost (B3) rectifier for off-line power supply with active power factor correction and a buck-buck-boost (B3) inverter for grid-connected photovoltaic system are proposed as two practical examples. Principle of operations, dedicated control algorithms, and filters for the new circuits are analyzed and designed in detail. Experimental results based on the laboratory prototype hardware prove that the proposed circuits outperform their conventional counterparts by showing low common mode noise and comparable efficiency.

Keywords: H-bridge converter with additional switch legs, electromagnetic interference, common mode noise, B3 power factor correction rectifier, B3 inverter.

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1. Introduction

1.1. Motivations and Backgrounds

Energy shortage and environmental problems are gathering global concerns in these days due to the fossil fuel depletion, energy demand increase, and carbon dioxide emission. Renewable energy sources including photovoltaic (PV) generation are highlighted as a solution to reduce the fossil fuel consumption and greenhouse gas emission, though they require appropriate interface circuits to cooperate with commercial AC distribution system [1]-[5]. As the interface circuits, power converters such as off-line AC-DC rectifiers and grid-connected DC-AC inverters play a key role in maximizing the performance of the renewable energy sources.

Among many requirements of the power converters such as size, weight, cost, and efficiency, electromagnetic compatibility (EMC) is one of the most important performance factors. Mitigating common mode current is critical in converter design because the current causes electromagnetic interference (EMI), system efficiency drops, and human safety issues. Commercial EMI standards from Comite International Special des Perturbations Radioelectrique (CISPR), Verband Deutscher Elektrotechniker (VDE), and Federal Communications Commission (FCC) mandate the power supply manufacturers to minimize the common mode noise level not to pollute the commercial power line and harm other electronic devices [14]-[16]. On the other hand, low EMI may help to reduce the converter size by allowing the use of smaller common mode EMI filters. Generally, EMI filters consist of bulky passive components such as coupled inductors and capacitors, and occupy considerable volume and weight in the power converter. Low common mode noise converters may use smaller filters to reduce the

circuit size and possibly improve efficiency. The reduced filter size also matches to recent trends of decreasing cost of semiconductor switches. Minimizing the number or the size of passive circuit components is therefore becoming more important than decreasing the number of semiconductor devices in circuit design.

Along with the EMC, simple circuit structure is also important for the power converter design. Generally, a circuit with the simple structure and small number of semiconductor switching devices is cost-effective and reliable [57] because the semiconductor devices are costly and fragile. Active switching devices such as metal-oxide-silicon field-effect transistor (MOSFET) and insulated-gate bipolar transistor (IGBT) generally accompany a driving circuit, which consists of additional circuit elements. If the source or the emitter terminal of the switching device is not grounded, i.e., device is floating, the driving circuit becomes more complicated to increase the cost and circuit complexity. Besides the driving circuit, conduction and switching losses of the semiconductor switches degrade the power conversion efficiency. To dissipate the power losses into heat and guarantee the reliable operation, heat sink should be attached to the semiconductor device though it makes the converter heavy and bulky [58]. Therefore, together with the EMC, the simple circuit structure that utilizes small number of switch devices is beneficial to the circuit cost, reliability, and possibly efficiency in the converter design.

1.2. Objectives

This dissertation proposes a set of new converter topologies with low common mode noise and simple circuit structure. By constructing proper topology, the common mode noise of the converter is maintained to be negligibly small, regardless of the control

method or power level of the interface circuit. In the dissertation, a new *H-bridge converter with additional switch legs (HA converter)* is proposed to fulfill the common mode EMI reduction and circuit simplification. The proposed circuit structure eliminates the common mode noise source by connecting the input and output terminal grounds. Providing a solid connection between the input and output grounds shorts the parasitic capacitance and eliminates the possibility of common mode current generation.

The low common mode noise of the HA converter is emphasized in the utility-related applications such as off-line power supplies and grid-connected inverters. Because the common mode noise may travel along the power line and harm the other devices, it is important to suppress the noise in such applications. Several regulations even mandate to halt the circuit operation if the EMI level of the circuit is larger than the defined values [17]-[20]. Additionally, the HA converter is also valuable when it is applied in the stand-alone power systems such as airplanes, ships, and electric vehicles. These stand-alone systems are prone to the conducted EMI because they utilize their metal chassis as the common ground instead of the earth ground. This ground configuration forms considerably large parasitic capacitances due to their material and mechanical characteristics. The HA converter minimizes the effect of the parasitic capacitances on the common mode EMI and reduces the noise.

Two new topology examples are derived from the HA converter and experimented in this dissertation: one is for the off-line power supply with active power factor correction (PFC), and the other is for the grid-connected inverter. The example circuits are created by merging two single-ended DC-DC converters in the HA converter to cope with positive and negative polarities of AC voltage terminal. According to their application,

the example circuits omit unnecessary switches among the six switches of the HA converter to further simplify their structures and improve the efficiencies. By analyzing the example circuits, dedicated control algorithms and filters are designed for practical implementations. Experimental results based on the laboratory prototypes prove that the new circuits derived from the HA converter outperform the conventional ones by demonstrating the low common mode EMI and comparable efficiency.

The HA converter has flexibility and expandability as well as its common mode noise immunity and simple structure. Advocating its flexibility, the HA converter acts as the general topology of the single-ended converters and operates as buck, boost, inverting buck-boost, and non-inverting buck-boost converter according to the application requirement. Various combinations of the DC-DC converters in the HA converter produce another diverse circuits which are applicable to AC-DC and DC-AC power conversion. In addition, the HA converter is capable of bidirectional power delivery due to its bilateral symmetry. By replacing passive switching elements with active ones in the practical implementation, the HA converter can control bidirectional power flow which is required in the system that includes energy storage devices.

1.3. Dissertation Outlines

The dissertation includes five following chapters. Chapter 2 reviews the common mode EMI problem in the typical applications such as off-line AC-DC PFC rectifier and grid-connected PV inverter. The ground connection method is articulated as a solution to the EMI problem. The chapter also illustrates the topological derivation of the HA converter by systematically combining single inductor and two voltage sources. The combination method is useful to derive the new topologies because the switch devices

are arranged with passive circuit elements freely and reasonably. The features of the proposed HA converter such as negligible common mode noise and simple structure are presented.

Chapter 3 derives a practical example of the HA converter for off-line PFC: the boost-buck-boost (B3) rectifier. The B3 rectifier employs two active switches and two passive switches and eliminates four bridge diodes. Comparing with the conventional circuits such as boost rectifier with bridge diodes and bridgeless rectifier [30], the B3 rectifier has simpler structure and lower common mode EMI. The chapter includes operation principles and control strategy of the B3 rectifier. To prove the performance of the newly suggested circuit, the B3 rectifier and a conventional boost rectifier are built and experimented. The common mode noises and efficiencies of the two circuits are measured and compared.

Chapter 4 suggests a grid-connected inverter example of the HA converter: the buck-buck-boost (B3) inverter. The B3 inverter uses four active switches to operate as the grid-connected inverter, which is the smaller number of semiconductors than the conventional circuits such as an HERIC (highly efficient and reliable inverter concept) [33] and an H5 inverter [34]. Operation principles and control strategy of the B3 inverter for single-phase AC grid are explained in this chapter. To compare the performances of the suggested and the conventional inverters, the B3 inverter and an H-bridge inverter with bipolar pulse width modulation (PWM) are built and experimented. The common mode noises and efficiencies are measured and compared, similar with in Chapter 3.

The flexibility of the HA converter is highlighted in Chapter 5. In addition to the aforementioned advantages such as simple structure and low common mode noise, the

versatility of the HA converter comes from the symmetric circuit structure, which is good for flexible operation such as bidirectional power delivery. Also, employing non-inverting buck-boost operation overcomes the limited operating condition of the AC-DC and DC-AC power conversion examples in Chapters 3 and 4.

Conclusion and further works are given in Chapter 6.

2. H-bridge Converter with Additional Switch Legs (HA Converter)

In this chapter, the common mode EMI in grid-connected applications is reviewed. Defining the parasitic capacitance between the converter ground and earth ground as a common mode noise source, a solid connection between the input and output ground terminals is suggested as the solution to eliminate the common mode EMI. The chapter also demonstrates a circuit element combination method to derive new topologies. By utilizing the combination method and ground connection concept, the HA converter is derived.

2.1. Review of Common Mode EMI

Noise emission in electronic circuits is categorized into two: the one is conducted emission and the other is radiated emission. The *conducted emission* is a term for radio frequency current (150 kHz to 30 MHz as defined in CISPR 22 regulation [14]) that flows through one or more conductors in electric circuit. Alternatively, it also indicates radio frequency voltage between conductors. The conducted emission is namely confined in the conductors of the circuit. The *radiated emission*, on the other hand, is a term for electromagnetic field released from the circuit. Being different from the conducted noise, the energy of the electromagnetic field can affect the other electronic devices which are not wired to the source circuit.

Though the definitions of the two terms look different from each other and tend to be considered as two separated concepts, the objective of conducted emission requirements are in fact the same with the radiation emission requirements [22]. For example of the commercial AC distribution line, a small radio frequency current in the circuit, which is

the object of the conducted emission regulations, generally causes negligible radiated emission because the size of the source circuit is not large enough to generate the electromagnetic field in the radio frequency bandwidth. However, the current may travel along the power distribution line and make it into an effective antenna, i.e., the source of radiated emission. Therefore, the conducted emission regulation is to limit both the conducted and radiated noise in the distribution system.

The common mode noise is generated by two things: the parasitic capacitances connected between the circuit and earth ground and the high-frequency voltage applied to them which is mainly due to the fast switching operation of the semiconductor devices. A circuit diagram to explain the generation and measurement of the common mode EMI is shown in Fig. 2.1. The shaded box can be any kind of the interface circuit including AC-DC rectifier and DC-AC inverter, and C_{cm} indicates the parasitic capacitance between the circuit and earth ground. Though there exist multiple parasitic capacitances in the practical implementation, Fig. 2.1 illustrates single capacitor for simplicity. A line impedance stabilization network (LISN) is inserted between the

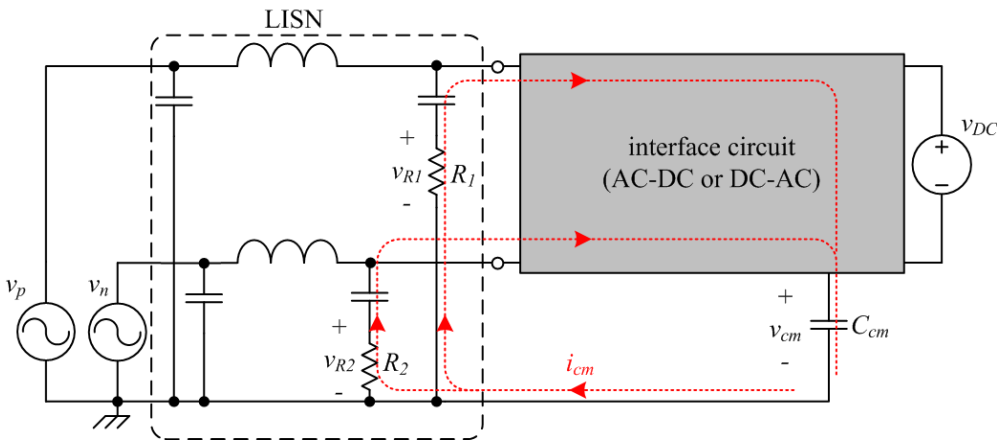


Fig. 2.1. Generation and measurement of the common mode EMI.

rectifier (or the inverter) and AC line. The common mode current i_{cm} is generated by the fluctuating voltage v_{cm} applied to C_{cm}. i_{cm} flows through phase and neutral paths according to the arrows shown in Fig. 2.1. The direction of the arrows does not mean much because the polarity of i_{cm} keeps alternating according to the fluctuation of v_{cm}. i_{cm}, in turn, generates the voltages across the resistors in the LISN. If the divided currents experience same impedance in the interface circuit, i_{cm}, v_{R1}, and v_{R2} in Fig. 2.1 are in the relationships as shown in (2.1),

$$i_{cm} = \frac{1}{2}\frac{v_{R1} + v_{R2}}{48}, \tag{2.1}$$

where 48 is the equivalent resistance of the LISN resistors R_1 and R_2, and v_{R1} and v_{R2} are voltages across R_1 and R_2 respectively. According to the CISPR regulations, v_{R1} and v_{R2} in the specified frequency range should be below the limits defined in [14]. An equivalent circuit of Fig. 2.1 in the radio frequency bandwidth is shown in Fig. 2.2. The parasitic capacitance C_{cm} is represented by the current source, and the inductors and capacitors in LISN are considered as open and short circuits. It is obvious that i_{cm} should be reduced to mitigate the voltages v_{R1} and v_{R2}.

Considering the basic relationship between the i_{cm} and v_{cm} as in (2.2), two solutions exist to mitigate the common mode EMI: the one is to reduce the capacitance C_{cm}, and the other is to decrease the high frequency fluctuation of v_{cm}.

$$i_{cm} = C_{cm}\frac{dv_{cm}}{dt} \tag{2.2}$$

Unfortunately, C_{cm} is hard to be fully eliminated because it is determined by circuit implementation such as wiring between the AC line and interface circuit and traces of printed circuit board (PCB) of the interface circuit. On the other hand, v_{cm} can be

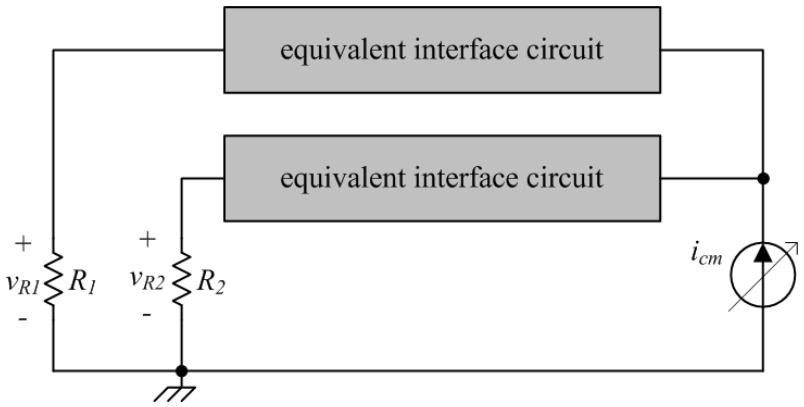


Fig. 2.2. Equivalent circuit of Fig. 2.1 in the radio frequency bandwidth.

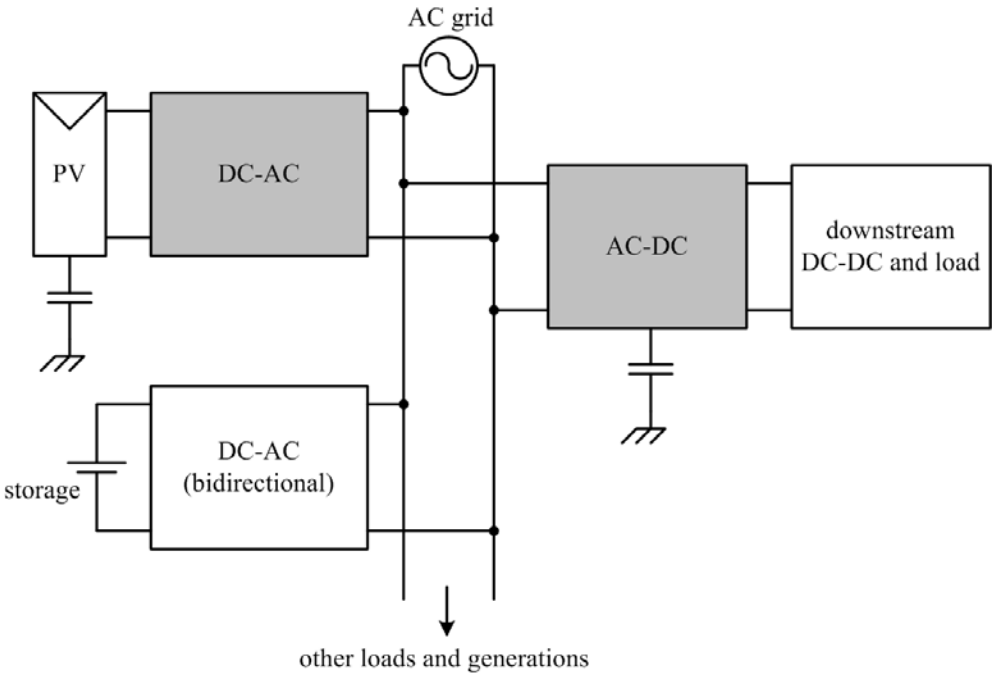


Fig. 2.3.Typical AC distribution system.

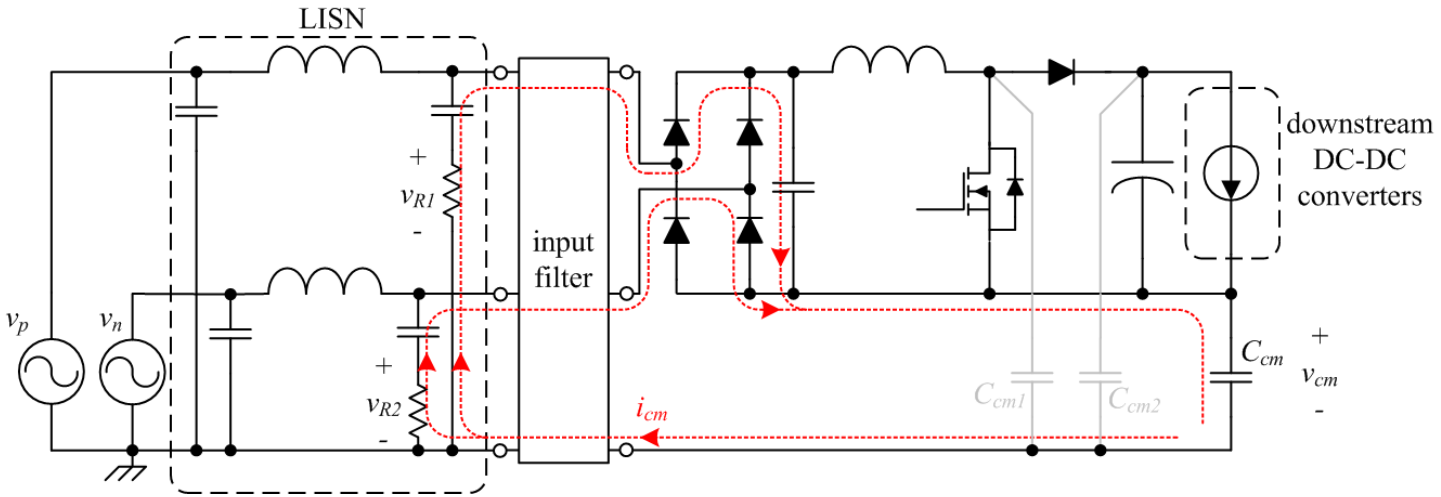
controlled to contain low or zero high-frequency component for common mode noise suppression by designing proper rectifier/inverter topology.

In the typical AC distribution system in Fig. 2.3, various kinds of interface circuits such as AC-DC rectifiers and DC-AC inverters are employed to interface the AC utility line to the DC renewable energy sources and DC loads. In the rest of Section 2.1, two representative power conversion applications are articulated in detail to revisit the common mode current problem: off-line AC-DC rectifier for DC load and grid-connected DC-AC inverter for PV panel. And by considering what the two applications have in common, origin and solution to the common mode noise problem are identified.

2.1.1. In Off-line AC-DC Rectifier

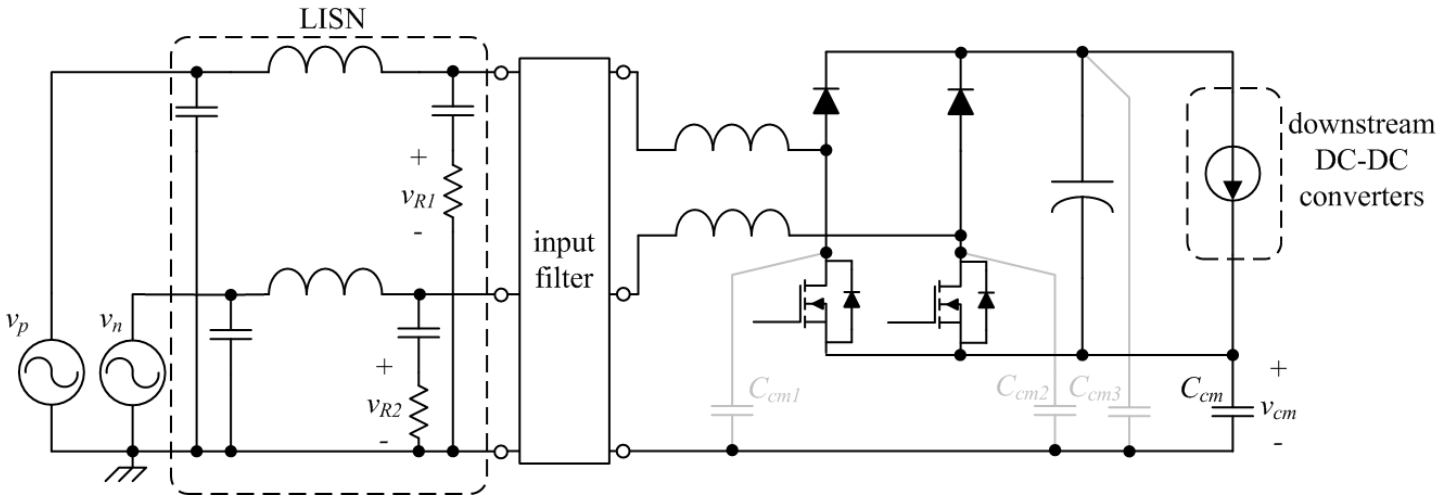
In AC-DC power conversion, distorted AC line current from non-resistive load causes problems such as power loss, noise, line voltage distortion, and reduced line utilization [59]. Regulations on harmonic current limit such as IEC61000-3-2 [21] and the internal specifications of many electronic equipment manufacturers are generally considered to alleviate these problems. An active PFC front-end rectifier with its input filter is a typical solution to minimize the harmonic components of line current and meeting the regulations.

Fig. 2.4 shows two typical boost PFC rectifier examples connected to commercial single-phase AC line through LISN. The capacitance C_{cm} is not the implemented element but the parasitic one that resides between the rectifier ground and earth ground. Other parasitic capacitances such as C_{cm1}, C_{cm2}, and C_{cm3} drawn by grey line are mainly due to the structure and connection of the heat sink for semiconductor devices. Typically, discrete MOSFET and diode have the component package named as transistor outline



(a)

Fig. 2.4. Typical boost PFC rectifiers connected to commercial single-phase AC line. (a) Boost rectifier with input bridge diodes.



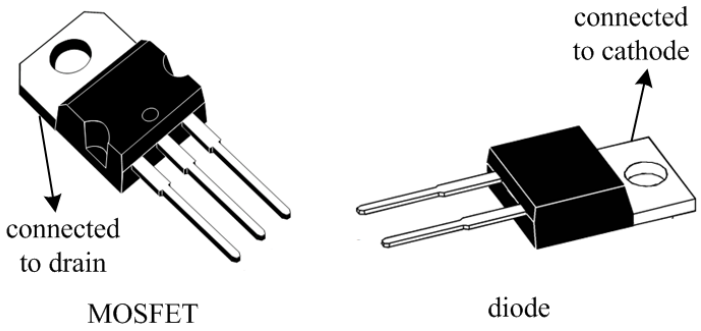
(b)

Fig. 2.4. (Cont'd) (b) Bridgeless dual-boost rectifier.

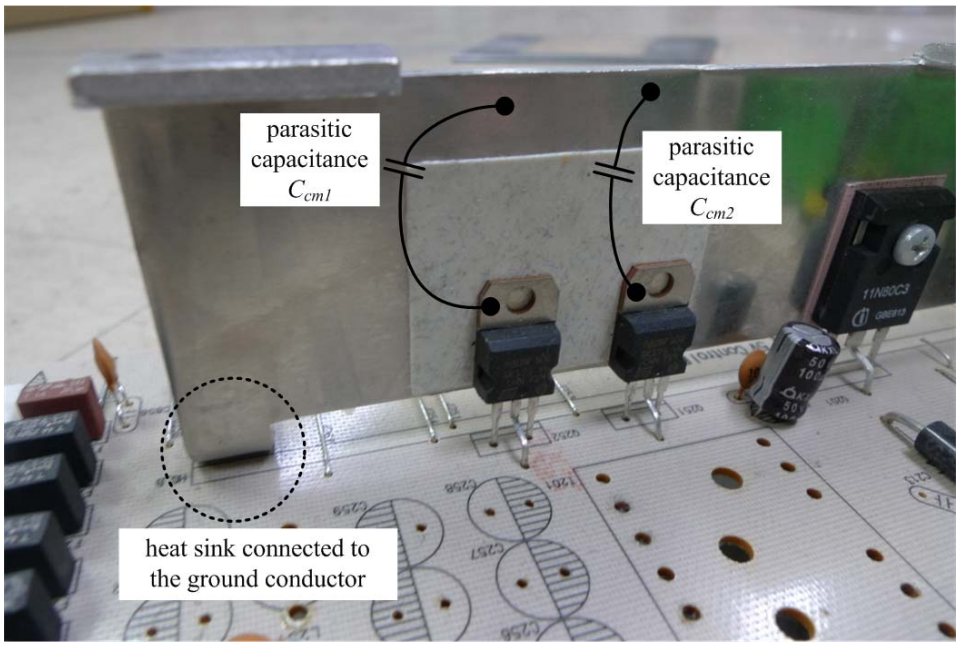
(TO), such as TO-220, TO-247, and TO-258. These packages have metal tabs used in mounting the device to the heat sink or PCB. The metal tab is electrically connected to drain (MOSFET) or cathode (diode) as shown in Fig. 2.5(a), and the heat sinks are generally connected to the earth ground conductor of PCB to avoid electric shock hazard. This configuration produces the parasitic capacitances such as C_{cm1} and C_{cm2} in Fig. 2.5(b).

In the case that the PFC rectifier is a bridgeless one shown in Fig. 2.4(b) for improved efficiency, the common mode noise problem induced by C_{cm} becomes much severer. In the rectifier with the bridge diodes as shown in Fig. 2.4(a), the ground conductor of the rectifier is always connected to the AC line through one of the bridge diodes, and therefore the voltage v_{cm} contains only a line frequency component. However, in the bridgeless dual-boost rectifier in Fig. 2.4(b), connection between the rectifier ground and earth ground is intervened by high-frequency switching devices. The intervened ground applies high frequency voltage to C_{cm} and causes significant common mode current in the bridgeless rectifier [23], [31], [32]. Specific experimental results of the rectifiers are presented in Chapter 3.

Various EMI mitigation schemes have been presented and are well classified and summarized in [23]. Among them, EMI reduction techniques related to the heat sink are presented in [22] and [24]-[26]. Ott [22] suggests that the heat sink is not connected to the earth ground to eliminate the parasitic capacitance, though it issues safety problem. In this case, the heat sink should be protected from being touched by users to avoid electric shock. Xin *et al*. [24] adds an anti-phase winding between the heat sink and converter ground to generate current with same magnitude but opposite polarity with the



(a)



(b)

Fig. 2.5. (a) Metal tabs of TO packages and (b) parasitic capacitances in the PCB implementation of TO packages.

common mode current to reduce EMI. This method does not require additional magnetic component, but its performance is sensitive to the leakage inductance of the main boost inductor. Knurek [25] inserts a shield layer between the MOSFET package and heat sink to reduce the capacitance between them, while the shield layer degrades the heat conductivity and increases the circuit cost. Sinclair [26] proposes to connect the heat sink to the earth ground through a resistor to reduce the common mode current.

In comparison with treating the heat sink, some researches change the topology of the rectifier to reduce the common mode EMI. Shoyama [27] makes the boost converter symmetric by splitting the boost inductance into two and employing an additional output diode. This technique confines the common mode current inside the converter circuit while it requires additional inductor and diode. For forward converter case, Knurek [25] suggests to change the location of the MOSFET and diode to remove the high-frequency component from the voltage across the parasitic capacitances. Though it does not need additional power components, gate drivers for floating MOSFET are required. An impedance balancing techniques for motor drive system and bridgeless PFC rectifier are reported in [28]-[29] using the concept of Wheatstone bridge.

The aforementioned references mainly focus on the heat sink-oriented capacitances such as C_{cm1}, C_{cm2}, and C_{cm3} in Fig. 2.4, which are not connected to the ground conductor of the converter. Research to reduce of the noise generated by C_{cm}, the capacitance between the earth and the converter ground, is relatively few in literature and generally relies on EMI filters.

2.1.2. In Grid-connected DC-AC PV Inverter

Another location in the AC distribution system in Fig. 2.3 where the common mode

EMI becomes an issue is the PV inverter (also referred as PV power conditioning system). PV inverter injects sinusoidal current which is synchronized to the AC line terminal from the PV panel. If a transformerless topology is employed for smaller size and higher efficiency [35], a capacitance that resides between the PV panel and earth ground affects the common mode current. Circuit diagram in Fig. 2.6 shows the location of the parasitic capacitance in the PV panel, interface inverter, and single-phase AC line. The parasitic capacitance C_{cm} in the grid-connected PV inverter is significantly larger than the other interface circuits due to the mechanical structure of the PV panel such as a wide plate in conjunction with the grounded metal casing [6]. Typical value of the capacitance is known to be approximately 10 nF/kW, while it depends on construction or weather conditions [7].

Additionally, it should be noted that the effect of the parasitic capacitance on the common mode noise is even substantial in the power systems for airplanes, ships, and electric vehicles by the similar reason with the PV panel. These stand-alone systems utilize their metal chassis as the common ground instead of the earth ground, which form considerable parasitic capacitances due to their material characteristic and mechanical structure.

For basic DC-AC inverter topology, full-bridge or H-bridge inverter has been widely used since 1960's thanks to its high power capability and versatility. Fig. 2.7 shows the basic H-bridge inverter which interfaces the PV panel and AC line. The H-bridge inverter consists of two switch legs, leg A and leg B, and the line filter. There exist several PWM methods for the H-bridge inverter such as unipolar, bipolar, and hybrid modulation [60]. Fig. 2.8(a) compares the v_{ab} waveforms of the unipolar and bipolar

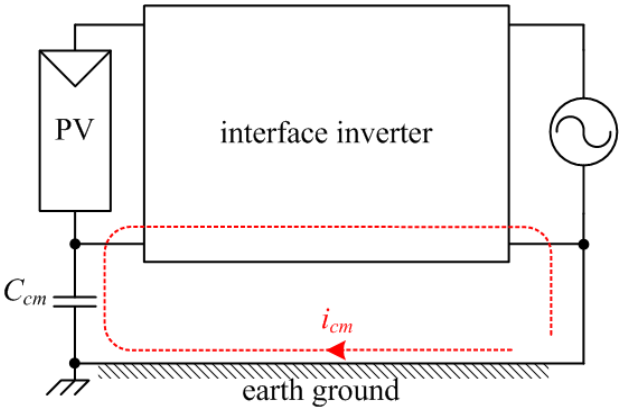


Fig. 2.6. Location of the parasitic capacitance in PV panel implementation.

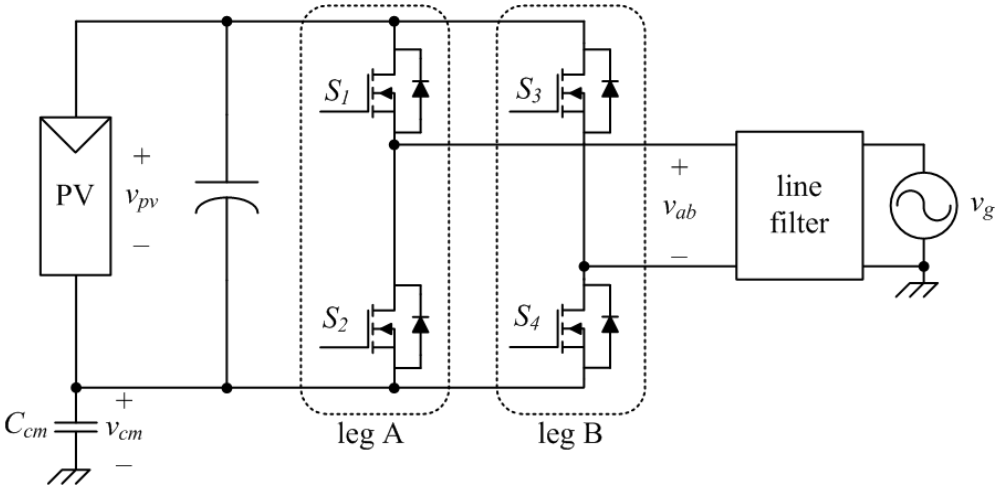


Fig. 2.7. Basic H-bridge inverter interfaces the PV panel and single-phase AC line.

modulation methods with the same switching frequency. The switching frequency is exaggerated with respect to the line frequency for clarity in Fig. 2.8(a). The unipolar PWM generates three-level v_{ab} as the input voltage of the line filter. The fundamental frequency of v_{ab} in unipolar modulated inverter is twice the semiconductor switching frequency. Therefore, the unipolar modulation requires a half of the switching frequency comparing with the bipolar counterpart assuming the same line filter characteristic. On the other hand, the bipolar PWM technique produces a two-level v_{ab}. Fundamental frequency of v_{ab} in bipolar PWM is the same with the semiconductor switching frequency. It is generally known that the unipolar PWM method achieves higher

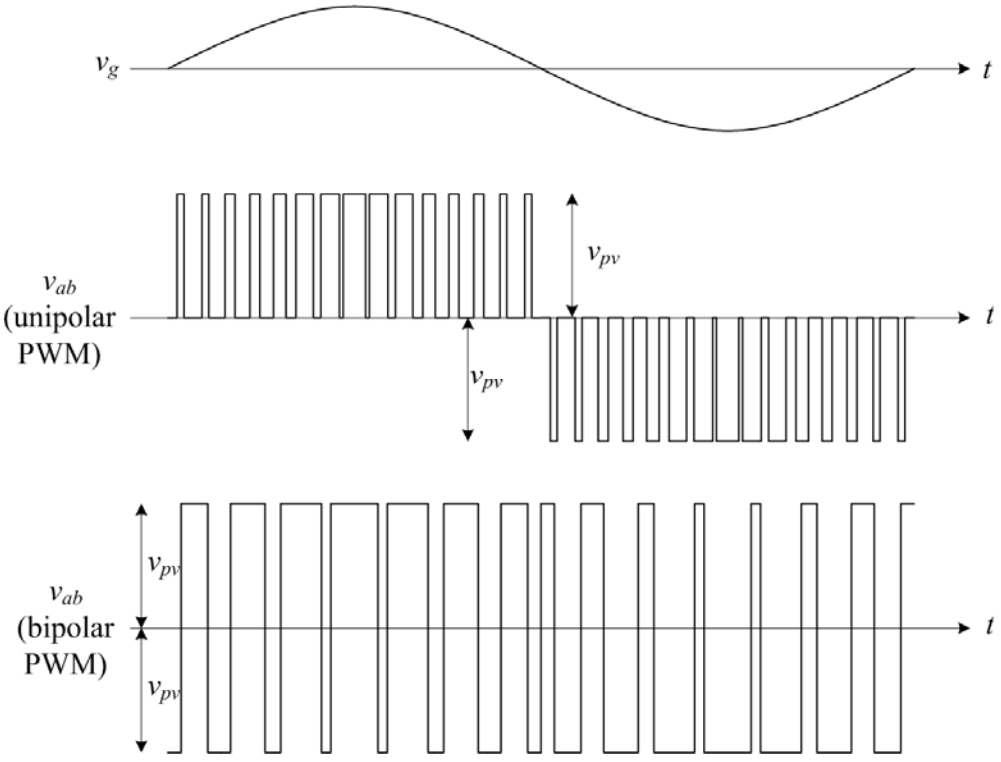


Fig. 2.8. (a) Comparison of v_{ab} waveforms between unipolar and bipolar modulation methods in H-bridge inverter.

efficiency than the bipolar one because the method features lower switching loss in semiconductors and core loss in the line filter.

However, large common mode current is the major drawback of the unipolar PWM method, while the bipolar method features relatively small common mode current [36]. Figs. 2.8(b) and 2.8(c) compare the simulated waveforms when the two modulation methods are applied to the same inverter which outputs 1 kW to 230 Vac line. Switching frequencies of the inverter are selected to be 15 kHz and 30 kHz for the unipolar and bipolar method respectively to apply the same fundamental frequency to the line filter.

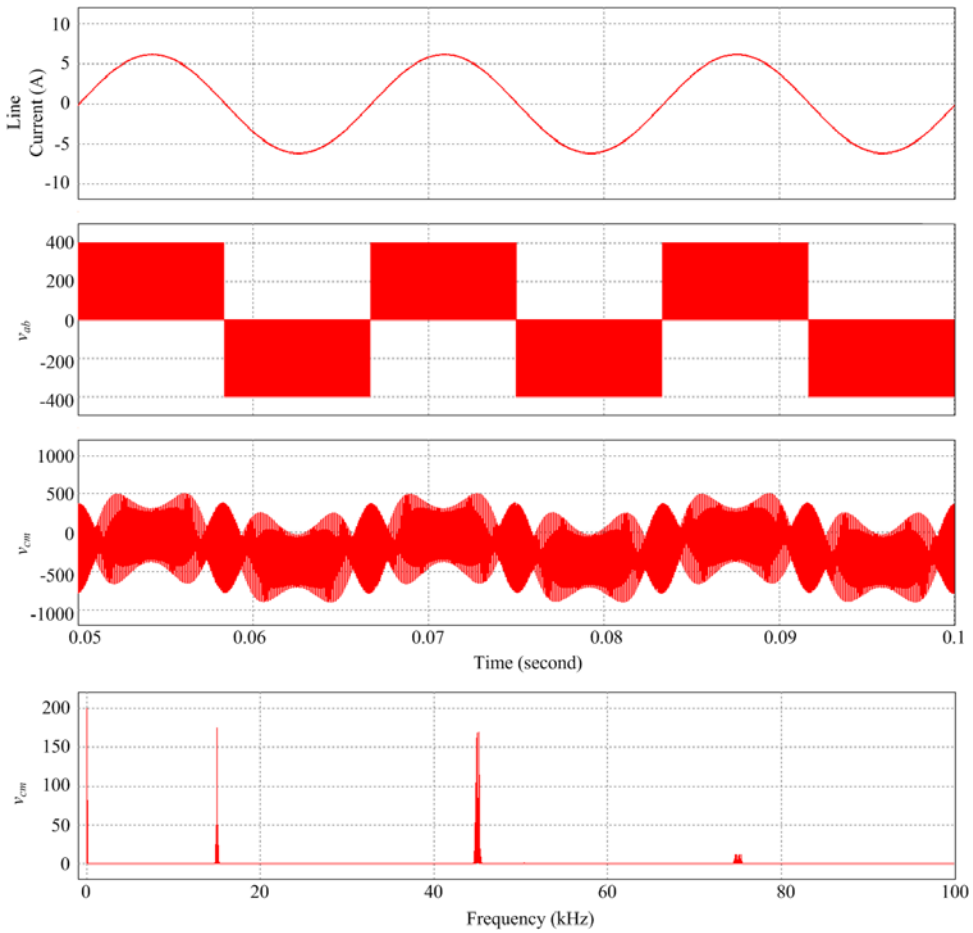


Fig. 2.8. (Cont.) (b) Simulated waveform of H-bridge inverter with unipolar PWM.

According to the time- and frequency-domain waveforms of the parasitic capacitance voltage v_{cm}, the switching frequency component is much larger than the line frequency component in the unipolar case (Fig. 2.8(b)), which in turn generates considerable common mode current. In the bipolar case (Fig. 2.8(c)), on the contrary, the line frequency component is dominant and the common mode current is negligible. Though the line frequency voltage across the C_{cm} also generates non-zero common mode current, the magnitude of the current stays in the acceptable level in the bipolar modulation.

Various topologies for the common mode current mitigation while maintaining

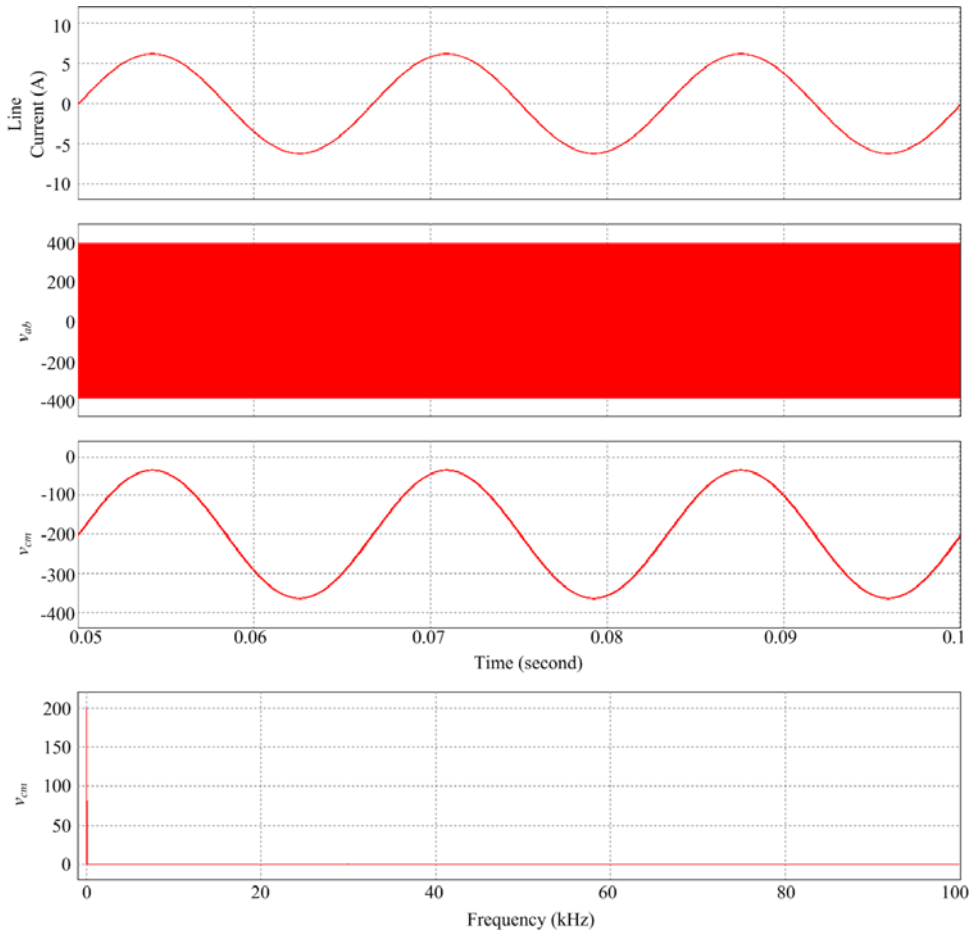


Fig. 2.8. (Cont.) (c) Simulated waveform of H-bridge inverter with bipolar PWM.

three-level v_{ab} waveform such as unipolar modulated H-bridge inverter are summarized in [36]. H5 (Fig. 2.9) [34], H6 [37], and HERIC (Fig. 2.10) [33] inverters employ one or two additional semiconductor devices to disconnect the common mode current source from the AC utility line. Operations of the H5 and HERIC inverter are explained in Appendix A.4. Though they operate with hybrid and unipolar PWM to lower the core loss without generating common mode current, extra conduction loss in the additional switch devices may deteriorate the inverter efficiency. REFU inverter [38] utilizes a unidirectional half-bridge circuit and additional DC-DC converters to mitigate the common mode current. Though it features relatively high efficiency and low common mode noise, its circuit structure and control are complicated. On the other hand, the flying inductor circuit [39] presents common mode current mitigation method based on the connected ground concept. By utilizing five switches and two diodes, the topology also shows a decreased common mode EMI. Among the aforementioned inverters with low common mode EMI, the bipolar modulated H-bridge inverter is selected as the conventional counterpart in this dissertation and compared with the newly proposed inverter in Chapter 4.

To conclude, the common mode noise originates from the fact that the voltage levels of the input and output terminal with respect to the earth ground are not always same to each other, whether it is generated in off-line AC-DC rectifier or in grid-connected DC-AC inverter. If the voltage across C_{cm} is fixed, the common mode current and EMI will be zero theoretically. Even if the voltage across C_{cm} is not fixed but contains low-frequency components only, the common mode EMI will still stay in the acceptable level. However, if the voltage has the high-frequency component such as switching

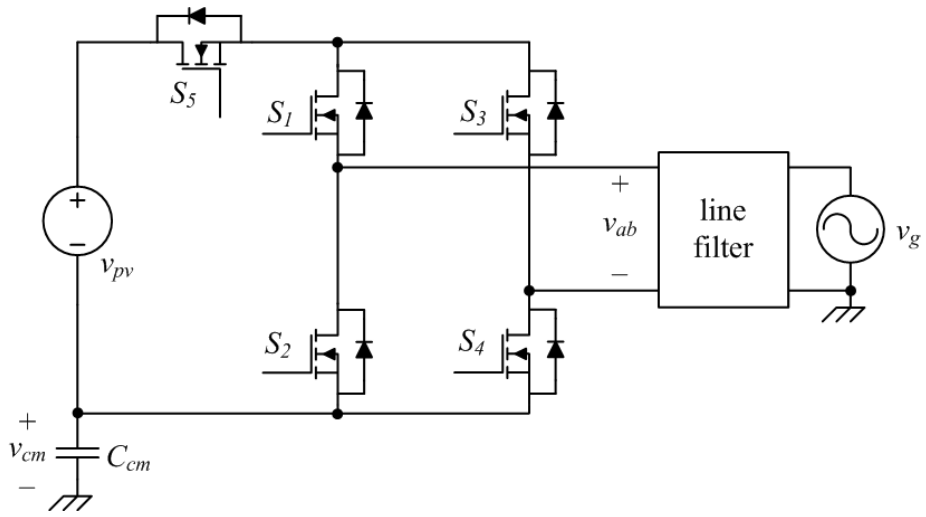


Fig. 2.9. H5 inverter [34].

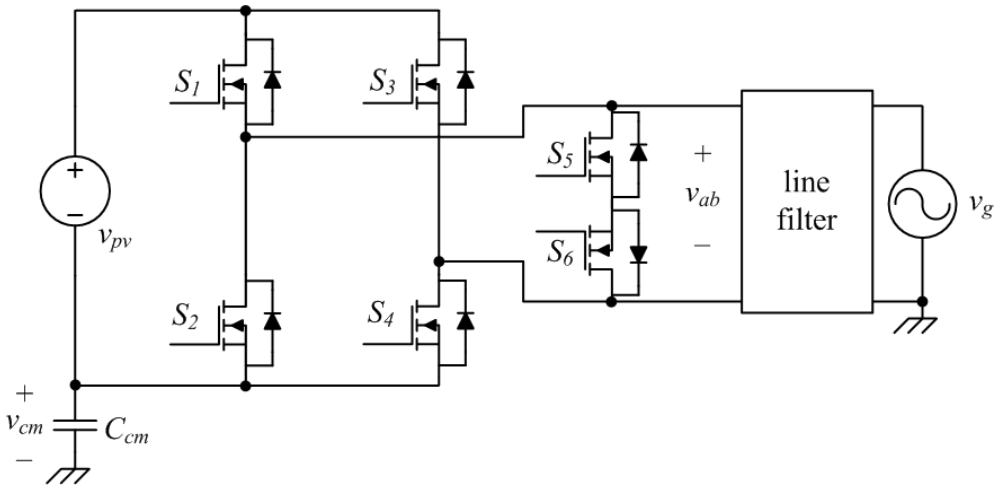


Fig. 2.10. HERIC inverter [33].

frequency and its harmonics, it will generate considerable common mode current. Therefore, making the voltage level of C_{cm} always same by providing solid connection between the input and output grounds reduces the common mode current and consequently the common mode EMI dramatically in the interface circuit.

In addition to meeting the EMI regulations, the reduced common mode noise results additional advantages in the practical circuit implementation by enabling the use of smaller filters. Line filters such as in Figs. 2.4, 2.7, 2.9, and 2.10 occupy considerable weight and volume when implemented, because they generally consist of bulky passive components such as coupled inductors and capacitors to separate differential and common mode noises from the AC line. If the common mode noise is reduced by selecting proper topology that contains connected grounds, the corner frequency of the line filter can be increased, which in turn decreases the filter inductance and filter size. Furthermore, decreased filter inductor in the line filter may help increase the efficiency of the power circuit. Though there are subtle differences between the core materials and manufacturers, inductor core loss is the strong function of the core weight and volume [65]. Therefore, using lighter and smaller magnetic element in the filter may induce smaller core loss and higher system efficiency.

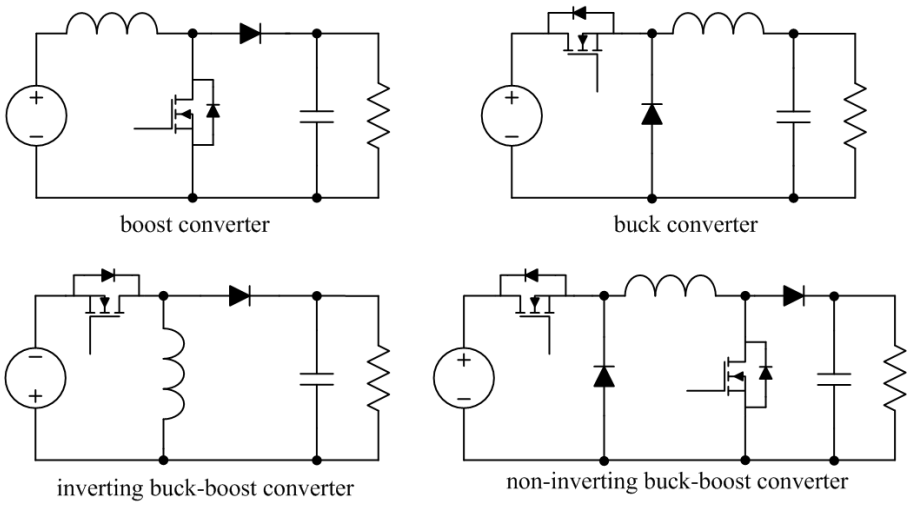
2.2. Topology Derivation

A systematic combination of the circuit elements to derive a new topology is suggested in this section. Conventionally, a majority of the new topology derivation or circuit refinement is fulfilled by changing a small part of the traditional circuits or adding extra circuits to them, which gives less insight to the new topology creation. The proposed combination method is powerful because it totally rearranges the circuit

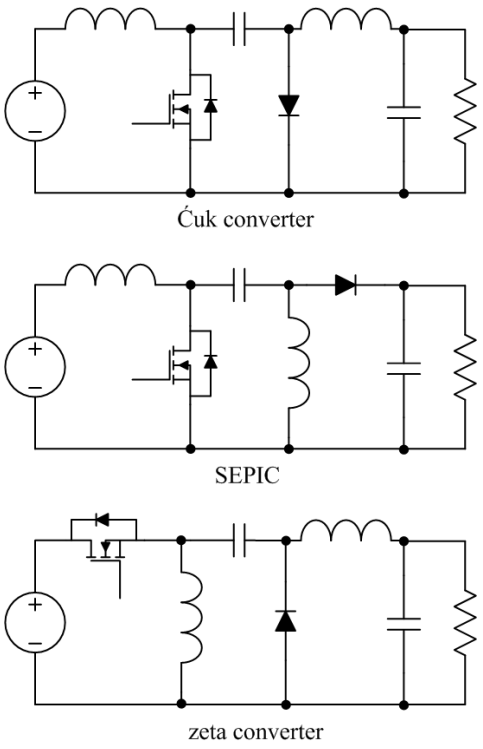
elements and finds new topologies, focusing on the basics of the topology – connection between the elements.

Before deriving new topology, single-ended DC-DC converters are classified according to the number of their energy storage elements because starting from the small number of energy storage elements simplifies the new topology derivation. In this dissertation, general single-ended DC-DC converters are classified into two groups. Neglecting the output capacitor which is common in all DC-DC converters, the converters in the first group contain single inductor as energy storage element, and the ones in the second group have one capacitor and two inductors. To be specific, buck, boost, inverting buck-boost, and non-inverting buck-boost converters belong to the first group because they use only one inductor as shown in Fig. 2.11(a). Ćuk converter, SEPIC (single-ended primary-inductance converter), and zeta converter in the second group use two inductors and a capacitor as their energy storage elements as in Fig. 2.11(b). The capacitor in these converters lies in the series conduction path and should have low equivalent series resistance (ESR) to be robust to high root-mean-square (rms) current for efficiency and reliability. Comparing the two groups, the first group converters have relatively simpler structure than the second group converters because utilization of single inductor downsizes the circuit volume and weight to minimize the number of bulky magnetic energy storage devices.

To build the new topology for simple structure and low common mode noise, circuit elements are combined in systematic way. Prior to make combinations, a couple of assumptions are considered to make the combination process straightforward and remove the possibility of resulting in low performance topology. First, only an inductor



(a)



(b)

Fig. 2.11. Classification of single-ended DC-DC converters: (a) the first group with single inductor and (b) the second group with two inductors and a capacitor.

is considered as the energy storage element and the use of capacitors is not allowed except the output capacitor, which is same with the first group converters with relatively simpler structure. And because the output capacitor is always shunted to the output terminal as in all converters in Fig. 2.11 and its voltage is regulated by controller, the output capacitor is considered as not a capacitor itself but a voltage source in the circuit element combination. Second, all the circuit elements used in the topology are two-terminal elements. Along with the passive circuit elements such as inductor or capacitor, the semiconductor devices developed so far are basically two-terminal elements, considering that the gate terminals of MOSFETs and IGBTs are not the power flow path. The semiconductor switches are to control the connectivity of the two different terminals. It is therefore obvious to assume that the circuit elements are all two-terminal components. The two assumptions make the combination and derivation process simple and straightforward.

A circuit diagram shown in Fig. 2.12 shows the three two-terminal circuit elements: an inductor and two voltage sources with stretched wires to systematically combine them. The voltage sources v_1 and v_2 can be DC or AC, and can also be power source or power sink, according to the application and switch operation.

An *intersection* in Fig. 2.13(a) is defined as the overlap of two wires in this dissertation. It is different from junction or jump of the wires as shown in Figs. 2.13(b) and 2.13(c). The *junction* indicates that the two wires are shorted together and always in same voltage potential, and the *jump* means the wires are not connected. The intersection should become a junction or jump according to the application, which will be explained later in this section. To simplify the combination, only an intersection with

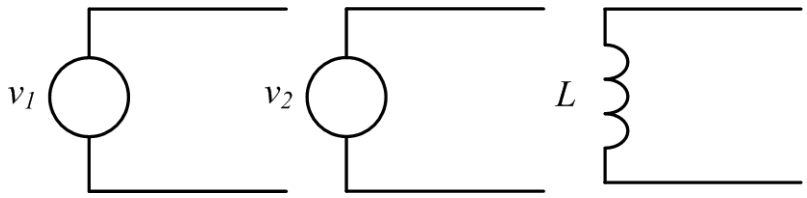


Fig. 2.12. Three two-terminal elements with extended wires for topology derivation.

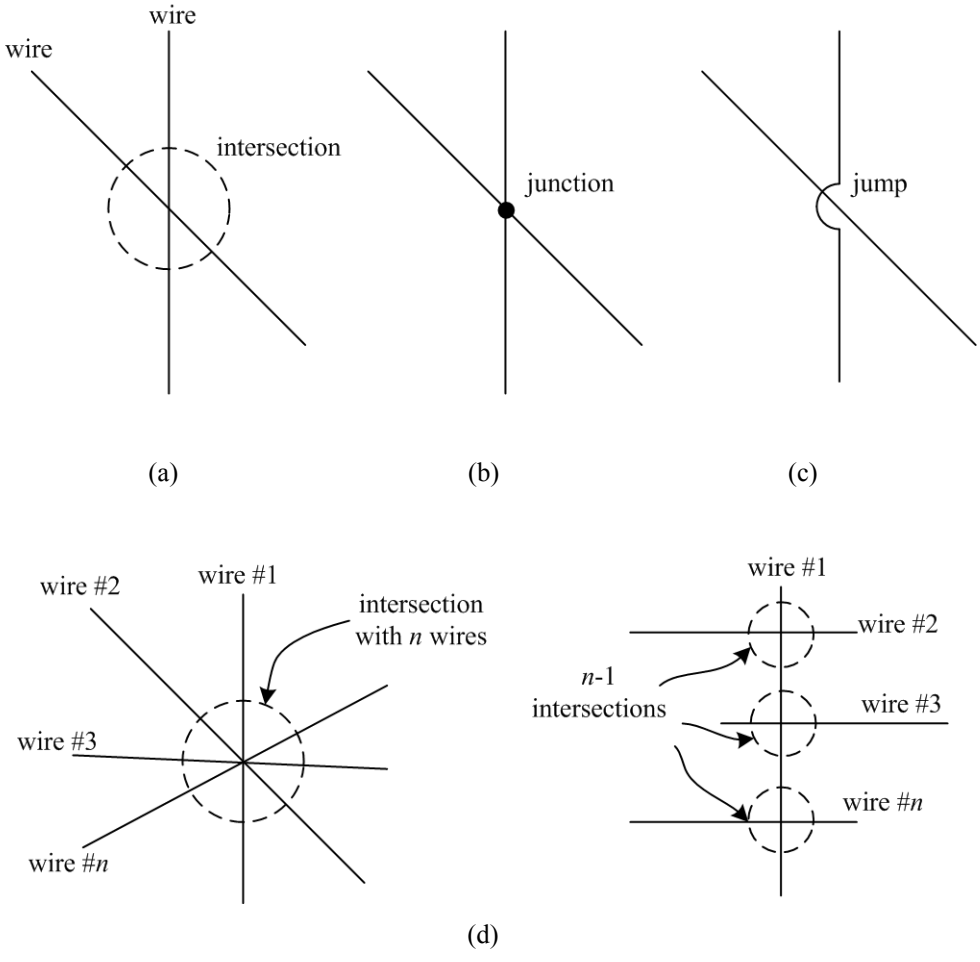


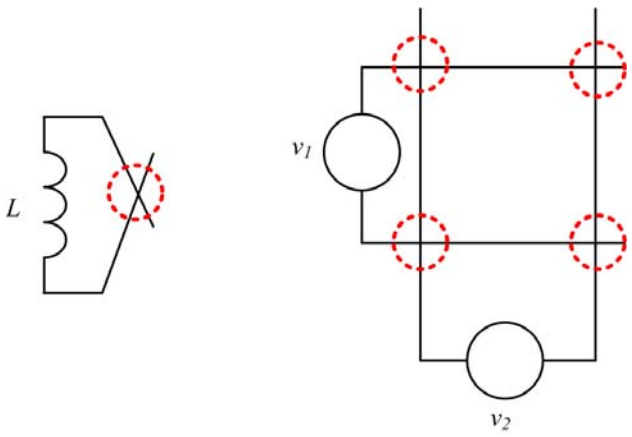
Fig. 2.13. Definitions of (a) intersection, (b) junction, and (c) jump. (d) Split of intersection with n wires into n-1 intersections.

two wires is considered. The intersection that joins more than two wires is not allowed in the combination because they can be divided into the equivalent multiple intersections with two wires. Fig. 2.13(d) shows that an intersection with n wires is disassembled into $n-1$ intersections with two wires.

Some intersections are prohibited to neglect the meaningless and faulty combination in the electric circuit. Fig. 2.14 shows such intersections as shorting the element itself and directly connecting the two voltage sources. These intersections should not be shorted or connected by a switch but should be left open only, and avoided in the elements combination. Intersections in Fig. 2.14(a) are meaningless because shorting the inductor does not have significant meaning. Any selection of the two intersections from the four in Fig. 2.14(b) is also prohibited because shorting a voltage source and directly connecting two different voltage sources are not allowed in the circuit theory.

2.2.1. Dual H-bridges

The intersection is treated in three ways: it can be left open (like the jump in Fig.



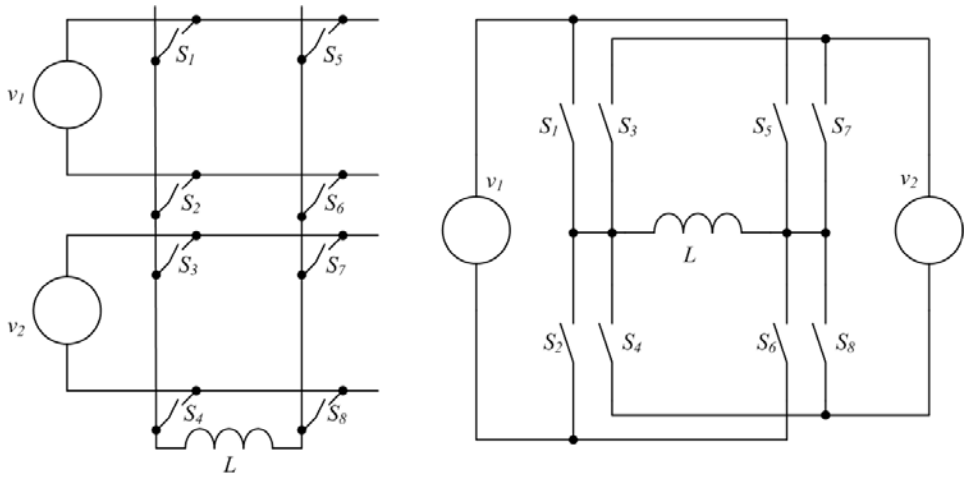
(a) (b)

Fig. 2.14. Prohibited wire combinations of two-terminal elements: (a) shorting the inductor and (b) direct connection of the voltages sources.

2.13(c)), or connected by an ideal switch, or shorted to each other (like the junction in Fig. 2.13(b)). Theoretically, the most general topology that contains the two voltage sources and an inductor occurs by arranging the three two-terminal elements as shown in Fig. 2.15. The maximum number of intersections is calculated by considering the binomial coefficients as expressed in (2.3).

$$ {}_6C_2 - \left({}_2C_2 + {}_4C_2 \right) = \frac{6!}{2!(6-2)!} - (1+6) = 8 \tag{2.3} $$

In (2.3), the terms in the parentheses are the number of prohibited intersections. The term ${}_2C_2$ represents shorting the inductor as in Fig. 2.14(a), and ${}_4C_2$ indicates the cases of prohibited voltage source connections in Fig. 2.14(b). Subtracting the number of these prohibited cases from the cases of selecting two wires from total six wires, ${}_6C_2$, maximum eight intersections are achieved. If all the eight intersections are connected with ideal switches as in Fig. 2.15(a), the topology can be redrawn as in Fig. 2.15(b),



(a) (b)

Fig. 2.15 (a) Eight-switch topology by systematic combination. (b) Two H-bridges with a single inductor which is the most generalized topology.

resulting in dual H-bridges in conjunction with each voltage source.

The dual H-bridges in Fig. 2.15(b) obtain maximum versatility by employing the maximum number of switches. It can emulate not only buck, boost, inverting buck-boost, and non-inverting buck-boost converters but also inverting buck and inverting boost converter which cannot be realized by single-ended topology. However, the circuit in Fig. 2.15(b) may not be practical because it contains many switch devices those are not required in the practical application. Also, the circuit is not good for reduced common mode noise either due to the intervened grounds of the two voltage sources. The effect of the grounds intervened by the fast switching elements are explained in Section 2.1 that revisits the concept of the common mode EMI.

2.2.2. HA Converter

In this section, the HA converter is derived by employing both concepts: the connected grounds and systematic element combination. The HA converter therefore achieves the low common mode EMI and simple and flexible structure.

As concluded in Section 2.1, it is important to provide fixed or at least low-

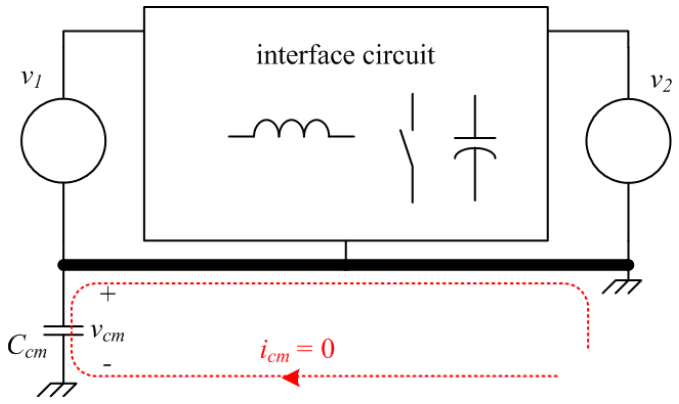


Fig. 2.16. Fundamental idea of HA converter that connects the grounds of input and output terminals.

frequency voltage to the parasitic capacitance to reduce the common mode current. If the two voltage sources v_1 and v_2 in Fig. 2.12 have their grounds always connected, the common mode current and common mode EMI will be reduced dramatically. Fig. 2.16 shows the fundamental idea of the HA converter which is articulated in this section. When the input and output grounds are solidly connected by a conductor as indicated by the bold line, any switching operation of the semiconductor devices in the interface circuit will not affect the common mode current. In other words, the common mode current is theoretically zero whatever PWM technique is employed in the interface circuit.

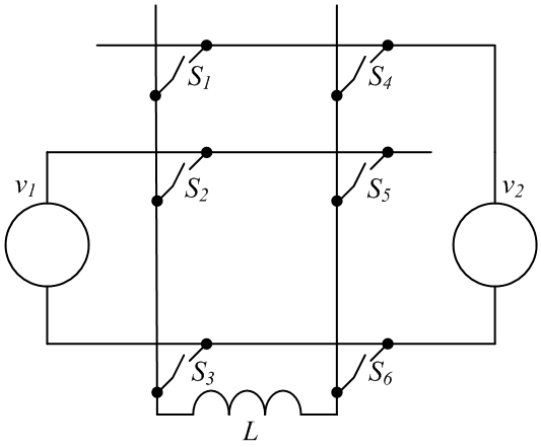
To utilize the same combination method in Section 2.2.1 and further simplify the general topology in Fig. 2.15(b) into the low common mode current circuit, the two voltage sources are connected to have their grounds in common and combined with an inductor as in Fig. 2.17(a). With five wires in total, i.e., three wires of the combined voltage sources and two of the inductor, the combination achieves six intersections according to (2.4).

$$ {}_5C_2 - \left({}_3C_2 + {}_2C_2 \right) = 6 \tag{2.4} $$

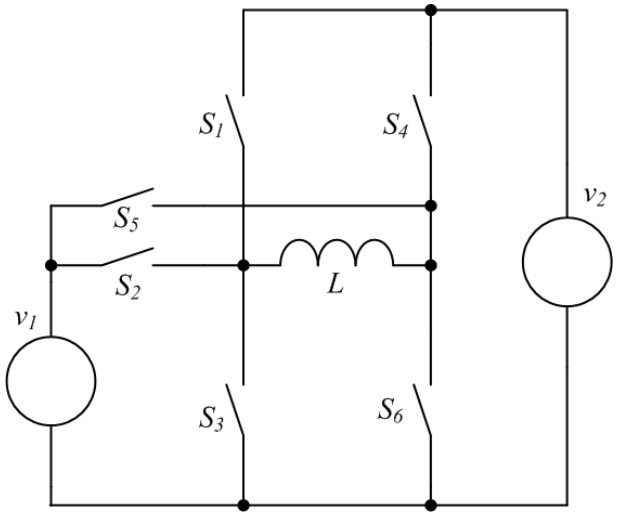
In (2.4), the terms in the parentheses are the number of prohibited intersections, similar with those in (2.3). The term ${}_3C_2$ represents shorting two wires among the three wires of the connected two voltage sources, and ${}_2C_2$ indicates shorting the inductor itself. If all the six intersections are connected with ideal switches as in Fig. 2.17(a), the topology can be redrawn as in Fig. 2.17(b) and *H-bridge converter with additional switch legs* (HA converter) is obtained. Switches S_1, S_3, S_4, and S_6 and the inductor L constitute the

H-bridge, and S_2 and S_5 organize additional switch legs.

The HA converter contains the solidly connected ground which is not intervened by the switching operation and thus features low common mode current. Six switches provide high versatility to emulate various single-ended converter operations and



(a)



(b)

Fig. 2.17. (a) General topology with six switches and common ground. (b) Redrawn H-bridge converter with additional switch legs (HA converter).

PWM methods for H-bridge inverter, and this maximizes the flexibility of the HA converter.

2.3. Feature of HA Converter

The HA converter acts as the general topology for single-ended DC-DC converter with single inductor, e.g., buck, boost, and buck-boost converters, advocating its versatility. The switches S_1 to S_6 are determined to be remained, shorted, or open in the implementation according to the required converter topology.

Figs. 2.18 to 2.21 show the switch manipulation for various DC-DC converter operations. It is assumed that v_1 is the input power source and v_2 is the output power sink for clear explanation. Fig. 2.18 is the buck operation of the HA converter when $v_1 > v_2 > 0$. S_2 and S_3 operate according to the PWM signal, while S_1, S_5, and S_6 are open and S_4 is shorted. Fig. 2.19 shows the boost operation of the HA converter when $v_2 > v_1 > 0$. S_4 and S_6 operate according to the PWM signal, while S_1, S_3, and S_5 are open and S_2 is shorted. Fig. 2.20 illustrates the inverting buck-boost operation of the HA converter when the polarities of v_1 and v_2 are different each other. S_1 and S_2 operate according to the PWM signal, and S_3, S_4, and S_5 are open and S_6 is shorted. Fig. 2.21 shows another inverting buck-boost operation of the HA converter. S_4 and S_5 operate according to the PWM signal. S_1, S_2, and S_6 are open, and S_3 is shorted. The HA converter can merge these operations in single circuit by properly selecting the switches and driving methods.

The two major advantages of the HA converter are the simple structure and low common mode noise. For the simple circuit structure, no additional active semiconductor switch devices are necessary for the HA converter except the six switches S_1 to S_6. The converter may require input or output filters for practical

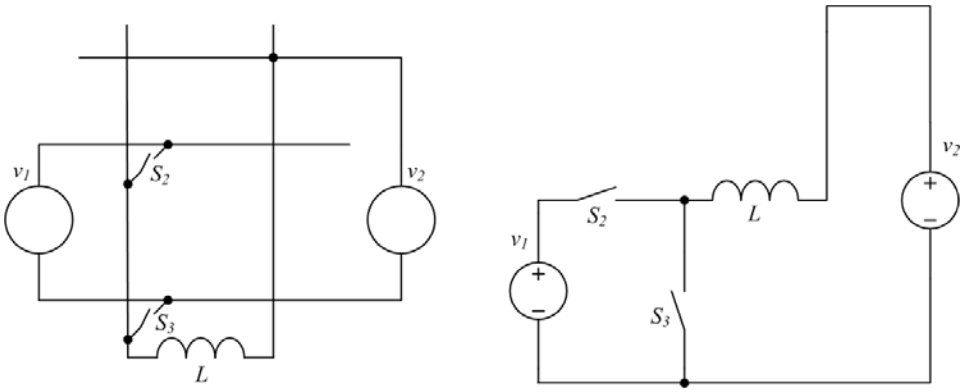


Fig. 2.18. Buck converter operation of the HA converter.

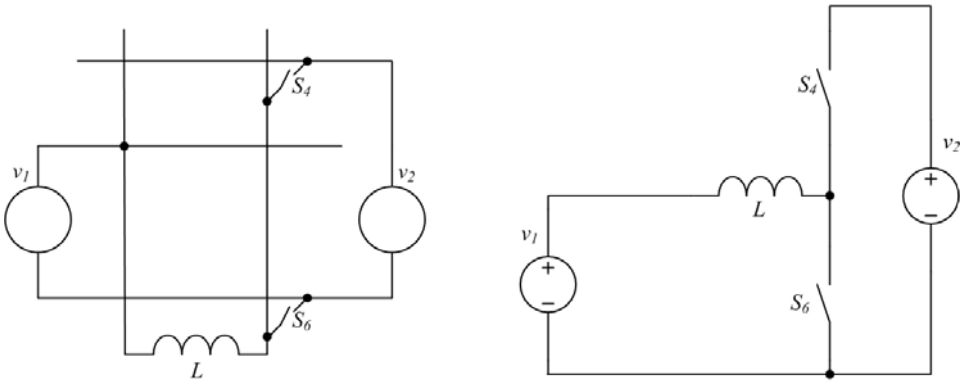


Fig. 2.19. Boost converter operation of the HA converter.

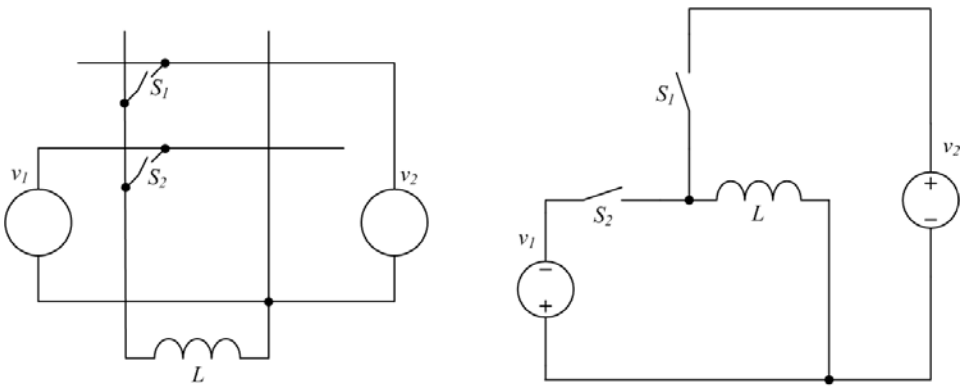


Fig. 2.20. Inverting buck-boost converter operation of the HA converter.

implementation, but it does not need switch devices such as bridge diodes in Fig. 2.4(a) and thyristor unfolding stages in Fig. 4.2. The simplicity of the structure also gives the opportunity to efficiency improvement because the switching and conduction losses in the semiconductor devices are decreased. Following chapters will explain the details of the circuit simplicity and efficiency with the practical HA converter examples. For the low common mode noise, the HA converter does not apply any fluctuating voltage to the parasitic capacitance. Because the HA converter connects the grounds of input and output voltage terminal and shorts the parasitic capacitance effectively, its offspring converters also achieve low common mode voltage and current.

Despite its strong flexibility, however, the HA converter cannot operate as inverting buck or inverting boost converter, which do not exist in the single-ended topology inherently. The inverting buck-boost converters in Figs. 2.20 and 2.21 are the only options for the HA converter to handle the input and output voltages with opposite polarities. The dual H-bridges shown in Fig. 2.15 may realize the inverting buck and inverting boost converter because it does not preserve the single-ended condition, i.e., the grounds are not solidly connected, and therefore it will be exposed to the high

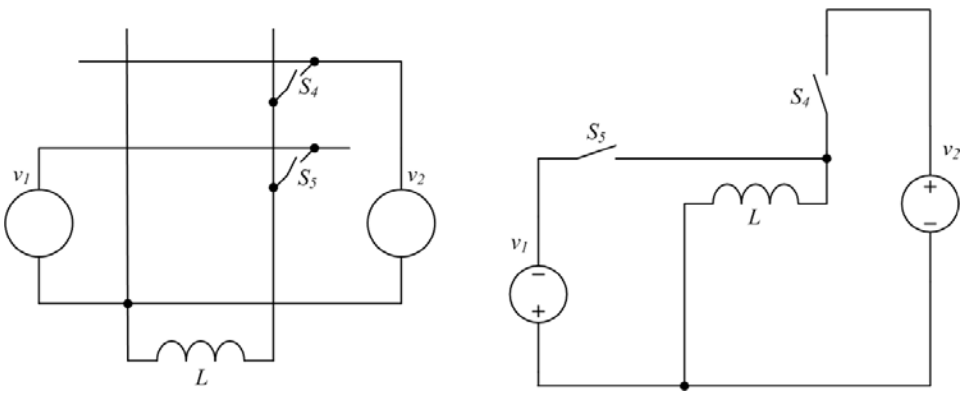
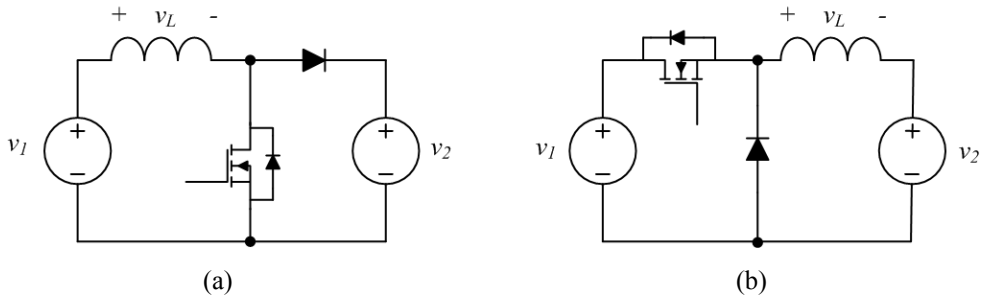


Fig. 2.21. Another inverting buck-boost converter operation of the HA converter.

common mode current.

The reason why the inverting buck and inverting boost converter do not exist in the single-ended topology is analyzed as following. Fig. 2.22 demonstrates the general boost and buck converter with their inductor voltage sign convention, v_L. Table 2.1 summarizes v_L at MOSFET on-time and off-time of each converters. The voltages in Table 2.1 determine the identities of the converter topologies. If the same voltages can be applied to the inductor with the two voltage sources with opposite polarities with common ground, the single-ended inverting buck or inverting boost converter will become also existent. Fig. 2.23 shows the two voltage sources with the common ground and an inductor, of which every terminal is named to distinguish it from the other terminals. The two terminals of the inductor are identified by their names *P* and *N*, and the three terminals of the voltage sources are by *G*, *I*, and *O*. Polarities of the two voltage sources are opposite to each other. The number of cases of connecting the two-terminal element, the inductor, and the three-terminal element, the voltage sources with the common ground, is equivalent of calculating two-permutations of three as shown in (2.5).



(a) (b)

Fig. 2.22. (a) Boost and (b) buck converter and their inductor voltage sign conventions.

$$ {}_3P_2 = \frac{3!}{(3-2)!} = 6 \tag{2.5} $$

Table 2.2 lists various inductor voltages v_L for six possible cases. Again, the inductor voltages at switch-on and switch-off interval give the identity of each converter. None of the combination applies voltages such as $v_1 - v_2$ and $v_2 - v_1$ to the inductor, which represent the identity of the buck and boost converter respectively. Therefore, the inverting buck and inverting boost converter cannot exist in the single-ended topology, and consequently in HA converter.

To apply the HA converter in AC-DC rectification and DC-AC inversion, two converter operations are selected and merged together according to the AC voltage polarity. In a half-line cycle that the polarity of the AC voltage source is same with that of the DC voltage source, one of topologies among buck, boost, and non-inverting buck-boost converter can be selected. In the other half of the line cycle that the AC voltage source has opposite polarity to the DC voltage source, inverting buck-boost converter operation should be employed according to the analysis in the previous paragraph.

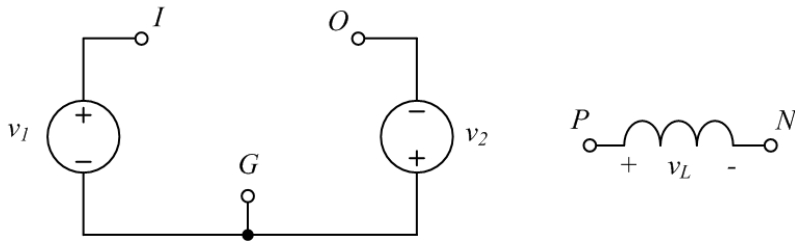


Fig. 2.23. Identification of the terminals of two voltage sources with common ground and inductor.

Table 2.1. Inductor voltages of buck and boost converter for MOSFET-on and MOSFET-off interval

	buck converter	boost converter
MOSFET-on	$v_1 - v_2$	$-v_1$
MOSFET-off	$-v_2$	$v_2 - v_1$

Table 2.2. Possible six inductor voltages according to the connection with two voltage sources with common ground and different polarities

terminal connected to *P*	terminal connected to *N*	v_L
I	*G*	v_1
I	*O*	$v_1 + v_2$
G	*I*	$-v_1$
G	*O*	v_2
O	*I*	$-v_1 - v_2$
O	*G*	$-v_2$

3. B3 Rectifier for AC-DC Conversion[1]

As mentioned in Chapter 2, the low common mode noise of HA converter is especially beneficial in line-related applications such as off-line power supplies and grid-connected inverters. As one of the HA converter offspring circuits, a new boost-buck-boost (B3) rectifier for off-line power supply with active PFC functionality is proposed in this chapter. The B3 rectifier suppresses the common mode current by inheriting the solid ground connection of the HA converter with simple circuit structure.

3.1. Advantage of B3 Rectifier

To cope with the alternating polarity of the AC input voltage, the proposed rectifier topology emulates the operations of two DC-DC converters. Fig. 3.1(a) shows the newly obtained B3 rectifier from the HA converter by merging the two converters in one, the boost converter in Fig. 2.19 and the inverting buck-boost converter in Fig. 2.20. v_g and v_O are AC line voltage and output voltage of the rectifier respectively. The proposed B3 rectifier alternates its equivalent topology according to the line voltage polarity: it works as the boost converter for positive line cycle, and operates as the inverting buck-boost converter for negative line cycle. As shown in Fig. 3.1(b), S_2 and S_6 are replaced by MOSFETs Q_2 and Q_6, and S_1 and S_4 are by diodes D_1 and D_4 for practical implementation. Merging or synthesizing different converters are reported in [40]-[42]. Dwari *et al.* [41] shows a simple parallel combination of the boost and buck-boost converter for energy harvesting application. Though the circuit proposed in [41] has

[1] The main idea of this Chapter is reported in the papers "A Low Common Mode Noise Bridgeless Boost-Buck-Boost Power Factor Correction Rectifier," IEEE Energy Conversion Congress and Exposition, 2012, pp. 2901-2907, and "Low-Common Mode Voltage H-Bridge Converter with Additional Switch Legs," IEEE Transactions on Power Electronics, volume 28, number 4, pp. 1773-1782, 2013.

improved the efficiency, its application is limited to low-voltage environment due to the forward voltage drop of diodes.

Fig. 3.2 shows the conventional off-line AC-DC PFC circuits: a boost rectifier with bridge diodes in Fig. 3.2(a) is the most widely used topology for its continuous line current and simple control. The bridgeless dual-boost rectifier in Fig. 3.2(b) eliminates

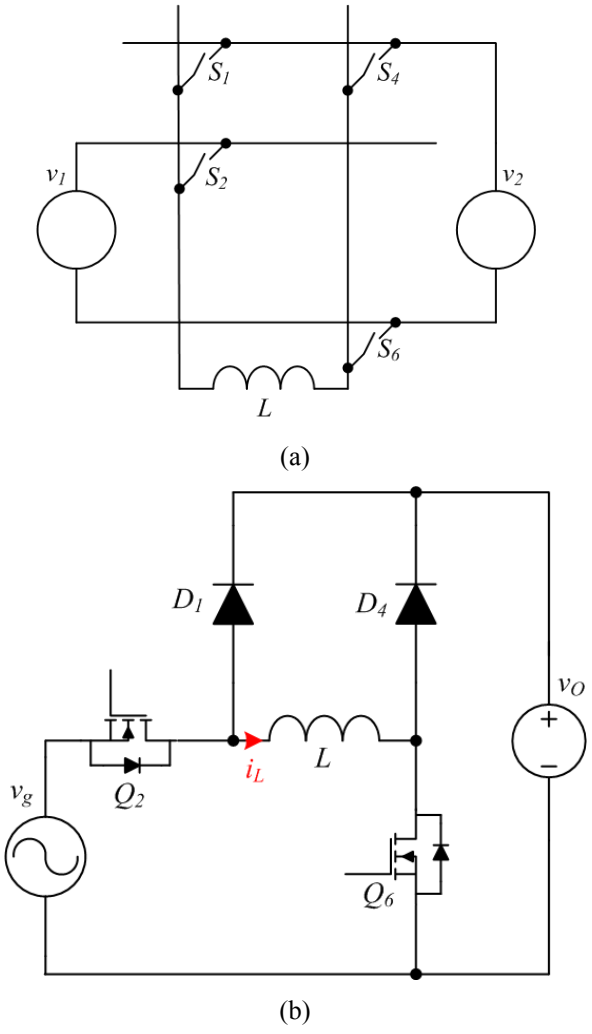
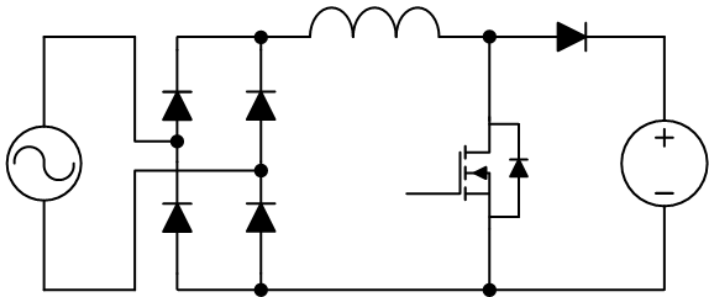


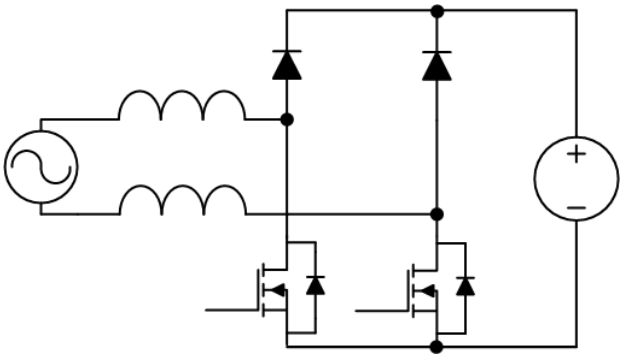
Fig. 3.1. (a) Switch selection for B3 rectifier in the HA converter. (b) B3 rectifier with practical semiconductor devices and reference direction of inductor current.

the bridge diodes in Fig. 3.2(a) to decrease the part count in the conduction path and improve the efficiency [30]. However, the bridgeless rectifier suffers from the high common mode EMI as the trade-off against the improved efficiency because the input and output ground terminals are intervened by high-frequency switching devices. The boost rectifier in Fig. 3.2(a) also contains the bridge diodes between the input and output grounds, but they switch in line frequency and do not cause severe common mode EMI.

The B3 rectifier fully removes the bridge diodes to simplify the circuit structure. Comparing the proposed rectifier in Fig. 3.1(b) with the one in Fig. 3.2(a), the B3



(a)



(b)

Fig. 3.2. Conventional off-line AC-DC PFC rectifiers: (a) boost rectifier with input bridge diodes and (b) bridgeless dual-boost rectifier.

rectifier requires two semiconductor devices, Q_2 and D_1, instead of removing the four slow-recovery bridge diodes. It should be also noted that the B3 rectifier is able to handle bidirectional power flow, i.e., the power delivery from the voltage source v_O to the voltage source v_g as well as from v_g to v_O, by simply replacing the diodes D_1 and D_4 by active switch devices such as MOSFETs. The proposed B3 rectifier can be called as *parallel* flying inductor topology while the circuit in [39] can be *series* flying inductor one.

Beside its circuit simplicity, the B3 rectifier obtains the low common mode current by inheriting the solidly connected grounds of the HA converter. Whether the B3 rectifier is in the boost or inverted buck-boost mode, the ground connection is not intervened by the switching of the semiconductor devices.

3.2. Operation

The B3 rectifier shows four topological states during the operation as illustrated in Fig. 3.3, assuming that the rectifier operates in continuous conduction mode. The direction of the inductor current i_L is expressed by the arrows in Fig. 3.3. States 1 and 2 occur during the positive half-line cycle ($v_g > 0$), and states 3 and 4 during the negative half-line cycle ($v_g < 0$). In state 1, both MOSFETs Q_2 and Q_6 are on and i_L increases by the positive voltage source v_g as shown in Fig. 3.3(a). Fig. 3.3(b) shows that Q_6 goes off in state 2 and i_L flows through D_4. The B3 rectifier operation in states 1 and 2 is the same with the boost converter one. In these states, D_1 does not participate in the operation because it is always reverse-biased. When v_g becomes negative, states 3 and 4 alternate. In state 3 as in Fig. 3.3(c), both MOSFETs Q_2 and Q_6 are on as in state 1. However, the direction of i_L is opposite due to the negative polarity of the voltage

source v_g. Q_2 goes off in state 4 and i_L flows through D_1 as illustrated in Fig. 3.3(d). The B3 rectifier in the states 3 and 4 operates like the inverting buck-boost converter. In the states 3 and 4, D_4 does not participate in the operation because it is always turned off.

The on/off state of Q_2 in states 1 and 2 does not affect the rectifier operation. However, it is recommended keeping Q_2 turned on during the positive line cycle and letting i_L flow through the junction of Q_2 when Q_2 is MOSFET because it decreases the conduction loss of Q_2 like synchronous rectifier. Similar with Q_2 in states 1 and 2, the on/off state of Q_6 in states 3 and 4 does not affect the rectifier operation. But, fully

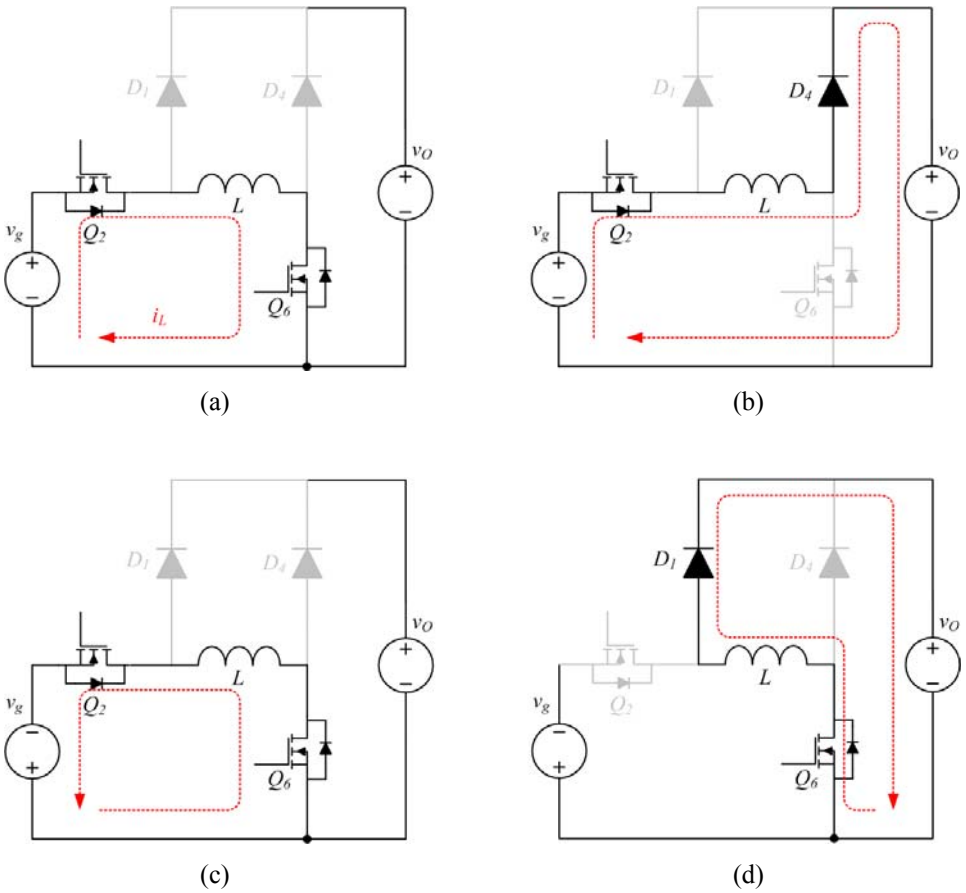


Fig. 3.3. Four operational states of the B3 rectifier: (a) state 1, (b) state 2, (c) state 3, and (d) state 4.

turning on Q_6 and steering i_L into the junction of Q_6 is also desirable to decrease the conduction loss in Q_6 during the negative half-line cycle if Q_6 is MOSFET. Fig. 3.4 summarizes the gate drive signals of Q_2 and Q_6 within a line cycle. If the active switches of the B3 rectifier are IGBTs, fully turning on Q_2 and Q_6 is not recommended because it does not help reduce the conduction losses but rather increases the power consumption in switch driving circuit.

3.3. Control

A properly designed controller is essential for the B3 rectifier to achieve good performance. This section shows what problem occurs in the B3 rectifier when conventional controller is applied, and investigates the cause of the problem. Then the proper controller is designed step by step, considering specially required design criteria

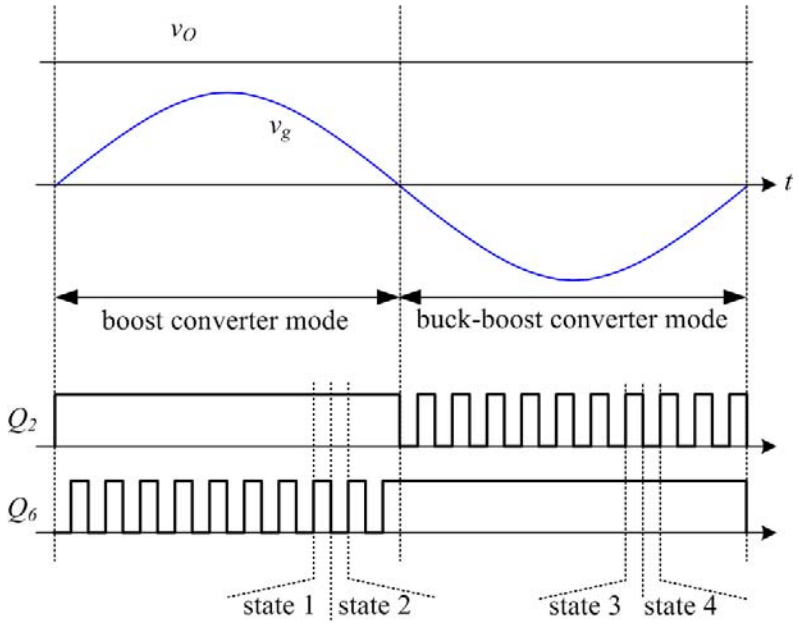
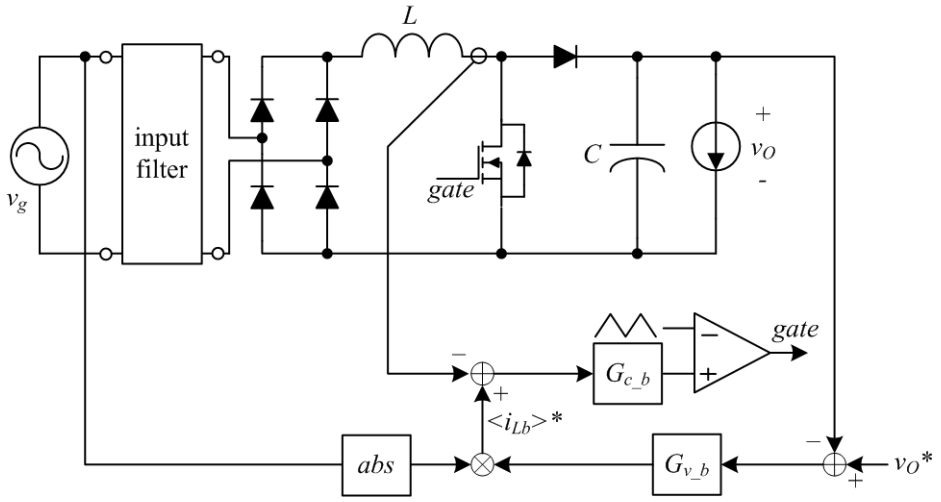


Fig. 3.4. Gate signals of Q_2 and Q_6 of B3 rectifier during a line cycle when they are MOSFETs.

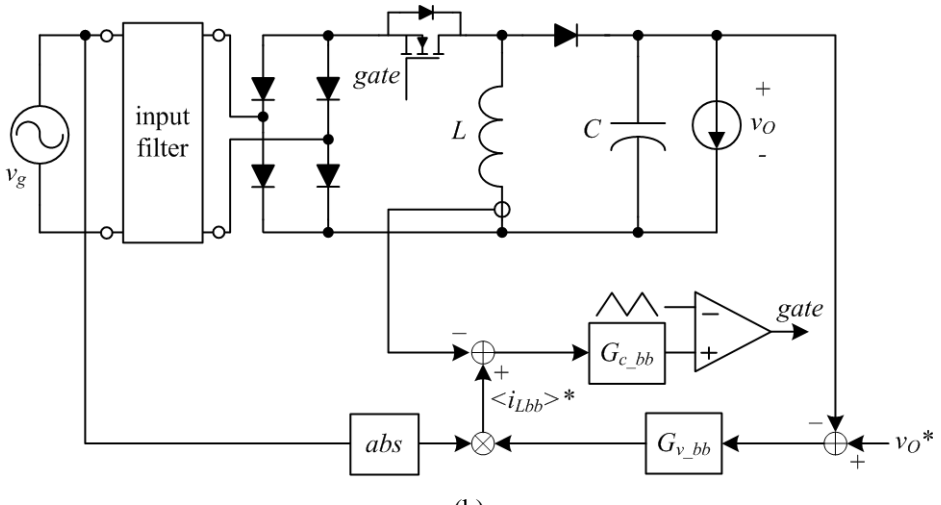
for the B3 rectifier. The power stage circuit parameters for the controller design are listed below:

1) line voltage: 230 Vac,

2) inductor L: 950 μH,



(a)



(b)

Fig. 3.5. Rectifiers with their own separate controllers: (a) boost rectifier and (b) buck-boost rectifier.

3) output capacitor C: 660 μF,

4) output voltage v_O: 400 V,

5) switching frequency f_s: 50 kHz.

3.3.1. Power Imbalance in a Line Cycle

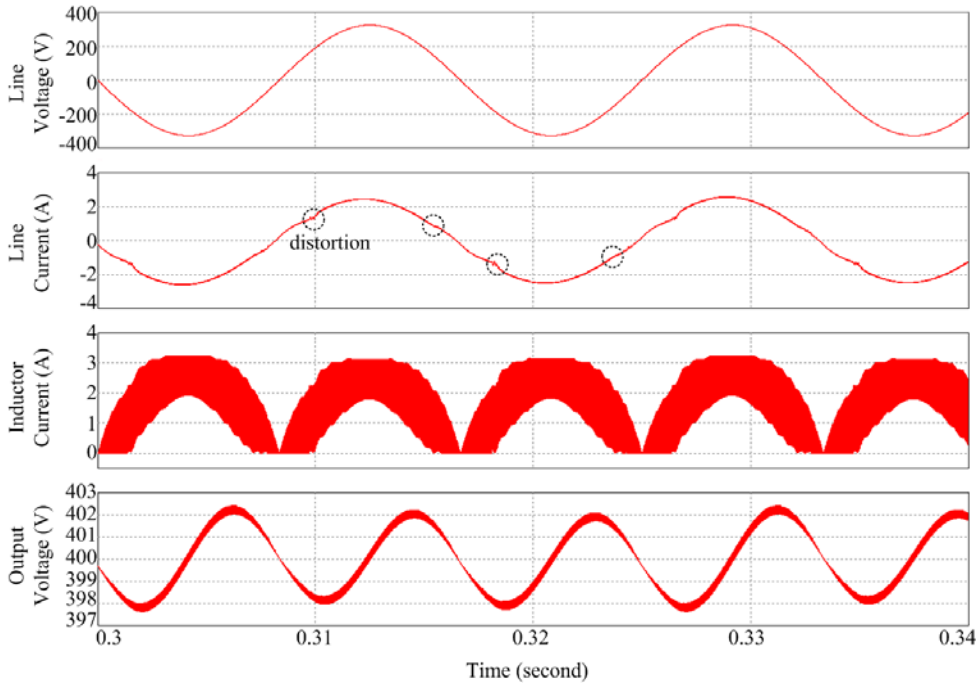
The B3 rectifier utilizes average current mode control [45]-[46] to shape the AC line current and minimize total harmonic distortion (THD). However, relationship between the average line current and average inductor current per switching cycle alternates according to the equivalent topology of the rectifier. In other words, the relationship between the average inductor and average line current when the rectifier operates as the boost converter is different from that when the rectifier works as the buck-boost converter.

If the controller is separately designed for each topological operation, the input power between the positive and negative half-line cycle will lose the balance. In other words, the controller that combines the two controllers, the one is optimized for the boost converter and the other is for the buck-boost converter, does not guarantee the proper operation of the proposed B3 rectifier. The imbalanced input power may induce undesirable stress on the semiconductor devices, rectification efficiency degradation, and poor output voltage regulation.

Figs. 3.5(a) and 3.5(b) show the separate boost and buck-boost rectifiers to simulate the power imbalance between the positive and negative halves of the line cycle. The power stages of the two rectifiers employ same input filters, inductors (950 μH), and capacitors (660 μF), and utilize two-loop average current mode controls with same inner and outer loop bandwidths with sufficient phase margins at 400 -W output condition. In

Fig. 3.5, the boxes named as G_{c_b}, G_{c_bb}, G_{v_b}, G_{v_bb}, and *abs* are current compensator for boost converter, current compensator for buck-boost converter, voltage compensator for boost converter, voltage compensator for buck-boost converter, and absolute value computation block. v_O*, $\langle i_{Lb} \rangle^*$, and $\langle i_{Lbb} \rangle^*$ are the references of output voltage, boost converter average inductor current, and buck-boost converter average inductor current respectively.

Simulation results by PSIM are shown in Fig. 3.6. Inspecting Figs. 3.6(a) and 3.6(b), the two rectifiers operate properly with their control loops. Both controllers regulate the output voltage and shape the line current well. Subtle differences in the output voltage ripple and input current shape between the two rectifiers are due to the different

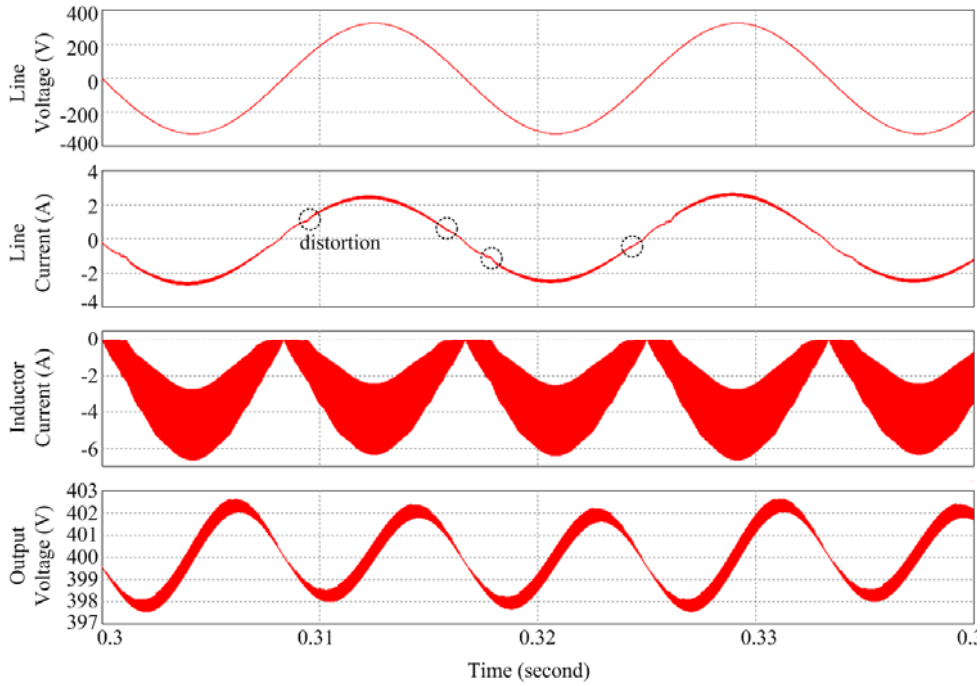


(a)

Fig. 3.6. (a) Simulation waveforms of boost rectifier in Fig. 3.5(a).

topological characteristics of the boost and buck-boost converter. No input current imbalance between the positive and the negative half-line cycles is observed in both rectifiers. In addition, there are distortions in the line current as marked by broken-line circles in Figs. 3.6(a) and 3.6(b): they are due to small signal characteristic change of the power stage caused by inductor current conduction mode transition. When the line voltage is low near zero crossing, inductor current is temporarily in discontinuous conduction mode. If the line voltage goes higher, the inductor current goes in continuous conduction mode and the distortion occurs.

The compensators designed and simulated in Figs. 3.5 and 3.6 are merged together to control the proposed B3 rectifier as shown in Fig. 3.7. Compensators G_{c_b}, G_{c_bb}, G_{v_b}, and G_{v_bb} are same with those shown in Fig. 3.5, and *pol* is the polarity of the AC line



(b)

Fig. 3.6. (Cont.) (b) Simulation waveforms of buck-boost rectifier in Fig. 3.5(b).

voltage. The two two-loop control blocks operate independently each other and control signal v_c is selected according to *pol*. Fig. 3.8 shows the simulation results of the circuit in Fig. 3.7. Though each compensator is optimized for boost or buck-boost converter, their control performance for the B3 rectifier is poor. The input current is not balanced between the positive and negative half-line cycle and causes undesirable stress on the semiconductor devices, rectification efficiency degradation, and poor output voltage

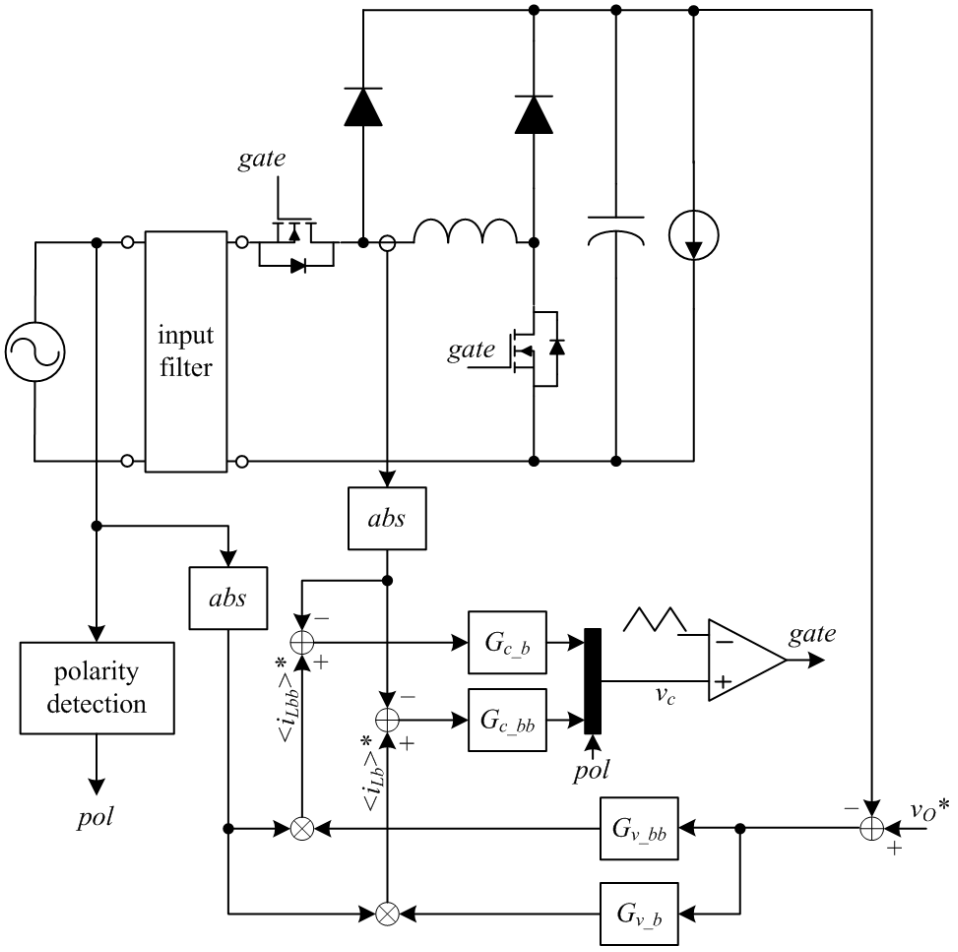


Fig. 3.7. B3 rectifier controlled by the merged controllers shown in Figs. 3.5(a) and 3.5(b) which results the input current imbalance.

regulation. This deteriorated performance of merged controllers originates from the fact that the bandwidths of the total loop gains are low. Generally, low bandwidth of the outer loop gain in active PFC controller is mandatory to achieve high power factor and low THD [49], but it causes the imbalance in the B3 rectifier control. To articulate, the control signal cannot follow the step change of power stage transfer functions, i.e., change between the boost and buck-boost functions, within a half-line cycle. Therefore, in addition to optimizing the compensators with their own topologies, a special method to avoid the current imbalance is required in the controller design.

3.3.2. Inductor Current Reference Calculation

The relationship between the average line current and average inductor current per switching cycle changes according to its equivalent topology of the proposed B3

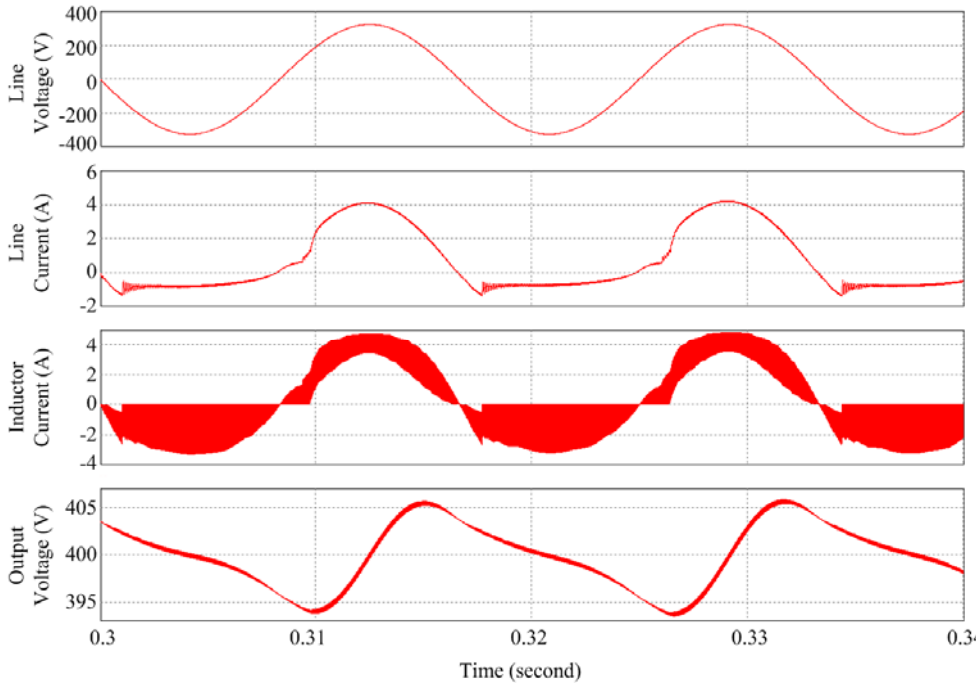


Fig. 3.8. Simulation results of the B3 rectifier in Fig. 3.7 contains input current imbalance.

rectifier. Therefore, a correction factor should be included in the control loop to properly shape the line current regardless of the equivalent topologies or operation modes of the B3 rectifier.

For the boost converter operation case when $v_g > 0$, the average inductor current in a unit switching cycle, $\langle i_L \rangle$ defined as shown in (3.1), is equal to the average line current because the inductor is series-connected to the AC voltage source through the fully turned-on switch Q_2.

$$\langle i_L \rangle = \frac{1}{T_S} \int_{T_S} i_L(t) dt \tag{3.1}$$

T_S is the switching period in (3.1). Assuming that the rectifier is in steady state and considering the reference direction of the inductor current in Fig. 3.1(b), the inductor current reference of the boost converter mode, $\langle i_{Lb} \rangle^*$, should be a sine wave to shape the line current into the same sine wave with negligible harmonic components as shown in (3.2).

$$\langle i_{Lb} \rangle^* = \langle i_L \rangle = I_m \sin \omega t \tag{3.2}$$

In (3.2), ω is angular frequency of the AC line voltage and I_m is the maximum line current in a half-line cycle which is determined by the controller according to the line voltage and load current of rectifier.

For the buck-boost converter operation when v_g is negative or $\pi \le \omega t < 2\pi$, on the other hand, the average line current is not equal to the average inductor current but equal to the average switch current. The average switch current of Q_2 per switching period $\langle i_{Q2} \rangle$ is dependent on the duty cycle ratio d in the buck-boost mode as defined in (3.3)

and is proportional to the sinusoid as expressed in (3.4).

$$d = \frac{v_O}{|v_g| + v_O} \tag{3.3}$$

$$\langle i_{Q2} \rangle = \langle i_L \rangle d = I_m \sin \omega t \tag{3.4}$$

Considering the input voltage is also a sinusoid as in (3.5) where $V_{g\max}$ is the maximum input voltage in a line cycle, the inductor current reference of the buck-boost converter mode $\langle i_{Lbb} \rangle^*$ is derived as (3.6).

$$v_g = V_{g\max} \sin \omega t \tag{3.5}$$

$$\langle i_{Lbb} \rangle^* = \langle i_L \rangle = \frac{I_m \sin \omega t}{d} = \left(1 + \frac{|V_{g\max} \sin \omega t|}{v_O} \right) \langle i_{Lb} \rangle^* \tag{3.6}$$

Inspecting (3.6), one can notice that a correction factor, the term in the parentheses in (3.6), is multiplied to $\langle i_{Lb} \rangle^*$ to yield $\langle i_{Lbb} \rangle^*$. Fig. 3.9 compares the magnitudes of $\langle i_{Lbb} \rangle^*$ with the normalized $\langle i_{Lb} \rangle^*$ in a line cycle assuming that v_g is a pure sine wave and v_O is 400 Vdc. The power imbalance and line current distortion observed in Fig. 3.8 are because the current reference for each topological state does not obey the relation in (3.6). Because of the low bandwidth of the voltage loops, the current reference cannot be aligned to satisfy (3.6) within a half-line cycle. Therefore, a feedforward of the correction factor for the inductor current reference should be included in the control loop of the B3 rectifier to overcome the slow response of the voltage compensator and achieve undistorted and balanced line current.

It is also noted from Fig. 3.9 that the inductor of the B3 rectifier may be larger in

size than that of the conventional boost rectifier, though their inductances are same to each other. The inductor of the proposed rectifier should be designed to avoid saturation considering the inductor current reference has higher peak value in the buck-boost mode than in the boost mode, i.e., when $\omega t = \frac{3}{2}\pi$.

Fig. 3.10 shows the control block diagram that contains the proper feedfoward to achieve balanced line input current. In Fig. 3.10, a phase-locked-loop (PLL) is applied to obtain noise-free sine wave which is synchronized with the AC line voltage. θ is the phase angle of the AC line voltage v_g. G_c and G_v represent unified current and voltage compensator respectively, which are designed in the next section. The computation block in the broken-line box is to feedforward the correction factor, $1+\frac{\left|V_{g\max}\sin\omega t\right|}{v_O}$. Thanks to this block, the controller overcomes the slow response of the voltage loop and

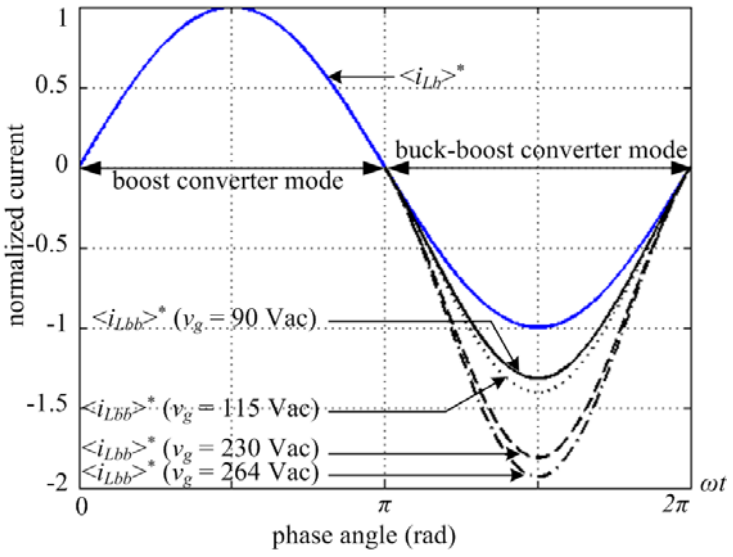


Fig. 3.9. Comparison of inductor current references in the positive and negative line cycles for various line voltages.

balances the positive and negative line current in every line cycle.

In addition, using the PLL in the PFC rectifier and drawing out sinusoidal current from the grid is controversial when the line voltage is not a pure sine wave but a distorted one. Controlling the input current of the PFC rectifier to have higher harmonics as well as the fundamental components may help reduce rms input current of the rectifier and imaginary power generated by the utility in some cases. However, present

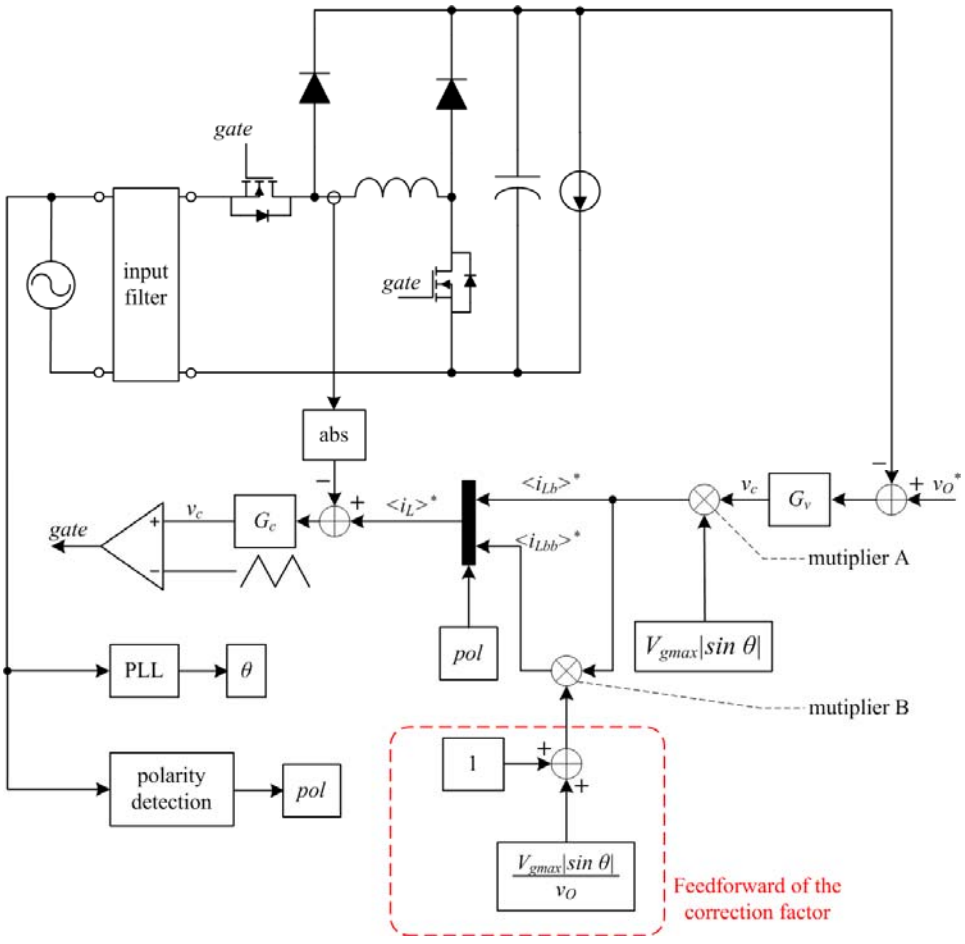


Fig. 3.10. Control block diagram that applies proper feedfoward to achieve balanced line input current for the B3 rectifier.

standard on the input current such as [21] does not have any regulation when the line voltage is distorted, because it assumes that the line voltage is an ideal sine wave. In this dissertation, the PLL is used for the present and draws sinusoidal input current whether the line voltage is distorted or not.

The control is able to be implemented in both analog and digital method. The diagram in Fig. 3.10 contains two multipliers such as multiplier A and B. Generally, commercial analog PFC rectifier control ICs contain one multiplier that functions as multiplier A. One additional external multiplier for multiplier B is therefore sufficient to realize the feedforward scheme in analog control implementation.

3.3.3. Compensator Design

Fig. 3.11 shows typical two-loop control blocks of the average current mode controlled PFC rectifier. G_{id} and G_{vd} are the power stage transfer functions from duty

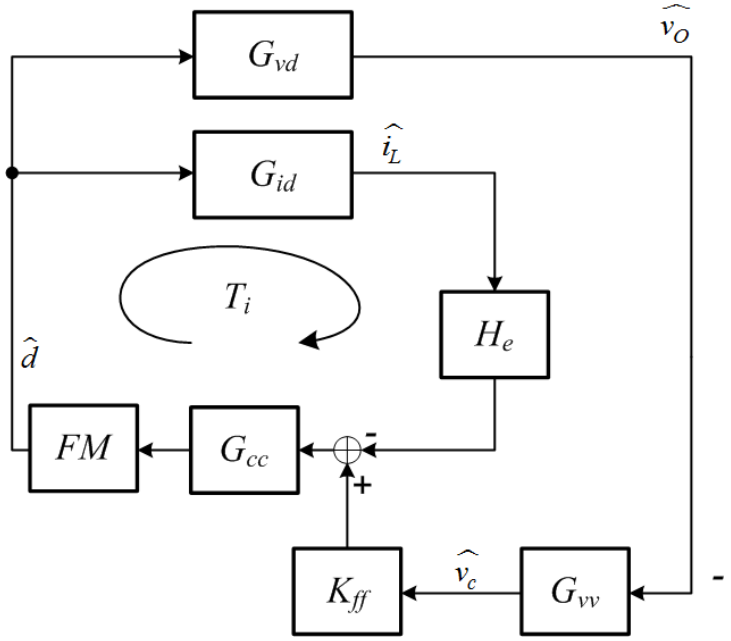


Fig. 3.11. Typical two-loop control diagram of average current mode controlled rectifier.

cycle to inductor current and duty cycle to output voltage respectively. G_{cc}, G_{vv}, K_{ff}, FM, and H_e are current compensator, voltage compensator, input voltage feedforward gain, modulator gain, and sampling effect [48]. $\hat{v}_c$ is the small signal component of the control voltage or the output of G_{vv}. The typical design process of the two-loop control follows three steps as following:

1) inner loop design: Inner current loop gain, T_i as expressed in (3.7), is firstly stabilized with sufficient bandwidth and phase margin.

$$T_i = G_{id} H_e G_{cc} FM \tag{3.7}$$

It is generally known that the proper bandwidth of the current loop of the PFC rectifier is around 5 kHz [47] for commercial AC line voltage.

2) control-to-output voltage transfer function derivation: A control-to-output voltage transfer function with inner loop closed, $\left.\frac{\hat{v}_O}{\hat{v}_c}\right|_{T_i \text{ closed}}$ defined as in (3.8), is derived next.

$$\left.\frac{\hat{v}_O}{\hat{v}_c}\right|_{T_i \text{ closed}} = \frac{G_{vd} K_{ff} G_{cc} FM}{1 + T_i} \tag{3.8}$$

Eq. (3.8) represents the new power stage characteristic with the inner current loop closed. The feedfoward gain K_{ff} is the rms of the sensed AC line voltage. Huliehel *et al.* [48] insists that it is a good approximation to replace the rectified sinusoidal voltage source with a DC voltage source with its rms value. With this approximation, if the AC line voltage is 230 Vac and it is sensed by the sensing gain 1, K_{ff} becomes 230.

3) outer loop design: Based on the control-to-output voltage transfer function, the voltage compensator G_{vv} is designed to close outer loop to regulate the output voltage. The outer loop gain T_v is defined in (3.9).

$$T_v = G_{vv}\left.\frac{\hat{v}_O}{\hat{v}_c}\right|_{T_i \text{ closed}} = \frac{G_{vv}G_{vd}K_{ff}G_{cc}FM}{1+T_i} \tag{3.9}$$

The bandwidth of T_v is usually low, i.e., 5 to 10 Hz, to attenuate the twice line frequency component of $\hat{v}_c$. If this component is not sufficiently suppressed, the line current will be distorted to degrade the performance of the rectifier [49].

To design the unified controller for B3 rectifier, the same procedure with the conventional rectifier controller design is required. A small signal block diagram in Fig. 3.12 is considered to control both the boost and buck-boost operation of the B3 rectifier. The power stage transfer functions, the shaded boxes in Fig. 3.12, are derived by utilizing state-space averaging [43]. Single-pole double-throw switches operate in twice line frequency, changing the signal path according to the AC line voltage polarity.

Defining that s is complex number in Laplace domain, four power stage transfer functions are shown in following equations.

$$G_{id\_bb} = \frac{\hat{i}_L}{\hat{d}} = \frac{V_O(1+D_{bb})}{D_{bb}D_{bb}{}'^2R}\frac{1+\frac{RC}{1+D_{bb}}s}{1+\frac{L}{D_{bb}{}'^2R}s+\frac{LC}{D_{bb}{}'^2}s^2} \tag{3.10}$$

$$G_{id\_b} = \frac{2V_O}{D_b{}'^2R}\frac{1+\frac{RC}{2}s}{1+\frac{L}{D_b{}'^2R}s+\frac{LC}{D_b{}'^2}s^2} \tag{3.11}$$

$$G_{vd\_bb} = \frac{\hat{v}_O}{\hat{d}} = \frac{V_O}{D_{bb}D_{bb}{}'}\frac{\left(1-\frac{D_{bb}L}{D_{bb}{}'^2R}s\right)}{1+\frac{L}{D_{bb}{}'^2R}s+\frac{LC}{D_{bb}{}'^2}s^2} \tag{3.12}$$

$$G_{vd\_b} = \frac{V_O}{D_b'} \frac{\left(1 - \frac{L}{D_b'^2 R} s\right)}{1 + \frac{L}{D_b'^2 R} s + \frac{LC}{D_b'^2} s^2} \tag{3.13}$$

From (3.10) to (3.13), G_{id} and G_{vd} represent open-loop transfer functions from duty cycle to inductor current and from duty cycle to output voltage respectively. Suffices $_b$ and $_{bb}$ indicate that the transfer function is for the boost and buck-boost converter. R, L, C, and V_O are load resistance, inductance, output capacitance, and DC output voltage respectively. Duty cycles and complementary duty cycles for the boost and buck-boost

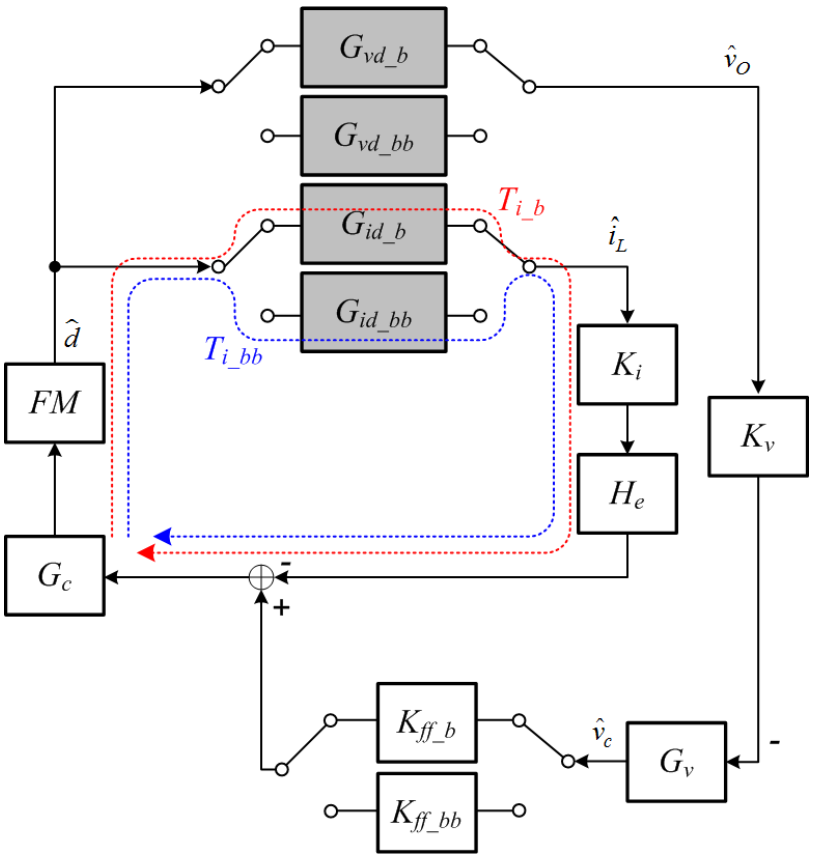


Fig. 3.12. Small signal block diagram of the B3 rectifier.

operations, D_b, D_b', D_{bb}, and D_{bb}', are defined in (3.14)-(3.17) where V_{grms} is the rms AC line input voltage.

$$D_b = 1 - \frac{V_{grms}}{V_O} \tag{3.14}$$

$$D_b' = 1 - D_b \tag{3.15}$$

$$D_{bb} = \frac{V_O}{V_{grms} + V_O} \tag{3.16}$$

$$D_{bb}' = 1 - D_{bb} \tag{3.17}$$

Inspecting the transfer function pairs (3.10)-(3.11) and (3.12)-(3.13), one can notice that the small signal characteristics of the boost and buck-boost converters are similar to each other.

1) inner loop design: Fig. 3.13 shows the Bode plot of G_{id_b} and G_{id_bb} up to the half of switching frequency, 25 kHz, when the B3 rectifier operates in the condition of 230

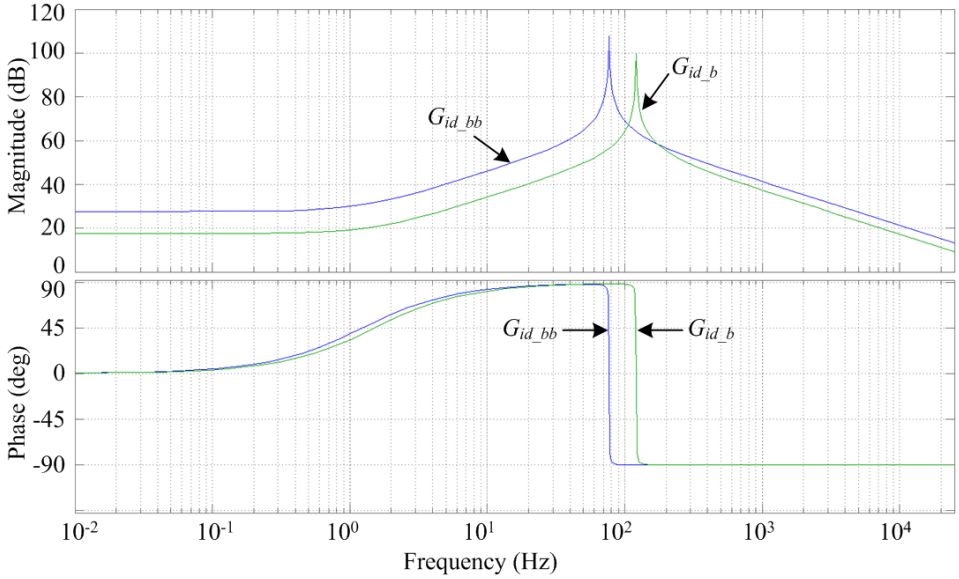


Fig. 3.13. Bode plot of G_{id_b} and G_{id_bb} up to the half of switching frequency, 25 kHz.

Vac line input voltage and 400 -V 500 -W output. Because the two curves in Fig. 3.13 do not show significant difference, single unified current compensator is sufficient to regulate the inductor current. For more precise control, two current loop compensators, the one for the boost operation and the other for the buck-boost operation, may be designed separately and adaptively selected according to the polarity of the line input voltage as simulated in Fig. 3.7. However, the effect of the adaptive control with the two compensators will be negligible comparing with that of the unified current loop compensator because the transfer functions G_{id_b} and G_{id_bb} are similar to each other.

G_c is designed as the unified current compensator to guarantee the sufficient bandwidths and phase margins for both boost and buck-boost operation. In this dissertation, G_c has an integrator and a zero in the frequency domain, i.e., G_c is a proportional-integral (PI) compensator, of which frequency response is shown in (3.18).

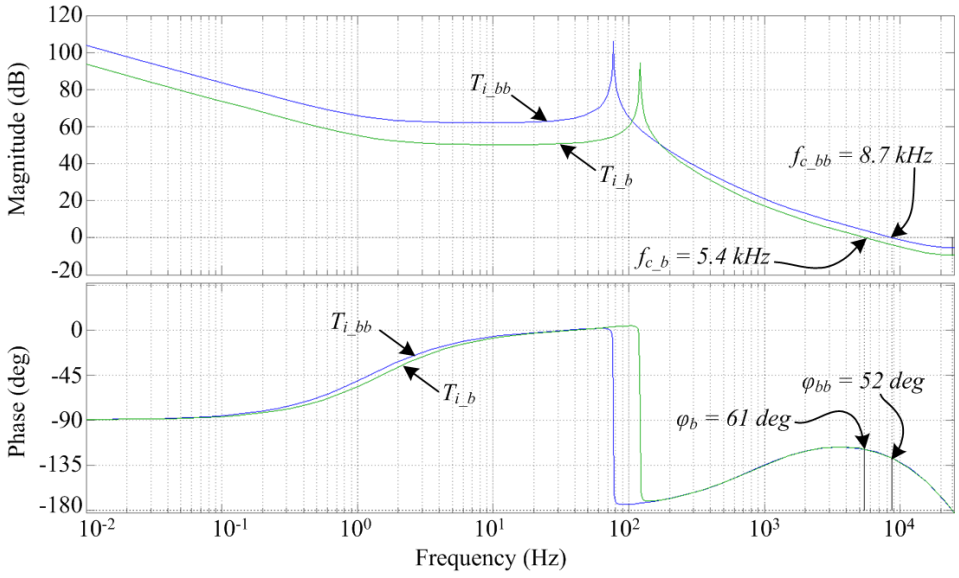


Fig. 3.14. Bode plot of inner loops T_{i_b} and T_{i_bb}.

$$G_c = \frac{\omega_{ic}}{s}\left(1+\frac{s}{\omega_{zc}}\right) \tag{3.18}$$

Assuming that the inductor current sensing gain K_i is 1 and that FM is 3,000 according to the specification of the digital controller, ω_{ic} and ω_{zc} in (3.18) are selected as 1,200 krad/s and 5.5 krad/s. Bode plot in Fig. 3.14 shows the curves for resultant inner loops T_{i_b} and T_{i_bb}, which are expressed in (3.19) and (3.20).

$$T_{i\_b} = G_{id\_b} G_c K_i H_e FM \tag{3.19}$$

$$T_{i\_bb} = G_{id\_bb} G_c K_i H_e FM \tag{3.20}$$

f_c and φ in Fig. 3.14 are the bandwidth and phase margin of each topological mode, according to their suffice $_b$ and $_{bb}$. When the unified current compensator G_c is applied to G_{id_b} and G_{id_bb} simultaneously, T_{i_b} has narrower bandwidth and higher phase margin than T_{i_bb}, i.e., $f_{c\_b} < f_{c\_bb}$ and $\varphi_b > \varphi_{bb}$ as shown in Fig. 3.14. It is generally known that the current loop bandwidth of the PFC rectifier is sufficient when it is around 5 kHz [47]. Considering that f_{c_b} and f_{c_bb} are 5.4 kHz and 8.7 kHz as indicated in Fig. 3.14, the inductor current of B3 rectifier is expected to be well regulated by the resultant current loop whether it is in the boost or buck-boost operation.

2) control-to-output voltage transfer function derivation: Feedfoward gains should be determined in advance to derive $\frac{\hat{v}_O}{\hat{v}_c}$. The feedforward gains in Fig. 3.12, K_{ff_b} and K_{ff_bb}, are the rms value of the input voltage feedforward and the correction factor for input current balancing evaluated in Section 3.3.2. In Fig. 3.10, the control signal v_c becomes the inductor current references, $<i_{Lb}>^*$ and $<i_{Lbb}>^*$, by being multiplied by the input and output voltage related quantities.

As mentioned in [48], the correction factor $1+\frac{\left|V_{g\max}\sin\omega t\right|}{v_O}$ which is marked as the broken-line box in Fig. 3.10 is also replaced by its rms value K_{corr}, of which derivation is shown in Appendix A.1. For 230 Vac line input voltage case, the feedforward gains are determined as in (3.21) and (3.22).

$$K_{ff\_b}=230 \tag{3.21}$$

$$K_{ff\_bb}=K_{corr}K_{ff\_b}=1.7K_{ff\_b}=391 \tag{3.22}$$

The resultant control-to-output voltage transfer functions with the inner loops closed are expressed in (3.23) and (3.24) and plotted in Fig. 3.15.

$$\left.\frac{\hat{v}_O}{\hat{v}_c}\right|_b=\frac{G_{id\_b}K_{ff\_b}G_cFM}{1+T_{i\_b}} \tag{3.23}$$

$$\left.\frac{\hat{v}_O}{\hat{v}_c}\right|_{bb}=\frac{G_{id\_bb}K_{corr}K_{ff\_b}G_cFM}{1+T_{i\_bb}} \tag{3.24}$$

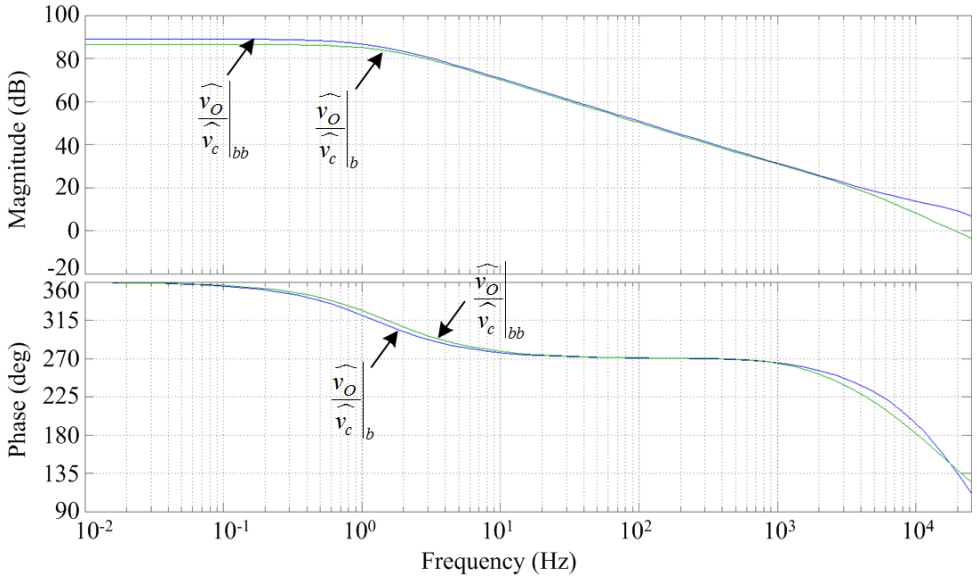


Fig. 3.15. Control-to-output voltage transfer functions with inner loops closed.

The two curves in Fig. 3.15 become more similar to each other thanks to the correction factor, comparing with those in Fig. 3.14.

3) outer loop design: The unified voltage compensator G_v is designed to regulate the voltage as the last step of the controller design. G_v is also designed to have an integrator and a zero like G_c, as in (3.25).

$$G_v = \frac{\omega_{iv}}{s}\left(1+\frac{s}{\omega_{zv}}\right), \tag{3.25}$$

ω_{iv} and ω_{zv} are determined as 0.003 rad/s and 10 rad/s in (3.25), considering the voltage sensing gain K_v as 1. The outer loop gains T_{v_b} and T_{v_bb} are in (3.26) and (3.27), and also plotted in Fig. 3.16.

$$T_{v\_b} = \frac{K_v G_v G_{id\_b} K_{ff\_b} G_c FM}{1+T_{i\_b}} \tag{3.26}$$

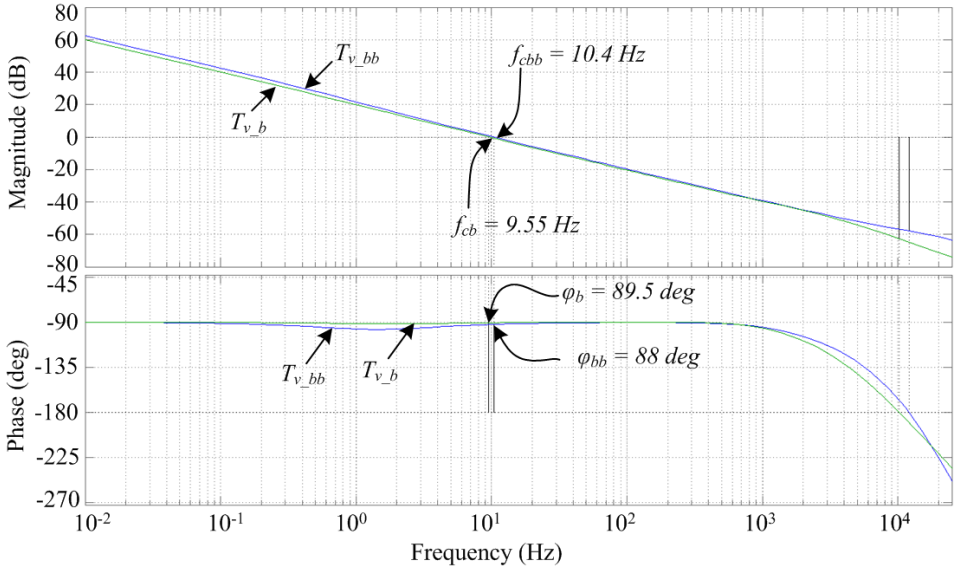
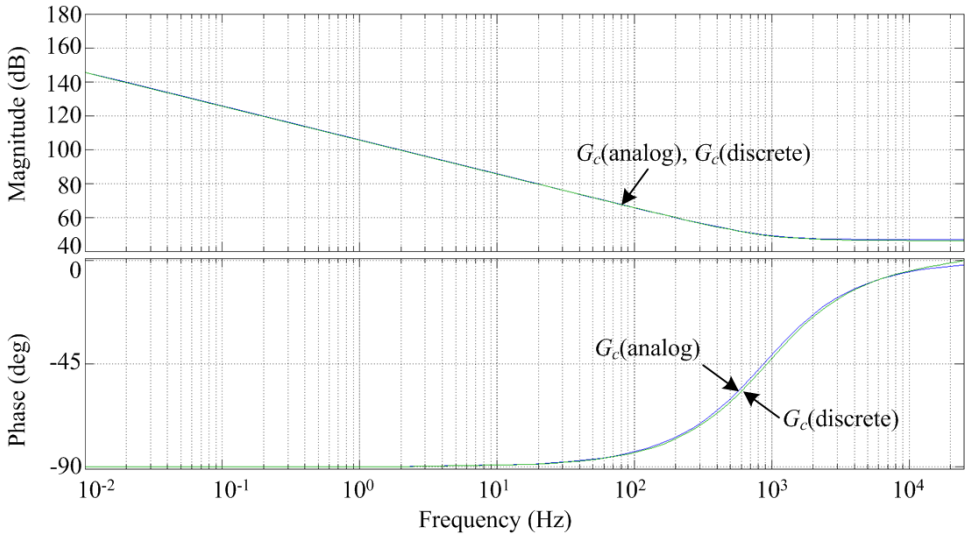


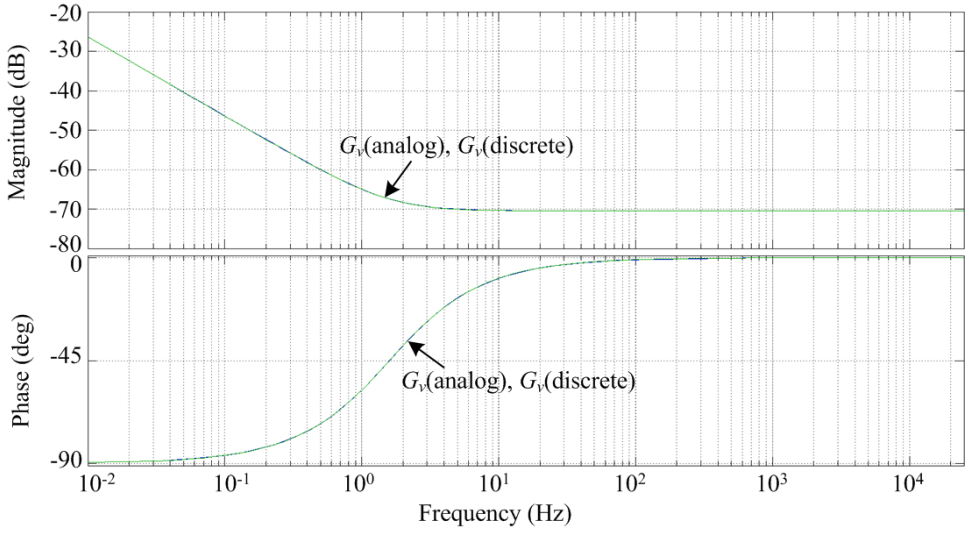
Fig. 3.16. Outer loop gains T_{v_b} and T_{v_bb}.

$$T_{v\_bb} = \frac{K_v G_v G_{id\_bb} K_{corr} K_{ff\_b} G_c FM}{1 + T_{i\_bb}} \tag{3.27}$$

Similar as the inner loops, the two outer loop gains are similar to each other though the separate voltage compensators are not used. The bandwidths of the outer loop for the



(a)



(b)

Fig. 3.17. Comparison of analog and discrete domain compensator transfer functions. (a) G_c. (b) G_v.

boost and the buck-boost operations are 10.4 Hz and 9.55 Hz, which are much smaller than the twice line frequency. The inductor current in the B3 rectifier is therefore expected to have negligible distortion.

For digital control modeling, the current and voltage compensators, as designed in (3.18) and (3.25) respectively, show negligible phase attenuation when their *s*-domain transfer functions are interpreted into *z*-domain ones. Bode plots in Fig. 3.17 compare analog and discrete compensator transfer functions interpreted by zero-order-hold method, and there are nearly zero differences between the phase curves. Therefore, the digital control algorithm that follows the dynamics of the *s*-domain functions will show almost same dynamic response with the analog counterpart.

Fig. 3.18 shows the simulation waveform of the B3 rectifier with the resultant controller when the rectifier input is 230 Vac and output is 400 V and 400 W, which are

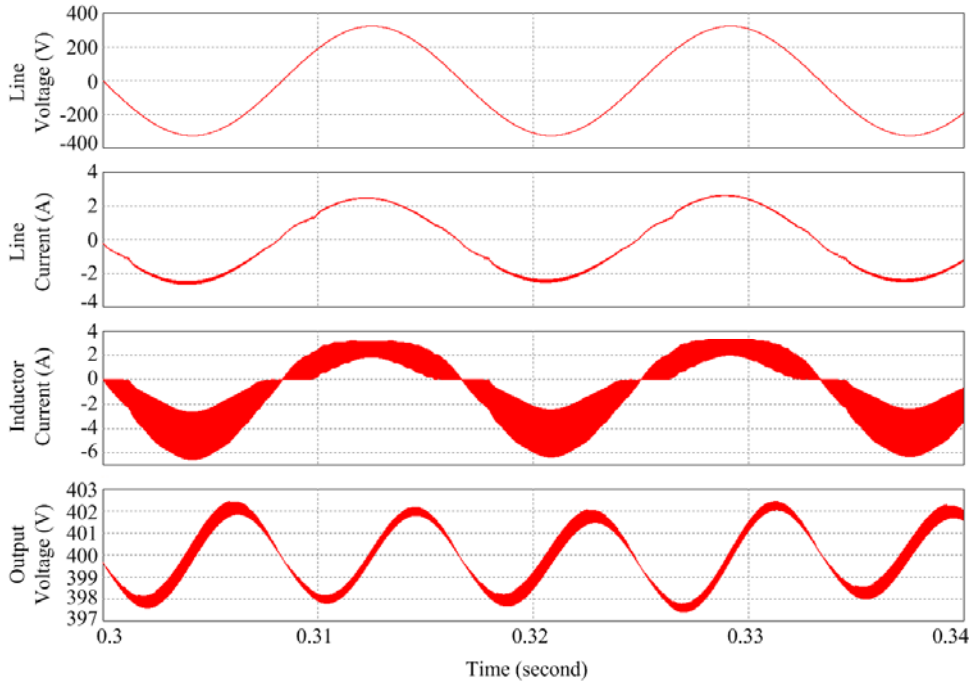
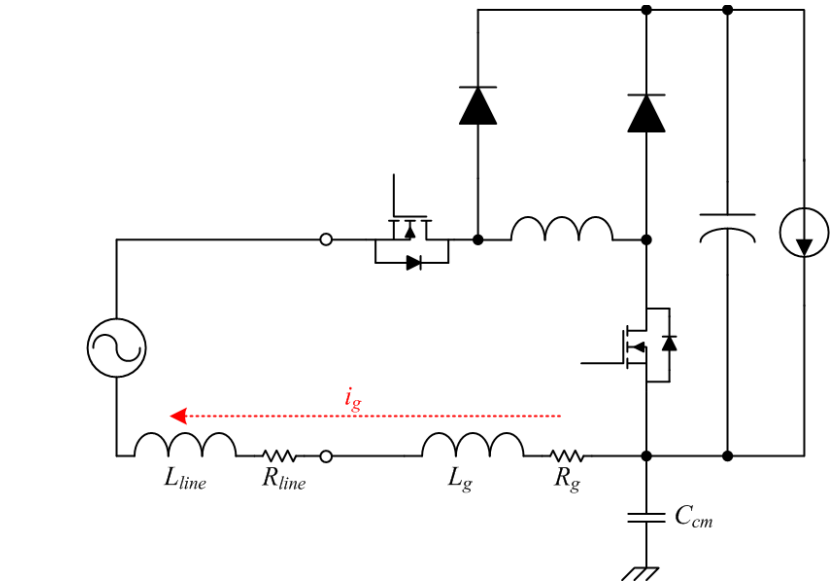


Fig. 3.18. Simulation waveform of the B3 rectifier with the resultant controller.

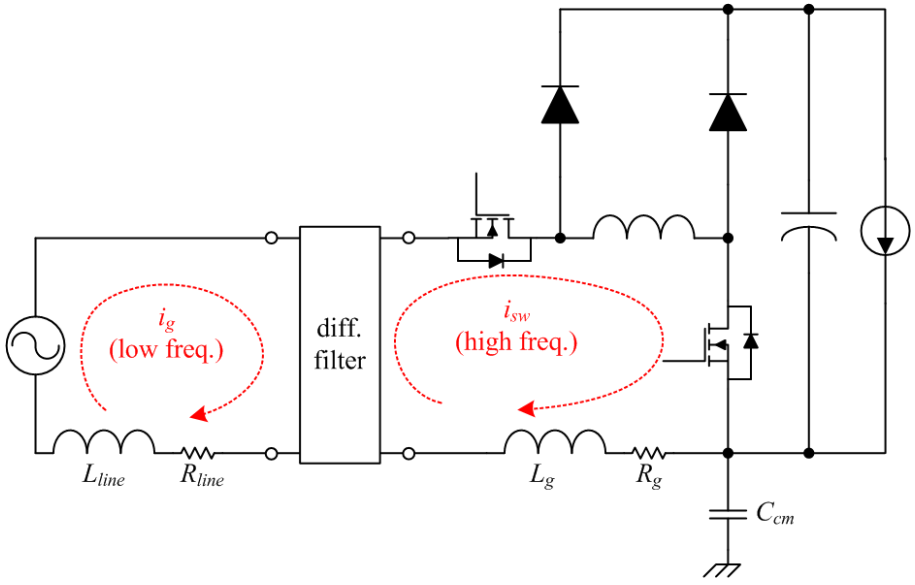
same with the case of Figs. 3.6 and 3.8. Comparing with Fig. 3.8, the line current with the unified compensators shows no current imbalance between the positive and negative half-line cycles. Output voltage ripple is also the similar level with those in Figs. 3.6(a) and 3.6(b). Besides, the line current ripple in the negative cycle is larger than that in the positive cycle. It is because the switch current is applied to the input filter during the negative line cycle, which has larger high frequency component than the inductor current.

3.4. Differential Input Filter Design

The B3 rectifier reduces the common mode current by inheriting the solid ground connection of the HA converter in theory. However, the conducted noise still exists in practically implemented B3 rectifier because the differential mode current flows through parasitic elements of the circuit. Fig. 3.19(a) shows the parasitic elements which contribute the conducted noise generation of the B3 rectifier. The parasitic inductance and resistance in the AC distribution line, L_{line} and R_{line}, and those in ground conductor of the B3 rectifier PCB, L_g and R_g, cause the EMI in the B3 rectifier. Though L_g and R_g may be minimized by optimizing the layouts of the PCB and carefully implementing the circuit, it is hard to control the line-related parasitic components such as L_{line} and R_{line}. Implying that there is no filter between the AC line and the B3 rectifier, the differential mode grid current i_g necessarily contains high frequency components due to the switching operation of the B3 rectifier. These components will be even larger when the rectifier operates in the buck-boost mode because the high-frequency switch current flows through the AC line. i_g in turn produces the high-frequency voltage across the parasitic elements and the common mode capacitance C_{cm}, which consequently



(a)



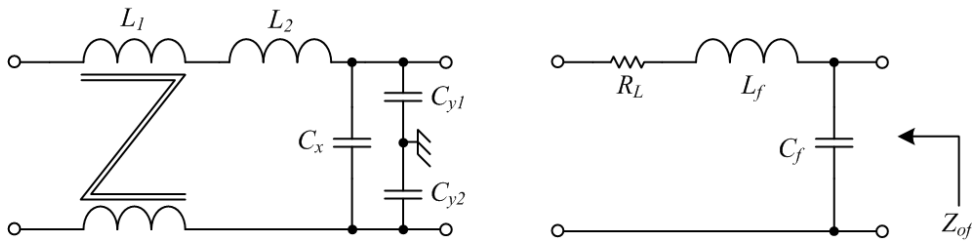
(b)

Fig. 3.19. (a) Conducted noise emission by parasitic elements and differential current in the B3 rectifier. (b) Separating currents by inserting a differential filter.

generates the conducted noise emission.

In this section, a differential mode input filter is designed to attenuate the switching frequency harmonics in the differential grid current and further reduce the conducted EMI in the B3 rectifier. Insertion of the differential filter will separate the high frequency current from the AC line as shown in Fig. 3.19(b). The differential input filter is much simple and compact comparing with the general AC line filter that contains both common and differential mode filter [50]. Fig. 3.20 shows the general structure of the second-order AC line filter and the second-order differential mode filter. In the general AC line filter in Fig. 3.20(a), the common mode current is suppressed by coupled inductor L_1, called as common mode choke inductor, and two capacitors, C_{y1} and C_{y2}, which are connected to the earth ground. The differential mode current is attenuated by inductor L_2 and capacitor C_x. L_2 is implemented not by the discrete element but by the leakage inductance of L_1 in many cases for simplicity of the filter.

In this dissertation, however, the differential input filter for the B3 rectifier is independently designed because the leakage inductance L_2 in Fig. 3.20(a) is not easy to control. The simple *L-C* filter shown in Fig. 3.20(b) is sufficient to attenuate the



(a) (b)

Fig. 3.20. (a) General AC line filter with choke inductor. (b) Simple *L-C* filter and its output impedance Z_{of}.

differential noise in the B3 rectifier. R_L is not a discrete element but the ESR of the filter inductor L_f.

To design the input filter in Fig. 3.20(b), the closed-loop input impedance of the B3 rectifier, Z_i, should be considered to sufficiently separate Z_i from the output impedance of the input filter, Z_{of}. Interaction between the filter and rectifier is then minimized and the rectifier can operate in desirable way [51]-[55]. Because the B3 rectifier keeps alternating its topological states, the input impedance of each topology should be separately derived.

The small signal block diagram for the boost mode operation in Fig. 3.21 additionally considers the two power stage transfer functions: open-loop audio-susceptibility G_{vg_b} and open-loop input voltage-to-inductor current G_{ivg_b} are defined in (3.28) and (3.29).

$$G_{vg\_b} = \frac{\hat{v}_O}{\hat{v}_g} = \frac{1}{D_b'} \frac{1}{1 + \frac{L}{D_b'^2 R} s + \frac{LC}{D_b'^2} s^2} \tag{3.28}$$

$$G_{ivg\_b} = \frac{\hat{i}_L}{\hat{v}_g} = \frac{1}{D_b'^2 R} \frac{1 + RCs}{1 + \frac{L}{D_b'^2 R} s + \frac{LC}{D_b'^2} s^2} \tag{3.29}$$

The closed-loop input admittance of the boost operation, Y_{i_b}, is expressed in (3.30). Appendix A.2 details the derivation process.

$$Y_{i\_b} = \frac{\hat{i}_L}{\hat{v}_g} = \frac{G_{ivg\_b} + G_{ivg\_b} G_{vd\_b} K_v G_v K_{ff\_b} G_c FM - G_{vg\_b} K_v G_v K_{ff\_b} G_c G_{id\_b} FM}{1 + G_{vd\_b} K_v G_v K_{ff\_b} G_c FM + K_i H_e G_c G_{id\_b} FM} \tag{3.30}$$

The small signal block diagram for the buck-boost mode operation in Fig. 3.22

employs four more power stage transfer functions G_{vg_bb}, G_{ivg_bb}, G_{igvg_bb}, and G_{igd_bb} shown from (3.31) to (3.34).

$$G_{vg\_bb} = \frac{\hat{v}_O}{\hat{v}_g} = \frac{D_{bb}}{D_{bb}'} \frac{1}{1 + \frac{L}{D_{bb}'^2 R} s + \frac{LC}{D_{bb}'^2} s^2} \tag{3.31}$$

$$G_{ivg\_bb} = \frac{\hat{i}_L}{\hat{v}_g} = \frac{D_{bb}}{D_{bb}'^2 R} \frac{1 + RCs}{1 + \frac{L}{D_{bb}'^2 R} s + \frac{LC}{D_{bb}'^2} s^2} \tag{3.32}$$

$$G_{igvg\_bb} = \frac{\hat{i}_g}{\hat{v}_g} = \frac{D_{bb}^2}{D_{bb}'^2 R} \frac{1 + RCs}{1 + \frac{L}{D_{bb}'^2 R} s + \frac{LC}{D_{bb}'^2} s^2} \tag{3.33}$$

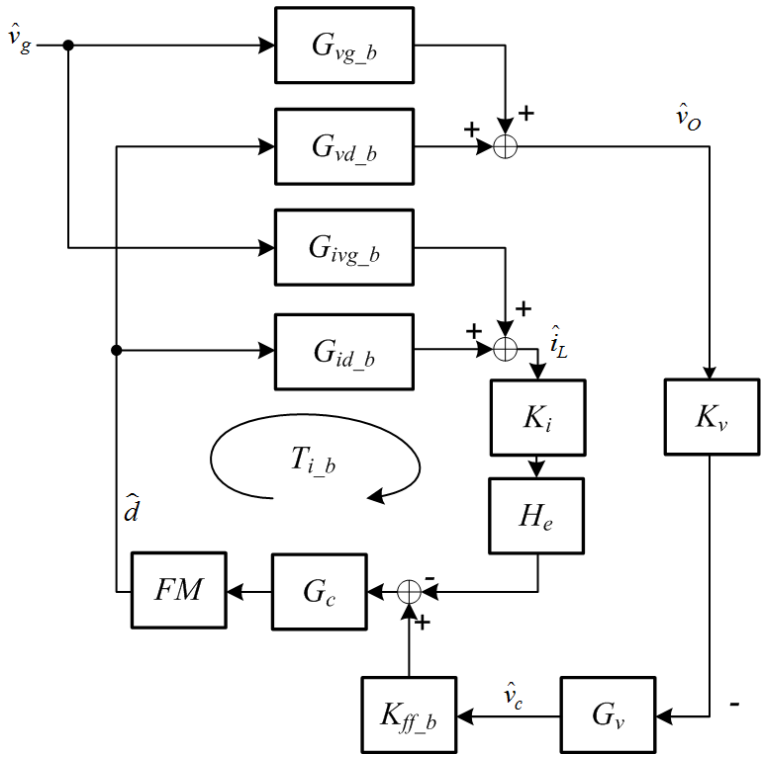


Fig. 3.21. Small signal block diagram for boost mode operation.

$$G_{igd\_b} = \frac{\hat{i}_g}{\hat{d}} = \frac{D_{bb}}{D_{bb}'} \frac{\frac{V_O}{D_{bb} D_{bb}'}\left(1 - \frac{D_{bb} L}{D_{bb}'^2 R} s\right)}{\left(\frac{R}{1+RCs}\right)\left(1 + \frac{L}{D_{bb}'^2 R} s + \frac{LC}{D_{bb}'^2} s^2\right)} \tag{3.34}$$

In the buck-boost mode, the B3 rectifier input current i_g is not the inductor current but the switch current, and one should introduce a new state variable, $\hat{i}_g$, the perturbation of the input current. For closed-loop input admittance of the buck-boost operation, Y_{i_bb}, the

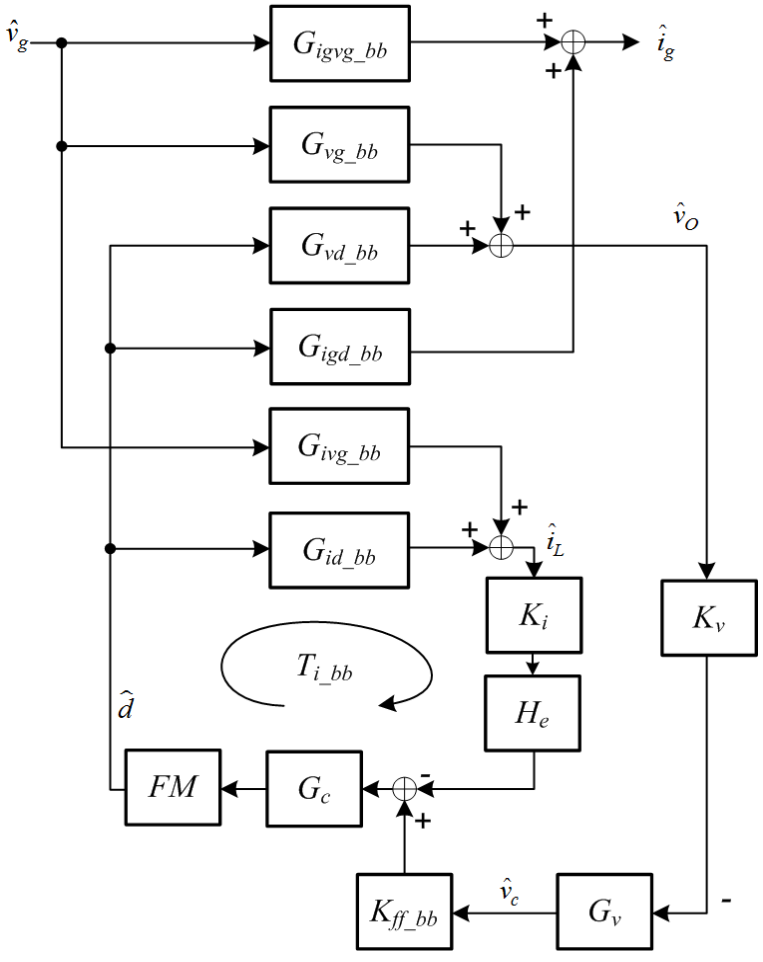


Fig. 3.22. Small signal block diagram for buck-boost mode operation.

block diagrams in Fig. 3.22 is rearranged as in Fig. A.3 to derive total gain from $\hat{v}_g$ to $\hat{i}_g$, and Y_{i_bb} is expressed in (3.35). The detailed derivation of (3.35) is presented in Appendix A.2.

$$Y_{i\_bb} = G_{igvg\_bb} - \frac{G_{vg\_bb}K_vG_vK_{ff\_bb}G_cG_{id\_bb}FM + G_{ivg\_bb}K_iH_eG_cG_{id\_bb}FM}{1 + G_{vd\_bb}K_vG_vK_{ff\_bb}G_cFM + G_{id\_bb}K_iH_eG_cFM} \tag{3.35}$$

Bode plot in Fig. 3.23 shows the reciprocals of Y_{i_b} and Y_{i_bb}, the closed-loop input impedances of the B3 rectifier. The impedance alters according to the equivalent topology of the rectifier. In this dissertation, the corner frequency of the input filter is designed to attenuate the fundamental component of switching frequency, 50 kHz, more than 80 dB. Considering the 50-mΩ stray resistance R_L in Fig. 3.20(b) as the damping

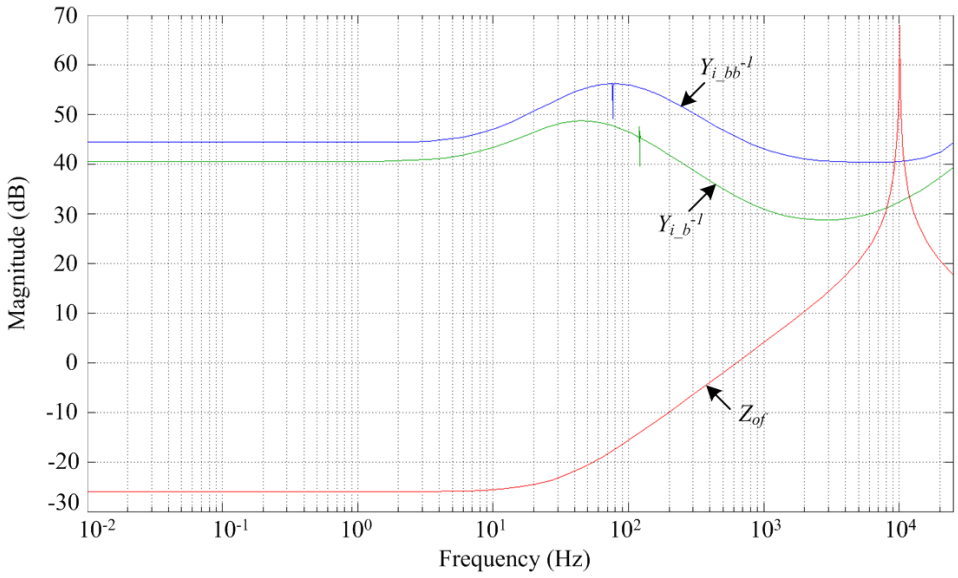


Fig. 3.23. Bode plot of $Y_{i\_b}^{-1}$, $Y_{i\_bb}^{-1}$, and $Z_{of.}$

factor, L_f and C_f are selected to be 250 μH and 1 μF. The output impedance of the input filter Z_{of}, in (3.36) is also plotted in Fig. 3.23.

$$Z_{of} = \frac{\left(R_L + sL_f\right)\frac{1}{sC_f}}{\left(R_L + sL_f\right) + \frac{1}{sC_f}} \tag{3.36}$$

There is not sufficient gap between the rectifier input impedances and Z_{of} in the vicinity of the filter corner frequency, but it is not always the case the overlap of the magnitude curves of the Bode plot predicts the system instability [56]. Defining the impedance ratio of the boost and the buck-boost operation T_{m_b} and T_{m_bb} as in (3.37) and (3.38), the curves of Nyquist plot in Fig. 3.24 do not include (-1, 0) point, which means that there is no system instability.

$$T_{m\_b} = \frac{Z_{of}}{Z_{i\_b}} \tag{3.37}$$

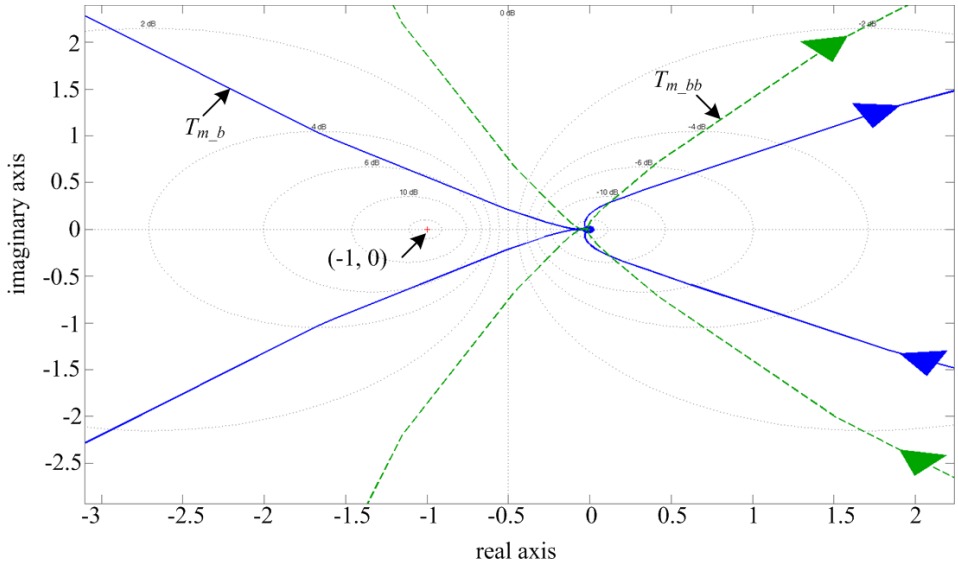


Fig. 3.24.Nyquist plot of T_{m_b} and T_{m_bb}.

$$T_{m\_bb} = \frac{Z_{of}}{Z_{i\_bb}} \tag{3.38}$$

In (3.37) and (3.38), input impedances Z_{i_b} and Z_{i_bb} are reciprocals of the input admittances Y_{i_b} and Y_{i_bb} respectively.

3.5. Experiments

3.5.1. Implementations

The B3 rectifier is implemented for experiment as designed in the previous sections. A four-layer PCB is used to build a 500 -W prototype rectifier. Fig. 3.25 illustrates the implementation of the B3 rectifier. Currents are sensed by Hall Effect sensors, and input and output voltages are sensed by inverting op-amp circuit and resistive voltage divider. Texas Instrument TMS320C28346 digital signal processor with external analog-to-digital converter (ADC) and digital-to-analog converter (DAC) is adopted as the controller of the proposed rectifier. An AC power supply Kikusui PCR2000L and an electric load Prodigit 3361F are used as the AC voltage source and the DC current sink. Part names and circuit parameters are summarized in the following:

1) D_1: DSEI12-10A (1,000 V, 12 A),

2) Q_2: STW13NK100Z (1,000 V, 13 A),

3) D_4: FSF10A60 (600 V, 10 A),

4) Q_6: STP11NM60FP (600 V, 11A),

5) L: 950 μH,

6) C_1-C_3: 220 μF/450V,

7) H_1-H_3: ACS756SCA,

8) R_1: 132.8 kΩ,

9) R_2, R_4: 820 Ω,

10) R_3: 265.6 kΩ,

11) A_1: LMV324,

12) v_g: 230 Vac, 60 Hz,

13) v_O: 400 Vdc,

14) V_{off}: 1.65 Vdc,

15) Switching frequency f_s: 50 kHz,

16) C_{cm}: 330 nF,

17) L_f: 250 μH,

18) R_L: 50 mΩ (stray resistance of L_f),

19) C_f: 1 μF (filter configurations including L_f, R_L, and C_f shown in Fig. 3.27).

For the buck-boost operation, D_1 and Q_2 are selected to have high voltage ratings such as 1,200 V and 1,000 V. v_{g_sen}, v_{O_sen}, i_{L_sen}, i_{ac_sen}, and i_{dc_sen} represent sampled value of the line voltage, output voltage, inductor current, line current, and output current from the power stage. They are input to the digital controller through the ADC and utilized to establish the system operation. i_{ac_sen} and i_{dc_sen} from H_1 and H_3 are for system protection and not directly related to the control of the rectifier. A photocoupler with auxiliary isolated DC-DC converter is used as the gate driver to turn on Q_2 during the positive half-line cycle and further improve the rectifier efficiency as explained in Section 3.2. Charge pump circuits or gate transformers may not be appropriate to turning on Q_2 for long time interval such as a half-line cycle.

To investigate the conducted noise of the prototype circuit, a common mode parasitic capacitor C_{cm} is intentionally implemented by a discrete film capacitor as well as LISN.

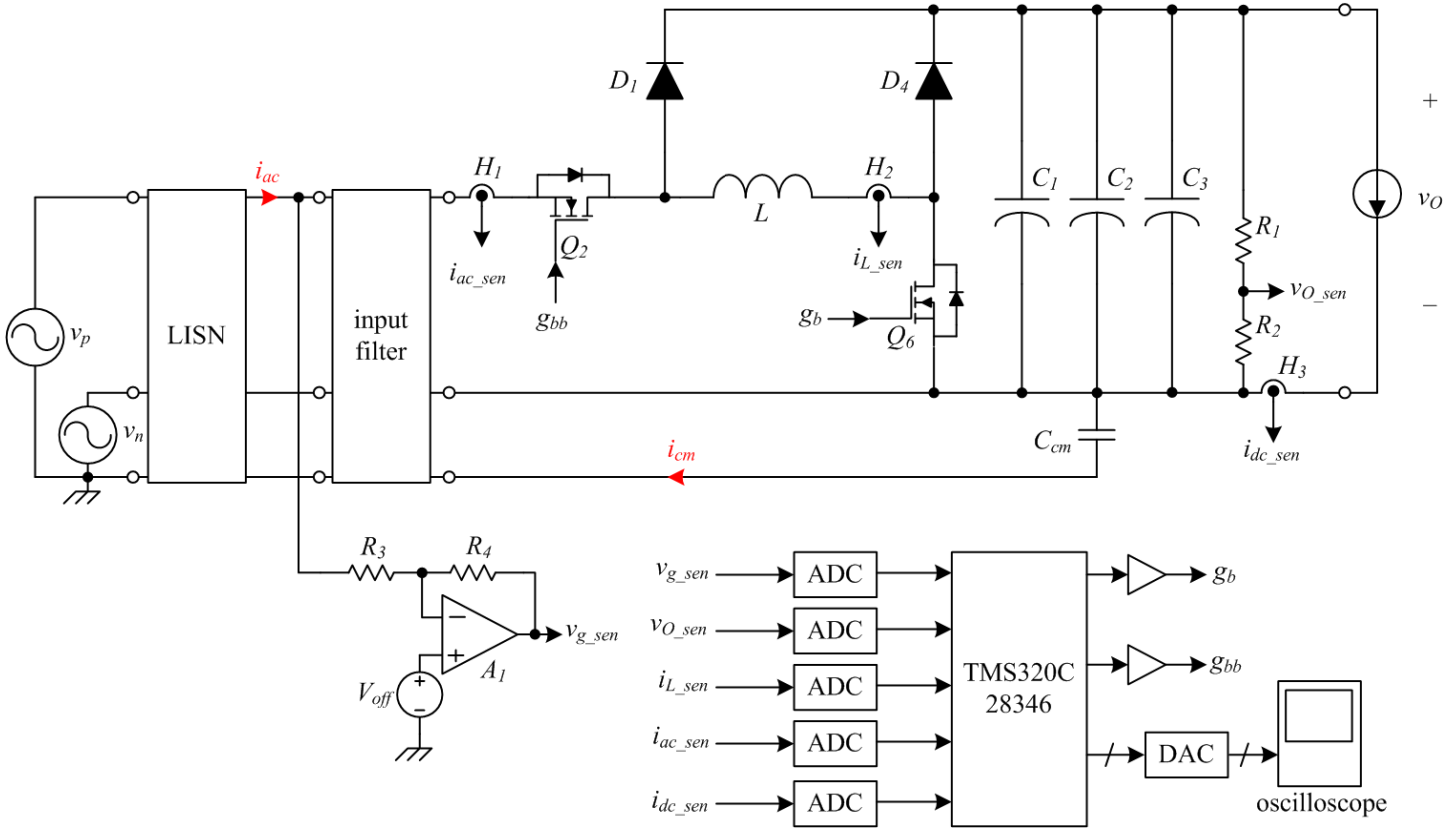


Fig. 3.25. Experimental setup of the proposed B3 rectifier.

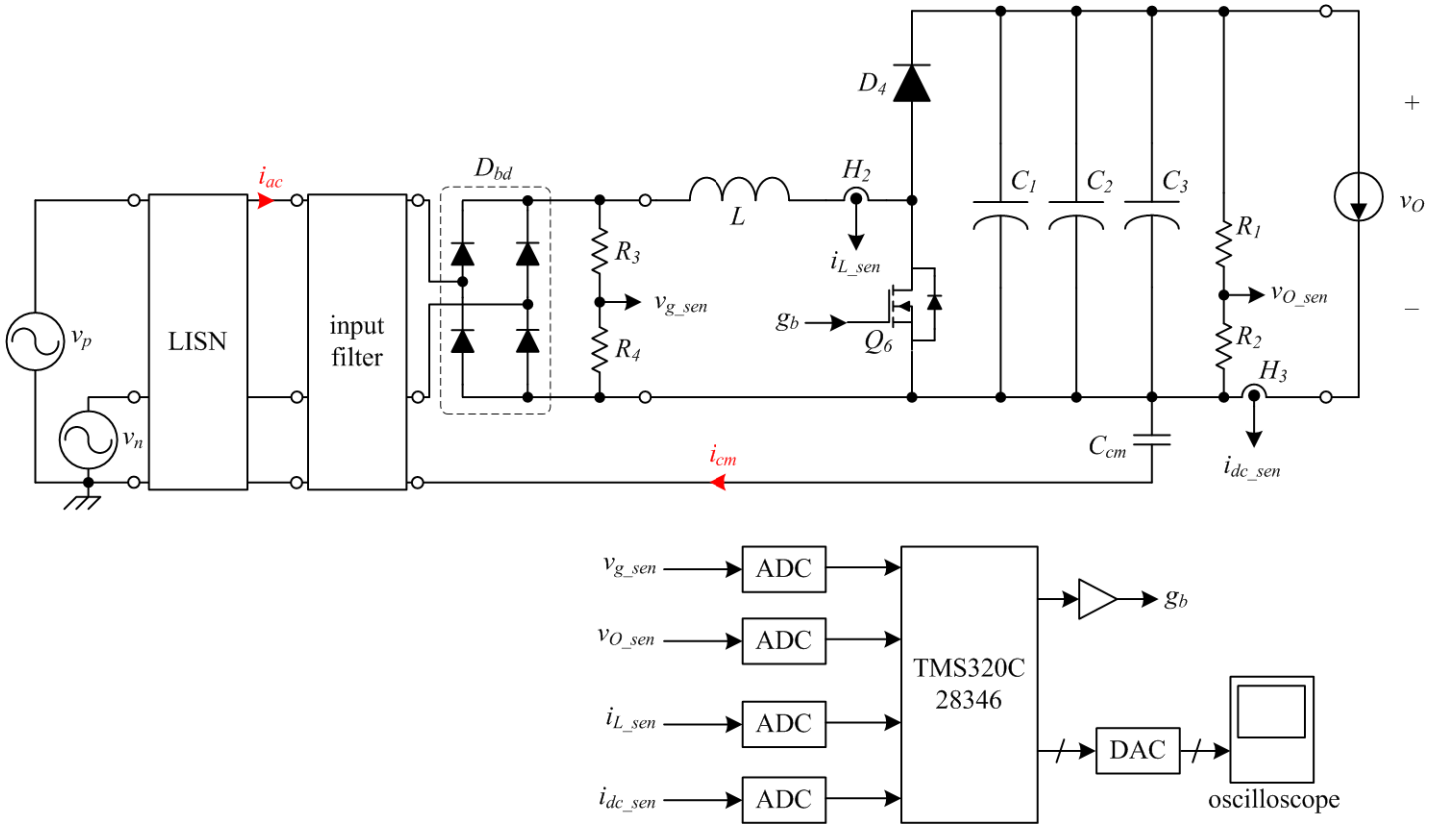


Fig. 3.26. Experimental setup of conventional boost rectifier with bridge diodes.

All the heat sinks attached to the semiconductor devices are not grounded to minimize their effect on the conducted noise [22]. All the prototype circuits are not shielded from radiated noise which may exist in the laboratory circumstance. The radiated noise may influence the conducted noise acquisition during the experiment, but it has little effect on comparing the conducted noises of the two rectifier circuits.

The conventional boost PFC rectifier with bridge diodes in Fig. 3.2(a) is also implemented for comparison as shown in Fig. 3.26. All the circuit components of the conventional rectifier implementation are same with those of the B3 rectifier except the addition of KBPC3506 as the bridge diodes D_{bd}. Semiconductor devices Q_6 and D_4 are same as Q_6 and D_4 in Fig. 3.25, STP11NM60FP and FSF10A60.

Same common mode and differential mode filters are applied to the two prototype circuits as their input filters for fair comparison. The input filter in Figs. 3.25 and 3.26 is configured as shown in Fig. 3.27. The common mode filter is realized by noise filter SN-E20H-CM manufactured by Fine Suntronix, and the differential one is as designed in Section 3.4.

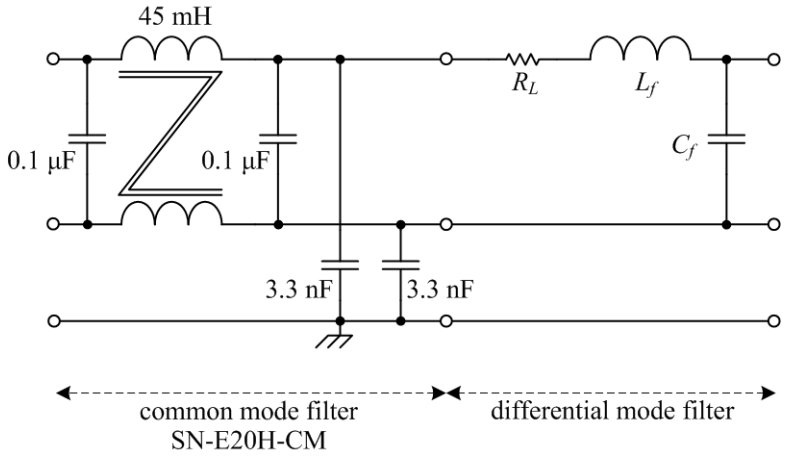
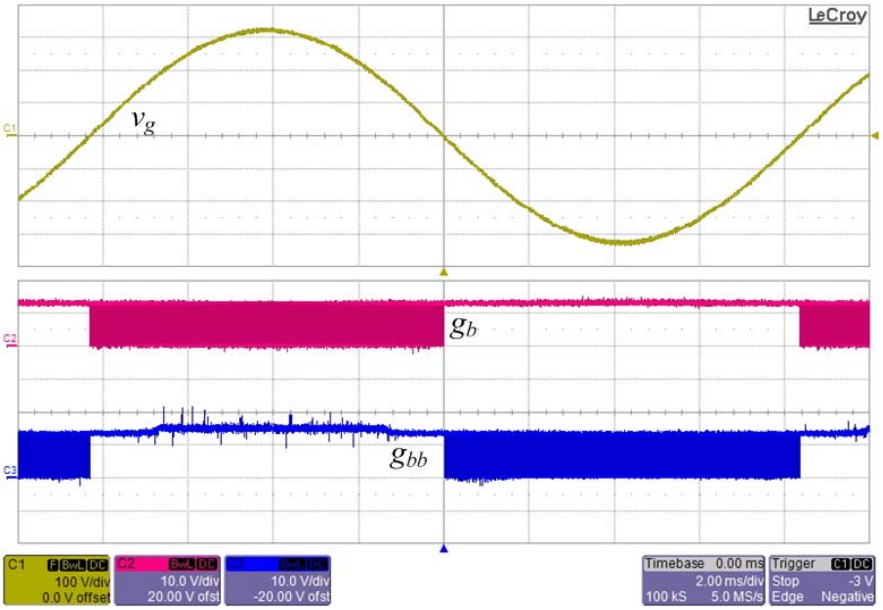
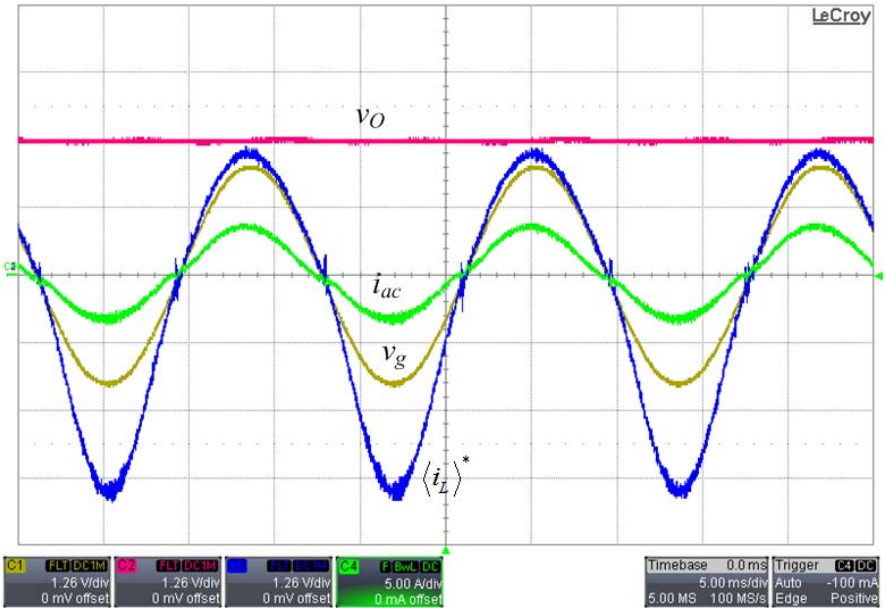


Fig. 3.27. Input filter commonly used in the prototype rectifiers



(a)



(b)

Fig. 3.28. Steady state waveforms of the proposed B3 rectifier when its output power is 500 W. (a) Gate signals for Q_2 and Q_6. (v_g: 100 V/div., g_b and g_{bb}: 10 V/div., 2 ms/div.) (b) Voltage and current waveforms. (v_g and v_O: 200 V/div., i_{ac}: 5 A/div., $\langle i_L \rangle^*$: 2 A/div., 5 ms/div.)

3.5.2. Results and Discussions

All the oscillograms in this section are captured by LeCroy Xi44. Fig. 3.28 shows the steady-state operation of the proposed B3 rectifier when its output power is 500 W. Fig. 3.28(a) illustrates the gate signal waveforms for Q_6 (g_b in channel 2) and Q_2 (g_{bb} in channel 3) of the B3 rectifier. Q_6 keeps switching and Q_2 is fully turned on in the positive line cycle, and Q_2 keeps switching and Q_6 is fully turned on in the negative line cycle in opposite. Fig. 3.28(b) shows the key currents and voltage waveforms. Channels 1, 2, and 3 are DAC outputs which stand for line voltage, output voltage, and reference inductor current respectively, and channel 4 is filtered line current measured by a current probe. The channel 3 waveform shows that the average inductor current of the buck-boost mode is controlled to be larger than that of the boost mode to obtain the power

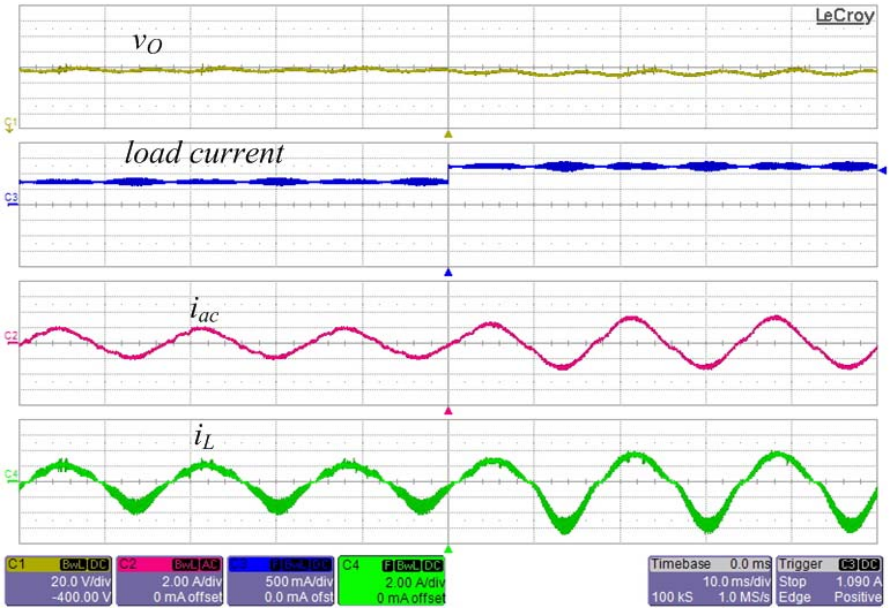


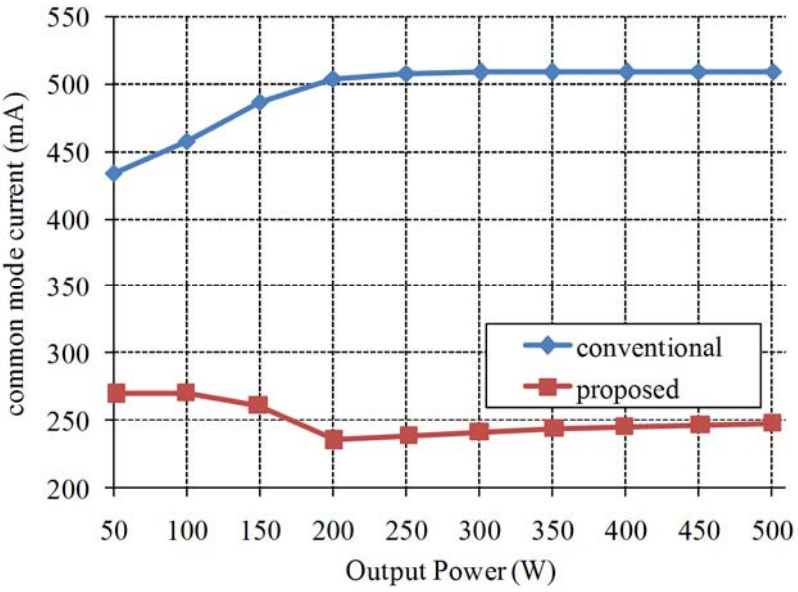
Fig. 3.29. Transient operation of the B3 rectifier when DC load current jumps from 0.75 A to 1.25 A. (v_O: 20 V/div. with −400 V offset, load current: 500 mA/div., i_{ac} and i_L: 2 A/div., 10 ms/div.)

balance between the positive and the negative half-line cycles as explained in Section 3.3.2. The filtered line current i_{ac} is following the sinusoid to minimize the line current distortion.

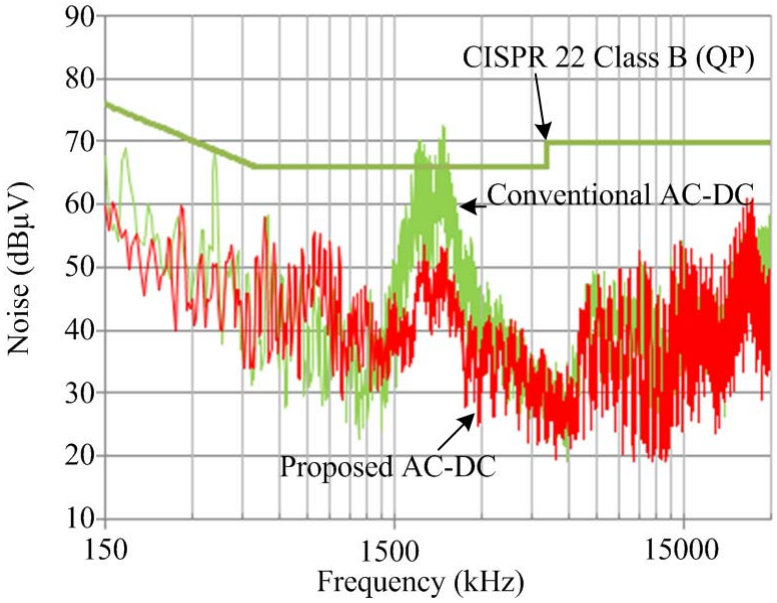
Transient operation of the B3 rectifier is shown in Fig. 3.29 when the load current abruptly jumps from 0.75 A to 1.25 A. The output voltage in channel 1 is measured by a voltage probe, and current in channels 2, 3, and 4 are by current probes. The controller regulates the converter such that the undershoot of v_O is smaller than 20 V and i_{ac} increases without any considerable distortion.

Common mode currents and noises of the proposed B3 rectifier and conventional counterparts are shown in Fig. 3.30. Fig. 3.30(a) presents the rms common mode current comparison between the two prototype rectifiers. The current through C_{cm} is directly measured by a current probe. The proposed rectifier shows smaller i_{cm} than the conventional counterpart. Fig. 3.30(b) displays the common mode noise measurements using the LISN and EMI receiver Agilent N9038A when the output power is 400 W. The noise is measured from 150 kHz to 30 MHz in the frequency domain. It shows that the noise levels of the proposed and conventional rectifiers in overall frequency range are similar with each other. It is because there are no high-frequency switching devices between the input and output terminal grounds in both circuits. However, the B3 rectifier shows smaller noise in the medium frequency region by 20 dBμV approximately and meets the CISPR 22 Class B regulation.

Theoretically, common mode characteristics of the two rectifiers, such as magnitude of i_{cm} or noise extracted from LISN, should be similar to each other. It is because the conventional boost rectifier in Fig. 3.26 always connects AC input and DC output



(a)



(b)

Fig. 3.30. Common mode characteristic comparison between the proposed B3 rectifier and its conventional counterpart: (a) rms common mode current and (b) common mode noise measured by LISN and EMI analyzer.

grounds through one of the bridge diodes regardless of the line voltage polarity. The switching frequency of the diodes is low, e.g., twice line frequency, and is supposed to have negligible effect on the common mode noise. In practice, however, the commutation of the bridge diodes seems to affect i_{cm} and common mode noise as well.

The connected ground of the B3 rectifier reduces differential mode noise as well as the common mode noise. The differential mode noises of the two rectifiers are also measured and compared as shown in Fig. 3.31. The proposed B3 rectifier demonstrates smaller differential noise than the conventional counterpart. This is because the current flows through the converter ground with parasitic resistance and inductance as explained in Section 3.4.

Fig. 3.32 shows efficiency curves of the two prototype circuits. The input power to the rectifier circuit is measured by a power analyzer Yokogawa WT210, and the output

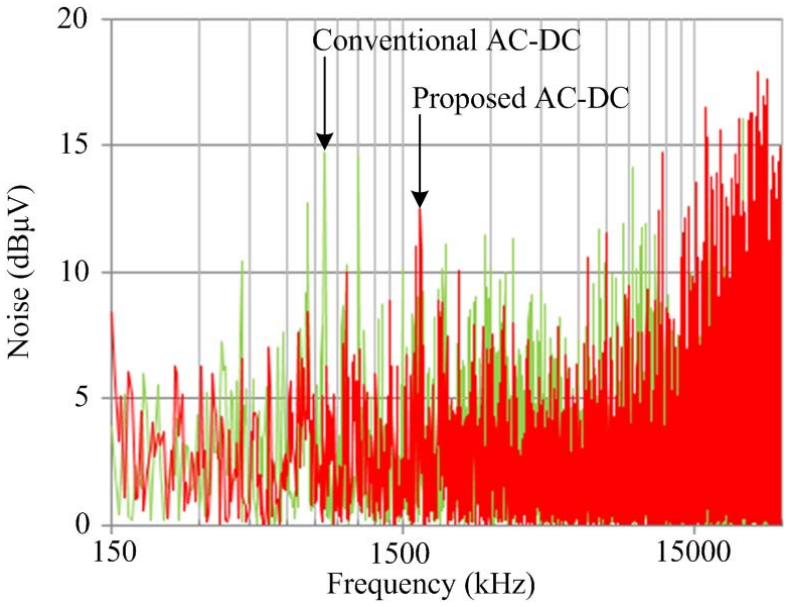


Fig. 3.31. Differential noise measured by LISN and EMI analyzer.

power from the rectifier is read from the electric load. The proposed B3 rectifier efficiency is similar but slightly lower than the conventional rectifier efficiency: by 1.2% at the worst case. The switching loss of Q_2 and D_1, which are responsible for the buck-boost operation in the B3 rectifier, and the additional conduction loss of fully turned-on switches (Q_2 for positive cycle and Q_6 for negative cycle) appear to be larger than the conduction losses of two diodes in KBPC3506; this loss may be the reason for the lower efficiency of the proposed rectifier.

Power loss of the semiconductor devices in full load operation is estimated to guide further efficiency improvement. Conduction losses in MOSFETs and diodes and switching loss in MOSFETs are calculated in Appendix A.3. According to the pie chart in Fig. 3.33 that shows the portion of various losses in the B3 rectifier, switches operate in the negative half-line cycle lose more power than those operate in the positive half-line cycle: for example, power losses in Q_2 such as P_{CQ2} and P_{SQ2} possess approximately 50% of total loss and it is larger than the losses in Q_6, the sum of P_{CQ6} and P_{SQ6} as 29%. It is because buck-boost operation gives higher voltage and current stresses to the semiconductor devices than boost operation. Therefore, carefully choosing the high-quality devices for Q_2 and D_1 is recommended to improve the rectifier efficiency. If the performance of the devices themselves is limited, adding soft-switching circuits to D_1 and Q_2 may reduce the switching losses and improve efficiency.

Though the proposed B3 rectifier shows lower efficiency than its conventional counterpart, it should be noted that there still exists the chance to improve the efficiency of the B3 rectifier. If the input filters are separately optimized for each rectifier topology, the filter for the B3 rectifier can use smaller components than that for the conventional

one, because the B3 rectifier demonstrates smaller common mode current and noise. As mentioned in Section 2.1, smaller filter inductor will show smaller core and conduction losses, which may help improve the B3 rectifier efficiency. Besides, reduction of filter size also matches to the recent circuit design trends that pursue the minimization of passive circuit components as mentioned in Section 1.1.

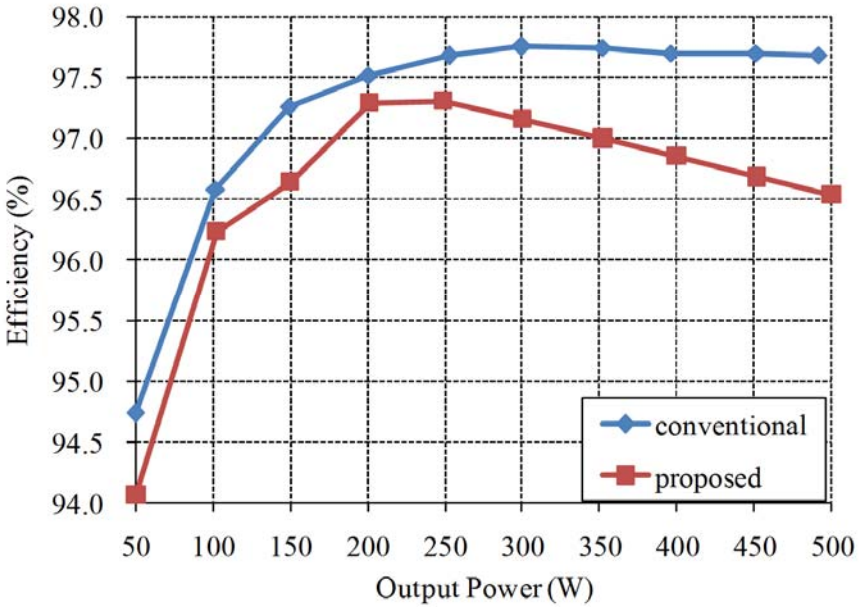


Fig. 3.32. Efficiency comparison between the proposed and conventional boost rectifier with bridge diodes.

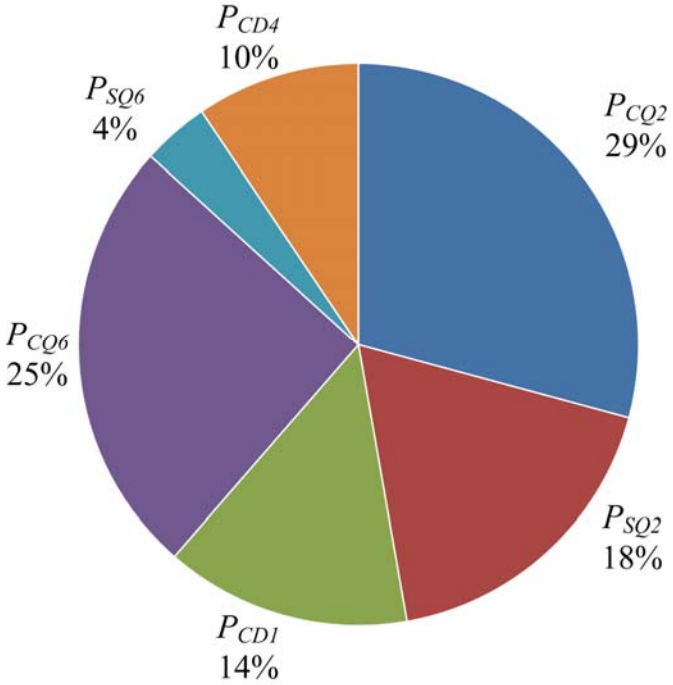


Fig. 3.33. Estimated power loss in switch devices at 500 -W operation.

4. B3 Inverter for DC-AC Conversion[2]

As a DC-AC inverter example of the HA converter, a new buck-buck-boost (B3) inverter is proposed for grid-connected PV inverter application. Similar with the B3 rectifier in Chapter 3, B3 inverter also suppresses the common mode EMI by inheriting the solid ground connection of the HA converter with simple circuit structure.

4.1. Advantage of B3 Inverter

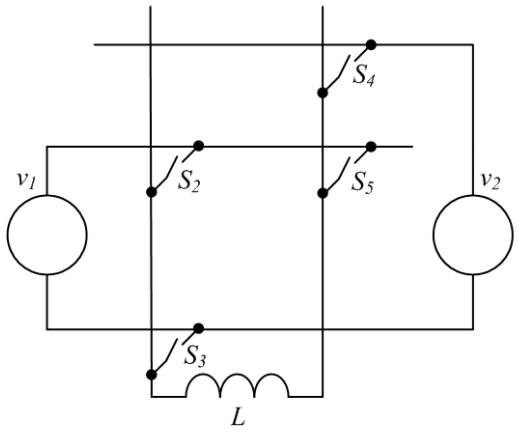
To cope with the alternating polarity of the AC line voltage, the proposed inverter emulates the operations of two DC-DC converter topologies. Fig. 4.1(a) shows the newly proposed B3 inverter from the HA converter by combining the two converters into one, the buck converter in Fig. 2.18 and the inverting buck-boost converter in Fig. 2.21. v_g and v_{pv} are the AC line voltage and PV voltage respectively. The proposed B3 inverter alternates its equivalent topology like the B3 rectifier in Chapter 3: the inverter works as the buck converter for positive AC line cycle, and operates as the inverting buck-boost converter for negative line cycle. As shown in Fig. 4.1(b), S_2, S_3, S_4, and S_5 are replaced by MOSFETs (or IGBTs) Q_2, Q_3, Q_4, and Q_5 for practical implementation.

The B3 inverter has simpler circuit structure than the conventional inverters. An example shown in Fig. 4.2 illustrates a flyback inverter which is widely used as low-power isolated PV inverter application. The flyback inverter controls its output current to be a rectified sinusoid, and the thyristors in unfolding stage switch according to the line frequency to change the direction of the output current. By employing the isolation transformer, the flyback inverter is free from the common mode noise problem, while its

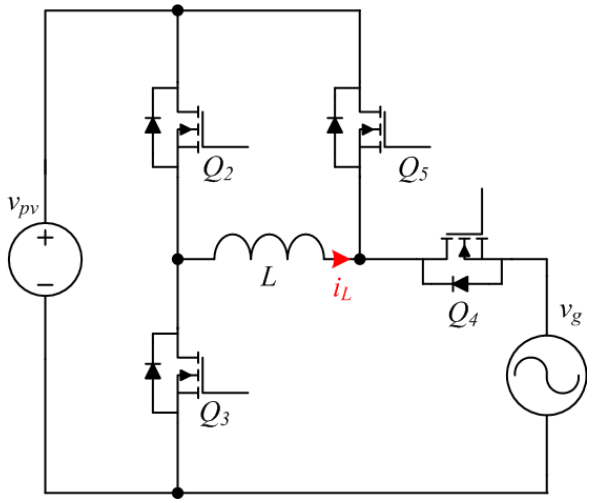
[2] The main idea of this Chapter is scheduled to be presented in the paper "A Low-Common Mode Noise and High-Efficiency Buck-Buck-Boost Inverter," IEEE Applied Power Electronics Conference, 2013.

volume and weight become larger and heavier and its efficiency is lower than the transformerless inverters [35]. The B3 inverter fully removes the unfolding stage to simplify the circuit structure, improve the efficiency, and possibly lower the cost. It is similar with the B3 rectifier which removes the bridge diodes of conventional circuit.

The structure of the B3 inverter is still competitive in the medium and high power



(a)



(b)

Fig. 4.1. (a) Switch selection for B3 inverter in the HA converter. (b) B3 inverter realized by practical switch devices (MOSFET in this case) and reference direction of inductor current.

application. It does not require any additional semiconductor devices comparing with the conventional H-bridge inverter in Fig. 2.7. Considering the refined H-bridge circuits to decrease the common mode noise such as HERIC [33], H5 [34], and H6 inverter [37], the B3 inverter needs even smaller number of switch devices. Figs. 2.9 and 2.10 show the H5 and HERIC inverter, which reduce the common mode current by employing additional one or two semiconductor switches. The H5 and HERIC inverters utilize hybrid and unipolar PWM techniques respectively and separate the PV panel and AC line by operating additional switches in their zero vector state: S_5 open in H5 inverter and S_5 and S_6 closed in HERIC inverter. Detailed explanation of the H5 and HERIC inverter is in Appendix A.4. Compared with these refined H-bridge circuits, the proposed B3 inverter uses less number of switches and thus has simpler circuit structure.

In addition to its circuit simplicity, the B3 inverter is robust to the conducted noise emission because it features low common mode current by inheriting the solid

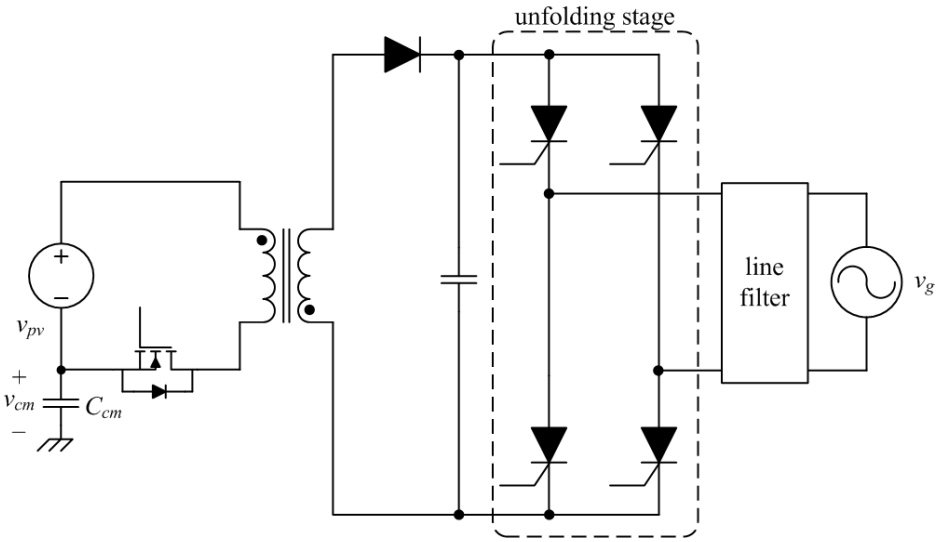


Fig. 4.2. A conventional low-power flyback inverter with thyristor unfolding stage.

connection between the input and output grounds of the HA converter. Whether the B3 inverter is in the buck or inverted buck-boost mode, the ground connection is not intervened by the switching operation of the switch devices.

4.2. Operation

Specifically, the B3 inverter shows four topological states during the operation as

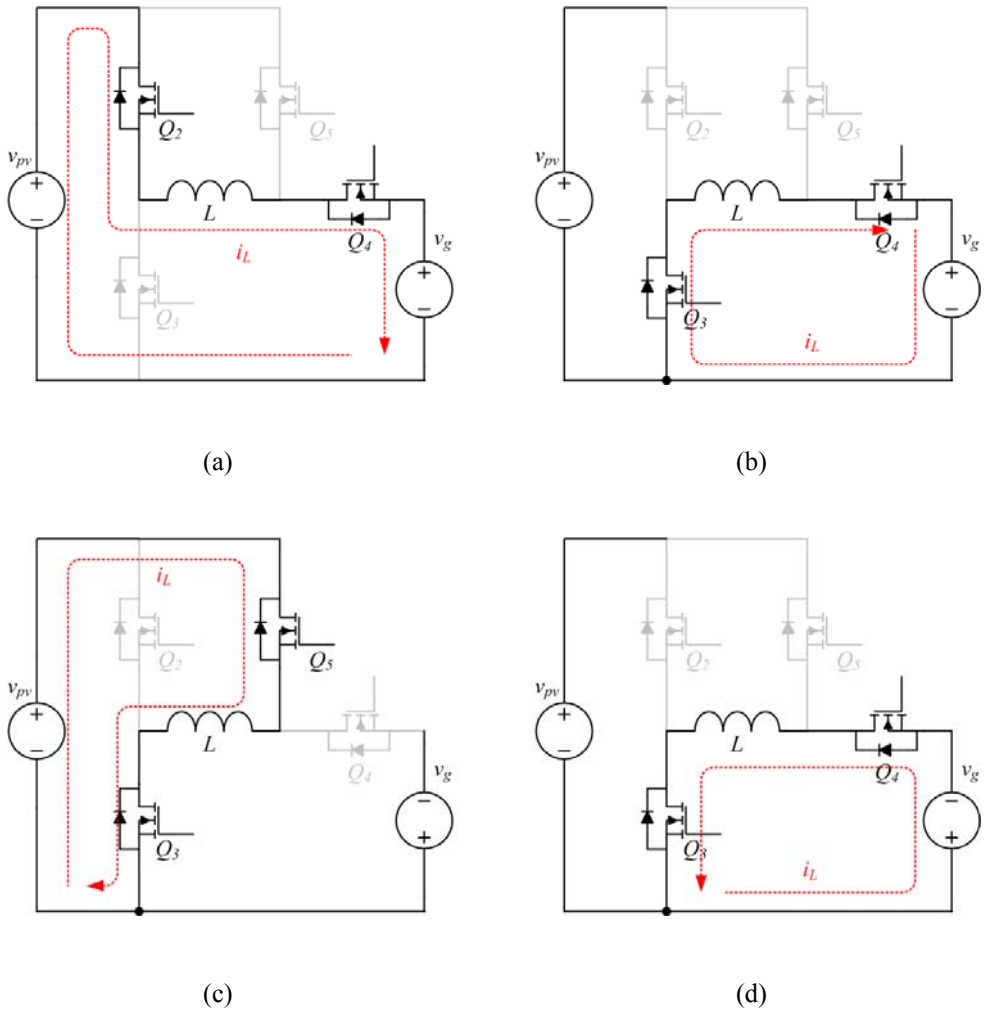


Fig. 4.3. Four operational states of the B3 inverter: (a) state 1, (b) state 2, (c) state 3, and (d) state 4.

illustrated in Fig. 4.3, assuming that the inductor current is in continuous conduction mode and the PV panel voltage v_{pv} is always larger than the line voltage v_g. The direction of the inductor current i_L is expressed by the arrows in Fig. 4.3. States 1 and 2 occur during the positive half-line cycle ($v_g > 0$), and states 3 and 4 during the negative half-line cycle ($v_g < 0$). In state 1, both MOSFETs Q_2 and Q_4 are on, and i_L increases by the positive voltage source v_{pv} as shown in Fig. 4.3(a). Fig. 4.3(b) shows that Q_2 turns off and Q_3 turns on in state 2. Q_4 is always turned on when $v_g > 0$. The operation of the B3 inverter in states 1 and 2 is the same with that of the buck converter. In these states, Q_5 does not participate in the operation because it is turned off and its body diode is reverse-biased. When v_g becomes negative, states 3 and 4 alternate. In state 3 as in Fig. 4.3(c), both switches Q_3 and Q_5 are on to increase i_L as in state 1. Q_5 goes off in state 4 and i_L flows through Q_4 as illustrated in Fig. 4.3(d). Q_3 is always turned on when $v_g < 0$. The B3 inverter in states 3 and 4 simulates the operation of the inverting buck-boost converter. The directions of i_L in state 2 and 4 are opposite to each other according to the polarity of v_g. In the states 3 and 4, Q_2 does not participate in the operation because it is always turned off.

The on/off state of Q_3 does not affect the inverter operation during the positive line cycle. However, it is recommended operating Q_3 complementary to Q_2 and letting i_L flows through the junction of Q_3 when Q_3 is a MOSFET because it decreases the conduction loss like synchronous rectifier. Similar with Q_3, the on/off state of Q_4 in states 3 and 4 does not affect the inverter operation during the negative half-line cycle. However, if Q_4 is the MOSFET, operating Q_4 complementary to Q_5 and steering i_L into the junction of Q_4 is also desirable to decrease the conduction loss. Fig. 4.4 summarizes

the gate drive signals of switches within a line cycle when the active switches of the B3 inverter are MOSFETs.

4.3. Control

4.3.1. Inductor Current Reference Calculation

The B3 inverter utilizes average current mode control [45], [46] to shape the AC line current and minimize its distortion. However, relationship between the average line current and average inductor current per switching cycle alternates according to the equivalent topology of the inverter. In other words, the relationship between the average inductor and average line current when the inverter operates as the buck converter is

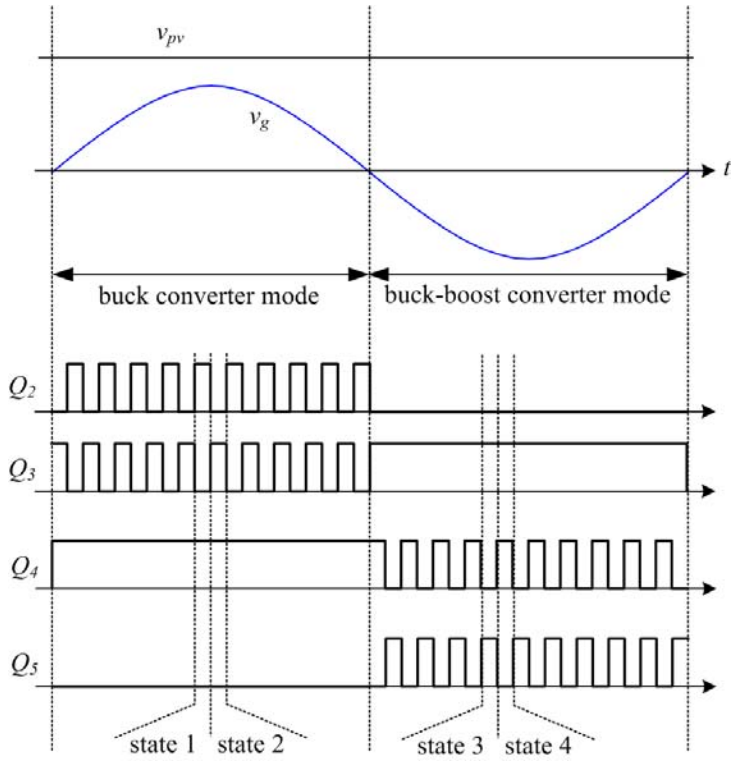


Fig. 4.4. Gate signals of B3 inverter during a line cycle when active switches are MOSFETs.

different from that when the inverter works as the buck-boost converter. Thus the controller that is only optimized for the buck and buck-boost converter dynamics and has no reference inductor current correction does not guarantee the proper operation of the B3 inverter. It may unbalance output power between the positive and negative half-line cycles to induce undesirable stress on the semiconductor devices, inverter efficiency degradation, and loss of maximum power point tracking (MPPT) of PV panel. Proper correction factor should be therefore included in the reference current calculation to properly shape and balance the line current regardless of the equivalent topologies of the B3 inverter.

Considering the reference direction of the inductor current in Fig. 4.1(b), the average inductor current in a unit switching cycle $\langle i_L \rangle$ defined in (3.1) is equal to the average line current when $v_g > 0$ because the inductor is series-connected to the AC line through the fully turned-on switch Q_4. Assuming that the inverter is in the steady state, the reference inductor current of the buck converter mode $\langle i_{Lbuck} \rangle^*$ should be a sine wave to shape the line current into the same sine wave that contains negligible harmonic components as shown in (4.1).

$$\langle i_{Lbuck} \rangle^* = \langle i_L \rangle = I_m \sin \omega t \tag{4.1}$$

In (4.1), ω is angular frequency of the AC line voltage and I_m is the maximum line current in a half-line cycle which is determined by the PV panel condition and MPPT algorithm.

For the buck-boost converter operation case when v_g is negative or $\pi \le \omega t < 2\pi$, on the other hand, the average line current is not equal to the average inductor current

but equal to the average switch current. The average switch current of Q_4 per switching period $\langle i_{Q4} \rangle$ is dependent on the duty cycle ratio d_{bb} in the buck-boost mode as defined in (4.2) and proportional to the sinusoid as expressed in (4.3).

$$d_{bb} = \frac{|v_g|}{v_{pv} + |v_g|} \tag{4.2}$$

$$\langle i_{Q4} \rangle = \langle i_L \rangle (1 - d_{bb}) = I_m \sin \omega t \tag{4.3}$$

Considering that the AC line voltage is an ideal sinusoid as in (4.4) where V_{gmax} is the maximum input voltage in a line cycle, the reference inductor current of the buck-boost converter mode $\langle i_{Lbb} \rangle^*$ is derived in (4.5).

$$v_g = V_{g\max} \sin \omega t \tag{4.4}$$

$$\langle i_{Lbb} \rangle^* = \langle i_L \rangle = \frac{I_m \sin \omega t}{1 - d_{bb}} = \left(1 + \frac{|V_{g\max} \sin \omega t|}{v_{pv}} \right) \langle i_{Lbuck} \rangle^* \tag{4.5}$$

Comparing (4.1) and (4.5), one can notice that a correction factor, the term in the parentheses in (4.5), should be multiplied to $\langle i_{Lbuck} \rangle^*$ to yield $\langle i_{Lbb} \rangle^*$. If the current references for each topological state do not obey the relation defined in (4.5), the power imbalance will occur. Therefore, multiplication of the correction factor to the inductor current reference should be included in the B3 inverter controller to avoid the undesirable power imbalance. Fig. 4.5 compares the magnitudes of $\langle i_{Lbb} \rangle^*$ with the normalized $\langle i_{Lbuck} \rangle^*$ in a line cycle for various line voltages, assuming that v_g is pure sine wave and v_{pv} is 400 Vdc.

It is interesting to notice that the curves in Fig. 4.5 are exactly same with those in Fig. 3.9. It is because the B3 inverter is essentially the same topology with the B3 rectifier. Because the HA converter is bilaterally symmetric, the reference inductor current does not change regardless of the direction of the power flow. The symmetry of the HA converter is articulated in Chapter 5.

Fig. 4.6 shows the control block diagram that applies the proper correction to achieve balanced line current. In Fig. 4.6, a PLL is applied to obtain noise-free sine wave which is synchronized with the AC line voltage. H_c represents a unified current compensator which is designed in the next section. θ and *pol* are the phase angle and polarity of the line voltage. An MPPT algorithm calculates I_m to extract the maximum power from the PV panel, and the controller in turn generates the inductor current reference using I_m. Unlike in the B3 rectifier in Chapter 3, the inductor current is not

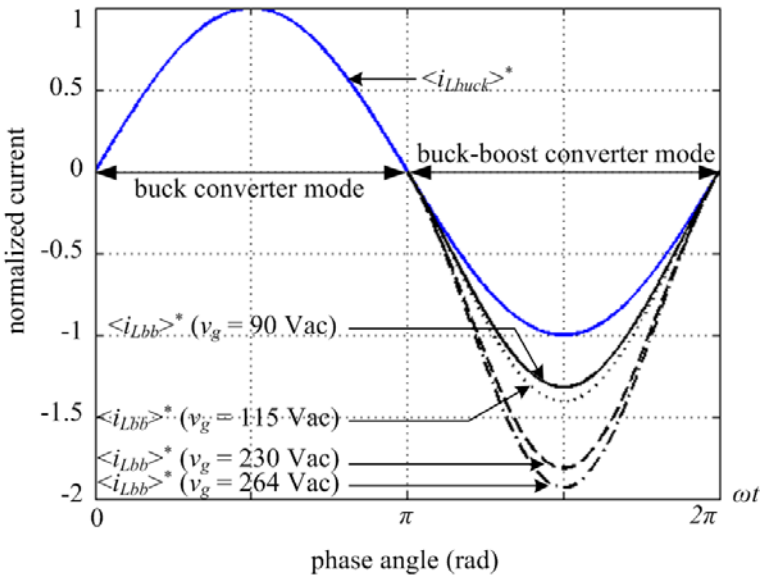


Fig. 4.5. Comparison of inductor current references of the B3 inverter in the positive and negative line cycles for various line voltages.

unidirectional in the B3 inverter, thus the polarity of the compensator should be changed in accordance with the sign of line voltage to maintain the negative feedback loop. The computation blocks in the broken-line box represent the correction factor, $1+\frac{\left|V_{g\max}\sin\omega t\right|}{v_{pv}}$. The controller balances the positive and negative line current thanks to these blocks.

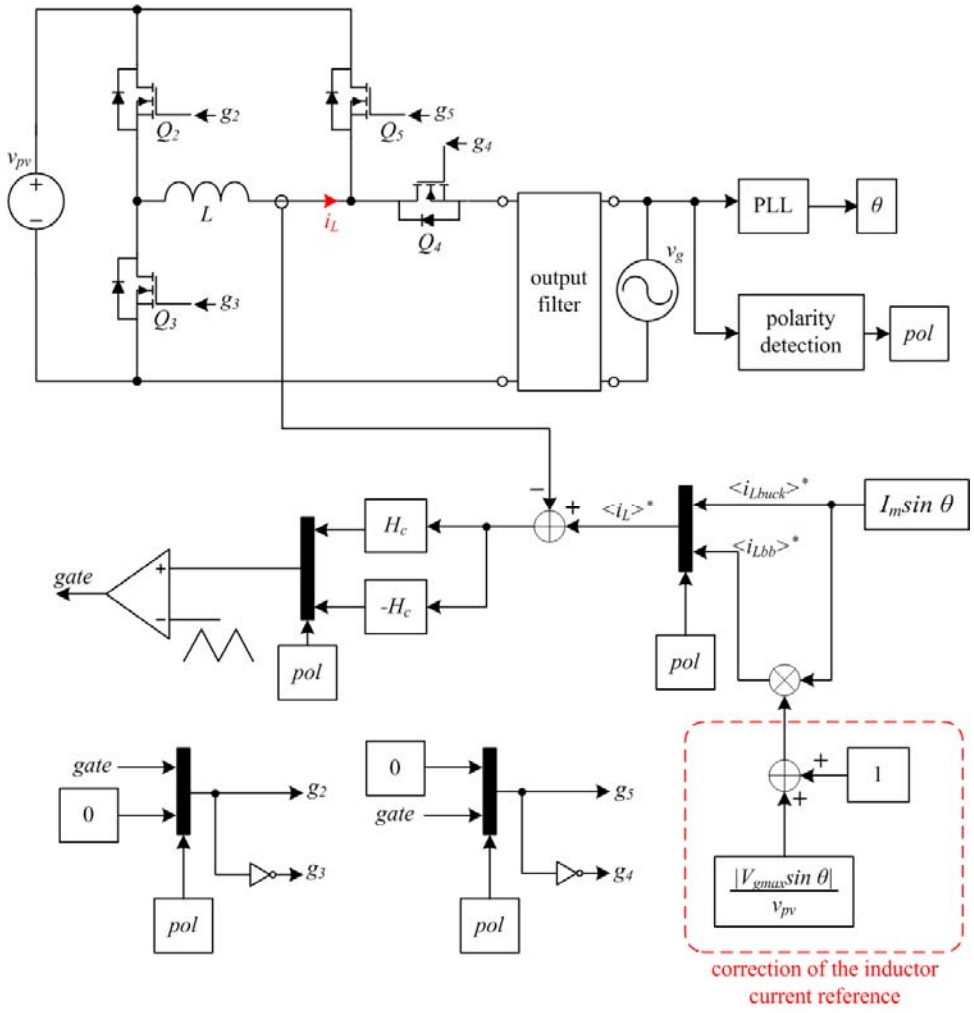


Fig. 4.6. Control block diagram with the reference correction to achieve balanced line input current for the B3 inverter.

Similar with the discussion in Section 3.3.2, using the PLL and injecting sinusoidal current to the grid is controversial when the line voltage is not a pure sine wave but a distorted one. Controlling the output current of the inverter to have higher harmonics as well as the fundamental components may help reduce rms current of the inverter and imaginary power from the utility in some cases. However, present standards on the injected current such as [17] and [19] do not have any regulation when the line voltage is distorted, because it applies when the line voltage has negligible distortion. In this dissertation, the PLL is used for the present to inject sinusoidal current to the grid whether the line voltage is distorted or not.

4.3.2. Compensator Design

A properly designed compensator is essential for the proposed B3 inverter to achieve good performance. The B3 inverter power stage circuit parameters for the compensator design are listed below.

1) inductance L: 4 mH,

2) switching frequency f_s: 20 kHz,

3) AC line voltage v_g: 230 Vac, 60 Hz,

4) PV voltage v_{pv}: 400 Vdc.

The PV panel can be modeled in various ways. Fig. 4.7 shows current-voltage characteristic curves of the typical PV panel for various operation conditions. A dot on each curve represents the maximum power point, and broken and solid lines indicate the curve deviations due to the temperature and irradiation increase. Assuming that the MPPT algorithm tracks the maximum output power and consequently the maximum output current of the PV panel [8]-[9], the PV voltage deviates according to the change

of operating conditions of the panel. Generally, dynamic of the PV panel is relatively slow because the temperature or irradiation does not change quickly, and the PV voltage changes slower than the instantaneous AC line voltage. In this dissertation, the PV panel is replaced by a DC voltage source in the small signal analysis for simple modeling, and by a DC power supply for experiment.

Fig. 4.8 shows the equivalent circuits of the B3 inverter in each topological state. Being different from the models of conventional DC-DC converters, the circuits in Fig. 4.8 have the voltage source at their output terminal instead of the output capacitor and load. The magnitude of the voltage source at the output terminal is equal to the rms AC line voltage as Huliehel's approximation [48]. The power processed by general DC-DC converter or AC-DC rectifier is determined by the load resistance, and the output voltage is considered as the system output which should be controlled in the small signal analysis. In the grid-connected inverter system, however, the power handled by the inverter is solely determined by the operational condition of the PV panel. The output voltage of the inverter is therefore considered as system input in the small signal

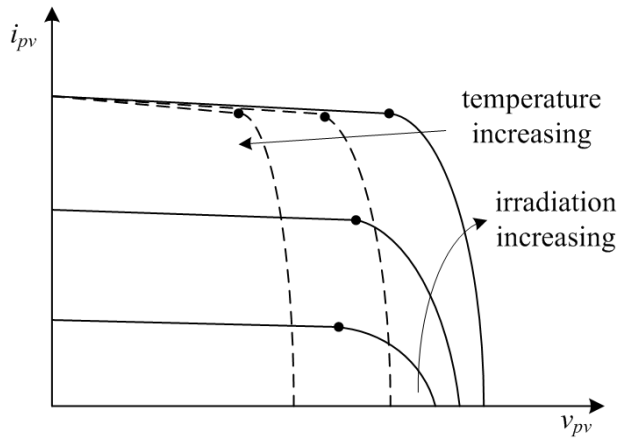


Fig. 4.7. Typical current-voltage characteristic curves of PV panel.

analysis, because it is not controlled but determined by the AC line.

The B3 inverter with the PV panel employs an average current mode single loop control. Small signal model for the B3 inverter is achieved in advance of the compensator design. The power stage transfer functions of B3 inverter are reduced to the first order model because the circuits in Fig. 4.8 are effectively single series inductance filters. Defining s is complex number in Laplace domain, the open-loop transfer functions of the B3 inverter in the buck mode operation is shown in (4.6) and (4.7).

$$H_{id\_buck} = \frac{\hat{i}_L}{\hat{d}} = \frac{V_{PV}}{sL} \tag{4.6}$$

$$H_{ivg\_buck} = \frac{\hat{i}_L}{\hat{v}_g} = -\frac{1}{sL} \tag{4.7}$$

The open-loop transfer functions when the B3 inverter works as the buck-boost converter are shown in (4.8) and (4.9).

$$H_{id\_bb} = \frac{V_{PV} + V_g}{sL} \tag{4.8}$$

$$H_{ivg\_bb} = -\frac{D_{bb}'}{sL} \tag{4.9}$$

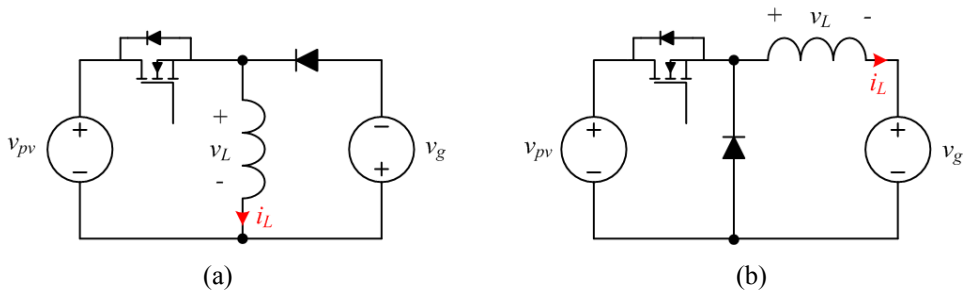


Fig. 4.8. Equivalent circuits of the B3 inverter for (a) negative and (b) positive line cycle.

From (4.6) to (4.9), H_{id} and H_{ivg} represent open-loop transfer function from duty cycle to inductor current and from line voltage to inductor current respectively. Suffices $_{buck}$ and $_{bb}$ indicate that the transfer function is for the buck and buck-boost converter operation. V_{PV}, V_g, and L are the DC component of the PV voltage, rms AC line voltage, and inductance. D_{bb}' is DC component of the complementary duty cycle in the buck-boost operation as defined in (4.10).

$$D_{bb}' = \frac{V_{PV}}{V_{PV} + V_g} \tag{4.10}$$

The open-loop transfer functions of the B3 inverter are the same with the general DC-DC converter transfer functions approximated in the low frequency region [46], [58]. Fig. 4.9 shows the Bode plot of H_{id_buck} and H_{id_bb} up to the half of switching frequency, 10 kHz.

To control the power that the B3 inverter handles, i.e., to track the maximum power

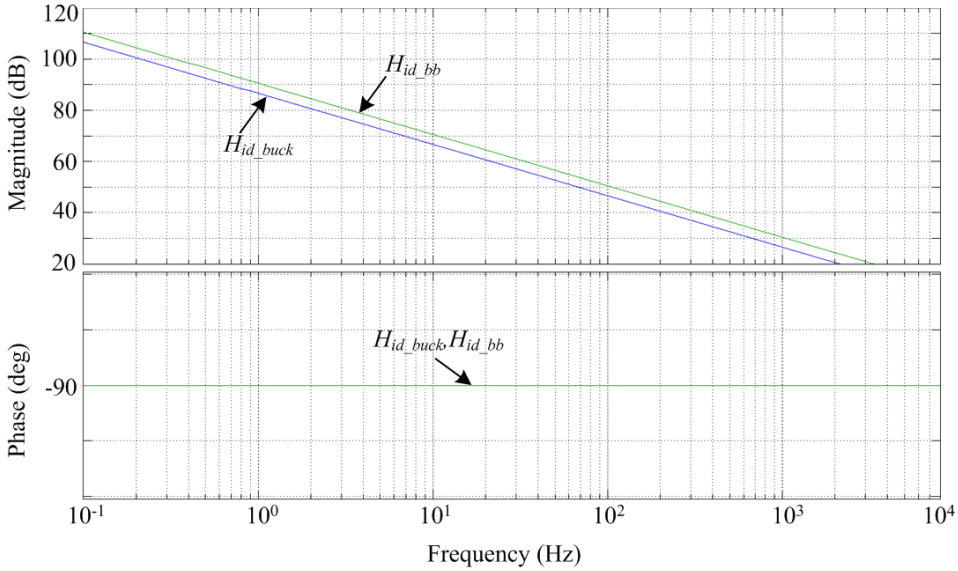


Fig. 4.9. Bode plot of H_{id_buck} and H_{id_bb} up to the half of the switching frequency, 10 kHz.

point of the PV panel according to the MPPT algorithm, a single loop control of the inductor current is sufficient as presented in Fig. 4.10. A unified controller for B3 inverter H_c, which is compatible for both the buck and the buck-boost operation, is designed to have only a proportional gain to guarantee the 90-degree phase margin of loop gains. Eqs. (4.11) and (4.12) express the loop gains T_{buck} and T_{bb}.

$$T_{buck} = H_{id\_buck} K_i H_c FM \tag{4.11}$$

$$T_{bb} = H_{id\_bb} K_i H_c FM \tag{4.12}$$

Considering that the inductor current sensing gain K_i is unity and the modulator gain FM is 7,500, H_c is selected to be 2,500 to make the bandwidth of the closed-loop gain to be approximately 5 kHz. From Fig. 4.11, the buck mode operation achieves 4.2 kHz bandwidth, and the buck-boost mode operation obtains 6.68 kHz bandwidth.

Similar with the B3 rectifier control design case, two separate current loop

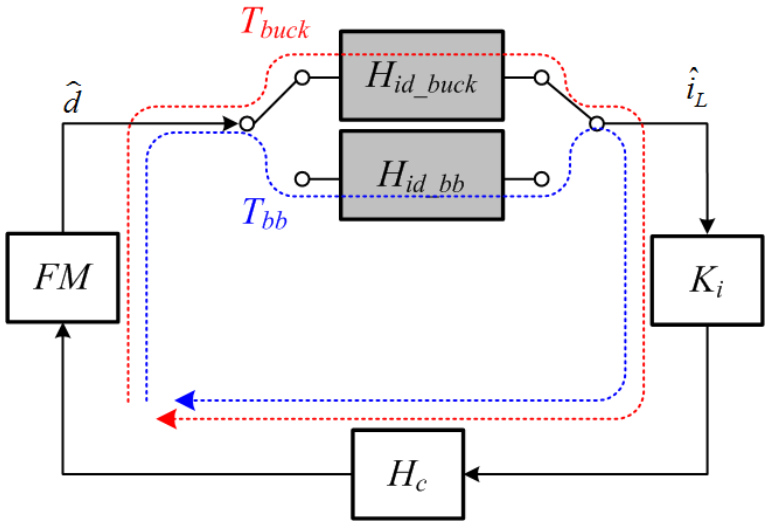


Fig. 4.10. Control block diagram of the single loop controlled B3 inverter.

compensators, the one for the buck operation and the other for the buck-boost operation, may be designed and adaptively selected according to the polarity of the AC line voltage. However, the effect of the adaptive control with the two compensators will be negligible comparing with that of the single current loop compensator because the loop gains T_{buck} and T_{bb} are similar with each other and their bandwidths are sufficiently higher than twice line frequency.

PSIM simulation waveform of the B3 inverter with the designed compensator is illustrated in Fig. 4.12. The B3 inverter delivers 650 W to the AC line at the beginning in the simulation. I_m steps at time 0.03 seconds from 4 to 2 A assuming the operating condition of the PV abruptly changes. The B3 inverter delivers 325 W after the reference change. The inductor current in Fig. 4.12 follows the reference within a short time, i.e., within a half-line cycle, and the line current may be distorted temporarily as well. In practice, however, the step change such as shown in the simulation hardly occurs

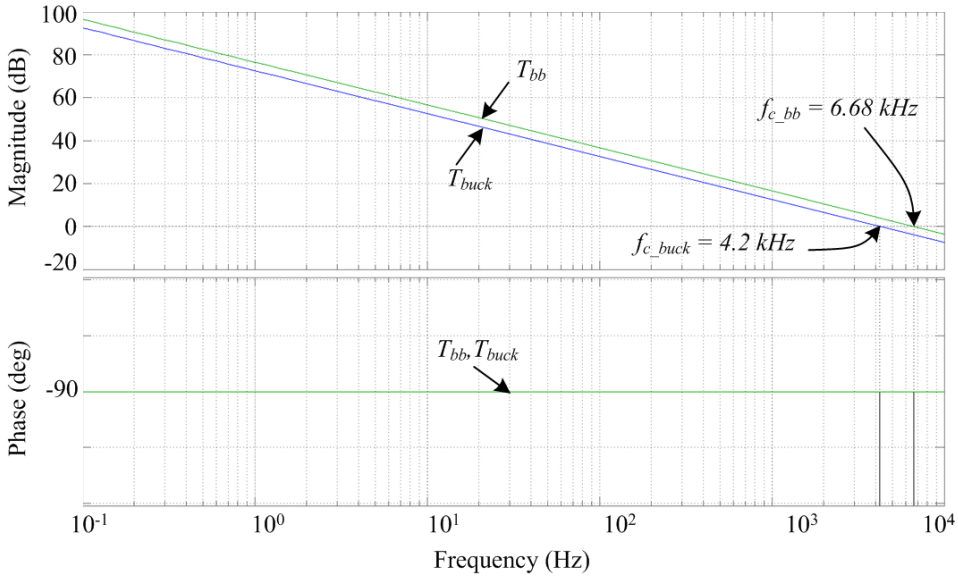


Fig. 4.11. Bodes plot of T_{buck} and $T_{bb.}$

because of the solar irradiation characteristic and the PV panel dynamics. Therefore the effect of the fast change of the inductor current reference on the line current distortion is negligible practically. One of the possible solutions to fully eliminate the current distortion within a line cycle is to decrease the magnitude of H_c to lower the control loop bandwidth. It is similar with the low-bandwidth output voltage loop of the AC-DC rectifier to secure the high power factor and low THD. Then the line current distortion due to the fast change of I_m may be mitigated, but the distortion caused by the weak DC gain of the control loop harms the THD of the line current in the B3 inverter again.

4.4. Differential Output Filter Design

The B3 inverter eliminates the common mode current by inheriting the solid ground connection of the HA converter. However, the conducted noise emission still occurs in the practical B3 inverter implementation because the differential mode current flows

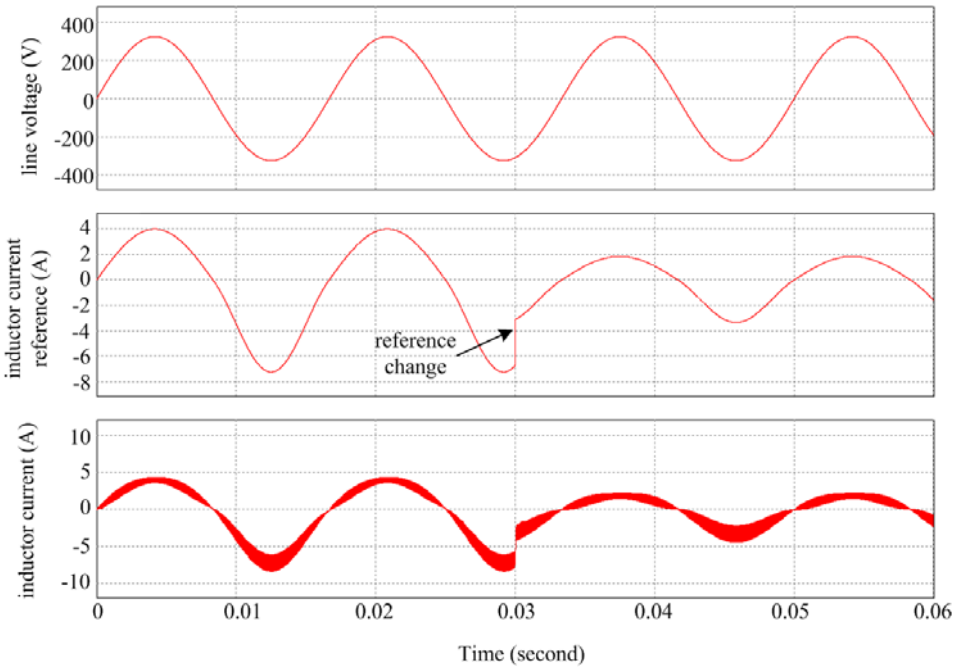
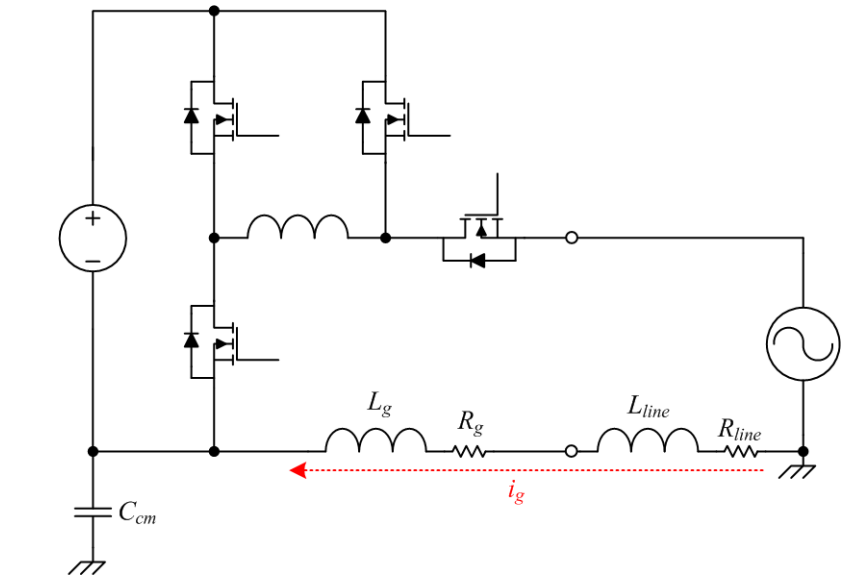


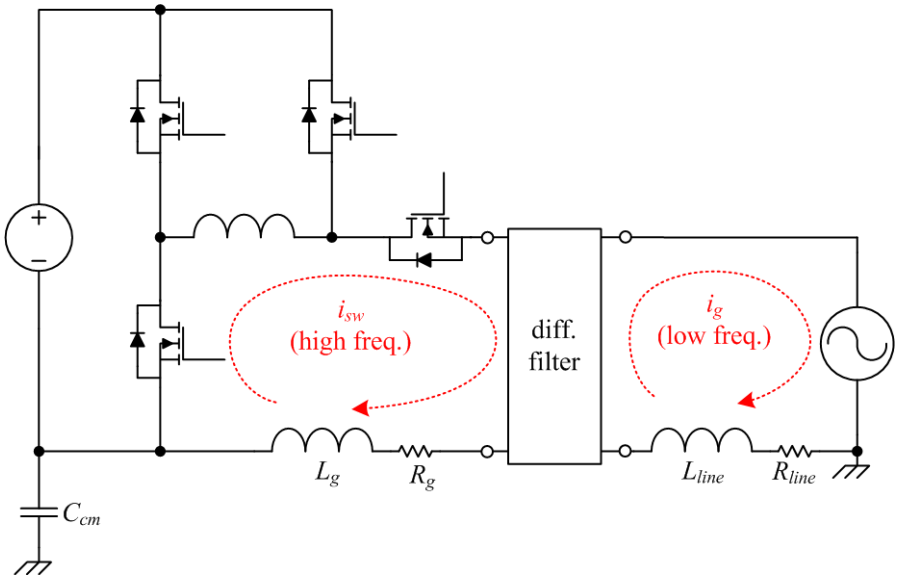
Fig. 4.12. Simulation results of the B3 inverter.

through parasitic elements of the circuit, similar with the B3 rectifier in Section 3.4. Fig. 4.13(a) shows the parasitic elements which contribute the conducted noise generation in the B3 inverter. The parasitic inductance and resistance in the AC distribution line, L_{line} and R_{line}, and those in the ground conductor in the PCB of the B3 inverter, L_g and R_g, cause the EMI in the B3 inverter. Implying that there is no filter between the line and the B3 inverter, the differential mode grid current i_g necessarily contains high frequency components due to the switching operation of the B3 inverter. These components will be even larger when the inverter operates in the buck-boost mode because not the inductor current but the switch current flows through the AC line. i_g in turn produces the high frequency voltage across the parasitic elements and the common mode capacitance C_{cm}, which consequently generates the conducted noise emission. Though L_g and R_g may be minimized by optimizing the layouts of the PCB, it is hard to control the line-related parasitic components such as L_{line} and R_{line}. In this section, a differential mode output filter is designed to attenuate the switching frequency harmonics in the grid current and reduce conducted EMI in the B3 inverter. Insertion of the differential output filter will separate the high frequency current from the AC line as shown in Fig. 4.13(b).

Before explaining the output filter design procedure, it should be noted that the filter designed in this section is optimized for the experimental setup that replaces the PV panel with a DC power supply. To properly design the output filter, the output impedances of the B3 inverter, Z_{O_buck} and Z_{O_bb}, should be considered to separate them from the input impedance of the output filter with sufficient margin. Interaction between the filter and the inverter is then minimized and the control loops of the inverter can operate in desirable way. Because the B3 inverter keeps alternating its topological states,



(a)



(b)

Fig. 4.13. (a) Conducted noise emission by parasitic elements and differential current in B3 inverter. (b) Separating currents by inserting a differential output filter.

the output impedances of the buck and buck-boost converters should be separately derived and considered.

The small signal block diagram for the buck mode operation in Fig. 4.14 additionally considers a power stage transfer function. Open-loop line voltage to inductor current transfer function in Fig. 4.14 is defined in (4.13).

$$H_{ivg\_buck} = \frac{\hat{i}_L}{\hat{v}_g} = -\frac{1}{sL} \tag{4.13}$$

The closed-loop output admittance of the buck operation Y_{O_buck} is shown in (4.14).

$$Y_{O\_buck} = \frac{H_{ivg\_buck}}{1 + H_{id\_buck} K_i H_c FM} \tag{4.14}$$

The line current in the buck-boost operation is not the inductor current but the switch current according to the current path shown in Figs. 4.3(c) and 4.3(d). The small signal block diagram for the buck-boost mode operation in Fig. 4.15 employs two more power stage transfer functions related to the new variable, $\hat{i}_d$, the perturbation of the Q_4

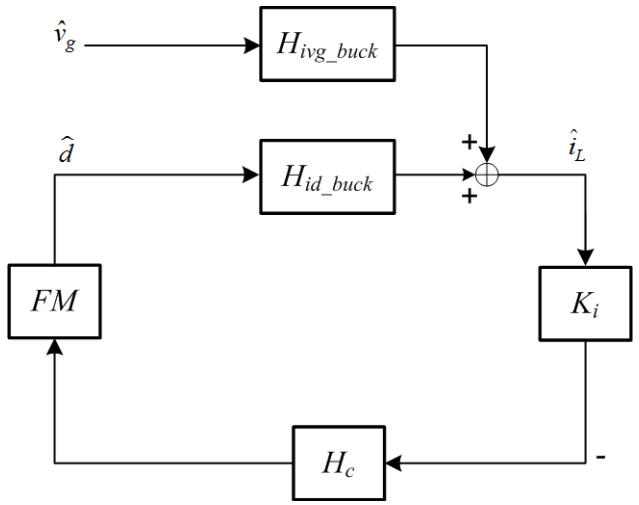
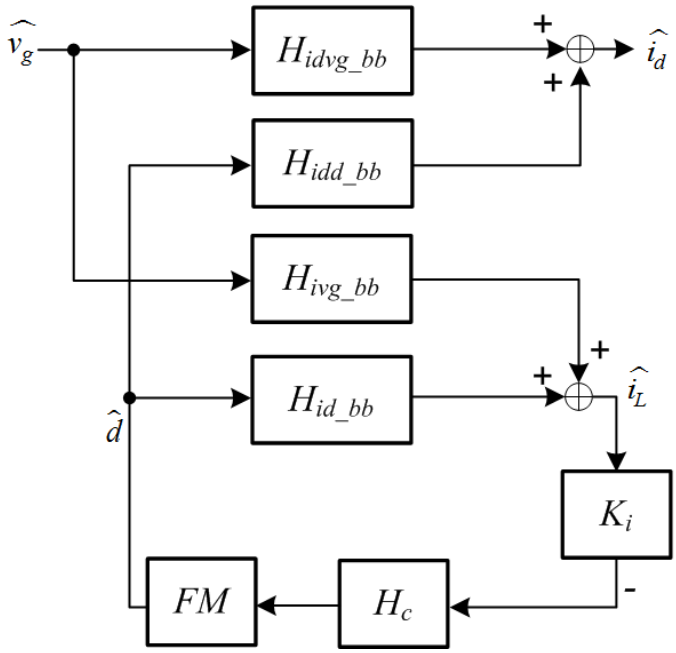
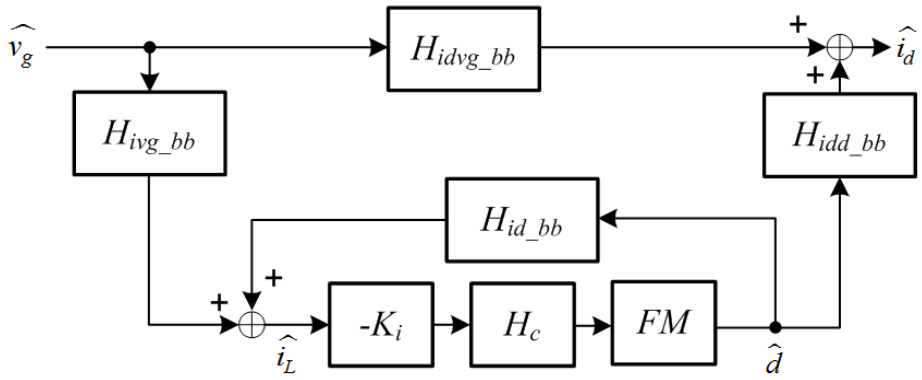


Fig. 4.14. Small signal block diagram for the buck mode operation of the B3 inverter.



(a)



(b)

Fig. 4.15. (a) Small signal block diagram for the buck-boost mode operation of the B3 inverter. (b) Rearranged block diagram of to derive Y_{O_bb}.

current. The suffix $_d$ means diode because Q_4 acts as the output diode of the buck-boost converter shown in Fig. 4.8(a). H_{idvg_bb} and H_{idd_bb} are shown in (4.15) to (4.16).

$$H_{idvg\_bb} = \frac{\hat{i}_d}{\hat{v}_g} = -\frac{D_{bb}'^2}{sL} \tag{4.15}$$

$$H_{idd\_bb} = \frac{\hat{i}_d}{\hat{d}} = \frac{V_{PV} D_{bb}'}{sL} \tag{4.16}$$

To derive closed-loop output admittance of the buck-boost mode B3 inverter Y_{O_bb}, the block diagram in Fig. 4.15(a) is rearranged as in Fig. 4.15(b), and resultant Y_{O_bb} is expressed in (4.17).

$$Y_{O\_bb} = H_{idvg\_bb} - \frac{H_{ivg\_bb} K_i H_c H_{idd\_bb} FM}{1 + H_{id\_bb} K_i H_c FM} \tag{4.17}$$

Fig. 4.16 shows the reciprocals of Y_{O_buck} and Y_{O_bb}, or the output impedances of the B3

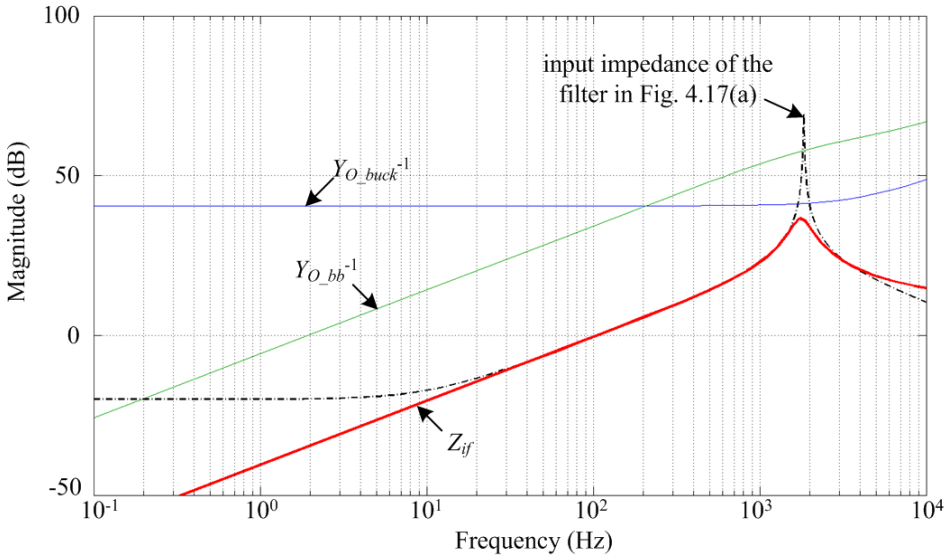


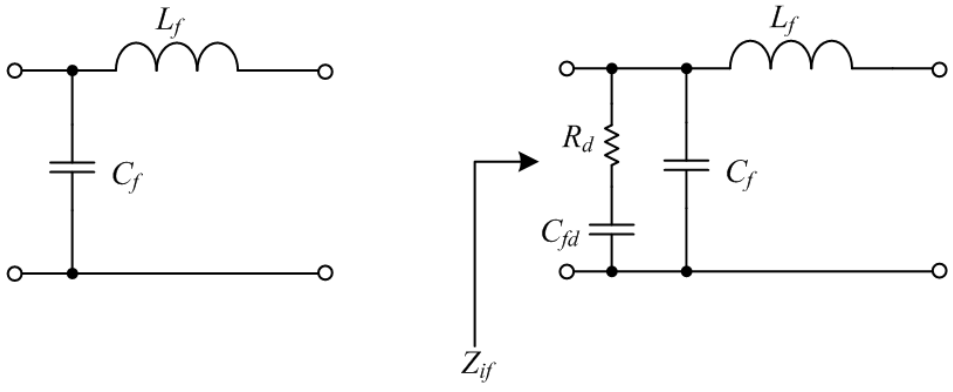
Fig. 4.16. Bode plot of $Y_{O\_bb}^{-1}$, $Y_{O\_buck}^{-1}$, and input impedances of the filters shown in Fig. 4.17.

inverter. The impedance alters according to the equivalent topology of the B3 inverter.

Because the B3 inverter is naturally a current source inverter, the filter to attenuate the high frequency ripple current in the line side should be applied. If the simple *L-C* filter as shown in Fig. 4.17(a) is applied as the output filter, considerable loading effect will occur in the low frequency region and the stability of the system may be degraded. The broken line in Fig. 4.16 indicates the input impedance of the output filter when the filter inductor L_{fl} and the filter capacitor C_{fl} are 1.5 mH and 5 μF. At low frequency region and around the corner frequency, the filter input impedance in Fig. 4.17(a) exceeds the inverter output impedance, which may cause the system instability. In this dissertation, a capacitively damped third order filter shown in Fig. 4.17(b) is selected as the output filter of the B3 inverter. Eq. (4.18) shows the mathematical expression of the output filter input impedance characteristic, Z_{if}.

$$Z_{if} = \frac{sL_f + s^2 L_f C_f C_{fd}}{1 + sC_{fd}R_d + s^2\left(L_f C_f + L_f C_{fd}\right) + s^3 L_f C_f C_{fd} R_d} \tag{4.18}$$

The bold curve in Fig. 4.16 represents Z_{if}, selecting L_f, C_f, C_{fd}, and R_d as 1.5 mH, 5 μF,



(a) (b)

Fig. 4.17. (a) Second order *L-C* filter and (b) capacitively damped third order filter as the differential output filter of the B3 inverter.

480 nF, and 5 Ω. The input impedance of the filter achieves sufficient gain margin with the inverter output impedances, which guarantees that there is no interaction between the B3 inverter with its control loop and the differential output current filter.

Fig. 4.18 shows simulation results of the B3 inverter with the designed output filter. The operation condition is same with that shown in Fig. 4.12. The line current is filtered to show negligible ripple, while the control performance of the inverter is still maintained. The line current ripple is larger in the buck-boost mode than in the buck mode, because the switch current which contains larger high-frequency components than inductor current is directly applied to the output filter.

4.5. Experiments

4.5.1. Implementations

To compare the performance of the inverters, two inverters are implemented for

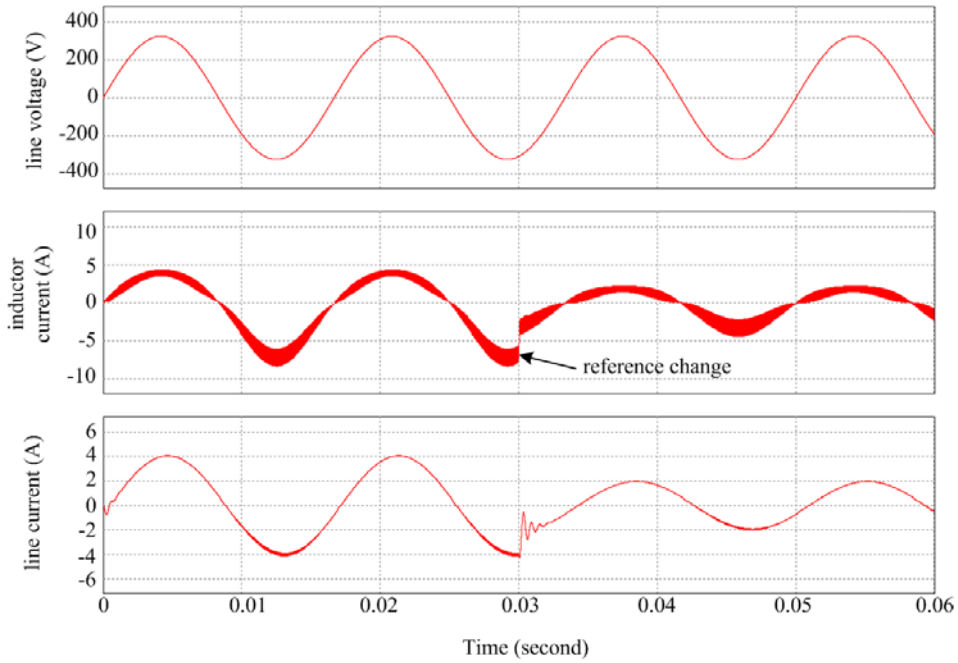


Fig. 4.18. Simulation results of B3 inverter with the output filter shown in Fig. 4.17(b).

experiment in this section: the B3 inverter and the H-bridge inverter with bipolar PWM. The two inverters utilize almost same PCB layouts and power components for fair comparison.

As designed in the previous sections, the B3 inverter is implemented with the output filter designed in Section 4.4. A four-layer PCB is used to build 650 -W prototype circuit. Fig. 4.19 illustrates the implementation of the B3 inverter. Currents are sensed by Hall Effect sensors, and input and output voltages are sensed by inverting op-amp circuit and resistive voltage divider respectively. Texas Instrument TMS320C28346 digital signal processor with auxiliary ADC and DAC is adopted as the controller of the proposed inverter. Part names and circuit parameters are summarized in the following:

1) Q_2, Q_3: STP11NM60FP (600 V, 11 A),

2) Q_4, Q_5: FGL35N120FTD (1,200 V, 35 A),

3) L: 4 mH,

4) H_1-H_3: ACS756SCA,

5) C_{cm}: 330 nF,

6) $v_p - v_n$: 230 Vac 60 Hz commercial AC line from wall outlet,

7) v_{pv}: 395 Vdc,

8) Switching frequency f_s: 20 kHz,

9) A_1: LMV32410) V_{off}: 1.65 V,

11) L_f: 1.5 mH,

12) C_f: 5 μF,

13) C_{fd}: 480 nF,

14) R_d: 5 Ω (filter configurations including L_f, C_f, C_{fd}, R_d shown in Fig. 4.22(a)).

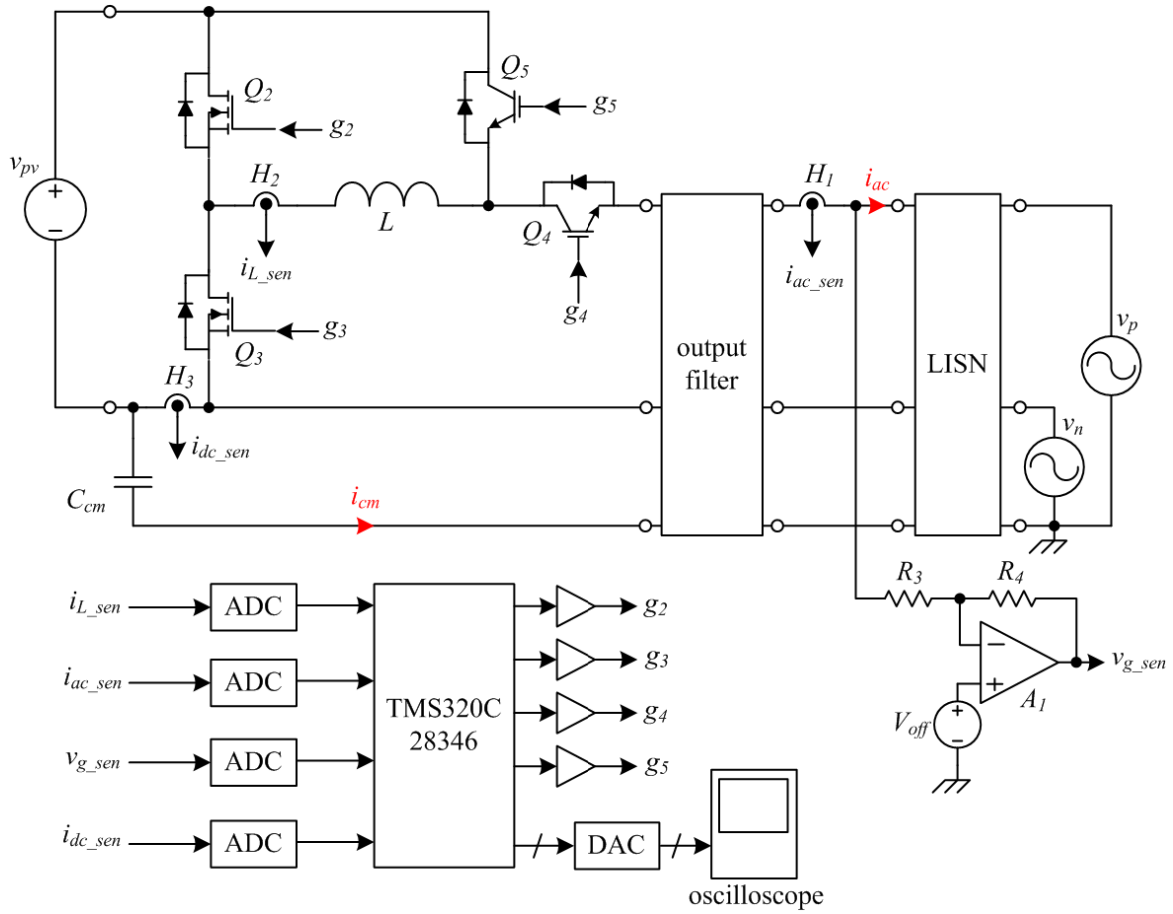


Fig. 4.19. Experimental setup of the B3 inverter.

To emulate PV panel voltage v_{pv}, a DC power supply Sorensen DLM600-5E with a choke filter, a diode, and 2.2 -mF electrolytic capacitors is used as the input voltage source of the two inverters as shown in Fig. 4.20. The choke filter is to block any possible noise generated by the DC power supply from the inverter and LISN, and the diode is to protect the supply from faulty reverse current. For the buck-boost operation, Q_4 and Q_5 are selected as IGBTs with 1,200 -V rating. i_{L_sen}, i_{ac_sen}, and i_{dc_sen} represent the sampled value of the inductor current, line current, and output current from the power stage. They are input to the digital controller through the ADC and utilized to establish the system operation. i_{ac_sen} and i_{dc_sen} from H_1 and H_3 are for system protection and not directly related to the control of the inverter. A photocoupler with auxiliary isolated DC-DC converter is used as the gate driver for Q_2, Q_4, and Q_5

Similar with the rectifier implementations in Chapter 3, a common mode parasitic capacitor C_{cm} is intentionally implemented to investigate the conducted noise of the prototype circuit. The common mode noise is measured by using LISN and EMI analyzer. All the heat sinks attached to the semiconductor devices are not grounded to

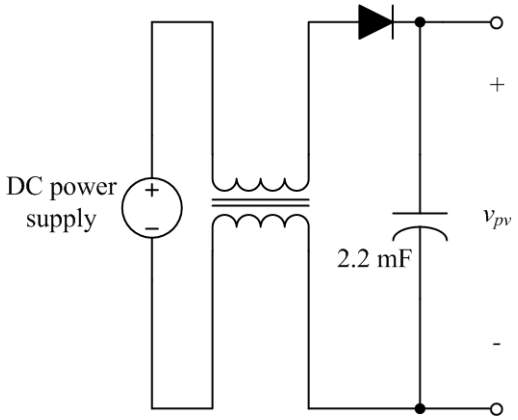


Fig. 4.20. Implementation of DC voltage source to emulate PV panel.

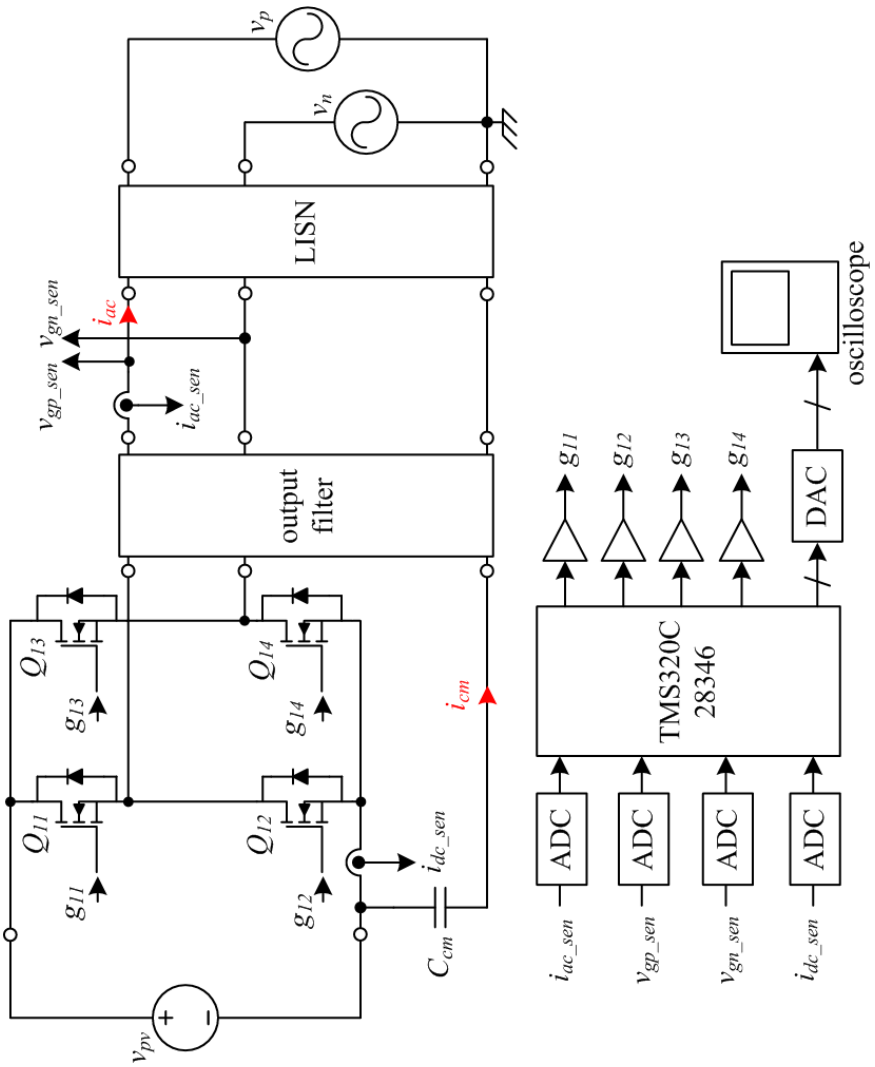


Fig. 4.21. Experimental setup of H-bridge inverter.

minimize their effect on the conducted noise [22]. Both B3 and H-bridge inverter are not shielded from radiated noise which may exist in the laboratory circumstance. The radiated noise may influence the conducted noise acquisition during the experiment, but it has little effect on comparing the conducted noises of the two prototype circuits.

The conventional H-bridge inverter controlled by bipolar PWM shown in Fig. 2.7 is also implemented for comparison as in Fig. 4.21. All the MOSFETs in Fig. 4.21, Q_{11} to

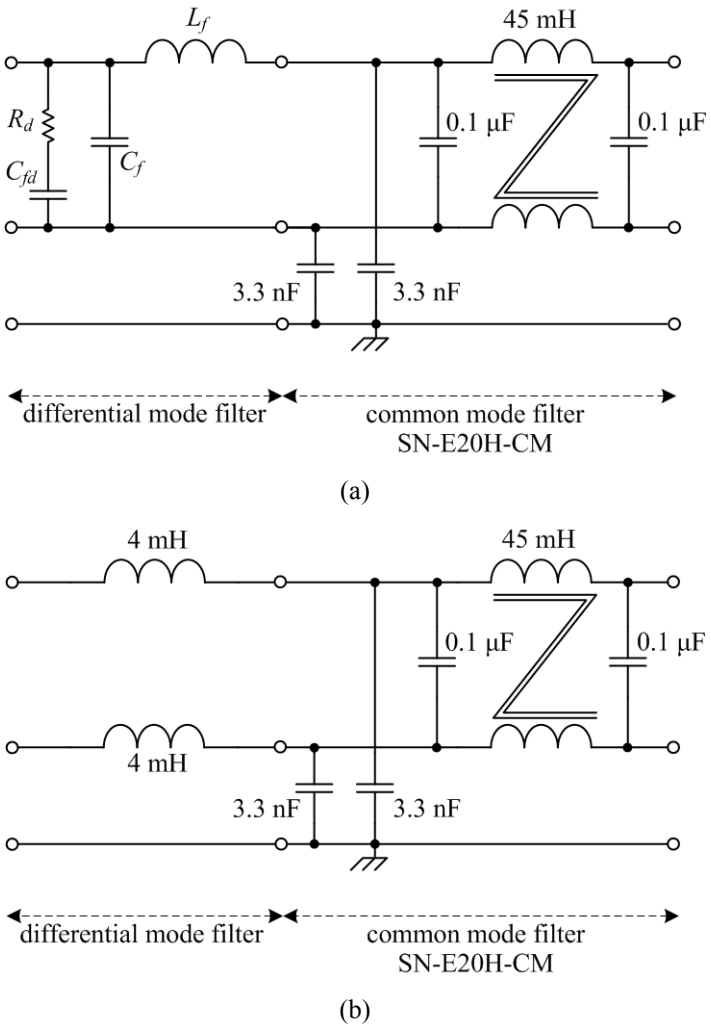


Fig. 4.22. Output filters used for (a) the B3 inverter and (b) H-bridge inverter.

Q_{14}, are the same ones with Q_2 and Q_3 in Fig. 4.19, STP11NM60FP. Contrary to the B3 inverter case, PLL for AC line voltage sensing in the conventional H-bridge inverter is accomplished by differentially sensing the phase and neutral conductor voltages of AC output terminal.

Being different from the rectifier input filter in Chapter 3, the B3 inverter and H-bridge inverter do not utilize same differential filter configuration. It is because the operation characteristics of the two inverters are different from each other: the proposed B3 inverter is a current source inverter because the inductor current is controlled, filtered, and injected to the AC line. The H-bridge inverter, on the other hand, is a voltage source inverter because it controls and filters inductor voltage (v_{AB} in Fig. 2.7) to transfer power to the AC line. Therefore, the B3 inverter employs capacitive filter as designed in Section 4.4, and H-bridge inverter utilizes inductive filters. Being combined with the common mode filters, the output filters used in the experiments in Figs. 4.19 and 4.21 are illustrated in Fig. 4.22.

4.5.2. Results and Discussions

Fig. 4.23 shows the steady state operation of the B3 inverter when the peak of the reference current I_m is 4 A. Channels 1 and 2 indicate the filtered line current i_{ac}, and inductor current i_L, which are measured by current probes, and channels 3 and 4 represent the gate signals g_5 and g_2 respectively. During the negative line cycle, the inductor current demonstrates different shape from that in the positive line cycle as explained in Section 4.3.1. The inductor current follows the reference current in Fig. 4.5 to balance the positive and negative line currents.

Fig. 4.24 displays the duty cycles of the buck and buck-boost operation, d_{buck} and d_{bb},

when I_m is 1 A. Channels 1 and 4 shows d_b and d_{bb} which are calculated by the controller and output through by DAC. Channel 2 and 3 represent filtered line current measured by current probe and calculated reference inductor current measured by DAC. In Fig. 4.23, d_{buck} follows the pure sine wave, while d_{bb} does not. It is because the inductor current and switch current are transferred to the AC line during the positive and negative line cycle as explained in Section 4.2. The trace of d_{bb} is the curve that follows Eq. (4.2), which is not the pure sinusoid. Considering d_{buck} is determined by (4.19) and compare it with (4.2), it is also obvious that the peak of d_{bb} is smaller than that of d_{buck}.

$$d_{buck} = \frac{|v_g|}{v_{pv}} \tag{4.19}$$

Line voltage v_g and line current i_{ac} are shown together in Fig. 4.25 when the B3

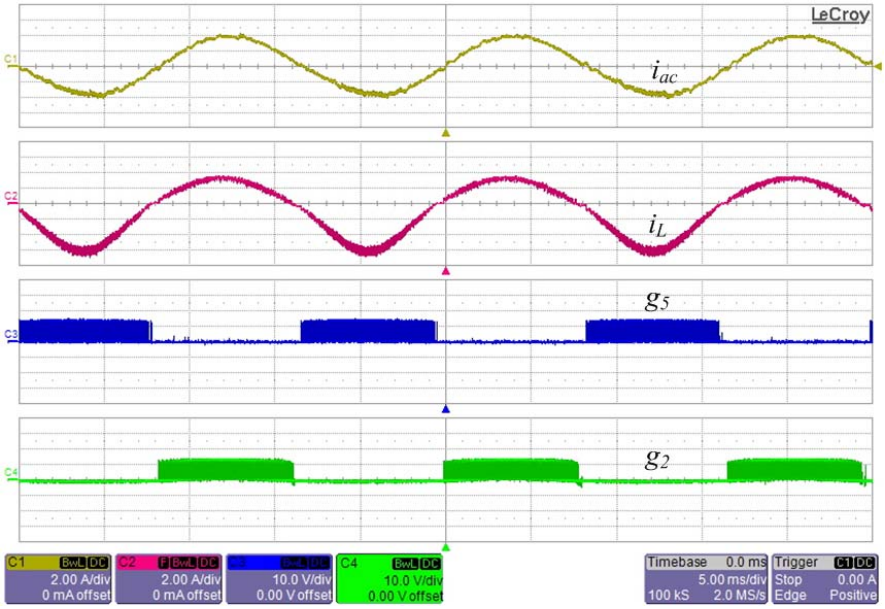


Fig. 4.23. Steady state waveforms of the B3 inverter when I_m is 4 A. (i_{ac} and i_L: 2 A/div., g_2 and g_5: 10 V/div., 5 ms/div.)

inverter outputs 520 W to the 230 Vac line. v_g is measured by differential voltage probe. It is confirmed from Fig. 4.25 that i_{ac} and v_g are synchronized together to demonstrate high power factor.

Fig. 4.26 shows the operation of the B3 inverter when I_m abruptly jumps from 1.8 A (45% of rated power) to 3.8 A (95% of rated power). Channels 1 through 4 represent the line voltage, filtered line current, inductor current, and common mode current i_{cm} that flows through C_{cm} respectively. All the quantities in Fig. 4.25 are directly measured by voltage and current probes, i.e., without using DAC. It is noted that i_{ac} follows the change of the reference current with small resonance as expected from the simulation results in Fig. 4.18. i_{cm} is larger in the negative line cycle than in the positive cycle in Fig. 4.26. It is because the voltages applied to the semiconductor devices such as Q_4 and

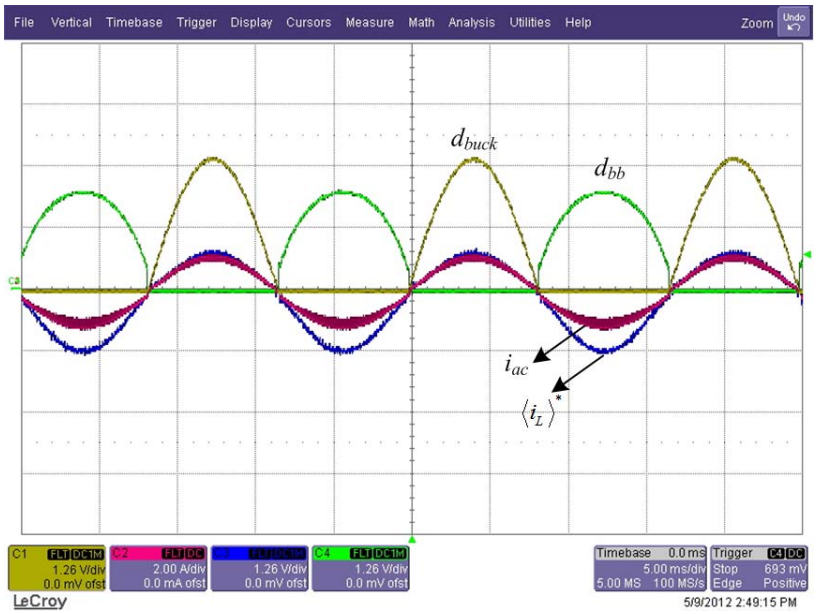


Fig. 4.24. Steady state waveforms of the B3 inverter when I_m is 1 A. (d_b and d_{bb}: 0.25 /div., $\langle i_L \rangle^*$ and i_{ac}: 2 A/div., 5 ms/div.)

Q_5 are larger than those applied to Q_2 and Q_3.

Common mode currents and noises of the proposed B3 inverter and conventional counterparts are shown in Fig. 4.27. Fig. 4.27(a) presents the rms common mode current comparison between the two prototype inverters. The current through C_{cm} is directly measured by current probe. The B3 inverter shows smaller i_{cm} than the conventional counterpart. Fig. 4.27(b) displays the common mode noise measurements using the LISN and EMI receiver Agilent N9038A when the output power is 650 W. The noise is measured from 150 kHz to 30 MHz in the frequency domain. It shows that the noise levels of the proposed inverter is smaller than that of the conventional counterpart in overall frequency range by approximately 30 dBμV. It is due to the connected ground configuration of the B3 inverter that dramatically minimizes the noise generation by the

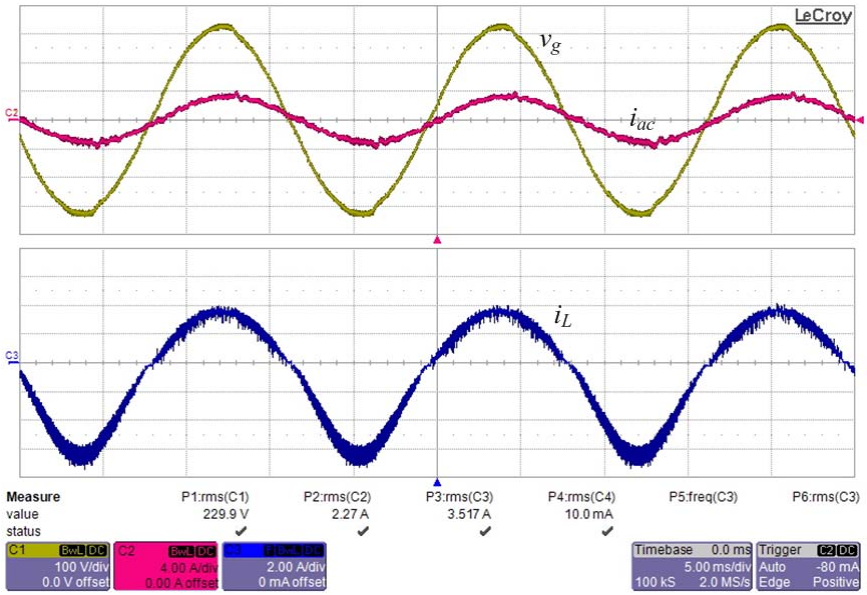


Fig. 4.25. Steady state waveforms of the B3 inverter when its output power is 520 W. (v_g: 100 V/div., i_{ac}: 4 A/div., i_L: 2 A/div., 5 ms/div.)

common mode parasitic capacitor C_{cm}.

The connected ground of the B3 inverter reduces differential mode noise as well as the common mode noise. The differential mode noises of the two inverters are also measured and compared as shown in Fig. 4.28. The proposed B3 inverter demonstrates smaller differential noise than its conventional counterpart. This is because the current flows through the converter ground with parasitic resistance and inductance as explained in Section 4.4.

Fig. 4.29 displays efficiency curves of the two prototype circuits. The output power to the AC line is measured by a power analyzer Yokogawa WT210, and the input power from the DC voltage source is read from the machine itself. The proposed B3 inverter efficiency is higher than the conventional one in overall load conditions. It is because

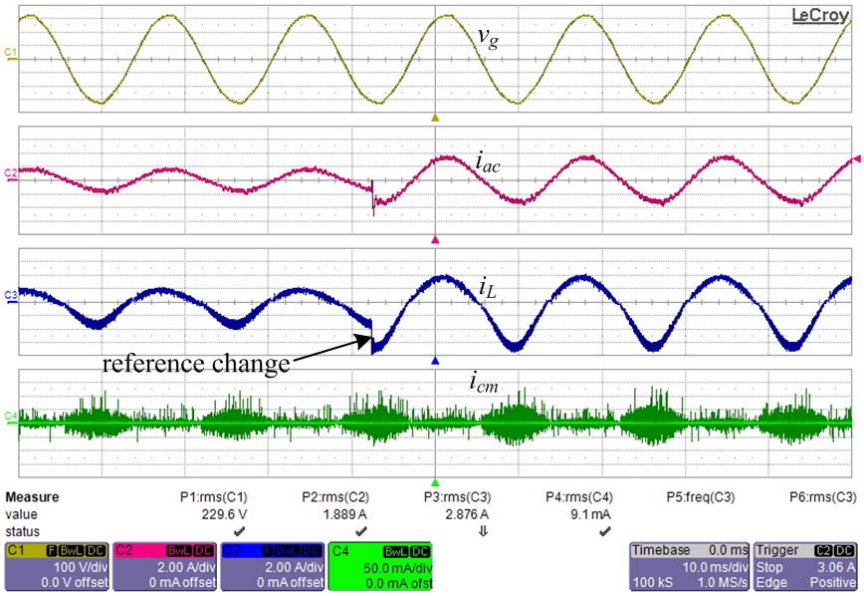
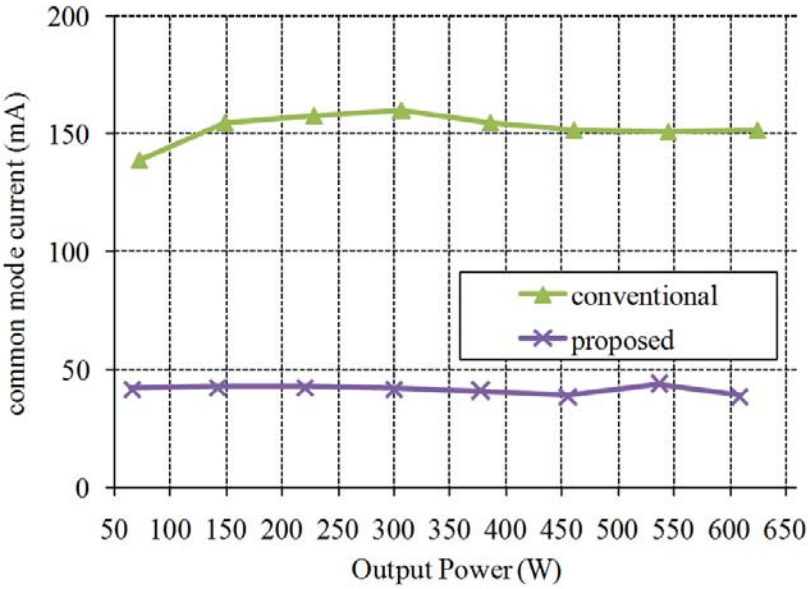
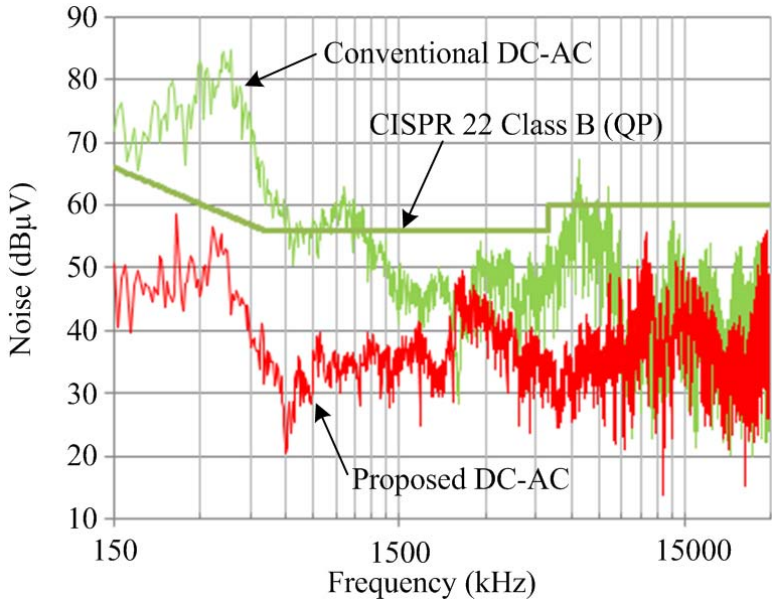


Fig. 4.26. Transient operation of the B3 inverter when I_m jumps from 1.8 A to 3.8 A. (v_g: 100 V/div., i_{ac}, i_L: 2 A/div., i_{cm}: 50 mA/div., 5 ms/div.)



(a)



(b)

Fig. 4.27. Common mode characteristic comparison between the proposed B3 inverter and its conventional counterpart: (a) rms common mode current and (b) common mode noise measured by LISN and EMI analyzer.

the switching loss of B3 inverter is smaller than that of the conventional counterpart. In B3 inverter, two of the four switch devices are not switching, i.e., the one is fully turned on and the other is fully off regardless of the AC line polarity, while all the switches in the H-bridge inverter always keeps switching.

It should be also noted that the reason why the absolute efficiencies in Fig. 4.29 are lower than those shown in Fig. 3.31, even though the rectifiers and inverters process similar power, is the additional circuit elements of the inverters such as the common mode choke filter, blocking diode, and large input capacitor in Fig. 4.20.

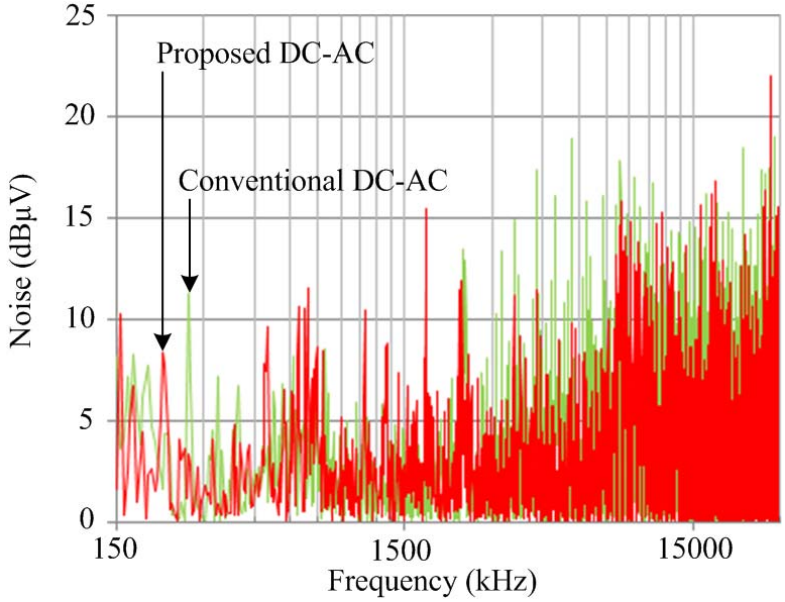


Fig. 4.28. Differential noise measured by LISN and EMI analyzer.

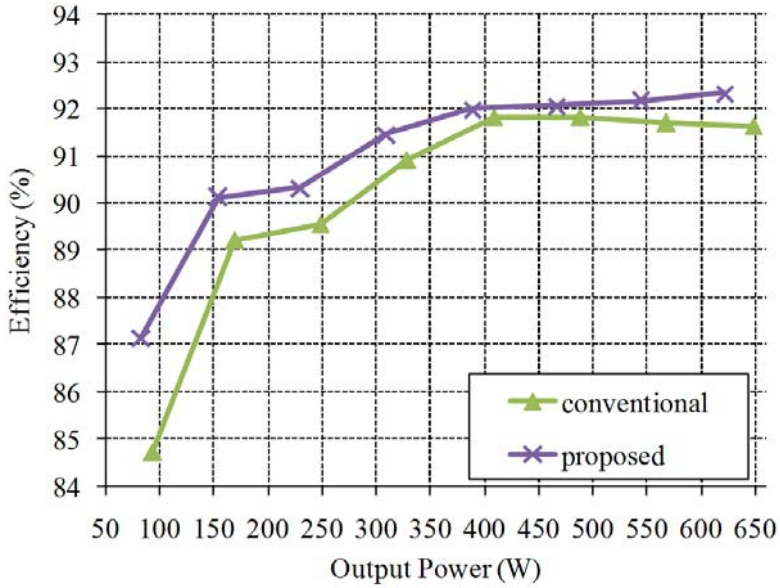
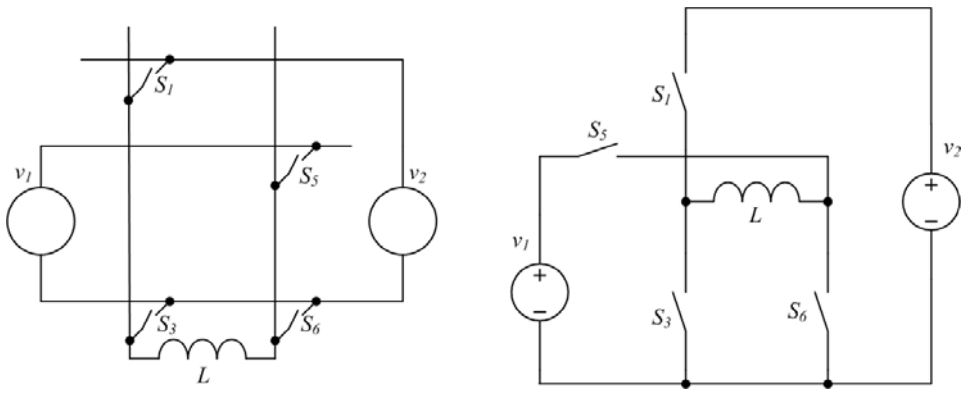


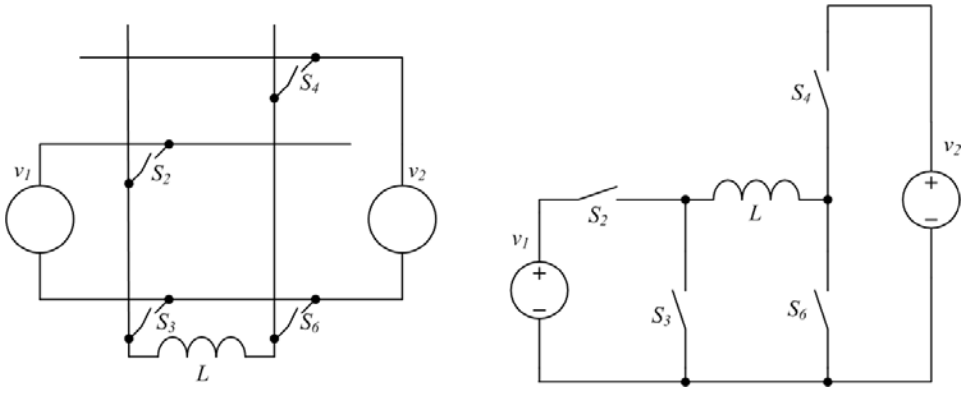
Fig. 4.29. Efficiency comparison between the proposed B3 inverter and the conventional H-bridge inverter.

5. Flexibility of HA Converter

As presented in Chapter 2, the HA converter is highly flexible because it can emulate all the single-ended DC-DC converters with single inductor. In addition to Figs. 2.18 to 2.21, non-inverting buck-boost converters are also realized by the HA converter. Fig. 5.1(a) shows an example of the non-inverting buck-boost operation of the HA converter when both v_1 and v_2 are positive. The magnitude of v_2 can be either larger than or smaller than v_1. The two switch pairs, S_5-S_6 pair and S_1-S_3 pair, operate according to the PWM signal and S_2 and S_4 are omitted. Fig. 5.1(b) shows another circuit



(a)



(b)

Fig. 5.1. Switch selections for non-inverting buck-boost converter operation of the HA converter.

configuration of the HA converter for non-inverting buck-boost emulation. The switch pairs S_2-S_6 and S_3-S_4 operate according to the PWM signal and S_1 and S_5 are eliminated.

The operation of the HA converter explained so far is not the only ways to mimic the DC-DC converters. As the broken line in Fig. 5.2 indicates, the HA converter is bilaterally symmetric. Depending on which source among v_1 and v_2 is selected to be an input, the HA converter has two options to emulate each DC-DC converter topology. For examples, the circuit in Fig. 2.18 is considered as the other switch configuration for boost converter operation when v_2 is the input power source and v_1 is the output power sink. Similarly, the one in Fig. 2.19 is for buck converter operation when v_2 is input and v_1 is output. The buck-boost circuits in Figs. 2.20, 2.21, and 5.1 are also able to change the power flow between the two sources by changing the switch operating sequence. To sum up, the HA converter can be a bidirectional converter in any switch configuration, if all the ideal switches are implemented by active semiconductor devices. Actually, the B3 inverter presented in Chapter 4 is the bidirectional version of the B3 rectifier in Chapter 3, replacing the diodes with the active switch devices. And in opposite, applying the

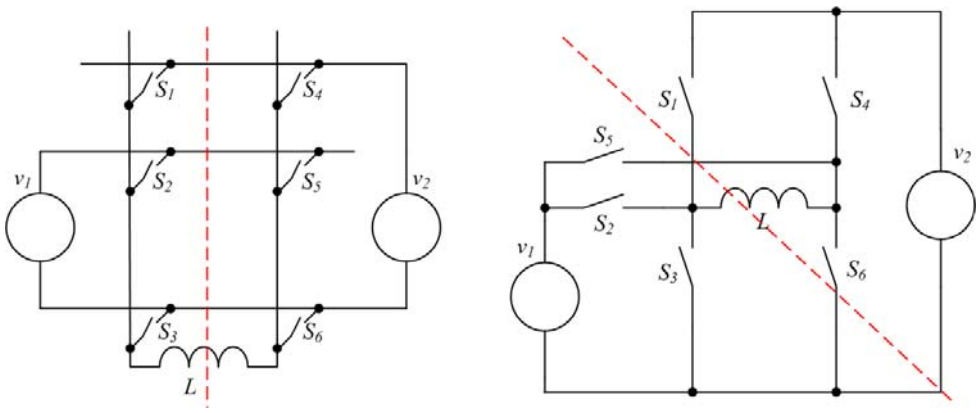


Fig. 5.2. Bilateral symmetry of the HA converter.

control loop designed in Section 3.3 to the B3 inverter in Chapter 4 will operate the circuit like the rectifier, delivering power from AC line to DC load.

The bidirectional power handling capability of the HA converter is feasible to the interface circuit related to energy storage devices such as batteries and supercapacitors, which are widely used in various power systems as the energy buffer [10]-[13]. They supply or absorb the power from the other part of the system according to the operational conditions of the power system or the energy scheduling scenario [61]. For the system which does not require the galvanic isolation, the HA converter is a good candidate advocating its simple circuit structure and low common mode noise. Especially, the HA converter is feasible for the stand-alone power system with large parasitic capacitance as already mentioned in Section 2.1.2.

The circuits demonstrated in Chapters 3 and 4 are merging boost or buck converter with inverting buck-boost converter in the HA converter. Though they have simple circuit structure by minimizing the number of semiconductor devices, there is a limit on the input and output voltage specification: the DC voltage should be always higher than the maximum AC voltage. In the system where DC voltage changes in wide range, the non-inverting buck-boost converters shown in Fig. 5.1 should be merged with the inverting buck-boost converters. As a trade-off against the circuit simplicity, the resultant circuits obtain the freedom from the voltage level specification of the system.

Fig. 5.3 shows a buck-boost-buck-boost type-1 (B4-I) rectifier that merges the non-inverting buck-boost converter in Fig. 5.1(b) and the inverting buck-boost converter in Fig. 2.21. Only S_1 in the HA converter is omitted as shown in Fig. 5.3(a) and all the other switches are realized by the practical switches as in Fig. 5.3(b). The ideal switch,

S_2, S_3, and S_5 are realized by the combination of two practical switch devices. S_2 and S_5 are replaced by the back-to-back connected MOSFET and diode pairs Q_2-D_2 and Q_5-D_5 to constitute unidirectional current path. Though the B4-I rectifier uses the higher number of semiconductor devices than the B3 rectifier, its output voltage need not be higher than the maximum AC input voltage. B4-I rectifier does not require any feedforward correction in the control loop because the relationship between the average

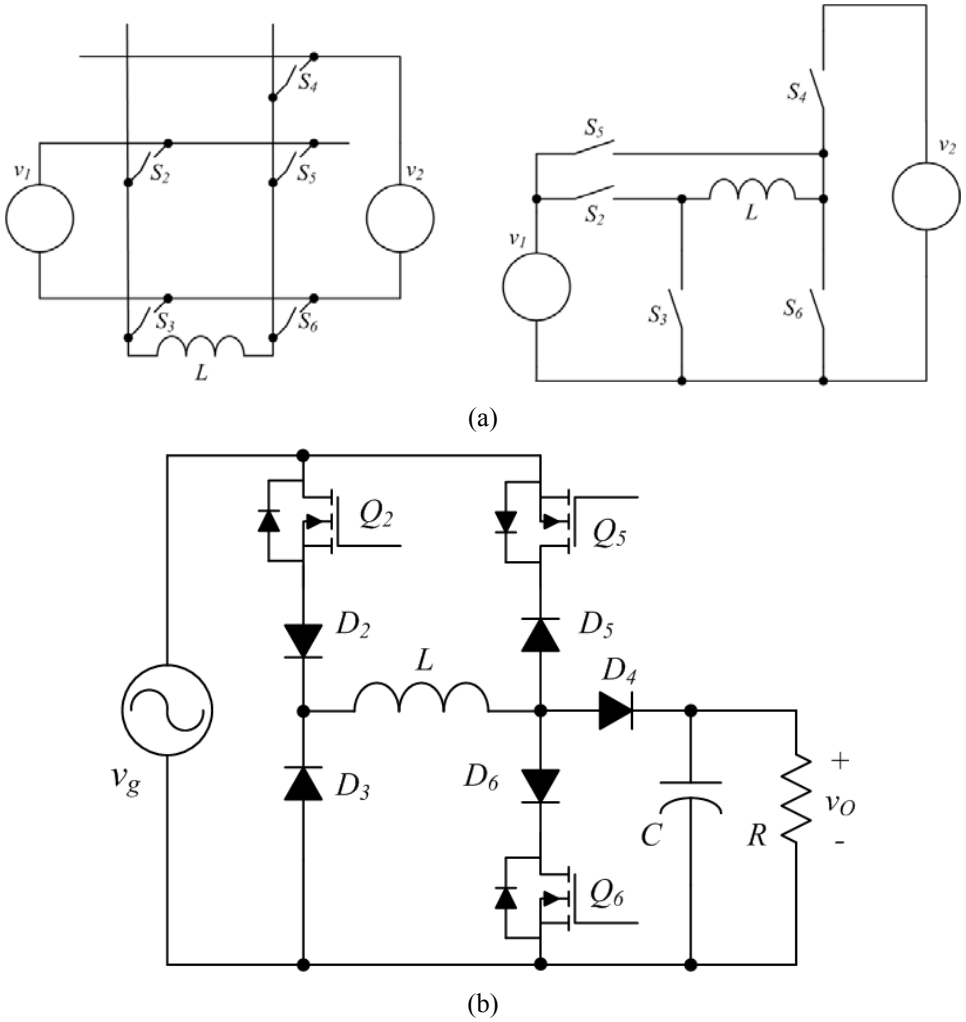


Fig. 5.3. (a) Switch selection in HA converter for B4-I rectifier. (b) Switch realization.

line and the average inductor current is constant regardless of the polarity of the line voltage. The gate signals for the B4-I rectifier is shown in Fig. 5.4.

Fig. 5.5(a) shows another type of the rectifier named as buck-boost-buck-boost type-2 (B4-II) rectifier. B4-II rectifier utilizes the same switches in the HA converter with the B4-I rectifier, S_2 to S_6, and they can be implemented as the combination of a MOSFET and a diode. S_3 is realized by a diode D_3 and a MOFSFET Q_3 to constitute a bidirectional current path. S_5 is made by a low-frequency switching device T_5 and a diode D_5. It always operates as the buck-boost converter whether the polarity of the AC line voltage is positive or negative, and is free from the feedforward gain correction and output voltage range limitation. The gate signals for active switch elements in the B4-II rectifier is shown in Fig. 5.5(b).

Fig. 5.6 shows another type of inverter named as buck-boost-buck-boost type-3 (B4-

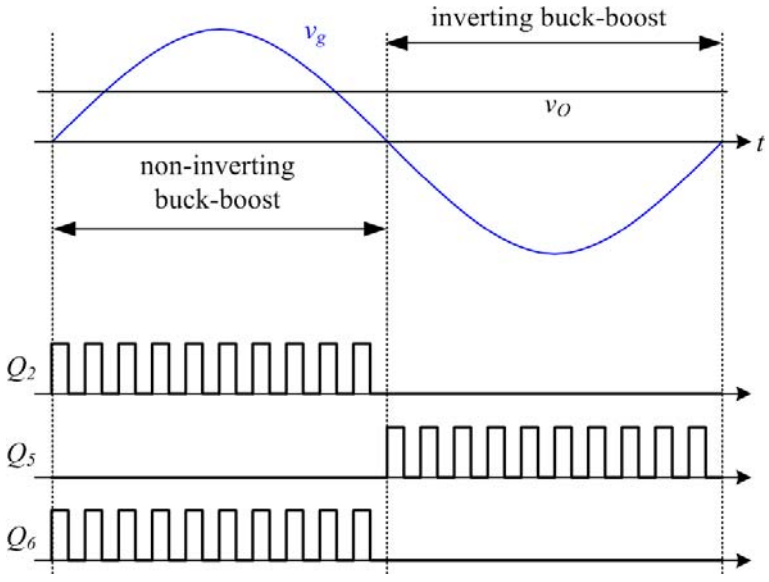


Fig.5.4. Gate signals of B4-I rectifier.

III) inverter. B4-III utilizes the switches S_1, S_2, S_3, S_4, and S_6 in the HA converter. Similar with the B4-I and B4-II rectifiers, the B4-III inverter always operates as the buck-boost converter whether the polarity of the AC line voltage is positive or negative, and is free from the feedforward gain correction and output voltage range limitation. Switches S_1, S_3, and S_4 are realized by a diode and a low-frequency switching devices. The gate signals for active switch elements in the B4-III inverter is shown in Fig. 5.6(b).

Though the B4-III inverter has more semiconductor switches than the B3 inverter in Chapter 4, it advocates higher flexibility in its operation than any other HA converter derived inverters. The B4-III inverter can operate with the different switching scheme shown in Fig. 5.6(c). If the PV panel voltage is higher than the maximum line voltage, the B4-III inverter can operate as the buck converter when v_g is positive. The only difference between the Figs. 5.6(b) and 5.6(c) is the switching of the active switch Q_6. The control algorithm for the buck and buck-boost operated B4-III inverter is totally same with that of the B3 inverter in Chapter 4. In general, the buck converter operation shows higher efficiency than the buck-boost converter one due to the smaller voltage stress and switching loss of the semiconductor devices than the buck-boost converter.

The circuits mentioned in this chapter contain more semiconductor devices than the B3 rectifier and B3 inverter, but they still maintain the solid connection of the grounds to minimize the common mode EMI. The circuits are free from the DC voltage magnitude limitation and improve flexibility in operation as the trade-off against the increased circuit complexity. The development and the application of the bidirectional switch will help the circuits in this chapter to simplify their implementation and improve the efficiency.

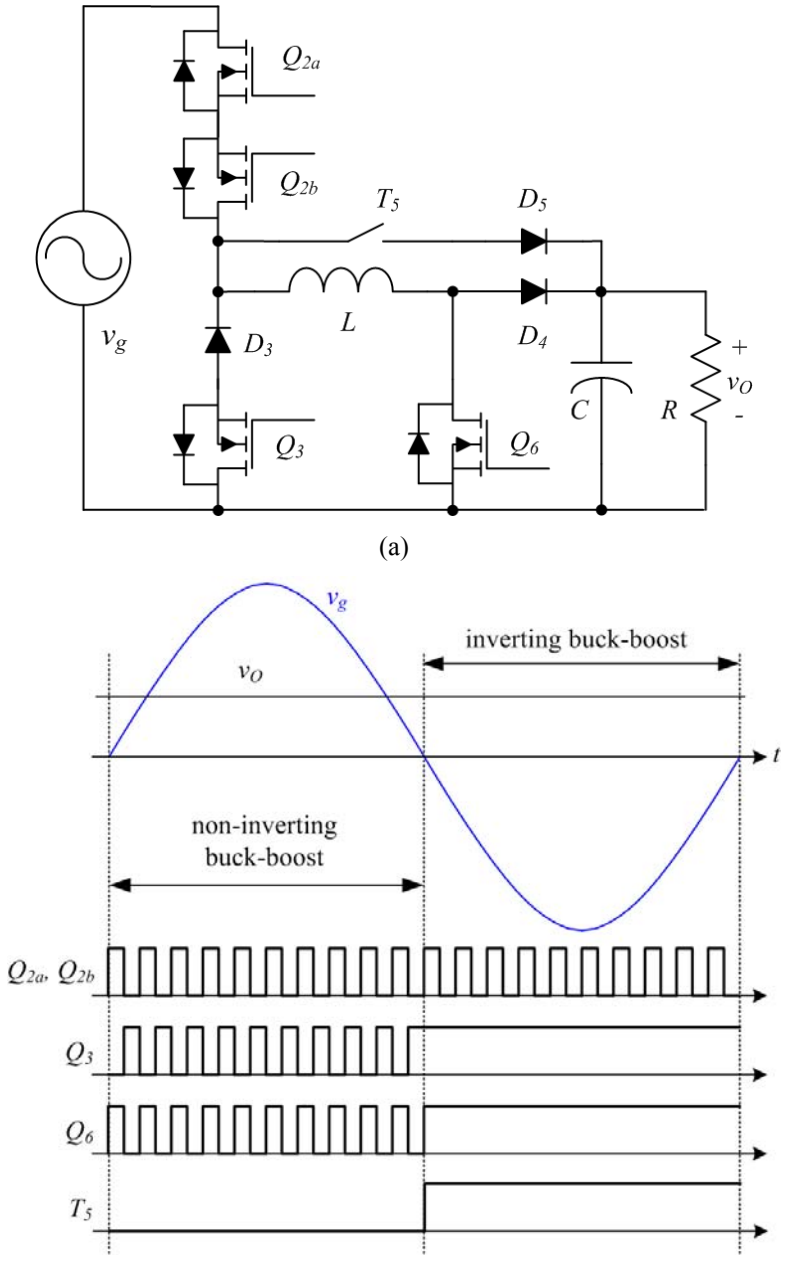
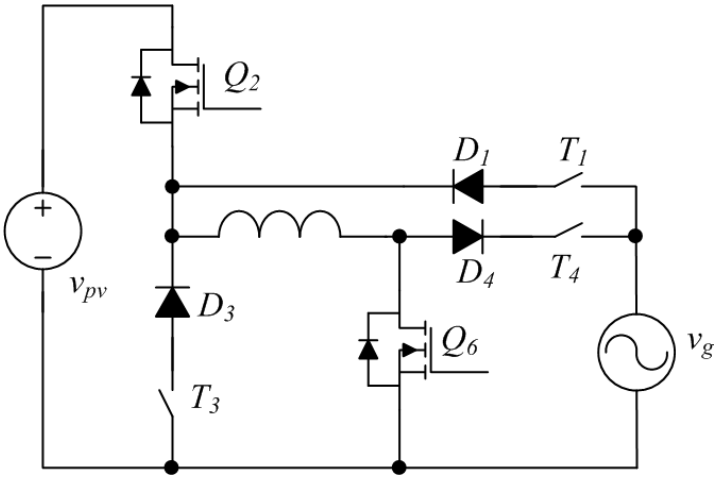
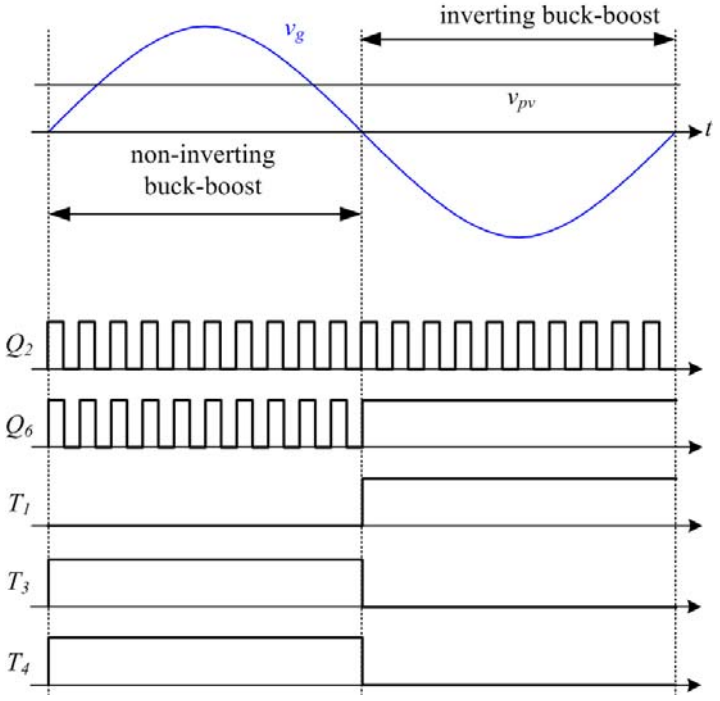


Fig.5.5. B4-II rectifier: (a) switch realization and (b) gate signals.



(a)



(b)

Fig.5.6. B4-III inverter: (a) switch realization and (b) gate signals.

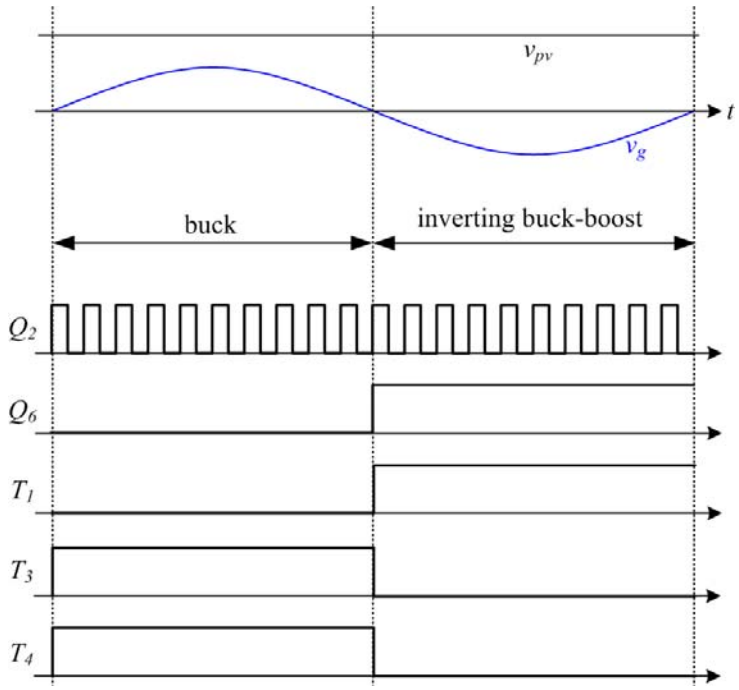


Fig.5.6. (Cont.) (c) Gate signals when buck converter operation is included in B4-III inverter.

6. Conclusion and Further Works

This dissertation proposes a set of new converter topologies with low common mode noise and simple circuit structure. With its proper switch selection and drive, the newly proposed HA converter fulfills the common mode EMI reduction and circuit simplification in both AC-DC rectification and DC-AC inversion. The proposed circuit structure eliminates the source of common mode noise by connecting the input and output terminal grounds. With six switch devices, the proposed HA converter achieves another advantages such as improved circuit reliability, reduced circuit cost, flexibility and possibly reduced circuit cost.

Two new topology examples derived from the HA converter are analyzed, designed, and experimented in this dissertation to prove their performance and feasibility. The example circuits are created by merging single-ended DC-DC converter in the HA converter to cope with any polarity of AC voltage terminal. The examples are employed to special power conversion application, one for AC-DC rectification and the other for DC-AC inversion. According to their application, the example circuits omit unnecessary switches among the six switches to further simplify their structure and improve the efficiency. The omission also makes the understanding of the topologies straightforward. Various experimental results including comparison to the conventional counterpart prove the advantages of the new topologies born from the HA converter.

Chapter 2 reviewed the common mode EMI and illustrated the topological derivation by systematically combining single inductor and two voltage sources. The combination method is simple and intuitive to derive new topologies. The HA converter is derived to eliminate the cause of the common mode current by using the systematic

combination method, i.e., arranging voltage sources with common ground and an inductor.

Chapter 3 showed a new AC-DC rectifier derived from the HA converter, the B3 rectifier. Principle of operation and control strategy of the B3 rectifier are illustrated in detail. Special feedforward is also designed to control both boost and buck-boost operation with low-bandwidth voltage loop. To prove the performance of the newly suggested B3 rectifier, a conventional boost rectifier with bridge diodes is also built and compared with the B3 rectifier. The comparison of the experimental results of the two rectifier circuits proves that the B3 rectifier shows lower common mode current and noise than the conventional counterpart with comparable efficiency. Power losses in the semiconductor devices are analyzed for further efficiency optimization.

Chapter 4 suggested a new DC-AC inverter derived from HA converter, the B3 inverter. Similar with Chapter 3, principle of operation and control strategy of the B3 inverter is articulated. To compare the performances of the suggested and the conventional inverters, an H-bridge inverter with bipolar modulation is also built along with the B3 inverter as the conventional counterpart. The common mode noise and efficiencies of the two circuits are measured and compared to conclude that the B3 inverter outperforms the conventional inverter. Especially, the common mode noise of the B3 inverter is smaller than that of the conventional inverter by 30 dBμV in low and medium frequency range.

The flexibility of the HA converter was highlighted in Chapter 5. With the insight that the HA converter is bilaterally symmetric, the versatility of the HA converter is explained. Three circuit configuration such as B4-I rectifier, B4-II rectifier, and B4-III

inverter are additionally derived from the HA converter by employing non-inverting buck-boost operation to overcome the limited operating condition, i.e., magnitudes of the input and output voltage.

For further works, efficiency optimization of the B3 rectifier should be fulfilled. Applying generic zero-voltage-switching or zero-voltage-transition auxiliary networks may help to reduce the switching loss of the semiconductors in the B3 rectifier and increase its efficiency. Also, expansion of the HA converter to the three-phase application should be considered. For example, the B3 inverter presented in Chapter 4 is focused on interfacing the single-phase AC source and the DC source. To apply the key idea of the connected ground to the three-phase systems, the topology should be extended to properly reduce the common mode current in another line connections such as corner grounded open delta and four-wire wye. For this, line current phase control should be considered to control not only the average power but also the complex power as the inverter output.

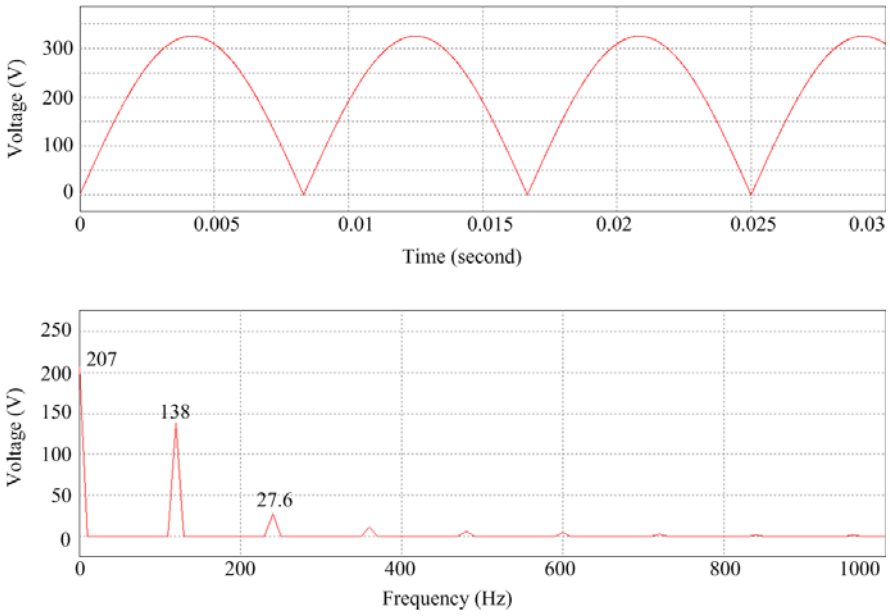
Appendix

A.1. Correction Factor of B3 Rectifier in Small Signal Model

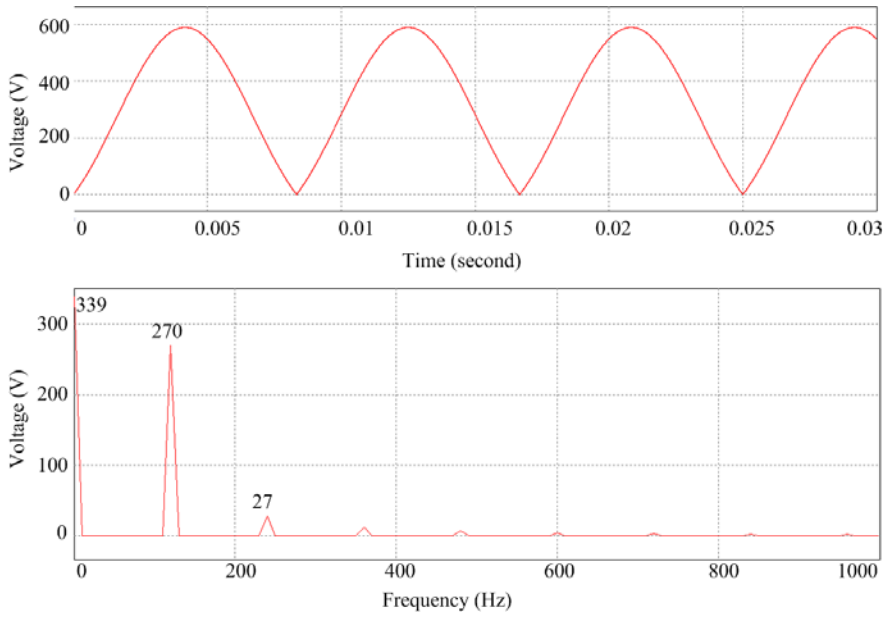
The control block and small signal diagrams of the average current mode two-loop controlled B3 rectifier are shown in Figs. 3.10 and 3.12. Sinusoidal input voltage is multiplied to the output of the voltage compensator to generate the inductor reference $\langle i_{Lb} \rangle^*$. The main idea of [48] is that the multiplication of a sinusoid in the time domain can be approximated to the multiplication of the rms value of the sinusoid in the frequency domain. According to the frequency spectrum of the rectified sinusoid shown in Fig. A.1(a), majority of the energy is concentrated in the DC component with the magnitude close to the rms value. Therefore the feedforward gain K_{ff} is simply the rms line voltage, $\frac{V_{g\max}}{\sqrt{2}}$, assuming that the line voltage sensing gain is unity.

In the control block and the small signal diagram of the B3 rectifier in the buck-boost converter mode, the correction term K_{corr} or $1+\frac{\left|V_{g\max}\sin\omega t\right|}{v_O}$ is additionally multiplied to the voltage compensator output and generates the buck-boost mode inductor current reference as indicated by the broken-line box in Fig. 3.10 and explained in Section 3.3.2. The total gain of the multiplication term $K_{ff\_bb}(t)$ in buck-boost converter operation is expressed in the time domain as in (A.1) and plotted in the time and frequency domains in Fig. A.1(b).

$$K_{ff\_bb}(t)=\left|V_{g\max}\sin\omega t\right|\left(1+\frac{\left|V_{g\max}\sin\omega t\right|}{v_O}\right) \tag{A.1}$$



(a)



(b)

Fig. A.1. Time and frequency domain plots of the feedforward signals in (a) boost and (b) buck-boost converter mode operation. $V_{g\max} = 230\sqrt{2}$ V and $v_O = 400$ V.

Similar with the rectified sine wave shown in Fig. A.1(a), $K_{ff\_bb}(t)$ is also approximated as the DC gain of its rms value in the small signal block diagram. Eq. (A.2) shows the definition of the rms of (A.1), K_{ff_bb} for a half-line cycle where T_L is the AC line period.

$$K_{ff\_bb} = \sqrt{\frac{2}{T_L}\int_{\frac{T_L}{2}} {K_{ff\_bb}}^2(t)dt} \tag{A.2}$$

Defining that $a = V_{g\max}$ and $b = \frac{{V_{g\max}}^2}{v_O}$, (A.2) is simplified as in (A.3).

$$K_{ff\_bb} = \sqrt{\frac{2}{T_L}\int_0^{\frac{T_L}{2}} \left\{ \left| V_{g\max}\sin\omega t \right| \left(1 + \frac{\left| V_{g\max}\sin\omega t \right|}{v_O} \right) \right\}^2 dt}$$

$$= \sqrt{\frac{1}{\pi}\int_0^{\pi} \left(a\sin(t) + b\sin^2(t) \right)^2 dt}$$

$$= \sqrt{\frac{a^2}{2} + \frac{8ab}{3\pi} + \frac{3b^2}{8}} \tag{A.3}$$

Considering the relationship between K_{ff_b}, K_{ff_bb}, and K_{corr} in (A.4) and assuming $V_{g\max} = 230\sqrt{2}$ and $v_O = 400$, K_{corr} is determined as 1.7.

$$K_{corr} = \frac{K_{ff\_bb}}{K_{ff\_b}} = \frac{\sqrt{\frac{\left(230\sqrt{2}\right)^2}{2} + \frac{8}{3\pi}230\sqrt{2}\frac{\left(230\sqrt{2}\right)^2}{400} + \frac{3}{8}\left(\frac{\left(230\sqrt{2}\right)^2}{400}\right)^2}}{230}$$

$$= 1.7 \tag{A.4}$$

A.2. Input Impedances of Boost and Buck-boost Converter

Mason's rule provides a convenient way to derive the system gain from the complicated signal flow graph [62]-[64]. According to the Mason's rule, the system gain

G is defined as in (A.5):

$$G = \frac{1}{\Delta}\sum_i G_i \Delta_i \ , \tag{A.5}$$

Terms such as node, path, forward path, loop, loop path, and loop gain in the Mason's rule and Δ, Δ_i, and G_i in (A.5) are defined in [64]. The block diagram in Fig. 3.21 is rearranged as in Fig. A.2 to derive total gain from $\hat{v}_g$ to $\hat{i}_L$ including the control loops. The block diagram in Fig. A.2 contains two forward paths as shown in (A.6) and (A.7).

$$G_{b1} = G_{ivg\_b} \tag{A.6}$$

$$G_{b2} = G_{vg\_b}\left(-K_v\right)G_v K_{ff\_b} G_c G_{id\_b} FM \tag{A.7}$$

Two loop gains l_{b1} and l_{b2} are in (A.8) and (A.9).

$$l_{b1} = G_{vd\_b}\left(-K_v\right)G_v K_{ff\_b} G_c FM \tag{A.8}$$

$$l_{b2} = \left(-K_i\right)H_e G_c G_{id\_b} FM \ , \tag{A.9}$$

System determinant Δ_b and forward path determinants Δ_{b1} and Δ_{b2} are in (A.10)-(A.12).

$$\Delta_b = 1 - \left(l_{b1} + l_{b2}\right) \tag{A.10}$$

$$\Delta_{b1} = 1 - l_{b1} \tag{A.11}$$

$$\Delta_{b2} = 1 - 0 \tag{A.12}$$

From (A.6) to (A.12), the input admittance of the boost mode operation is derived as in (A.13) which is equivalent to (3.30).

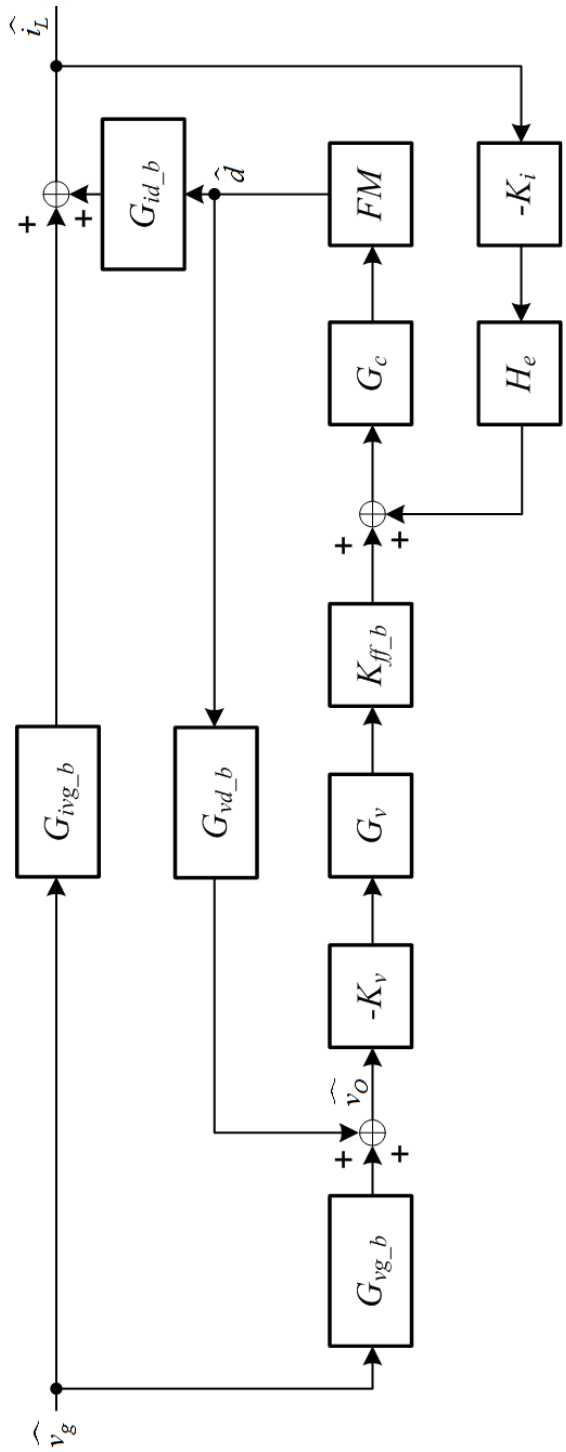


Fig. A.2. Rearranged block diagram of Fig. 3. 21 to derive Y_{i_b}.

$$Y_{i\_b} = \frac{1}{\Delta_b}\left(G_{b1}\Delta_{b1} + G_{b2}\Delta_{b2}\right)$$

$$= \frac{G_{ivg\_b}\left(1 + G_{vd\_b}K_vG_vK_{ff\_b}G_cFM\right) - G_{vg\_b}K_vG_vK_{ff\_b}G_cG_{id\_b}FM}{1 + G_{vd\_b}K_vG_vK_{ff\_b}G_cFM + K_iH_eG_cG_{id\_b}FM} \tag{A.13}$$

The block diagram in Fig. 3.22 is rearranged as shown in Fig. A.3. It contains three forward paths as shown in (A.14)-(A.16).

$$G_{bb1} = G_{igvg\_bb} \tag{A.14}$$

$$G_{bb2} = G_{vg\_bb}\left(-K_v\right)G_vK_{ff\_bb}G_cG_{id\_bb}FM \tag{A.15}$$

$$G_{bb3} = G_{ivg\_bb}\left(-K_i\right)H_eG_cG_{id\_bb}FM \tag{A.16}$$

Two loop gains l_{bb1} and l_{bb2} are in (A.17) and (A.18).

$$l_{bb1} = G_{vd\_bb}\left(-K_v\right)G_vK_{ff\_bb}G_cFM \tag{A.17}$$

$$l_{bb2} = G_{id\_bb}\left(-K_i\right)H_eG_cFM\ , \tag{A.18}$$

System determinant Δ_{bb} and forward path determinants Δ_{bb1}, Δ_{bb2}, and Δ_{bb3} are in (A.19)-(A.22).

$$\Delta_{bb} = 1 - \left(l_{bb1} + l_{bb2}\right) \tag{A.19}$$

$$\Delta_{bb1} = 1 - \left(l_{bb1} + l_{bb2}\right) \tag{A.20}$$

$$\Delta_{bb2} = 1 - 0 \tag{A.21}$$

$$\Delta_{bb3} = 1 - 0 \tag{A.22}$$

From (A.14) to (A.22), the input admittance of the buck-boost mode operation is derived

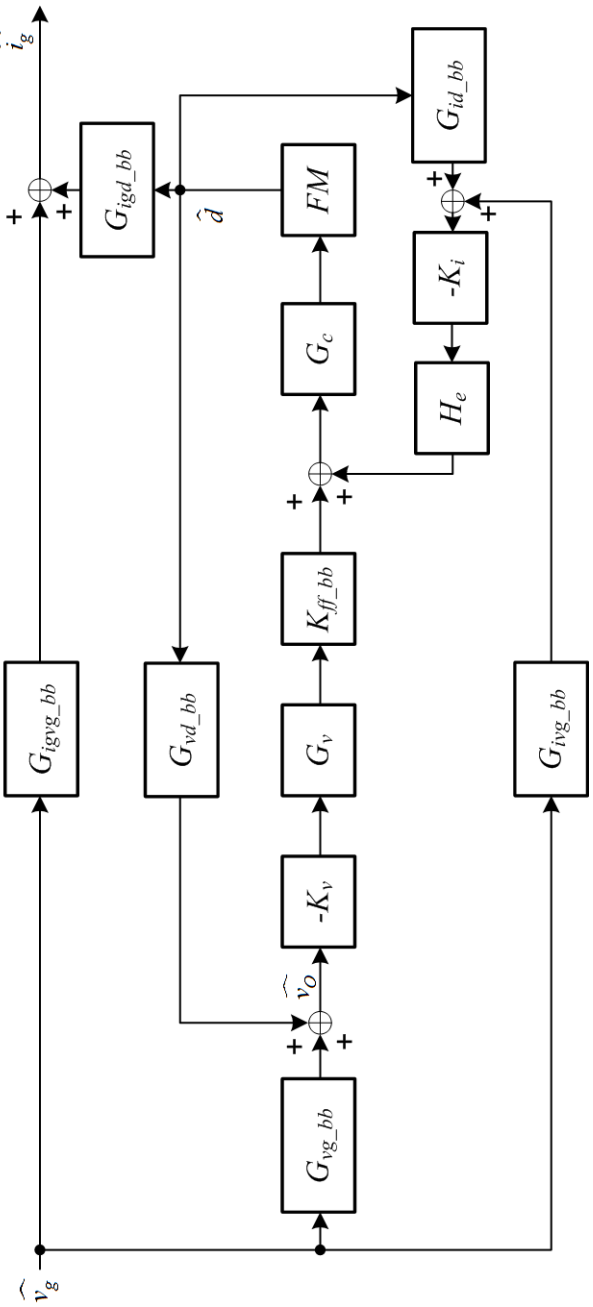


Fig. A.3. Rearranged block diagram of Fig. 3. 22 to derive Y_{i_bb}.

as in (A.23) which is equivalent to (3.35).

$$Y_{i\_bb} = \frac{1}{\Delta_{bb}}\left(G_{bb1}\Delta_{bb1} + G_{bb2}\Delta_{bb2} + G_{bb3}\Delta_{bb3}\right)$$

$$= G_{bb1} + \frac{1}{\Delta_{bb}}\left(G_{bb2} + G_{bb3}\right)$$

$$= G_{igvg\_bb} - \frac{G_{vg\_bb}K_v G_v K_{ff\_bb} G_c G_{id\_bb} FM + G_{ivg\_bb} K_i H_e G_c G_{id\_bb} FM}{1 + G_{vd\_bb} K_v G_v K_{ff\_bb} G_c FM + G_{id\_bb} K_i H_e G_c FM} \tag{A.23}$$

A.3. Loss Estimation of B3 Rectifier Switches

Power losses of B3 rectifier semiconductor switches are classified in two: conduction and switching loss. Table A.1 summarizes nomenclature related to the switching and conduction losses of switch devices according to the line voltage polarity. Q_2 and D_1 in positive half-line cycle and Q_6 and D_4 in negative half-line cycle show no switching loss because they do not switch.

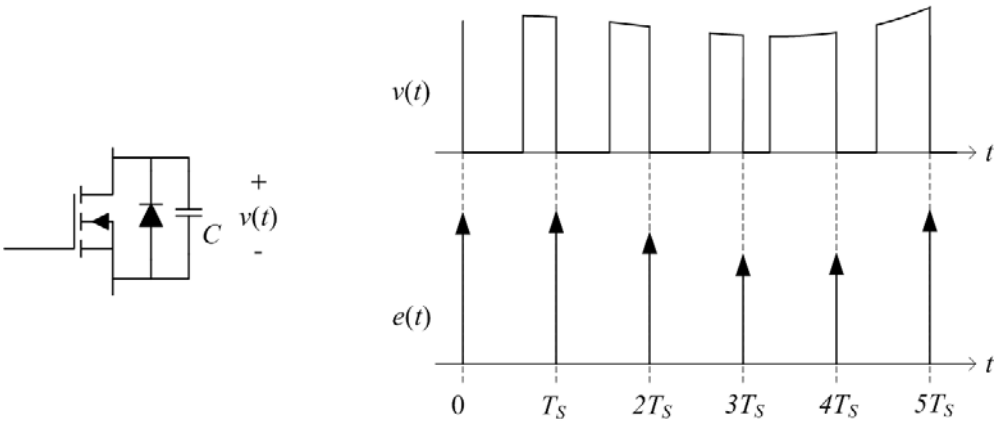
A.3.1. Switching Losses

Table A.1. Nomenclature of power losses in B3 rectifier switches

loss / device	positive half-line cycle		negative half-line cycle	
	switching	conduction	switching	conduction
Q_2	not exist	P_{CQ2p}	P_{SQ2n}	P_{CQ2n}
D_1	not exist	P_{CD1p}	neglected	P_{CD1n}
Q_6	P_{SQ6p}	P_{CQ6p}	not exist	P_{CQ6n}
D_4	neglected	P_{CD4p}	not exist	P_{CD4n}

Switching loss of the semiconductor devices is originated by parasitic parallel capacitance of the device, e.g., junction capacitance of the reverse-biased diode and output capacitance of MOSFET. However, switching losses of D_4 in positive half-line and D_1 in negative half-line cycle are neglected in this Appendix because diode junction capacitance are sufficiently smaller than MOSFET output capacitances and gives negligible contribution to the power loss of the B3 rectifier.

MOSFET switching loss in power electronics circuit is determined by the energy dissipated from the capacitance, and the energy is generated in discrete way synchronized with the turn-on instant as shown in Fig. A.4. In Fig. A.4(b), C, $e(t)$, and $v(t)$ are parasitic capacitance of MOSFET, instantaneous energy dissipated from the capacitance, and voltage across MOSFET. The energy is dissipated once in a switching period and thus shown as a series of weighted delta functions. Power is the sum of energy divided by a certain time interval by definition, and the power loss of the parasitic capacitance during n switching periods is therefore expressed as in (A.24):



(a) (b)

Fig. A.4. Switching loss of MOSFET: (a) circuit diagram and (b) energy and power waveform.

$$P_S = \frac{1}{nT_S}\left(\sum_{k=1}^{n}\frac{1}{2}Cv(kT_S)^2\right), \tag{A.24}$$

where P_S and T_S are switching power loss and switching period. The summation in parentheses is the total energy dissipated from the capacitance during the time interval nT_S. If $v(t)$ is constant as V, (A.24) is simplified as (A.25), which is widely used in DC-DC converter switching loss estimation.

$$P_S = \frac{1}{nT_S}\sum_{k=1}^{n}\frac{1}{2}CV^2 = \frac{1}{T_S}\frac{1}{2}CV^2 \tag{A.25}$$

In the boost converter operation in positive half-line cycle, switching loss of Q_6, P_{SQ6p}, is easily expressed in mathematic form such as in (A.26), because the voltage stress of Q_6 is fixed as the constant rectifier output voltage v_O.

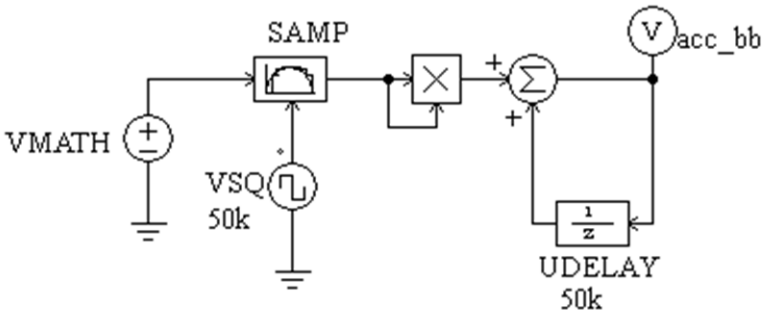
$$P_{SQ6p} = \frac{1}{2}C_{Q6}{v_O}^2 f \tag{A.26}$$

In (A.26), C_{Q6} and f are output capacitance of Q_6 and switching frequency respectively. Considering C_{Q6} is 230 pF from the datasheet [66] and f is 50 kHz, P_{SQ6p} is calculated as 0.92 W as in (A.27).

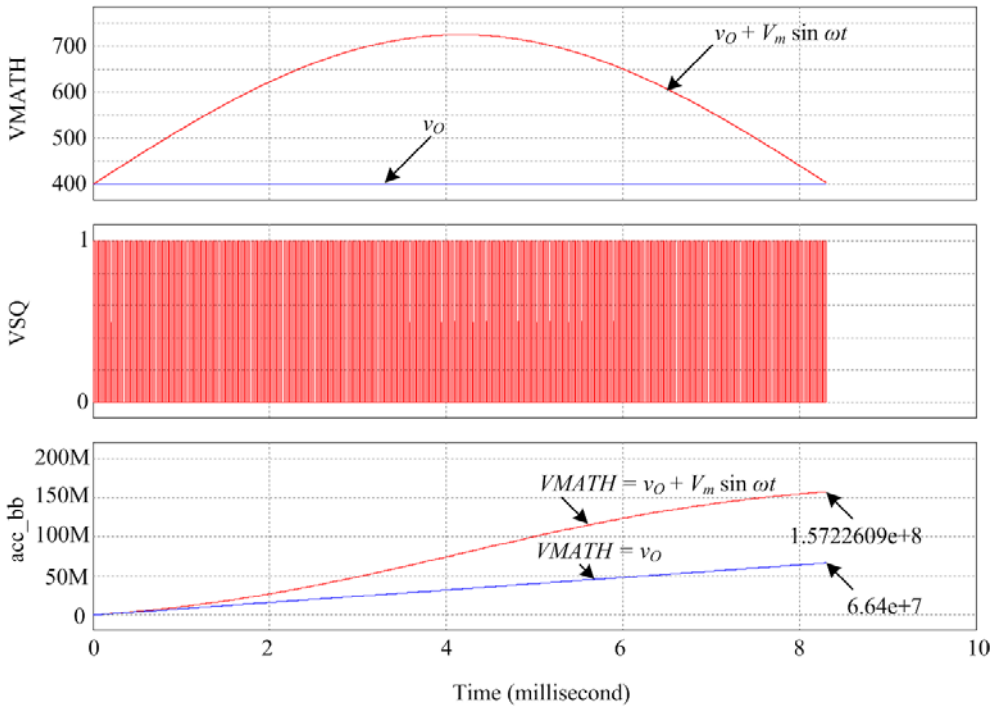
$$P_{SQ6p} = \frac{1}{2}\left(230\cdot10^{-12}\right)\left(400\right)^2\left(50\cdot10^3\right) = 0.92\ \text{W} \tag{A.27}$$

Being different from P_{SQ6p}, the switching loss of Q_2 in buck-boost operation, P_{SQ2n}, is not expressed in implicit form because the voltage stress across Q_2 is not constant but rather changes during the negative half-line cycle. Assuming T_{ac} is a half of line period and C_{Q2} is the output capacitance of Q_2, turn-on loss of Q_2 during the negative half-line cycle P_{SQ2n} is as (A.28):

$$P_{SQ2n} = \frac{1}{T_{ac}} \sum_{k=1}^{\left\lceil \frac{T_{ac}}{T_S} \right\rceil} \frac{1}{2} C_{Q2} v(kT_S)^2 = \frac{1}{2T_{ac}} C_{Q2} \left(\sum_{k=1}^{\left\lceil \frac{T_{ac}}{T_S} \right\rceil} v(kT_S)^2 \right) \tag{A.28}$$



(a)



(b)

Fig. A.5. (a) Simulation for summation. (b) Summation results according to VMATH.

The summation in (A.28) is calculated by PSIM simulation to avoid complicated mathematics.[3] Fig. A.5(a) shows the simulation diagram to achieve the summation or the term in the parentheses in (A.28). The voltage across the MOSFET is sampled, squared, and accumulated to achieve the summation in the simulation. VMATH is a math-expressed voltage source that represents the voltage stress of the MOSFET, which is the sum of the input and output voltage of the B3 rectifier as in (A.29):

$$\text{VMATH} = v_O + V_{g\max} \sin \omega t , \tag{A.29}$$

where v_O, $V_{g\max}$, and ω are 400 V, $230\sqrt{2}$ V, and 120π rad/s. SAMP in Fig. A.5(a) is a sample-and-hold block that samples VMATH in switching frequency according to a square-wave voltage source VSQ of which the frequency and the duty cycle are 50 kHz and 0.1. Sampled VMATH voltages are squared and accumulated by multiplication, summation, and unit delay block UDELAY of which the sampling frequency is also 50 kHz. A voltage probe acc_bb outputs the summation result. Fig. A.5(b) exhibits the simulation results that the summation in (A.27) is 1.5722609e+8. Considering T_{ac} is 0.0083 seconds and C_{Q2} is 455 pF [67], P_{SQ2n} is calculated as 4.29 W according to (A.28) as shown in (A.30).

$$P_{SQ2n} = \frac{1}{2 \cdot 0.0083}\left(455 \cdot 10^{-12}\right)\left(1.5722609 \cdot 10^{8}\right) = 4.29 \text{ W} \tag{A.30}$$

To prove the accuracy of the simulation, P_{SQ6p} is again calculated using the simulation to compare the value with the result achieved in (A.27). VMATH is set as v_O or constant 400 V, which is the voltage stress of Q_6 in the positive half-line cycle, and

[3] Eq. (A.28) is equal to $\frac{1}{2} C_{Q2}\left({v_O}^2 + \frac{4}{\pi} V_{g\max} v_O + \frac{1}{2} {V_{g\max}}^2 \right)\frac{1}{T_S}$ after some manipulation.

the summation result is 6.64e+7 as shown in Fig. A.5(b). Reminding that C_{Q6} is 230 pF, P_{SQ6p} is calculated as 0.9163 W as in (A.31).

$$P_{SQ6p} = \frac{1}{2 \cdot 0.0083}\left(230 \cdot 10^{-12}\right)\left(6.64 \cdot 10^{7}\right) = 0.9163\ \text{W} \tag{A.31}$$

Comparing (A.27) and (A.31) confirms that the loss estimation by simulation demonstrates negligible error, comparing with the estimation by mathematic analysis.

A.3.2. Conduction Losses

To simplify conduction loss calculation, inductor current slope is neglected assuming that the inductance is sufficiently large.

Conduction loss in MOSFET is calculated by (A.32):

$$P_{CQ} = I_{rms}{}^{2} R_{ds}\,, \tag{A.32}$$

where P_{CQ}, I_{rms}, and R_{ds} are conduction loss, rms current, and on-state drain-to-source resistance of the MOSFET respectively, and conduction loss in diode is by (A.33):

$$P_{CD} = I_{avg} V_F\,, \tag{A.33}$$

where P_{CD}, I_{avg}, and V_F are conduction loss, average current, and forward voltage drop of the diode.

- In Positive Half-line Cycle

Inductor current in the positive half-line cycle i_{Lp} is sinusoidal as in Section 3.3.2 and (A.34), and its rms value i_{Lprms} is shown in (A.35).

$$i_{Lp} = I_m \sin \omega t \tag{A.34}$$

$$i_{Lprms} = \frac{I_m}{\sqrt{2}} \tag{A.35}$$

In 230 Vac input and 500 W output operation, i_{Lprms} is determined as in (A.36).

$$i_{Lprms} = \frac{500}{\frac{V_{g\max}}{\sqrt{2}}} = 2.17\,\text{A} \tag{A.36}$$

Q_2 is fully turned on and inductor current flows through it and D_1 is reverse-biased and experiences no current, and their conduction losses are in (A.37) and (A.38):

$$P_{CQ2p} = {i_{Lprms}}^2 R_{dsQ2} = 2.6465\,\text{W}, \tag{A.37}$$

$$P_{CD1p} = 0\,\text{W}, \tag{A.38}$$

where R_{dsQ2} in (A.37) is on-state drain-to-source resistance of Q_2, 0.56 Ω [67].

Q_6 operates as the boost converter switch and its rms current is determined in (A.39), of which detailed derivation is shown in [68].

$$i_{Q6prms} = i_{Lprms}\sqrt{1 - \frac{8}{3\pi}\frac{v_O}{V_{g\max}}} \tag{A.39}$$

Conduction loss in Q_6 is therefore determined as in (A.40):

$$P_{CQ6p} = {i_{Q6prms}}^2 R_{dsQ6} = 0.5856\,\text{W}, \tag{A.40}$$

where R_{dsQ6} in (A.40) is on-state drain-to-source resistance of Q_6, 0.4 Ω [66].

Average current in D_4 is same as output load current I_O, and the conduction loss of D_4 is as (A.41).

$$P_{CD4p} = I_O V_{FD4} = \frac{P}{v_O} V_{FD4} = \frac{500}{400} 1.8 = 2.25\,\text{W} \tag{A.41}$$

V_{FD4} is the forward voltage drop of D_4 in (A.41) as 1.8 V [69].

- In Negative Half-line Cycle

Inductor current in the negative half-line cycle i_{Ln} is not a sinusoid but the sum of sinusoid and squared sinusoid as in (A.42).

$$i_{Ln} = \left(1 + \frac{V_{g\max}\sin\omega t}{v_O}\right) I_m \sin\omega t \tag{A.42}$$

Rms value of i_{Lnrms} is derived in (A.43).

$$\begin{aligned}
i_{Lnrms} &= \sqrt{\frac{1}{T_{ac}}\int_{T_{ac}}^{2T_{ac}} \left\{\left(1 + \frac{V_{g\max}\sin\omega t}{v_O}\right) I_m \sin\omega t\right\}^2 dt} \\
&= \sqrt{\frac{1}{\pi}\int_0^{\pi} {I_m}^2 \left(\sin t + \frac{V_{g\max}}{v_O}\sin^2 t\right)^2 dt} \\
&= \left[\frac{{I_m}^2}{96}\left\{12\left(3\left(\frac{V_{g\max}}{v_O}\right)^2 + 4\right)t + 3\left(\frac{V_{g\max}}{v_O}\right)^2 \sin 4t - 24\left(\left(\frac{V_{g\max}}{v_O}\right)^2 + 1\right)\sin 2t\right.\right. \\
&\quad \left.\left. -144\left(\frac{V_{g\max}}{v_O}\right)\cos t + 16\left(\frac{V_{g\max}}{v_O}\right)\cos 3t\right\}\right]_0^{\pi} \\
&= \frac{I_m}{\sqrt{2}}\sqrt{1 + \frac{16}{3\pi}\frac{V_{g\max}}{v_O} + \frac{3}{4}\left(\frac{V_{g\max}}{v_O}\right)^2} \\
&= i_{Lprms}\sqrt{1 + \frac{16}{3\pi}\frac{V_{g\max}}{v_O} + \frac{3}{4}\left(\frac{V_{g\max}}{v_O}\right)^2}
\end{aligned} \tag{A.43}$$

Q_2 operates as the buck-boost converter switch and its rms current i_{Q2nrms} is determined in (A.44).

$$\begin{aligned}
i_{Q2nrms} &= \sqrt{\frac{1}{T_{ac}}\int_0^{T_{ac}} \left(\frac{1}{T_S}\int_t^{t+T_S} i_{Q2}(\tau)^2 d\tau\right) dt} \\
&= \sqrt{\frac{1}{T_{ac}}\int_0^{T_{ac}} d_{bb}{i_{Ln}}^2 dt} \\
&= \sqrt{\frac{1}{T_{ac}}\int_0^{T_{ac}} \left(\frac{v_O}{v_O + V_{g\max}\sin\omega t}\right)\left\{\left(1 + \frac{V_{g\max}\sin\omega t}{v_O}\right) I_m \sin\omega t\right\}^2 dt}
\end{aligned} \tag{A.44}$$

$$= \sqrt{\frac{{I_m}^2}{T_{ac}} \int_0^{T_{ac}} \sin^2 \omega t + \frac{V_{g\max}}{v_O} \sin^3 \omega t dt}$$

$$= \frac{I_m}{\sqrt{2}} \sqrt{1 + \frac{8}{3\pi} \frac{V_{g\max}}{v_O}}$$

$$= i_{Lprms} \sqrt{1 + \frac{8}{3\pi} \frac{V_{g\max}}{v_O}} \tag{A.44}$$

Conduction loss in Q_2 is therefore as in (A.45).

$$P_{CQ2n} = {i_{Q2\,prms}}^2 R_{dsQ2} = {i_{Lprms}}^2 \left(1 + \frac{8}{3\pi} \frac{V_{g\max}}{v_O}\right) R_{dsQ2} = 4.3061\,\text{W} \tag{A.45}$$

Q_6 is fully turned on and inductor current flows through it and D_4 is reverse-biased and experiences no current, and their conduction losses are in (A.46) and (A.47).

$$P_{CQ6n} = {i_{Lnrms}}^2 R_{dsQ6} = {i_{Lprms}}^2 \left(1 + \frac{16}{3\pi} \frac{V_{g\max}}{v_O} + \frac{3}{4}\left(\frac{V_{g\max}}{v_O}\right)^2\right) R_{dsQ6} = 5.4375\,\text{W} \tag{A.46}$$

$$P_{CD4n} = 0\,\text{W} \tag{A.47}$$

Average current in D_1 is same as output load current I_O, and the conduction loss of D_1 is as (A.48).

$$P_{CD1n} = I_O V_{FD1} = \frac{P}{v_O} V_{FD1} = \frac{500}{400} 2.7 = 3.375\,\text{W} \tag{A.48}$$

V_{FD4} in (A.48) is the forward voltage drop of D_1 as 2.7 V [70].

Considering both positive and negative half-line cycles, the switching and conduction losses in semiconductor devices are as following.

$$P_{CQ2} = \frac{P_{CQ2p} + P_{CQ2n}}{2} = 3.4763\,\text{W} \tag{A.49}$$

$$P_{SQ2} = \frac{P_{SQ2n}}{2} = 2.145\,\text{W} \tag{A.50}$$

$$P_{CD1} = \frac{P_{CD1p} + P_{CD1n}}{2} = 1.6875\,\text{W} \tag{A.51}$$

$$P_{CQ6} = \frac{P_{CQ6p} + P_{CQ6n}}{2} = 3.0116\,\text{W} \tag{A.52}$$

$$P_{SQ6} = \frac{P_{SQ6p}}{2} = 0.4582\,\text{W} \tag{A.53}$$

$$P_{CD4} = \frac{P_{CD4p} + P_{CD4n}}{2} = 1.125\,\text{W} \tag{A.54}$$

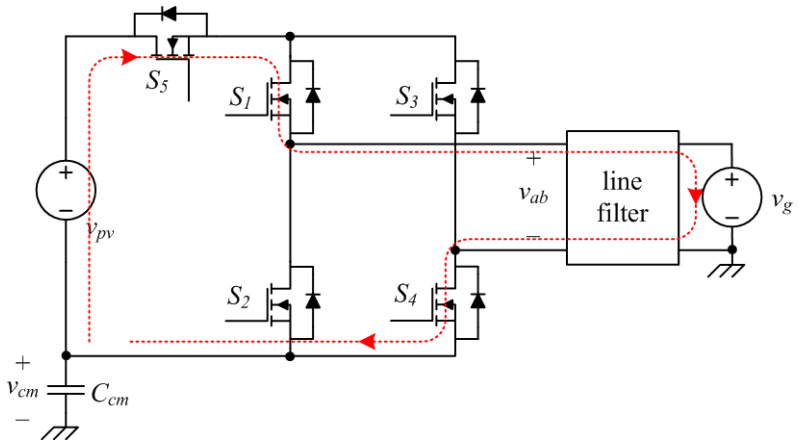
From (A.49) to (A.54), P_{CQ2}, P_{SQ2}, P_{CD1}, P_{CQ6}, P_{SQ6}, and P_{CD4} are conduction loss in Q_2, switching loss in Q_2, conduction loss in D_1, conduction loss in Q_6, switching loss in Q_6, and conduction loss in D_4 in a unit line cycle respectively. The pie chart in Fig. 3.32 shows the ratio of the loss in each device to the total estimated loss P_{tot}, which is in (A.55).

$$P_{tot} = P_{CQ2} + P_{SQ2} + P_{CD1} + P_{CQ6} + P_{SQ6} + P_{CD4} = 11.9036\,\text{W} \tag{A.55}$$

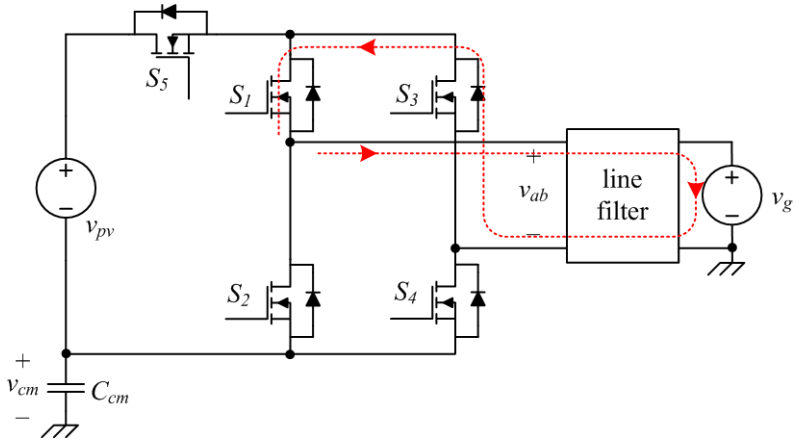
A.4. H5 and HERIC Inverter Operations

The operations of the H5 and HERIC inverter as the conventional counterparts of B3 inverter are articulated for further understanding in this Appendix. The H5 inverter [34] shown in Fig. 2.9 contains additional fifth switch, S_5, to separate the PV panel from the AC line during the freewheeling state. Switching states of the operation and corresponding current paths are summarized in Fig. A.6. States 1 and 2 (Figs. A.6(a) and

A.6(b) respectively) are repeated when the line voltage v_g is positive. When v_g is negative, states 3 and 4 (Figs. A.6(c) and A.6(d) respectively) occur. During the operation, switches in H-bridge are operated by the hybrid operation [60], i.e., S_1 and S_3 in AC line frequency and S_2 and S_4 in switching frequency. S_5 is synchronized to S_2 or S_4 according to the line voltage polarity: when v_g is positive, S_5 is synchronized with S_4, and when v_g is negative, S_5 is with S_2. S_5 goes off when the inverter is in the zero vector state to separate C_{cm} from the noise generation. Gate signals of H5 inverter



(a)

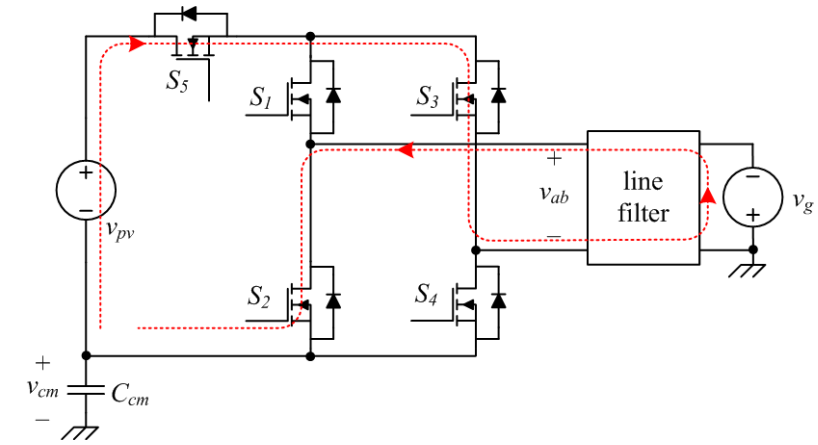


(b)

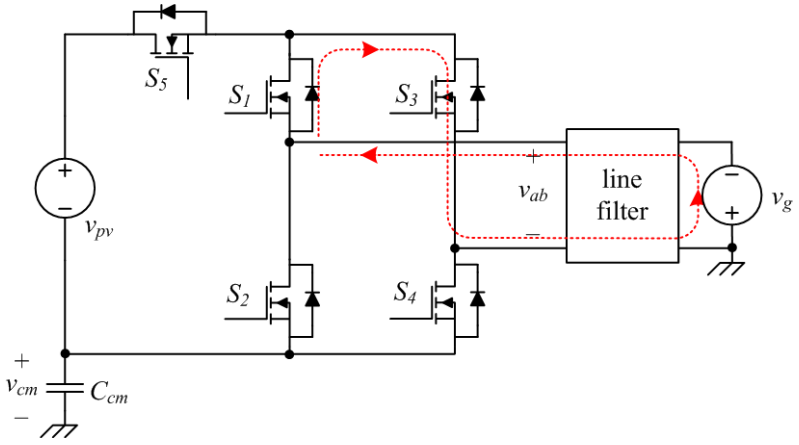
Fig. A.6. Operational states of the H5 inverter: (a) state 1 and (b) state 2.

is shown in Fig. A.7.

The HERIC inverter [33] shown in Fig. 2.10 is also one of the conventional counterparts of the B3 inverter. As illustrated in Fig. 2.10, the HERIC inverter adds two semiconductor switches S_5 and S_6 which are connected back-to-back to separate the freewheeling current from the PV panel. Switching states of the operation and corresponding current paths are summarized in Fig. A.8. States 1 and 2 (Figs. A.8(a) and A.8(b) respectively) are repeated when the line voltage v_g is positive. When v_g is



(c)



(d)

Fig. A.6. (Cont.) Operational states of the H5 inverter: (c) state 3 and (d) state 4.

negative, states 3 and 4 (Figs. A.8(c) and A.8(d) respectively) occur. Gate drive signals for S_1 to S_6 of the HERIC inverter are in Fig. A.9. For smooth current transition into the freewheeling state such as state 2 and state 4, S_5 and S_6 are fully turned on during the positive and negative line cycle respectively.

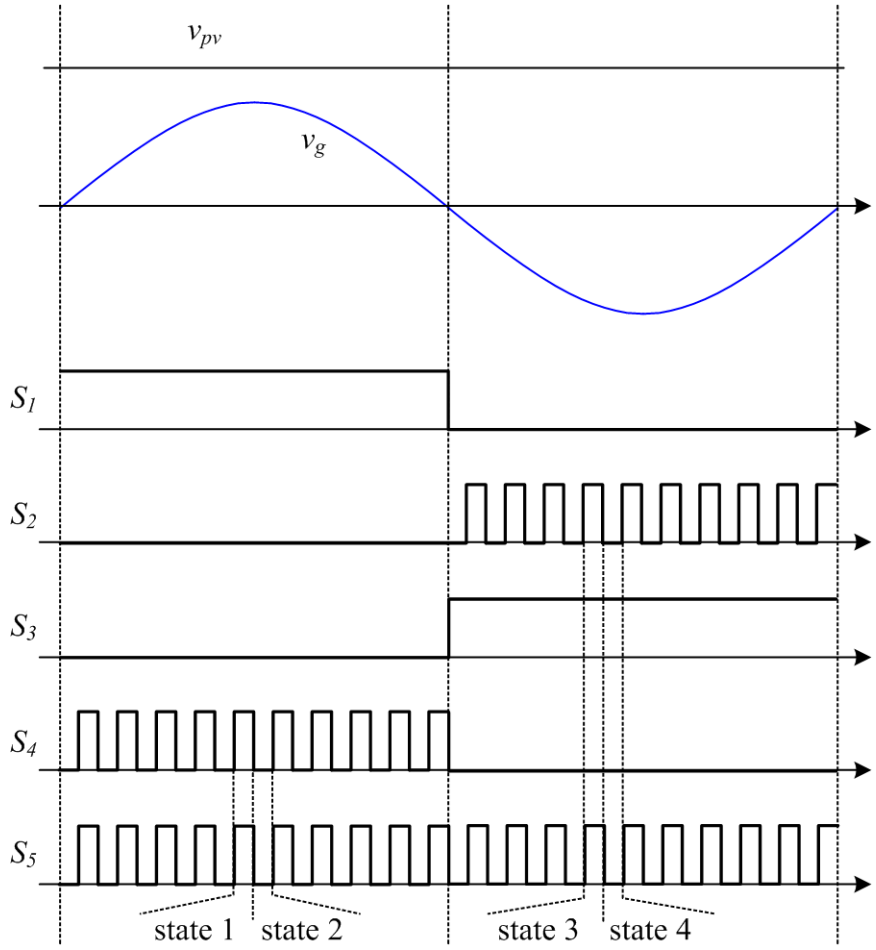
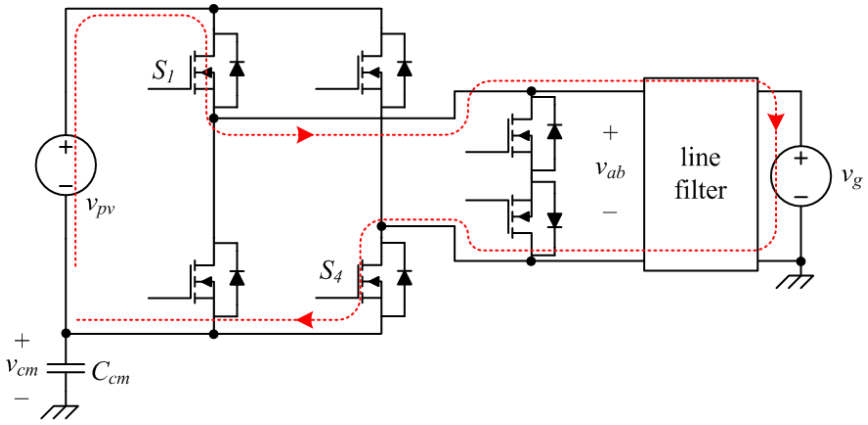
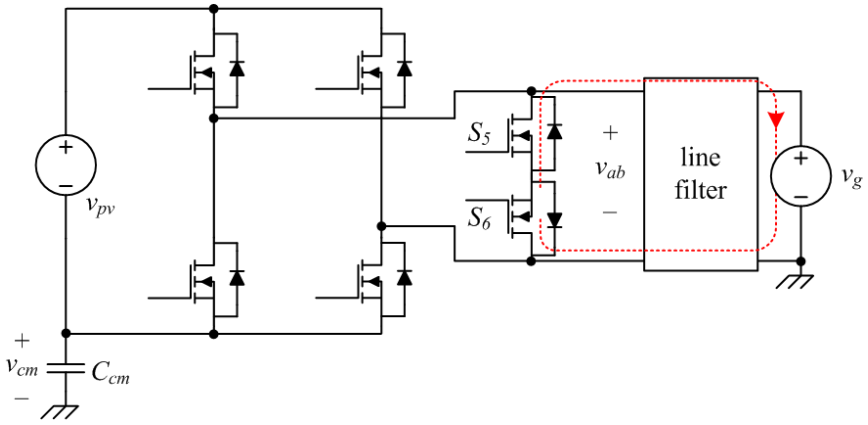


Fig. A.7. Gate signals of the H5 inverter during a line cycle.

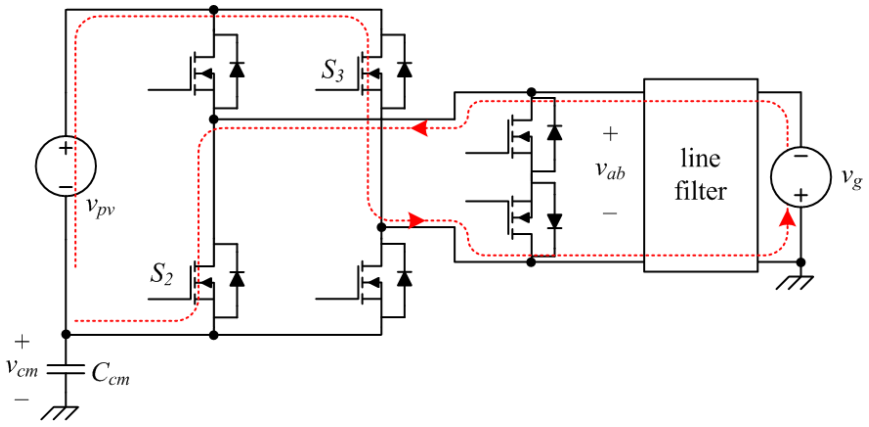


(a)

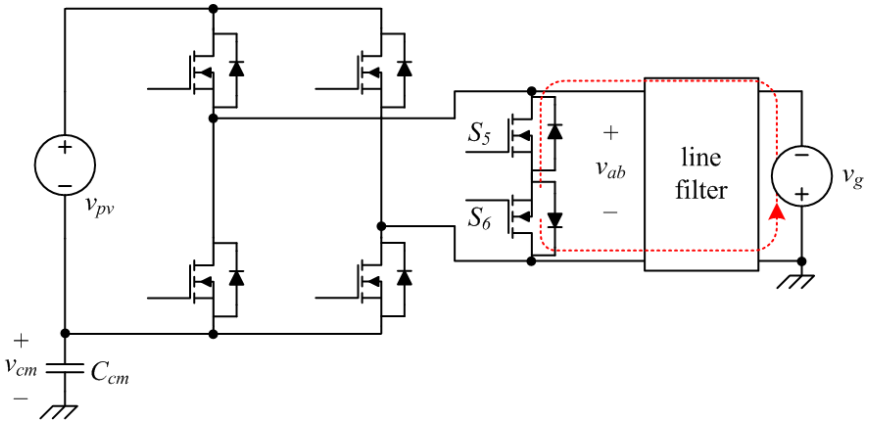


(b)

Fig. A.8. Operational states of the HERIC inverter: (a) state 1 and (b) state 2.



(c)



(d)

Fig. A.8. (Cont.) Operational states of the HERIC inverter: (c) state 3 and (d) state 4.

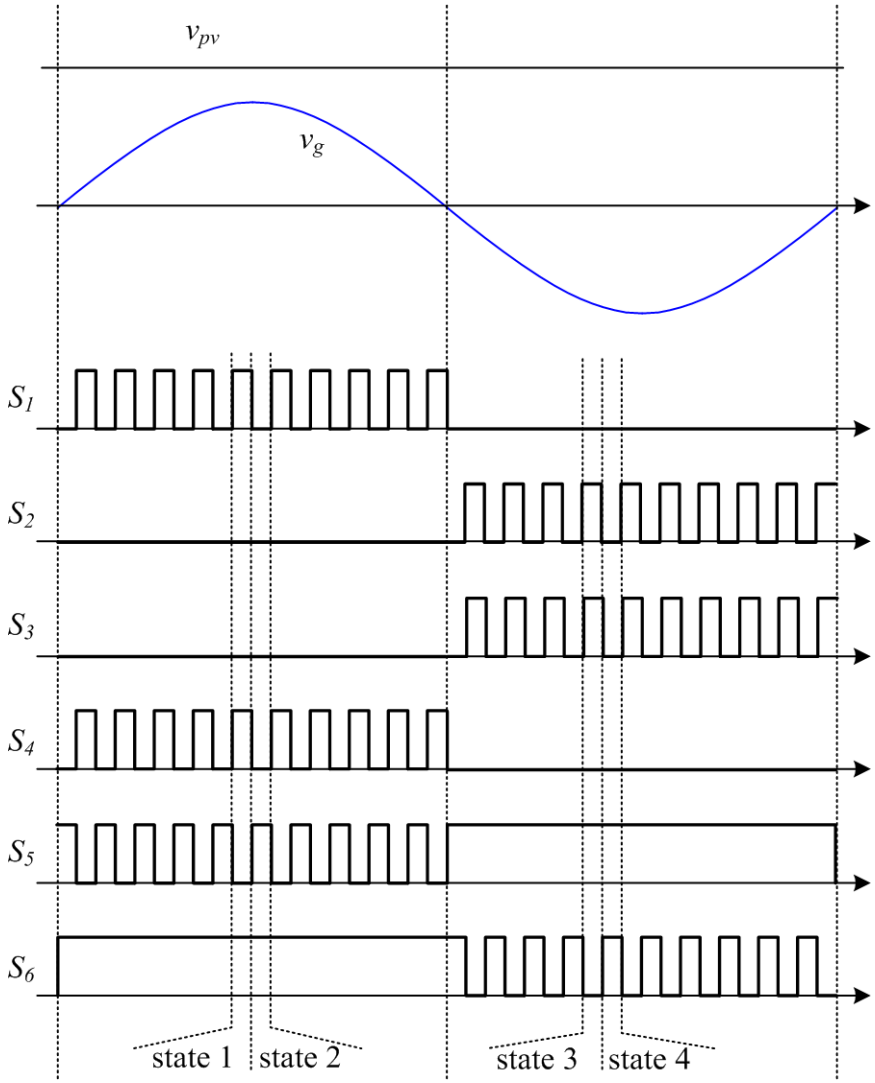


Fig. A.9. Gate signals of the HERIC inverter during a line cycle.

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국문 초록

본 논문은 구조가 간단하고 노이즈에 강인하며 유연성 및 확장성이 뛰어난 *추가 레그를 가지는 H-브릿지 컨버터(HA 컨버터)*를 제안한다. 새로이 제안하는 HA 컨버터는 하나의 인덕터를 가지는 싱글 엔드형(single-ended) DC-DC 컨버터의 일반적 구조로 작용하며, 스위치의 운전에 따라 벅 컨버터, 부스트 컨버터, 반전(inverting) 벅-부스트 컨버터, 그리고 비반전(non-inverting) 벅-부스트 컨버터로 동작할 수 있다. HA 컨버터의 입력 단자 측과 출력 단자 측의 기준 전위(ground)는 항상 연결되어 있는데, 이와 같은 구조는 기생 커패시턴스에 인가되는 고주파 전압을 억제하여 공통 모드 전류 및 공통 모드 노이즈를 크게 줄일 수 있다. 따라서 이 회로를 태양광 발전 시스템 및 독립 전원 시스템 등 기생 커패시턴스가 큰 전력 시스템에 적용할 경우 그 장점을 극대화할 수 있다.

본 논문에서는 HA 컨버터의 두 가지 실용적 예로서 AC-DC 변환을 위한 B3 정류기 및 DC-AC 변환을 위한 B3 인버터를 새로이 제안하고, 이들의 동작을 분석하며, 제어 알고리즘 및 필터를 설계한다. 또한 새 회로들의 성능을 분석하기 위해 실험을 수행하며, 기존 회로와의 비교 분석을 포함한 실험 결과를 통하여 B3 정류기 및 B3 인버터의 장점 및 실제 사용 가능성을 역설한다.

감사의 글

전기공학부에 입학한 지 십 년 만에 졸업을 합니다. 저의 이 작은 성취는 많은 분들의 진실한 도움과 따뜻한 배려가 있었기에 가능한 것이라 더욱 감개 무량합니다. 좁은 지면을 빌려 저의 부족한 글로나마 고마운 마음을 전합니다.

먼저, 저의 스승이신 조보형 교수님께 가장 큰 감사의 말씀을 올립니다. 제가 학부 시절에 접했던 교수님의 강의가 지금의 저를 있게 하였습니다. 대학원 과정을 밟는 6년 반 동안 교수님께서 몸소 보여주신 깊은 지식과 높은 인격, 그리고 부드러운 리더십은 제 삶의 훌륭한 모범입니다. 저의 논문심사 위원장이 되어 주신 설승기 교수님께도 깊은 감사의 뜻을 전합니다. 시간이 지나도 지칠 줄 모르는 교수님의 뜨거운 열정, 우국과 애국의 마음가짐, 그리고 유쾌함을 언제까지나 존경합니다. 심사 위원을 흔쾌히 맡아 주신 원충연 교수님께도 큰 감사의 마음을 전합니다. 교수님의 귀중한 지도 덕분에 더욱 나은 졸업 논문을 쓸 수 있었습니다. 하정익 교수님께도 진심을 담아 감사드립니다. 2011년 미국의 학회장에서 학회 안내 책자의 좁은 여백에 회로를 그려가며 나누었던 교수님과의 대화를 잊지 못합니다. 교수님의 번뜩이는 직관과 안목에 힘입어, 처음에는 작고 간단했던 저의 아이디어가 졸업 논문으로까지 발전했습니다. 먼 길의 수고로움도 마다하지 않고 저의 졸업 논문을 심사해 주신 선배, 최성진 교수님께도 큰 감사를 드립니다. 교수님의 꼼꼼하고 사려 깊은 지도가 더욱 좋은 논문의 밑거름이 되었습니다.

연구실 밖에서 저를 비롯한 후배들을 힘껏 이끌고 밀어 주시는 이규찬, 김정원, 이동영, 최항석 선배님께 감사의 마음을 전합니다. 선배님들의 배려와 마음 씀이 언제나 저희 후배들에게 큰 힘이 됩니다.

제가 연구실에서 배움을 시작하던 시절, 저를 많이 가르쳐 주신 이재호, 채수용, 김우섭, 현병철 선배님께도 고마움을 전합니다. 선배님들께서 전해 주신 지식과 경험, 그리고 삶의 태도는 저로 하여금 대학원 과정을 무사히 마칠 수 있게 해준 귀중한 원동력이었습니다.

또한 현재까지 저와 연구실에서 함께 부대끼는 동료들께도 진심으로 감사 드립니다. 열심으로 살아가는 여러분과 공유한 수많은 추억 덕에, 저의 20대 후반을 수놓은 연구실 생활을 멋지게 즐길 수 있었습니다. 먼저, 연구실 내에서 저와 가장 많은 시간을 공유한 종복 형께 감사 드립니다. 언제나 연구실을 위해 애쓰는 형의 모습을 통해 조용한 리더십과 사려 깊은 내조란 무엇인지를 배웠습니다. 항상 즐거운 분위기로 연구실을 이끄는 후배 규식에게도 고마움을 전합니다. 나와 가장 잘 어울리는 동료이자 소중한 친구 갑수에게 또한 진심 어린 감사를 전합니다. 함께 나누었던 수많은 아이디어와 고민, 그리고 공감은 오래도록 잊혀지지 않을 것입니다. 밝은 성격과 어울리는 환한 미소를 가진 창윤 형, 넓은 도량으로 모두에게 좋은 친구인 승운, 흔들리지 않는 성실함과 분석 능력은 물론 인간적인 따뜻함을 가진 바울, 꾸준한 노력으로 꿋꿋이 연구에 매진하는 혜진, 많은 독서량에 어울리는 유연한 정신을 가진 우인, 누구보다도 빠른 속도로 발전하는 제현에게도, 그리고 묵묵함과

성실함으로 실력을 닦고 있는 기봉, 두호, 준혁과 신입생 상우, 성현에게도 감사의 뜻을 전합니다. 또한, 논문에 실린 실험 결과를 얻는 데에 큰 도움을 준 후배 호준에게도 깊은 고마움을 전합니다. 호준의 훌륭한 실험 설계 및 수행 능력을 빌리지 않았다면, 제 논문은 쓰여지지 못했을 것입니다.

마지막으로, 언제나 저를 걱정해 주시고 응원해 주시는 저의 소중한 가족께 깊은 감사를 드립니다. 존경하는 아버님, 어머님, 장인 어르신, 장모님, 아끼는 동생 정민과 처남 문주, 그리고 사랑하는 아내 지현의 진심이 있었기에 학문에 정진하는 즐거움을 누릴 수 있었습니다.

저는 이제 정든 연구실을 나가 세상을 누빕니다. 앞으로 겪게 될 행복과 고난의 모든 순간에, 제가 대학원에서 받은 여러분의 선의와 신뢰, 그리고 기대를 떠올리며 감사하는 마음으로 열심히 살기를 다짐합니다.

고맙습니다.

2013년 1월,