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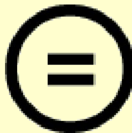

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공학박사 학위논문

The Characteristics and Reliability of In-Ga-Zn-O Thin-Film Transistors on Glass and Flexible Polyimide Substrate under Temperature and Illumination Stress

유리와 플라스틱 기판에 제작한 인듐갈륨징크 산화물 박막 트랜지스터의 온도와 빛의 특성 및 신뢰성에 관한 연구

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Abstract

The Characteristics and Reliability of In-Ga-Zn-O Thin-Film Transistors on Glass and Flexible Polyimide Substrate under Temperature and Illumination Stress

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Recently, flexible displays have attracted considerable attention in the emerging electronic device market. Flexible plastic substrates have the advantages such as flexibility, ruggedness and light-weight and its low cost, compared to glass substrate. Indium-Gallium-Zinc-Oxide thin-film transistors (IGZO TFTs) are promising candidates for next generation display backplane due to high mobility, good uniformity, and low process temperature, which suitable for flexible display.

In this thesis, the characteristics and reliability of flexible IGZO TFTs were presented and discussed.

Firstly, the electrical characteristics and reliability of IGZO TFTs on glass substrate are discussed. The IGZO TFTs were fabricated on a glass substrate with an inverted staggered structure. The initial electrical characteristics and gate bias induced instability was investigated. And drain bias induced instability is investigated. Unique degradation phenomenon was observed under the high

drain bias stress. After the high drain bias stress, the drain current, measured at the low drain bias, was significantly decreased. Based on the experimental results, I proposed a degradation model for the high drain bias induced degradation. And light-induced hysteresis of IGZO TFTs is investigated. Hysteresis was observed under the 450-nm illumination, and was increased with temperature. And hysteresis was increased with wavelength decrease. Light-induced hysteresis occurs due to increased sub-band gap states at the interface between the gate insulator layer and the active layer. Also, bias illumination stress induced instability is investigated. The transfer curve did not change after positive bias illumination stress. However, the transfer curve shifted to a negative direction after negative bias illumination stress. The transfer curve could be shifted to the negative direction after negative bias illumination stress due to the increase of V_O^{2+} states.

Secondly, the electrical characteristics and reliability of IGZO TFTs on flexible substrate are discussed. The IGZO TFTs were fabricated on a polyimide (PI) substrate with an inverted staggered structure. An inorganic buffer layer, composed of SiO_2 and SiN_x multi-layer, was employed, in order to prevent the environmental stress, such as water or oxygen molecules. The effects of PI and inorganic buffer layer on the characteristics and reliability of IGZO TFTs were investigated. And the effects of passivation layer on the electrical stability of IGZO TFTs with single passivation layer and double passivation layer fabricated on PI substrate were investigated. The positive bias stress and negative bias stress were applied to the IGZO TFTs at various temperatures from 20 °C to 80 °C. The threshold voltage shift of double passivation device was larger than that of single passivation device under NBTS. The threshold voltage shift of double passivation device was slightly less than that of single passivation device under PBTS. The threshold voltage shift of NBTS is considerably increased than that of PBTS at high temperature due to

the difference between conduction band offset and valence band offset. Lastly, the effects of mechanical bending on the electrical stability of flexible IGZO TFTs were investigated.

Keywords: thin-film transistor, Indium-Gallium-Zinc-Oxide (IGZO), flexible display, reliability
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Chapter 1 Introduction

Recently, flexible displays have attracted considerable attention in the emerging electronic device market. Flexible plastic substrates have the advantages such as flexibility, ruggedness and light-weight and its low cost, compared to glass substrate. Indium-Gallium-Zinc-Oxide thin-film transistors (IGZO TFTs) are promising candidates for next generation display backplane due to high mobility, good uniformity, and low process temperature, which suitable for flexible display. There have been a lot of attempts to apply the IGZO TFTs for flexible display, but still need more verification. Therefore, it is very critical to investigate the characteristics and reliability of flexible IGZO TFTs.

1.1 Evolution of display technology

Flat panel displays (FPDs) were considered a very attractive alternative to the cathode ray tube (CRT) as illustrated in Figure 1-1. There are various FPDs such as a liquid crystal display (LCD), a plasma display panel (PDP), an organic light emitting diode (OLED) display, and a field emission display (FED), which can be defined by the types of materials and the display method they use [1-4]. They have the merits providing large area, the slim and light-weight and high-resolution images, which are not achieved easily with CRTs and projection display.

Among all the FPDs, the most successful display technology to emerge so far is the LCDs. LCDs are thin, light-weight, bright and cost-effective due to the low-temperature process on glass substrates. Therefore, they have enabled successful applications to laptop computers or desktop monitors, which occupy the large portion of FPD market. Also, the low voltage drive for portable applications is possible, so that the target market is not limited by an increasing diverse set of systems.

The development of active matrix liquid crystal displays (AMLCDs) for high resolution and full-color display has been achieved by the thin-film transistors (TFTs). The active matrix display employing the TFT as a pixel switch has enhanced the capability of high quality image processing, so that the importance of LCDs in commercial fields increases. Hydrogenated amorphous silicon thin film transistors (a-Si:H TFTs) have been widely used for AMLCDs due to their high productivity on large area glass substrates by low temperature process below 400 °C. The a-Si TFT can represent the gray scale by switching the voltage data and charging the capacitors of each pixel element. However, the poor current driving characteristics of a-Si:H TFT due to the low field effect mobility

(< 0.5 cm^2/V·sec) are the limitation in realization of the high resolution display [5, 6].

The problem of low carrier mobility of a-Si:H TFTs can be solved by employing the polycrystalline silicon (Poly-Si) film as an active layer in the TFT. Generally, Poly-Si film is fabricated by recrystallization of the a-Si:H film deposited at low temperature below 400 °C. Poly-Si TFTs have attracted considerable attentions due to its high electron mobility (30 ~ 500 cm^2/V·sec) and current driving capability [7, 8]. Compared with an a-Si:H TFT, the superior electrical characteristics of the poly-Si TFT allow a fast switching, required for the high resolution image. In addition, poly-Si TFTs enable implementing the complementary metal oxide semiconductor (CMOS) technology and integrating the peripheral driver circuits and pixel switching devices simultaneously on a glass substrate.

ELA technologies have been extensively studied to fabricated high qualty poly-Si thin film on a large area glass substrate [8-10]. It employs the pulsed laser induced rapid heating of the a-Si film, and more than 90% of the excimer laser energy is absorbed within shallow depth (~20 nm) from the surface of a-Si film during the tens of nano-seconds of laser pulse duration. It is noted that the low temperature (< 400 °C) crystallization of a-Si film on a glass can be obtained by ELA without any thermal damage to the glass. Therefore, it is possible to integrate the digital and analog drivers such as inverter, level-shifter, shift register, digital-to-analog converter (DAC), and amplifier by employing low temperature poly-Si (LTPS) TFTs on the glass panel.

However, although the ELA LTPS TFT technology is attractive and researched widely due to its high performances, the electrical properties of the ELA LTPS TFTs are still insufficient to realize the high quality displays and need to be

improved yet in terms of the non-uniformity of grain-boundaries induced by the fluctuation of ELA energy. Additionally, the LTPS technology has a cost issue to fabricate TFTs compared with a-Si technology. The crystallization of a-Si film is critical to proceed to the stable process. The troublesome vacuum break process such as the crystallization and the doping process lead to low throughput and high sensitivity of electrical properties variation. Therefore, the conventional LTPS TFT process requires more process steps than a-Si TFT, decreasing the process yield.

In 1987, *C. W. Tang* and *S. A. VanSlyke* reported luminescence from an organic material [11]. They deposit small molecules to form a layered structure in a vacuum. The layered structure is sandwiched between an anode and cathode. The thin (< 1 μm) of organic material permits a high electric field at low voltage. Thus, a light from thin film organic materials is usually produced at low voltage. OLED displays exhibit superb electro-optical properties such as a fast response (~ several μsec) to the image addressing and a wide viewing angle due to self-emissive characteristics. Many research groups have been investigating new organic materials and new configurations of devices to improve efficiency and stability of OLED displays [12-15]. Therefore, AMOLED displays employing the TFT backplane have the potential for new technology comparable to the AMLCDs.

The electro-optical performance of AMOLED is very sensitive to the characteristics of TFT. A small variation of the OLED current in the each pixel may cause a critical non-uniform image problem because the OLED luminance is controlled by the current driving. Thus, each TFT pixel in AMOLED panel requires a constant current source that maintains a desired image data during the whole emission time.

For a reliable current driving with a low voltage in a limited pixel area, such as a

high density display, LTPS TFTs may be attracted as the pixel element rather than a-Si TFTs because they can supply sufficient OLED current by a small circuit area due to their high current driving capability. Although some LTPS TFT based AMOLED display have been shown, they need to be improved due to the current non-uniformity [14, 16]. The random creation of grain boundaries during the crystallization varies the output current in pixel to pixel due to the non-uniform field effect mobility and threshold voltage of the poly-Si TFT [8-10]. Therefore, the I_{OLED} compensation pixel circuits, which can compensate the non-uniform characteristics of poly-Si TFTs, are required for the uniform luminance in the display panel. There are two approaches to compensate the current variation: the voltage programming and the current programming, and each method have merits and drawbacks in itself [17, 18].

The a-Si technology widely used in AMLCDs is considered for large area AMOLED displays due to its low fabrication cost and excellent uniformity. However, the critical problem of the long-term device degradation would be a huge barrier to meet the needs for high quality. Therefore, the degradation of the a-Si:H TFT should be compensated by the pixel circuit and the new driving scheme to suppress the degradation of a-Si TFTs itself should be developed. This would require a rather complicated compensation circuit compared with the poly-Si TFT based pixel design. However, it is not easy to fabricate the compensation circuit in every pixel of limited dimension due to large size a-Si:H TFT components and the space required for the layout of additional signals and capacitors of the circuit.

Nowadays, TFT technology is challenging the realization of flexible displays on transparent plastic substrate and metal foil [19, 20]. Flexible plastic substrates have some merits such as flexibility, ruggedness and light-weight and its low cost, ultimately, compared with glass substrate. These merits make plastic substrate

attractive for portable systems such as a smart phone, and a tablet PC. However, the TFT technology on plastic substrate must overcome the limitation of process temperature. Plastic substrate has a much lower thermal budget, so that the process temperature of the TFT fabrication should be sufficiently low [21]. The most of commercially developed plastic substrates can stand low temperature below 200 °C, and the critical temperature of plastic substrates is determined by the inherent characteristics of plastics [21]. Limited process temperature affects the deposition of films and the physical properties of the films tend to be deteriorated with the decrease of the process temperature. Due to the lack of thermal treatment, characteristics of the TFTs on plastic may be degraded much compared with those of the TFTs on glass.

Oxide semiconductor materials are promising candidates for next generation display materials due to a relative high mobility, which is large enough to fabricate a high-speed transistor for driving the AMLCDs [22-24]. In addition, oxide semiconductor materials have an amorphous phase, which shows uniform electrical properties even with a large-size display [22, 25, 26]. High resolution, such as ultra-high defition (UD : 3840 × 2160), a high frame rate (> 240 Hz), and large size display (more than 70 inches) require the higher electrical performance than that of the a-Si TFTs. At least 3 $cm^2/V \cdot s$ of field-effect mobility is required to satisfy such demands, which is not so easy to achieve by the conventional amorphous silicon material [27].

Furthermore, the oxide semiconductor TFTs has advantageous to the AMOLED. In general, LTPS TFTs employed to drive AMOLEDs because they exhibit high mobility and good electrical stability than a-Si:H TFTs. However, the LTPS TFT has a problem with the uniformity which is originated from the non-uniform grain sizes in the poly-Si film. Consequently, the LTPS TFT is not suitable for the AMOLED TV. Even for a small size AMOLED panel, a compensation circuit is

required in order to maintain uniform image quality for the LTPS TFT. Therefore, many demonstrations of AMOLEDs driven by the oxide semiconductor TFTs have been shown [27, 28]. Figure 1-2 shows four-inch QVGA bottom-emission AMOLED display driven by oxide TFTs without any pixel compensation circuit [27].

Another advantage of the oxide semiconductor based TFTs over the silicon-based TFTs is that the oxide semiconductors are transparent in the visible light region. Zinc oxide based semiconductor, such as indium-gallium-zinc-oxide, exhibits large optical band gap (> 2.8 eV) compared to silicon-based semiconductor [29, 30]. Due to large band gap characteristics, the oxide semiconductor exhibits low leakage current.

Figure 1-1 The evolution of display technology.

Figure 1-2 Four-inch QVGA bottom-emission AMOLED display driven by oxide TFTs without any pixel compensation circuit. [27]

1.2 Outline of this thesis

This study focuses on the characteristics and reliability of flexible IGZO TFTs under various environments. Recent technical trend in flat panel display industry is the high resolution display and flexible display. In order to meet the two trends, IGZO TFTs are promising candidates. In this thesis, IGZO TFTs were fabricated on glass and flexible substrate, and investigated the characteristics and reliability under various environments.

Chapter 2 gives a brief introduction to the IGZO semiconductor. Recent issues of IGZO TFTs, such as reliability under negative bias illumination stress and reliability under various environments, are reviewed. Also, various backplane materials for flexible display are reviewed.

Chapter 3 focuses on the electrical characteristics and reliability of IGZO TFTs on glass substrate. Fabrication process and initial electrical characteristics of IGZO TFTs are introduced. Instability of IGZO TFTs under gate bias and drain bias without illumination is investigated. In addition, light-induced hysteresis phenomenon under various temperatures and wavelengths is investigated. Reliability of IGZO TFTs under illumination is also investigated.

Chapter 4 concentrates on the electrical characteristics and reliability of IGZO TFTs on flexible substrate. Comparison between IGZO TFTs on glass substrate and flexible substrate is investigated. The effects of buffer layer, passivation layer, and mechanical bending on the electrical characteristics and reliability of flexible IGZO TFTs are also investigated.

Lastly, I summarize the results of the characteristics and reliability of IGZO TFTs under various environments in Chapter 5.

Chapter 2 Review of IGZO TFTs and flexible display technology

The flexible IGZO TFTs is now considered as a next generation display technology in active matrix displays. In this chapter, the recent issues of IGZO TFTs, such as reliability under bias temperature stress, negative bias illumination stress, and various environments, are reviewed. Also, various backplane materials for flexible display are reviewed.

2.1 Recent issues of IGZO TFTs

In 2004, Nomura et al. reported an amorphous oxide semiconductors based on IGZO deposited at room temperature, and exhibited high mobility compared to amorphous silicon TFTs ($\mu_{sat} \approx 7\ cm^2/V{\cdot}s$) [22]. Despite the amorphous state, the origin of the high mobility was attributed to the electronic orbital structure of the material. Figure 2-1 shows schematic orbital drawings for the carrier transport paths in crystalline and amorphous semiconductors. Covalent semiconductors have carrier transport paths composed of strongly directive sp^3 orbitals, so structural randomness greatly degrades the magnitude of bond overlap, that is, carrier mobility [22]. However, amorphous oxide semiconductors composed of post-transition-metal cations. Spheres denote metal s orbitals. The contribution of oxygen 2p orbitals is small. Direct overlap between neighbouring metal s orbitals is rather large, and is not significantly affected even in an amorphous structure [22]. Therefore, amorphous oxide semiconductor could exhibits high mobility even in an amorphous phase.

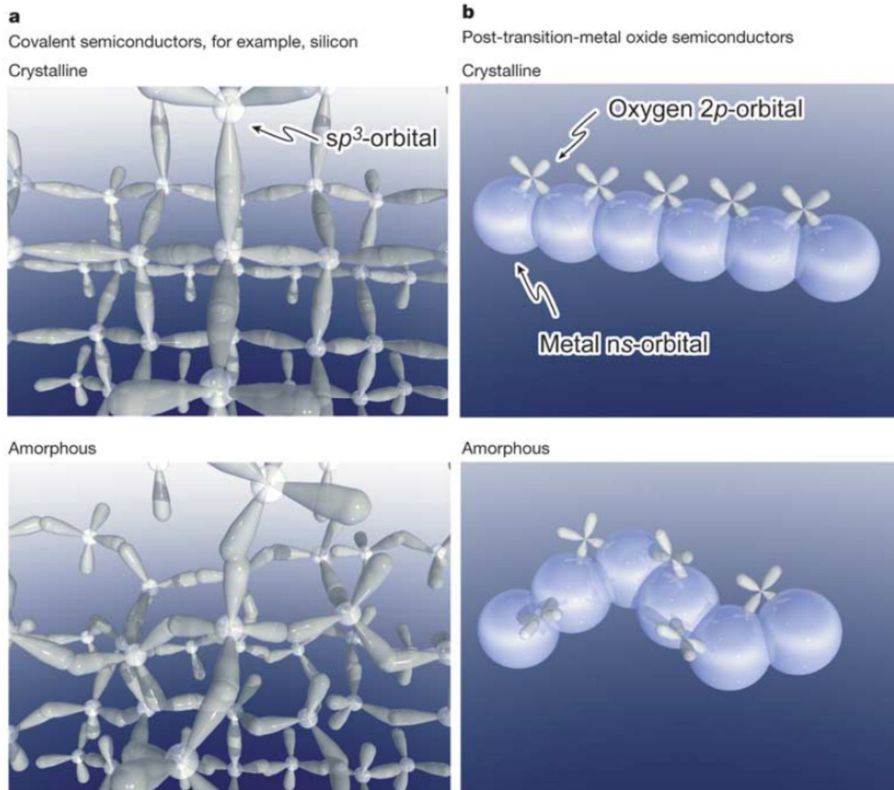


Figure 2-1 Schematic orbital drawings for the carrier transport paths in crystalline and amorphous semiconductors. (a) Covalent semiconductor, for example, silicon (b) oxide semiconductor. [22]

2.1.1 Reliability under bias temperature stress

For the stable operation, the device instability under the bias temperature stress should be investigated. During the operation of the display, TFTs have been applied positive or negative bias continuously. It is reported that threshold voltage is positively shifted under positive bias stress, while threshold voltage is scarcely shifted under negative bias stress. Figure 2-2 shows the comparison of the effect of a positive and a negative gate bias stress on the transfer characteristics. [31] The field effect mobility or the sub-threshold slope was not altered. When positive gate bias is applied to the IGZO TFTs, the electrons are accumulated at the channel, and electrons could be trapped at the interface between the IGZO and gate insulator layer. On the other hand, when negative gate bias is applied to the IGZO TFTs, the electrons are depleted at the channel, and electrons could not be trapped. Holes could not accumulate under negative bias, because IGZO is inherently n-type semiconductor.

Threshold voltage shift and hysteresis could be improved by high quality gate insulator or plasma treatment at the gate insulator [32-35]. Figure 2-3 (a) shows the variations in the V_{TH} shift for IGZO TFTs with various gate dielectrics (SiN_x 150 °C, SiN_x 350 °C, and SiO_x 350 °C) as a function of stress time [32]. The positive Vth shift in the a-IGZO TFTs with the SiN_x gate dielectric deteriorated significantly during constant bias stress due to the higher hydrogen content in the SiN_x films providing more charge trap sites, which would produce a high shallow hydrogen-related states. Figure 2-3 (b) shows the variations in the Von and mobility shift for IGZO TFTs with plasma treatment as a function of stress time [35]. The interface treatment by O_2 plasma significantly improves the stability of the a-IGZO TFT. This suggests that the V_{TH} shift is determined by the properties of the gate dielectrics, such as the density of charge traps.

The degradation mechanism is classified into the charge trapping and the defect state creation. The degradation mechanisms are originated from a-Si:H TFTs [36-39]. The charge trapping process shows the logarithmic time dependence and has very small temperature dependence. On the other hand, the defect state creation process shows the power law time dependence and is thermally activated [37, 39]. The stretched exponential time dependence could be fitted to the charge trapping process [36]. The fabrication process and structure of the IGZO TFTs are not same each other, so the experimental results are. Therefore, the degradation mechanism of IGZO TFTs under bias temperature stress is still debated [31-33, 40-47].

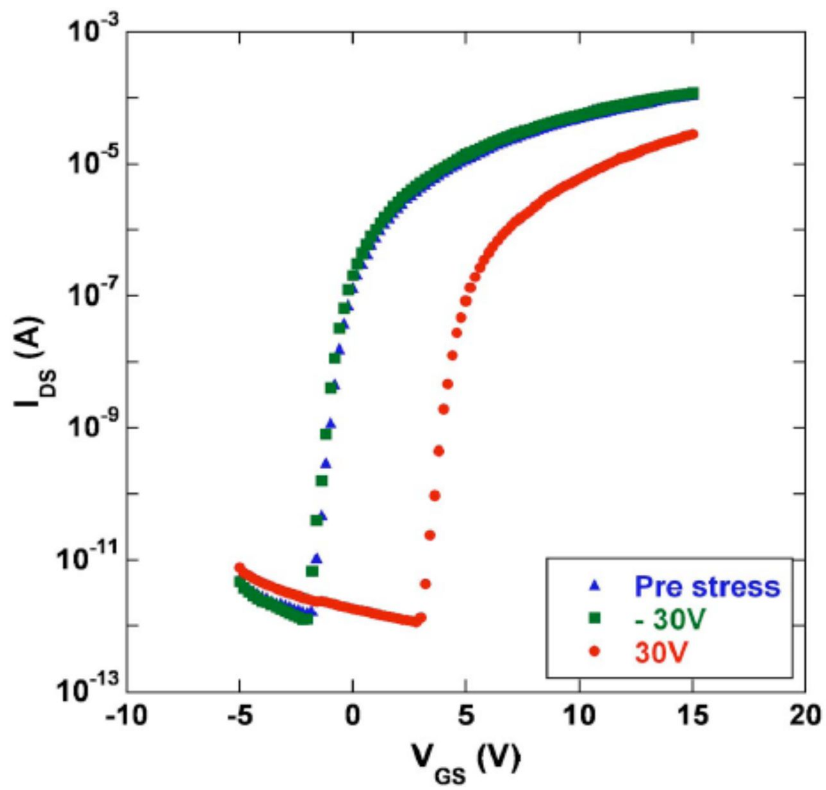
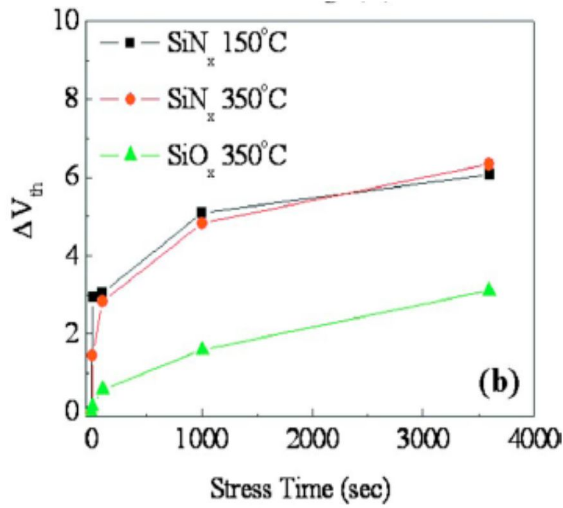
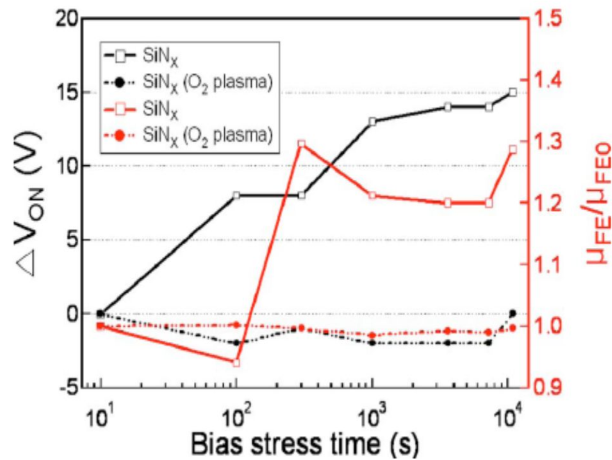


Figure 2-2 Comparison of the effect of a positive and a negative gate bias stress on the transfer characteristics. [31]



(a)



(b)

Figure 2-3 (a) The variations in the V_{TH} shift for IGZO TFTs with various gate dielectrics (SiN_x 150 °C, SiN_x 350 °C, and SiO_x 350 °C) as a function of stress time. [32] (b) The variations in the Von and mobility shift for IGZO TFTs with plasma treatment as a function of stress time. [35]

2.1.2 Reliability under negative bias illumination stress

For the stable operation, the device instability under the bias, thermal, illumination, and environmental stress have been intensively studied [31-35, 41, 43, 46, 48-78]. As a result, significant advances in reliability have been made. Nevertheless, reliability under negative bias illumination stress is still remained issue [51-68]. Since switching TFTs of active-matrix liquid crystal displays or organic light emitting diodes are almost always negatively biased and exposed to light during their operation, instability caused by the negative bias illumination stress is a crucial problem to be resolved [57]. Figure 2-4 shows transfer curves as a function of the applied -20 V negative bias stress (NBS) time (a) in the dark and (b) under green light exposure. The device did not suffer from any V_{on} shift by NBS in the dark. Meanwhile, V_{on} shift of -5.2 V with insignificant change in SS was observed under illumination.

In the case of amorphous silicon, prolonged light illumination reduces the conductivity of the a-Si film, which can be attributed to the formation of a meta-stable deep-level defect (so called Staebler–Wronski effect) [79, 80]. Therefore, a-Si TFTs under light illumination conditions would be affected adversely by stretching-out of the sub-threshold drain current [56].

In case of oxide TFTs, however, prolonged negative bias stress with light illumination results in a huge negative shift of the threshold voltage. A couple of degradation models have been proposed to account for this observation. First degradation model is the trapping of photo-generated hole carriers [51, 52]. Figure 2-5 shows the schematic energy band diagram to explain photo-induced hole trapping [51]. Second degradation model is photo-desorption of the oxygen-related molecules [60]. Figure 2-6 shows the schematic energy band diagram showing the photo-desorption of oxygen molecules into the ambient atmosphere

for the un-passivated device under the application of NBS [60]. Third degradation model is the creation of sub band gap states [57, 59]. Figure 2-7 shows the schematic energy band diagram showing the sub-band gap states related to oxygen vacancy [57]. However, the degradation mechanism to explain overall phenomenon is unclear at this stage.

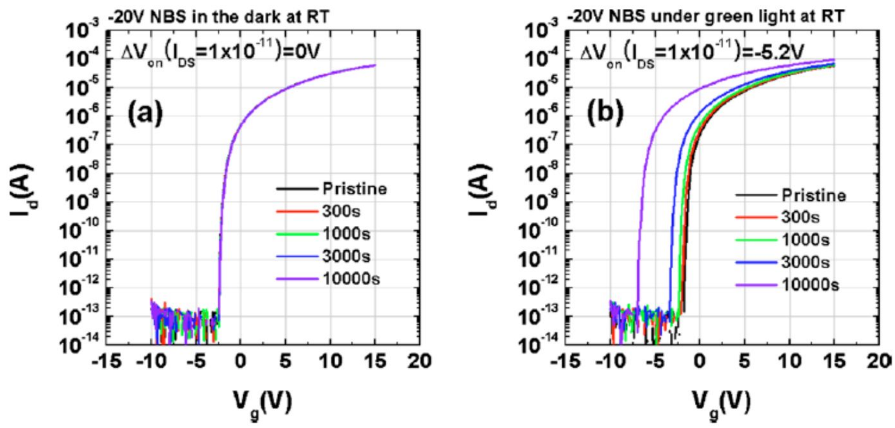


Figure 2-4 The evolution of transfer curves as a function of the applied -20 V NBS time (a) in the dark and (b) under green light exposure. [57]

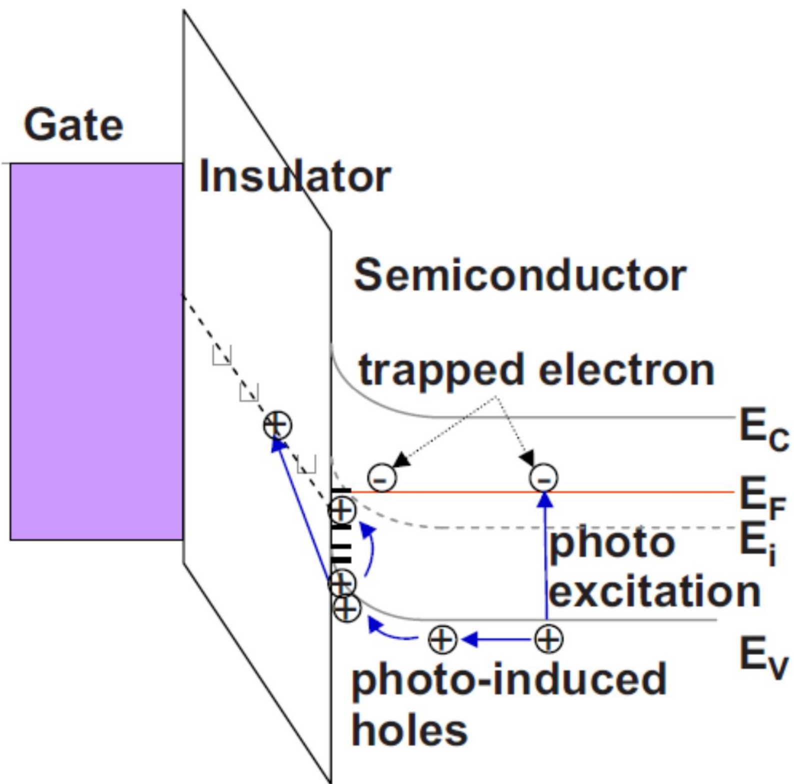


Figure 2-5 Schematic energy band diagram to explain photo-induced hole trapping. [51]

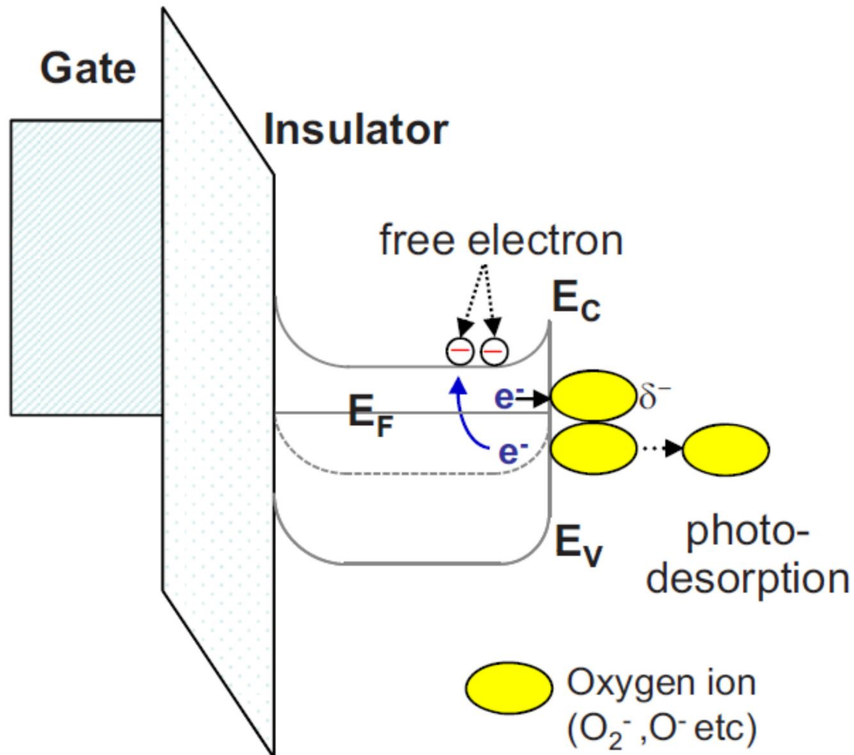


Figure 2-6 Schematic energy band diagram showing the photo-desorption of oxygen molecules into the ambient atmosphere for the un-passivated device under the application of NBS. [60]

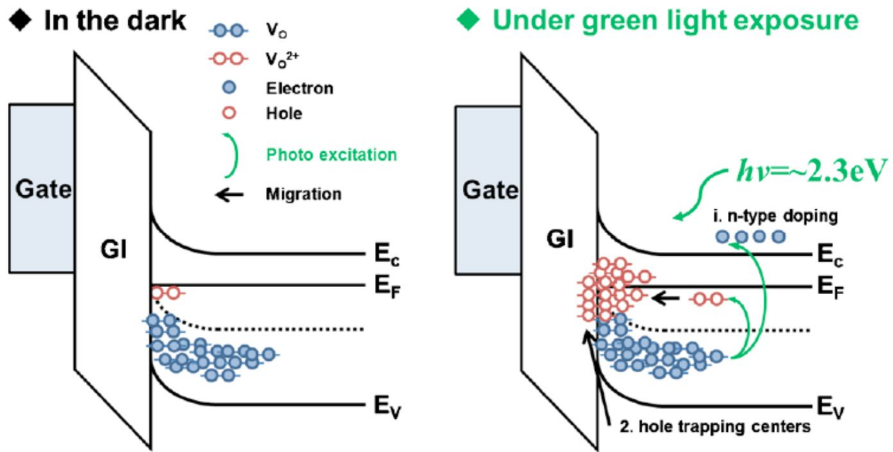


Figure 2-7 Schematic energy band diagram showing the sub-band gap states related to oxygen vacancy. [57]

2.1.3 Reliability under various environments

The oxide semiconductor TFTs are sensitive to environmental air, such as oxygen, hydrogen, or water molecules [51, 54, 70-78]. Figure 2-8 shows the shifts of transfer curves at different oxygen partial pressures. [70] As oxygen partial pressure increases, transfer curve is positively shifted. The adsorbed oxygen forms depletion layer below the surface, resulting in positive shift of threshold voltage. Figure 2-9 shows the comparison of the transfer curves before and after the water exposure [73]. Leakage current and sub-threshold slope was increased, after water exposure of the IGZO TFTs.

Left of Figure 2-10 shows the schematic showing the electric-field-induced adsorption of oxygen molecules from the ambient atmosphere under the application of positive bias stress. Right of Figure 2-10 shows schematic showing the electric-field-induced desorption of water molecules into the ambient atmosphere under positive bias stress [71].

$$O_2(gas) + e^- = 2O^-(solid) \text{ ------------------ } (1)$$

The interaction between the backchannel of active layer and ambient plays a critical role in the threshold voltage shifts. The adsorbed oxygen can capture an electron from the conduction band and that the resulting oxygen species can exist in various forms such as O^{2-}, O^-, or O_2^-, as described by the equation (1). As a result, a depletion layer is formed beneath the oxide semiconductor surface, leading to an increase in the threshold voltage.

In order to prevent the effects of the environmental air, the passivation layer is employed. The effects of passivation layer on the stability of IGZO TFTs have been intensively studied [71, 81-87]. Figure 2-11 shows the variations in the V_{TH} shift for IGZO TFTs with different passivation layer (SiN_x and SiO_x) as a function

of stress time [86]. The IGZO TFTs employing SiO_x passivation layer shows better reliability. The hydrogen incorporation during the nitride growth has generated bulk defects within the semiconductor and/or at the interface between the semiconductor and gate insulator layer. In order to reduce the damage during the deposition of the passivation layer, organic passivation layer and inorganic multi-layer passivation was reported [82, 84].

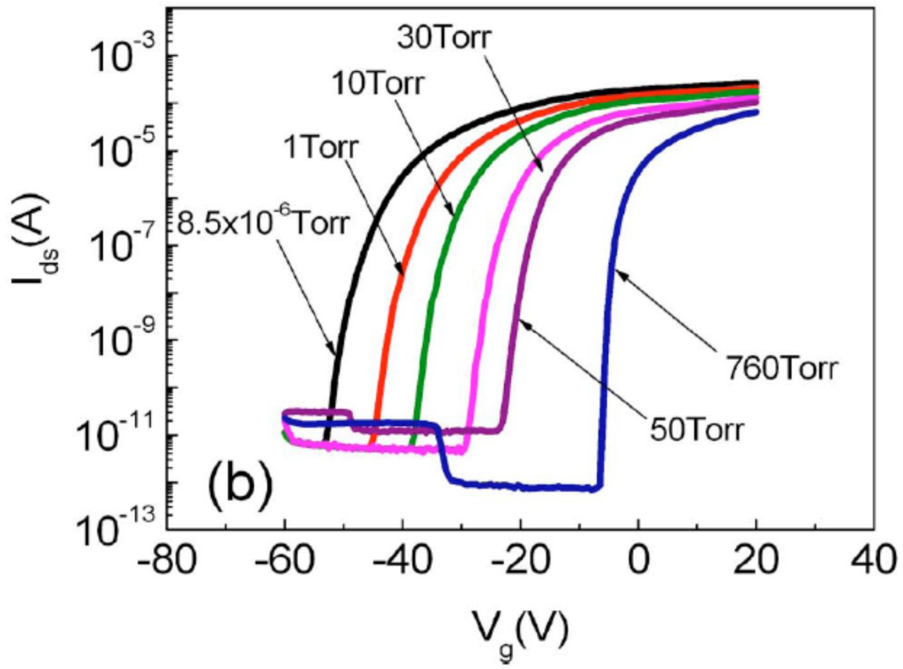


Figure 2-8 Shifts of transfer curves at different oxygen partial pressures. [70]

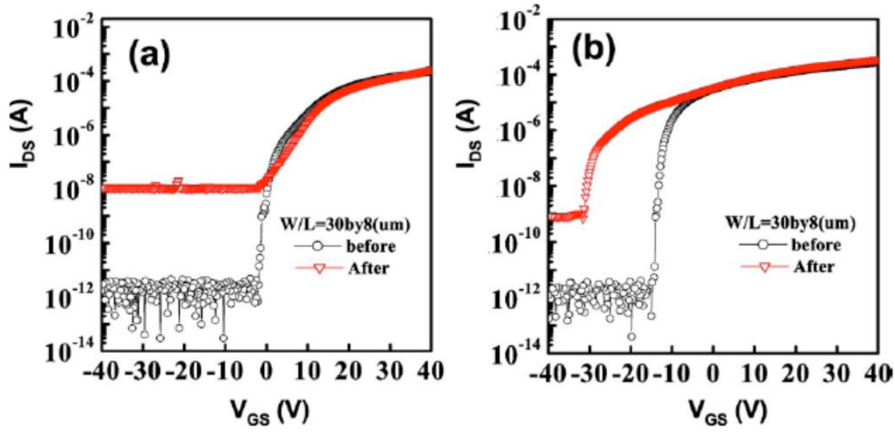


Figure 2-9 The comparison of the transfer curves before and after the water exposure for the device with (a) 35-nm-thick and (b) 150-nm-thick channels, respectively. [73]

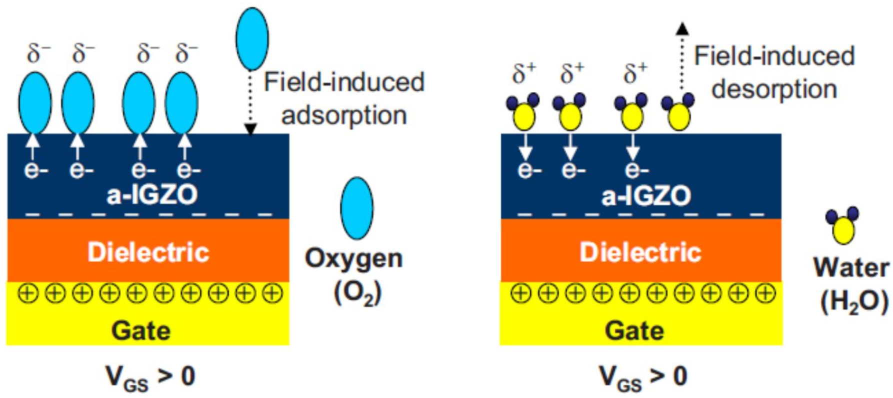


Figure 2-10 Schematic showing the electric-field-induced adsorption of oxygen molecules from the ambient atmosphere under the application of positive bias stress (left). Schematic showing the electric-field-induced desorption of water molecules into the ambient atmosphere under positive bias stress (right). [71]

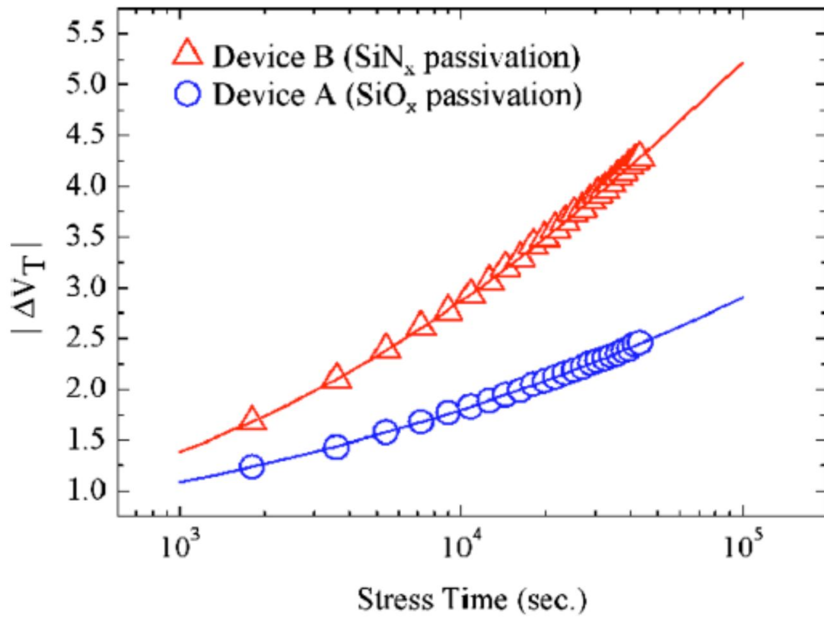


Figure 2-11 The variations in the V_{TH} shift for IGZO TFTs with different passivation layer (SiN_x and SiO_x) as a function of stress time. [86]

2.2 Various backplane materials for flexible display

Recently, flexible displays have attracted considerable attention in the emerging electronic device market. Flexible plastic substrates have the advantages such as flexibility, ruggedness and light-weight and its low cost, compared to glass substrate. These merits make plastic substrate attractive for portable systems such as a smart phone, and a tablet PC.

However, the TFT technology on plastic substrate must overcome the limitation of process temperature. Plastic substrate has a much lower thermal budget, so that the process temperature of the TFT fabrication should be sufficiently low [21]. The most of commercially developed plastic substrates can stand low temperature below 250 °C, and the critical temperature of plastic substrates is determined by the inherent characteristics of plastics [21]. Limited process temperature affects the deposition of films and the physical properties of the films tend to be deteriorated with the decrease of the process temperature. Due to the lack of thermal treatment, characteristics of the TFTs on plastic may be degraded much compared with those of the TFTs on glass.

Polyethylene naphthalate (PEN), polyethylene terephthalate (PET), polyether sulfone (PES), polycarbonate (PC), polyimide (PI), stainless steel, and thin glass were used as flexible substrate materials [20, 88-94].

PI exhibits 275 °C of the continuous use temperature, orange color, high CTE, good chemical resistance, expensive cost, and high moisture absorption. PES exhibits 230 °C of the continuous use temperature, clear, good dimensional stability, poor solvent resistance, expensive cost, and moderate moisture absorption. PC exhibits 155 °C of the continuous use temperature, clear, poor CTE, inexpensive cost, moderate moisture absorption. PEN exhibits 150 °C of the

continuous use temperature, clear, moderate CTE, good chemical resistance, inexpensive cost, moderate moisture absorption. PET exhibits 120 °C of the continuous use temperature, clear, moderate CTE, good chemical resistance, inexpensive cost, moderate moisture absorption. Table 2-1 summarizes the continuous use temperature and characteristics of the plastic substrates [93, 94].

Various active materials, such as amorphous silicon, low temperature poly silicon, single crystalline silicon, and oxide semiconductor, were considered as flexible display backplane [90, 95-97]. Flexible displays are demonstrated with the combination of various active materials and substrate materials [19, 20, 22, 88-92, 95-106]. Among the various active materials, oxide semiconductor has an advantage of low process temperature. Most of plastic substrates can stand low temperature below 250 °C. Therefore, oxide semiconductor could be fabricated on various plastic substrates.

In this thesis, the PI, coated on glass as rigid carrier, was used, overcoming difficulties in handling flexible freestanding plastic substrates, eliminating the problem of plastic shrinkage with high temperature processing and allowing the use of standard semiconductor fabrication equipment. Until now, deposition of gate insulator and post thermal annealing process are high temperature process (> 300 °C). Therefore, the PI is the most suitable for flexible substrate of oxide TFTs.

Table 2-1 The continuous use temperature and characteristics of the plastic substrates. [93, 94]

Continuous use temperature	Material	Characteristics
275 °C	Polyimide (PI)	Orange color, high CTE, good chemical resistance, expensive, high moisture absorption
230 °C	Polyether Sulfone (PES)	Clear, good dimensional stability, poor solvent resistance, expensive, moderate moisture absorption
155 °C	Polycarbonate (PC)	Clear, poor CTE, inexpensive, moderate moisture absorption
150 °C	Polyethylene naphthalate (PEN)	Clear, moderate CTE, good chemical resistance, inexpensive, moderate moisture absorption
120 °C	Polyethylene terephthalate (PET)	Clear, moderate CTE, good chemical resistance, inexpensive, moderate moisture absorption

Chapter 3 The electrical characteristics and reliability of IGZO TFTs on glass substrate

3.1 Overview

Indium-Gallium-Zinc-Oxide thin-film transistors (IGZO TFTs) have gained considerable attention for active matrix displays due to the high field effect mobility and good uniformity [26, 107]. In order to adopt the IGZO TFTs for actual display backplane, the stable characteristics under various stress conditions, such as bias, temperature, and illumination, are required.

In this chapter, the electrical characteristics and reliability of IGZO TFTs on glass substrate are discussed. Firstly, the fabrication process is introduced. The IGZO TFTs were fabricated on a glass substrate with an inverted staggered structure. The etch stopper layer were employed, in order to improve the reliability of IGZO TFTs. After the introduction of device fabrication, the initial electrical characteristics, such as threshold voltage, mobility, sub-threshold slope, on-off ratio, and leakage current level, are introduced. Following the introduction of the initial characteristics, gate bias induced instability without illumination is investigated.

And, drain bias induced instability without illumination is investigated. Unique degradation phenomenon was observed under the high drain bias stress. After the high drain bias stress, the drain current, measured at the low drain bias, was significantly decreased. Based on the experimental results, I proposed a degradation model for the high drain bias induced degradation.

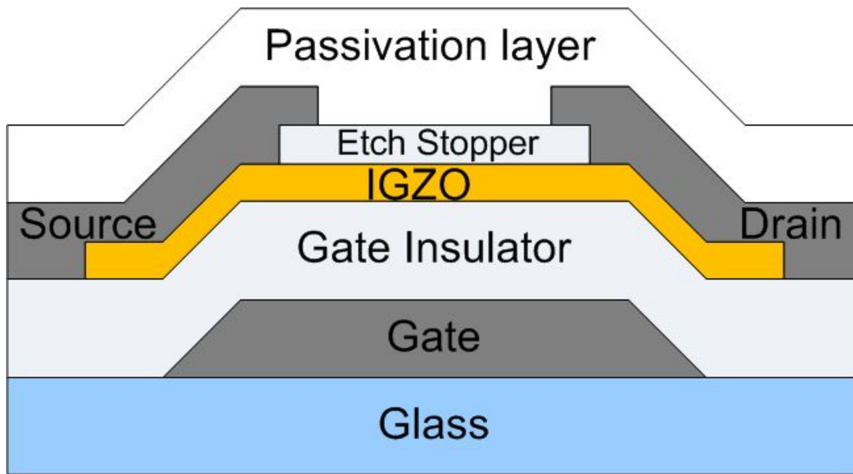
Following the drain bias induced instability, light-induced hysteresis of IGZO TFTs is investigated. Hysteresis was observed under the 450-nm illumination, and was increased with temperature. And hysteresis was increased with wavelength decrease. Light-induced hysteresis occurs due to increased sub-band gap states at the interface between the gate insulator layer and the active layer.

Lastly, bias illumination stress induced instability is investigated. The transfer curve did not change after positive bias illumination stress. However, the transfer curve shifted to a negative direction after negative bias illumination stress. The transfer curve could be shifted to the negative direction after negative bias illumination stress due to the increase of V_O^{2+} states.

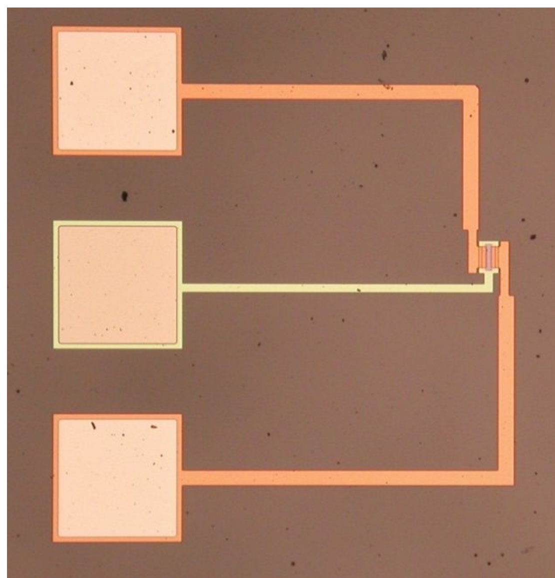
3.2 Fabrication process of IGZO TFTs on glass substrate

The a-IGZO TFTs were fabricated on a glass substrate with an inverted staggered structure. Figure 3-1 (a) shows the cross sectional view of the fabricated IGZO TFTs. First, Mo/AlNd were deposited and patterned as the gate electrode. SiO_2 of 2,000 Å thickness was then deposited by plasma-enhanced chemical vapor deposition (PECVD) and served as the gate dielectric layer. The IGZO (In:Ga:Zn = 1:1:1) layer with a thickness of 500 Å was deposited by sputtering. The SiO_2 etch stop layer was deposited by PECVD. The source and drain were formed by depositing a layer of Mo and were patterned by dry etching. The SiO_2 layer was used as a passivation layer. Annealing of the device was performed as the final process at 300 °C in ambient air. Table 3-1 summaries the layers information of the fabricated oxide TFTs. Figure 3-1 (b) shows the microscope image of the fabricated oxide TFTs.

The channel width was 24 μm and the length was 12 μm. The transfer characteristics of the TFTs were evaluated using an Agilent B1500A semiconductor parameter analyzer. For the light illumination test, the device was irradiated by a xenon lamp using narrow band pass filters.



(a)



(b)

Figure 3-1 (a) The cross-sectional view and (b) the microscope image of the fabricated oxide TFTs

Table 3-1 The layers information of the fabricated oxide TFTs.

Layer	Material	Equipment
Gate	Mo/AlNd	DC sputter
Gate Insulator	SiO_2 200 nm	PECVD
Active	IGZO 50nm	DC sputter
Etch stopper	SiO_2 50 nm	PECVD
Source/Drain	Mo	DC sputter
Passivation	SiO_2 200 nm	PECVD

3.3 Electrical characteristics of IGZO TFTs

Figure 3-2 shows the transfer curves of fabricated IGZO TFTs by repeated measurement. The transfer curve maintains its origin state under repeated measurement. The threshold voltage (V_{TH}) is -0.2 V, and the field effect mobility is 12 $cm^2/V \cdot s$. The sub-threshold slope is 200 mV/dec, and the on-off ratio is greater than 10^8. The leakage current level is less than 10^{-12} A. Table 3-2 summaries the extracted parameter of the fabricated IGZO TFTs.

Despite the amorphous state, the origin of the high mobility was attributed to the electronic orbital structure of the material [22]. Zinc oxide based semiconductor, such as IGZO, exhibits large optical band gap (>2.8 eV) compared to silicon-based semiconductor [29, 30]. Due to large band gap characteristics, the oxide semiconductor exhibits low leakage current. Large on-off ratio is attributed to the high mobility and low leakage current. Zinc oxide based semiconductor, such as IGZO, exhibits low sub-band gap states compared to amorphous silicon [108-110]. Small sub-threshold slope of IGZO TFTs is originated from low sub-band gap states characteristics.

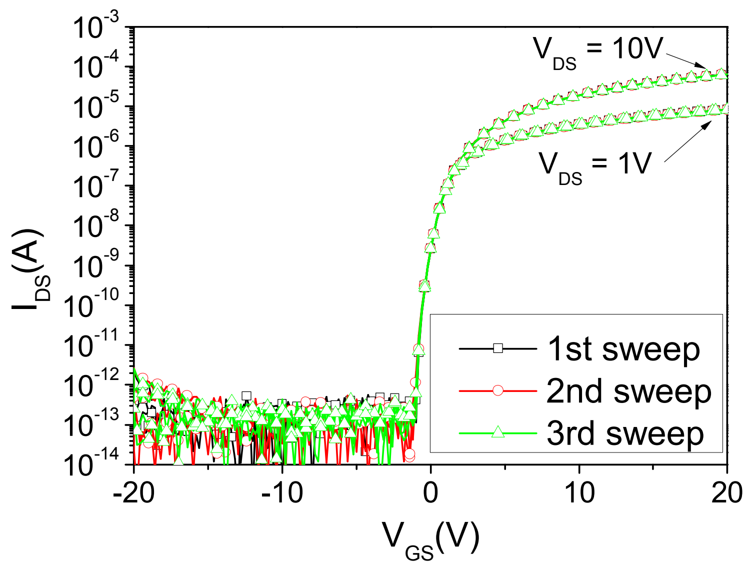


Figure 3-2 Transfer curves of fabricated IGZO TFTs by repeated measurement.

Table 3-2 The extracted parameter of the fabricated IGZO TFTs.

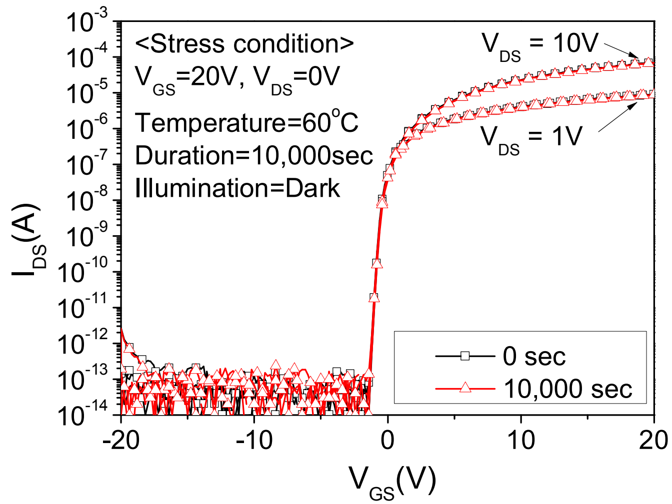
Parameter	Value	Unit
V_{TH}	-0.2	V
Mobility	12	$cm^2/V{\cdot}s$
Sub-threshold slope	200	mV/dec
On-off ratio	$> 10^8$	-
Leakage current	$< 10^{-12}$	A

3.4 Gate bias induced instability without illumination

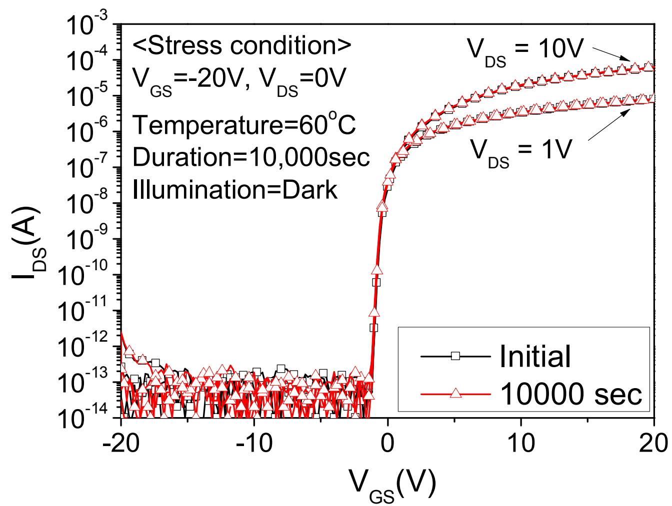
Figure 3-3 shows the transfer curves before and after (a) positive bias temperature stress and (b) negative bias stress conditions. For positive bias stress, gate-source voltage (V_{GS}) was applied to 20 V, and drain-source voltage (V_{DS}) was applied to 0 V under no illumination for 10,000 seconds. The temperature was set to 60 °C, in order to accelerate degradation. For negative bias stress, V_{GS} was applied to -20 V, and the other stress condition was same to positive bias stress. Transfer curve was scarcely changed after positive bias tress (20 V) and negative bias stress (-20 V).

In order to investigate gate bias induced degradation, we applied 30 V and 50 V to the gate bias stress. The other stress condition was same to the above condition. Figure 3-4 shows the transfer curves before and after 30 V and 50 V gate bias stress. In case of 30 V gate bias stress, transfer curve was scarcely changed. The fabricated devices show superior reliability compared to the literatures [31, 41, 46]. In case of 50 V gate bias stress, threshold voltage was positively shifted by the amount of 1.5 V. The other parameters, such as mobility or sub-threshold slope, were scarcely changed.

The dominant degradation mechanism is electron trapping at the interface between gate insulator and IGZO. Figure 3-5 shows the schematic drawing of trapped electrons at the interface between the gate insulator layer and IGZO layer due to high gate bias induced degradation.

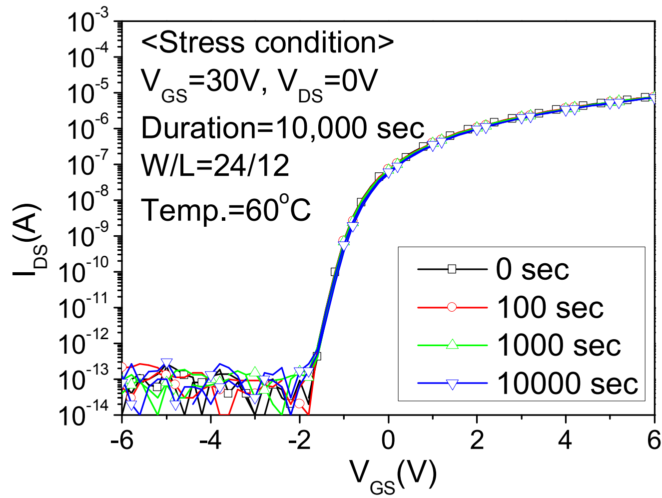


(a)

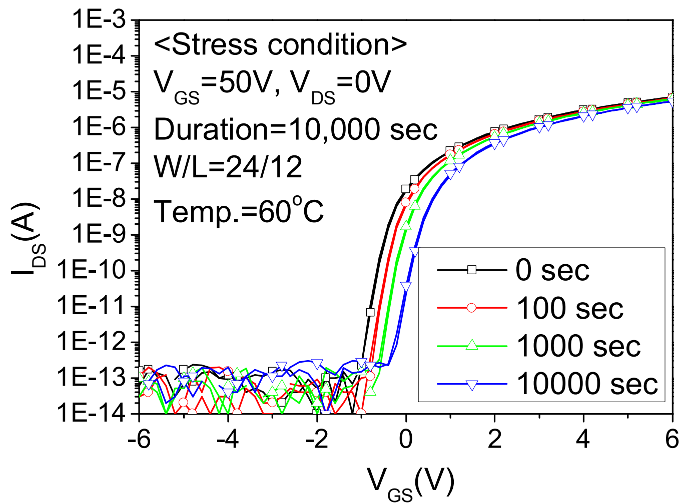


(b)

Figure 3-3 Transfer curves before and after (a) positive bias temperature stress and (b) negative bias stress conditions. A detailed stress condition is shown in the figures.



(a)



(b)

Figure 3-4 Transfer curves before and after (a) 30 V and (b) 50 V gate bias stress. A detailed stress condition is shown in the figures.

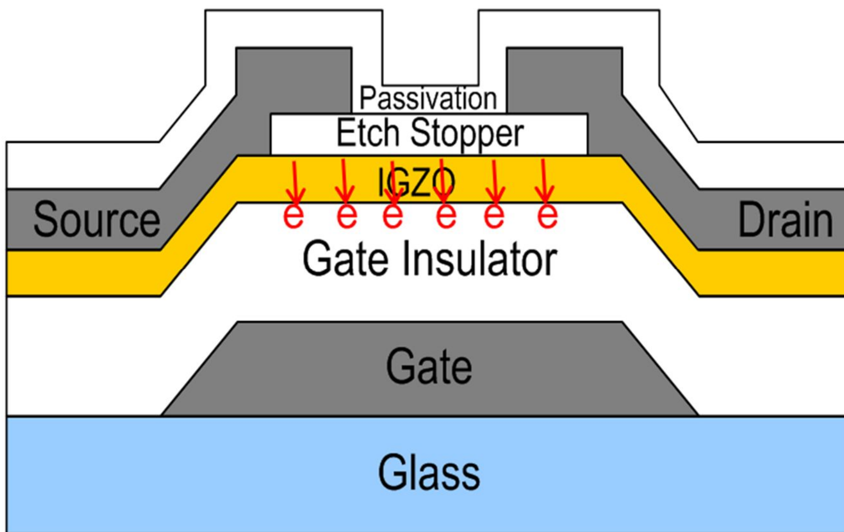


Figure 3-5 Schematic drawing of trapped electrons at the interface between the gate insulator layer and IGZO layer due to high gate bias induced degradation.

3.5 Drain bias induced instability without illumination

3.5.1 Introduction

Amorphous Indium-Gallium-Zinc-Oxide (IGZO) thin-film transistors (TFTs) have gained considerable attention for active matrix displays due to the high field effect mobility and good uniformity [26, 107]. The electrical stability of IGZO TFTs under the bias, temperature, and illumination has been intensively studied [45, 46, 62].

The effects of gate bias stress on IGZO TFTs have been widely researched [31, 41, 43]. However, there are a few reports on the drain bias induced degradation in IGZO TFTs [41, 111]. It is reported that the effect of the drain bias on the stability of IGZO TFTs is not significant compared to the gate bias induced stress [41]. In the previous works, the high gate bias was applied simultaneously with the drain bias stress, which is different from our experimental condition [41, 111]. In our experimental results, however, a-IGZO TFTs with the etch stopper structure was degraded under the high drain bias stress. Our experimental results show that a linear region of an output curve was severely decreased after the high drain bias stress. Furthermore, in the transfer curve, the drain current measured at the low drain bias (V_{DS} = 1 V) was significantly decreased after the high drain bias stress. High drain bias could be applied to the transistor of the shift register [112]. And the applied drain bias to the driving transistor of the OLED TV is enhanced as the size of the panel increases.

The purpose of our work is to investigate the high drain induced degradation in IGZO TFTs with the etch stopper structure. I propose a degradation model for the

high drain bias induced degradation. Computer aided device simulations and capacitance-voltage (C-V) measurements were employed to support my degradation model.

3.5.2 Experimental methods

The IGZO TFTs were fabricated on a glass substrate with the bottom gate structure. The bottom gate structure is widely used for a-IGZO TFTs, to adapt a conventional mass production process and design [23, 61, 113]. Most of the bottom gate structures have employed the etch stopper layer, to improve the reliability of a-IGZO TFTs [23, 61, 113]. The detailed fabrication process is reported elsewhere [114]. The SiO_2 etch stopper layer was employed to reduce the damage of the IGZO layer during the source-drain dry etching process.

3.5.3 Experimental results and discussions

In order to investigate the drain bias induced degradation, we applied the various drain bias (10 V ~ 50 V) to the IGZO TFTs under 30 and 60 °C for 100 seconds. For the purpose of minimizing the effect of gate bias, we fixed the gate bias to 1 V. The degradation was not observed under 30 V drain bias stress as shown in Figure 3-6 (a). Over 40 V drain bias stress, however, the drain current at low drain bias regime was decreased. Figure 3-6 (b) shows the output curve before and after 40 V drain bias stress. The output curve was measured at 2 V, 6 V, and 10 V gate bias. Regardless of the measuring gate bias, the linear region of the output curve was slightly decreased after 40 V drain bias stress. Figure 3-6 (c) shows the transfer curve before and after 40 V drain bias stress. The transfer curve was measured at 1 V and 10 V drain bias. The drain current measured at 1 V drain bias was slightly decreased, while the drain current measured at 10 V drain bias was scarcely decreased. In case of 50 V drain bias stress, the drain current at low drain bias regime was decreased significantly. Figure 3-6 (d) and (e) show the output curve and transfer curve before and after 50 V drain bias stress. Linear region of output curve was severely distorted after 50 V drain bias stress. In terms of the transfer curve, the drain current measured at 1 V drain bias was significantly decreased, while the drain current measured at 10 V drain bias was slightly decreased. The degradation was occurred in a short time compared to the high gate bias induced stress. However, the degradation did not proceed additionally, as the stress time increased.

When high gate bias stress is applied, threshold voltage is shifted according to the polarity of the applied gate bias [31, 41, 43]. On-current level of the output curve could be changed according to the shift of threshold voltage, while linear region of output curve is hardly changed. The high gate bias induced degradation

mechanism is the charge trapping at the interface between the gate insulator layer and active layer. Our experimental result is a unique degradation phenomenon compared to the previous reports.

To explain the unique degradation phenomenon, we assumed that the electrons could be trapped at the etch stopper layer due to the high drain bias. In this case, the drain bias has an effect on the electrons vertically, not laterally. In the gate-drain overlapped region, the electrons could have a vertical electric field. Figure 3-7 (a) shows the schematic drawing of trapped electrons at the etch stopper layer due to high drain bias induced degradation. The electrons are trapped at the etch stopper layer near the drain electrode due to high vertical field. Figure 3-7 (b) shows the band diagram of the low drain bias measurement condition (V_{DS} = 1 V) after the high drain bias induced degradation. When the electrons are trapped at the etch stopper layer, the energy barrier is formed near the drain electrode due to the trapped electrons. In case of the low drain bias measurement condition (V_{DS} = 1 V), the energy barrier blocks the carriers and the drain current could be decreased significantly. In case of the high drain bias measurement condition (V_{DS} = 10 V), however, the energy barrier is lowered due to the applied drain bias and the drain current could be decreased slightly.

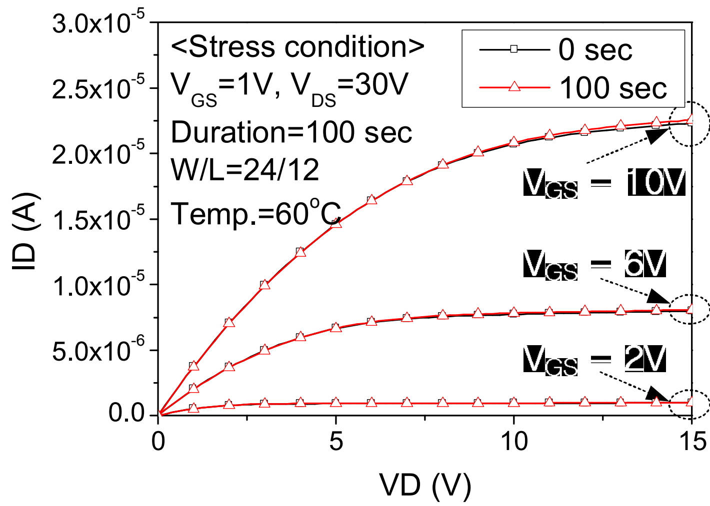
The Capacitance-Voltage (C-V) characteristics were investigated, in order to verify the degradation model. Figure 3-8 (a) and (b) show gate-source capacitance (C_{GS}) and gate-drain capacitance (C_{GD}) before and after the 40 V drain bias stress. The C_{GS} was measured with a floating drain, while the C_{GD} was measured with a floating source. The C-V curve of C_{GS} was not altered after stress, while the C-V curve C_{GD} was positively shifted by amount of 1.23 V after 40 V drain bias stress. Figure 3-8 (c) and (d) show the C-V curve of C_{GD} before and after the 30 V and 50 V drain bias stress. The C-V curve of C_{GD} was positively shifted by amount of 0.28 V (4.96 V) after 30 V (50 V) drain bias stress. As the

applied drain bias increased, the amount of shift of C-V curve was increased.

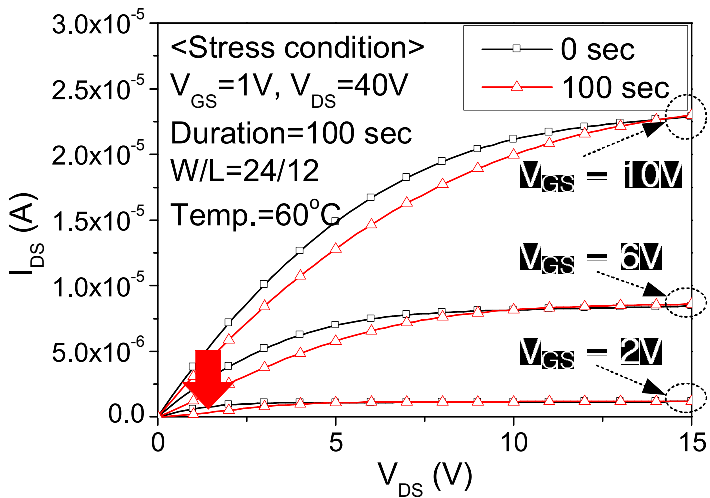
When the electrons are trapped at the insulator in MIS structure, C-V curve could be positively shifted. Density of interface trapped electrons (ΔQ_n) could be calculated using the following equation ($\Delta Q_n = C \cdot \Delta V_{shift}$). The calculated Q_n is about to 2E11 cm^{-2} (30 V drain bias stress), 8E11 cm^{-2} (40 V drain bias stress), and 3E12 cm^{-2} (50 V drain bias stress). The C-V characteristics suggest that the electron is trapped at the etch stopper layer near the drain region and support my degradation model.

In order to support our degradation model, we employed the computer aided device simulation. We used ATLAS device simulator made by Silvaco. The interface trapped electrons were introduced at the etch stopper layer near the drain electrode in consideration of high drain bias induced degradation. Density of interface trapped electron is applied to the extracted data from our experimental results. Figure 3-9 (a) and (b) show the simulated output curves and transfer curves, and they are well matched to our experimental results. Figure 3-9 (c) and (d) show the free electron concentration in IGZO layer calculated by the computer aided device simulation (assuming Q_n = 3E12 cm^{-2}). Blue-dashed-squared region in Figure 3-7 (a) represents the simulation region. Figure 3-9 (c) shows the electron concentration in the IGZO layer under 1 V drain bias measurement condition. The free electrons in IGZO layer are depleted under the etch stopper layer due to the electric field induced by the interface trapped electrons at the etch stopper layer. Figure 3-9 (d) shows the electron concentration in IGZO layer under the 10 V drain bias measurement condition. The electrons are not depleted anymore at 10 V drain bias measurement condition because 10 V drain bias lowers the energy barrier made by the interface trapped electrons. The simulation results support my degradation model.

Figure 3-10 shows the comparison of output curves and transfer curves before and after high drain bias stress between (a, c) simulation and (b, d) experimental data. The simulated output curve and transfer curve are well matched that of the experimental results. These curves are support my degradation model.



(a)



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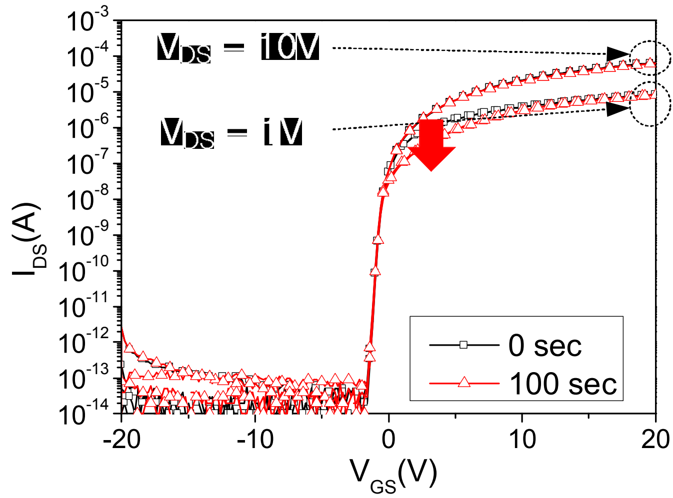

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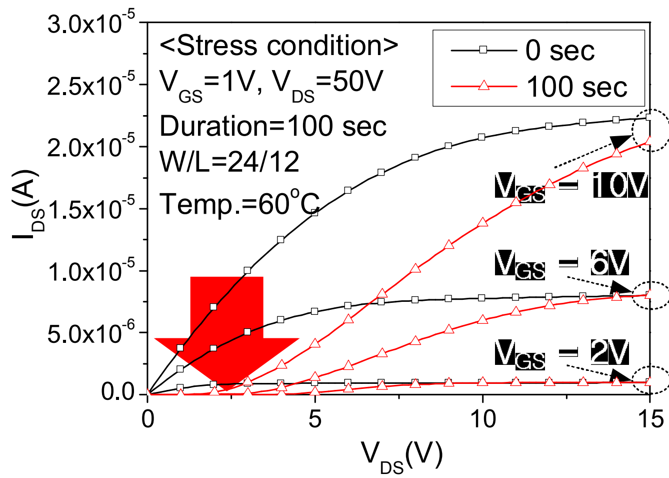
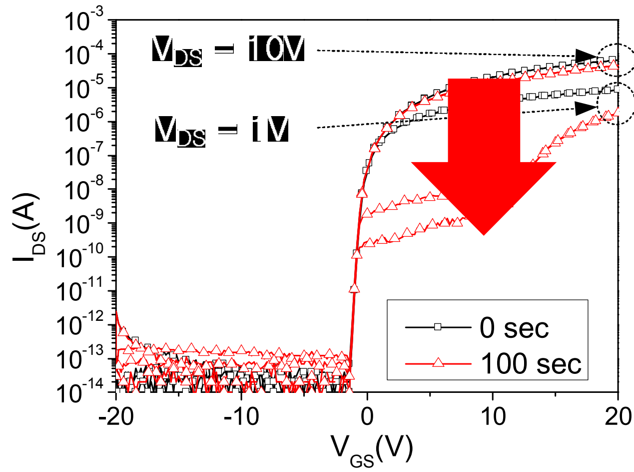
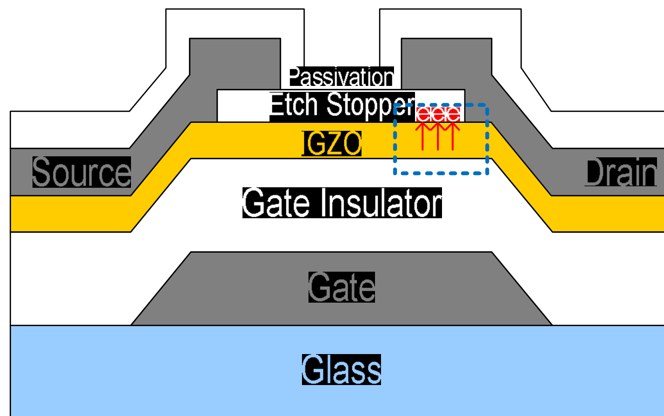


(d)



(e)

Figure 3-6 (a) Output curve before and after 30 V drain bias stress. (b) Output curve and (c) transfer curve before and after 40 V drain bias stress. (d) Output curve and (e) transfer curve before and after 50 V drain bias stress. Detailed stress condition is shown in figures.



(a)

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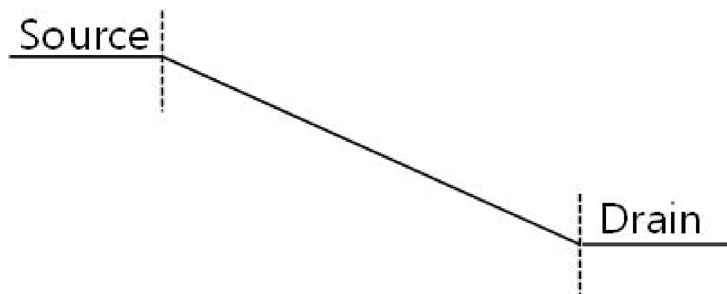
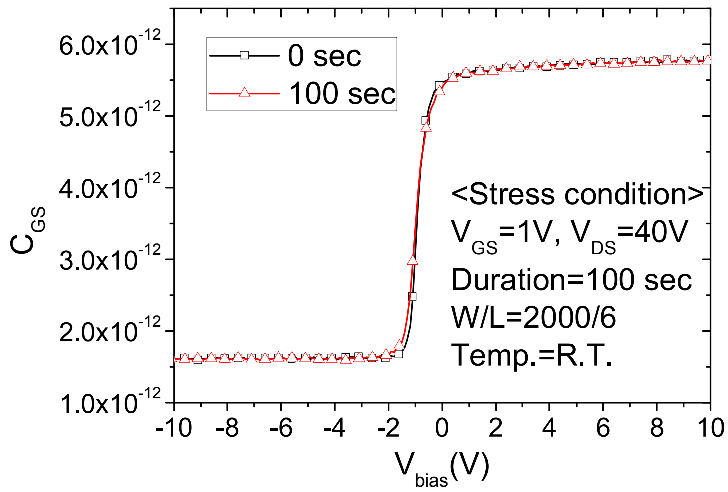
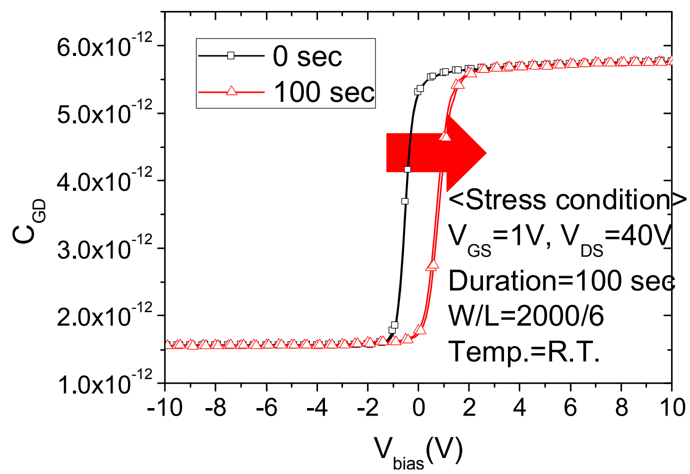


(c)

Figure 3-7 (a) Schematic drawing of trapped electrons at the etch stopper layer due to high drain bias induced degradation. (b) Band diagram of low drain bias measurement condition (V_{DS} = 1V) and (c) high drain bias measurement condition (V_{DS} = 10V) after degradation.



(a)



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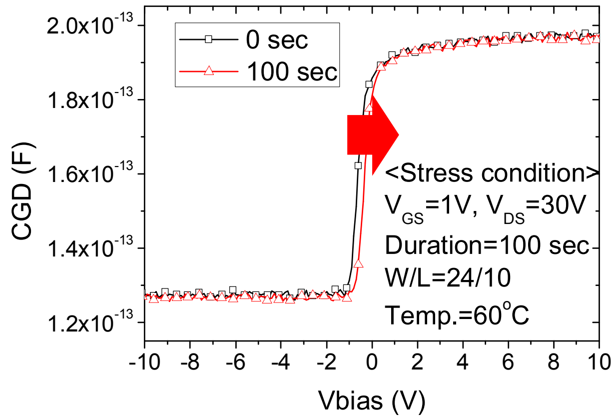

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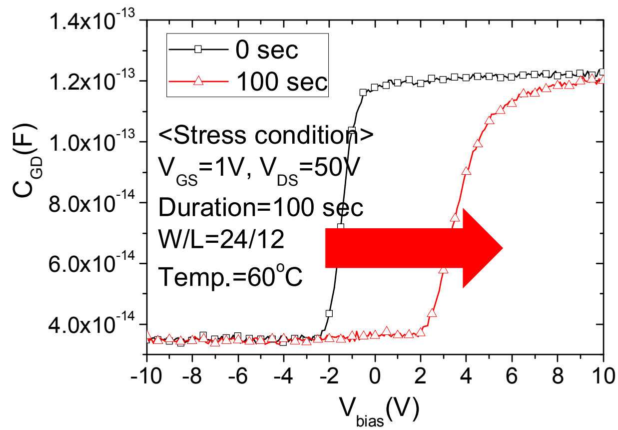
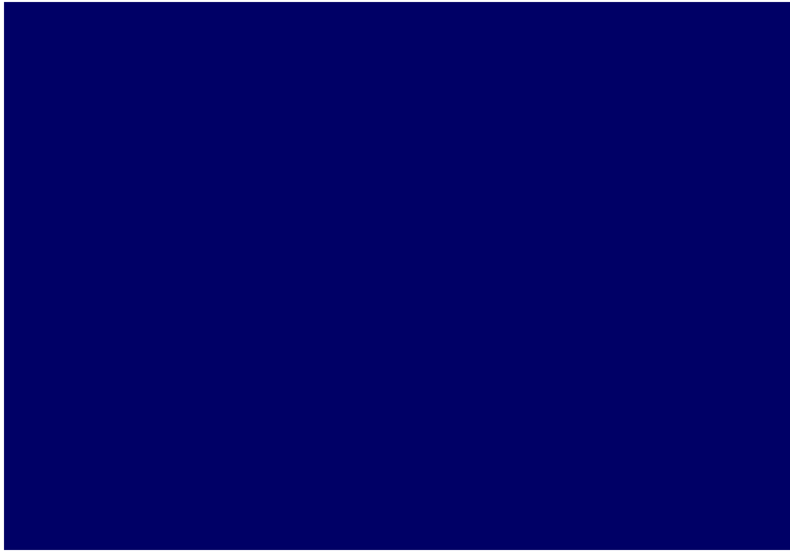


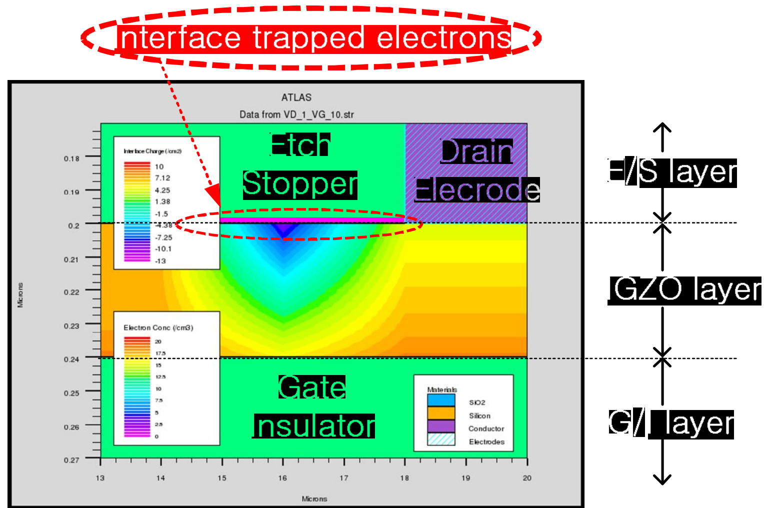
(d)

Figure 3-8 (a) Gate-source capacitance (C_{GS}) and (b) gate-drain capacitance (C_{GD}) versus gate bias curves (C-V curves) before and after 40 V drain bias stress. C_{GD} versus gate bias curves before and after (c) 30 V drain bias stress and (d) 50 V drain bias stress.



(a)

(b)



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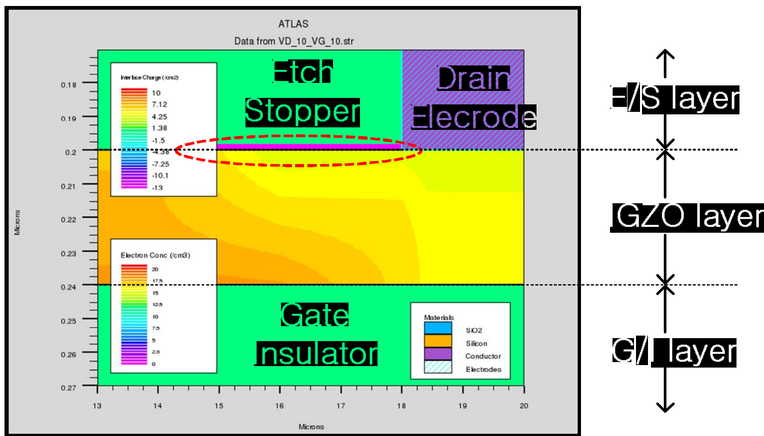


(d)

Figure 3-9 Simulated (a) output curves and (b) transfer curves by assuming the interface trapped electrons (Q_n = 0, 2E11, 8E11, 3E12 cm^{-2}). And electron concentration in IGZO layer calculated by computer aided device simulation (SILVACO) under (c) 1 V drain bias measurement condition and (d) 10 V drain bias measurement condition.

(a)

(b)

(c)

(d)

Figure 3-10 Comparison of output curves before and after high drain bias stress between (a) simulation and (b) experimental data. Comparison of transfer curves before and after high drain bias stress between (a) simulation and (b) experimental data.

3.5.4 Conclusion

I have investigated the high drain bias induced degradation in IGZO TFTs with the etch stopper structure. The drain current, measured at the low drain bias, was significantly decreased after the high drain bias stress. The electrons were trapped at the etch stopper layer due to the high drain bias. The drain bias has an effect on the electrons vertically, not laterally. The computer aided simulation and C-V measurements support our degradation mechanism. Highly reliable etch-stopper-free-structure should be developed, to solve the high drain bias induced degradation and establish simple fabrication process.

3.6 Light-Induced Hysteresis of IGZO TFTs with Various Wavelengths

3.6.1 Introduction

Indium-Gallium-Zinc Oxide thin-film transistors (IGZO TFTs) are promising candidate for next generation display backplane, due to its large mobility and good uniformity. Threshold voltage (V_{TH}) of IGZO TFTs was not shifted under positive gate bias stress (PBS) or negative gate bias stress (NBS) without illumination. However, V_{TH} of IGZO TFT was negatively shifted significantly under NBS with light illumination. In order to investigate this unique degradation phenomenon, stability of IGZO TFT under negative bias illumination stress (NBIS) has been intensively studied [57, 59, 68].

However, light-induced changes in device characteristics, such as hysteresis, are scarcely reported. Recently, I reported light-induced hysteresis and its mechanism of IGZO TFTs under various temperatures [114]. My experimental results showed that sub-threshold slope (S.S.) under 450-nm illumination increased compared to dark state during the forward sweep. However, S.S. under 450-nm illumination did not change compared to dark state during the reverse sweep. This phenomenon could be called light-induced hysteresis.

In this paper, I report the effects of wavelength and negative bias on light-induced hysteresis of IGZO TFTs. Hysteresis was increased, as wavelength decreased. And hysteresis was increased, as applied negative bias increased.

3.6.2 Experimental methods

The IGZO TFTs were fabricated on a glass substrate with an inverted staggered structure. First, Mo/AlNd were deposited and patterned as the gate electrode. SiO_2 of 2000 Å thickness was then deposited by plasma enhanced chemical vapor deposition (PECVD) and served as the gate dielectric layer. The IGZO (In:Ga:Zn = 1:1:1) layer with a thickness of 500 Å was deposited by sputtering. The SiO_2 etch stop layer was deposited by PECVD. The source and drain were formed by depositing a layer of Mo and patterned by dry etching. The SiO_2 layer was used as a passivation layer. Annealing of the device was performed as the final process at 300°C in an ambient air. For the light illumination test, the device was irradiated by a Xenon lamp with narrow band pass filters.

3.6.3 Experimental results and discussions

Figure 3-11 (a) shows the transfer curves under dark and illumination conditions at 60°C. The center wavelengths of band pass filters were 550nm, 500nm, 450nm, and 400nm and light intensity was adjusted to 1 mW/cm^2. The transfer curves were measured by the double sweep method from −20V to 20V and the drain bias was fixed to 10 V. The transfer curves measured under dark condition and illumination conditions of 550 nm and 500 nm did not show any hysteresis. On the other hand, the transfer curves measured under 450 nm and 400 nm illumination conditions showed hysteresis. The magnitude of hysteresis increased as the wavelength decreased. Figure 3-11 (b) shows the magnitude of hysteresis (ΔV) and mobility extracted from Figure 3-11 (a). Mobility was not altered regardless of wavelength. Moreover, mobility was not changed under dark condition.

The mobility of the IGZO TFT strongly depends on carrier concentration [22]. Electron concentration could be increased by light and thermal energy. To increase the mobility of IGZO TFTs under the illumination conditions, the light-induced free carrier concentration (Δn_L) should be increased as much as the intrinsic carrier concentration. The intrinsic carrier concentration of IGZO is known to be 10^{16-20} cm^{-3} [22, 115]. According to Lambert-Beer's law, the approximated quantum efficiency (η) could be estimated using the following equation ($\eta = 1-\exp[-\alpha_{sub}\cdot d]$, where α_{sub} is the sub-band gap absorption coefficient and d is the thickness of the IGZO film) [116]. When α_{sub} is assumed to be 10^4 cm^{-1} [110], η is calculated to be 4.9%. If light of a 400-nm wavelength and 1 mW/cm^2 intensity is illuminated to IGZO TFTs, Δn_L could be estimated using following equation ($\Delta n_L = \tau\cdot\eta\cdot I\cdot \lambda/[h\cdot c\cdot d]$). τ is the electron life-time (assumed to 10^{-6} sec), I and λ are the intensity and wavelength of the illuminated light, h is

Planck's constant, and c is the speed of light. Δn_L is calculated to be approximately 10^{13} cm^{-3}, which is far less than the intrinsic carrier concentration. Under the illumination condition of wavelength longer than 400nm, Δn_L should be decreased, due to the decrease of α_{sub}. It is suggested that light induced channel defect concentration is not large enough to change the mobility of IGZO TFTs.

Figure 3-12 (a) shows the transfer characteristics of IGZO TFTs under various sweep ranges (V_{GS} = -10 ~ 10V, -20 ~ 20V, -30 ~ 30V) with 450 nm illumination at 60 ^oC. The magnitude of hysteresis increased as sweep range increased. In order to investigate hysteresis mechanism in detail, we measured IGZO TFTs asymmetrically. Figure 3-12 (b) shows the transfer characteristics of IGZO TFTs under various sweep ranges (V_{GS} = -30 ~ 30V, -30 ~ 10V, -10 ~ 30V) with 450 nm illumination at 60 ^oC. The magnitude of hysteresis was similar between (V_{GS} = -30 ~ 30V) and (V_{GS} = -30 ~ 10V). The magnitude of hysteresis was decreased when sweep range is (V_{GS} = -10 ~ 30V). We have found that the magnitude of hysteresis was strongly dependent on the magnitude of applied negative gate bias. And we have found that the magnitude of hysteresis was independent on the magnitude of applied positive gate bias.

When a ZnO based semiconductor is deposited, the deposited film has the native point defect, such as the oxygen vacancy. The oxygen vacancy has 3 possible charge states (V_O, V_O^+, and V_O^{2+}). Neutral oxygen vacancy (V_O) is located near valence band maximum (VBM), and doubly ionized oxygen vacancy (V_O^{2+}) is located near conduction band minimum (CBM). Figure 3-13 (a) shows the energy level of sub-band states of neutral oxygen vacancy (V_O), singly ionized oxygen vacancy (V_O^+) and doubly ionized oxygen vacancy (V_O^{2+}). The energy level of sub-band states could be calculated using the first-principle calculations. Figure 3-13 (b) shows the formation energies vs Fermi level for oxygen vacancies in ZnO in

the 0, 1+, and 2+charge states, under Zn-rich conditions. [117]

Figure 3-14 shows the schematic configuration coordinate diagrams for (a) negative gate bias and (b) positive gate bias. When the negative V_{GS} is applied, the Fermi level moves toward the valence band. The formation energy of V_O^{2+} states could be smaller than that of V_O states. It is suggested that V_O^{2+} states are more stable than V_O states under negative gate bias. The formation energy of V_O^{2+} states is reduced further, as the Fermi level decreases. When the energy over the energy barrier is applied, V_O states could be turned to V_O^{2+} states. The energy barrier from V_O states to V_O^{2+} states is considered to about 2.75 eV, because light-induced hysteresis could not be observed under the illumination of longer than 450 nm. Therefore, V_O^{2+} states could be observed during the forward sweep.

When the positive V_{GS} is applied, the Fermi level moves toward the conduction band. The formation energy of V_O^{2+} states is increased, and the formation energy of V_O states could be smaller than that of V_O^{2+} states. It is suggested that V_O states are more stable than V_O^{2+} states under positive gate bias. The energy barrier from V_O^{2+} states to V_O states could be smaller than 2.75 eV. Therefore, V_O^{2+} states could not be observed during the reverse sweep.

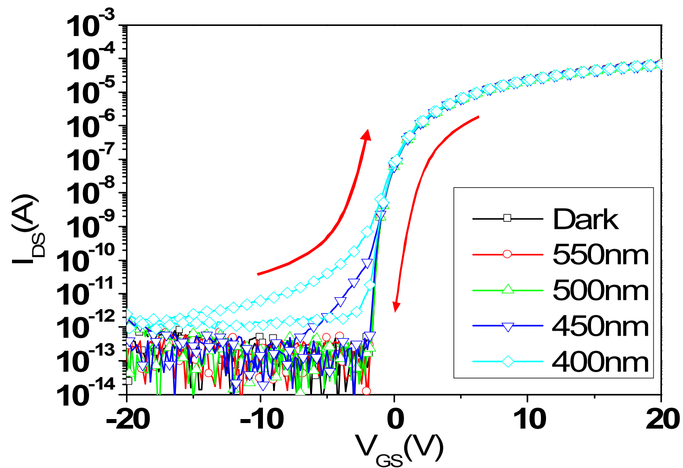
Figure 3-15 shows band diagram of IGZO TFTs with light illumination under negative gate bias (a) and positive gate bias (b). Photon irradiation and negative gate bias causes the transition of neutral oxygen vacancy (V_O) to the doubly ionized oxygen vacancy (V_O^{2+}) and the donation of two electrons to the conduction band. The V_O^{2+} states are created at the interface, and the generated V_O^{2+} states from the bulk could be migrated to the interface due to the applied negative gate bias. Interface states could be increased during this time, resulting in increase of sub-threshold slope. When the gate bias is changed from negative bias to positive bias, V_O^{2+} states at the interface are neutralized to V_O states by

capturing two electrons. Therefore, transfer curves under dark and illumination are almost identical at the positive gate bias regime.

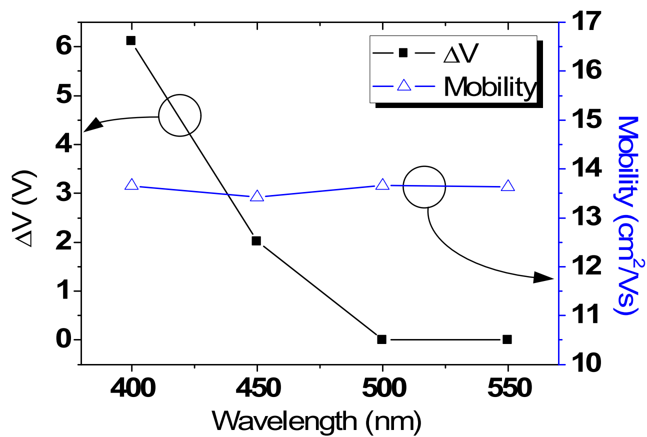
In contrast to forward sweep, transfer curves under dark and illumination are almost identical during a whole reverse sweep. At the beginning of the reverse sweep, positive gate bias is applied so that V_O^{2+} states could not be generated at the interface. When the gate bias is changed from positive bias to negative bias during reverse sweep, transfer curves turn to off state. Therefore, transfer curves under dark and illumination could be identical during the whole reverse sweep.

As wavelength decreased, absorption coefficient of IGZO film increased. It is obvious that more V_O states could be excited to the V_O^{2+} states, as the wavelength decreased. Therefore, the magnitude of hysteresis is enhanced, as the wavelength is shifted to deep blue. Our experimental results suggested that V_O states ranged from 2.75 eV (wavelength ~ 450nm) below the conduction band minimum.

When sweep range is changed from (-10V ~ 10V) to (-30V ~ 30V), the magnitude of initial negative bias and time to be applied negative bias are increased, resulting in increase of interface state and sub-threshold slope. Therefore, hysteresis could be increased with the magnitude of applied initial negative gate bias.

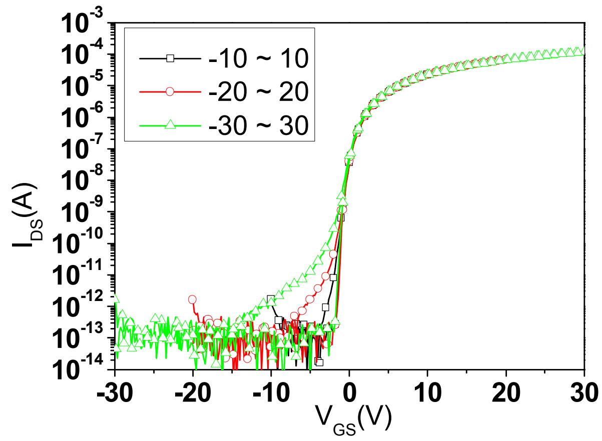


(a)

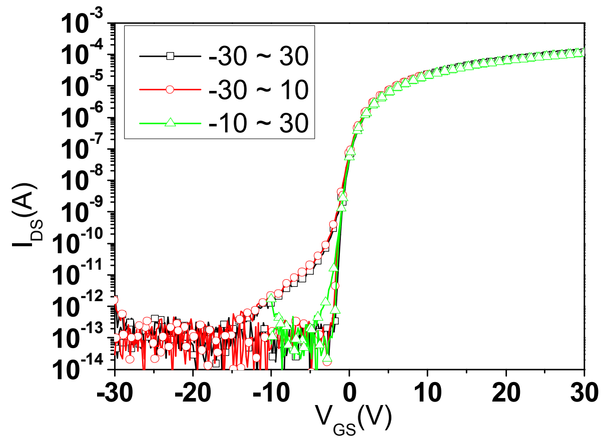


(b)

Figure 3-11 (a) Transfer characteristics of IGZO TFTs under dark and various wavelengths at 60 ^{o}C (Wavelength = 550 nm, 500 nm, 450 nm, and 400 nm, Intensity = 1 mW/cm^2) (b) Magnitude of hysteresis and mobility as a function of wavelength.

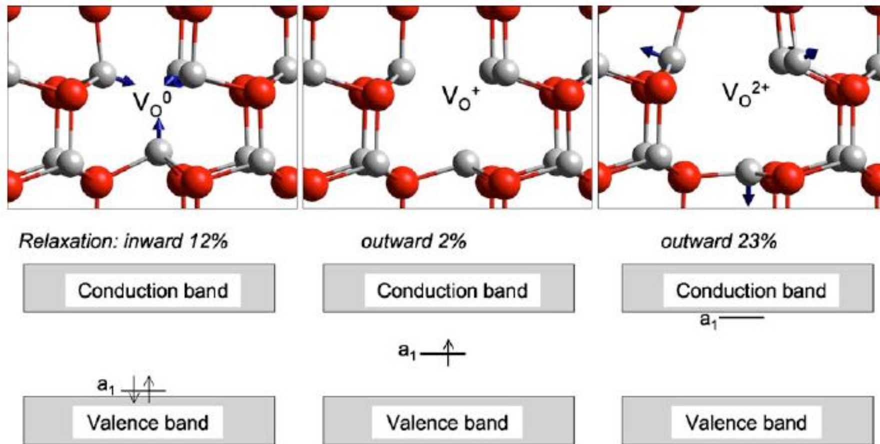


(a)

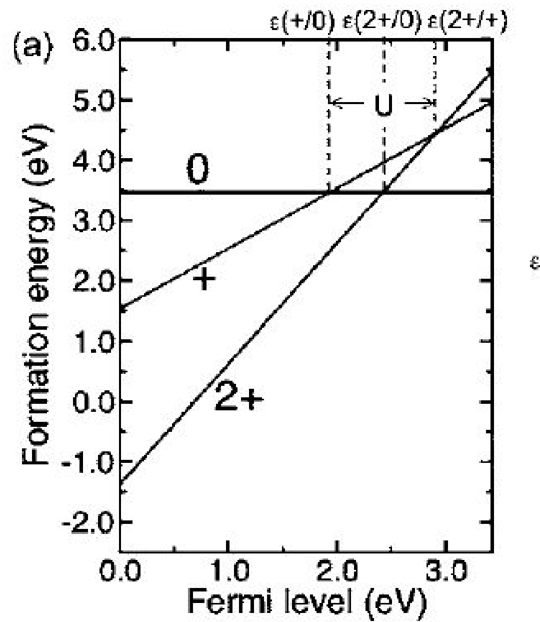


(b)

Figure 3-12 Transfer characteristics of IGZO TFTs under various sweep ranges with 450 nm illumination (a) [V_{GS} = -10 ~ 10V, -20 ~ 20V, -30 ~ 30V], (b) [V_{GS} = -30 ~ 30V, -30 ~ 10V, -10 ~ 30V]



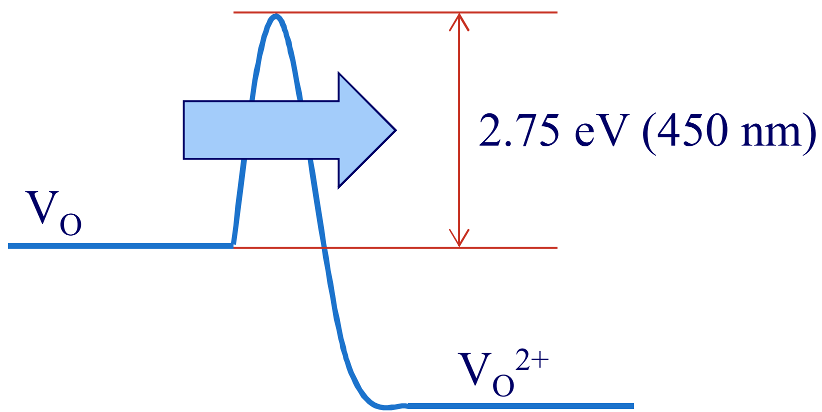
(a)



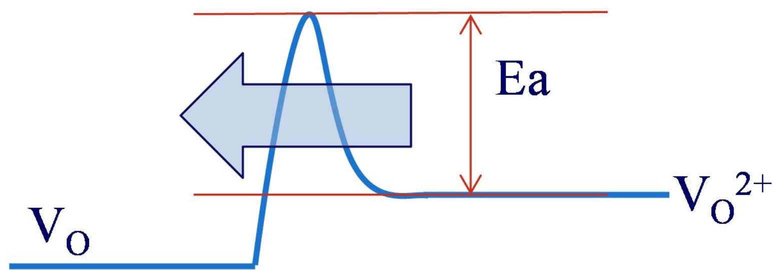
ε

(b)

Figure 3-13 (a) The energy level of sub-band states of neutral oxygen vacancy (V_O), singly ionized oxygen vacancy (V_O^+) and doubly ionized oxygen vacancy (V_O^{2+}). (b) Formation energies vs Fermi level for oxygen vacancies in ZnO in the 0, 1+, and 2+charge states, under Zn-rich conditions. [117]

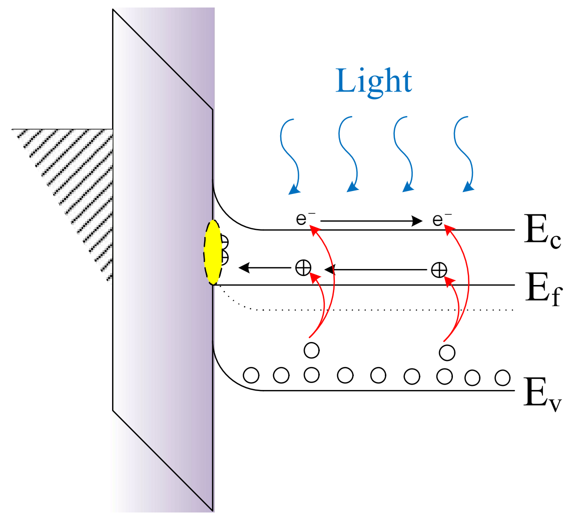


(a)

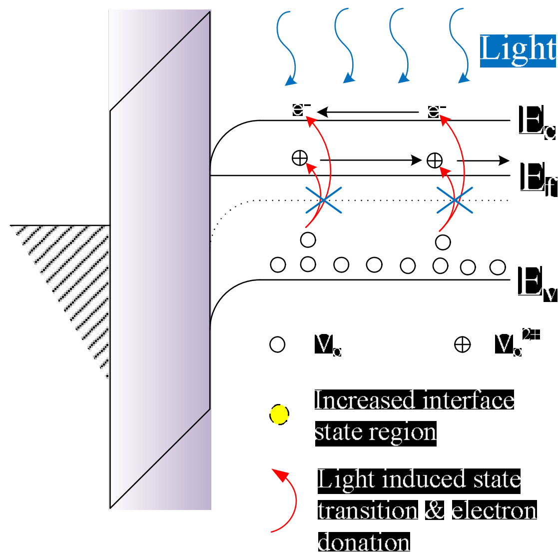


(b)

Figure 3-14 Schematic configuration coordinate diagrams for (a) negative gate bias and (b) positive gate bias.



(a)



(b)

Figure 3-15 Band diagram of IGZO TFTs with light illumination under (a) negative gate bias and (b) positive gate bias.

3.6.4 Conclusion

I have observed light-induced hysteresis under various wavelengths and sweep ranges, and have investigated its mechanism. Light-induced hysteresis is caused by the increase of V_0^{2+} states at the interface due to initial negative gate bias and light. Increased sub band gap states at the interface cause increase of sub-threshold slope during forward sweep. The magnitude of light-induced hysteresis increased, as the wavelength decreased. And the magnitude of light-induced hysteresis increased, as the magnitude of applied initial negative bias increased.

3.7 Light-Induced Hysteresis of IGZO TFTs with Various Temperatures

3.7.1 Introduction

Recently, amorphous Indium-Gallium-Zinc Oxide thin-film transistors (a-IGZO TFTs) have attracted considerable attention due to their high mobility and good uniformity [22, 27]. Device characteristics under light illumination and various temperatures are critical issues because display backplanes suffer from light illumination and thermal energy simultaneously.

The reliability of a-IGZO TFTs under bias, temperature, environment, and illumination has been intensively studied [57, 59, 65, 68, 118]. However, light-induced changes in device characteristics, such as hysteresis, are scarcely reported. It has been reported that the sub-threshold slope (S.S.) and off current increases as wavelength decreases from 700 nm to 450 nm [119]. Our experimental results show that S.S. increased compared to dark state during the forward sweep under 450-nm illumination condition. However, S.S. did not change compared to dark state during the reverse sweep. This could be called light-induced hysteresis. Our experimental results show that this light-induced hysteresis increases as temperature increases. The mobility of IGZO TFTs also increased, as temperature increased.

The purpose of my work is to investigate the light-induced hysteresis of a-IGZO TFTs under various temperatures.

One of the important parameters for stable driving of an active matrix display is the hysteresis of TFTs. When the hysteresis occurs, threshold voltage shift and current variation could be observed according to the previously applied gate bias.

And current could be altered, when the mobility changes. A small variation of drain current may alter the brightness of organic light emitting diode (OLED) because OLED is a current-driven device.

3.7.2 Experimental methods

The a-IGZO TFTs were fabricated on a glass substrate with an inverted staggered structure. First, Mo/AlNd were deposited and patterned as the gate electrode. SiO_2 of 2,000 Å thickness was then deposited by plasma-enhanced chemical vapor deposition (PECVD) and served as the gate dielectric layer. The IGZO (In:Ga:Zn = 1:1:1) layer with a thickness of 500 Å was deposited by sputtering. The SiO_2 etch stop layer was deposited by PECVD. The source and drain were formed by depositing a layer of Mo and were patterned by dry etching. The SiO_2 layer was used as a passivation layer. Annealing of the device was performed as the final process at 300 °C in ambient air. The channel width was 24 μm and the length was 12 μm. The transfer characteristics of the TFTs were evaluated using an Agilent B1500A semiconductor parameter analyzer. For the light illumination test, the device was irradiated by a xenon lamp using narrow band pass filters.

3.7.3 Experimental results and discussions

Figure 3-16 (a) shows the transfer curves under the 450-nm illumination at 30°C, 60 °C, and 90 °C. The center wavelengths of the band pass filters were 450-nm and the light intensity was adjusted to 1 mW/cm^2. The transfer curves were measured by the double sweep method from −20V to 20V, and the drain bias was fixed to 10 V. The transfer curves measured under dark condition did not show any hysteresis. However, the transfer curves measured at 450-nm illumination showed hysteresis, and it increased as temperature increased. In order to confirm whether or not this phenomenon is hysteresis, we measured IGZO TFT under various sweep ranges. Figure 3-16 (b) shows the transfer curves measured under various sweep ranges at 60 °C. The magnitude of hysteresis (ΔV) was 4.02 V (0.57 V) when the transfer curve was measured from -30V to 30 (from -10V to 10V). ΔV increased according to the initial negative gate bias. ΔV was extracted by the difference between the gate voltages of the forward sweep and the reverse sweep at a drain current of 10^{-11} A. These experimental results support that this phenomenon is light-induced hysteresis.

Figure 3-17 (a) shows the magnitude of hysteresis (ΔV) under lights of various temperatures. ΔV was increased from 0.89 V to 4.35 V as temperature increased from 30 °C to 90 °C. When the transfer curve was measured from −20 V to 20 V, an increased sub-threshold slope was observed under the 450-nm illumination. It has recently been reported that light-induced device characteristics and reliability were related to oxygen vacancy [57, 59, 65]. It has also been reported that neutral oxygen vacancies (V_O) are distributed above the valence band maximum, while doubly ionized oxygen vacancies (V_O^{2+}) are distributed below the conduction band minimum [59, 120]. Photon irradiation and negative gate bias causes the transition of V_O states to the V_O^{2+} states and the donation of two

electrons to the conduction band. The generated V_O^{2+} states at the channel diffuse to the interface due to applied negative gate bias during the forward sweep. V_O^{2+} could diffuse in amorphous phase with the aid of negative gate bias [59, 65].

Figure 3-17 (a) shows mobility as a function of temperature. Mobility increased from 13.3 cm^2/V·s to 15.5 cm^2/V·s as temperature increased from 30 °C to 90 °C. The mobility of the a-IGZO TFT strongly depends on carrier concentration [22]. Electron concentration could be increased by light and thermal energy. The light-induced electron concentration can be ignored since the light illumination conditions were fixed. To increase the mobility of a-IGZO TFTs, thermal-induced free carrier concentration should be increased as much as the intrinsic carrier concentration. The intrinsic carrier concentration of IGZO is known to be 10^{16-20} cm^{-3} [22, 115].

$$\Delta n = N_{sites} \exp\left(-\frac{E^f}{k_B \cdot \Delta T} \right) \quad (1)$$

A ZnO-based oxide semiconductor exhibits unintentional n-type conductivity due to its native point defects [120, 121]. The native point defect concentration increased as the operating temperature increased. Thermal-induced free carrier concentration could be estimated using equation (1) [120]. E^f is the formation energy, N_{sites} is the number of sites the defect can be incorporated on, k_B is the Boltzmann constant, and T is the temperature. As temperature increases from 30 °C to 90 °C, Δn could be increased as much as the intrinsic carrier concentration. The mobility of the a-IGZO TFTs increased as the electron concentration increased.

Figure 3-17 (b) shows why light-induced hysteresis was increased as temperature increased. As discussed above, the point defect concentration is

increased with the temperature. And state transition frequency is increased with the temperature. As temperature increased, more V_O^{2+} states could be generated under the same illumination condition. The sub-threshold slope of the forward sweep increased due to the increased V_O^{2+} states. Therefore, light-induced hysteresis was increased with the temperature.

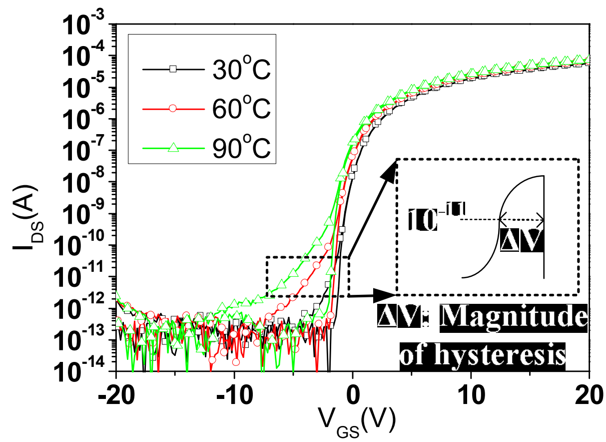
Figure 3-18 shows C-V characteristics under dark and illumination condition (center wavelength = 450 nm, intensity = 1mW/cm^2) measured at (a) 60 °C (W/L = 1000/6) and (b) 90 °C (W/L = 2000/6). C-V curves were measured by double sweep method from -20V to 20V. Large width samples were employed in order to measure C-V characteristics accurately. Hysteresis was observed under illumination condition, while hysteresis was not observed under dark condition. And the magnitude of hysteresis increases, as temperature increases from 60 °C to 90 °C. The C-V characteristics suggested that interface states are generated during forward sweep. And the C-V characteristics supported the mechanism of light-induced hysteresis.

Figure 3-19 shows the energy band diagrams under (a) large negative V_{GS}, (b) small negative V_{GS}, and (c) positive V_{GS}. When large negative V_{GS} is applied under the illumination, positive interface states are generated. It results in the positive shift of threshold voltage. The generated interface states are filled by electrons, as the surface potential increases. When the states are filled, the charge states become neutral. When the positive V_{GS} is applied, all of the interface states are occupied.

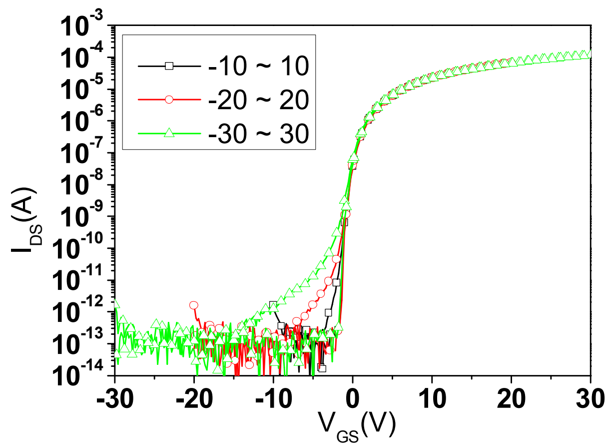
Figure 3-20 (a) shows the transfer curve before and after a positive bias illumination temperature stress (PBITS) condition. Gate bias was applied at 25 V and drain bias was applied at 0 V for 3,000 seconds. The device was irradiated with 450 nm wavelength light and temperature was set to 60°C. The transfer

curve and magnitude of hysteresis did not change after PBITS stress. Figure 3-20 (b) shows the transfer curve before and after a negative bias illumination temperature stress (NBITS) condition. Gate bias was applied at −20 V and drain bias was applied at 0 V for 3,000 seconds. The other stress conditions were the same as the PBITS condition. The transfer curve shifted to a negative direction after NBITS stress, and the magnitude of hysteresis was increased as much as 0.74 V.

Similar to the explanation of light-induced hysteresis, light-induced V_O^{2+} is temporarily trapped to the interface due to the negative gate bias. When prolonged negative bias and illumination stress are applied to the device, the V_O^{2+} states turn to the stable states due to the proceeding of outward relaxation [59, 120]. The transfer curve could be shifted to a negative direction after NBITS stress due to the trapped V_O^{2+} states. The magnitude of hysteresis could be increased due to the increased sub-band gap states. These experimental results also support our proposed explanation of light-induced hysteresis.

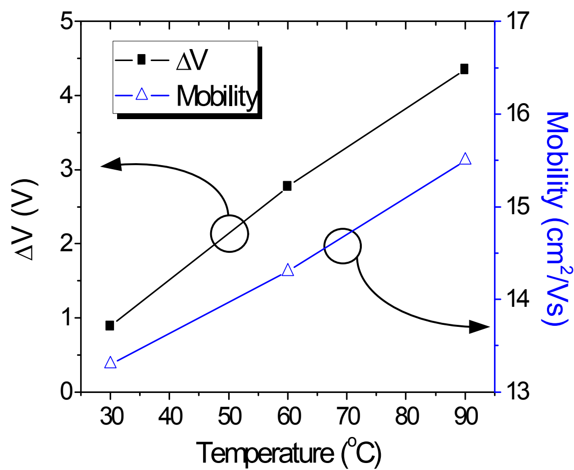


(a)

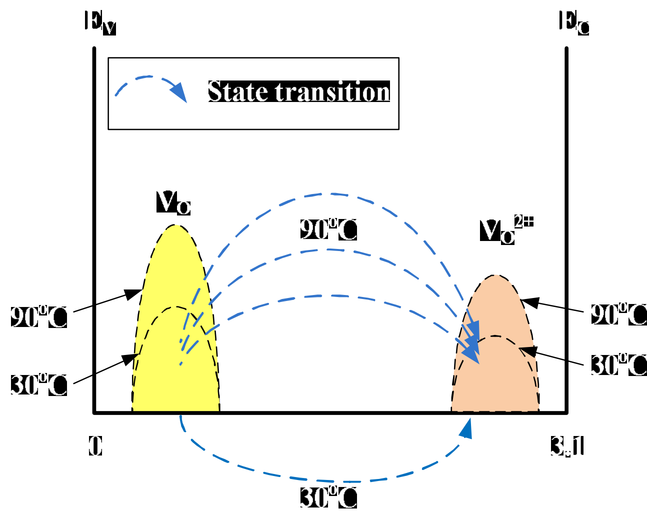


(b)

Figure 3-16 (a) Transfer curves under the 450-nm illumination condition at 30 °C, 60 °C, and 90 °C. (b) Transfer curves measured under various sweep ranges.

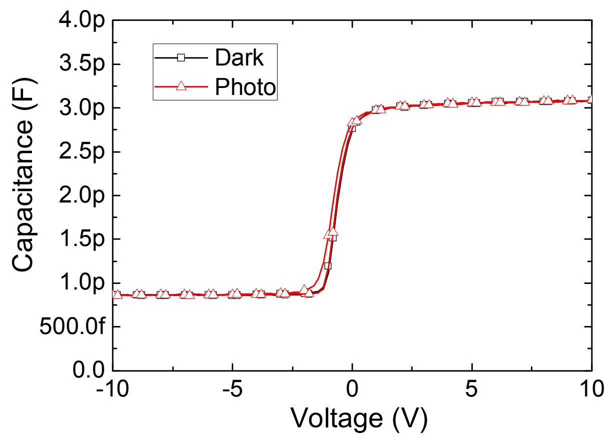


(a)

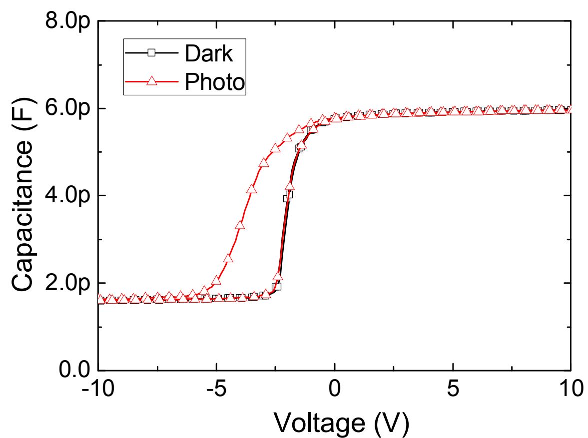


(b)

Figure 3-17 (a) The magnitude of hysteresis and mobility as a function of temperature. (b) Schematic sub-band gap states to explain why light-induced hysteresis increases as temperature increases.

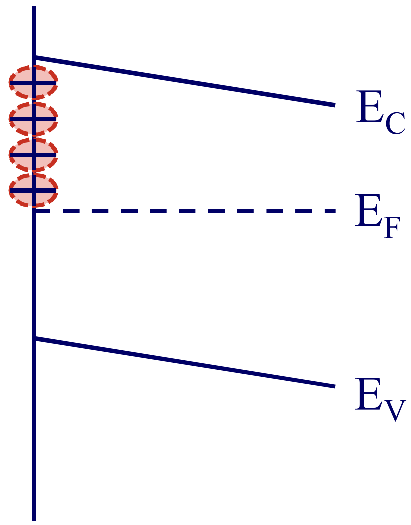


(a)

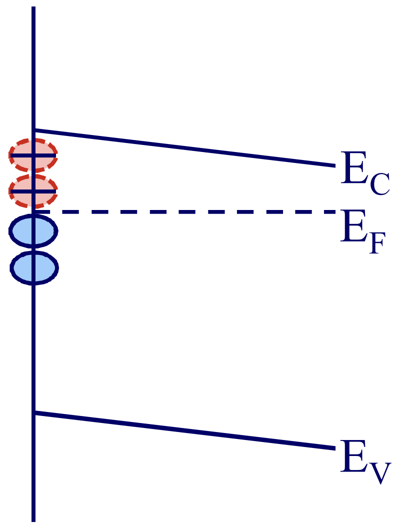


(b)

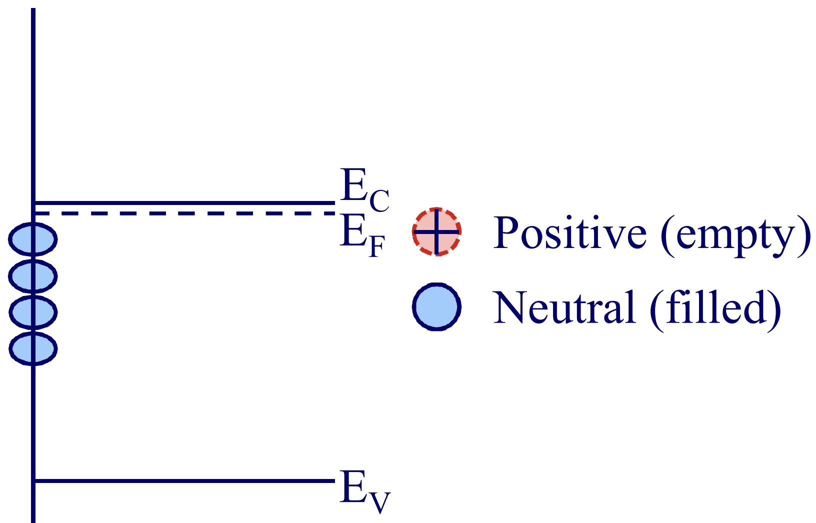
Figure 3-18 C-V characteristics under dark and light-illumination measured at (a) 60°C (W/L = 1000/6) and (b) 90°C (W/L = 2000/6).



(a)

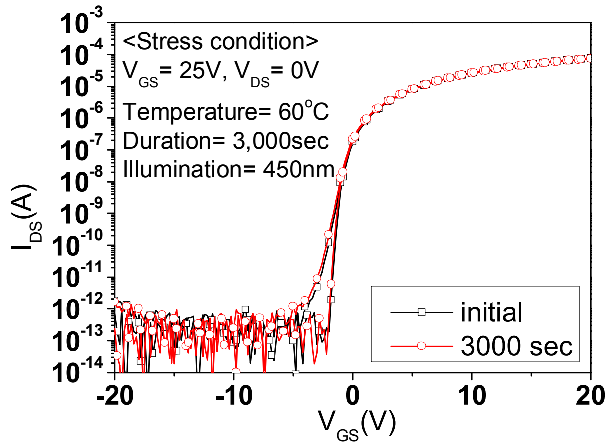


(b)

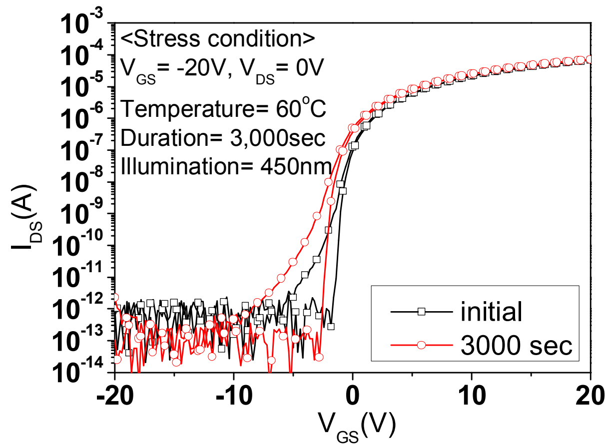


(c)

Figure 3-19 Energy band diagrams under (a) large negative V_{GS}, (b) small negative V_{GS}, and (c) positive V_{GS}.



(a)



(b)

Figure 3-20 Transfer curves before and after (a) positive bias illumination temperature stress and (b) negative bias temperature illumination stress conditions. A detailed stress condition is shown in the figures.

3.7.4 Conclusion

I have investigated the light-induced hysteresis of a-IGZO TFTs, which is caused by the increased V_O^{2+} states at the interface due to initial negative gate bias and light. Increased sub-band gap states at the interface increase the sub-threshold slope during the forward sweep. The magnitude of light-induced hysteresis and transition rate from V_O states to V_O^{2+} states are increased, as the temperature increases. We have observed light-induced hysteresis under various temperatures, and have investigated its mechanism.

3.8 Bias illumination stress induced instability

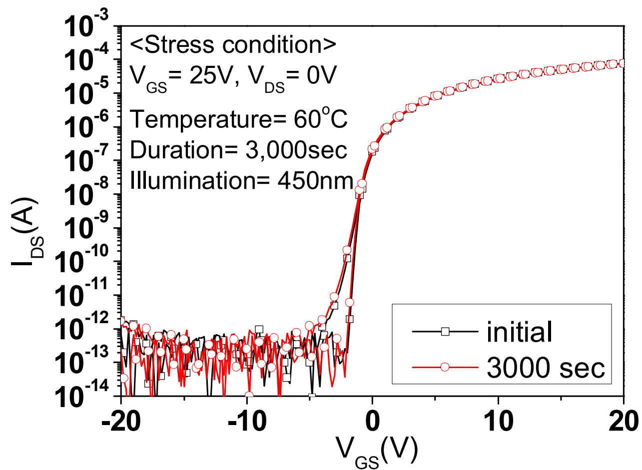
Figure 3-21 shows the transfer curves before and after (a) positive bias illumination temperature stress and (b) negative bias temperature illumination stress. For positive (negative) bias illumination temperature stress, the gate bias was applied at 25 V (-20 V) and drain bias was applied at 0 V for 3,000 seconds. The device was irradiated with 450 nm wavelength light and temperature was set to 60 °C. The transfer curve and magnitude of hysteresis did not change after positive bias illumination temperature stress. The transfer curve shifted to a negative direction by the amount of 0.83 V after negative bias illumination temperature stress. The threshold voltage shift accelerated under negative bias illumination stress, and these results coincide with the previous reports [56, 57, 61, 66].

In order to investigate the negative bias illumination temperature stress in detail, we have applied negative bias illumination temperature stress under various gate bias and various temperatures. Figure 3-22 shows the transfer curves before and after (a) -10 V, (b) -20 V, and (c) -30 negative bias temperature illumination stress for 3,000 seconds. The device was irradiated with 450 nm wavelength light and temperature was set to 30 °C. The change of transfer curve after negative bias illumination stress was not significant, as the magnitude of applied stress bias increased. Figure 3-23 shows the transfer curves before and after negative bias temperature illumination stress under (a) 30 °C, (b) 60 °C, and (c) 90 °C. The gate bias was applied to -20 V, and the drain bias was applied at 0 V for 3,000 seconds. The illumination condition was same to the above experiment. As the temperature increased, the magnitude of threshold voltage shift was increased. Figure 3-24 shows the time dependence of threshold voltage shift (ΔV_{TH}) due to the above negative bias illumination stress conditions (a)

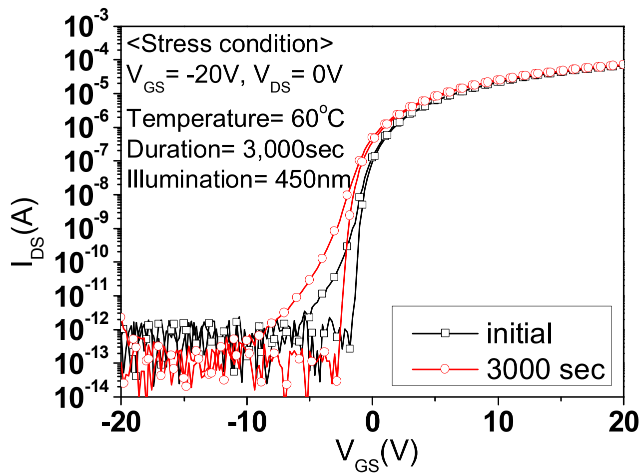
under different stress gate bias (V_{GS} = -10 V, -20 V, -30 V) and (b) under different temperatures (T = 30 °C, 60 °C, 90 °C). As the magnitude of stress gate bias increased from -10 V to -30 V, the threshold voltage shift was increased from 0.23 V to 0.52 V. As the temperature increased from 30 °C to 90 °C, the threshold voltage shift was increased from 0.36 V to 1.86 V. We could conclude that the effect of temperature on negative bias illumination stress is more significant than that of the magnitude of negative bias.

Figure 3-25 shows the time dependence of threshold voltage shift (ΔV_{TH}) due to negative bias illumination stress under 90 °C. Fitting to (a) power law and (c) logarithmic law are shown as solid lines. The power law fitting has the lower value of the standard error than the logarithmic fitting law. The state creation process shows the power law time dependence and is thermally activated [37, 39].

Light-induced V_O^{2+} is temporarily trapped to the interface due to the negative gate bias. When prolonged negative bias and illumination stress are applied to the device, the V_O^{2+} states turn to the stable states due to the proceeding of outward relaxation [59, 120]. The transfer curve could be shifted to a negative direction after negative bias illumination temperature stress due to the trapped V_O^{2+} states. As the temperature increases, the state creation process is increased, resulting in increase of threshold voltage shift.

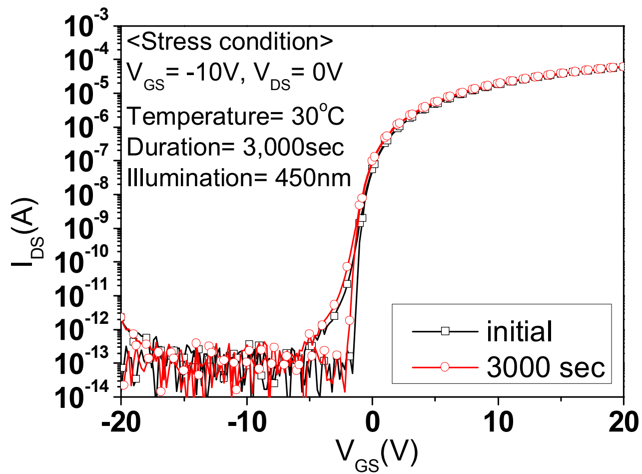


(a)

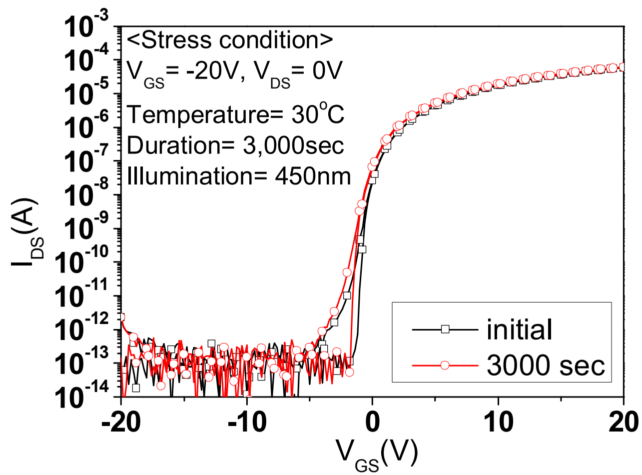


(b)

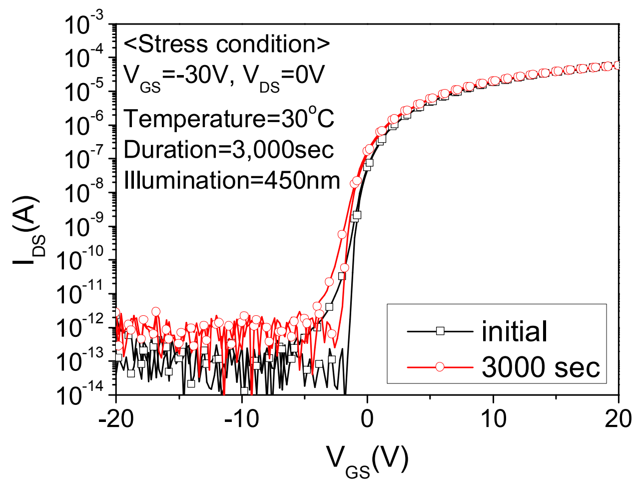
Figure 3-21 Transfer curves before and after (a) positive bias illumination temperature stress and (b) negative bias temperature illumination stress. A detailed stress condition is shown in the figures.



(a)

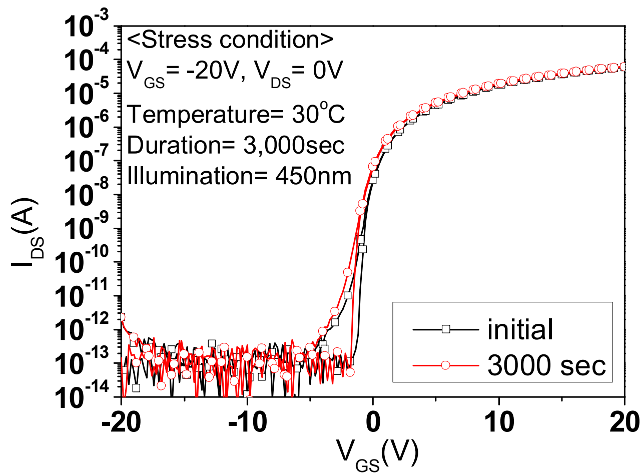


(b)

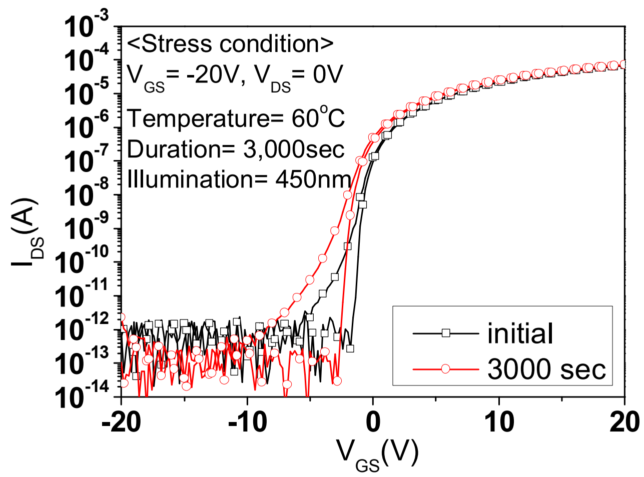


(c)

Figure 3-22 Transfer curves before and after (a) -10 V, (b) -20 V, and (c) -30 negative bias temperature illumination stress. A detailed stress condition is shown in the figures.



(a)



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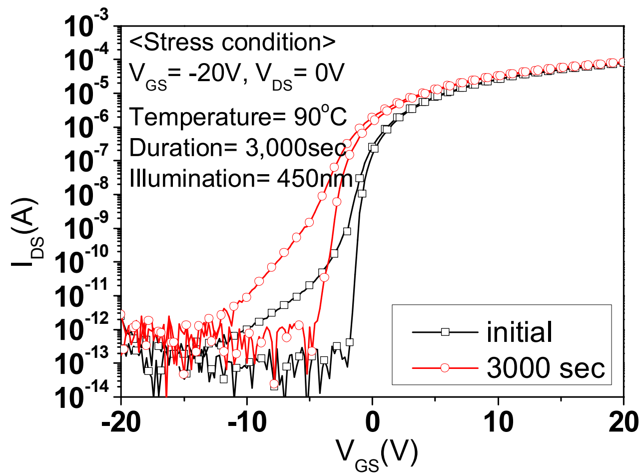
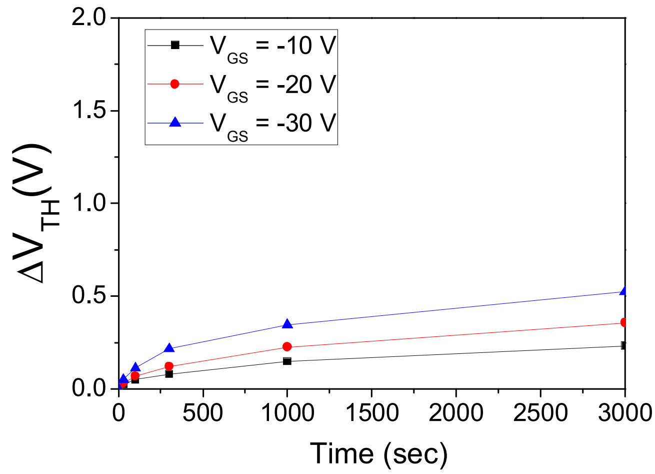
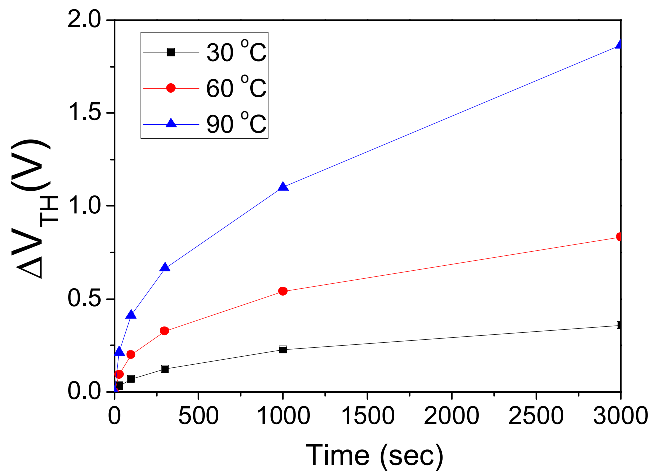


(c)

Figure 3-23 Transfer curves before and after negative bias temperature illumination stress under (a) 30 °C, (b) 60 °C, and (c) 90 °C. A detailed stress condition is shown in the figures.

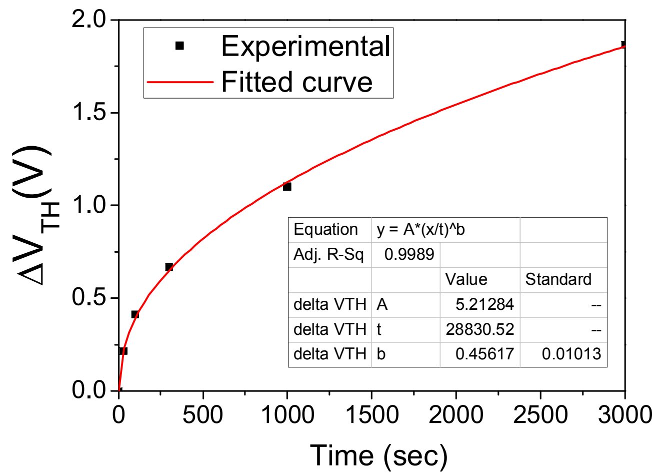


(a)

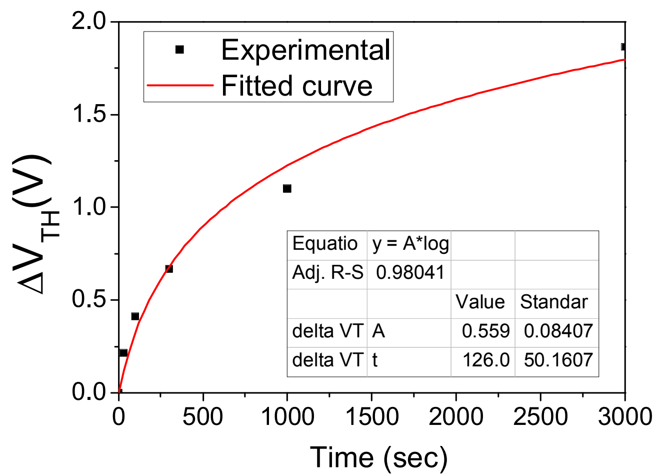


(b)

Figure 3-24 Time dependence of threshold voltage shift (ΔV_{TH}) due to negative bias illumination stress (a) under different stress gate bias (V_{GS} = -10 V, -20 V, -30 V) and (b) under different temperatures (T = 30 °C, 60 °C, 90 °C).



(a)



(b)

Figure 3-25 Time dependence of threshold voltage shift (ΔV_{TH}) due to negative bias illumination stress under 90 °C. Fitting to (a) power law and (c) logarithmic law are shown as solid lines.

Chapter 4 The electrical characteristics and reliability of IGZO TFTs on flexible substrate

4.1 Overview

In this chapter, the electrical characteristics and reliability of IGZO TFTs on flexible substrate are discussed. Firstly, the fabrication process is introduced. The IGZO TFTs were fabricated on a polyimide (PI) substrate with an inverted staggered structure. An inorganic buffer layer, composed of SiO_2 and SiN_x multi-layer, was deposited over the entire substrate area by plasma enhanced chemical vapor deposition (PECVD), in order to prevent the environmental stress, such as water or oxygen molecules.

In order to investigate the effects of PI on the characteristic and reliability of IGZO TFTs, I have fabricated the IGZO TFTs on glass substrate and PI substrate. The transfer curves of IGZO TFTS on glass substrate and PI substrate were not changed under the temperature from 30 °C to 90 °C. Threshold voltage shift between glass substrate and PI substrate was almost identical regardless of temperature (from 30 °C to 90 °C). We could conclude that the effects of PI on the characteristic and reliability of IGZO TFTs were negligible.

In order to investigate the effects of the buffer layer on the characteristic of IGZO TFTs, we have fabricated the IGZO TFTs on PI substrate with 2 kinds of multi-buffer layer structures (oxide interface and nitride interface). In case of employing nitride interface, threshold voltage was decreased and mobility was increased. When nitride interface is employed, more hydrogen could be introduced. Secondary ion mass spectroscopy (SIMS) profile supports the hydrogen incorporation.

And the effects of passivation layer on the electrical stability of IGZO TFTs with single passivation layer and double passivation layer fabricated on PI substrate were investigated. The positive bias stress and negative bias stress were applied to the

IGZO TFTs at various temperatures from 20 °C to 80 °C. The threshold voltage shift of double passivation device was larger than that of single passivation device under NBTS. The threshold voltage shift of double passivation device was slightly less than that of single passivation device under PBTS. The threshold voltage shift of NBTS is considerably increased than that of PBTS at high temperature due to the difference between conduction band offset and valence band offset.

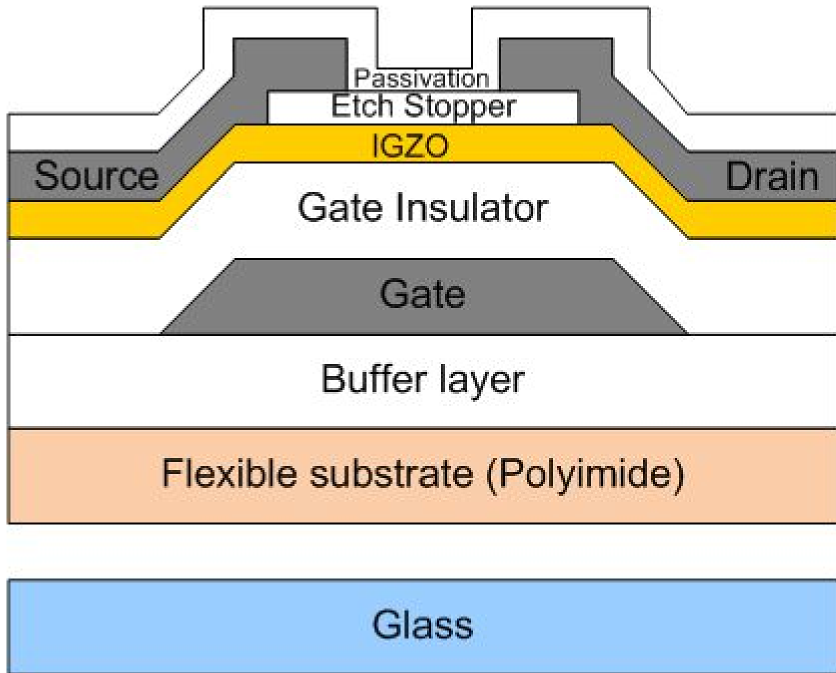
Lastly, the effects of mechanical bending on the electrical stability of flexible IGZO TFTs were investigated.

4.2 Fabrication process of IGZO TFTs on polyimide substrate

The IGZO TFTs were fabricated on a polyimide (PI) substrate with an inverted staggered structure. Figure 4-1 (a) shows the cross sectional view of the fabricated IGZO TFTs. PI is spin-coated onto glass substrate, in order to overcome difficulties in handling flexible freestanding plastic substrates, eliminating the problem of plastic shrinkage with high temperature processing and allowing the use of standard semiconductor equipment.

An inorganic buffer layer, composed of SiO_2 and SiN_x multi-layer, was deposited over the entire substrate area by plasma enhanced chemical vapor deposition (PECVD). Mo/AlNd were deposited and patterned as the gate electrode. SiO_2 of 2,000 Å thickness was then deposited by plasma-enhanced chemical vapor deposition (PECVD) and served as the gate dielectric layer. The IGZO (In:Ga:Zn = 1:1:1) layer with a thickness of 500 Å was deposited by sputtering. The SiO_2 etch stop layer was deposited by PECVD. The source and drain were formed by depositing a layer of Mo and were patterned by dry etching. The SiO_2 layer was used as a passivation layer. After device fabrication, the PI substrates were released by laser irradiation process. Table 4-1 summaries the layers information of the fabricated flexible IGZO TFTs. Figure 4-1 (b) shows the photograph of the fabricated flexible oxide TFTs after laser detaching.

The transfer characteristics of the TFTs were evaluated using an Agilent B1500A semiconductor parameter analyzer. For the light illumination test, the device was irradiated by a xenon lamp using narrow band pass filters.



(a)

(b)

Figure 4-1 (a) The cross-sectional view and (b) the photograph of the fabricated flexible oxide TFTs after laser detaching.

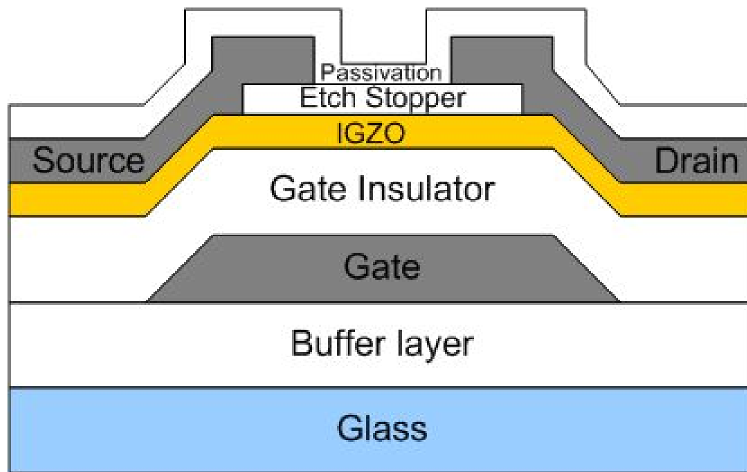
Table 4-1 The layers information of the fabricated flexible oxide TFTs.

Layer	Material	Equipment
Buffer layer	SiO_2 / SiN_x multi-layer	PECVD
Gate	Mo/AlNd	DC sputter
Gate Insulator	SiO_2 200 nm	PECVD
Active	IGZO 50nm	DC sputter
Etch stopper	SiO_2 50 nm	PECVD
Source/Drain	Mo	DC sputter
Passivation	SiO_2 200 nm	PECVD

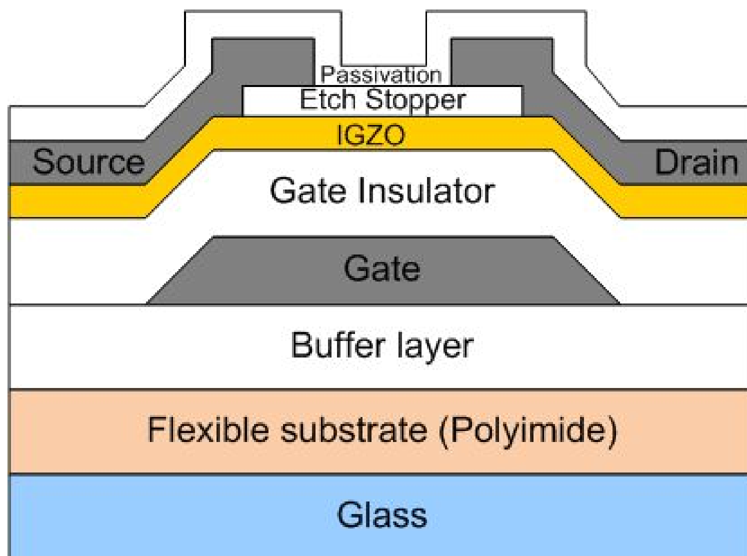
4.3 Comparison between IGZO TFTs on glass substrate and flexible substrate

In order to investigate the effects of polyimide (PI) on the characteristic and reliability of IGZO TFTs, we have fabricated the IGZO TFTs on glass substrate and PI substrate. The fabrication process was identical between two samples except for PI coating and inorganic buffer layer deposition. Figure 4-2 shows the cross-sectional view of fabricated IGZO TFTs on (a) glass substrate and (b) polyimide substrate. The channel width was 43 μm, and the channel length was 10 μm.

Figure 4-3 shows the transfer curves of fabricated IGZO TFTS on glass substrate and PI substrate under (a) 30 °C (b) 90 °C. The transfer curves of IGZO TFTS on glass substrate and PI substrate were not changed regardless of temperature (from 30 °C to 90 °C). Figure 4-4 shows the comparison of threshold voltage shift (ΔV_{TH}) between glass substrate and PI substrate under negative bias temperature stress. Gate-source voltage was applied to -30 V, and drain-source voltage was applied to 0.1 V for 3,600 seconds for negative bias temperature stress. Temperature is from 30 °C to 90 °C. Threshold voltage shift between glass substrate and PI substrate was almost identical regardless of temperature. We could conclude that the effects of PI on the characteristic and reliability of IGZO TFTs were negligible.

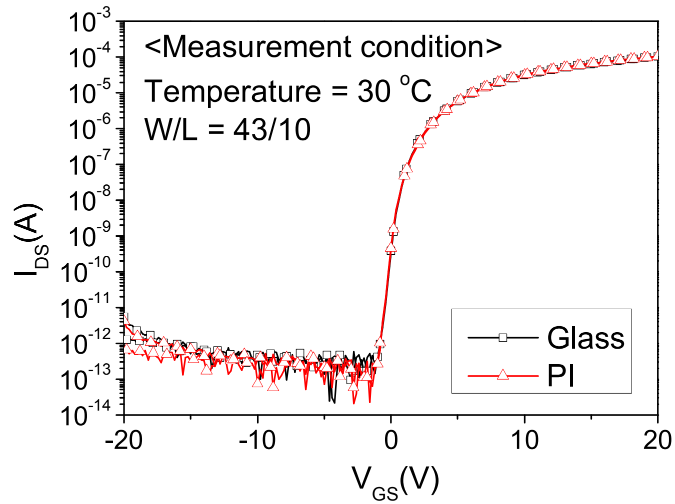


(a)

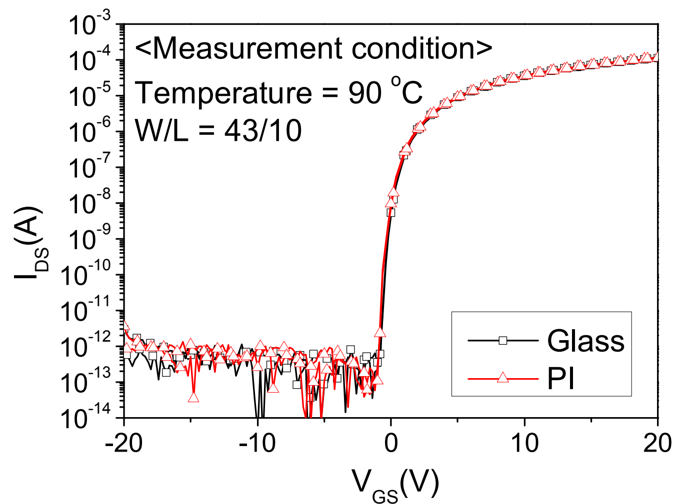


(b)

Figure 4-2 The cross-sectional view of fabricated IGZO TFTs on (a) glass substrate and (b) polyimide substrate.



(a)



(b)

Figure 4-3 Comparison of transfer curves between glass substrate and PI substrate under (a) 30 °C (b) 90 °C.

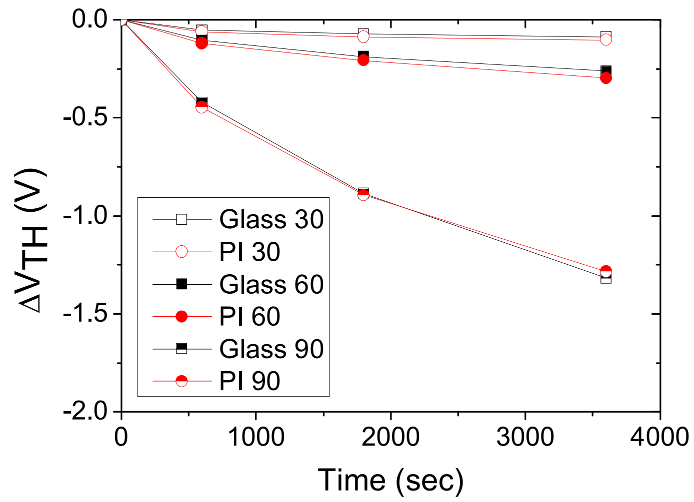


Figure 4-4 Comparison of threshold voltage shift (ΔV_{TH}) between glass substrate and PI substrate under negative bias temperature stress. Temperature is from 30 °C to 90 °C.

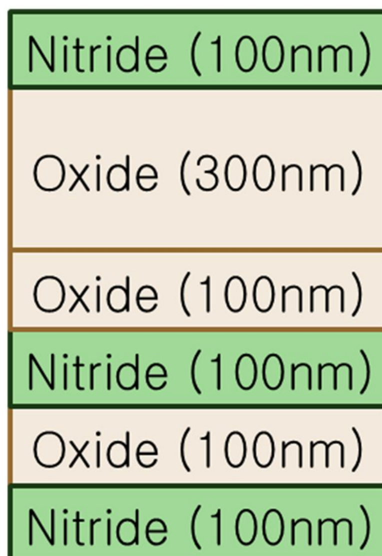
4.4 Effects of the buffer layer on the electrical characteristics of flexible IGZO TFTs

In order to investigate the effects of the buffer layer on the characteristic of IGZO TFTs, we have fabricated the IGZO TFTs on PI substrate with 2 kinds of multi-buffer layer structures. The fabrication process was identical between two samples except for the inorganic multi-buffer layer. Figure 4-5 shows the schematic of inorganic multi-buffer layer with an (a) oxide interface and (b) nitride interface. The (SiN_X of 100 nm thickness/ SiO_2 of 100 nm thickness/ SiN_X of 100 nm thickness/ SiO_2 of 100 nm thickness/ SiO_2 of 300 nm thickness) were deposited for oxide interface multi-buffer layer, and (SiN_X of 100 nm thickness/ SiO_2 of 100 nm thickness/ SiN_X of 100 nm thickness/ SiO_2 of 100 nm thickness/ SiO_2 of 300 nm thickness/ SiN_X of 100 nm thickness) were deposited for nitride interface multi-buffer layer. The channel width was 43 μm, and the channel length was 10 μm.

Figure 4-6 shows the transfer curves of fabricated IGZO TFTs employing oxide interface and nitride interface. The transfer curves measured under 30 °C. Threshold voltage of the oxide interface was 0.53 V, while that of the nitride interface was -0.12 V. Mobility of the oxide interface was 11.75 $cm^2/V{\cdot}s$, while that of the nitride interface was 13.54 $cm^2/V{\cdot}s$. In case of employing nitride interface, threshold voltage was decreased and mobility was increased. SiN_X has higher nitrogen concentration than SiO_2. Some of hydrogen could be diffused to IGZO layer during post thermal annealing process. Figure 4-7 shows the hydrogen atomic ratio versus depth profile of oxide interface and nitride interface measured by secondary ion mass spectroscopy (SIMS). Hydrogen atomic ratio of nitride interface was 2.81 %, while hydrogen atomic ratio of oxide interface was 2.48 %. The difference of hydrogen atomic ratio results in

the difference of threshold voltage and mobility. When the hydrogen is introduced in the oxide semiconductor, hydrogen contributes shallow donor states, resulting in increase of their electrical conductivity [122, 123]. Therefore, threshold voltage could be negatively shifted and mobility could be increased, in case of nitride interface.

(a)



(b)

Figure 4-5 Schematic of inorganic multi-buffer layer with an (a) oxide interface and (b) nitride interface. Detailed layer information is shown in figures.

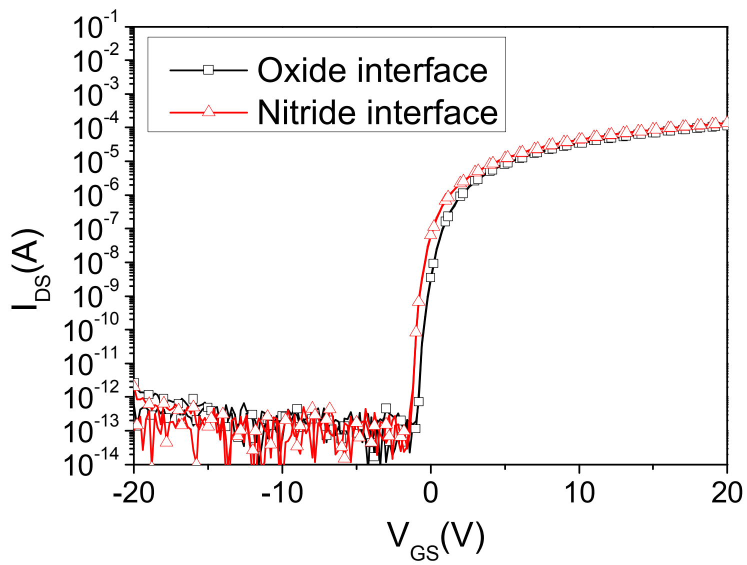


Figure 4-6 Transfer curves of fabricated IGZO TFTs employing oxide interface and nitride interface.

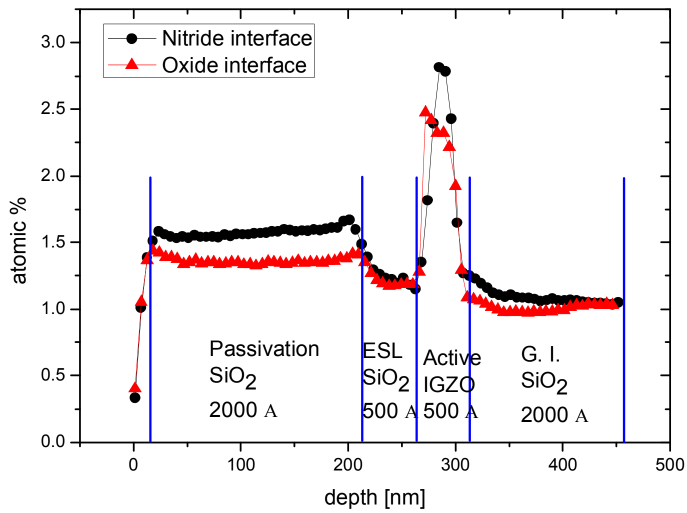


Figure 4-7 Hydrogen atomic ratio versus depth profile of oxide interface and nitride interface measured by secondary ion mass spectroscopy (SIMS).

Table 4-2 The extracted parameters of the fabricated IGZO TFTs employing oxide interface and nitride interface.

Sample	V_{TH}	Mobility
Oxide interface	0.53 V	11.75 $cm^2/V \cdot s$
Nitride interface	-0.12 V	13.54 $cm^2/V \cdot s$

4.5 Effects of passivation layer on the electrical stability of flexible IGZO TFTs

4.5.1 Introduction

Recently, considerable amount of attention is paid on the flexible display. Indium-Gallium-Zinc-Oxide thin-film transistor (IGZO TFT) is a promising candidate for the flexible display, due to its high mobility, good uniformity, and low temperature process.

Device characteristics and reliabilities of IGZO TFTs are closely related to their passivation layer. [71, 81, 87] It is well known that back-interface of IGZO TFTs are easily react with oxygen or water molecules. [70, 73, 76] The absorbed oxygen forms depletion layer below the back interface, resulting in positive shift of threshold voltage. [70] On the other hand, the absorbed water donates free electron, resulting in negative shift of threshold voltage. [73, 76] For the stable operation of flexible IGZO TFTs, high quality passivation layer should be employed.

Silicon oxide (SiO_x) and silicon nitride (SiN_x) are widely used for passivation layer of semiconductor devices. When SiN_x are deposited directly on the active layer, IGZO could be turned into a conductor due to hydrogen rich plasma. [84] Therefore, SiO_x single passivation layer and SiO_x/ SiN_x double passivation layer are mainly studied for passivation layer of IGZO TFTs.

It has been reported on negative bias illumination temperature stress (NBITS) of IGZO TFTs with SiO_x single passivation layer and SiO_x/ SiN_x double passivation layer. [84, 85] However, the reliability of IGZO TFTs with double passivation layer and single passivation layer under various temperatures was not reported

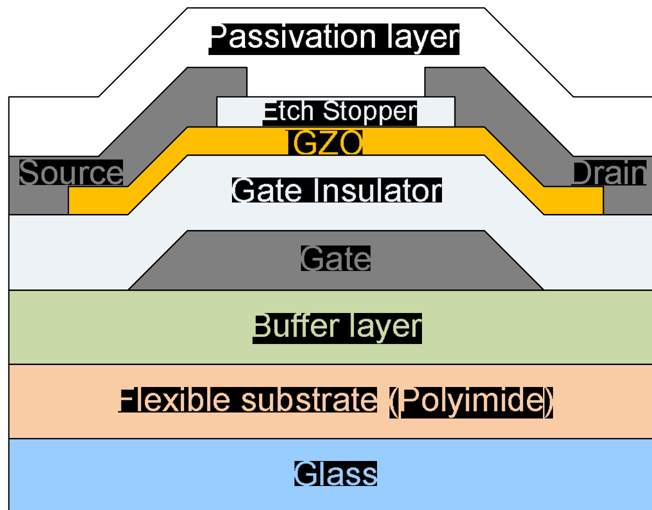
yet. The electrical stability at high temperature is important, because the actual display backplane could be operated over 70 ^{o}C due to backlight or battery.

The purpose of our work is to investigate the effects of passivation layer on the PBTS and NBTS at various temperatures. In this work, we have fabricated IGZO TFTs on polyimide (PI) substrate with with single passivation layer and double passivation layer. The PBTS and NBTS were applied to the fabricated devices at various temperatures from 20 ^{o}C to 80 ^{o}C.

4.5.2 Experimental methods

We have fabricated inverted staggered bottom-gate structure IGZO TFT on PI substrate, as shown in Figure 4-8. An inorganic buffer layer was deposited by plasma enhanced chemical vapor deposition (PECVD). AlNd/ Mo bi-layer was deposited by sputter, and served as a gate electrode. A SiO_x of 2000 Å thickness film was deposited by PECVD, and served as gate insulator. The IGZO layer was deposited by DC sputtering. A SiO_x layer was deposited by PECVD, and served as etch stopper layer. Mo/ Al/ Mo tri-layer was deposited by sputter, and served as a source drain electrode. The SiO_x of 2000 Å thickness single passivation layer and SiO_x/ SiN_x of 2000 Å/ 300 Å thickness double passivation layer was deposited by PECVD, respectively.

To compare the different dimension devices, we normalized drain current ($I_{DS}|_{normalized}$) by channel width and channel length. Threshold voltage (V_{TH}) is taken as the gate voltage corresponding to $I_{DS}|_{normalized} = 10^{-8}$ A.



<Single passivation>

<Double passivation>

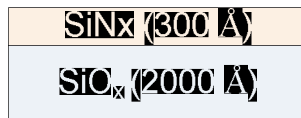


Figure 4-8 Cross sectional view of fabricated IGZO TFT on glass/ PI substrate. SiO_x (2000 Å) single passivation layer and SiO_x/ SiN_x (2000 Å/ 300 Å) double passivation layer are fabricated respectively.

4.5.3 Experimental results and discussions

Figure 4-9 shows the transfer curves of fabricated IGZO TFTs with single passivation layer and double passivation layer measured at 20 ^{o}C. The transfer curves were measured by the double sweep method from −20 V to 20 V and the drain bias was varied from 1 V to 10 V. V_{TH}, mobility and sub-threshold slope (SS) of fabricated device was summarized at Table 4-3. V_{TH} of double passivation layer is negatively shifted, compared to that of single passivation layer. Difference of V_{TH} is attributed to the hydrogen, which is known to shallow donor of oxide semiconductor. [122] During SiN_x deposition, a small part of hydrogen could be reached at IGZO layer, because the size of hydrogen is very small. When hydrogen is introduced at IGZO layer, electron concentration is increased. And it results in negative shift of V_{TH}. Mobility of double passivation layer is larger than that of single passivation layer. Difference of mobility could be explained same way. Sub-threshold slope of double passivation layer is slightly increased due to the sub-band gap state made by hydrogen.

Figure 4-10 shows threshold voltage shifts with respect to time at various temperatures. For PBTS test, gate-source voltage (V_{GS}) was applied to 30 V and drain-source voltage (V_{DS}) was applied to 0.1 V for 3 hours. For NBTS test, V_{GS} was applied to -30 V and V_{DS} was applied to 0.1 V for 3 hours. Even 80 ^{o}C stress, the absolute value of ΔV_{TH} ($|\Delta V_{TH}|$) was less than 1.30 V. These results suggest that our fabricated devices are highly reliable.

The $|\Delta V_{TH}|$ of double passivation device was larger than that of single passivation device under NBTS test at all temperature range. Negative shift of V_{TH} during NBTS test is attributed to trapping of positive ions. In case of double passivation layer, hydrogen ions (H^+) could be introduced during SiN_x deposition. Therefore, positive ion concentration of double passivation device could be larger than that

of single passivation device. And it results in negative shift of V_{TH} under NBTS test.

The ΔV_{TH} of double passivation device was slightly less than that of single passivation device under PBTS test. These results might be attributed to passivation effect due to hydrogen plasma during SiN_x deposition. Hydrogen plasma could reduce interface trap density between gate insulator layer and active layer. [124] Electron trapping could be decreased at double passivation layer due to the passivation effect. However, passivation effect of hydrogen plasma could be very small, due to the existence of passivation layer and IGZO layer.

Figure 4-11 shows the plot of $|\Delta V_{TH}|$ vs 1/T for single passivation layer and double passivation layer devices under NBTS and PBTS tests. $|\Delta V_{TH}|$ of NBTS is more thermally activated than that of PBTS. This result is caused by the difference between conduction band offset (ΔE_C) and valence band offset (ΔE_V).

Figure 4-12 shows the band diagram of IGZO/ SiO_x stack structure. The band offsets were calculated using the values reported in the literature. [59] The calculated ΔE_C is about to 4.4 eV and ΔE_V is about to 1.4 eV. Negative ions are hardly trapped to the interface due to large ΔE_C. On the other hand, positive ions could be more easily trapped to the interface than negative ions due to small ΔE_V. If thermally activated positive ion concentration equals negative ion concentration, more positive ions could be trapped to the interface. Therefore, $|\Delta V_{TH}|$ of NBTS could be larger than that of PBTS at high temperature regime.

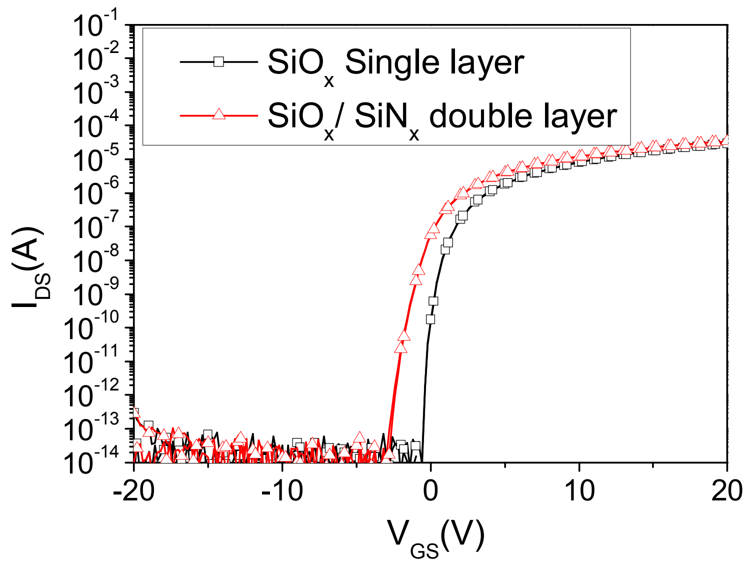
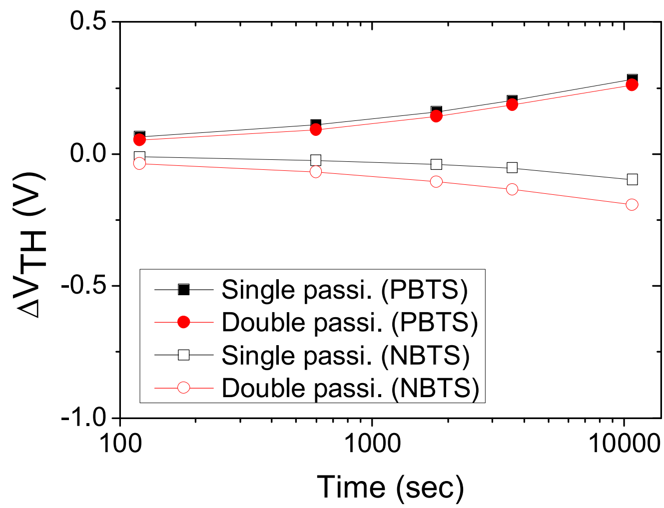
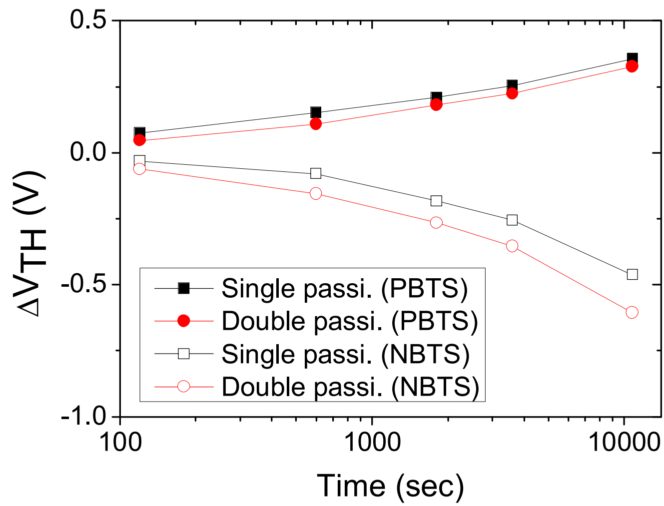


Figure 4-9 Transfer curves of fabricated IGZO TFTS with single passivation layer and double passivation layer measured at 20 °C.



(a)



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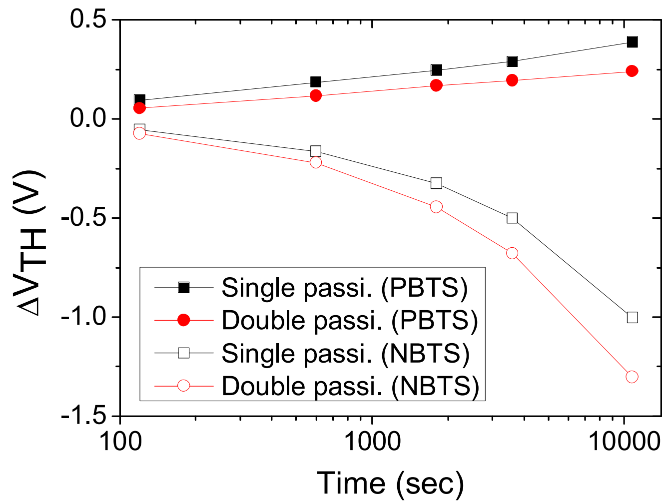
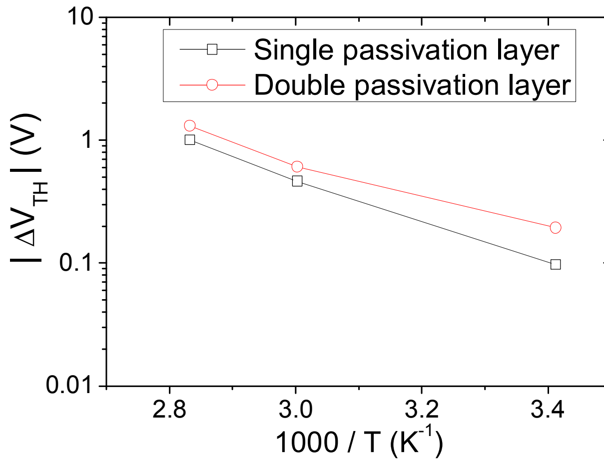
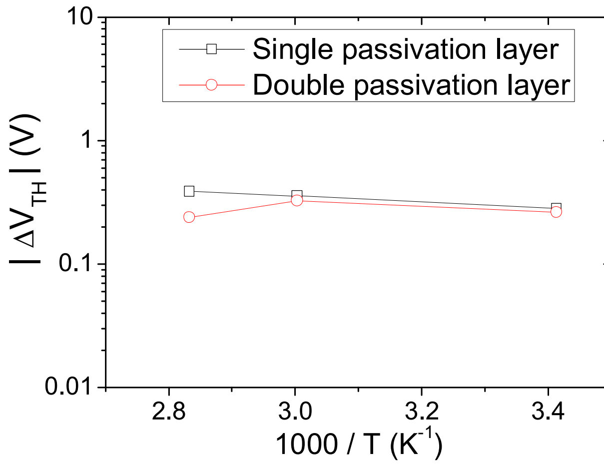


(c)

Figure 4-10 Threshold voltage shift vs stress time for stress applied at various temperature: (a) 20 °C, (b) 60 °C, and (c) 80 °C. For PBTS (NBTS) test, V_{GS} was applied to 30 V (-30 V) and V_{DS} was applied to 0.1V for 3 hours.



(a)



(b)

Figure 4-11 Plot of $|\Delta V_{TH}|$ vs 1/T for single passivation layer and double passivation layer devices, under (a) NBTS and (b) PBTS.

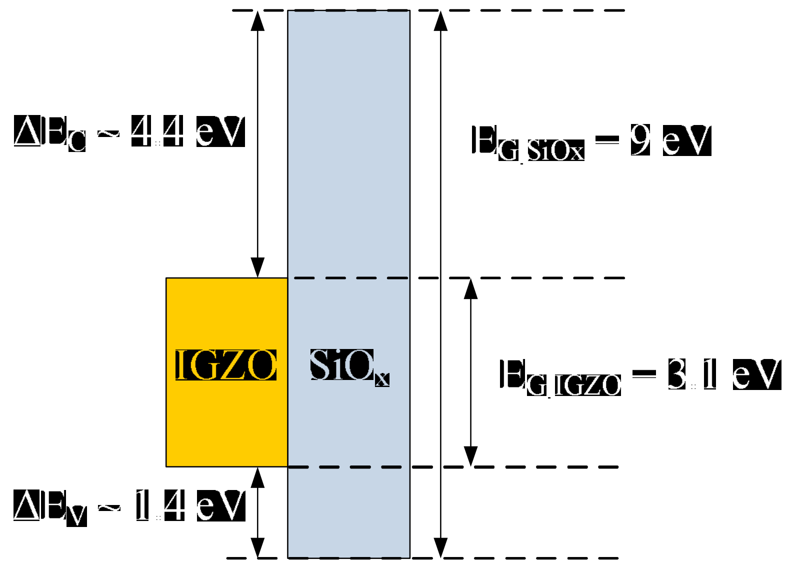


Figure 4-12 Band diagram of IGZO/ SiO_x stack structure.

Table 4-3 Fabricated device parameters measured at 20 ^{o}C.

Split	V_{TH} (V)	Mobility ($cm^2/V\cdot s$)	SS (V/dec)
Single passivation layer	0.66	13.41	0.121
Double passivation layer	-0.63	14.23	0.352

4.5.4 Conclusion

I have investigated effects of passivation layer on the electrical stability of IGZO TFTs with single passivation layer and double passivation layer at various temperatures. In case of double passivation layer, hydrogen ions (H^+) could be introduced during SiN_x deposition. Absorbed hydrogen increases carrier concentration and mobility, resulting in negative shift of V_{TH}. The absorbed hydrogen accelerates NBTS stress. $|\Delta V_{TH}|$ of NBTS is more thermally activated than that of PBTS due to the difference between ΔE_C and ΔE_V.

4.6 Effects of humidity on the electrical characteristics of IGZO TFTs

In order to investigate the effects of the humidity on the characteristic of IGZO TFTs, we have fabricated the un-passivated IGZO TFTs. The highly boron doped silicon wafer served as a gate electrode, and 2,000 Å thickness of thermal oxide served as a gate dielectric. The IGZO (In:Ga:Zn = 1:1:1) layer with a thickness of 500 Å was deposited by sputtering. The source and drain were formed by depositing a layer of ITO employing sputtering. The active and source-drain were pattered by using shadow mask. The channel width was 2,000 μm, and the channel length was 200 μm. Figure 4-13 shows the cross-sectional view of the fabricated un-passivated oxide TFTs.

Figure 4-14 shows the transfer curves of the fabricated un-passivated IGZO TFTs under (a) 30 °C (b) 50 °C (c) 70 °C as a function of relative humidity. In case of 30 °C and 50 °C, the transfer curves were scarcely changed as the relative humidity increased. However, In case of 70 °C, the transfer curves were significantly changed as the relative humidity increased.

Figure 4-15 shows the threshold voltage as a function of relative humidity measured by (a) forward sweep method (from -20 V to 20 V) and (b) reverse sweep method (from 20 V to -20 V) under 30 °C, 50 °C, and 70 °C. In case of 30 °C and 50 °C, the threshold voltage was scarcely changed. In case of 70 °C, the threshold voltage measured by forward sweep method was negatively shifted from 0 V to -5.13 V, as the relative humidity increased from 30 % to 90 %. In case of 70 °C, the threshold voltage measured by reverse sweep method was negatively shifted from 0.36 V to -2.67 V, as the relative humidity increased from 30 % to 90 %. The hysteresis was defined as the difference of the threshold

voltage measured by the forward sweep method and the reverse sweep method (V_{TH}|forward – V_{TH}|reverse). The hysteresis also increased from 0.36 V to 2.46 V, as the relative humidity increased from 30 % to 90 %. Figure 4-16 shows the leakage current as a function of relative humidity under 30 °C, 50 °C, and 70 °C. In case of 30 °C and 50 °C, the leakage current was scarcely changed as the relative humidity increased. In case of 70 °C, the leakage current was increased from 8.34 pA to 41.3 pA, as the relative humidity increased from 30 % to 90 %.

Figure 4-17 (a) shows the saturated water vapor as a function of temperature. As the temperature increased from 30 °C to 70 °C, the saturated water vapor was increased from 30 g/m^3 to 200 g/m^3. The relative humidity is defined as the ratio of the partial pressure of water vapor (H_2O) ($P_{present}$) in the mixture to the saturated vapor pressure of water ($P_{saturated}$) at a prescribed temperature. Relative humidity is normally expressed as a percentage and is calculated by using the following equation.

$$R.H. = \frac{P_{present}}{P_{saturated}} \times 100(\%)$$

Figure 4-17 (b) shows the current amount of water vapor as a function of relative humidity under 30 °C, 50 °C, and 70 °C. Over 140 g/m^3 of water vapor (corresponds to 70 °C of temperature and 70 % of relative humidity), the effects of humidity on the electrical characteristics of IGZO TFTs get more significant.

As the water vapor increased, the amount of the adsorbed water molecules at the back-interface of IGZO TFTs is increased. When the water molecules are adsorbed at the back-interface of IGZO TFTs, the free electrons are donated and the electric field is generated due to dipole moments. The leakage current could be increased due to the Fermi level pinning of the back-interface. And threshold voltage could be negatively shifted due to the dipole moment of the adsorbed

water molecules. I could estimate the number of absorbed water molecules about 3.28 X 10^{11} cm^{-2}, when 70 °C of temperature and 90 % of relative humidity is, by the following equation : $Q = C_i \cdot \Delta V_{TH}/q$ (C_i is the gate insulator capacitance per unit area, ΔV_{TH} is the threshold voltage shift). Figure 4-18 shows the schematic showing the adsorption of the water molecules under (a) high water vapor and (b) low water vapor. As the water vapor increased, the adsorbed water molecules at the back-interface are increased, resulting in increase of leakage current and threshold voltage shift.

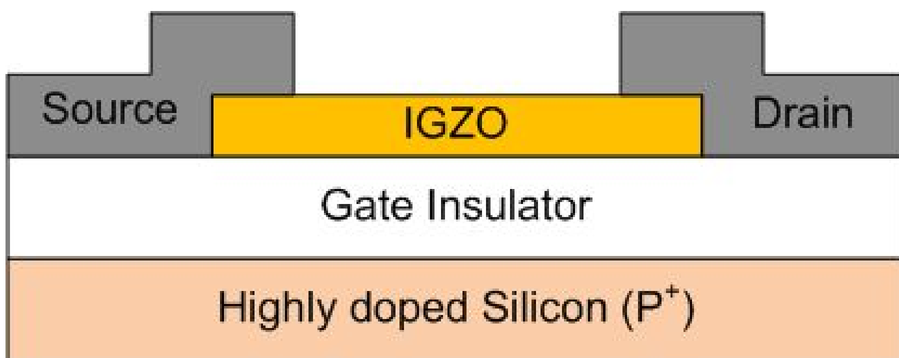
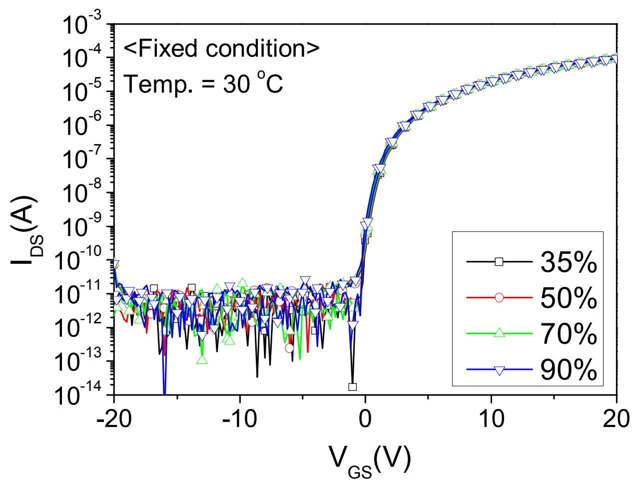
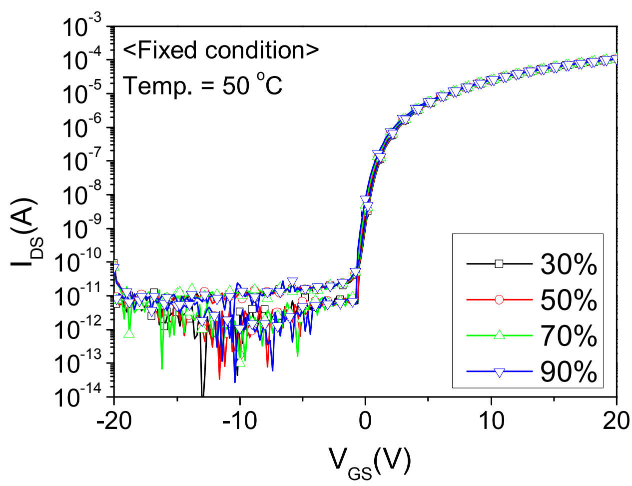


Figure 4-13 The cross-sectional view of the fabricated un-passivated oxide TFTs.



(a)



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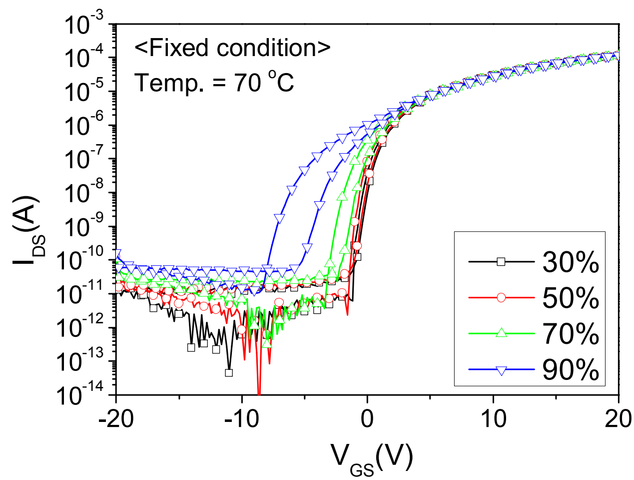
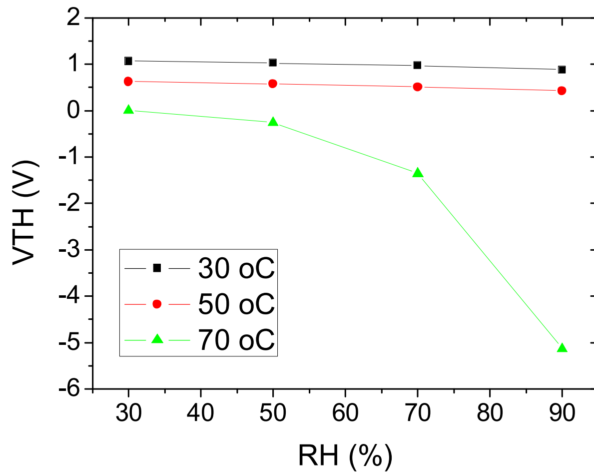
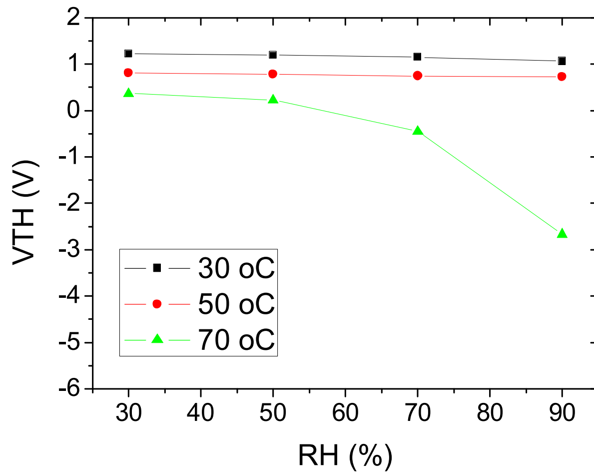


(c)

Figure 4-14 The transfer curves of the fabricated un-passivated IGZO TFTs under (a) 30 °C (b) 50 °C (c) 70 °C as a function of relative humidity.



(a)



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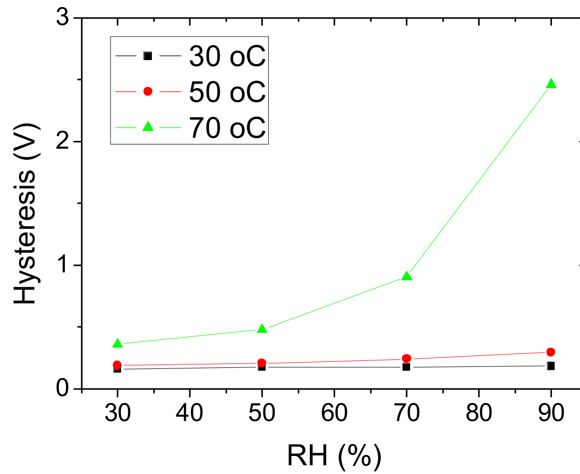


(c)

Figure 4-15 Threshold voltage as a function of relative humidity measured by (a) forward sweep method (from -20 V to 20 V) and (b) reverse sweep method (from 20 V to -20 V) under 30 °C, 50 °C, and 70 °C. (c) Hysteresis (V_{TH}|forward – V_{TH}|reverse) as a function of relative humidity under 30 °C, 50 °C, and 70 °C.

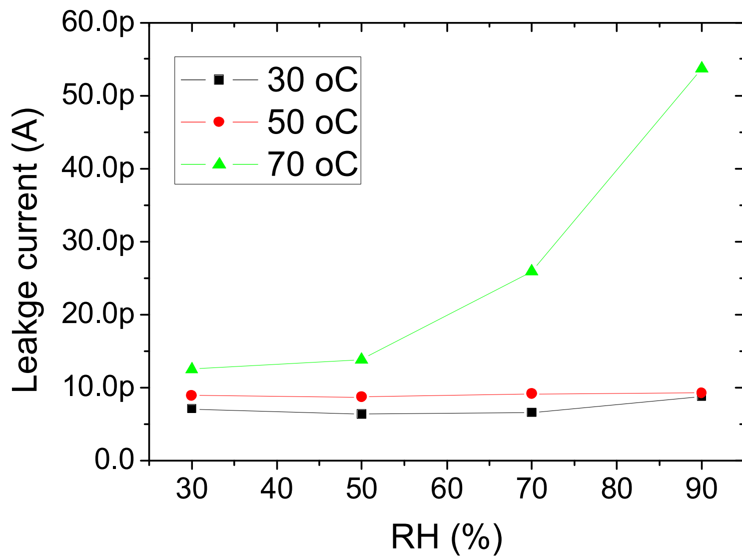
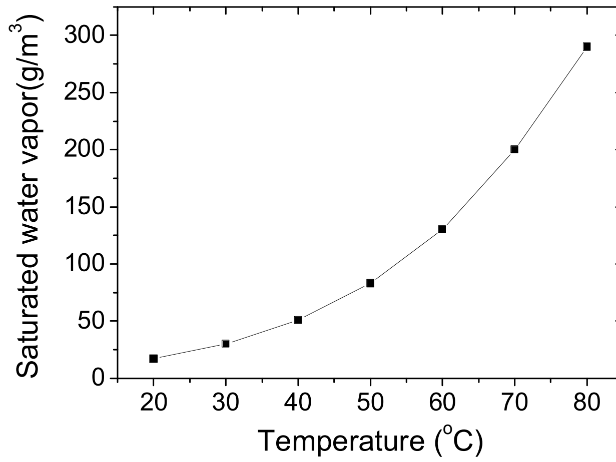
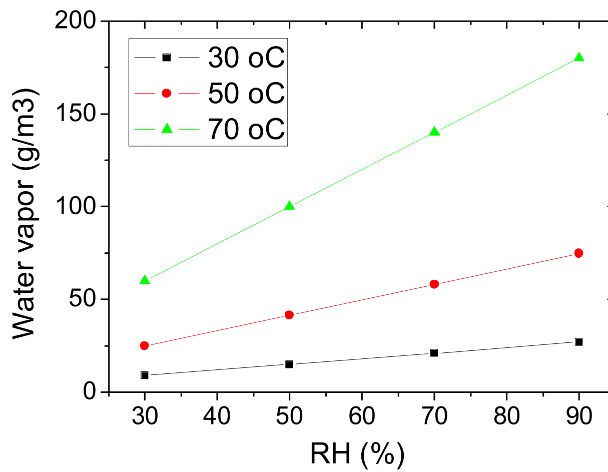


Figure 4-16 Leakage current as a function of relative humidity under 30 °C, 50 °C, and 70 °C.

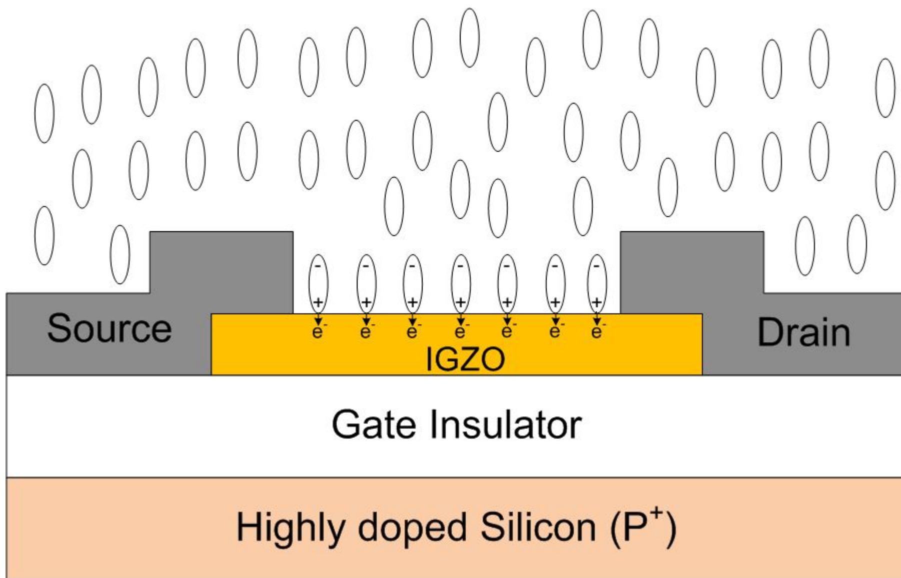


(a)



(b)

Figure 4-17 (a) Saturated water vapor as a function of temperature. (b) Current amount of water vapor as a function of relative humidity under 30 °C, 50 °C, and 70 °C.



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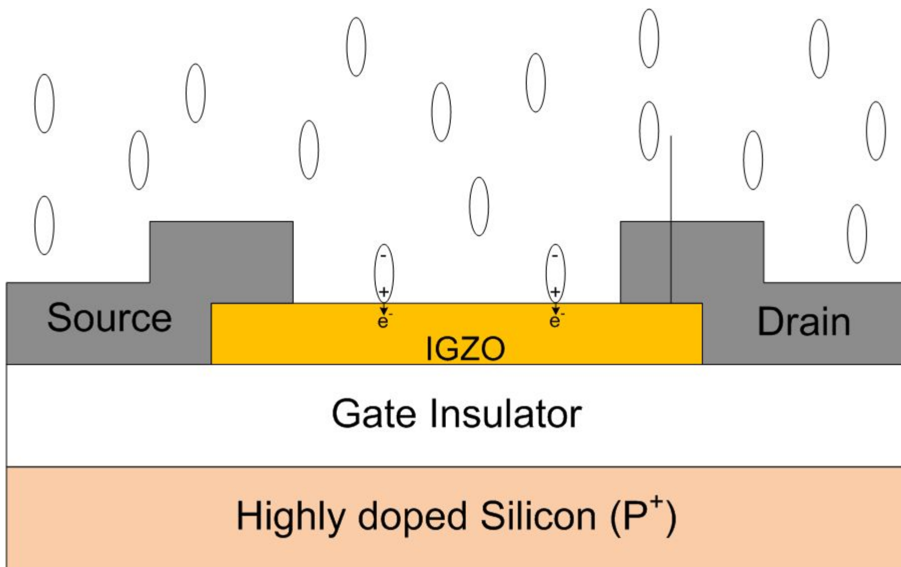


(b)

Figure 4-18 Schematic showing the adsorption of the water molecules under (a) high water vapor and (b) low water vapor.

4.7 Effects of mechanical bending on the electrical stability of flexible IGZO TFTs

In order to investigate the effects of mechanical bending on the electrical stability of IGZO TFTs, I have fabricated the IGZO TFTs on the PI substrate. The fabrication process is same as that of the explained at chapter 4.2. Figure 4-19 (a) shows a photograph of bending measurement system. I could measure the electrical characteristics of IGZO TFTs under the 5 mm bend radius condition. Figure 4-19 (b) shows the schematic showing bending direction perpendicular to channel (left) and parallel to channel (right). Temperature is set to room temperature.

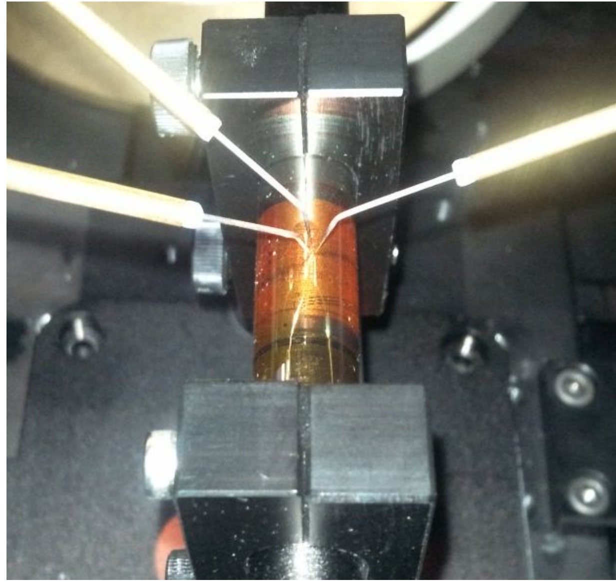
Figure 4-20 (a) shows a change of transfer curves on standing state for 3 hours under 5 mm bending radius. The bending direction is parallel to channel direction. The transfer curves were not changed for 3 hours. We measured the transfer curves on standing state for additional 16 hours under 5 mm bending radius. Figure 4-20 (b) shows a change of transfer curves on standing state for additional 16 hours. The transfer curves were not changed for total 19 hours. I could conclude that the effects of mechanical bending on the electrical characteristics of flexible IGZO TFTs on PI substrate are negligible.

In order to investigate the effects of bending direction, I applied positive bias temperature stress (PBTS) to the flexible IGZO TFTs under 5 mm bending radius with 2 types of bending directions. Figure 4-21 shows the shifts of transfer curves under PBTS (V_{GS} = 30 V, V_{DS} = 0.1 V) under 5 mm bending radius. Bending direction of Figure 4-21 (a) is perpendicular to channel and bending direction of Figure 4-21 (b) is parallel to channel. The effects of bending direction on the stability under PBTS were negligible. I applied negative bias temperature stress

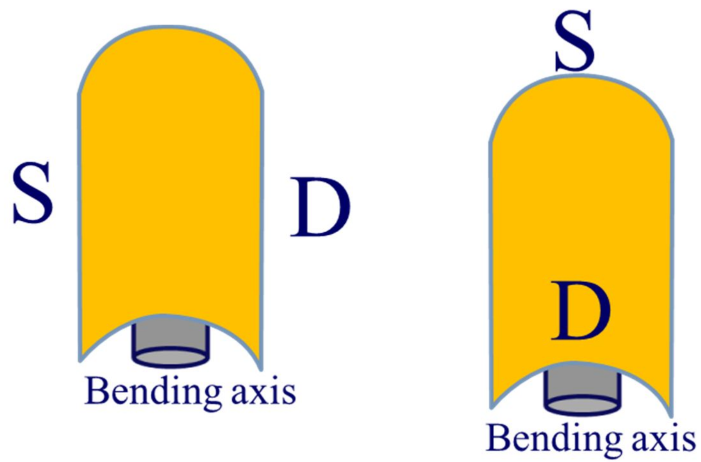
(NBTS) to the flexible IGZO TFTs under 5 mm bending radius with 2 types of bending directions. Figure 4-22 shows the shifts of transfer curves under NBTS (V_{GS} = -30 V, V_{DS} = 0.1 V) under 5 mm bending radius. Bending direction of Figure 4-22 (a) is perpendicular to channel and bending direction of Figure 4-22 (b) is parallel to channel. The effects of bending direction on the stability under NBTS were also negligible.

In order to compare the flat state and bending state, I applied positive bias temperature stress (PBTS) to the flexible IGZO TFTs under the flat state and bending state. Figure 4-23 shows the shifts of transfer curves under PBTS (V_{GS} = 30 V, V_{DS} = 0.1 V) under (a) flat condition and (b) bending condition. Figure 4-23 (c) shows the threshold voltage shift under PBTS as a function of time of flat condition and bending condition. The threshold voltage shifts under PBTS between the flat condition and the bending condition were very similar each other. And I applied negative bias temperature stress (NBTS) to the flexible IGZO TFTs under the flat state and bending state. Figure 4-24 shows the shifts of transfer curves under NBTS (V_{GS} = -30 V, V_{DS} = 0.1 V) under (a) flat condition and (b) bending condition. Figure 4-24 (c) shows the threshold voltage shift under NBTS as a function of time of flat condition and bending condition. The threshold voltage shifts under NBTS between the flat condition and the bending condition were very similar each other. Figure 4-25 shows the shifts of transfer curves under PBITS (V_{GS} = 30 V, V_{DS} = 0.1 V, λ = 400nm, Intensity = 0.2 mW/cm^2) under (a) flat condition and (b) bending condition. Figure 4-25 (c) shows the threshold voltage shift under PBITS as a function of time of flat condition and bending condition. The threshold voltage shifts under PBITS between the flat condition and the bending condition were very similar each other. Figure 4-26 shows the shifts of transfer curves under NBITS (V_{GS} = -30 V, V_{DS} = 0.1 V, λ = 400nm, Intensity = 0.2 mW/cm^2) under (a) flat condition and (b) bending condition.

Figure 4-26 (c) shows the threshold voltage shift under NBITS as a function of time of flat condition and bending condition. The threshold voltage shifts under NBITS between the flat condition and the bending condition were very similar each other. I could conclude that the effects of mechanical bending on the stability of IGZO TFTs were negligible.

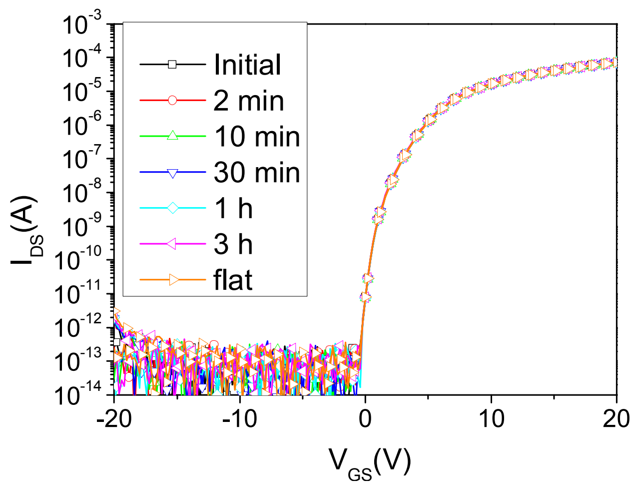


(a)

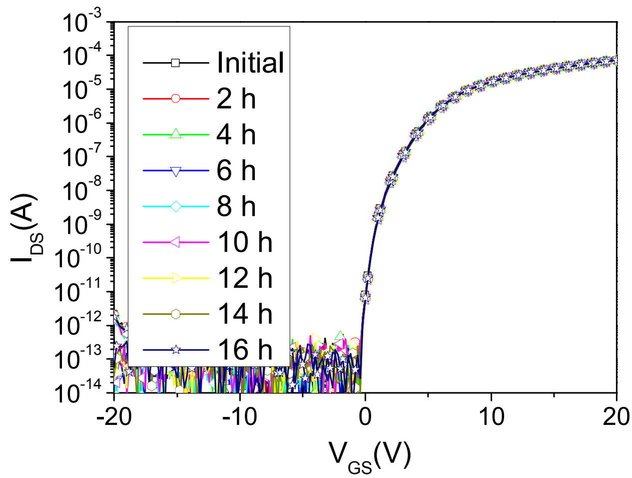


(b)

Figure 4-19 (a) A photograph of bending measurement system. (b) Schematic showing bending direction perpendicular to channel (left) and parallel to channel (right).

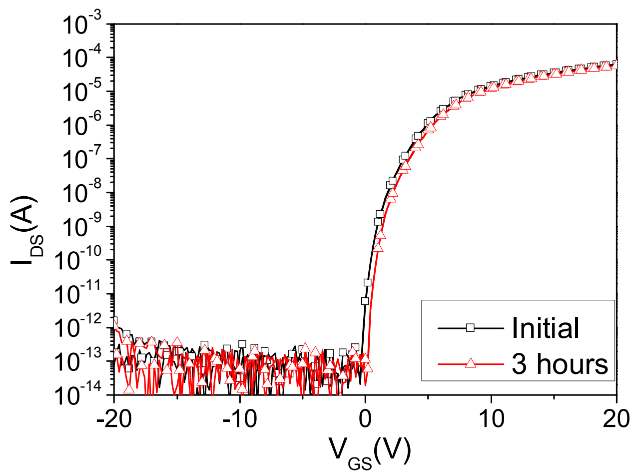


(a)



(b)

Figure 4-20 (a) A change of transfer curves on standing state for 3 hours under 5 mm bending radius. (b) A change of transfer curves on standing state for additional 16 hours under 5 mm bending radius.



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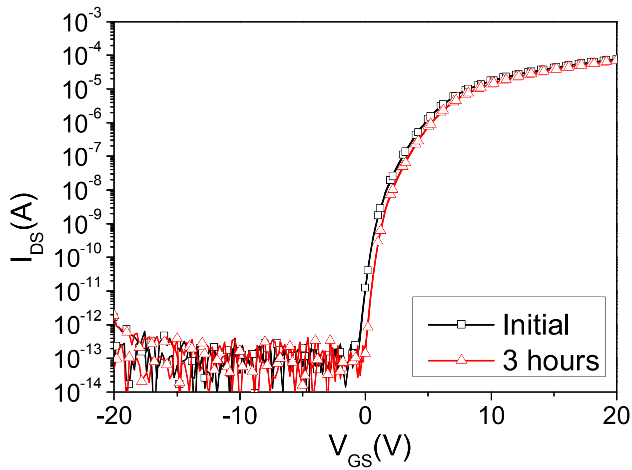
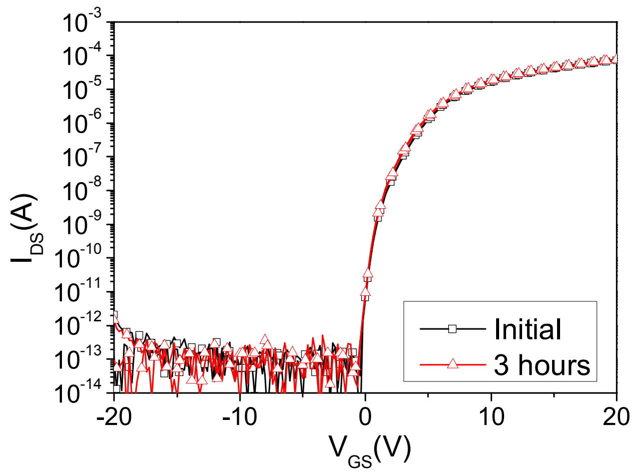
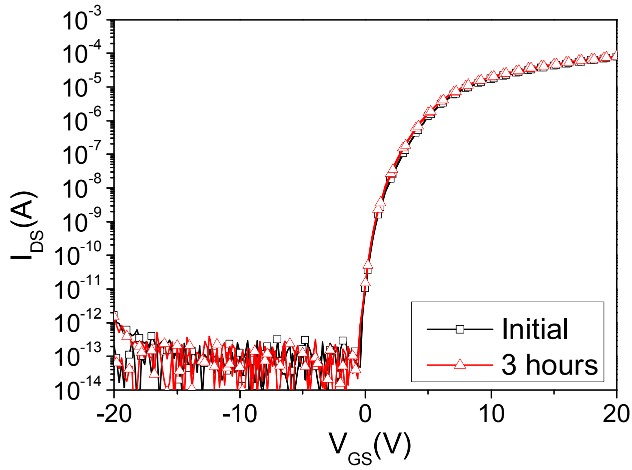


(b)

Figure 4-21 Shifts of transfer curves under PBTS (V_{GS} = 30 V, V_{DS} = 0.1 V) under 5 mm bending radius. (a) Bending direction is perpendicular to channel and (b) bending direction is parallel to channel.

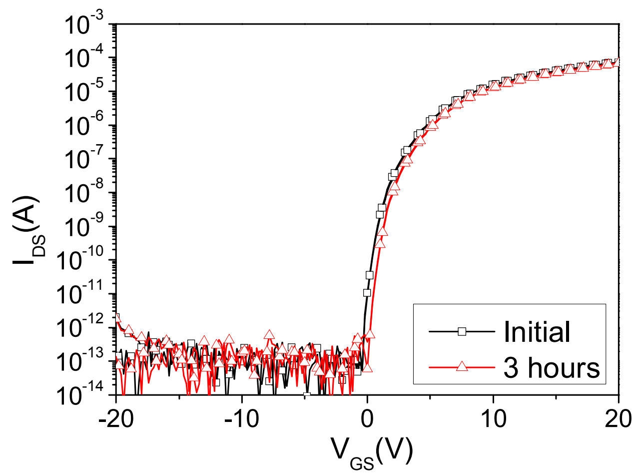


(a)

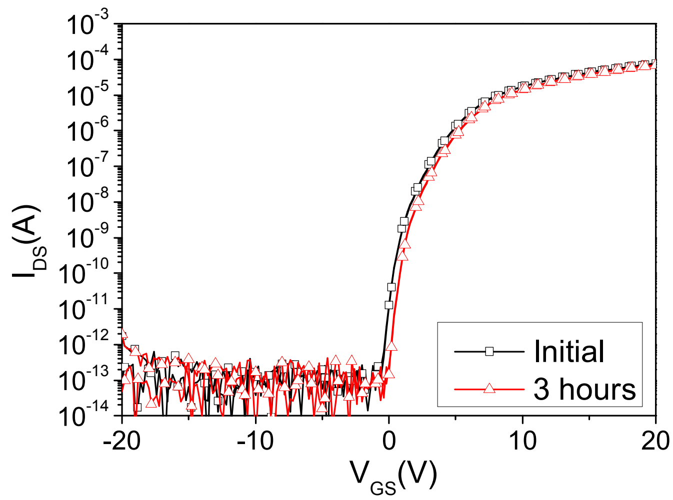


(b)

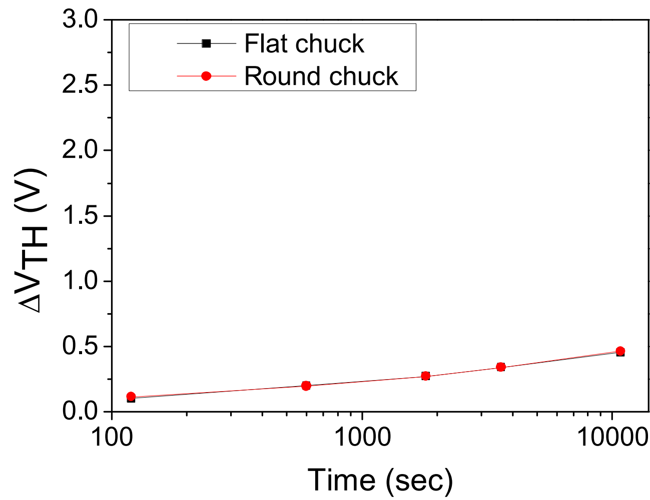
Figure 4-22 Shifts of transfer curves under NBTS (V_{GS} = -30 V, V_{DS} = 0.1 V) under 5 mm bending radius. (a) Bending direction is perpendicular to channel and (b) bending direction is parallel to channel.



(a)

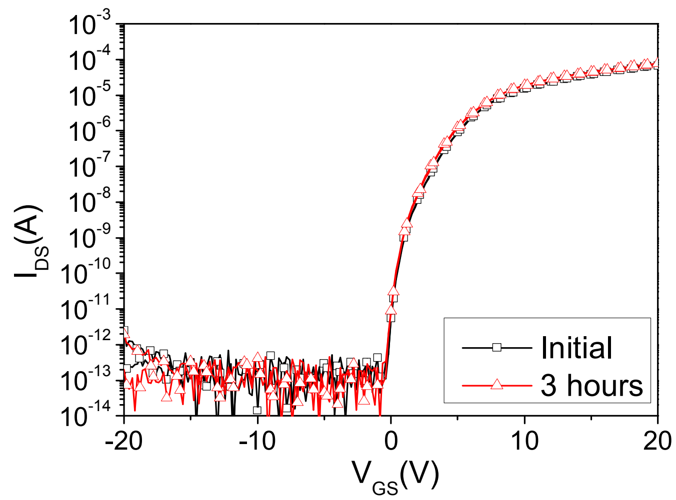


(b)

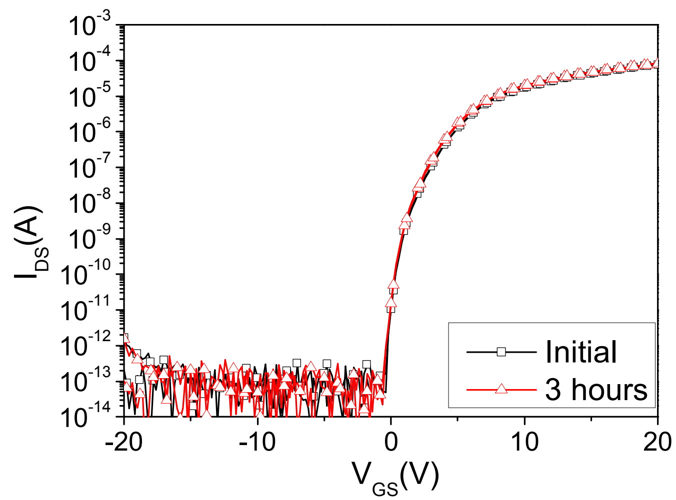


(c)

Figure 4-23 Shifts of transfer curves under PBTS (V_{GS} = 30 V, V_{DS} = 0.1 V) under (a) flat condition and (b) 5 mm bending radius. (c) Threshold voltage shift under PBTS as a function of time of flat condition and bending condition.



(a)



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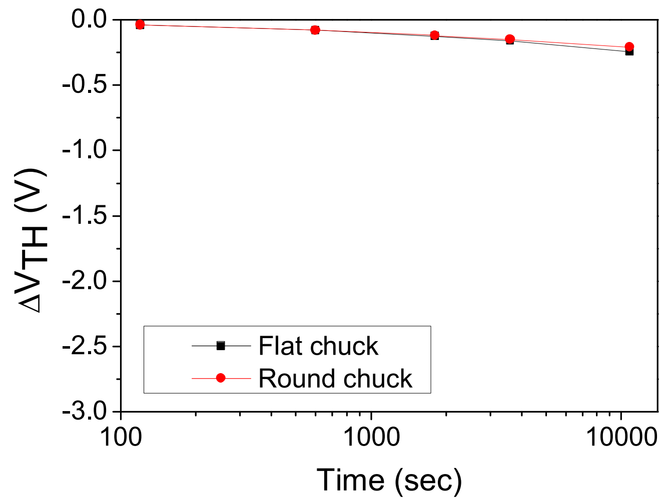
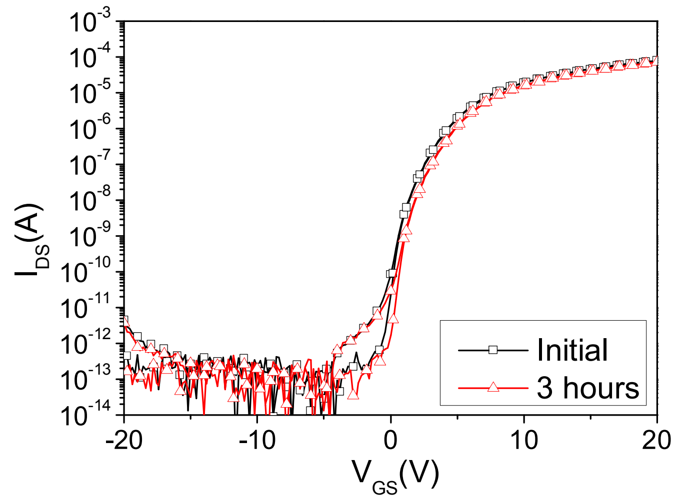
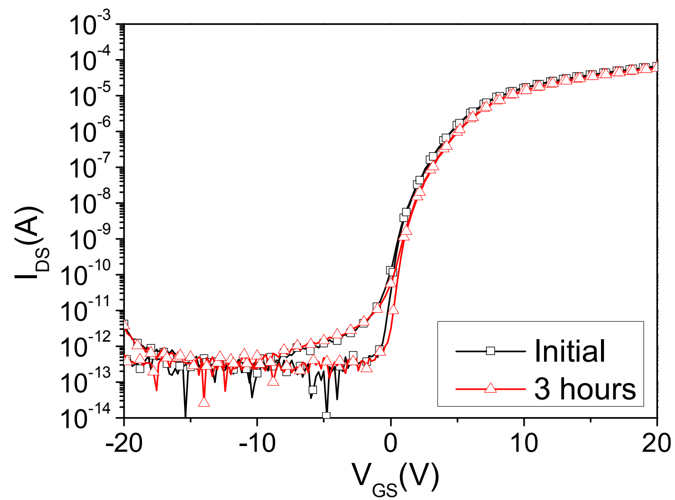


(c)

Figure 4-24 Shifts of transfer curves under NBTS (V_{GS} = -30 V, V_{DS} = 0.1 V) under (a) flat condition and (b) 5 mm bending radius. (c) Threshold voltage shift under NBTS as a function of time of flat condition and bending condition.



(a)



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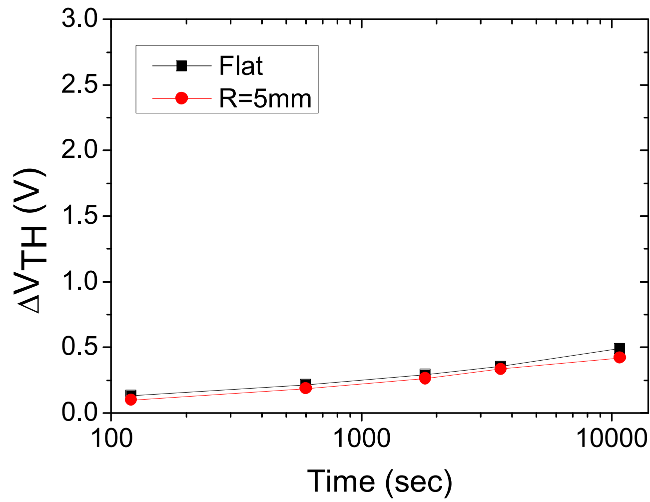
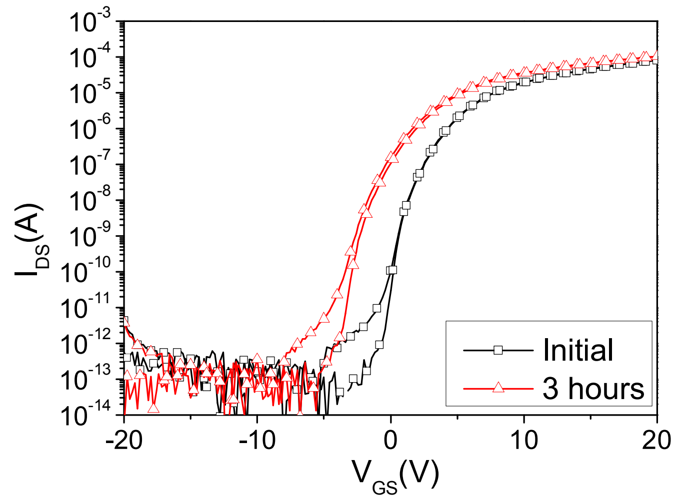
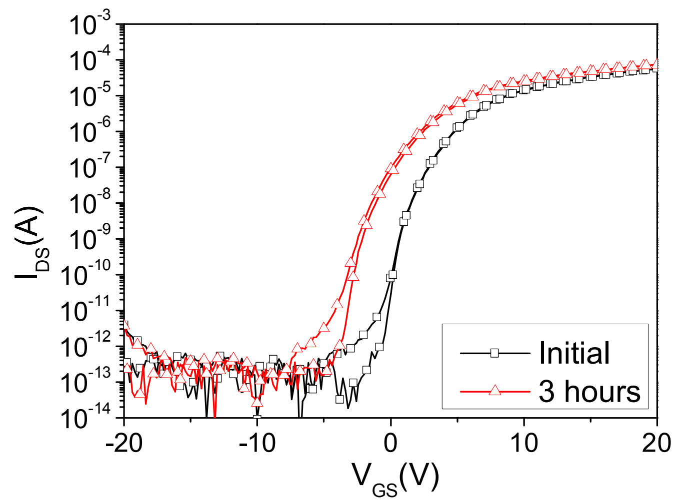


(c)

Figure 4-25 Shifts of transfer curves under PBITS (V_{GS} = 30 V, V_{DS} = 0.1 V, λ = 400nm, Intensity = 0.2 mW/cm^2) under (a) flat condition and (b) 5 mm bending radius. (c) Threshold voltage shift under PBITS as a function of time of flat condition and bending condition.



(a)



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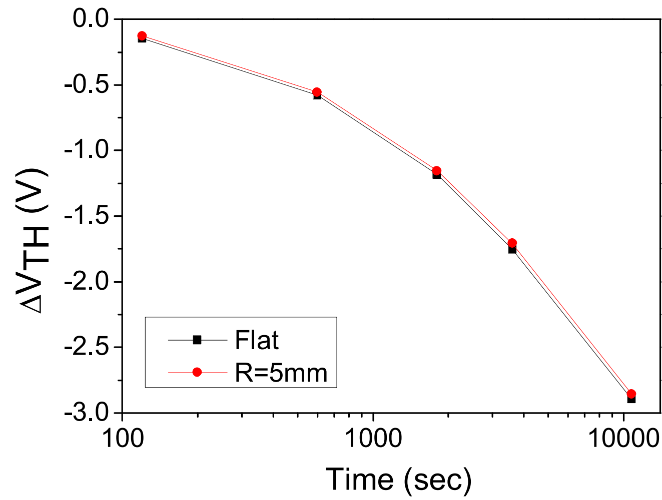

(c)

Figure 4-26 Shifts of transfer curves under NBITS (V_{GS} = -30 V, V_{DS} = 0.1 V, λ = 400nm, Intensity = 0.2 mW/cm^2) under (a) flat condition and (b) 5 mm bending radius. (c) Threshold voltage shift under NBITS as a function of time of flat condition and bending condition.

Chapter 5 Summary

In this study, the characteristics and reliability of flexible IGZO TFTs were investigated.

Firstly, the electrical characteristics and reliability of IGZO TFTs on glass substrate are discussed. The IGZO TFTs were fabricated on a glass substrate with an inverted staggered structure. The initial electrical characteristics and gate bias induced instability was investigated. And drain bias induced instability is investigated. Unique degradation phenomenon was observed under the high drain bias stress. After the high drain bias stress, the drain current, measured at the low drain bias, was significantly decreased. Based on the experimental results, I proposed a degradation model for the high drain bias induced degradation. And light-induced hysteresis of IGZO TFTs is investigated. Hysteresis was observed under the 450-nm illumination, and was increased with temperature. And hysteresis was increased with wavelength decrease. Light-induced hysteresis occurs due to increased sub-band gap states at the interface

between the gate insulator layer and the active layer. Also, bias illumination stress induced instability is investigated. The transfer curve did not change after positive bias illumination stress. However, the transfer curve shifted to a negative direction after negative bias illumination stress. The transfer curve could be shifted to the negative direction after negative bias illumination stress due to the increase of V_O^{2+} states.

Secondly, the electrical characteristics and reliability of IGZO TFTs on flexible substrate are discussed. The IGZO TFTs were fabricated on a polyimide (PI) substrate with an inverted staggered structure. An inorganic buffer layer, composed of SiO_2 and SiN_x multi-layer, was employed, in order to prevent the environmental stress, such as water or oxygen molecules. The effects of PI and inorganic buffer layer on the characteristics and reliability of IGZO TFTs were investigated. And the effects of passivation layer on the electrical stability of IGZO TFTs with single passivation layer and double passivation layer fabricated on PI substrate were investigated. The positive bias stress and negative bias stress were applied to the IGZO TFTs at various temperatures from 20 ^oC to 80 ^oC. The threshold voltage shift of double passivation device was larger than that of single passivation device under NBTS. The threshold voltage shift of double passivation device was slightly less than that of single passivation device under PBTS. The threshold voltage shift of NBTS is considerably increased than that of PBTS at high temperature due to the difference between conduction band offset and valence band offset. Lastly, the effects of mechanical bending on the electrical stability of flexible IGZO TFTs were investigated.

Bibliography

[1] T. SUNATA, T. YUKAWA, K. MIYAKE, Y. MATSUSHITA, Y. MURAKAMI, Y. UGAI, J. TAMAMURA and S. AOKI, "A large-area high-resolution active-matrix color LCD addressed by a-Si TFT's," Electron Devices, IEEE Transactions on, vol. 33, pp. 1212-1217, 1986.

[2] L. F. WEBER, "Measurement of wall charge and capacitance variation for a single cell in the AC plasma display panel," Electron Devices, IEEE Transactions on, vol. 24, pp. 864-869, 1977.

[3] A. Dodabalapur, "Organic light emitting diodes," Solid State Communications, vol. 102, pp. 259-267, 1997.

[4] W. B. Choi, D. S. Chung, J. H. Kang, H. Y. Kim, Y. W. Jin, I. T. Han, Y. H. Lee, J. E. Jung, N. S. Lee, G. S. Park, and J. M. Kim, "Fully sealed, high-brightness carbon-nanotube field-emission display," Applied Physics Letters, vol. 75, pp. 3129-3131, 1999.

[5] H. Meiling, J. Westendorp, J. Hautala, Z. Saleh and C. Malone, "Influence of the deposition rate of the a-Si: H channel on the field-effect mobility of TFTs deposited in a VHF glow discharge," in MATERIALS RESEARCH SOCIETY SYMPOSIUM PROCEEDINGS, 1994, pp. 65-65.

[6] C.-y. Chen and J. Kanicki, "High field-effect-mobility a-Si: H TFT based on high deposition-rate PECVD materials," Electron Device Letters, IEEE, vol. 17, pp. 437-439, 1996.

[7] K. SERA, F. OKUMURA, H. UCHIDA, S. ITOH, S. KANEKO and K. HOTTA, "High-performance TFTs fabricated by XeCl excimer laser annealing of

hydrogenated amorphous-silicon film," Electron Devices, IEEE Transactions on, vol. 36, pp. 2868-2872, 1989.

[8] K. Shimizu, O. Sugiura and M. Matsumura, "High-mobility poly-Si thin-film transistors fabricated by a novel excimer laser crystallization method," Electron Devices, IEEE Transactions on, vol. 40, pp. 112-117, 1993.

[9] T. Sameshima, S. Usui and M. Sekiya, "XeCl Excimer laser annealing used in the fabrication of poly-Si TFT's," Electron Device Letters, IEEE, vol. 7, pp. 276-278, 1986.

[10] H. J. Kim and J. S. Im, "New excimer-laser-crystallization method for producing large-grained and grain boundary-location-controlled Si films for thin film transistors," Applied Physics Letters, vol. 68, pp. 1513-1515, 1996.

[11] C. W. Tang and S. A. VanSlyke, "Organic electroluminescent diodes," Applied Physics Letters, vol. 51, pp. 913-915, 1987.

[12] T. Tohma, "Recent progress in development of organic electroluminescent display devices," in SID CONF REC INT DISPLAY RES CONF. pp. F 1-F 4. 1997, 1997.

[13] M. T. Bernius, M. Inbasekaran, J. O'Brien and W. Wu, "Progress with light-emitting polymers," Advanced Materials, vol. 12, pp. 1737-1750, 2000.

[14] M. Stewart, R. S. Howell, L. Pires, M. K. Hatalis, W. Howard and O. Prache, "Polysilicon VGA active matrix OLED displays-technology and performance," in Electron Devices Meeting, 1998. IEDM'98. Technical Digest., International, 1998, pp. 871-874.

[15] M. Stewart, R. S. Howell, L. Pires and M. K. Hatalis, "Polysilicon TFT technology for active matrix OLED displays," Electron Devices, IEEE Transactions on, vol. 48, pp. 845-851, 2001.

[16] T. Shimoda, M. Kimura, S. Seki, H. Kobayashi, S. Kanbe, S. Miyashita, R. Friend, J. Burroughes, C. Towns and I. Millard, "Technology for active matrix light emitting polymer displays," in Electron Devices Meeting, 1999. IEDM'99. Technical Digest. International, 1999, pp. 107-110.

[17] A. Nathan, G. R. Chaji and S. J. Ashtiani, "Driving schemes for a-Si and LTPS AMOLED displays," Display Technology, Journal of, vol. 1, pp. 267-277, 2005.

[18] J.-H. Lee, J.-H. Kim and M.-K. Han, "A new a-Si:H TFT pixel circuit compensating the threshold voltage shift of a-Si:H TFT and OLED for active matrix OLED," Electron Device Letters, IEEE, vol. 26, pp. 897-899, 2005.

[19] K. Shih-Chin, Z. Hsiao-Wen, H. Jung-Jie and K. Bo-Cheng, "Self-Heating Effect on Bias-Stressed Reliability for Low-Temperature a-Si:H TFT on Flexible Substrate," Electron Devices, IEEE Transactions on, vol. 57, pp. 588-593, 2010.

[20] Y. Juhn-Suk, J. Sang-Hoon, K. Yong-Chul, B. Seung-Chan, K. Jong-Moo, C. Nack-Bong, Y. Soo-Young, K. Chang-Dong, H. Yong-Kee and C. In-Jae, "Highly Flexible AM-OLED Display With Integrated Gate Driver Using Amorphous Silicon TFT on Ultrathin Metal Foil," Display Technology, Journal of, vol. 6, pp. 565-570, 2010.

[21] N. Young, I. French, M. Trainor, D. Murley, D. McCulloch and R. Wilks, "LTPS for AMLCD on glass and polymer substrates," in Proceedings of the sixth international display workshop, 1999, pp. 219-222.

[22] K. Nomura, H. Ohta, A. Takagi, T. Kamiya, M. Hirano and H. Hosono, "Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors," Nature, vol. 432, pp. 488-492, 2004.

[23] M. Kim, J. H. Jeong, H. J. Lee, T. K. Ahn, H. S. Shin, J.-S. Park, J. K. Jeong, Y.-G. Mo and H. D. Kim, "High mobility bottom gate InGaZnO thin film transistors with SiOx etch stopper," Applied Physics Letters, vol. 90, p. 212114, 2007.

[24] K. Nomura, A. Takagi, T. Kamiya, H. Ohta, M. Hirano and H. Hosono, "Amorphous oxide semiconductors for high-performance flexible thin-film transistors," Japanese Journal of Applied Physics, vol. 45, p. 4303, 2006.

[25] H. Yabuta, M. Sano, K. Abe, T. Aiba, T. Den, H. Kumomi, K. Nomura, T. Kamiya and H. Hosono, "High-mobility thin-film transistor with amorphous InGaZnO4 channel fabricated by room temperature rf-magnetron sputtering," Applied Physics Letters, vol. 89, p. 112123, 2006.

[26] J. K. Jeong, J. H. Jeong, H. W. Yang, J.-S. Park, Y.-G. Mo and H. D. Kim, "High performance thin film transistors with cosputtered amorphous indium gallium zinc oxide channel," Applied Physics Letters, vol. 91, p. 113505, 2007.

[27] J. Y. Kwon, K. S. Son, J. S. Jung, T. S. Kim, M. K. Ryu, K. B. Park, B. W. Yoo, J. W. Kim, Y. G. Lee, K. C. Park, S. Y. Lee, and J. M. Kim, "Bottom-Gate Gallium Indium Zinc Oxide Thin-Film Transistor Array for High-Resolution AMOLED Display," Electron Device Letters, IEEE, vol. 29, pp. 1309-1311, 2008.

[28] H. S. Shin, B. D. Ahn, K. H. Kim, J.-S. Park and H. J. Kim, "The effect of thermal annealing sequence on amorphous InGaZnO thin film transistor with a plasma-treated source–drain structure," Thin Solid Films, vol. 517, pp.

6349-6352, 2009.

[29] T. Kamiya, K. Nomura, M. Hirano and H. Hosono, "Electronic structure of oxygen deficient amorphous oxide semiconductor a-InGaZnO4−x: Optical analyses and first-principle calculations," physica status solidi (c), vol. 5, pp. 3098-3100, 2008.

[30] H. Seo, Y.-J. Cho, J. Kim, S. M.bobade, K.-Y. Park, J. Lee and D.-K. Choi, "Permanent optical doping of amorphous metal oxide semiconductors by deep ultraviolet irradiation at room temperature," Applied Physics Letters, vol. 96, p. 222101, 2010.

[31] A. Suresh and J. F. Muth, "Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors," Applied Physics Letters, vol. 92, p. 033502, 2008.

[32] J. Lee, J.-S. Park, Y. S. Pyo, D. B. Lee, E. H. Kim, D. Stryakhilev, T. W. Kim, D. U. Jin and Y.-G. Mo, "The influence of the gate dielectrics on threshold voltage instability in amorphous indium-gallium-zinc oxide thin film transistors," Applied Physics Letters, vol. 95, p. 123502, 2009.

[33] J.-M. Lee, I.-T. Cho, J.-H. Lee, W.-S. Cheong, C.-S. Hwang and H.-I. Kwon, "Comparative study of electrical instabilities in top-gate InGaZnO thin film transistors with Al2O3 and Al2O3/SiNx gate dielectrics," Applied Physics Letters, vol. 94, p. 222112, 2009.

[34] C.-T. Tsai, T.-C. Chang, S.-C. Chen, I. Lo, S.-W. Tsao, M.-C. Hung, J.-J. Chang, C.-Y. Wu and C.-Y. Huang, "Influence of positive bias stress on N2O plasma improved InGaZnO thin film transistor," Applied Physics Letters, vol. 96, p. 242105, 2010.

[35] Y.-K. Moon, S. Lee, W.-S. Kim, B.-W. Kang, C.-O. Jeong, D.-H. Lee and J.-W. Park, "Improvement in the bias stability of amorphous indium gallium zinc oxide thin-film transistors using an O2 plasma-treated insulator," Applied Physics Letters, vol. 95, p. 013507, 2009.

[36] F. R. Libsch and J. Kanicki, "Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors," Applied Physics Letters, vol. 62, pp. 1286-1288, 1993.

[37] M. J. Powell, C. v. Berkel and J. R. Hughes, "Time and temperature dependence of instability mechanisms in amorphous silicon thin-film transistors," Applied Physics Letters, vol. 54, pp. 1323-1325, 1989.

[38] W. B. Jackson, J. M. Marshall and M. D. Moyer, "Role of hydrogen in the formation of metastable defects in hydrogenated amorphous silicon," Physical Review B, vol. 39, p. 1164, 1989.

[39] M. J. Powell, C. v. Berkel, I. D. French and D. H. Nicholls, "Bias dependence of instability mechanisms in amorphous silicon thin-film transistors," Applied Physics Letters, vol. 51, pp. 1242-1244, 1987.

[40] K. Hoshino, D. Hong, H. Q. Chiang and J. F. Wager, "Constant-Voltage-Bias Stress Testing of a-IGZO Thin-Film Transistors," Electron Devices, IEEE Transactions on, vol. 56, pp. 1365-1370, 2009.

[41] M. Fujii, H. Yano, T. Hatayama, Y. Uraoka, T. Fuyuki, J. S. Jung and J. Y. Kwon, "Thermal Analysis of Degradation in Ga2O3–In2O3–ZnO Thin-Film Transistors," Japanese Journal of Applied Physics, vol. 47, pp. 6236-6240, 2008.

[42] C. In-Tak and et al., "Charge trapping and detrapping characteristics in amorphous InGaZnO TFTs under static and dynamic stresses," Semiconductor Science and Technology, vol. 24, p. 015013, 2009.

[43] J.-M. Lee, I.-T. Cho, J.-H. Lee and H.-I. Kwon, "Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors," Applied Physics Letters, vol. 93, p. 093504, 2008.

[44] K. Nomura, T. Kamiya, M. Hirano and H. Hosono, "Origins of threshold voltage shifts in room-temperature deposited and annealed a-In–Ga–Zn–O thin-film transistors," Applied Physics Letters, vol. 95, p. 013502, 2009.

[45] K. Nomura, T. Kamiya, Y. Kikuchi, M. Hirano and H. Hosono, "Comprehensive studies on the stabilities of a-In-Ga-Zn-O based thin film transistor by constant current stress," Thin Solid Films, vol. 518, pp. 3012-3016, 2010.

[46] M. D. H. Chowdhury, P. Migliorato and J. Jang, "Time-temperature dependence of positive gate bias stress and recovery in amorphous indium-gallium-zinc-oxide thin-film-transistors," Applied Physics Letters, vol. 98, p. 153511, 2011.

[47] M. Kimura, T. Nakanishi, K. Nomura, T. Kamiya and H. Hosono, "Trap densities in amorphous-InGaZnO4 thin-film transistors," Applied Physics Letters, vol. 92, p. 133512, 2008.

[48] M. E. Lopes, H. L. Gomes, M. C. R. Medeiros, P. Barquinha, L. Pereira, E. Fortunato, R. Martins and I. Ferreira, "Gate-bias stress in amorphous oxide semiconductors thin-film transistors," Applied Physics Letters, vol. 95, p. 063502, 2009.

[49] C. Geng-Wei, C. Ting-Chang, J. Jhe-Ciou, T. Tsung-Ming, S. Yong-En, C. Kuan-Chang, T. Ya-Hsiang, J. Fu-Yen and H. Ya-Chi, "Abnormal Subthreshold Leakage Current at High Temperature in InGaZnO Thin-Film Transistors," Electron Device Letters, IEEE, vol. 33, pp. 540-542, 2012.

[50] T.-C. Chen, T.-C. Chang, C.-T. Tsai, T.-Y. Hsieh, S.-C. Chen, C.-S. Lin, M.-C. Hung, C.-H. Tu, J.-J. Chang and P.-L. Chen, "Behaviors of InGaZnO thin film transistor under illuminated positive gate-bias stress," Applied Physics Letters, vol. 97, p. 112104, 2010.

[51] K.-H. Lee, J. S. Jung, K. S. Son, J. S. Park, T. S. Kim, R. Choi, J. K. Jeong, J.-Y. Kwon, B. Koo and S. Lee, "The effect of moisture on the photon-enhanced negative bias thermal instability in Ga–In–Zn–O thin film transistors," Applied Physics Letters, vol. 95, p. 232106, 2009.

[52] J.-H. Shin, J.-S. Lee, C.-S. Hwang, S.-H. K. Park, W.-S. Cheong, M. Ryu, C.-W. Byun, J.-I. Lee and H. Y. Chu, "Light Effects on the Bias Stability of Transparent ZnO Thin Film Transistors " ETRI Journal, vol. 31, p. 62, 2009.

[53] K. Ghaffarzadeh, A. Nathan, J. Robertson, S. Kim, S. Jeon, C. Kim, U.-I. Chung and J.-H. Lee, "Instability in threshold voltage and subthreshold behavior in Hf--In--Zn--O thin film transistors induced by bias-and light-stress," Applied Physics Letters, vol. 97, p. 113504, 2010.

[54] J. S. Jung, K. S. Son, K.-H. Lee, J. S. Park, T. S. Kim, J.-Y. Kwon, K.-B. Chung, J.-S. Park, B. Koo and S. Lee, "The impact of SiN[sub x] gate insulators on amorphous indium-gallium-zinc oxide thin film transistors under bias-temperature-illumination stress," Applied Physics Letters, vol. 96, p. 193506, 2010.

[55] D. W. Kwon, J. H. Kim, J. S. Chang, S. W. Kim, M.-C. Sun, G. Kim, H. W. Kim, J. C. Park, I. Song, C. J. Kim, U. I. Jung, and B.-G. Park, "Charge injection from gate electrode by simultaneous stress of optical and electrical biases in HfInZnO amorphous oxide thin film transistor," Applied Physics Letters, vol. 97, p. 193504, 2010.

[56] J.-Y. Kwon, J. S. Jung, K. S. Son, K.-H. Lee, J. S. Park, T. S. Kim, J.-S. Park, R. Choi, J. K. Jeong, B. Koo, and S. Y. Lee, "The impact of gate dielectric materials on the light-induced bias instability in Hf–In–Zn–O thin film transistor," Applied Physics Letters, vol. 97, p. 183503, 2010.

[57] H. Oh, S.-M. Yoon, M. K. Ryu, C.-S. Hwang, S. Yang and S.-H. K. Park, "Photon-accelerated negative bias instability involving subgap states creation in amorphous In–Ga–Zn–O thin film transistor," Applied Physics Letters, vol. 97, p. 183502, 2010.

[58] J. S. Park, T. S. Kim, K. S. Son, K.-H. Lee, W.-J. Maeng, H.-S. Kim, E. S. Kim, K.-B. Park, J.-B. Seon, W. Choi, M. K. Ryu, and S. Y. Lee, "The influence of SiO[sub x] and SiN[sub x] passivation on the negative bias stability of Hf–In–Zn–O thin film transistors under illumination," Applied Physics Letters, vol. 96, p. 262109, 2010.

[59] B. Ryu, H.-K. Noh, E.-A. Choi and K. J. Chang, "O-vacancy as the origin of negative bias illumination stress instability in amorphous In–Ga–Zn–O thin film transistors," Applied Physics Letters, vol. 97, p. 022108, 2010.

[60] S. Yang, D.-H. Cho, M. K. Ryu, S.-H. K. Park, C.-S. Hwang, J. Jang and J. K. Jeong, "Improvement in the photon-induced bias stability of Al–Sn–Zn–In–O thin film transistors by adopting AlO[sub x] passivation layer," Applied Physics

Letters, vol. 96, p. 213511, 2010.

[61] K. H. Ji, J.-I. Kim, H. Y. Jung, S. Y. Park, R. Choi, Y. G. Mo and J. K. Jeong, "Comprehensive studies of the degradation mechanism in amorphous InGaZnO transistors by the negative bias illumination stress," Microelectronic Engineering, vol. 88, pp. 1412-1416, 2011.

[62] B. Kim, E. Chong, D. Hyung Kim, Y. Woo Jeon, D. Hwan Kim and S. Yeol Lee, "Origin of threshold voltage shift by interfacial trap density in amorphous InGaZnO thin film transistor under temperature induced stress," Applied Physics Letters, vol. 99, p. 062108, 2011.

[63] J. H. Kim, U. K. Kim, Y. J. Chung, J. S. Jung, S. H. Ra, H. S. Jung, C. S. Hwang, J. K. Jeong and S. Y. Lee, "The effects of device geometry on the negative bias temperature instability of Hf-In-Zn-O thin film transistors under light illumination," Applied Physics Letters, vol. 98, p. 023507, 2011.

[64] S. Kim, S. Kim, C. Kim, J. Park, I. Song, S. Jeon, S.-E. Ahn, J.-S. Park and J. K. Jeong, "The influence of visible light on the gate bias instability of In–Ga–Zn–O thin film transistors," Solid-State Electronics, vol. 62, pp. 77-81, 2011.

[65] K. Nomura, T. Kamiya and H. Hosono, "Highly stable amorphous In-Ga-Zn-O thin-film transistors produced by eliminating deep subgap defects," Applied Physics Letters, vol. 99, p. 053505, 2011.

[66] H. Oh, S.-M. Yoon, M. K. Ryu, C.-S. Hwang, S. Yang and S.-H. K. Park, "Transition of dominant instability mechanism depending on negative gate bias under illumination in amorphous In-Ga-Zn-O thin film transistor," Applied Physics Letters, vol. 98, p. 033504, 2011.

[67] S. Yang, K. Hwan Ji, U. Ki Kim, C. Seong Hwang, S.-H. Ko Park, C.-S. Hwang, J. Jang and J. Kyeong Jeong, "Suppression in the negative bias illumination instability of Zn-Sn-O transistor using oxygen plasma treatment," Applied Physics Letters, vol. 99, p. 102103, 2011.

[68] S. Y. Lee, S. J. Kim, Y. W. Lee, W. G. Lee, K. S. Yoon, J. Y. Kwon and M. K. Han, "The Effect of the Photo-Induced Carriers on the Reliability of Oxide TFTs Under Various Intensities of Light," Electron Device Letters, IEEE, vol. 33, pp. 218-220, 2012.

[69] T. Y. Luo, M. Laughery, G. A. Brown, H. N. Al-Shareef, V. H. C. Watt, A. Karamcheti, M. D. Jackson and H. R. Huff, "Effect of H2 content on reliability of ultrathin in-situ steam generated (ISSG) SiO2," Electron Device Letters, IEEE, vol. 21, pp. 430-432, 2000.

[70] D. Kang, H. Lim, C. Kim, I. Song, J. Park, Y. Park and J. Chung, "Amorphous gallium indium zinc oxide thin film transistors: Sensitive to oxygen molecules," Applied Physics Letters, vol. 90, p. 192101, 2007.

[71] J. K. Jeong, H. Won Yang, J. H. Jeong, Y.-G. Mo and H. D. Kim, "Origin of threshold voltage instability in indium-gallium-zinc oxide thin film transistors," Applied Physics Letters, vol. 93, p. 123508, 2008.

[72] D. H. Levy, D. Freeman, S. F. Nelson, P. J. Cowdery-Corvan and L. M. Irving, "Stable ZnO thin film transistors by fast open air atomic layer deposition," Applied Physics Letters, vol. 92, p. 192101, 2008.

[73] J.-S. Park, J. K. Jeong, H.-J. Chung, Y.-G. Mo and H. D. Kim, "Electronic transport properties of amorphous indium-gallium-zinc oxide semiconductor upon exposure to water," Applied Physics Letters, vol. 92, p.

072104, 2008.

[74] P.-T. Liu, Y.-T. Chou and L.-F. Teng, "Environment-dependent metastability of passivation-free indium zinc oxide thin film transistor after gate bias stress," Applied Physics Letters, vol. 95, p. 233504, 2009.

[75] S.-Y. Sung, J. H. Choi, U. B. Han, K. C. Lee, J.-H. Lee, J.-J. Kim, W. Lim, S. J. Pearton, D. P. Norton and Y.-W. Heo, "Effects of ambient atmosphere on the transfer characteristics and gate-bias stress stability of amorphous indium-gallium-zinc oxide thin-film transistors," Applied Physics Letters, vol. 96, p. 102107, 2010.

[76] W.-F. Chung, T.-C. Chang, H.-W. Li, C.-W. Chen, Y.-C. Chen, S.-C. Chen, T.-Y. Tseng and Y.-H. Tai, "Influence of H2O Dipole on Subthreshold Swing of Amorphous Indium-Gallium-Zinc-Oxide Thin Film Transistors," Electrochemical and Solid-State Letters, vol. 14, pp. H114-H116, 2011.

[77] C.-S. Fuh, S. M. Sze, P.-T. Liu, L.-F. Teng and Y.-T. Chou, "Role of environmental and annealing conditions on the passivation-free in-Ga–Zn–O TFT," Thin Solid Films, vol. 520, pp. 1489-1494, 2011.

[78] S.-Y. Huang, T.-C. Chang, M.-C. Chen, S.-C. Chen, C.-T. Tsai, M.-C. Hung, C.-H. Tu, C.-H. Chen, J.-J. Chang and W.-L. Liau, "Effects of Ambient Atmosphere on Electrical Characteristics of Al2O3 Passivated InGaZnO Thin Film Transistors during Positive-Bias-Temperature-Stress Operation," Electrochemical and Solid-State Letters, vol. 14, pp. H177-H179, 2011.

[79] D. L. Staebler and C. R. Wronski, "Optically induced conductivity changes in discharge-produced hydrogenated amorphous silicon," Journal of Applied Physics, vol. 51, pp. 3262-3268, 1980.

[80] M. Stutzmann, W. B. Jackson and C. C. Tsai, "Light-induced metastable defects in hydrogenated amorphous silicon: A systematic study," Physical Review B, vol. 32, pp. 23-47, 1985.

[81] S.-H. Choi and M.-K. Han, "Effect of Deposition Temperature of SiOx Passivation Layer on the Electrical Performance of a-IGZO TFTs," Electron Device Letters, IEEE, vol. 33, pp. 396-398, 2012.

[82] S.-H. Choi, J.-H. Jang, J.-J. Kim and M.-K. Han, "Low-Temperature Organic (CYTOP) Passivation for Improvement of Electric Characteristics and Reliability in IGZO TFTs," Electron Device Letters, IEEE, vol. 33, pp. 381-383, 2012.

[83] W. B. Jackson, R. Hoffman, B. Yeh, T. Emery, T. Koch, C. McConica and O. Kwon, "Metastability in multicomponent oxide transistors," physica status solidi (a), vol. 207, pp. 695-699, 2010.

[84] J. S. Jung, K.-H. Lee, K. S. Son, J. S. Park, T. S. Kim, J. H. Seo, J.-H. Jeon, M.-P. Hong, J.-Y. Kwon, B. Koo, and S. Lee, "The Effect of Passivation Layers on the Negative Bias Instability of Ga-In-Zn-O Thin Film Transistors under Illumination," Electrochemical and Solid-State Letters, vol. 13, pp. H376-H378, 2010.

[85] S.-I. Kim, S. W. Kim, C. J. Kim and J.-S. Park, "The Impact of Passivation Layers on the Negative Bias Temperature Illumination Instability of Ha-In-Zn-O TFT," Journal of The Electrochemical Society, vol. 158, pp. H115-H118, 2011.

[86] J. S. Park, T. S. Kim, K. S. Son, K.-H. Lee, W.-J. Maeng, H.-S. Kim, E. S. Kim, K.-B. Park, J.-B. Seon, W. Choi, M. K. Ryu, and S. Y. Lee, "The influence of SiOx and SiNx passivation on the negative bias stability of Hf--In--Zn--O thin film

transistors under illumination," Applied Physics Letters, vol. 96, p. 262109, 2010.

[87] L. Shou-En, Y. Ming-Jiue, L. Chang-Yu, H. Geng-Tai, C. Chun-Cheng, L. Chih-Ming, L. Chrong-Jung, K. Ya-Chin and Y. Yung-Hui, "Influence of Passivation Layers on Characteristics of a-InGaZnO Thin-Film Transistors," Electron Device Letters, IEEE, vol. 32, pp. 161-163, 2011.

[88] B. Hekmatshoar, A. Z. Kattamis, K. H. Cherenack, L. Ke, C. Jian-Zhang, S. Wagner, J. C. Sturm, K. Rajan and M. Hack, "Reliability of Active-Matrix Organic Light-Emitting-Diode Arrays With Amorphous Silicon Thin-Film Transistor Backplanes on Clear Plastic," Electron Device Letters, IEEE, vol. 29, pp. 63-66, 2008.

[89] G. Fortunato, A. Pecora, L. Maiolo, M. Cuscuna, D. Simeone, A. Minotti and L. Mariucci, "Excimer Laser Annealing for Low-Temperature Polysilicon Thin Film Transistor Fabrication on Plastic Substrates," in Advanced Thermal Processing of Semiconductors, 2007. RTP 2007. 15th International Conference on, 2007, pp. 301-305.

[90] J.-S. Park, T.-W. Kim, D. Stryakhilev, J.-S. Lee, S.-G. An, Y.-S. Pyo, D.-B. Lee, Y. G. Mo, D.-U. Jin and H. K. Chung, "Flexible full color organic light-emitting diode display on polyimide plastic substrate driven by amorphous indium gallium zinc oxide thin-film transistors," Applied Physics Letters, vol. 95, p. 013503, 2009.

[91] N. Munzenrieder, K. H. Cherenack and G. Troster, "The Effects of Mechanical Bending and Illumination on the Performance of Flexible IGZO TFTs," Electron Devices, IEEE Transactions on, vol. 58, pp. 2041-2048, 2011.

[92] S. Yang, J. Y. Bak, S.-M. Yoon, M. K. Ryu, H. Oh, C.-S. Hwang, G. H. Kim, S.-H. K. Park and J. Jang, "Low-Temperature Processed Flexible In-Ga-Zn-O Thin-Film Transistors Exhibiting High Electrical Performance," Electron Device Letters, IEEE, vol. 32, pp. 1692-1694, 2011.

[93] G. Fortunato, A. Pecora and L. Maiolo, "Polysilicon thin-film transistors on polymer substrates," Materials Science in Semiconductor Processing, 2012.

[94] N. D. Young, M. J. Trainor, S. Y. Yoon, D. J. McCulloch, R. W. Wilks, A. Pearson, S. Godfrey, P. W. Green, S. Roosendaal and E. Hallworth, "Low Temperature Poly-Si on Flexible Polymer Substrates for Active Matrix Displays and Other Applications," in Materials Research Society Symposium - Proceedings, 2003, pp. 17-28.

[95] S. H. Won, J. K. Chung, C. B. Lee, H. C. Nam, J. H. Hur and J. Jang, "Effect of Mechanical and Electrical Stresses on the Performance of an a-Si:H TFT on Plastic Substrate," Journal of The Electrochemical Society, vol. 151, pp. G167-G170, 2004.

[96] F. Templier, B. Aventurier, P. Demars, J.-L. Botrel and P. Martin, "Fabrication of high performance low temperature poly-silicon backplanes on metal foil for flexible active-matrix organic light emission diode displays," Thin Solid Films, vol. 515, pp. 7428-7432, 2007.

[97] A. Jong-Hyun, K. Hoon-Sik, L. Keon Jae, Z. Zhengtao, E. Menard, R. G. Nuzzo and J. A. Rogers, "High-speed mechanically flexible single-crystal silicon thin-film transistors on plastic substrates," Electron Device Letters, IEEE, vol. 27, pp. 460-462, 2006.

[98] S. D. Theiss and S. Wagner, "Amorphous silicon thin-film transistors on steel

foil substrates," Electron Device Letters, IEEE, vol. 17, pp. 578-580, 1996.

[99] S. Maikap, C. Y. Yu, S. R. Jan, M. H. Lee and C. W. Liu, "Mechanically strained strained-Si NMOSFETs," Electron Device Letters, IEEE, vol. 25, pp. 40-42, 2004.

[100] Y. J. Yang, W. S. Ho, C. F. Huang, S. T. Chang and C. W. Liu, "Electron mobility enhancement in strained-germanium n-channel metal-oxide-semiconductor field-effect transistors," Applied Physics Letters, vol. 91, p. 102103, 2007.

[101] T. Afentakis, M. Hatalis, A. T. Voutsas and J. Hartzell, "Design and fabrication of high-performance polycrystalline silicon thin-film transistor circuits on flexible steel foils," Electron Devices, IEEE Transactions on, vol. 53, pp. 815-822, 2006.

[102] P.-C. Kuo, A. Jamshidi-Roudbari and M. Hatalis, "Effect of mechanical strain on mobility of polycrystalline silicon thin-film transistors fabricated on stainless steel foil," Applied Physics Letters, vol. 91, p. 243507, 2007.

[103] I.-H. Peng, P.-T. Liu and T.-B. Wu, "Effect of bias stress on mechanically strained low temperature polycrystalline silicon thin film transistor on stainless steel substrate," Applied Physics Letters, vol. 95, p. 041909, 2009.

[104] S. Nai-Chao, W. Shui-Jinn, H. Chin-Chuan, C. Yu-Han, H. Hao-Yuan, C. Chen-Kuo and A. Chin, "Low-Voltage-Driven Flexible InGaZnO Thin-Film Transistor With Small Subthreshold Swing," Electron Device Letters, IEEE, vol. 31, pp. 680-682, 2010.

[105] M. J. Gadre and T. L. Alford, "Highest transmittance and high-mobility amorphous indium gallium zinc oxide films on flexible substrate by room-

temperature deposition and post-deposition anneals," Applied Physics Letters, vol. 99, p. 051901, 2011.

[106] D. H. Lee, K. Nomura, T. Kamiya and H. Hosono, "Diffusion-Limited a-IGZO/Pt Schottky Junction Fabricated at 200 ◦C on a Flexible Substrate," Electron Device Letters, IEEE, vol. 32, pp. 1695-1697, 2011.

[107] E. Fortunato, P. Barquinha and R. Martins, "Oxide Semiconductor Thin-Film Transistors: A Review of Recent Advances," Advanced Materials, vol. 24, pp. 2945-2986, 2012.

[108] S. Lee, S. Park, S. Kim, Y. Jeon, K. Jeon, J.-H. Park, J. Park, I. Song, C. J. Kim, Y. Park, D. M. Kim, and D. H. Kim, "Extraction of Subgap Density of States in Amorphous InGaZnO Thin-Film Transistors by Using Multifrequency Capacitance-Voltage Characteristics," Electron Device Letters, IEEE, vol. 31, pp. 231-233, 2010.

[109] W. J. Lee, B. Ryu and K. J. Chang, "Electronic structure of oxygen vacancy in crystalline InGaO3(ZnO)m," Physica B: Condensed Matter, vol. 404, pp. 4794-4796, 2009.

[110] K. Nomura, T. Kamiya, H. Yanagi, E. Ikenaga, K. Yang, K. Kobayashi, M. Hirano and H. Hosono, "Subgap states in transparent amorphous oxide semiconductor, In–Ga–Zn–O, observed by bulk sensitive x-ray photoelectron spectroscopy," Applied Physics Letters, vol. 92, p. 202117, 2008.

[111] T. Y. Hsieh, T. C. Chang, T. C. Chen, M. Y. Tsai, Y. T. Chen, F. Y. Jian, Y. C. Chung, H. C. Ting and C. Y. Chen, "Investigating the Drain-Bias-Induced Degradation Behavior Under Light Illumination for InGaZnO Thin-Film Transistors," Electron Device Letters, IEEE, vol. 33, pp. 1000-1002, 2012.

[112] B. Kim, C.-I. Ryoo, S.-J. Kim, J.-U. Bae, H.-S. Seo, C.-D. Kim and M.-K. Han, "New Depletion-Mode IGZO TFT Shift Register," Electron Device Letters, IEEE, vol. 32, pp. 158-160, 2011.

[113] S.-H. K. Park, C.-S. Hwang, M. Ryu, S. Yang, C. Byun, J. Shin, J.-I. Lee, K. Lee, M. S. Oh and S. Im, "Transparent and Photo-stable ZnO Thin-film Transistors to Drive an Active Matrix Organic-Light- Emitting-Diode Display Panel," Advanced Materials, vol. 21, pp. 678-682, 2009.

[114] S.-H. Kuk, S.-Y. Lee, S.-J. Kim, B. Kim, S.-J. Park, J.-Y. Kwon and M.-K. Han, "Light-Induced Hysteresis of In-Ga-Zn-O Thin-Film Transistors With Various Temperatures," Electron Device Letters, IEEE, vol. 33, pp. 1279-1281, 2012.

[115] J.-S. Park, J. K. Jeong, Y.-G. Mo, H. D. Kim and C.-J. Kim, "Control of threshold voltage in ZnO-based oxide thin film transistors," Applied Physics Letters, vol. 93, p. 033513, 2008.

[116] G. Zaccanti and P. Bruscaglioni, "Deviation from the Lambert-Beer Law in the Transmittance of a Light Beam Through Diffusing Media: Experimental Results," Journal of Modern Optics, vol. 35, pp. 229-242, 1988.

[117] A. Janotti and C. G. V. d. Walle, "Oxygen vacancies in ZnO," Applied Physics Letters, vol. 87, p. 122102, 2005.

[118] S.-J. Kim, S.-Y. Lee, Y. W. Lee, S.-H. Kuk, J.-Y. Kwon and M.-K. Han, "Effect of Charge Trapping/Detrapping on Threshold Voltage Shift of IGZO TFTs under AC Bias Stress," Electrochemical and Solid-State Letters, vol. 15, pp. H108-H110, 2012.

[119] J. H. Kim, U. K. Kim, Y. J. Chung and C. S. Hwang, "Correlation of the change

in transfer characteristics with the interfacial trap densities of amorphous In–Ga–Zn–O thin film transistors under light illumination," Applied Physics Letters, vol. 98, p. 232102, 2011.

[120] A. Janotti and C. G. Van de Walle, "Native point defects in ZnO," Physical Review B, vol. 76, p. 165202, 2007.

[121] S. J. Clark, J. Robertson, S. Lany and A. Zunger, "Intrinsic defects in ZnO calculated by screened exchange and hybrid density functionals," Physical Review B, vol. 81, p. 115311, 2010.

[122] C. G. Van de Walle, "Hydrogen as a Cause of Doping in Zinc Oxide," Physical Review Letters, vol. 85, pp. 1012-1015, 2000.

[123] S. Kohiki, M. Nishitani, T. Wada and T. Hirao, "Enhanced conductivity of zinc oxide thin films by ion implantation of hydrogen atoms," Applied Physics Letters, vol. 64, pp. 2876-2878, 1994.

[124] Y.-B. Park and S.-W. Rhee, "Effect of hydrogen plasma precleaning on the removal of interfacial amorphous layer in the chemical vapor deposition of microcrystalline silicon films on silicon oxide surface," Applied Physics Letters, vol. 68, pp. 2219-2221, 1996.

초 록

최근, 차세대 디스플레이 후보로서 플렉시블 디스플레이가 각광을 받고 있다. 플리스틱과 같은 플렉시블 기판은 유리 기판에 비해서 유연하고, 깨지지 않으며, 무게가 가볍고, 가격이 저렴한 장점이 있다. 인듐−갈륨−아연−산화물 박막 트랜지스터는 이동도가 높고 균일성이 우수하며, 공정 온도가 낮아 차세대 플렉시블 디스플레이 백플레인으로서 관심이 집중되고 있다.

본 학위 논문에서는 플렉시블 디스플레이의 실제 적용을 위해 플라스틱 기판에 제작한 인듐−갈륨−아연−산화물 박막 트랜지스터의 특성과 신뢰성에 대해 연구하였다.

인듐−갈륨−아연−산화물 박막 트랜지스터를 플라스틱 기판에 적용하기 전에 먼저 유리 기판에 제작한 인듐−갈륨−아연−산화물 박막 트랜지스터의 전기적 특성과 신뢰성에 대해 연구하였다. 인듐−갈륨−아연−산화물 박막 트랜지스터는 유리 기판에 역 스태거드 (inverted staggered) 구조로 제작하였다. 제작한 소자의 초기 특성과 게이트 전압, 드레인 전압에 의한 신뢰성에 대해 연구하였다. 높은 드레인 전압이 인가될 때에는 특이한 열화 현상을 보였다. 높은 드레인 전압에 의한 열화가 일어난 후에는, 낮은 드레인 전압 측정 영역에서 드레인 전류가 크게 감소하였다. 위 실험 결과에 근거하여 높은 드레인 전압에 의한 열화 모델을 세우고 검증하였다. 그리고 인듐−갈륨−아연−산화물 박막 트랜지스터의 빛에 의한 이력 현상 (hysteresis)에 대해 연구하였다. 이력 현상은 450−nm 이하 파장 영역에서 관찰 되었으며, 온도가 증가할수록, 조사하는 빛의 파장이 짧아질수록 이력 현상이 증가하였다. 이와 같은

빛에 의한 이력 현상은 게이트 절연막과 활성화 층 사이의 계면에서 밴드갭 이하의 상태 생성에 기인한다. 빛과 전압이 같이 인가 될 때의 신뢰성에 대해서도 연구를 진행하였다. 양의 전압이 인가될 때에는 빛의 유무에 상관없이 열화 정도가 유사하였다. 반면, 음의 전압이 인가될 때에는 빛이 조사될 경우 문턱전압이 음의 방향으로 크게 이동하였다. 이는 지속된 음의 전압과 빛에 의해 계면에서 V_O^{2+} 상태가 증가하였기 때문이다.

두 번째로, 플라스틱 기판에 제작한 인듐-갈륨-아연-산화물 박막 트랜지스터의 전기적 특성과 신뢰성에 대해 연구하였다. 인듐-갈륨-아연-산화물 박막 트랜지스터는 폴리이미드 (Polyimide) 기판에 역 스태거드 구조로 제작하였다. SiO_2 와 SiN_x 의 다층 구조로 이루어진 완충층 (buffer layer)을 폴리이미드와 게이트 금속 사이에 적용하여 수분이나 산소와 같은 주변 대기 효과를 최소화 하였다. 먼저, 추가로 적용한 폴리이미드와 완충층이 인듐-갈륨-아연-산화물 박막 트랜지스터의 특성과 신뢰성에 끼치는 영향성에 대해 분석하였다. 그 이후, 보호막이 인듐-갈륨-아연-산화물 박막 트랜지스터의 특성과 신뢰성에 끼치는 영향성에 대해 분석하였다. 마지막으로 물리적인 구부림이 플라스틱 기판에 제작한 인듐-갈륨-아연-산화물 박막 트랜지스터의 특성과 신뢰성에 끼치는 영향성에 대해 분석하였다.

주요어: 박막 트랜지스터, 인듐-갈륨-아연-산화물, 플렉시블 디스플레이, 신뢰성

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