Ph.D. Dissertation

A Design of Calibration-Free Phase-Locked Loops (PLLs)

캘리브레이션이 필요 없는 위상고정루프의 설계

by

Hwanseok Yeo

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School of Electrical Engineering and Computer Science
College of Engineering
Seoul National University

A Design of Calibration-Free Phase-Locked Loops (PLLs)

지도 교수 김 재 하

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위 원 장	정 덕 균	(인)
부위원장	김 재 하	(인)
위 원	남 상 욱	(인)
위 원	박 병 하	(인)
위 원	김 태 익	(인)

Abstract

A PVT-insensitive-bandwidth PLL and a chirp frequency synthesizer PLL are proposed using a constant-relative-gain digitally-controlled oscillator (DCO), a constant-gain time-to-digital converter (TDC), and a simple digital loop filter (DLF) without an explicit calibration or additional circuit components.

A digital LC-PLL that realizes a PVT-insensitive loop bandwidth (BW) by using the constant-relative-gain LC-DCO and constant-gain TDC is proposed. In other words, based on ratiometric circuit designs, the LC-DCO can make a fixed percent change to its frequency for a unit change in its digital input and the TDC can maintain a fixed range and resolution measured in reference unit intervals (UIs) across PVT variations. With such LC-DCO and TDC, the proposed PLL can realize a bandwidth which is a constant fraction of the reference frequency even with a simple proportional-integral digital loop filter without any explicit calibration loops. The prototype digital LC-PLL fabricated in a 28-nm CMOS demonstrates a frequency range of 8.38~9.34 GHz and 652-fs_{rms} integrated jitter from 10-kHz to 1-GHz at 8.84-GHz while dissipating 15.2-mW and occupying 0.24-mm^2. Also, the PLL across three different die samples and supply voltage ranging from 1.0 to 1.2V demonstrates a nearly constant BW at 822-kHz with the variation of ±4.25-% only.

A chirp frequency synthesizer PLL (FS-PLL) that is capable of precise triangular frequency modulation using type-III digital LC-PLL architecture for X-band FMCW imaging radar is proposed. By employing a phase-modulating two-point modulation (TPM), constant-gain TDC, and a simple second-order DLF with polarity-

alternating frequency ramp estimator, the PLL achieves a gain self-tracking TPM realizing a frequency chirp with fast chirp slope (=chirp BW/chirp period) without increasing frequency errors around the turn-around points, degrading the effective resolution achievable. A prototype chirp FS-PLL fabricated in a 65nm CMOS demonstrates that the PLL can generate a precise triangular chirp profile centered at 8.9-GHz with 940-MHz bandwidth and 28.8-μs period with only 1.9-MHz_{rms} frequency error including the turn-around points and 14.8-mW power dissipation. The achieved 32.63-MHz/μs chirp slope is higher than that of FMCW FS-PLLs previously reported by 2.6×.

Keywords : digital phase-locked loop (DPLL), digitally-controlled oscillator (DCO), time-to-digital converter (TDC), bang-bang phase-frequency detector (BB-PFD), frequency synthesizer phase-locked loop (FS-PLL), calibration, adaptive-bandwidth, bandwidth tracking, frequency modulated continuous wave (FMCW), Radar, frequency chirp.

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Chapter 1

Introduction

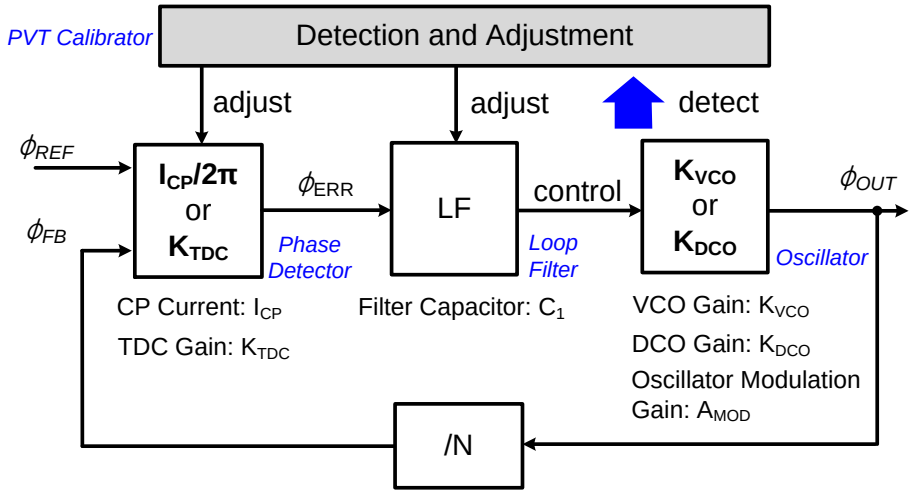
1.1 Motivation

The significant increase of the required calculating power and communication bandwidth imposes an increase of power consumption, area, and design complexity on recent system-on-chips (SoCs) for mobile application processor, graphic processing unit (GPU), and so on. Therefore, a scaling of CMOS technology is inevitable and in continuous concerns for satisfying these requirements. However, as the CMOS technology scales down continuously, variations of device characteristics according to process, voltage, and temperature (PVT) conditions are increased accordingly. These variations are originated from the small feature of transistors, resulting in non-uniform carrier mobility between devices and R/C variation on on-chip interconnects and via structures. In addition, near threshold operation of transistors by low supply voltage also increases the variation due to inaccurate device modeling in sub-threshold operations.

With the large PVT variations, a phase-locked loop (PLL) that maintains its performance such as jitter, lock time, and bandwidth is critical for the overall system performances. However, it is becoming more difficult to satisfy all these requirements in limited die area and power budget, because the large variation on device characteristics result in various trade-offs in PLL design [1]. To circumvent these trade-offs, this paper presents a design concept and its validation results for PVT-insensitive PLL, minimizing trade-offs.

In charge-pump PLLs, a loop characteristic varies due to PVT-sensitive circuit parameters such as the voltage-controlled oscillator (VCO) gain and charge-pump (CP) current [2]. Even in digital PLLs, the uncertainties of loop characteristics still remains due to the variation in the digitally-controlled oscillator (DCO) gain and time-to-digital converter (TDC) gain [3].

To cope with these uncertainties, prior works have adopted a calibration method for loop parameters [3]-[9]. Most of the calibrations are generally conducted by a detection of loop parameter variation and an adjustment of other loop parameters to compensate for the variations. As shown in Fig. 1.1, a dedicated PVT calibrator detects the variation of loop parameter such as the VCO gain K_{VCO}, the DCO gain K_{DCO}, or loop gain at first. Next, the PVT calibrator adjusts other loop parameters, i.e., the charge-pump current I_{CP}, a filter capacitor C_1, a TDC gain K_{TDC}, or a modulation gain for oscillator A_{MOD}.



Reference	Detection	Adjustment
[4]	VCO Gain: K_{VCO}	I_{CP} and C_1
[5]	VCO Gain: K_{VCO}	I_{CP}
[3]	DCO Gain: K_{DCO}	K_{TDC}
[6]	Loop Gain: $K_{TDC}K_{DCO}/N$	K_{TDC}
[7], [8], [9], [34]	Control Signal: V_{CTRL}, I_{CTRL}, D_{CTRL}	I_{CP} or A_{MOD}

Fig. 1.1. Detection and adjustment of loop parameters by PVT calibrator against PVT variations in previously-reported PLLs.

These calibration methods can be largely categorized as a foreground and a background operation. Since most of the calibrations are performed in foreground, they need a periodic recalibration if the environmental conditions (e.g., voltage and temperature) change [3]-[6]. Unlike the foreground calibration, the background calibra-

tion can handle the real-time drift due to voltage and temperature [7]-[9]. However, most of the background calibrations monitor analog voltage/current or digital code to detect the voltage and temperature drifts. Therefore, these methods are susceptible to a linearity and noise performance of the detection blocks, so that it is hard to apply them for the deeply-scaled CMOS technologies with low voltage headroom (V_{DD}-V_{TH}) and larger device noises. In addition, the background calibration needs additional blocks and feedback loops to detect and compensate the variation of control voltage/current or code.

To mitigate such drawbacks, this paper presents a digital PLL that desensitize the loop characteristics to PVT variations using functional blocks with PVT-insensitive transfer. The PVT-insensitive transfer characteristic can be realized by a ratiometric design that utilizes a ratio between currents, a fixed ratio between device size, or a fixed fraction of the reference clock period. Also, since we are intended to reduce the uncertainty in functional block-level such as DCO, TDC, and DLF, the proposed PLLs realize predictable characteristics in background without explicit calibration or additional circuits.

Consequently, two design concepts covering this thesis can be summarized as:

1. Without additional blocks, we build the calibration-free PLLs to keep the PVT-insensitive performances, focusing on the performance of basic PLL blocks.
2. Based on the ratiometric design, we make the transfer characteristic of these functional blocks to be only determined by a relative portion of specific variable, size of identical elements, or given clock period or unit interval.

1.2 Thesis Organization

This thesis is organized as follows.

In Chapter 2, the characteristics of basic charge-pump PLL and digital PLL are explained. Also, based on their loop dynamics, key design parameters to realize a calibration-free PLL without explicit calibration are introduced.

In Chapter 3, by reviewing the frequently-used oscillators and phase detectors, their variation which causes the uncertainties of loop characteristics is introduced.

In Chapter 4, in order to mitigate the variation of both oscillator and phase detector, the design concepts of covering this paper are explained and compared to previous one.

In chapter 5, a digital LC-PLL that has a PVT-insensitive loop bandwidth (BW) by using a constant-relative-gain DCO and a constant-gain TDC is explained. A motivation and the prior works implementing PVT-insensitive loop BW PLL are explained. To obtain the PVT insensitive loop BW which is a constant fraction of the reference frequency, the PLL architecture even with a simple proportional-integral digital loop filter without explicit calibration is explained. Then, the circuit implementation is explained and the measurement results are shown.

In chapter 6, an 8.9-GHz, digitally-controlled frequency synthesizer PLL capable of precise triangular frequency chirp designed with proposed design concepts is explained. A FMCW radar principle, required specification and the prior works implementing chirp frequency synthesizer PLL are explained. To obtain the precise triangular chirp profile, a proposed calibration-free two-point modulation via a type-

III PLL architecture and a polarity-alternation with given chirp slope information is explained and the simulation results are shown using behavioral model. Then, the circuit implementation is explained and the measurement results are shown.

Chapter 7 summarizes the proposed works and concludes this thesis.

Chapter 2

Conventional Phase-Locked Loop (PLL)

In this section, we'll overview the conventional PLL architectures to bring up the critical loop parameters, determining the key performance of the PLL such as jitter, phase noise, lock time, and modulation capability, etc.

2.1 Charge-Pump PLL

A charge-pump PLL is the most popular architecture in various fields such as wireless and wireline communications, and system on chips (SoCs) applications [2]. This is because the integral control via a charge-pump and filter capacitor helps suppress static phase offset because it ensures that the loop will not settle until ϕ_{ERR} reaches zero. When ϕ_{ERR} become zero, i.e., no input from the charge-pump, the control voltage maintains constant if a leakage current is not quite large.

2.1.1 Operating Principle

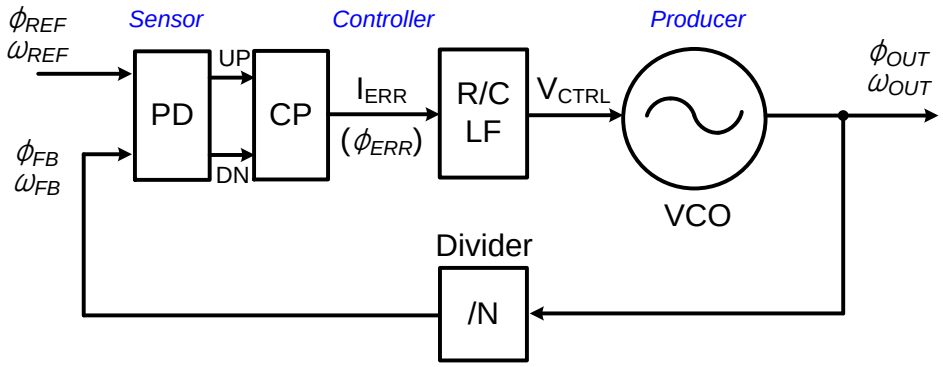


Fig. 2.1. Conventional charge-pump PLL.

Fig. 2.1 shows a block diagram of a conventional charge-pump PLL, consisting of a phase detector as a sensor, a charge-pump (CP) and R/C loop filter (LF) as a controller, and a voltage-controlled oscillator (VCO) as a producer. A PLL is a feedback system that tries to match the oscillator output phase ϕ_{OUT} and frequency ω_{OUT} to those of the reference clock, ϕ_{OUT} and ω_{OUT}, respectively. A PD measures the error between the two phases, ϕ_{REF} and ϕ_{FB}. Upon the detection of the phase error, ϕ_{ERR}, the LF makes appropriate adjustments on the VCO frequency ω_{OUT} to reduce this error. After the phase and frequency between input and output are same, ϕ_{OUT} and ω_{OUT} are equal to $N\phi_{REF}$ and $N\omega_{REF}$, respectively.

2.1.2 Loop Dynamics

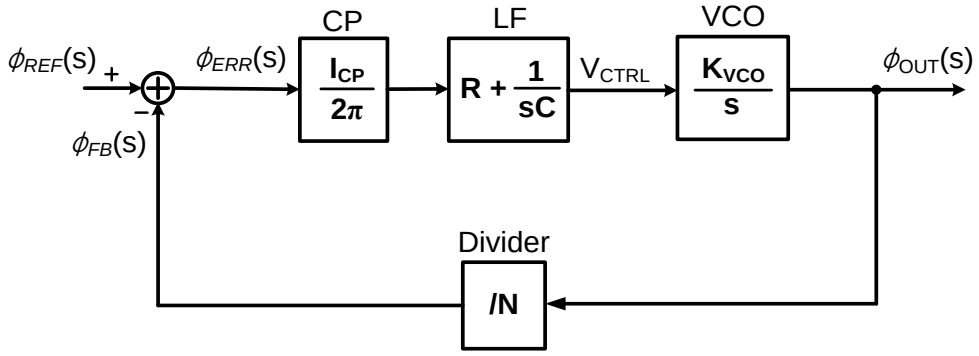


Fig. 2.2. The s-domain model of a second-order charge-pump PLL.

Fig. 2.2 shows the s-domain model of a second-order charge-pump PLL which can guide the role of the basic loop parameters for PLL dynamics. First, the open-loop transfer function the PLL *G(s)* can be expressed as:

$$G(s) = \frac{\phi_{OUT}}{\phi_{ERR}} = \frac{I_{CP}}{2\pi} \cdot Z(s) \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N} = \frac{I_{CP}}{2\pi} \cdot \left(R + \frac{1}{sC} \right) \cdot \frac{K_{VCO}}{s} \cdot \frac{1}{N} \quad (3.1)$$

where *Z(s)* is the transfer function of 1st order loop filter (LF), I_{CP} is the charge-pump current, K_{VCO} is the gain of VCO, and *N* is the division ratio of the clock divider. And, R and C are the LF resistance and capacitance, respectively.

The unit of the gains of the PD and the CP, i.e., $I_{CP}/2\pi$ and the VCO, i.e., K_{VCO} are A/rad and rad/s/V, respectively.

Using the *G(s)*, the overall closed-loop transfer function of the PLL *H(s)* can be expressed as:

$$H(s) = \frac{\phi_{OUT}}{\phi_{REF}} = \frac{NG(s)}{1+G(s)} = \frac{\frac{I_{CP}K_{VCO}}{2\pi C} \cdot (1+sRC)}{s^2 + \frac{I_{CP}K_{VCO}R}{2\pi N} s + \frac{I_{CP}K_{VCO}}{2\pi NC}} = \frac{N\omega_n^2 \cdot (1+sRC)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad (3.2)$$

From the definition shown in the last line of (3.2), we can express ω_n and ζ as:

$$\zeta = \frac{R}{2} \cdot \sqrt{\frac{I_{CP} K_{VCO} C}{2\pi N}} \qquad \omega_n = \sqrt{\frac{I_{CP} K_{VCO}}{2\pi NC}} \tag{3.3}$$

$$\omega_{BW} \approx 2\zeta\omega_n = \frac{I_{CP} K_{VCO} R}{2\pi N} \tag{3.4}$$

where ω_{BW} is the loop bandwidth of the PLL.

(3.3) and (3.4) tells us that the loop bandwidth ω_{BW} as well as the natural frequency ω_n and damping factor ζ of the charge-pump PLL are significantly dependent on the loop parameters such as I_{CP}, K_{VCO}, R, and C, varying with process, voltage, and temperature (PVT) conditions.

2.2 Digital PLL

A digital phase-locked loop (PLL) that can be realized entirely in digital circuits has been an actively pursued goal in recent literature [3]. The motivation is to eliminate the analog circuits and control signals in conventional charge-pump PLLs so that their designs are insensitive to a leakage current on the capacitors and can be easily migrated to various process technologies. In addition, the digital PLL removes an area penalty imposed by the RC loop filter for narrow loop bandwidth, a dynamic range problem of the charge-pump in deeply-scaled technologies as the supply voltage approaches near the device threshold, and an up/down current mismatch incurring reference spur.

2.2.1 Operation Principle

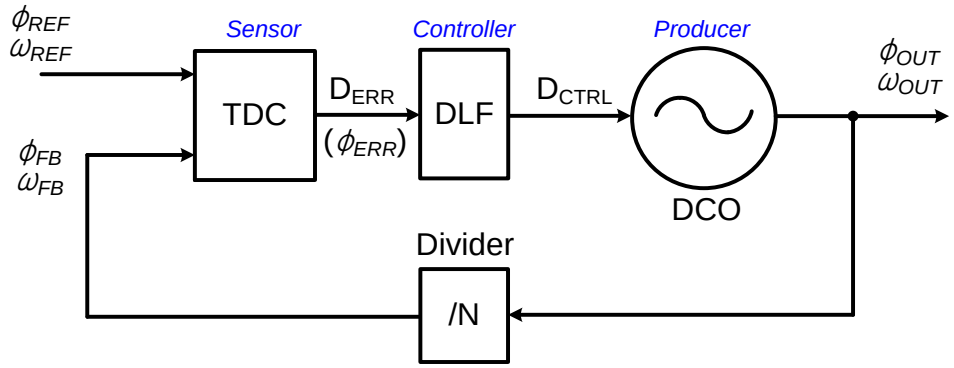


Fig. 2.3. A digital PLL equivalent to the conventional charge-pump PLL.

Fig. 2.3 shows a block diagram of a digital PLL equivalent to the charge-pump PLL in Fig. 2.1, which consists of a time-to-digital converter (TDC), a digital loop filter (DLF), a digitally-controlled oscillator (DCO), and a divide-by-N frequency divider. The TDC provides a digitized measure D_{ERR} of the phase error between the two phases, ϕ_{REF} and ϕ_{FB}. Upon this D_{ERR}, the DLF updates the DCO input code D_{CTRL} proportional to the phase error. According to the D_{CTRL}, the DCO controls its frequency. Finally, the divide-by-N divider generates feedback clock phase ϕ_{FB} for the TDC.

2.2.2 Loop Dynamics

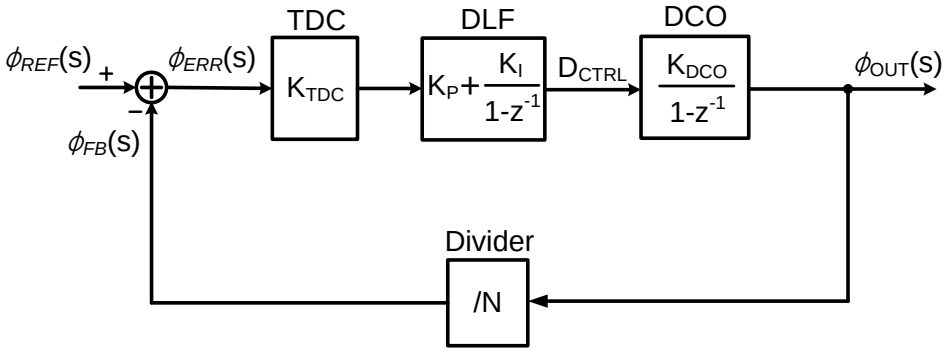


Fig. 2.4. The z-domain model of a second-order digital PLL.

Fig. 2.4 shows the z-domain model of a second-order digital PLL. First, the open-loop transfer function the PLL *G(s)* can be expressed as:

$$G(z) = \frac{\phi_{OUT}}{\phi_{ERR}} = K_{TDC} \cdot \left(K_P + \frac{K_I}{1 - z^{-1}} \right) \cdot \frac{K_{DCO}}{1 - z^{-1}} \cdot T_S \cdot \frac{1}{N} \quad (3.5)$$

Where K_{TDC} and K_{DCO} is the TDC and DCO gains, in units of bits/radian and rad/s/bit, respectively and N is the division ratio of the clock divider. K_P and K_I are the fixed proportional and integral gains of the DLF, respectively and T_S is the sampling period of the DLF.

Here, *G(z)* can be converted into s-domain continuous-time model by approximating z^{-1} as $\exp(-sT_S) \approx 1-sT_S$, while this approximation is valid only for a frequency range well below the sampling frequency ($1/T_S$) [10].

Therefore, the s-domain open-loop transfer function can be derived as:

$$G(s) = \frac{\phi_{OUT}}{\phi_{ERR}} = \frac{K_{TDC} K_{DCO}}{N T_S} \cdot \frac{K_P T_S s + K_I}{s^2} \quad (3.6)$$

Using the *G(s)*, the overall closed-loop transfer function of the PLL *H(s)* can be expressed as:

$$H(s)=\frac{\phi_{OUT}}{\phi_{REF}}=\frac{NG(s)}{1+G(s)}=\frac{\frac{K_{TDC}K_{DCO}}{T_S}\cdot\left(K_P T_S s+K_I\right)}{s^2+\frac{K_P K_{TDC}K_{DCO}}{N}s+\frac{K_I K_{TDC}K_{DCO}}{NT_S}}=\frac{N\omega_n^2\cdot\left(1+s\frac{K_P}{K_I}T_S\right)}{s^2+2\zeta\omega_n s+\omega_n^2} \quad (3.7)$$

$$\zeta=\frac{K_P}{2}\cdot\sqrt{\frac{K_{TDC}K_{DCO}T_S}{NK_I}} \qquad \omega_n=\sqrt{\frac{K_I K_{TDC}K_{DCO}}{NT_S}} \quad (3.8)$$

$$\omega_{BW}\approx 2\zeta\omega_n=\frac{K_{TDC}K_{DCO}K_P}{N} \quad (3.9)$$

Equation (3.8) and (3.9) implies that the loop bandwidth ω_{BW} as well as the natural frequency ω_n and damping factor ζ of the digital PLL are also dependent on the loop parameters such as K_{TDC} and K_{DCO}, varying with PVT conditions.

Therefore, even though the digital PLL has many advantages compared to the charge-pump PLL, these uncertainties on loop parameters are still problematic in the use of digital PLLs.

Chapter 3

Variations on Phase-Locked Loop (PLL)

In this section, we'll review the variation of oscillator and phase detector gains which are key parameters to determine the loop characteristics of the PLL.

3.1 Oscillator Gain Variation

As explained in Chapter 2, an oscillator generates a clock that has a frequency controlled by a control signal from the loop filter. There are two kinds of the most popular oscillators. At first, a ring oscillator is used in many consumer SoCs and energy-efficient transceivers due to its wide tuning range, low power, and multi-phase outputs. While the ring oscillator has many advantages, it typically has a poor jitter performance compared to an LC oscillator [11]. In contrast, the LC oscillator has the superior jitter and phase noise performance at high frequency, so that it is widely used for RF and wireline transceivers with high data rate. However, it typically op-

erates only over a narrow tuning range and dissipates large power. Unfortunately, the gain of both ring and LC oscillators are PVT-sensitive parameters. For instance, in 65nm CMOS technologies, the gain of the ring oscillator varies by a factor of 3~6 and the gain of the LC oscillator with varactor-based tuning varies by a factor of 1~2.

3.1.1 Ring Voltage-Controlled Oscillator

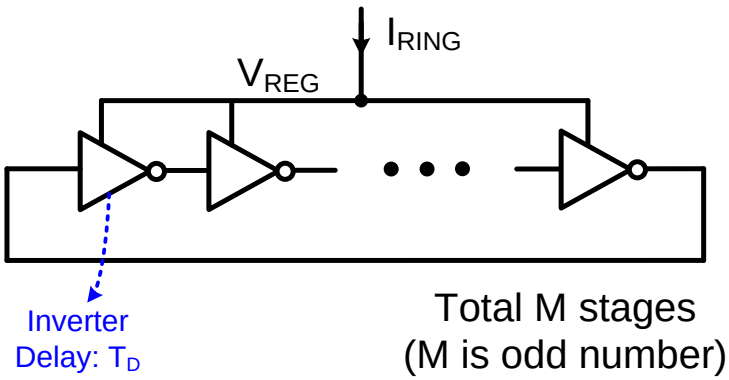


Fig. 3.1. A ring oscillator composed of M stage inverters.

Fig. 3.1 shows a ring oscillator, consisting of M stage CMOS inverters. A delay T_D of a single stage inverter and an oscillator frequency f_{osc} can be expressed as:

$$T_D = \frac{C \cdot V_{REG}}{I_{RING}}$$
$$f_{osc} = \frac{1}{2MT_D} = \frac{I_{RING}}{2MCV_{REG}} \quad (3.10)$$

Where C is the total load capacitance of each inverter stage, M is the number of stages, I_{RING} is the oscillator driving current, and V_{REG} is the supply voltage of the ring oscillator.

By differentiating the last line of (3.10) according to T_D, the gain of the ring oscillator can be derived as:

$$K_{RING} = \frac{\partial f_{osc}}{\partial T_D} = -\frac{1}{2M} \cdot \frac{1}{T_D^2} \quad (3.11)$$

Equation (3.11) implies that the gain of ring oscillator is inversely proportional to the square of the T_D. This result implies that the gain is nonlinear and sensitive to the PVT variations of the delay element.

For instance, the simulated FO4 delay of thin oxide NMOS in TSMC 65nm CMOS technology is shown in Fig. 3.2. By (3.11), delay variation by a factor of 2.4 results in the gain decrease by factor of 5.78.

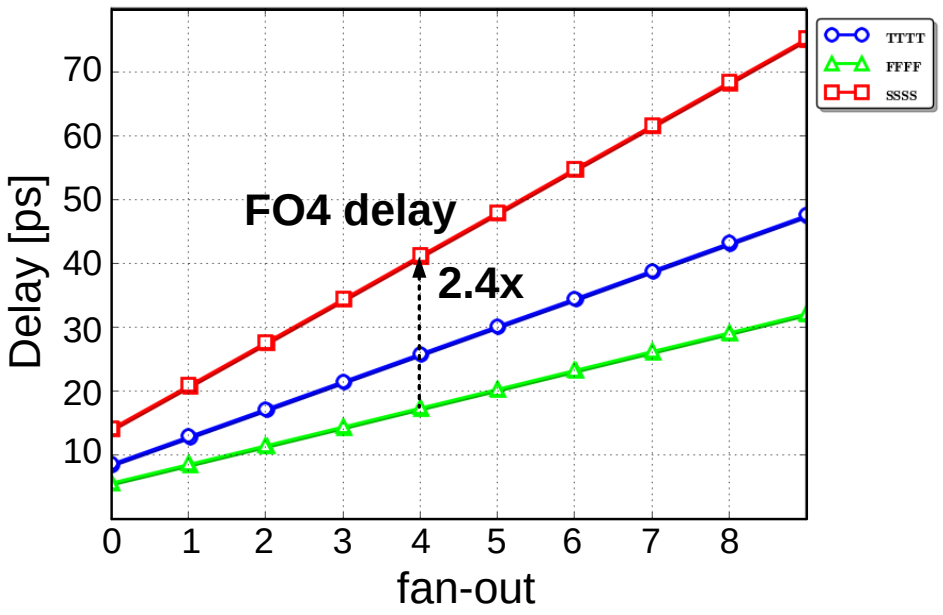


Fig. 3.2. Simulated delay variation of the inverter versus fan-out.

3.1.2 LC Voltage-Controlled Oscillator

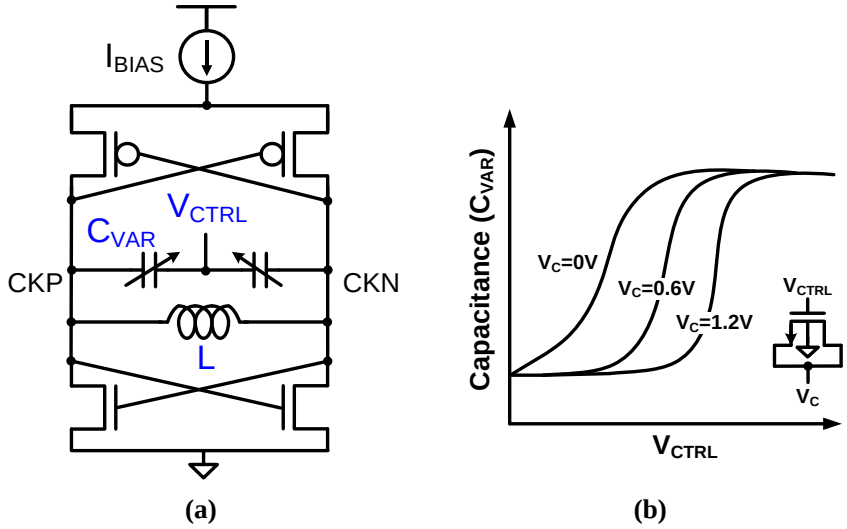


Fig. 3.3. (a) Conventional LC-VCO with varactor tuning. (b) Varactor tuning curve.

Fig.3.3 shows the schematic of conventional LC-VCO with varactor-based tuning. The VCO gain K_{VCO} can be written as:

$$K_{VCO} = \left| \frac{\partial \omega_{osc}}{\partial V_{CTRL}} \right| = \left| \frac{\partial \omega_{osc}}{\partial C_{VAR}} \right| \cdot \left| \frac{\partial C_{VAR}}{\partial V_{CTRL}} \right| \quad (3.12)$$

Where V_{CTRL} and C_{VAR} are the control voltage and the capacitance of varactor, respectively. The oscillation frequency ω_{osc} is given by:

$$\omega_{osc} = \frac{1}{\sqrt{L \cdot (C_o + C_{VAR})}} \quad (3.13)$$

Where C_0 is the tank capacitance excluding the C_{VAR}.

By differentiating (3.13) with respect to C_{VAR}, the frequency change over C_{VAR} can

be derived as:

$$\left|\frac{\partial \omega_{osc}}{\partial C_{VAR}}\right| = \frac{L}{2} \cdot \omega_{osc}^{3} \quad (3.14)$$

Therefore, from (3.12), the VCO gain K_{VCO} can be derived as:

$$K_{VCO} = \frac{L}{2} \cdot \omega_{osc}^{3} \cdot \left|\frac{\partial C_{VAR}}{\partial V_{CTRL}}\right| \quad (3.15)$$

Equation (3.15) indicates that the gain of LC-VCO is proportional to $|\partial C_{VAR}/\partial V_{CTRL}|$. As shown in Fig. 3.3(b), the slope $|\partial C_{VAR}/\partial V_{CTRL}|$ on varactor tuning curve is changed by the average voltage of oscillation node (V_C) that is changed by PVT conditions [12]. In addition, the K_{VCO} are proportional to ω^3_{OUT} even if linear capacitor tuning is possible, i.e., constant $|\Delta C_{VAR}/\Delta V_{CTRL}|$. Therefore, the gain of LC-VCO is nonlinear according to operating frequency and sensitive to PVT conditions.

3.1.3 LC Digitally-Controlled Oscillator (LC-DCO)

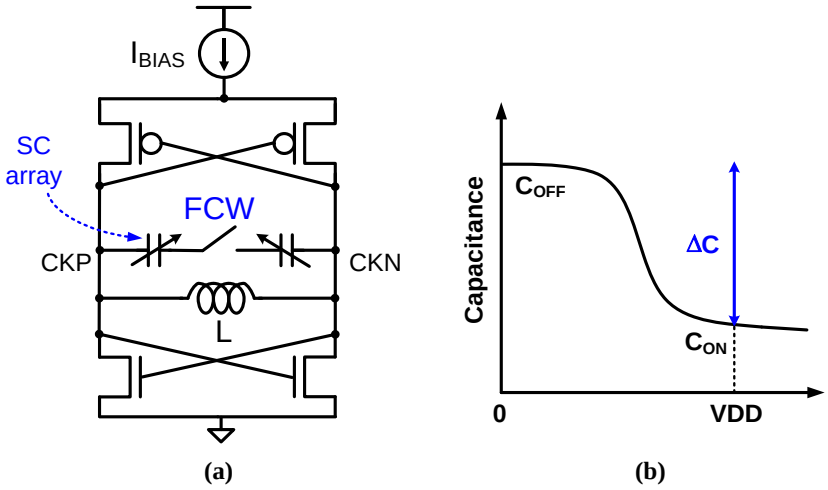


Fig. 3.4. (a) LC-DCO with switched-capacitor (SC) array. (b) Switched-capacitor tuning curve.

As shown in Fig. 3.4(a), an LC digitally-controlled oscillator (LC-DCO) is usually implemented by using switched-capacitor (SC) array [13]. Fig. 3.4(b) also shows the tuning curve of varactor used in SC array. When a frequency control word (FCW) is low and high, the capacitance is large (C_{OFF}) and small (C_{ON}). The input FCW controls the frequency of LC-DCO by changing the number of switched-capacitors operating in large or small capacitance region.

Similar to the LC-VCO, the DCO gain K_{DCO} can be expressed as:

$$K_{DCO} = \frac{L}{2} \cdot \omega_{osc}^{3} \cdot \left| \frac{\Delta C}{\Delta D_{CTRL}} \right| \quad (3.16)$$

Where D_{CTRL} is the FCW from a digital loop filter and ΔC is the difference between C_{OFF} and C_{ON}, respectively.

According to (3.16), if the ΔC is changed by PVT conditions, the DCO gain K_{DCO} also changes. In addition, since the K_{DCO} is also proportional to ω^3_{osc}, the variation of ΔC can greatly affect the K_{DCO} in the vicinity of high frequency.

3.2 Phase Detector Gain Variation

As explained in Chapter 2, a phase detector (PD) measures the phase error between the reference clock phase and the feedback clock phase. There are two kinds of widely used phase detectors.

3.2.1 Linear Phase Detector (PD)

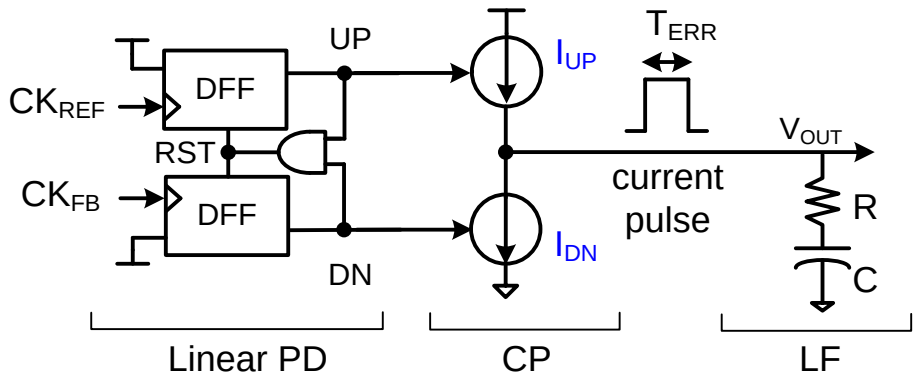


Fig. 3.5. Linear PD and CP convert phase error to current pulse.

As shown in Fig. 3.5, a linear PD which is implemented by two edge-triggered DFFs with reset logic is widely used in most of charge-pump PLLs due to its linear transfer function regardless of PVT and frequency conditions. However, although

the transfer characteristic of linear PD is insensitive to PVT conditions, extent of current pulse produced by the charge pump (CP) followed by linear PD (i.e., linear PD + CP) varies with PVT conditions. This is because the CP current I_{UP} and I_{DN} change according to PVT conditions. It is well known that the gain of linear PD is determined as $I_{CP}/2\pi$. So, the gain of linear PD is also PVT-sensitive design parameter.

3.2.2 Linear Time-to-Digital Converter (TDC)

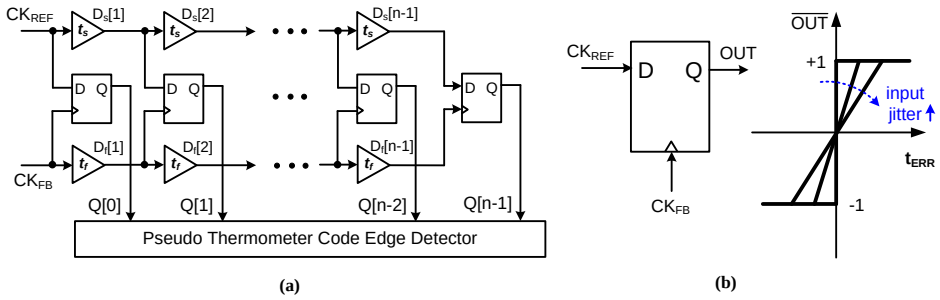


Fig. 3.6. (a) Vernier TDC based on delay chains. (b) BBPD and its transfer curve.

Fig. 3.6(a) shows the linear time-to-digital converter (TDC) based on delay chain. One problem with the delay chain TDC is that its gain and resolution may vary with the operating conditions. For instance, a Vernier TDC in [14] is composed of two delay chains, of which delay can change with the PVT conditions. Ring oscillator based TDCs also have a problem due to the delay variation, and need to be compensated [39],[40].

On the other hand, in Fig. 3.6(b), a bang-bang PD (BBPD) using a single D-type flip-flop can serve as a linear TDC in presence of the input jitter, but its effective gain depends strongly on the standard deviation of input jitter, i.e., $K_{BB} \propto 1/\sigma$ [15]. One way to alleviate this dependency is to add an intentional dither jitter that can overwhelm the other jitter components [16], [17]. However, the resulting TDC characteristic may still be subject to PVT variations, unless the dither jitter is generated in a PVT-independent way.

Chapter 4

Proposed DCO and TDC for Calibration-Free PLL

In previous sections, we have reviewed the PVT variations on PLLs. In this section, in order to mitigate these variations, we'll investigate the principle of key building blocks, reducing the variations on the PLL. Thanks to the proposed DCO and TDC, the PLL can realize PVT-insensitive loop characteristics without an explicit calibration or additional circuits.

4.1 Digitally-Controlled Oscillator (DCO)

4.1.1 Overview

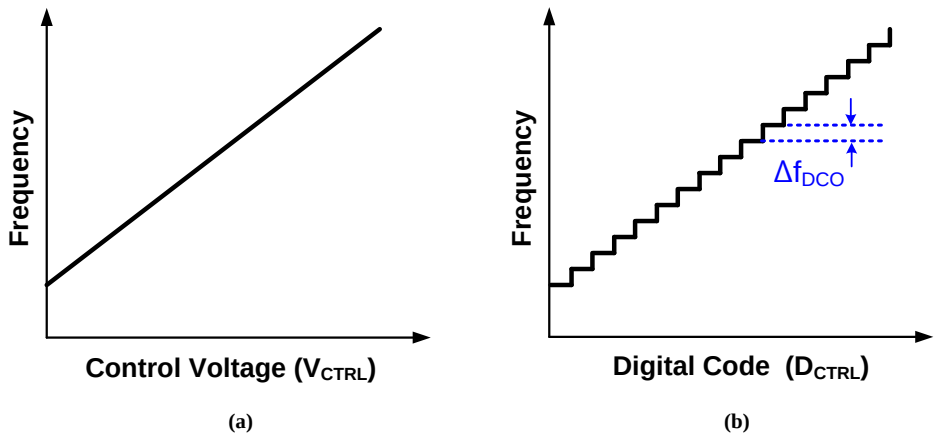


Fig. 4.1. Transfer characteristics of (a) VCO and (b) DCO.

A digitally-controlled oscillator (DCO) performs a digital-to-frequency conversion for digital PLL. Therefore, the DCO clock frequency is controlled by the input digital code contrary to the control voltage in the VCO. Fig. 4.1 shows the transfer characteristics of the VCO and DCO. As explained in Section 3.1, while the VCO gain indicates a frequency change with respect to the control voltage change, i.e., $|\partial f_{VCO}/\partial V_{CTRL}|$, the DCO gain represents a frequency change with respect to the unit change of input digital code, i.e., $|\partial f_{DCO}/\partial D_{CTRL}|$.

Generally, most of the VCO and DCO designs focus on the linear voltage-to-frequency (V-to-*f*) and code-to-frequency (D-to-*f*) characteristics, respectively. If the gain of VCO and DCO is ideally constant, these linear transfer characteristics are effective in entire frequency tuning range. The main reason of this linearization is that the minimized gain variation can improve noise sensitivity of the oscillator [8].

Likewise, a LC-VCO for low noise PLL tries to reduce the oscillator gain itself by utilizing multiple low gain V-to-*f* curves in the RF applications [7].

Unfortunately, the VCO and DCO with linear transfer have fundamental drawback. As shown in Fig. 4.2, the gain of the VCO and DCO still vary with PVT conditions.

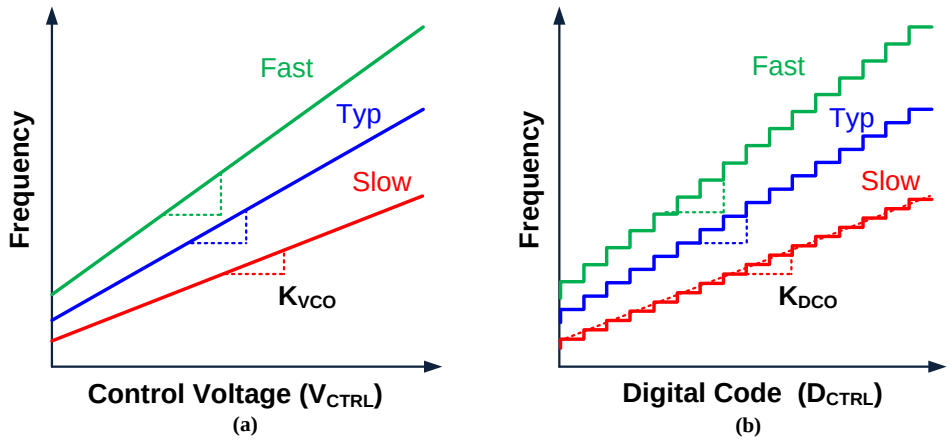


Fig. 4.2. Oscillator gain variation vs. PVT conditions: (a) VCO and (b) DCO.

Even if the ring-VCO PLL operates at single frequency, the gain variation by PVT change results in large variation of loop characteristics such as natural frequency and damping factor [1]. Also, in the LC-VCO PLL with linear varactor tuning, the gain variation according to PVT and ω_{OUT} changes results in the variation of loop transfer [7]. For instance, in wireless application such as Radar, the loop bandwidth variation deteriorates a modulation accuracy of chirp signal generator. Also, in wireline application such as SONET [18], the variation of jitter peaking bring about large jitter amplification when multiple PLLs are in cascade.

4.1.2 Constant-Relative-Gain DCO

To address this problem, a VCO and DCO with constant relative-gain were presented in [19],[20]. The constant-relative-gain DCO changes its frequency by a constant fraction of the current operating frequency ω_{OUT} in response to a unit step in its digital input:

$$\frac{\Delta\omega_{OUT}/\omega_{OUT}}{\Delta D_{IN}} = constant \quad (4.1)$$

That is, at a given operating frequency ω_{OUT}, which is fixed by the reference frequency and multiplication ratio of the PLL, the DCO has a constant gain, or equivalently a gain that scales proportionally with ω_{OUT} as shown in Fig. 4.3.

In a linear DCO with constant gain $\Delta\omega_{OUT}/\Delta D_{IN}$, as the ω_{OUT} increases, the relative change according to unit code change $\Delta\omega_{OUT}/(\Delta D_{IN}\cdot\omega_{OUT})$ decreases. On the other hand, in constant-relative-gain DCO follows (4.1), the relative change according to unit code change $\Delta\omega_{OUT}/(\Delta D_{IN}\cdot\omega_{OUT})$ stays constant. In other words, the DCO gain $K_{DCO}=\Delta\omega_{OUT}/\Delta D_{IN}$ is solely proportional to $\omega_{OUT}=N\cdot\omega_{REF}$, which is typically well-controlled. The constant-relative-gain DCO can be achieved by the ratiometric circuit design and this will be explained in circuit implementations.

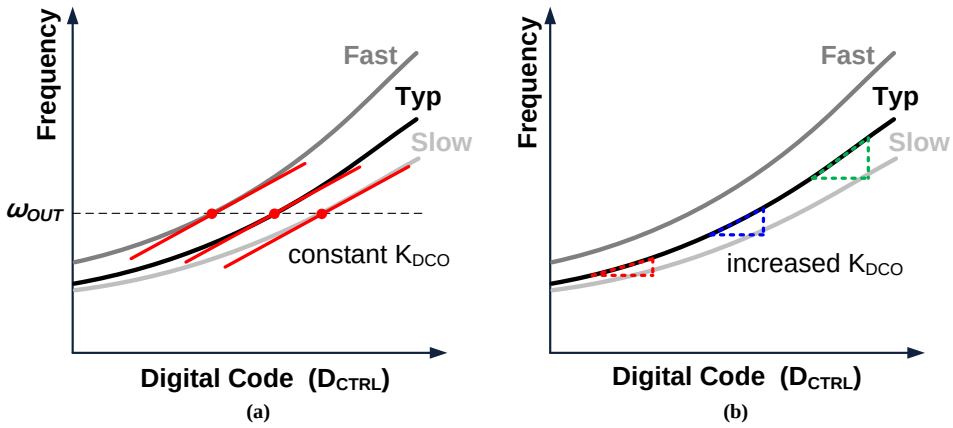


Fig. 4.3. Constant relative-gain characteristics: (a) constant K_{DCO} at given operating frequency ω_{OUT} and (b) K_{DCO} is proportional to ω_{OUT}.

In addition, in case of the LC-DCO covering relatively wide frequency range with single tuning curve, the K_{DCO} are significantly nonlinear according to ω_{OUT} [7]. In (3.16), the K_{DCO} are proportional to ${\omega^3}_{OUT}$ even though linear capacitor tuning is adopted, i.e., constant $|\Delta C/\Delta D_{CTRL}|$. As a result, at high frequency, phase noise performance may worsen by large K_{DCO}. On the other hand, since the constant-relative-gain DCO has the K_{DCO} proportional to ω_{OUT}, the K_{DCO} is much smaller than that of linear capacitor-tuned LC-DCO at high frequency. Fig. 4.4 shows the comparison of K_{DCO} according to ω_{OUT} between linear switched-capacitor-based LC-DCO and constant relative-gain LC-DCO.

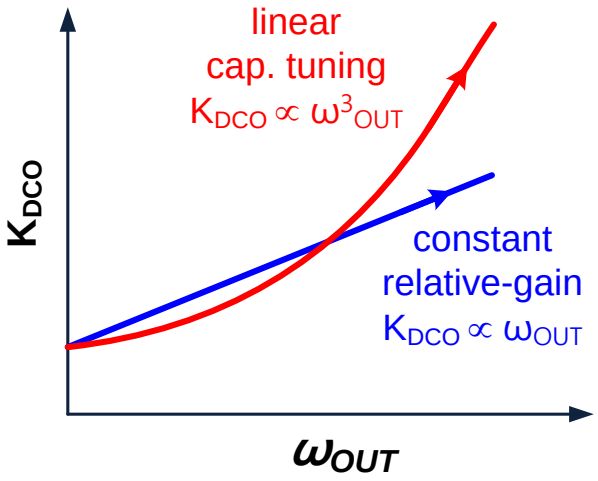


Fig. 4.4. Comparison of K_{DCO} according to ω_{OUT} between the linear capacitor-tuned LC-DCO and constant relative-gain LC-DCO.

4.2 Time-to-Digital Converter (TDC)

4.2.1 Overview

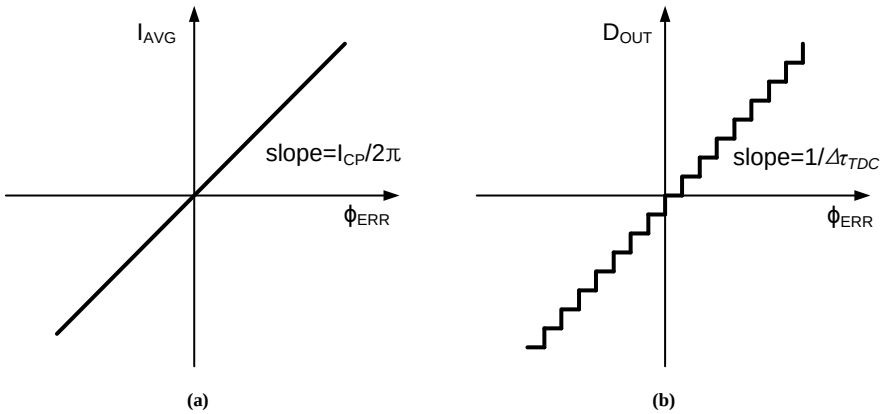


Fig. 4.5 Transfer characteristic of (a) linear PD and (b) TDC.

Fig. 4.5 shows the transfer characteristic of linear phase detector (PD) and linear time-to-digital converter (TDC). The linear PD converts the phase error ϕ_{ERR} to voltage in a charge-pump PLL. In similar way, the TDC generates a digital code which is proportional to the ϕ_{ERR} between the reference and feedback clock phases.

The TDC output D_{OUT} can be expressed by:

$$D_{OUT} = \frac{\Delta t}{\Delta \tau_{TDC}} = \left(\frac{\Delta \phi}{2\pi} \cdot T_{REF} \right) \cdot \frac{1}{\Delta \tau_{TDC}} = \frac{T_{REF}}{2\pi \cdot \Delta \tau_{TDC}} \cdot \Delta \phi \quad (4.3)$$

Where $\Delta\tau_{TDC}$ is the unit delay of delay chain. And, Δt and $\Delta\phi$ are the time and phase error, respectively [14].

Therefore, the TDC gain K_{TDC} in units of bit/rad can be written as:

$$K_{TDC} = \frac{\Delta D_{OUT}}{\Delta \phi} = \frac{T_{REF}}{2\pi \cdot \Delta \tau_{TDC}} \quad (4.4)$$

(4.4) indicates that the TDC gain is determined by the unit delay of delay chain and operating frequency. As explained in Chapter 3.1, delay variation by a factor of 2~4 in CMOS inverter results in significant change of the K_{TDC}, so that it is problematic for predictable PLL loop characteristics. In addition, the K_{TDC} is also changed by an operating frequency (=1/T_{REF}). Therefore, the TDC gain calibration method has been actively studied [17].

4.2.2 Constant-Gain TDC

To mitigate the TDC gain variation, we presented the constant-gain TDC architecture regardless of PVT, input jitter, and operating frequency conditions [20]. The proposed constant-gain TDC provides a digitized measure of the phase error with a constant resolution measured in radians or UIs. The TDC gain K_{TDC} in units of bits/UI stays constant regardless of the PVT and frequency conditions.

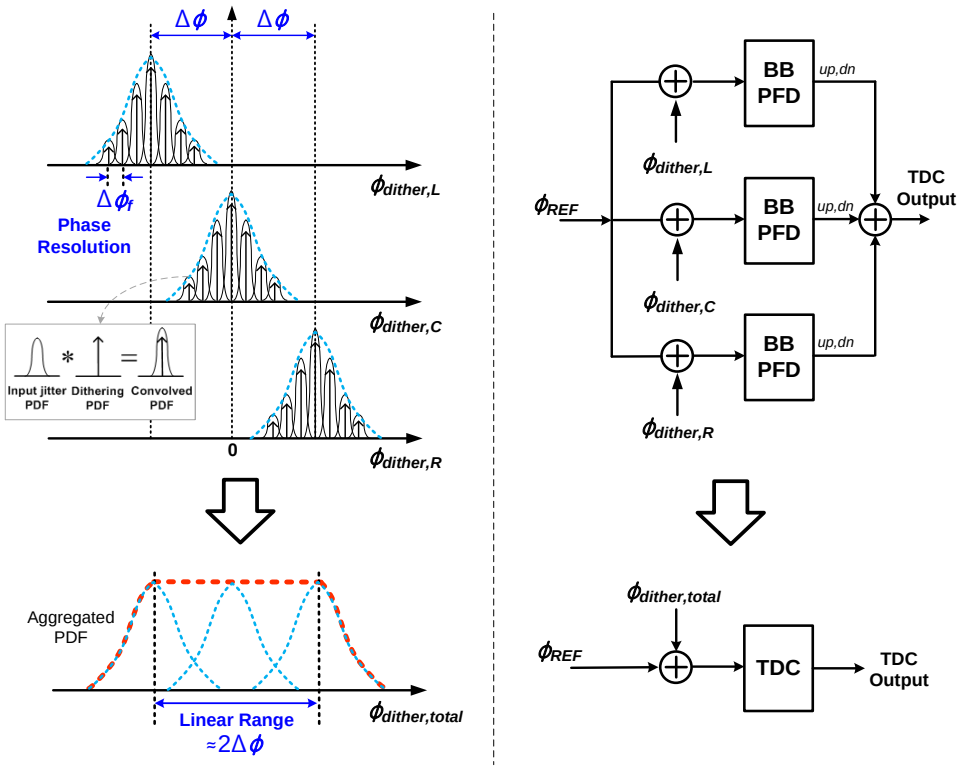


Fig. 4.6. (a) Linearization of the TDC characteristics with added random dither. (b) Implementation of constant-gain TDC.

Fig. 4.6 illustrates how the proposed TDC provides a linear measure on the phase error. A TDC gain which is independent of the PVT, input jitter, and frequency conditions can be achieved by using three oversampling BB-PFDs triggered by individually dithered clocks. These three dithered clocks with a unit phase step of $\Delta\phi_f$ and a phase offset of $-\Delta\phi$, 0, or $+\Delta\phi$ serve as sampling clocks for BB-PFDs. Both the dither jitter step $\Delta\phi_f$ and phase offset $\Delta\phi$ are digitally programmable in units of a phase interpolator (PI) resolution steps via an external I^2C interface.

Basically, each BB-PFD recovers the linear measure in a statistical sense by comparing the phase error with a different threshold. Furthermore, the use of multiple BB-PFDs whose sampling phases dither at different offsets ($\phi_{dither,L}$, $\phi_{dither,C}$,and $\phi_{dither,R}$) enhances the accuracy of the phase error that can be recovered in a finite time period.

Fig. 4.6(a) illustrates the probability density functions (PDFs) of the individual feedback clock phases triggering the BB-PFDs and the aggregate PDF of all the clock phases combined ($\phi_{dither,tot}$). When finite input jitter is present, the effective jitter PDF experienced by the BB-PFDs is the input jitter PDF convolved with the added dither jitter PDF. It can be shown that with a proper amount of dither jitter and phase offset between the unit PDFs, the aggregate PDF can take an approximately uniform distribution in the range of $-\Delta\phi \sim +\Delta\phi$. This uniform PDF results in a linear TDC characteristic within the range of $2\Delta\phi$ when the TDC output is computed as a difference between the *up* and *dn* counts of the BB-PFDs, accumulated over a given period.

Consequently, as long as the phase offset ($\Delta\phi$) and dither jitter step ($\Delta\phi_f$) maintain constant magnitudes in units of UIs (i.e., in fixed numbers of phase steps), the effec-

tive TDC gain is determined mainly by $\Delta\phi$, which can remain constant despite the change in the PVT, input jitter conditions at given operating frequency. Even if the operating frequency changes, the TDC gain in units of bit/UI maintains by the operating principle using fixed number of phase steps.

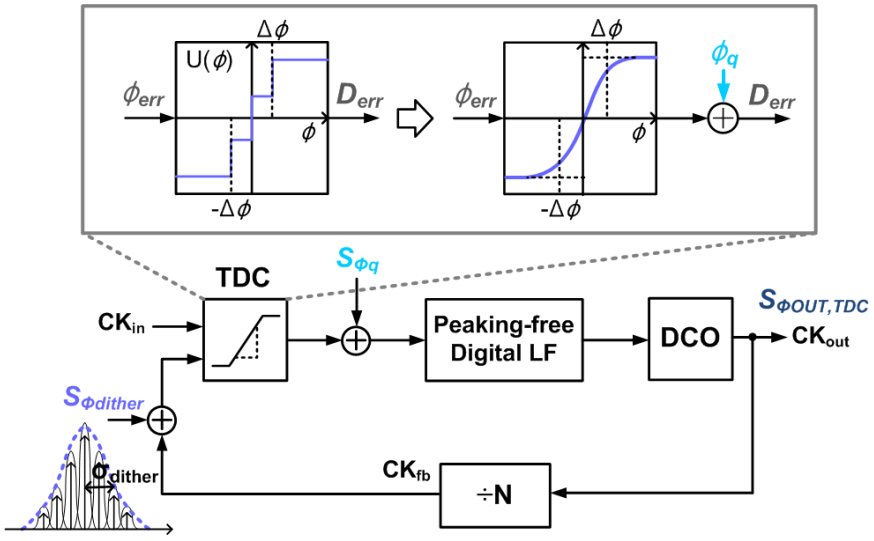
However, the dithering jitter and quantization noise of the oversampling TDC can degrade the overall phase noise performance of the PLL. Fig. 4.7(a) depicts the noise model to analyze these TDC-related noises. Using the pseudo-linear approach described in [41], the TDC is modeled as a linear gain element followed by an additive white noise source, where the effective linear gain $K_{TDC,eff}$ and the noise variance ϕ_q^2 can be derived using the following equations:

$$K_{TDC,eff} = \frac{E[\phi_{err} \cdot U(\phi_{err})]}{E[{\phi_{err}}^2]} = \frac{\int_{-\infty}^{+\infty} U(\phi_{err}) \cdot \phi_{err} \cdot f(\phi_{err}) d\phi_{err}}{\int_{-\infty}^{+\infty} {\phi_{err}}^2 \cdot f(\phi_{err}) d\phi_{err}} \quad (4.5)$$

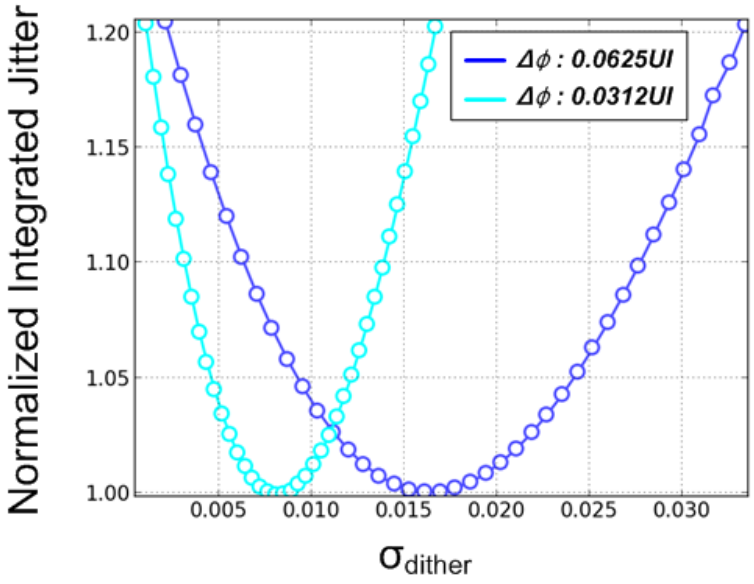
$$\begin{aligned} {\sigma_q}^2 &= E[U(\phi_{err})^2] - {K_{TDC,eff}}^2 \cdot E[{\phi_{err}}^2] \\ &= \int_{-\infty}^{+\infty} U(\phi_{err})^2 \cdot f(\phi_{err}) d\phi_{err} - {K_{TDC,eff}}^2 \int_{-\infty}^{+\infty} {\phi_{err}}^2 \cdot f(\phi_{err}) d\phi_{err} \end{aligned} \quad (4.6)$$

$U(\cdot)$ denotes the raw transfer function of the TDC and $f(\phi_{err})$ is the PDF of the phase error including the dither. Once this linearized TDC model is derived, the power spectral density (PSD) of the PLL output phase noise due to the TDC quantization noise (ϕ_q) and dither jitter (ϕ_{dither}) can be obtained:

$$S_{\phi_{OUT},TDC}(f) = \left(S_{\phi dither}(f) + S_{\phi q}(f) / {K_{TDC,eff}}^2\right) |H(f)|^2 \quad (4.7)$$



(a)



(b)

Fig. 4.7. (a) A PLL model for analyzing the noise contribution of the TDC quantization noise and dither jitter. (b) The normalized total integrated jitter.

Using Eq. (4.5)-(4.7), it can be shown that for a given BB-PFD phase spacing of $\Delta\phi$, there exists an optimal amount of dither jitter (σ_{dither}) that minimizes the contribution of the TDC-related noises to the output phase noise, $S_{\phi OUT,TDC}$. Fig. 4.7(b) plots the normalized integrated jitter of $S_{\phi OUT,TDC}$ as a function of σ_{dither} for the $\Delta\phi$ values of 0.0625 and 0.0312-UI when the PLL has a bandwidth of 750-kHz and damping factor of 1. The optimal σ_{dither} values are found to be 0.016 and 0.008-UI, respectively. When the high-frequency dither jitter is sufficiently filtered by the PLL bandwidth, the contribution of the quantization noise (ϕ_q) dominates over that of the dither jitter (ϕ_{dither}).

Chapter 5

PVT-Insensitive-Bandwidth PLL

In this section, a PVT-insensitive loop bandwidth PLL with a constant-gain TDC and a constant relative-gain LC-DCO will be introduced as an example corresponding proposed design concepts. Based on ratiometric circuit designs, the LC-DCO makes a fixed 0.011% change to its current frequency for a unit change in its digital input and the TDC can maintain a fixed range of –0.13~0.13-UI and fixed resolution of 0.00781-UI across PVT variations. With such DCO and TDC, the prototype digital PLL fabricated in a 28-nm CMOS technology operates over an 8.38~9.34-GHz frequency range and realizes a bandwidth which is a constant fraction of 0.00305±2.95% of the reference frequency across the whole range. Also, at 8.84-GHz, the PLL dissipates 15.2-mW, achieves 652-fs_{rms} integrated jitter from 10-kHz to 1-GHz, and has a nearly constant BW at 822-kHz with the worst-case deviation of only ±4.25% across three different die samples and the supply ranging from 1.0 to 1.2V.

5.1 Overview

Various standards for wireless and wireline communications require a phase-locked loop (PLL) that maintains a well-controlled loop bandwidth (BW) as well as low phase noise against process, voltage, and temperature (PVT) variations [1]. As explained in Section 3, PLL design parameters determining the loop characteristics are changed according to PVT and/or frequency conditions.

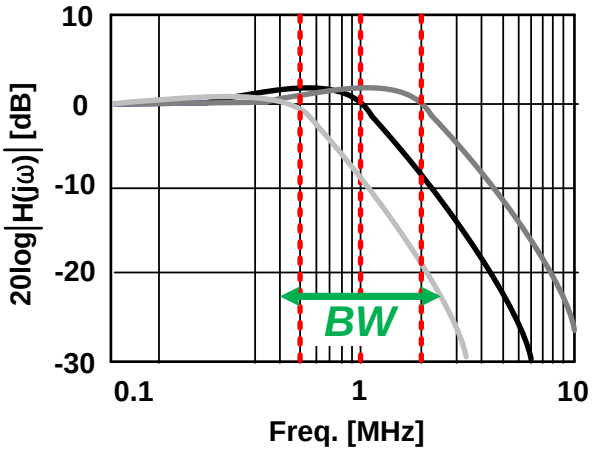


Fig. 5.1. The PLL loop bandwidth variation according to PVT conditions.

As shown in Fig. 5.1, in analog PLLs, the loop BW may vary due to PVT-sensitive circuit parameters such as the voltage-controlled oscillator (VCO) gain and charge pump (CP) current. Even in digital PLLs, the loop BW may deviate from its optimum value due to the variation in the digitally-controlled oscillator (DCO) gain and time-to-digital converter (TDC) gain. To suppress such undesired variation in the loop BW, this work presents a digital PLL that desensitizes the loop BW to PVT variations using a LC-DCO and TDC with constant gains at a given operating frequency.

5.2 Prior Works

Prior works have demonstrated that the PLL BW can be kept constant by adapting the loop parameters and compensating the variations in the oscillator characteristics [4]-[8].

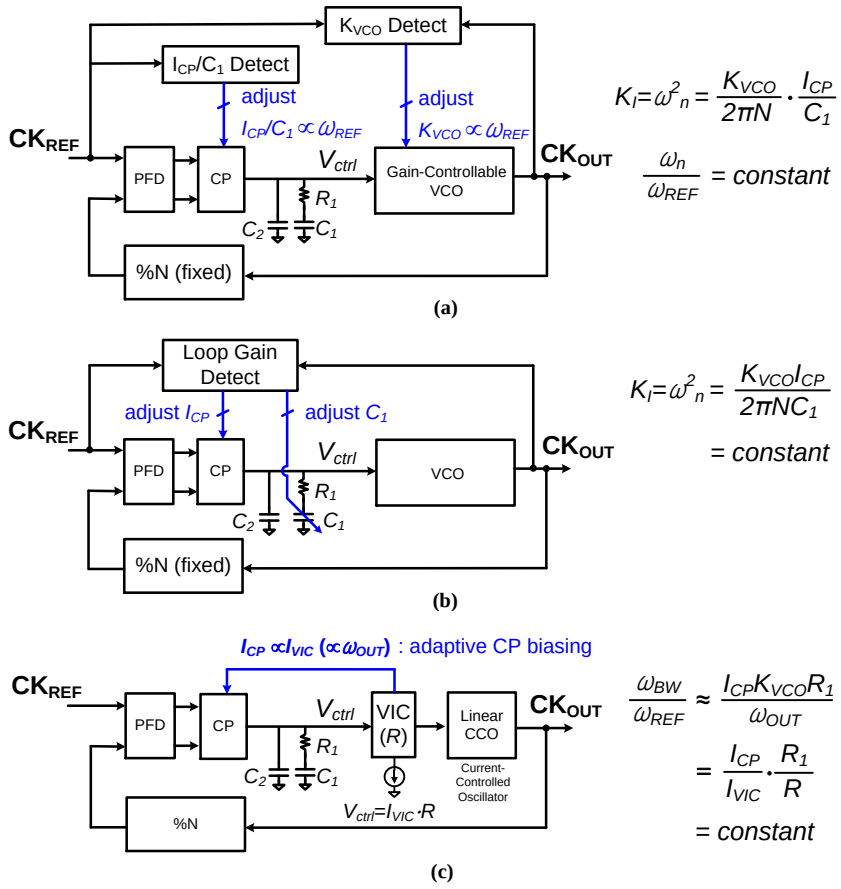


Fig. 5.2. The previously-reported PVT-insensitive loop BW PLLs: (a) BW tracking PLL via loop BW calibration [4], (b) constant loop BW PLL via loop BW calibration [5], [6], and BW tracking PLL via adaptive CP biasing [7], [8].

For instance, the PLLs presented in [4]-[6] employed a digital calibration scheme that measures the DCO or VCO gain and adjusts the TDC gain, CP current, or filter capacitor, accordingly. As shown in Fig. 5.2(a), a loop BW calibration is conducted for the constant natural frequency ω_n by calibrating the VCO gain K_{VCO} and the charge pump current I_{CP} over a loop filter capacitor C_1 (i.e., I_{CP}/C_1) in comparison with the reference frequency ω_{REF} [4]. As a result, it realizes not only process-independent ω_n at each operating frequency but also constant BW-to-frequency ratio i.e., ω_n/ω_{REF}=constant. The loop BW calibration in Fig. 5.2(b) adjusts the I_{CP} and C_1 to compensate for the loop gain variation. The constant natural frequency ω_n can be achieved by calibrating the charge pump current I_{CP} and loop filter capacitor C_1 by measuring the VCO gain or an integral path gain [5],[6]. However, one drawback of this approach is that the calibration is performed in foreground, requiring recalibration if the environmental conditions drift.

On the other hand, the PLLs in [7],[8] calibrate the BW in the background by maintaining a constant ratio between the currents of the charge pump and oscillator, as shown in Fig. 5.2(c). Since the ratio between the bandwidth ω_{BW} and reference frequency ω_{REF} is fixed by this current ratio, the BW can stay constant for a given operating frequency. However, it is becoming difficult to keep the current ratio constant over a wide operating range for deeply-scaled technologies as the supply voltage approaches near the device threshold.

To address these problems, this paper presents a digital PLL with a constant relative-gain LC-DCO and a constant-gain TDC, realizing a PVT-insensitive loop bandwidth without requiring any explicit calibration loop or additional components.

5.3 Proposed PVT-Insensitive-Bandwidth PLL

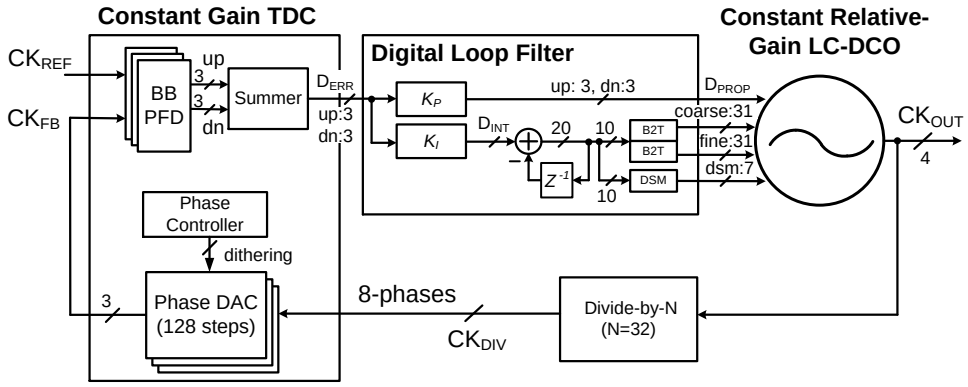


Fig. 5.3. The proposed digital PLL with PVT-insensitive loop bandwidth.

Fig. 5.3 illustrates the architecture of the proposed PLL, consisting of a TDC, a proportional-integral digital loop filter (DLF), an LC-DCO with quadrature phase outputs, and a divide-by-32 frequency divider. The key to achieving the PVT-insensitive loop BW without any calibration loop or adaptive CP biasing is the constant-gain TDC and the constant-relative-gain DCO. A constant-gain TDC provides a digitized measure of the phase error with a constant resolution measured in radians or UIs. In other words, the TDC gain in units of bits/UI stays constant over the PVT and frequency conditions. On the other hand, a constant-relative-gain DCO changes its frequency by a constant fraction of the current operating frequency ω_{OUT} in response to a unit step in its digital input:

$$\frac{\Delta\omega_{OUT}/\omega_{OUT}}{\Delta D_{IN}} = constant \quad (5.1)$$

That is, at a given operating frequency ω_{OUT}, which is fixed by the reference frequency and multiplication ratio of the PLL, the DCO has a constant gain, or equivalently a gain that scales proportionally with ω_{OUT}. The constant-gain TDC and constant-relative-gain DCO are realized by ratiometric designs, i.e. using circuits that rely only on relative ratios between identical elements, as explained in Section 4. Therefore, the characteristics of the TDC and DCO are fixed at the design stage and not affected by the change in the absolute parameters such as PVT variations or model uncertainties.

With a constant-gain TDC and constant-relative-gain DCO, a digital PLL can realize a bandwidth which is a constant fraction of the reference frequency even with a simple proportional-integral digital loop filter without any explicit calibration loops. It is well known that the loop BW ω_{BW} and damping factor ζ of a digital PLL are expressed as [20]:

$$\omega_{BW} \approx 2\zeta\omega_n = \frac{K_P K_{TDC} K_{DCO}}{N} \propto K_P K_{TDC} \omega_{REF} \quad (5.2)$$

$$\zeta = \frac{K_P}{2} \cdot \sqrt{\frac{2\pi K_{TDC} K_{DCO}}{K_I N \omega_{REF}}} \propto \frac{K_P}{2} \cdot \sqrt{\frac{2\pi K_{TDC}}{K_I}} \quad (5.3)$$

where K_P and K_I are the fixed proportional and integral gains of the DLF, respectively and K_{TDC} and K_{DCO} are the TDC and DCO gains, in units of bits/rad and rad/s/bit, respectively. These expressions imply that when K_{TDC} is constant and K_{DCO} is proportional to $\omega_{OUT} = N \cdot \omega_{REF}$, ω_{BW} will be a constant fraction of ω_{REF} and ζ will be constant. Therefore, at a given reference frequency ω_{REF}, which is typically well-

controlled, the digital PLL with a constant-gain TDC and a constant-relative-gain DCO will have a well-predicted loop BW insensitive to PVT variations.

5.4 Circuit Implementation

5.4.1 Capacitor-Tuned LC-DCO

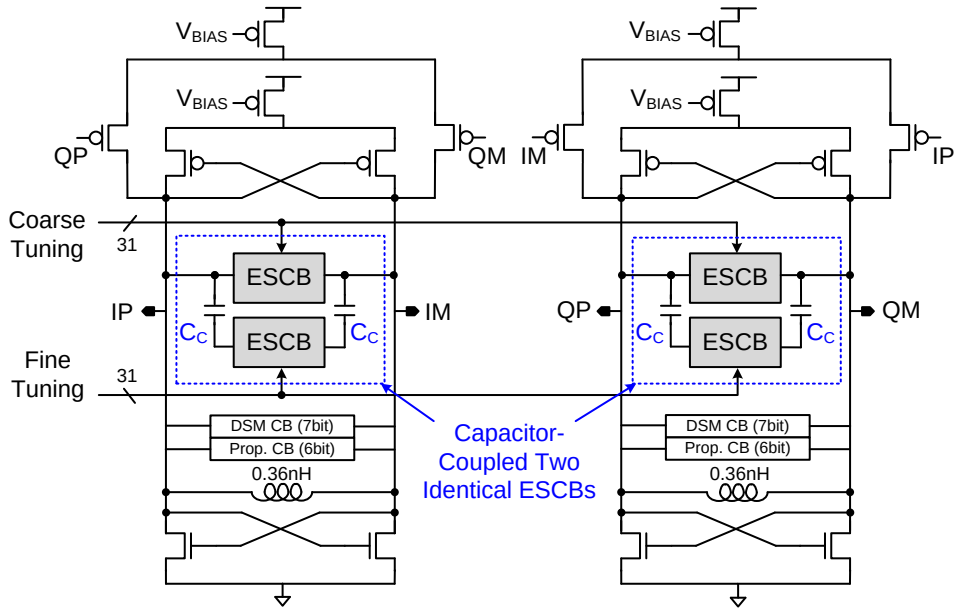


Fig. 5.4. The proposed constant relative-gain quadrature LC-DCO implemented with the capacitor-coupled two identical ESCBs.

Fig. 5.4 shows the overall schematic of the proposed constant relative-gain LC-DCO employing exponentially-sized capacitor banks (ESCBs) for frequency tuning [27]. The LC-DCO is composed of two coupled LC oscillator cores for quadrature phase generation and each core is composed of a 31-bit-thermometer-coded coarse

ESCB and a 31-bit-thermometer-coded fine ESCB for wide-range frequency tuning, a 6-bit-binary-coded capacitor bank (CB) for direct proportional control [21], and a 7-bit-binary-coded CB for a delta-sigma modulator (DSM) dithering. The fine ESCB is identical to the coarse ESCB except being coupled to the nodes IP(QP) and IM(QM) via series capacitors *Cc*. Adding this series capacitors *Cc* can improve the frequency resolution of the DCO without degrading the tuning range or phase noise [22].

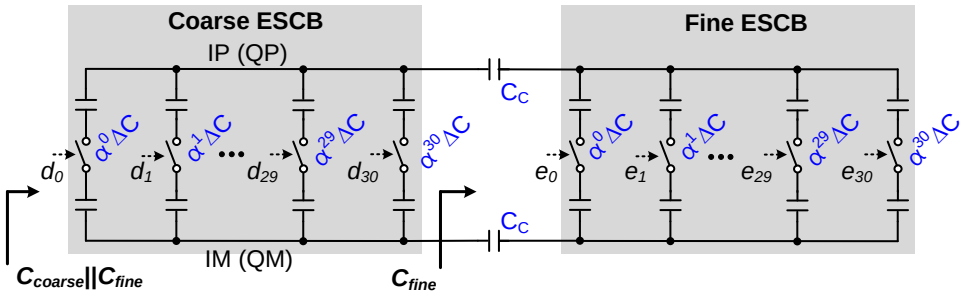


Fig. 5.5. Detailed schematic of the coarse and fine ESCBs.

As shown in Fig. 5.5, each ESCB consists of exponentially-sized switched-capacitors with a constant radix of α, so that the DCO frequency can change by a constant fraction of the current frequency set by α. Each CB is made of a set of parallel NMOS varactors and switches each of which shorts the internal node either to power or to ground. The switches are controlled by a 31-bit thermometer code d_0~d_{30} (for coarse ESCB) or e_0~e_{30} (for fine ESCB), which are generated from two binary-to-thermometer (B2T) encoders.

The coarse capacitance C_{coarse} and fine capacitance C_{fine} of the capacitor-coupled two identical ESCBs assuming $C_0 \gg \Delta C$ can be calculated as:

$$C_{coarse} = C_0 + T_C \cdot \Delta C \quad (T_C = d_o + d_1 \cdot \alpha^1 + \cdots + d_{30} \cdot \alpha^{30}) \tag{5.4}$$

$$C_{fine} = \frac{(C_0 + T_F \cdot \Delta C) \cdot \frac{C_C}{2}}{(C_0 + T_F \cdot \Delta C) + \frac{C_C}{2}} = \frac{\left(C_o + T_F \cdot \Delta C\right) \cdot \frac{C_C}{2C_0}}{1 + \frac{T_F \Delta C}{C_0} + \frac{C_C}{2C_0}} \approx \frac{C_C}{2} + T_F \cdot \Delta C \cdot \frac{C_C}{2C_0}$$

$$(T_F = e_o + e_1 \cdot \alpha^1 + \cdots + e_{30} \cdot \alpha^{30}) \tag{5.5}$$

Where ΔC is the unit capacitance and C_0 is the total fixed capacitance on the nodes *IP*(*QP*) and *IM*(*QM*).

Using the total capacitance $C_{total} = C_{coarse} + C_{fine}$, the constant relative gain *k* can be expressed as:

$$k = \frac{\omega_{n+1}}{\omega_n} = \sqrt{\frac{\left(C_0 + \frac{1-\alpha^{N_C}}{1-\alpha} \cdot \Delta C\right) + \left(\frac{C_C}{2} + \frac{1-\alpha^{N_F}}{1-\alpha} \cdot \Delta C \cdot \frac{C_C}{2C_o}\right)}{\left(C_0 + \frac{1-\alpha^{N_C}}{1-\alpha} \cdot \Delta C\right) + \left(\frac{C_C}{2} + \frac{1-\alpha^{N_F-1}}{1-\alpha} \cdot \Delta C \cdot \frac{C_C}{2C_o}\right)}} \approx 1 + \frac{\Delta C \cdot C_C}{2C_0^2} \tag{4}$$

where *n* is the 10-bit binary-coded index of the frequency control code ($n=2^5 N_C + N_F$). And, N_C (coarse) and N_F (fine) are upper and lower 5-bits, respectively. In the prototype design, the value of α is set to be 0.9958, which realizes a constant relative gain *k* of 1.00011 (=0.011%/step). At 8.4-GHz, it corresponds to a frequency resolution of 924-kHz. The capacitance *Cc* is sized to $C_0/16$ for seamless hand-over between the coarse and fine ESCB ranges. However, since this capacitance was implemented using metal-to-metal capacitors for their linearity instead of the MOS varactors used in the ESCBs, possible gain mismatch may exist due to their variations.

Each oscillator core uses a 364-pH symmetric-square planar inductor with a 25μm-wide, 2.225μm-thick top-metal layer, achieving a quality factor of 16 at 8-GHz with the total series resistance less than 1Ω as shown in Fig. 5.6.

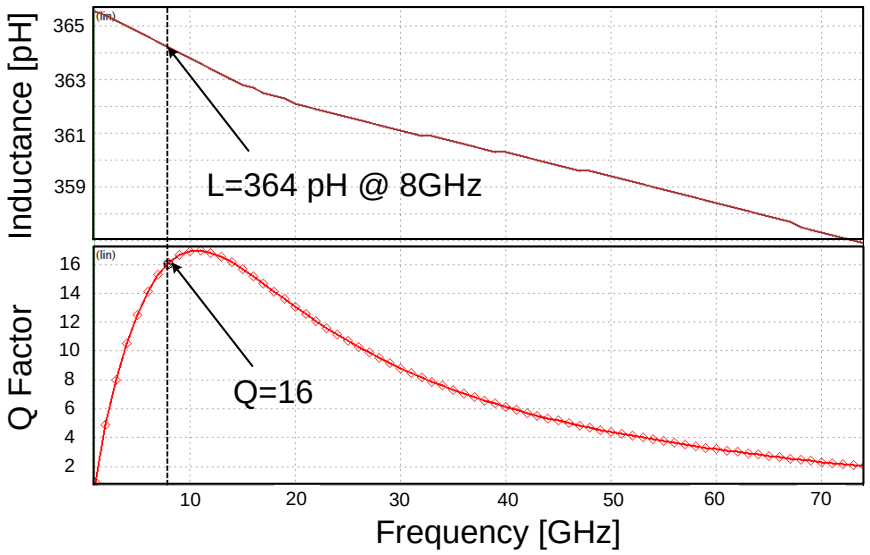


Fig. 5.6. Inductance and quality factor of the designed inductor.

As shown in Fig. 5.7, the proposed capacitor-tuned LC-DCO was designed to have a 10-bit resolution with a constant relative gain of 1.00011 (=0.011%/step) over an 8.4~9.3-GHz range, while dissipating 9.1-mW at the frequency of 9.3-GHz.

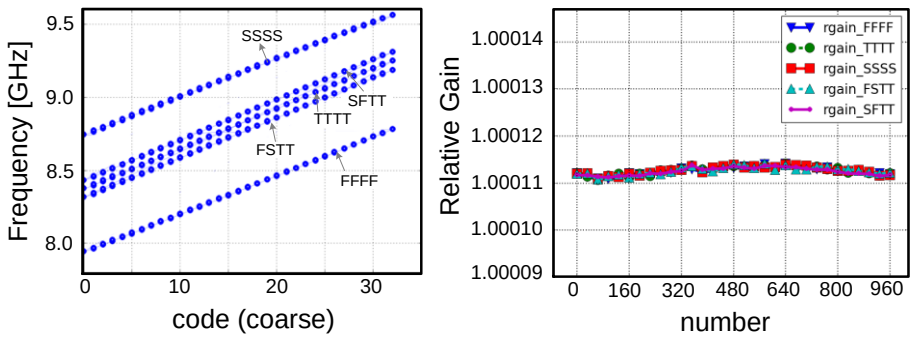


Fig. 5.7. Simulation results: (a) frequency tuning range and (b) relative gain at hand-over between the coarse and fine ESCB ranges (32-points).

In addition, the simulated phase noise of the LC- DCO at 8.9 GHz was -110.1-dBc/Hz at 1-MHz offset and -135-dBc/Hz at 10-MHz offset as shown in Fig. 5.8.

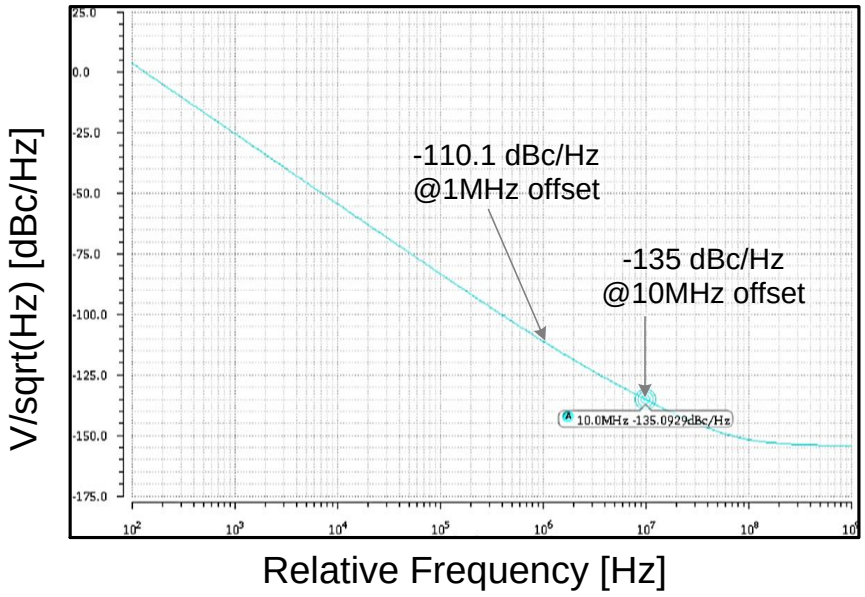


Fig. 5.8. Simulated phase noise at 8.9GHz.

5.4.2 Transformer-Tuned LC-DCO

As explained in Section 4, uncertainties in the DCO gain can make the precise control of the PLL's bandwidth and damping factor difficult. Sparing margins to accommodate these uncertainties may sacrifice the key performance metrics such as phase noise and power dissipation. To alleviate such a DCO gain variation, the LC-DCO that has constant relative-gain is proposed. The constant relative-gain is secured by the ratiometric circuit design, i.e., frequency is controlled by the ratio between two currents.

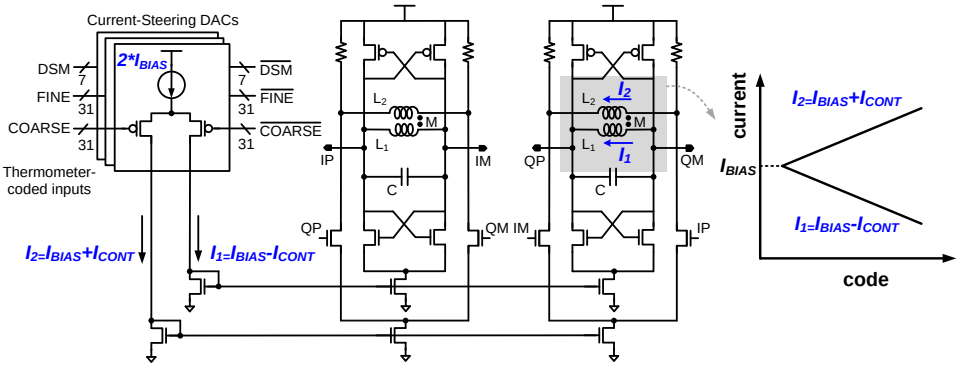


Fig. 5.9 Transformer-tuned (magnetically-tuned) LC-DCO.

Fig. 5.9 shows the schematic of the proposed transformer-based LC-DCO that realizes a predictable gain without the aid of an explicit calibration. The principle of the transformer-based frequency tuning is explained in [26]. The effective inductance of the primary inductor L_1 is tuned by adjusting the current flowing in the secondary inductor L_2. The two coupled LC oscillator cores enforce the necessary quadrature-phase relationship between the currents in the primary and secondary inductors, I_1 and I_2, respectively. The oscillation frequency ω_{OSC} can be expressed as:

$$\omega_{OSC} = \frac{\omega_0}{2Q}\cdot\frac{M}{L_1}\cdot\frac{I_2}{I_1} + \sqrt{\left(\frac{\omega_0}{2Q}\cdot\frac{M}{L_1}\cdot\frac{I_2}{I_1}\right)^2 + \omega_0^2} \quad (5.16)$$

where ω_0 is the LC tank's resonant frequency without the secondary inductor, Q is the quality factor, and M is the mutual-inductance of the transformer. Equation (16) shows that the oscillation frequency varies with the ratio I_2/I_1, which is controlled by a current-steering DAC.

The ratio I_2/I_1 using n-bit binary control can be expressed by:

$$\left(\frac{I_2}{I_1}\right)_n = \frac{I_{BIAS}+I_{CONT}}{I_{BIAS}-I_{CONT}} = \frac{1+\frac{n\Delta I}{I_{BIAS}}}{1-\frac{n\Delta I}{I_{BIAS}}} \approx e^{\frac{2\Delta I}{I_{BIAS}}\cdot n}$$

$$x = \frac{I_{CONT}}{I_{BIAS}} = \frac{n\Delta I}{I_{BIAS}} \quad (0 < x < 1) \quad (5.17)$$

Where I_{BIAS} and I_{CONT} are the fixed bias current and varying current by digital code, respectively.

The current-steering DAC adjusts the two currents I_1 and I_2 in a complementary fashion, realizing a pseudo-exponential D-to-*f* characteristic and a PVT-invariant relative gain of the DCO. When I_1 varies as $I_{BIAS}\cdot(1-x)$ and I_2 varies as $I_{BIAS}\cdot(1+x)$ where x is a tuning parameter, the ratio I_2/I_1 varies exponentially with x since $exp(2x) \cong (1+x)/(1-x)$ and so does the oscillation frequency according to Eq. (5.16). Therefore, for a unit change in the input code, the DCO frequency will change by a constant fraction of the current frequency, i.e., constant relative-gain of $exp(2\Delta I/I_{BIAS})$. The LC-DCO was designed to have a 10-bit resolution with a constant relative gain of 0.0064%/step over an 8.9~9.5-GHz range, while dissipating 51-mW at the frequency of 9.2-GHz. The simulated phase noise of the LC- DCO at 9.2 GHz was -91.2-dBc/Hz at 1-MHz offset and -120.9-dBc/Hz at 10-MHz offset.

However, the measured gain was 0.0047%/step due to the mis-estimation of the transformer's self- and mutual-inductances in presence of the routing wires.

Unfortunately, as discussed in Section 5, the designed DCO exhibits rather high phase noise and power dissipation compared to the state-of-the-art LC oscillators reported in literature and multiple reasons can be attributed to this. First, a half of the power dissipation is wasted on the second oscillator core generating the quadra-

ture-phase clocks required for the transformer-based tuning. While this was to generate precise quadrature clocks against PVT variation, it does incur more power than the alternative solution of using inverter-based 90-degree phase shifters [19]. Second, the frequency tuning was done by decreasing the main current I_1 while increasing the auxiliary current I_2, degrading the phase noise as the ratio I_2/I_1 increases. Furthermore, to ensure the proper start-up of the oscillator even with the lowest I_1, the overall current level had to be increased and energy-storing transistors had to be oversized, degrading both the power and phase noise. Lastly, the load resistors added in the outer loop to down-shift the voltage levels degraded the quality factor of the LC tank and added thermal noise while satisfying the voltage-rating requirement on the transistors.

In [20] with separate prototype, the transformer-tuning LC-DCO had a tuning range of 8.9~9.5-GHz and its phase noise was less than -120-dBc/Hz at a 10-MHz offset. The PLL with this LC-DCO consumed 63.9-mW in total and its majority, 51mW, was dissipated in the DCO. In addition, the PLL had -92.8-dBc/Hz phase noise at 1-MHz offset and -114-dBc/Hz phase noise at 10-MHz offset at 9.2-GHz.

5.4.3 Oversampling-Based Constant-Gain TDC

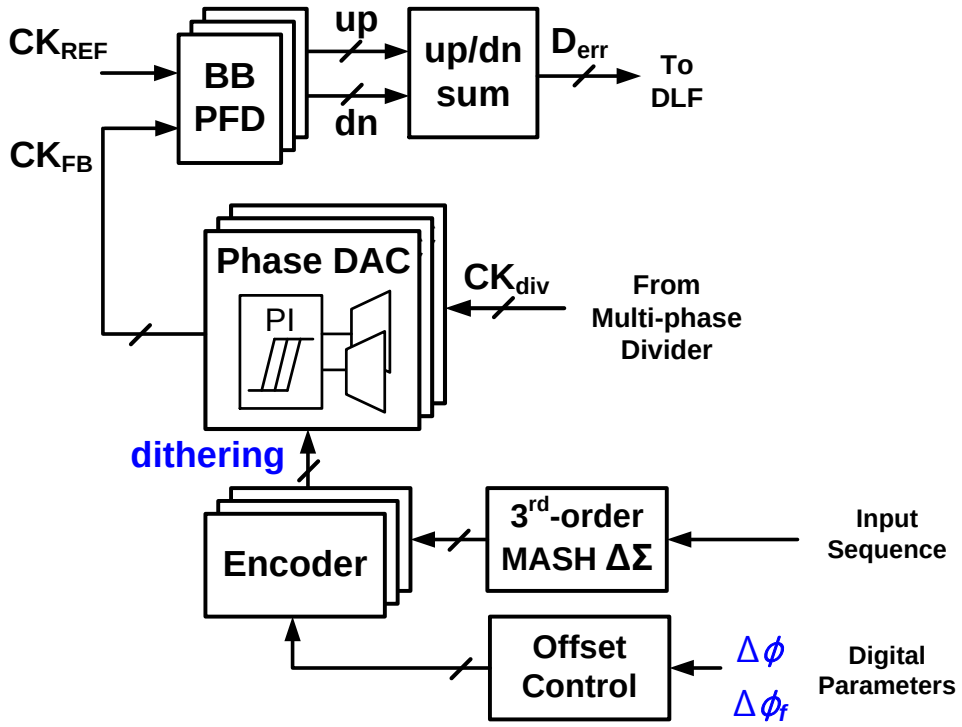


Fig. 5.10. The block diagram of the constant-gain TDC.

Fig. 5.10 shows the block diagram of the proposed TDC. A constant TDC gain which is independent of the PVT, input jitter, and frequency conditions is achieved by using three oversampling BB-PFDs triggered by individually dithered clocks using a set of phase digital-to-analog converters (DACs) and a 1-1-1 third-order multi-stage noise-shaping (MASH) DSM. The DSM generates a random dithering sequence whose noise power is shaped into a high frequency range by using the mini-

mum fractional value possible as the input [23]. Each phase DAC then converts the sequence into a dithering clock with a unit phase step size of $\Delta\phi_f$ and a phase offset of -$\Delta\phi$, 0, or +$\Delta\phi$.

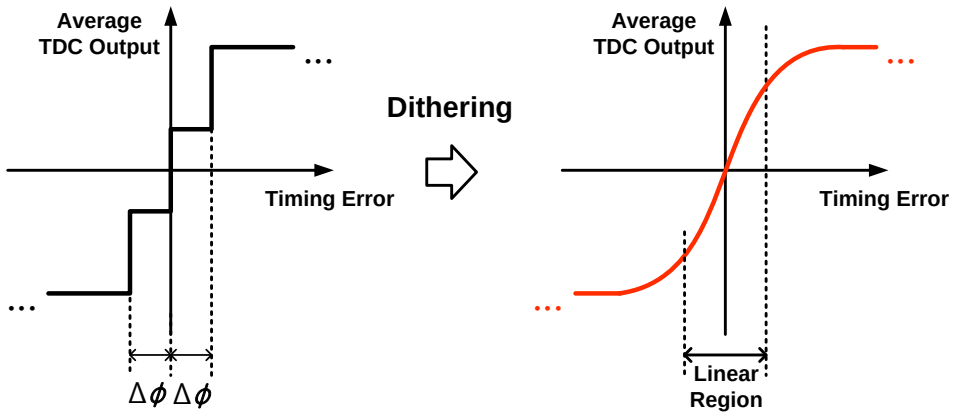


Fig. 5.11. Linearization of the TDC with the addition of random dither.

The TDC linearization principle is illustrated in Fig. 5.11. With a sufficiently large dither, the overall TDC characteristic becomes a straight line whose slope is determined largely by the phase spacing between the BB- PFDs. Since this phase spacing is set as a fixed fraction of the clock period by the use of phase-interpolating DACs, the slope, corresponding to the effective TDC gain, will remain unchanged despite the change in the PVT, input jitter, and frequency conditions.

Both the dither jitter step ($\Delta\phi_f$) and phase offset ($\Delta\phi$) are digitally programmable in units of PI resolution steps via an external I^2C interface. When the up/down counter tallies the BB-PFD outputs (*up* and *dn*) over multiple input cycles, the difference in their counts indicates the digitized phase error (D_{err}).

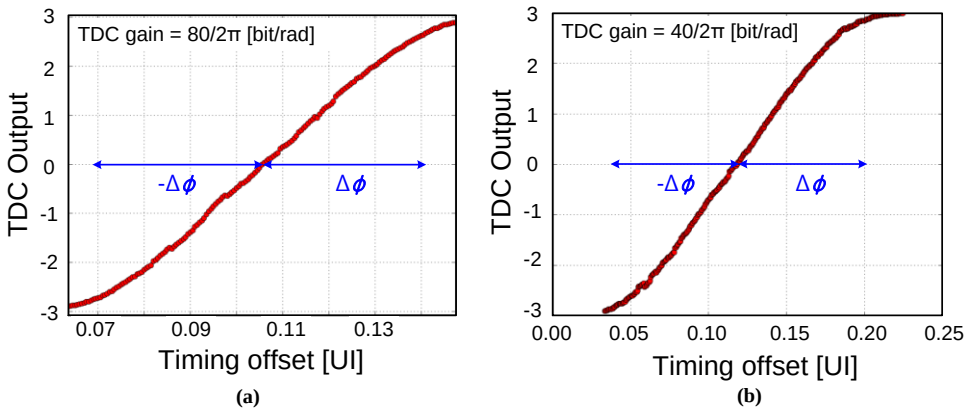


Fig. 5.12. Simulated effective TDC gain: (a) when $\Delta\phi$=0.037 UI and (b) when $\Delta\phi$=0.083 UI.

Fig. 5.12 plots the simulated TDC gain when the phase offset is set by $\Delta\phi$=0.037 UI and $\Delta\phi$=0.083 UI at 280 MHz frequency. The input clock has 1-ps_{rms} jitter. Thus, simulated TDC gains are $80/2\pi$=12.7 [bit/rad] and $40/2\pi$=6.36 [bit/rad], respectively. From these,), the effective TDC gain is determined mainly by $\Delta\phi$, which can stay constant regardless of the PVT and input jitter conditions. Even if the operating frequency changes, the TDC gain in units of bit/UI stays constant.

5.4.4 Phase Digital-to-Analog Converter

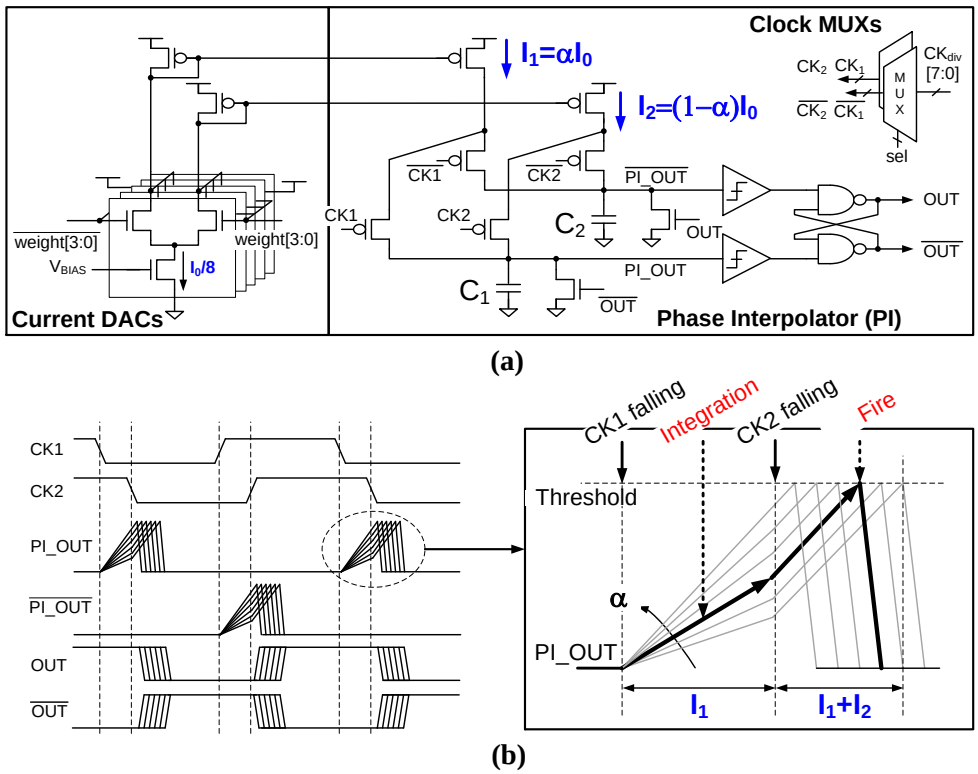


Fig. 5.13. (a) Circuit implementation of phase-domain DAC. (b) Operating waveform of phase interpolator (PI).

Fig. 5.13(a) shows the phase DAC circuit which is a set of two multiplexers followed by a digitally controlled phase interpolator (PI). Fig. 5.13(b) illustrates the operation of the PI, of which main advantage over the other published ones is that there is no contention between the two driving stages, saving power dissipation due to crowbar currents. The basic circuit topology is similar to the one in [25], except that two complementary stages work in an alternating fashion to interpolate both the

rising and falling edges of the input clocks. In each stage, two switched current sources each biased at I_1 and I_2 charge a shared capacitor when the respective input clocks (*CK1* and *CK2*) fall low. It then gives rise to a ramp signal on the node *PI_OUT*, which toggles the output clock *OUT* when *PI_OUT* crosses the threshold of a Schmitt-trigger type comparator. It can be shown that the interpolation weight α between the two input phases can be adjusted by controlling I_1 and I_2 as $\alpha \cdot I_0$ and $(1-\alpha) \cdot I_0$, respectively, using a 4-bit binary-coded current-steering DAC. The implemented phase DAC dissipates only 102 μW, whose output spans the entire 360° range with a resolution of 2.8125° (128-steps).

Fig. 5.14(a) shows the simulated transfer characteristic of the phase DAC with input code from 0 to 31. Fig. 5.14(b) shows that the phase DAC was designed to have a DNL less than 0.5 LSB.

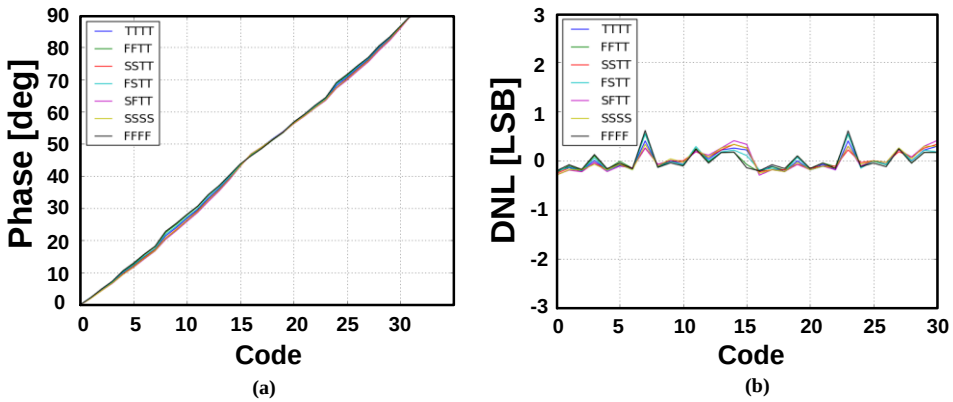


Fig. 5.14. Simulated results: (a) transfer characteristic of the phase DAC and (b) differential nonlinearity (DNL).

5.4.5 Digital Loop Filter

Thanks to the constant-relative-gain DCO and constant-gain TDC, the digital loop filter (DLF) used in the proposed PVT-insensitive loop BW PLL is a simple one that has proportional and integral paths. The proportional path updates the DCO input code by a factor of K_P, so that corrects the phase error. The integral path corrects the frequency error by updating DCO input code with the amount of time integral of the phase error, multiplied by K_I.

In order to realize the loop BW determined and scaled solely by the ω_{REF}, the constant-relative-gain DCO changes its frequency by a constant fraction of the current operating frequency ω_{OUT} in response to a unit step in its digital input. That is, $(\Delta \omega_{OUT}/\omega_{OUT})/\Delta D_{in}$ is always constant. Therefore, the DLF only need to update the DCO input code proportional to the phase error in entire frequency range without explicit calibration.

Unlike the constant-relative-gain DCO, conventional linear D-to-*f* DCO as explained Section 4.1 changes its frequency by a constant quantity in response to a unit step in its digital input, i.e., constant gain $(=\Delta\omega_{OUT}/\Delta D_{in})$. So, $(\Delta\omega_{OUT}/\omega_{OUT})/\Delta D_{in}$ is decreased with respect to the increase of ω_{OUT}. To scale the loop BW proportional to the ω_{REF} in whole tuning range, explicit calibration is inevitable in the digital loop filter [3].

5.4.6 Frequency Divider

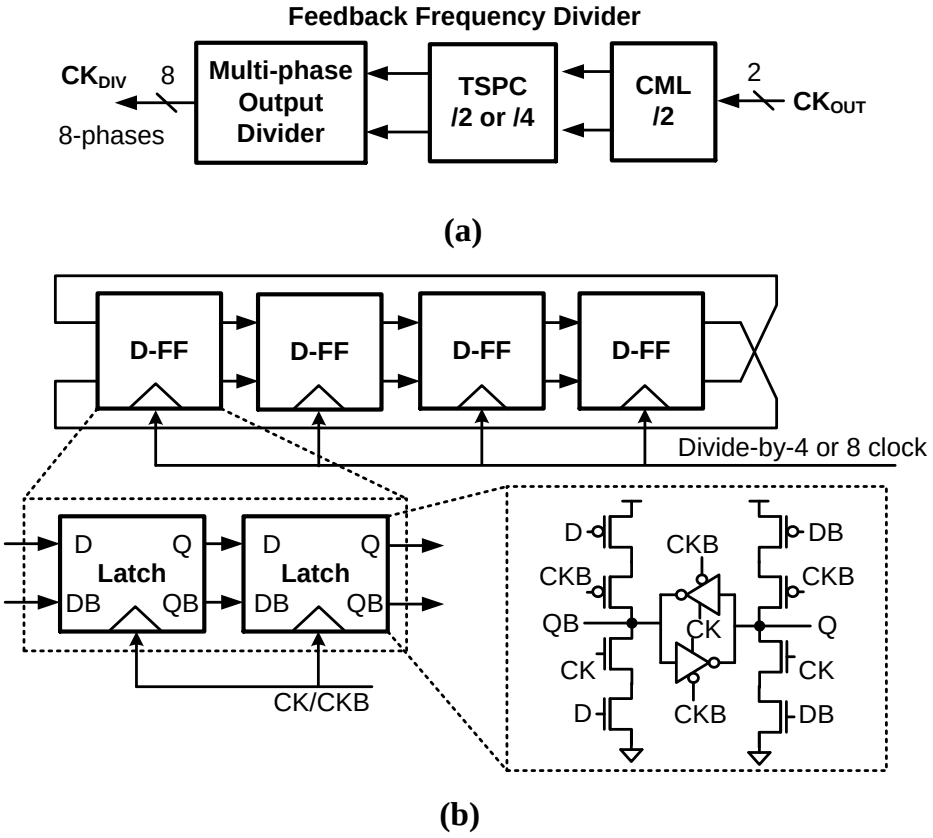


Fig. 5.15. (a) Feedback frequency divider with division ratio of 4 or 8. (b) 8-phase output divider.

Fig. 5. 15(a) shows the configuration of feedback frequency divider. It receives a differential input clock from the LC-DCO and generates 8-phase clocks. The total division ratio is 32 or 64. It is composed of a current-mode logic (CML) divider (/2), a true single phase clock (TSPC) divider (/2 or /4), and a multi-phase output divider. The multi-phase output divider in Fig. 5.15(b) consists of cascaded four differential sense-amplifier-type D-FFs with ring topology. This ring topology enables the di-

vider to generate 8-phase clocks with division ratio of eight. The feedback frequency divider was designed to have 10-GHz operating frequency, while dissipating 4.5 mW.

5.4.7 Bang-Bang Phase Frequency Detector

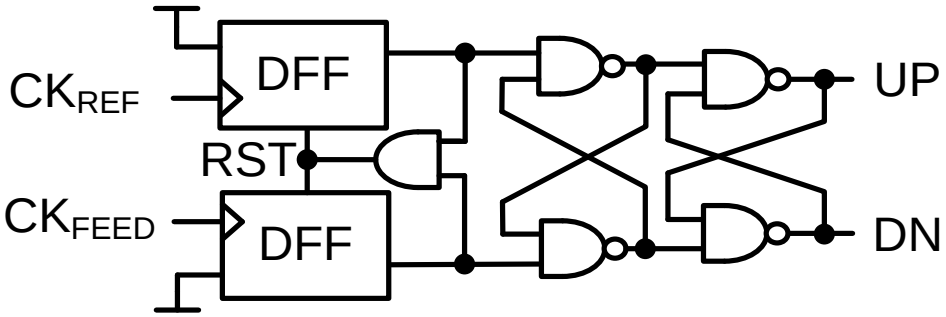


Fig. 5.16. Schematic of BB-PFD.

Fig. 5.16 shows the BB-PFD circuit which is basically a linear PFD followed by two cascaded SR-latches [24].

5.5 Cell-Based Design Flow

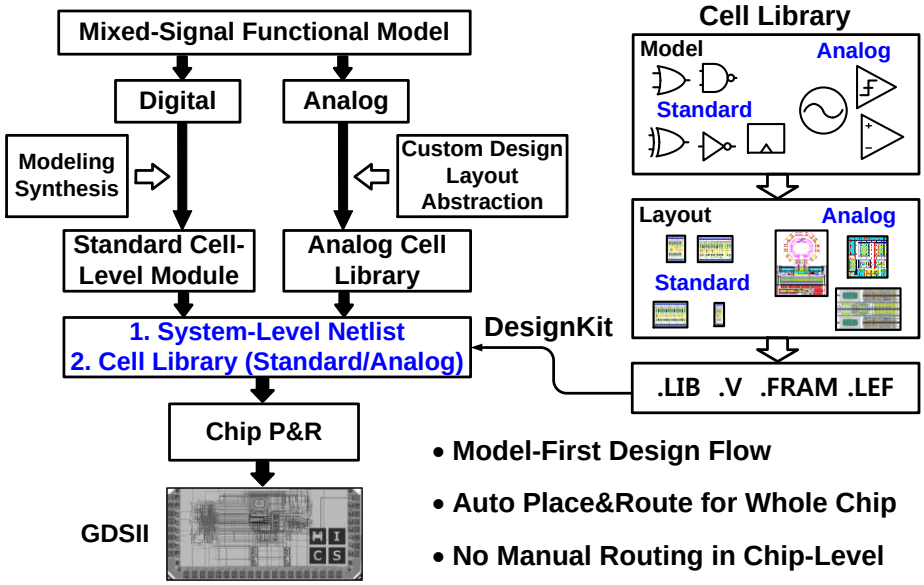
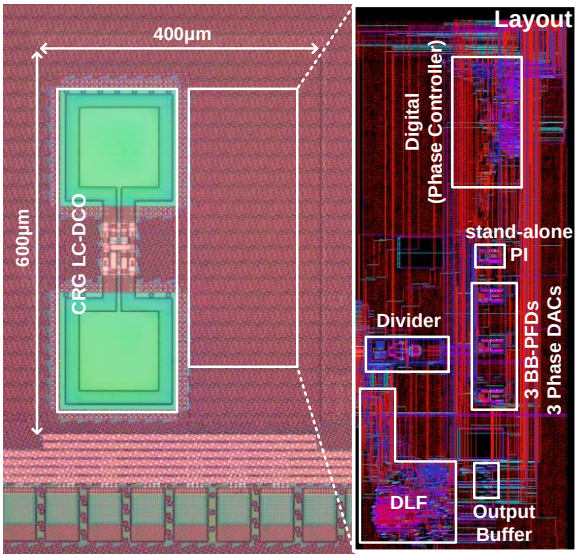


Fig. 5.17. Cell-based design flow.

The prototype chip was made by the cell-based design flow similar to the digital design flow as shown in Fig. 5.17. Basically, this flow starts from the mixed-signal functional model which is built with the Verilog model. Digital blocks prepared from the modeling and synthesis is described by the standard cell-level module. Then, analog blocks prepared from the circuit design, layout, and abstraction are organized as analog cell library. As you can find in the right figure, cell library includes both standard and analog cells. Because we make the same design-kit describing two kinds of cells, the standard and analog cells are same with respect to the place and route (P&R) tool. Key is that the analog cells are well drawn to satisfy the requirements as standard cells. Finally, P&R tool can place and route for the whole chip. In addition, we don't need to use manual routings in chip-level.

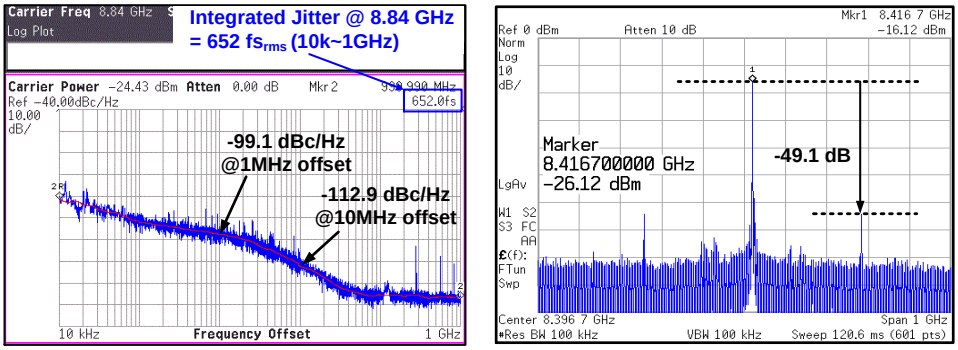
5.6 Measurement Results



Technology	28nm 1P10M Logic CMOS
Supply Voltage	1.0 – 1.2 V
Input Frequency	261.8 – 291.8 MHz
Output Frequency	8.38 – 9.34 GHz (10.83%)
Loop BW Variation	822 kHz ± 4.25 % @ 8.84 GHz
Integrated Jitter	652 fs_{rms} @ 8.84 GHz
PLL Phase Noise @ 1MHz offset	-103.2 dBc/Hz @ 8.5 GHz -99.1 dBc/Hz @ 8.84 GHz -97.3 dBc/Hz @ 9.3 GHz
PLL Phase Noise @ 10MHz offset	-118.9 dBc/Hz @ 8.5 GHz -112.9 dBc/Hz @ 8.84 GHz -112.3 dBc/Hz @ 9.3 GHz
Jitter FoM ($=10\cdot\log[\sigma_{rms}^2\cdot P(mW)]$)	-232 dB
Reference Spur	-49.1 dB
Power Dissipation	15.2 mW
Active Area	0.24 mm^2

Fig. 5.18. Chip micrograph and performance summary.

The prototype IC of the described PLL is fabricated in a 28nm CMOS technology and its die micrograph and performance summary are shown in Fig. 5.18. The PLL consumes an active area of 0.24 mm^2 and total power of 15.2-mW while operating at 1.0-V nominal supply. The DCO has a nominal resolution of 10-bits and achieves a 10.83% tuning range from 8.38 to 9.34-GHz. At the output frequency of 8.84-GHz and reference frequency of 276.25-MHz, the PLL has an integrated jitter from 10 kHz to 1 GHz of 652-fs_{rms} and phase noise of -99.1-dBc/Hz at 1-MHz offset and -112.9-dBc/Hz at 1-MHz offset as shown in Fig. 5.18. Also, the measured reference spur was -49.1-dBc.



(a) **(b)**

Fig. 5.19. Measured results of the PLL: (a) PLL phase noise and RMS integrated jitter and (b) power spectrum.

Fig. 5.20 shows the measured characteristics of the fabricated LC-DCO, showing its constant relative-gain against process and voltage variations. The relative gain of the DCO is measured across the entire frequency range from 8.38 to 9.34-GHz for three different die samples and for three different supply levels of 1.0, 1.1, and 1.2V. The measurement results in Fig. 5.20(a) and (b) demonstrate a nearly constant relative gain of 1.000111 with only ±4.4-% variation, which is very close to the design target of 1.00011 with α=0.9958. In fact, the variation in the DCO relative gain is mainly due to the gain mismatch between the coarse and fine ESCBs (e.g. the *Cc* mismatch) and is virtually insensitive to the die and voltage differences. On the other hand, the measured phase noise of the stand-alone DCO at 8.568 GHz was -108-dBc/Hz at 1-MHz offset and -125.6-dBc/Hz at 10-MHz offset, as shown in Fig. 5.20(c). The measured figure-of-merit with tuning range (FoM_T) was calculated as -180 dBc, i.e., $FoM_T = PN - 20 \cdot log\{(f_0/\Delta f) \cdot (FTR/10\%)\} + 10 \cdot log(Power/1mW)$.

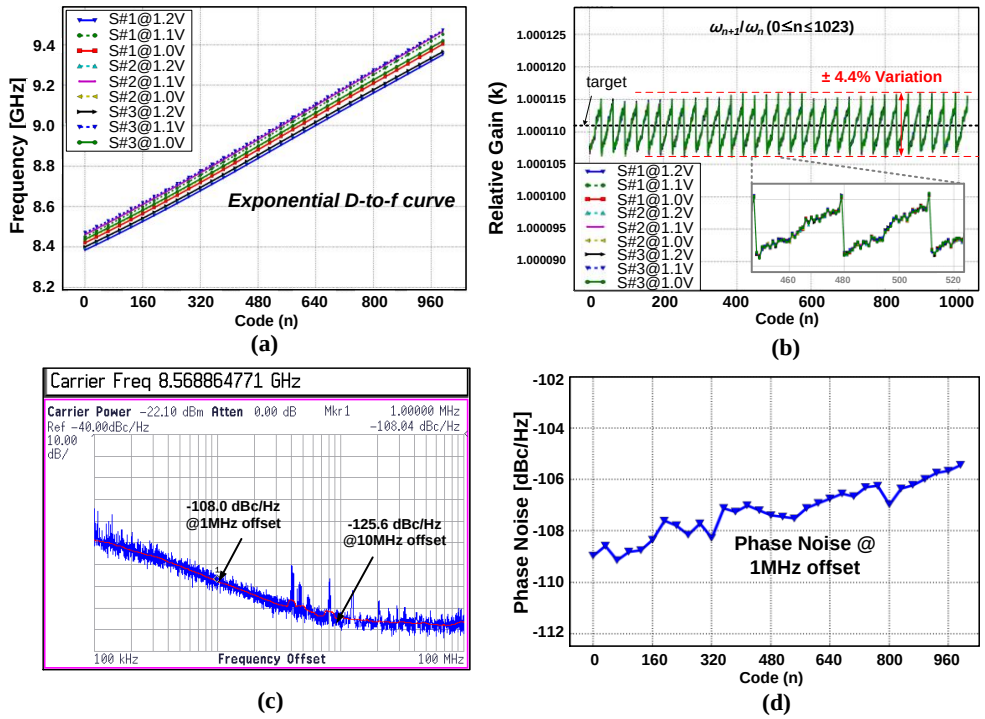


Fig. 5.20. Measured results of the LC-DCO: (a) exponential digital-to-frequency (D-to-f) curve, (b) relative gain versus input digital code with target value, (c) LC-DCO phase noise, and (d) phase noise according to frequency.

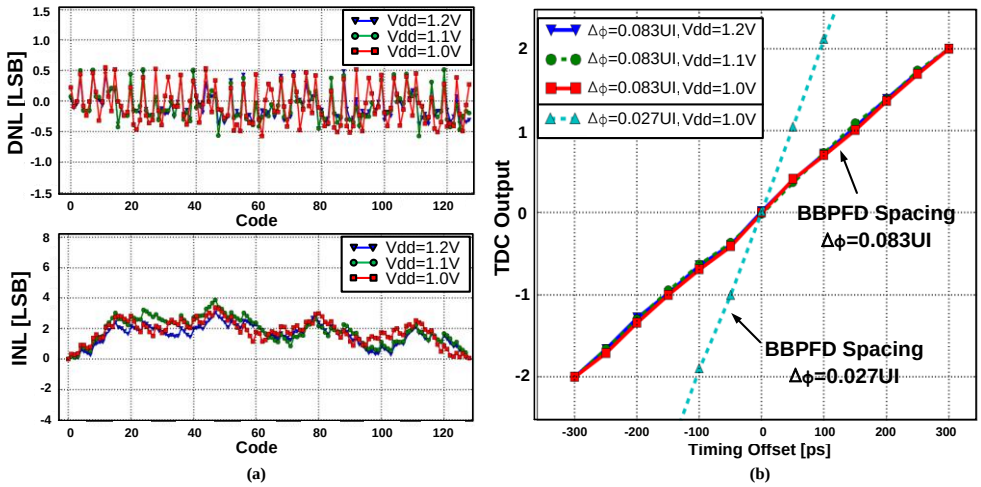


Fig. 5.21. Measured results of the TDC at 280MHz: (a) DNL and INL of the phase interpolator (PI), (b) TDC transfer across supply voltage and phase spacing.

Fig. 5.21 plots the measured differential and integral nonlinearity (DNL/INL) of the PI and the TDC transfer curve over supply voltage and phase spacing, showing its constant linear transfer characteristic at 280-MHz reference frequency. The TDC transfer curve is measured using a BIST circuit, which adds a fixed number to the TDC output D_{ERR} while the PLL feedback is closed. The resulting static phase offset of the PLL then indicates the input phase error for which the TDC yields the applied number. With a BB-PFD phase spacing ($\Delta\phi$) of 0.083 UI, the TDC has a constant gain of 12.7 bit/rad across three voltage conditions. When $\Delta\phi$ is changed to 0.027 UI, the TDC gain increases to 39.8-bit/rad, demonstrating that the TDC gain is mainly controlled by $\Delta\phi$.

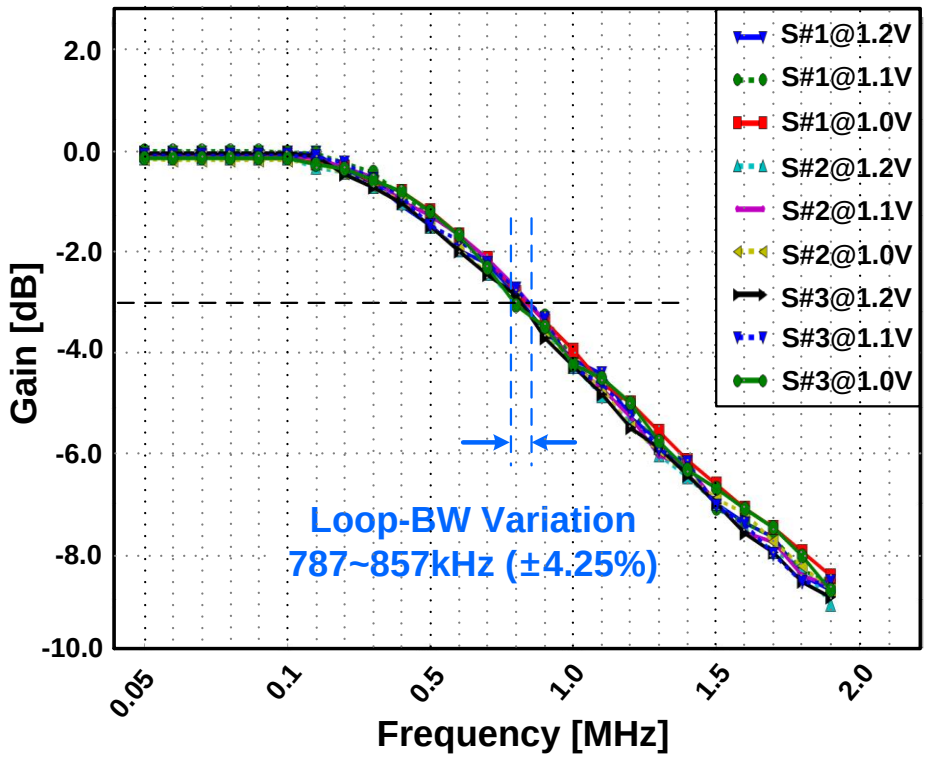


Fig. 5.22. Measured loop transfer function on three samples and three different supply voltages.

Fig. 5.22 demonstrates that the constant-relative-gain DCO and constant-gain TDC indeed achieve a digital PLL with PVT-insensitive loop BW and phase noise. The measured loop BW was nearly constant at 822-kHz with the variation of ±4.25% across the supply ranging from 1.0 to 1.2V and three different die samples at 8.84 GHz.

As shown in Fig. 5.23, the measured phase noise at 1-MHz and 10-MHz offset across supply variation was also constant as expected. In addition, the nearly constant BW-to-frequency ratio of 0.00305 with the variation of ±2.95% was measured.

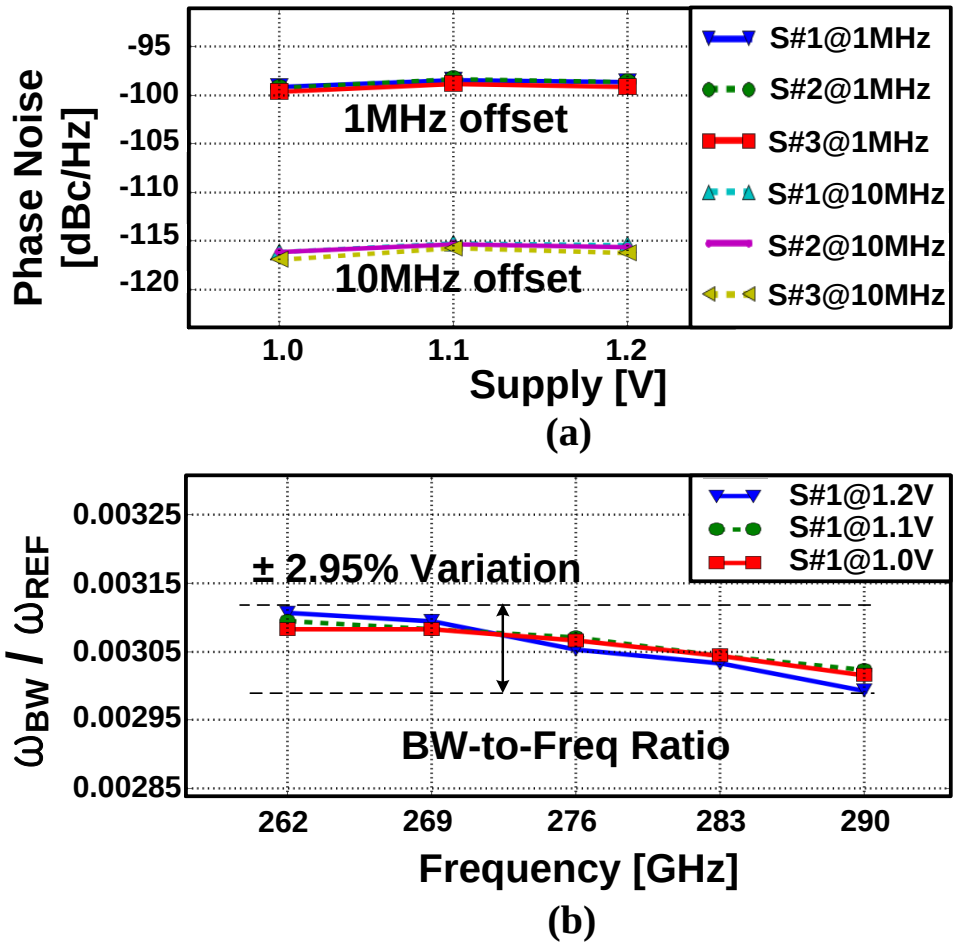


Fig. 5.23. (a) Measured phase noise variations. (b) loop BW to reference frequency ratio.

Fig. 5.24 shows the measured phase noise at 4.4 GHz divide-by-2 output clock for three different temperatures of 0°C, 25°C, and 80°C. The loop BW and damping factor were unchanged with three temperature conditions. It indicates that the proposed PLL had nearly same transfer characteristic over temperature variation without any explicit calibration.

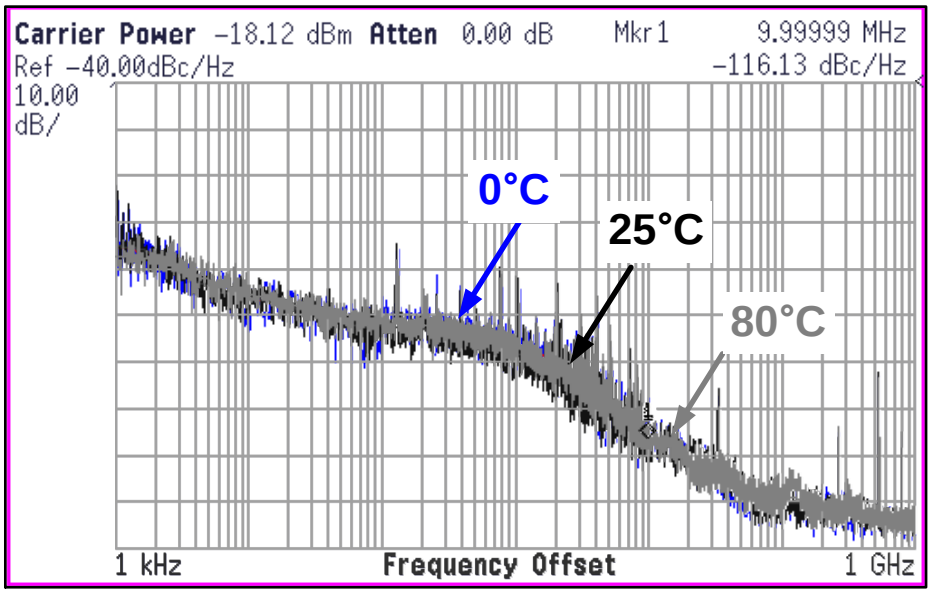


Fig. 5.24. Measured phase noise for three different temperatures.

	This Work	ISSCC07 Jung [8]	JSSC09 Wu [7]	JSSC14 Ryu [20]	JSSC12 Shin [5]	JSSC13 Ferriss [6]	ISSCC11 Rong [42]	JSSC15 Hekmet [43]
Oscillator Type	**Quad. LC-DCO**	Ring-VCO	LC-VCO	**Quad. LC-DCO**	LC-VCO	LC-VCO	**Quad. LC-VCO**	**8-phase LC-DCO**
PVT-insensitive Loop BW	Yes (Background: No Calibration)				Yes (Foreground Cal.)		No	
Integrated RMS Jitter [fs] (integration range: Hz)	652 (10k-1G)	5690	–	1200 (10k-100M)	–	–	–	394 (1k-100M)
Phase Noise@1MHz [dBc/Hz]	-99.1	–	-110.4	-92.8	-111.5	–	-100	-102
Phase Noise@10MHz [dBc/Hz]	-112.9	–	-129	-114	–	-126.7	-113	–
Output Frequency [GHz]	**8.38-9.34**	0.5-2	3.1-3.9	**8.9-9.5**	1.9-3.8	20.1-26.7	**8.4-12**	21.4-25.1
Tuning Range [%]	10.83	120	22.8	6.52	66.6	28.2	35.2	15.9
Reference Frequency [MHz]	261.8-291.8	4	16	143.75	40	195.3125	–	390
Power Dissipation [mW]	**15.2**	1.2	**48**	**63.9**	**15.3**	**33**	80	64
Figure of Merit (FoM*) [dB]	**-232**	-224.1	**–**	-220.3	**–**	**–**	–	-230
Supply Voltage [V]	1	1	1.5	1.2	1.2	1	1.2	1
Area [mm^2]	**0.24**	0.02	1.5	0.374	0.651	1.096	3	0.1
Technology [nm]	28	90	130	65	130	32 (SOI)	130	40

***FoM = 10·log[σ_{rms}^2·P(mW)]**

Table 5.1. Performance comparison of the proposed PVT-insensitive loop BW PLL with prior arts.

Table 5.1 compares the key performance metrics of the proposed PLL with the previous works. The proposed calibration-free LC-PLL with PVT-insensitive loop BW exhibits low power consumption and good figure-of-merit (FoM), in comparison with the other LC-PLLs having PVT-insensitive loop BW [5], [6], [7], [20]. Even comparing with the LC-PLLs with multi-phase outputs in similar frequency band [42], [43], the presented PLL exhibits comparable performance.

Chapter 6

Chirp Frequency Synthesizer PLL

In this section, a chirp frequency synthesizer PLL with calibration-free two-point modulation (TPM) using the proposed design concepts will be introduced as second example. The proposed chirp PLL achieves PVT-insensitive chirp profile for X-band FMCW radar for imaging with the constant-gain TDC and TPM with polarity-alternating second-order digital loop filter. A prototype IC fabricated in a 65nm CMOS demonstrates that the PLL can generate a precise triangular chirp profile centered at 8.9-GHz with 940-MHz bandwidth and 28.8-μs period with only 1.9-MHz_{rms} frequency error including turn-around points and 14.8-mW power dissipation. The achieved 32.63 MHz/μs chirp slope is higher than that of FMCW PLLs previously reported by 2.6×.

6.1 Overview

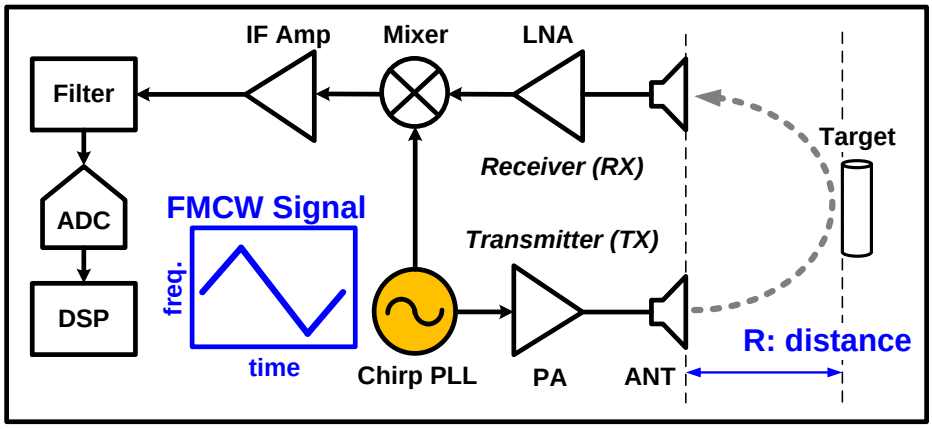


Fig. 6.1. FMCW Radar transceiver.

FMCW radar is a system where a frequency modulated continuous wave energy is transmitted and then received from the target, as shown in Fig. 6.1. The frequency of the FMCW signal goes up and down during the fixed period [29]. This radar is mainly used in adaptive cruise control, through-wall detection, and so on. Design target in this section is the implementation of the chirp frequency synthesizer PLL for the short range radar.

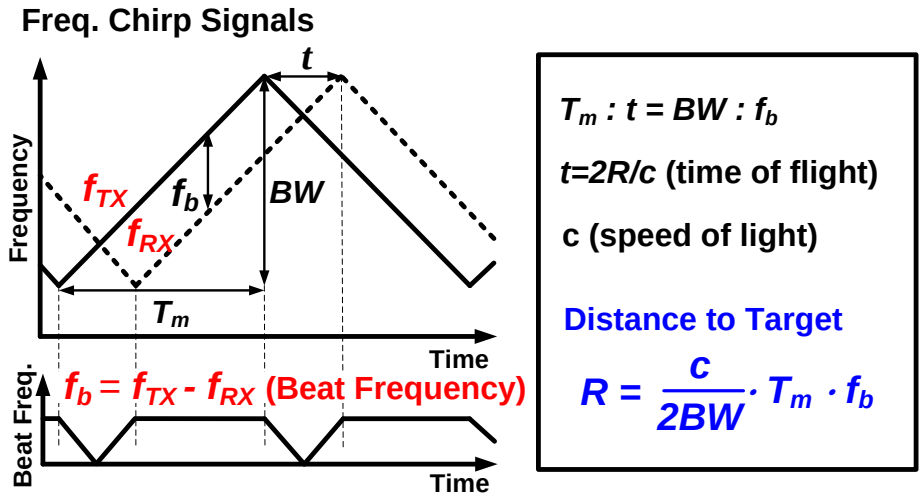


Fig. 6.2. FMCW Radar operating principle.

Fig.6.2 introduces the FMCW radar principle. To obtain the distance to the target, a frequency difference between the transmitted and received signals should be determined. The frequency difference is detected by the homodyne receiver in which the transmitted signal is mixed with the received signal [29]. This frequency difference is called beat frequency f_b. In the distance equation in Fig. 6.2, BW means the chirp bandwidth and T_m means the chirp period. Distance is proportional to the beat frequency f_b. For high-resolution, short-range FMCW radar, a chirp PLL which have a wide bandwidth and short period is required. In recent CMOS process, a flicker noise corner which means the intersection between thermal noise and flicker noise is getting larger than 1MHz. To obtain a 15cm range resolution ΔR within 15m distance, the beat frequency should be larger than this flicker noise corner. Therefore, linear frequency chirp with fast chirp slope ($=BW/T_m$) over 7.5MHz/us is required to obtain 15cm range resolution.

$$\frac{\Delta R}{\Delta f_b} = \frac{c \cdot T_m}{2BW} \propto \frac{1}{BW/T_m} \quad (6.1)$$

Ideally, fast chirp slope is intended to realize better range resolution in frequency chirp. However, three nonlinearities, such as nonlinear chirp, overshooting at turn-around, and stair-like chirp will be occurred as shown in Fig. 6.3. These nonlinearities in fast frequency chirp result in errors when measuring the distance.

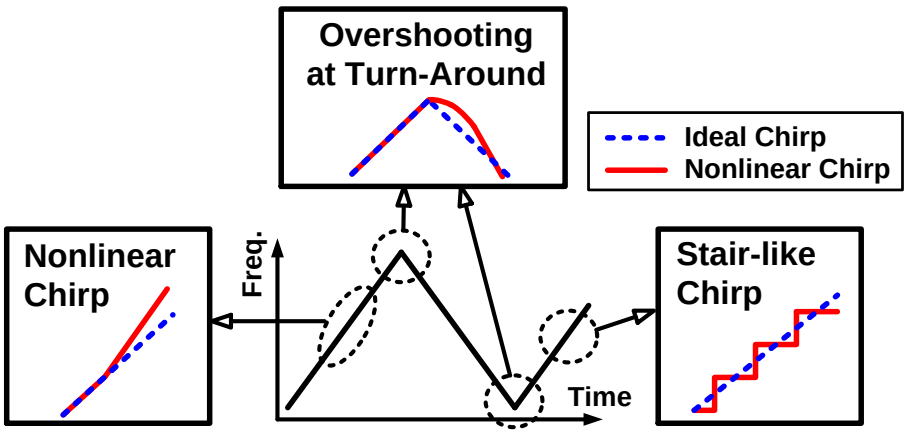


Fig. 6.3 Nonlinearity on the frequency chirp profile.

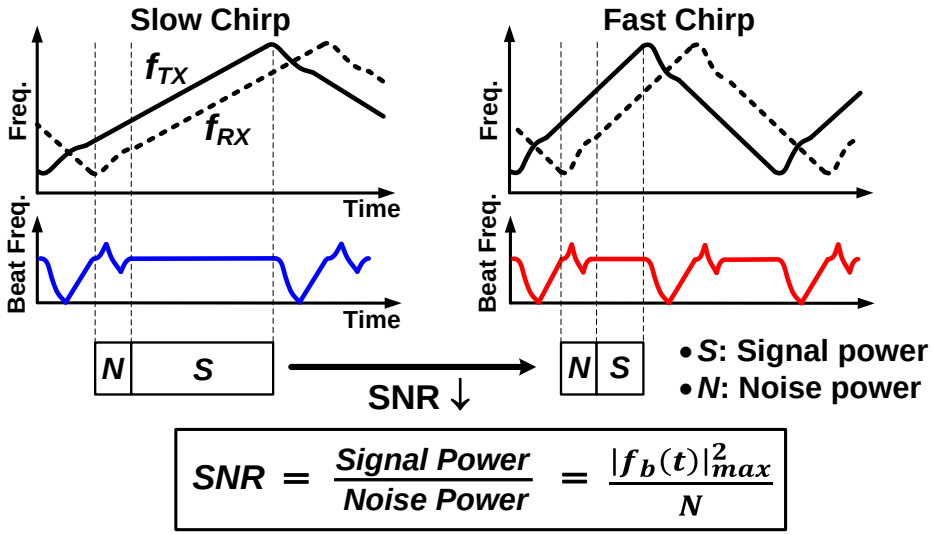


Fig. 6.4 *SNR* degradation by frequency overshooting at turn-around.

As shown in Fig. 6.4, if we make chirp slope faster, the portion of the signal power is decreased compared to the noise power. Therefore, the fast chirp slope implies lower signal-to-noise ratio (*SNR*) because the nonlinearity impact is getting bigger. This is because the peak *SNR* of the radar system will be decreased depending on the linearity of the convolved signal in the matched filter receiver such as radar transceiver. As a result, the effective range resolution will be degraded [28]. The detailed explanation for the matched filter receiver will be reviewed in Chapter 6.6.

6.2 Prior Works

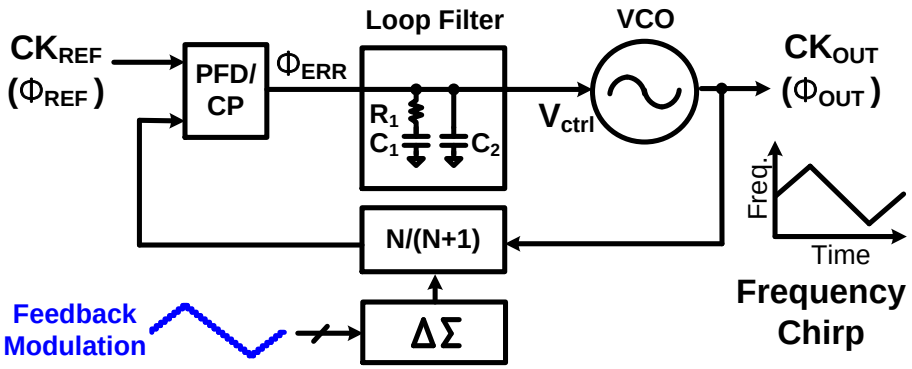


Fig. 6.5 One-point modulation PLL.

As shown in Fig. 6.5, the easiest way to realize the chirp frequency synthesizer PLL is to modulate one-point in the PLL. Modulating either the reference or feedback clock frequency can make the frequency chirp [29]-[31]. However, the finite loop bandwidth of the PLL (ω_{BW}) limits the maximum chirp slope as well as the linearity of the chirp profile. This is because PLL is basically low-pass filtering system. When the modulation frequency is smaller than the PLL loop BW, the frequency chirp of the output clock looks like a triangular shape. But the modulation frequency is larger than the PLL loop BW, which means the fast chirp slope, the frequency chirp of the output clock shows nonlinear profile. Thus, fast chirp requires large ω_{BW} in one-point modulation PLL. Unfortunately, increased ω_{BW} allows more DSM quantization noise to pass through the PLL.

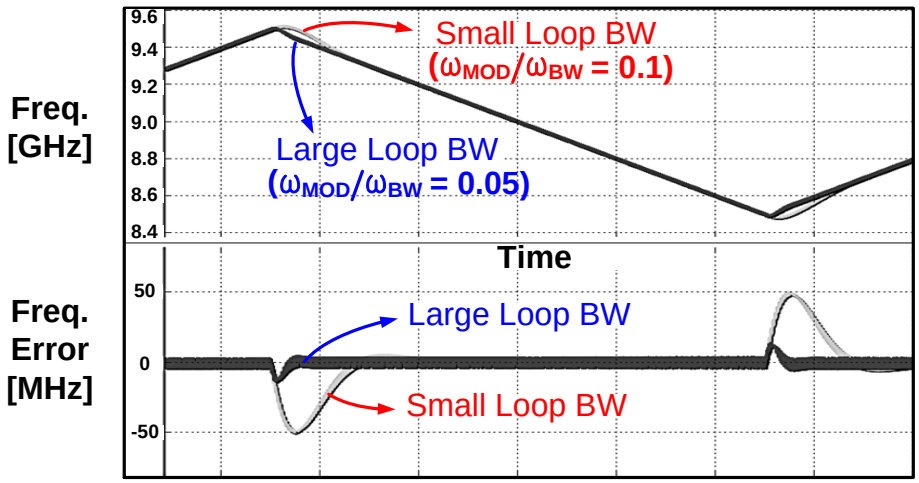


Fig. 6.6 Simulated frequency chirp profiles and frequency errors according to loop bandwidth.

As shown in Fig. 6.6, we can verify the effect of the loop bandwidth to the accuracy of frequency chirp using a behavioral model built by XMODEL. From the simulation results of the charge pump PLL adopting one-point modulation, the larger PLL loop bandwidth is, the smaller frequency error is. Here, ω_{MOD} is the modulation frequency and ω_{BW} is the loop bandwidth of PLL. From the simulation result, even if we increase the loop bandwidth against the modulation frequency such as ω_{MOD}/ω_{BW}=0.1, the frequency error at turn around points (TAPs) will not be disappeared perfectly. The frequency error means the difference between the ideal triangular profile and the PLL frequency profile.

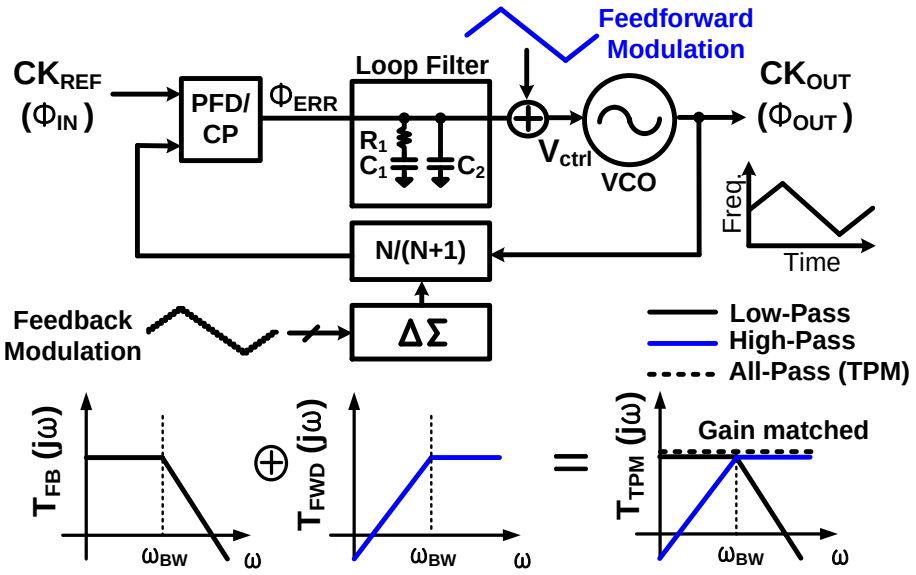


Fig. 6.7 Two-point modulation (TPM) PLL (no gain mismatch).

To decouple the conflicting requirements on the PLL loop bandwidth, we can modulate the other point in the PLL as well as the one point in the PLL as shown in Fig. 6.7. Adding the feedforward modulation in front of the VCO, their respective low-pass and high-pass transfer functions can sum up to an all-pass characteristic [32]-[34]. As a result, the limitation by the PLL loop bandwidth is disappeared.

Although the TPM is widely used, it is sensitive to gain mismatch because of the independent modulations for each other. As shown in Fig. 6.8, if the VCO gain gets higher due to the PVT variation, the gain of the feedforward path also gets higher. In this situation, PLL will try to correct the gain mismatch, because the PLL seems to be in unlocked state. Therefore, extra gain and timing calibration circuit for feedforward modulation is needed.

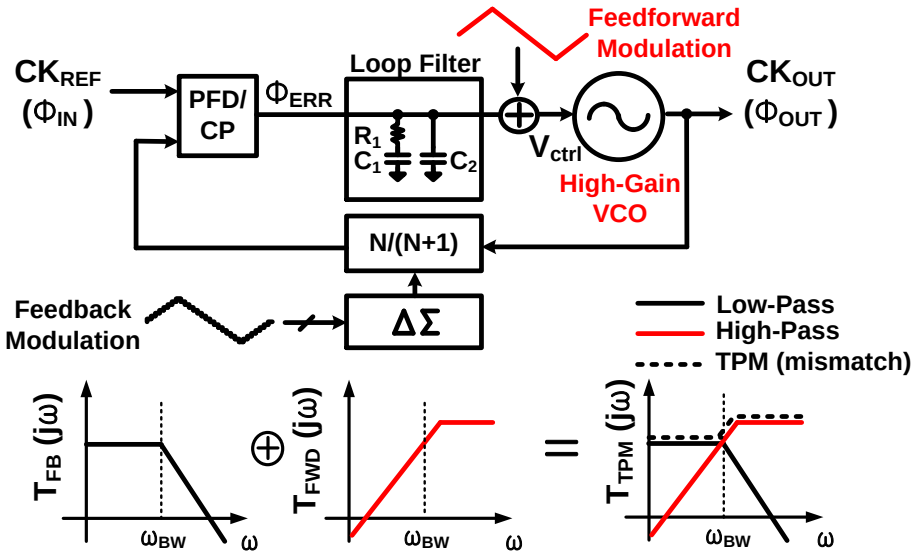


Fig. 6.8 Two-point modulation (TPM) PLL with high gain VCO.

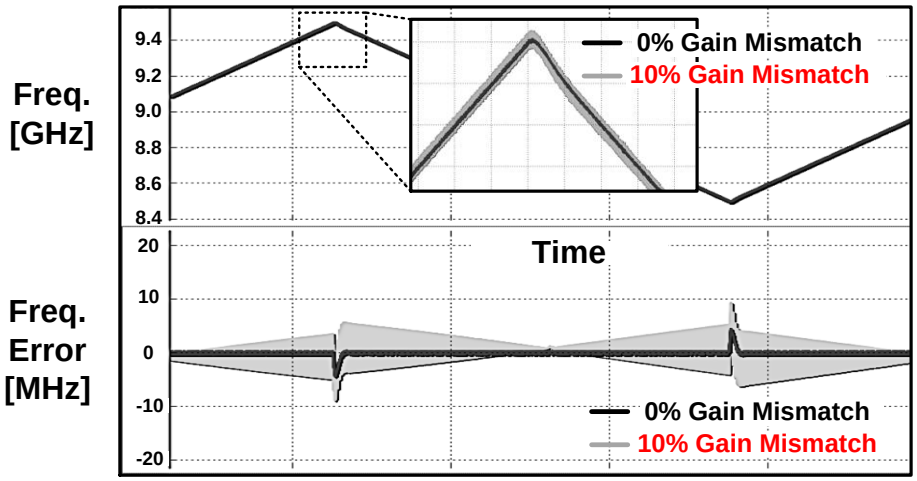


Fig. 6.9 Simulated frequency chirp profiles and frequency errors in the TPM PLL according to gain mismatch.

In the TPM PLL without gain mismatch as shown in Fig. 6.9, the frequency error at TAPs is greatly improved regardless of PLL loop bandwidth. However, if the TPM PLL has 10% gain mismatch between two modulation paths, overall frequency error will be increased to correct these mismatch, represented by gray line.

6.3 Proposed Chirp Frequency Synthesizer PLL

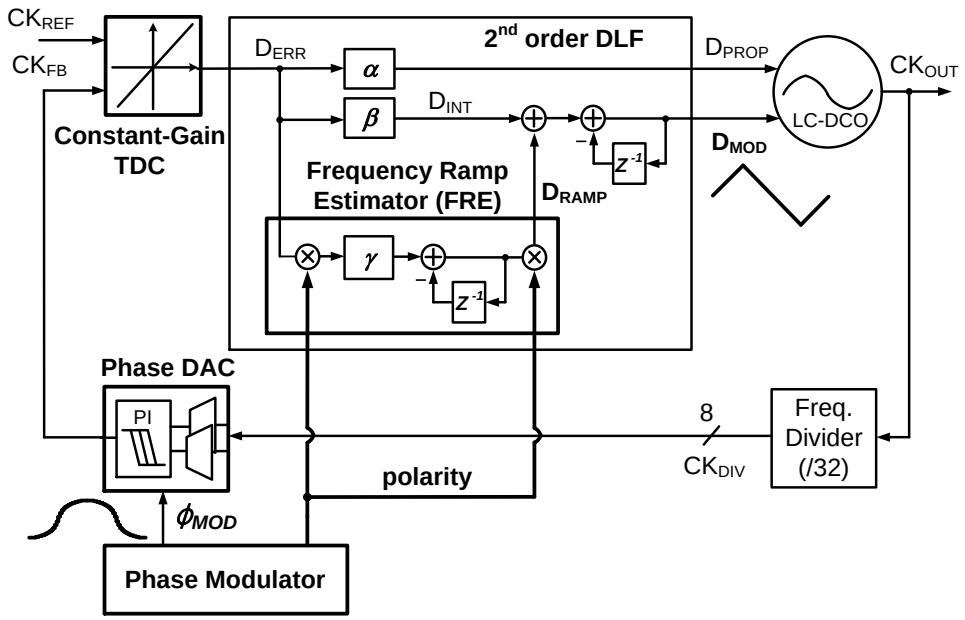


Fig. 6.10. Proposed type-III third-order chirp frequency synthesizer PLL architecture.

Fig. 6.10 shows the overall architecture of proposed chirp frequency synthesizer PLL (FS-PLL) presented in [28]. The proposed chirp FS-PLL consists of a linear TDC with constant-gain [36], a second-order DLF using frequency ramp estimator (FRE), an LC-DCO, a frequency divider, a phase DAC and a phase modulator. We made three solutions dealing with the nonlinearities as shown before. First is that a second-order DLF is adopted for the frequency ramp tracking [37]. This frequency ramp tracking enables the proposed PLL to fulfill the gain self-tracking without additional calibration loop. Second is that the polarity-alternation can switch the slope of frequency ramp instantly to remove the frequency overshooting at turn-around. Third is that a phase modulation using phase DAC is adopted for wide-range and low-power modulation. In addition, the constant-gain TDC minimize the variation of the loop performance such as phase noise, because the gain of TDC stays constant even when the frequency is modulated.

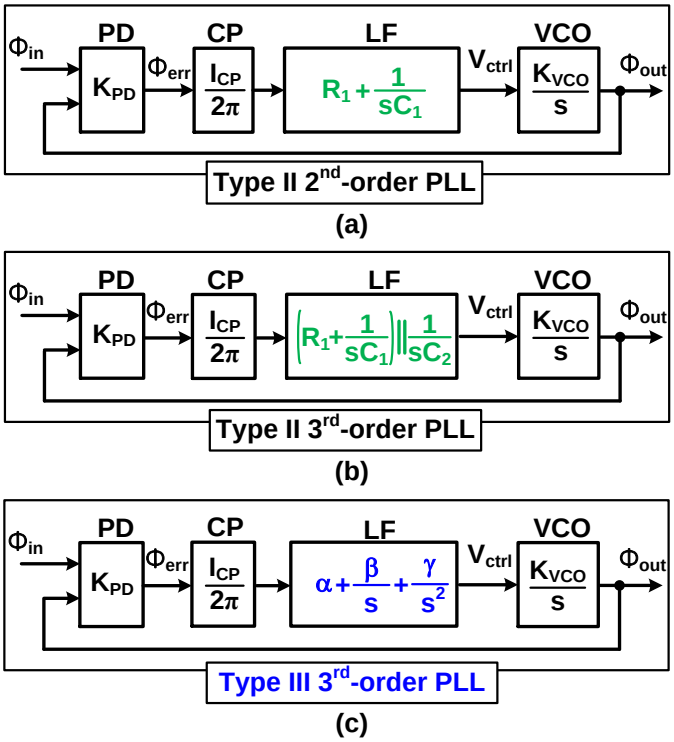


Fig. 6.11. Comparison of the type-II and type-III PLLs.

PLL Input = $\Phi_{in}(s)$		PLL Steady-State Phase Error (Φ_{err})		
		Type II 2nd-order	Type II 3rd-order	Type III 3rd-order
Phase Step (ΔΦ rad)	$\frac{\Delta\emptyset}{s}$	0	0	**0**
Frequency Step (Δω rad/sec)	$\frac{\Delta\omega}{s^2}$	0	0	**0**
Frequency Ramp (R rad/sec²)	$\frac{R}{s^3}$	$\frac{R}{\omega_n^2}$	$\frac{R(2\xi+1)}{\omega_n^2}$	**0**

Fig. 6.12. Steady state phase error of the type-II and type-III PLLs.

A conventional type-II PLL in Fig. 6.11(a) and (b) can track phase and frequency of the PLL input clock. However, in terms of the frequency ramp input, there remains the steady state phase error. Even in case of type-II third-order PLL, this

phase error still exists as listed in Fig. 6.12. Therefore, they are not suitable for the frequency ramp input clock. Although the increasing natural frequency (ω_n) can be a solution to minimize this phase error, it is not desired in terms of jitter performances. On the other hand, a type-III PLL in Fig. 6.11(c) can make the steady-state phase error zero about the frequency ramp. It equips a second-order loop filter (LF) to realize type-III control loop.

Here, we can realize type-III digital PLL with second-order digital loop filter (DLF) which has the LF transfer function of (6.2).

$$T(z) = \alpha + \frac{\beta}{1-z^{-1}} + \frac{\gamma}{(1-z^{-1})^2} \quad (6.2)$$

With this DLF, the steady state phase error for the frequency ramp input will be zero. It means that the output frequency follows the input frequency ramp exactly. Therefore, this type-III third-order PLL is suitable for the chirp FS-PLL.

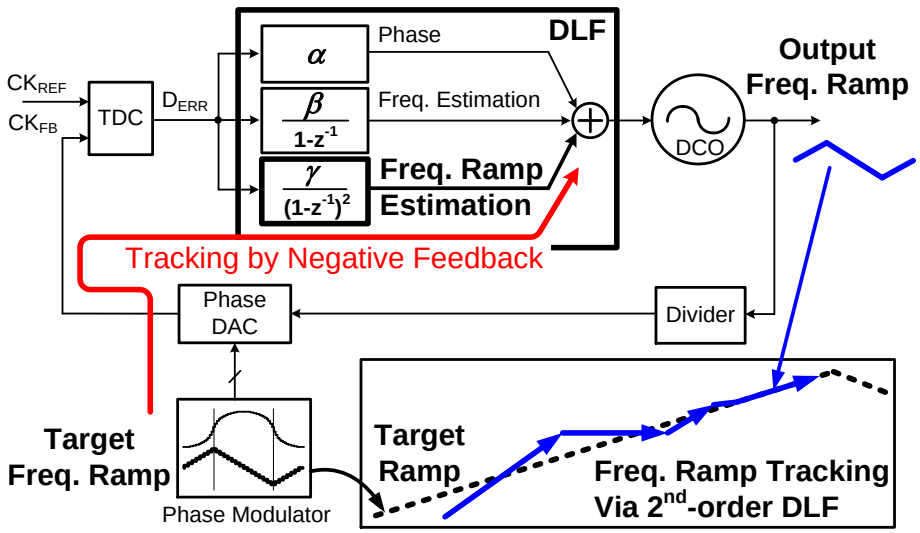


Fig. 6.13. Gain self-tracking for feedforward modulation signal.

Fig. 6.13 shows the second-order DLF as noted with solid box. Since a type-III PLL with this loop filter follows the frequency ramp input exactly, we can build a calibration-free two-point modulation. The key to achieving the gain self-tracking of feedforward modulation is the second-order DLF that makes the slope of output frequency ramp to track the slope of target frequency ramp by negative feedback. Upon the detection of phase error for frequency ramp, frequency ramp estimation carries out a negative feedback operation in order that the output ramp tracks the target frequency ramp. In other words, it leverages the DLF output to calibrate the gain of the feedforward modulation path in reference to the gain of feedback modulation path. It is noteworthy that this self-tracking is operating in background with respect to the PVT variations.

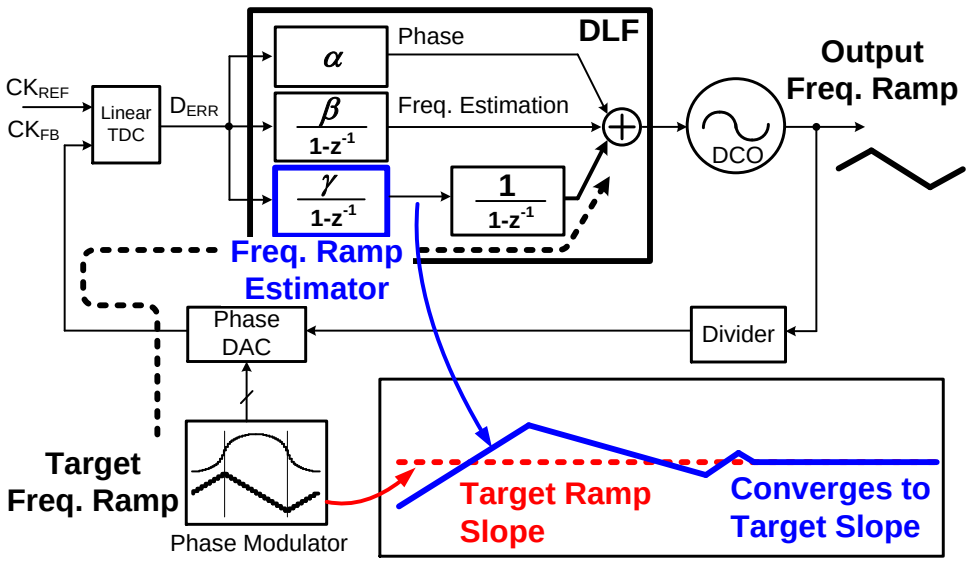


Fig. 6.14. FRE operation which tracks target ramp slope.

Fig. 6.14 shows that the output of the FRE converges to the target ramp slope. If the DCO gain K_{DCO} is changed by some PVT condition, the FRE output converges to another ramp slope in order to track the target frequency ramp. Because there is an accumulator behind the FRE, the FRE output means the slope of the DCO control signal. Finally, this second-order DLF can generate the gain calibrated feedforward modulation signal, which can compensate for the K_{DCO} variation.

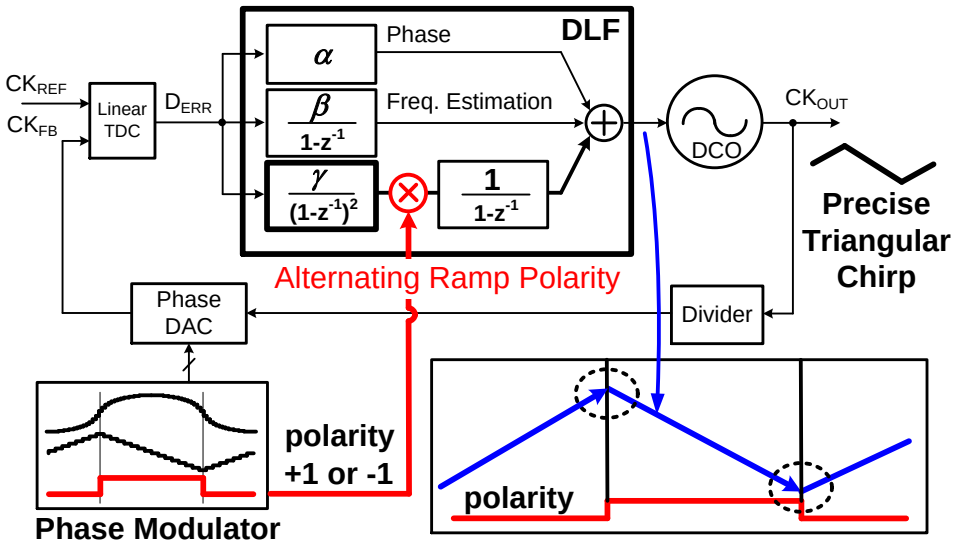


Fig. 6.15. Polarity alternation of integration according to the sign of ramp slope.

As shown in Fig. 6.15, the FRE realizes the frequency ramp tracking to follow the target frequency ramp. However, when the frequency-ramp suddenly changes its polarity, a third-order PLL cannot track this event exactly because it takes some time to readjust for the new slope. So, the proposed second-order DLF can switch the polarity of integration instantly. Because it is directed by the polarity signal from the phase modulator. Here, the polarity signal is self-generated and aligned with the ramp slope change.

In other words, the second-order DLF can effectively generate a calibrated second modulation signal D_{MOD} having instant switching capability, which can compensate any variation in the loop parameters, such as the DCO gain K_{DCO}. Thanks to this architecture, the proposed chirp FS-PLL does not exhibit any increased frequency errors at TAPs, which is a key difference with the previously-reported TPM PLLs with an automatic gain calibration [34].

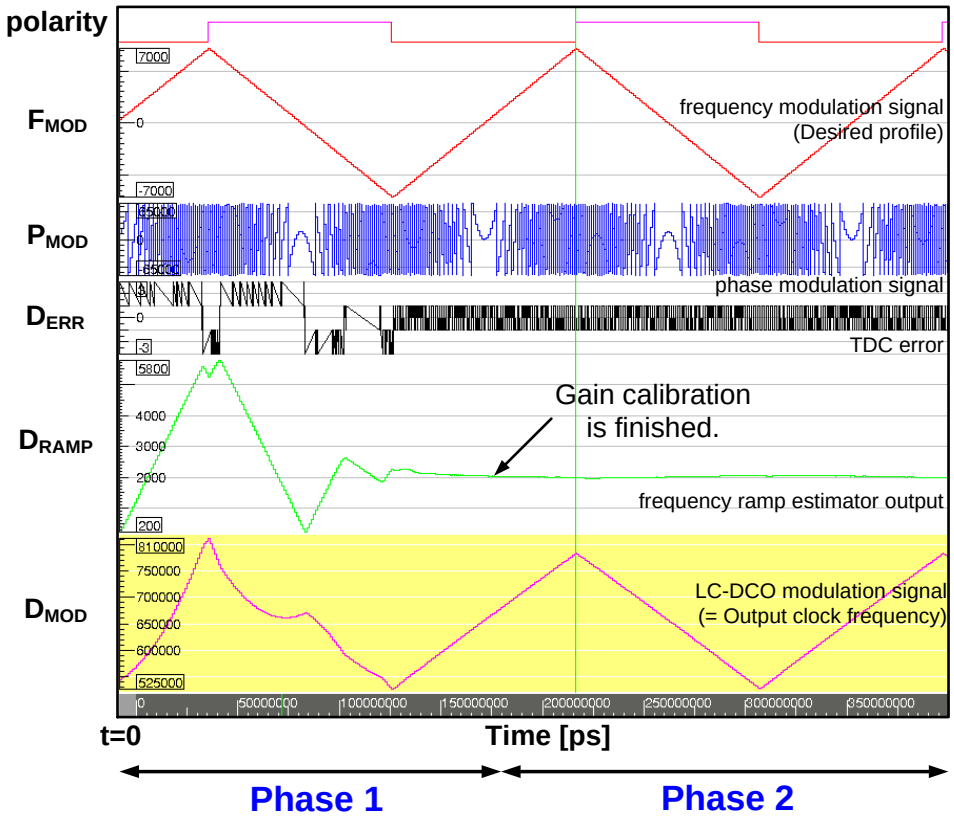


Fig. 6.16. Behavioral simulation results for gain self-tracking.

Fig. 6.16 shows a behavioral simulation result using XMODEL shows the process of the gain self-tracking between the triangular frequency modulation signal (F_{MOD}) and LC-DCO modulation signal (D_{MOD}) by the role of the polarity-alternating frequency ramp estimator (D_{RAMP}). We can divide the entire operation into two phases. In phase 1, the FRE accumulates the phase error from constant-gain linear TDC, which is made by the difference between the target ramp and the output ramp. This process is carried out until the phase error from the TDC becomes zero. Through the phase 1 operation, the frequency ramp slope D_{RAMP} is determined. In phase 2, polari-

ty alternation will be effective. After the ramp slope is determined, only the polarity of integration is switched when the polarity signal is changed. So, triangular frequency chirp can be obtained without overshooting at turn-around points.

6.4 Circuit Implementation

6.4.1 Second-Order Digital Loop Filter

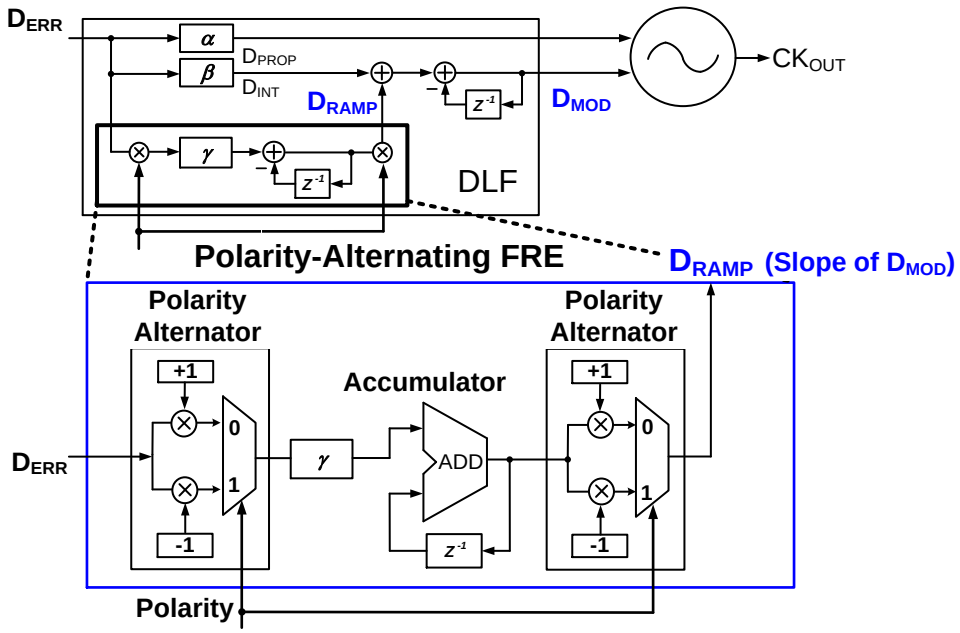


Fig. 6.17. Implementation of the proposed second-order DLF.

Fig. 6.17 shows the details of the polarity-alternating FRE. Unlike an analog PLL using more capacitors to make a higher-order loop filter, this FRE can be simply created by one accumulator and two polarity alternators. The FRE accumulates error signal D_{ERR} from the TDC according to the polarity signal and generates the D_{RAMP} signal, denoting the ramp slope of the feedforward modulation signal D_{MOD}. During

the phase error integration, if the polarity input by the phase modulator is switched, the polarity of integration is changed instantly because the target ramp slope was changed earlier. Without instant change of the integrating direction in the FRE, D_{MOD} signal diverges. Due to this instant switching capability, the proposed chirp FS-PLL does not exhibit increased frequency error when the ramp slope is suddenly changed.

6.4.2 Phase Modulator

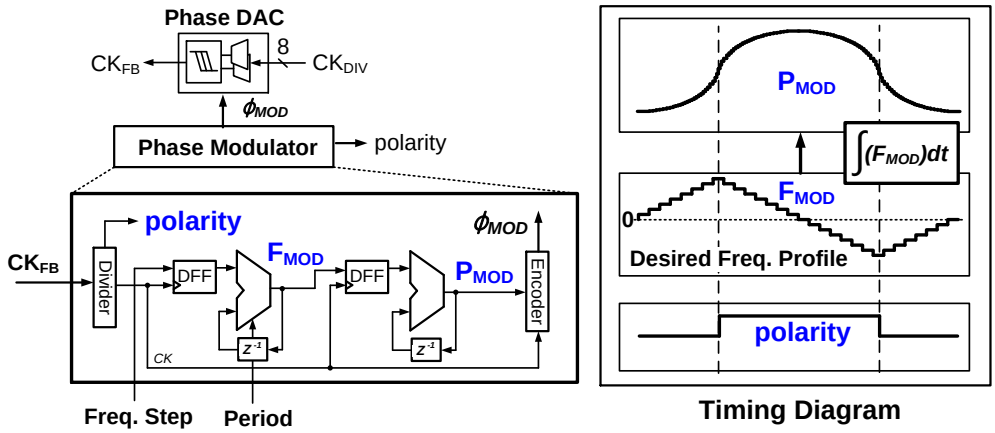


Fig. 6.18. Implementation of the phase modulator and its operating waveform.

Fig. 6.18 shows the circuit implementation of the phase modulator that generates a phase modulation signal. The phase modulator uses two cascaded digital accumulators to emulate the quadratic phase-domain waveform P_{MOD}. F_{MOD} which is the desired triangular frequency profile is obtained from the integration of the frequency step during the chirp period. P_{MOD} is simply generated by the integration of the F_{MOD}.

It also generates a polarity signal indicates whether the frequency is increasing or decreasing.

The phase DAC comprises of two phase multiplexers and a phase interpolator (PI), of which output spans the entire 360° range with a uniform resolution of 2.8125° (128-steps), supporting an infinite range phase rotation which is necessary to emulate a large frequency offset. This phase DAC has same topology and specification in Chapter 5.

Feedback phase modulation signal (ϕ_{MOD}) modulates the phase of the feedback clock by digitally shifting the input code. The main advantage of doing phase modulation is that a low-power phase DAC and fixed modulus frequency divider are used. If it is necessary to increase the chirp bandwidth, we do not need to change the circuit of the phase DAC and the frequency divider. On the contrary, in the feedback frequency modulation via a multi-modulus frequency divider (MMFD) with DSM dithering, we have to increase the number of division ratio and the resolution of DSM. Therefore, the feedback frequency modulation obviously increases the power and area of PLL. Consequently, compared to the feedback frequency modulation, the proposed feedback phase modulation can reduce the power and area to enhance the bandwidth (BW) of frequency chirp.

6.4.3 Constant-Gain TDC

In frequency modulation PLL, if the TDC gain varies according to the frequency modulation, the loop bandwidth ω_{BW} also varies. As shown in Fig. 6.19, when the PLL is modulated at two points (i.e., feedback modulation path and feedforward

modulation path), the ω_{BW} variation causes irregular modulation gain in the vicinity of ω_{BW}. This is because the K_{DCO} over the DCO tuning range and PVT conditions is not constant. Therefore, the TDC and DCO gain variation during frequency modulation deteriorates the gain matching of the TPM, resulting in the degraded jitter performance [38]. In addition, this gets worse when the wide-band modulation is required.

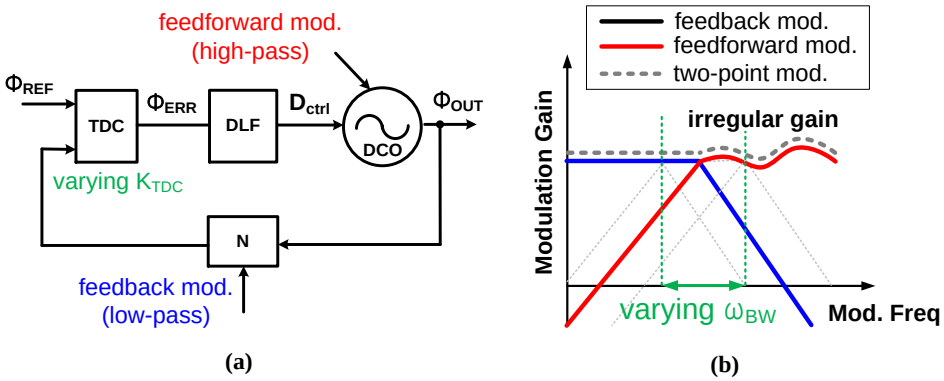


Fig. 6.19. (a) Two-point modulation. (b) Gain mismatch between two modulation paths due to nonlinear DCO gain in wide-band modulation.

To mitigate this, the proposed constant-gain TDC introduced in Section 5.4.2 is adopted in this PLL. Therefore, it can minimize the variation of the ω_{BW}, because the gain of TDC stays constant even when the frequency is modulated.

6.4.4 Varactor-Based LC-DCO

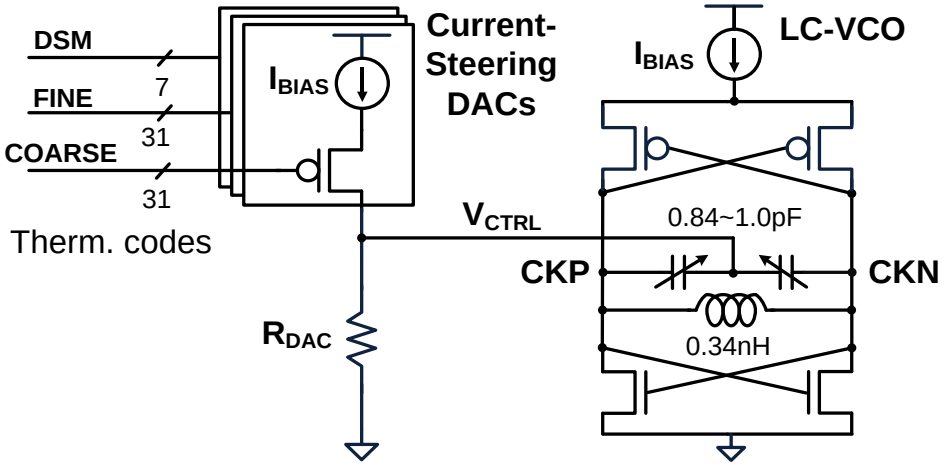


Fig. 6.20. Implementation of the varactor-based LC-DCO, consisting of current-steering DACs and LC-VCO.

Fig. 6.20 also depicts the circuit implementation of the LC-DCO, of which frequency is tuned only by a pair of varactors instead of the capacitor banks occupying large area and incurring loss due to lengthy wires. The control voltage modulating the varactors is generated by a set of thermometer-coded current-steering DACs, including the coarse, fine, and DSM DACs. These current DACs occupy an area of $80\times30\text{-}\mu m^2$ only, which is much smaller than that of the spiral inductor.

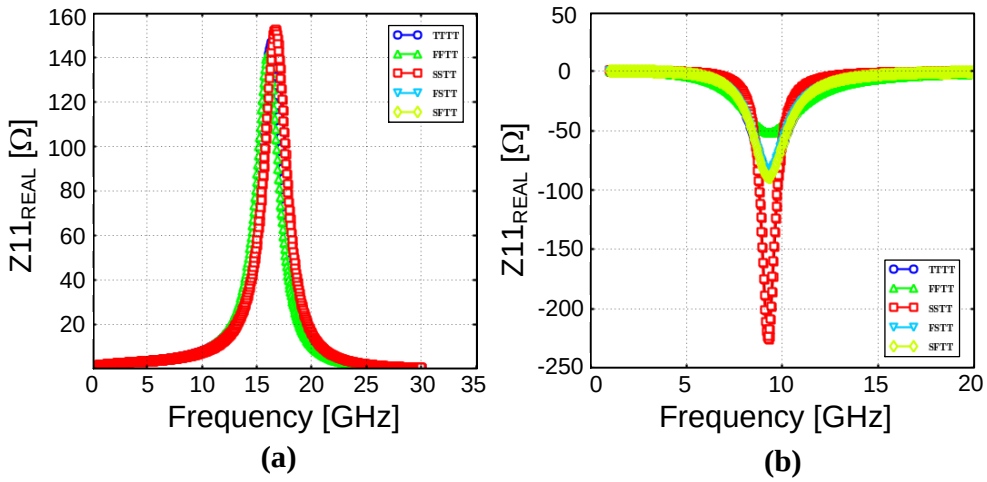


Fig. 6.21. (a) Simulated ohmic loss of the LC tank. (b) Compensated effective resistance R_{eff} by negative G_m.

Fig 6.21 shows the simulation results to guarantee the oscillation start-up of the LC-VCO. Fig 6.21(a) is the simulated ohmic loss of the LC tank without negative transconductance (G_m) circuit, i.e., cross-coupled latch. To compensate for this ohmic loss, the G_m should be selected to satisfy the condition of $|R_{tank}| >> |1/G_m|$. Fig. 6.21(b) shows a simulated effective resistance (R_{eff}) including negative G_m circuit and parasitic R and C after layout. At 8.9 GHz, the R_{eff} denotes negative value in all PVT conditions. It means that the designed LC-VCO has enough start up margin to meet the condition of $g_{active} > (3\sim5)\cdot g_{tank}$ [44].

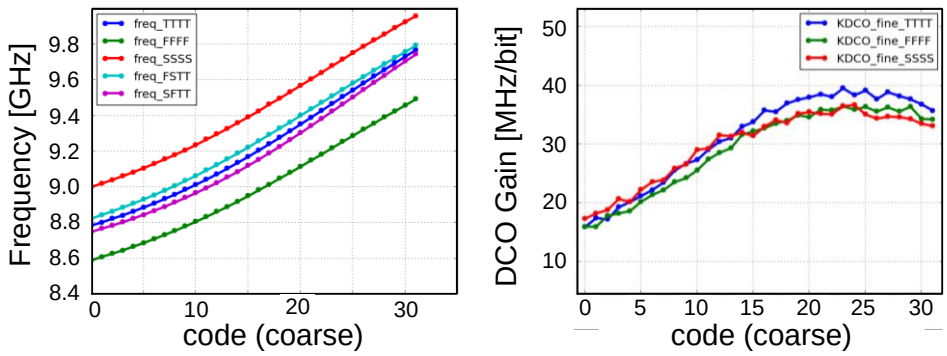


Fig. 6.22. (a) Simulated LC-DCO frequency tuning range. (b) DCO gain.

As shown in Fig. 6.22, the LC-DCO has a 10-bit resolution with a 1-GHz tuning range covering 8.8~9.8-GHz and a varying DCO gain of 17~40 MHz/bit, while dissipating 10-mW at the frequency of 9.8-GHz. The simulated phase noise of the LC-DCO at 8.8 GHz was -104.9-dBc/Hz at 1-MHz offset.

6.4.5 Overall Clock Chain

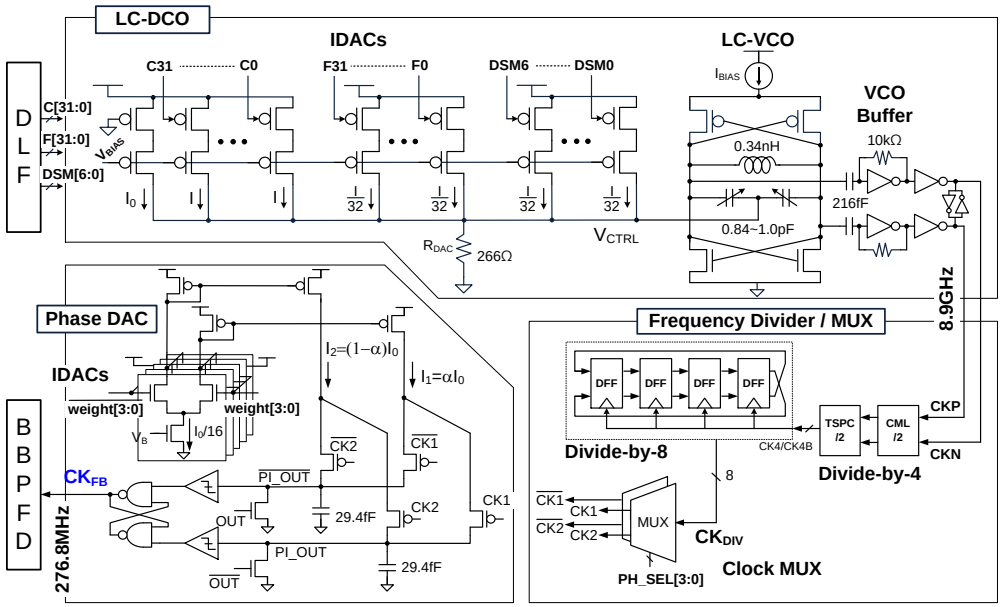
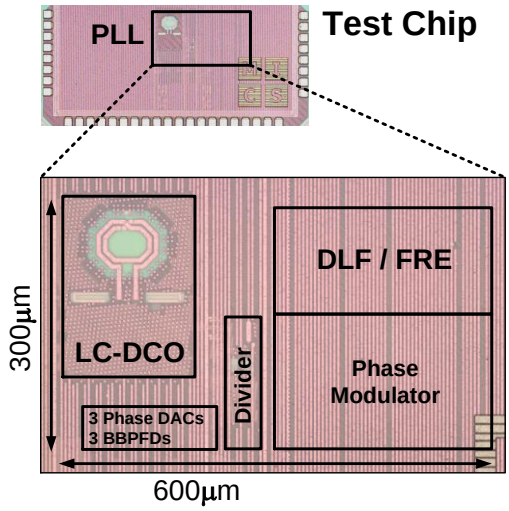


Fig. 6.23. Overall clock chain with important design parameters.

Fig. 6. 23 shows the overall clock chain with important design parameters including the LC-DCO, frequency divider, clock MUX, and phase DAC. In detail, the LC-DCO is composed of three current DACs, LC-VCO, and VCO buffer. The VCO buffer to convert CML signal to CMOS signal has an AC-coupled inverter topology with pseudo-differential configuration.

6.5 Measurement Results



Technology	65nm 1P9M CMOS LP
Supply Voltage	1.1 ~ 1.3 V
Input Freq.	276.8 MHz
Output Freq.	8.4 ~ 9.4 GHz
Maximum Chirp Slope	32.63 MHz/µs
RMS Freq. Error	< 1.9 MHz (including turn-arounds)
Phase Noise (PLL)	-105.0 dBc/Hz @ 1MHz
Power Dissipation	14.8 mW
Active Area	0.18 mm^2

Fig. 6.24. Chip micrograph and performance summary.

The prototype IC of the described FMCW FS-PLL is fabricated in a 65-nm LP CMOS technology and its die photograph and performance summary are shown in Fig. 6.24. The PLL consumes an active area of 0.3×0.6mm^2 and power of 14.8mW while operating at a 1.2V single supply. With a 276.8 MHz reference clock, the PLL can generate a FMCW signal in the range of 8.4~9.4 GHz with the maximum chirp bandwidth of 956 MHz and minimum chirp period of 5 µs.

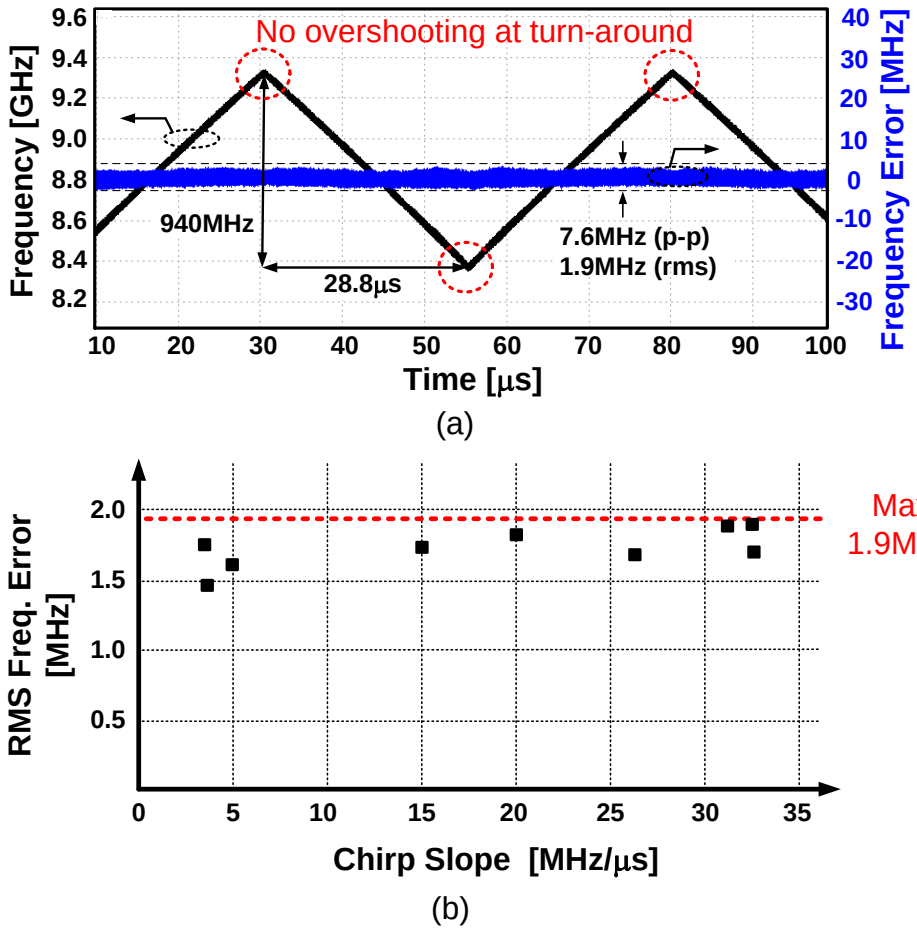


Fig. 6.25. (a) The measured FMCW chirp profile. (b) RMS frequency error across the entire operating range.

Fig. 6.25(a) demonstrates that a precise triangular chirp without any distortion or overshooting around TAPs can be generated for the chirp bandwidth of 940MHz and the chirp period of 28.8μs. Fig. 6.25(b) shows that the rms frequency error including the TAPs is less than 1.9-MHz_{rms} for all values of BW less than 956-MHz and T_m longer than 6.5μs.

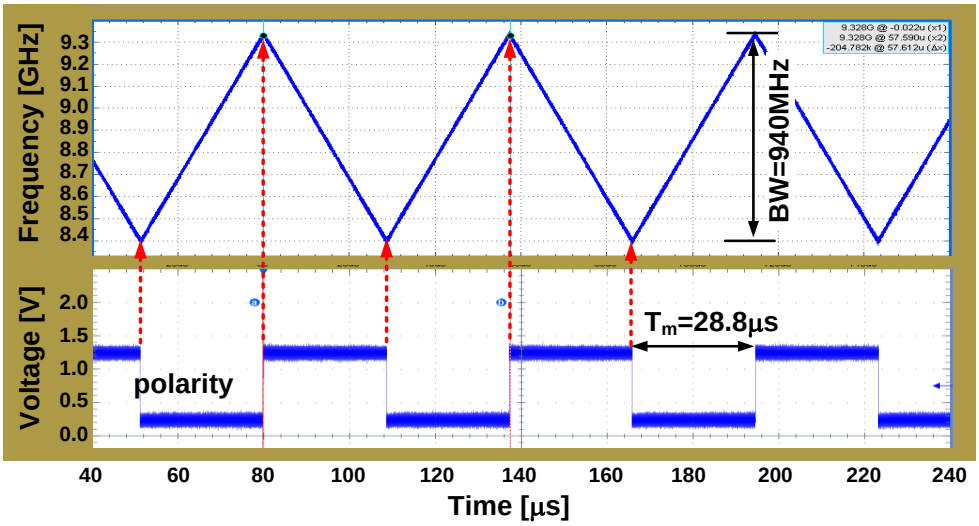


Fig. 6.26. Instant switching of frequency chirp directed by polarity signal.

Fig. 6.26 shows the instant switching capability at turn-around. The frequency chirp slope is directed by the polarity signal as we expected.

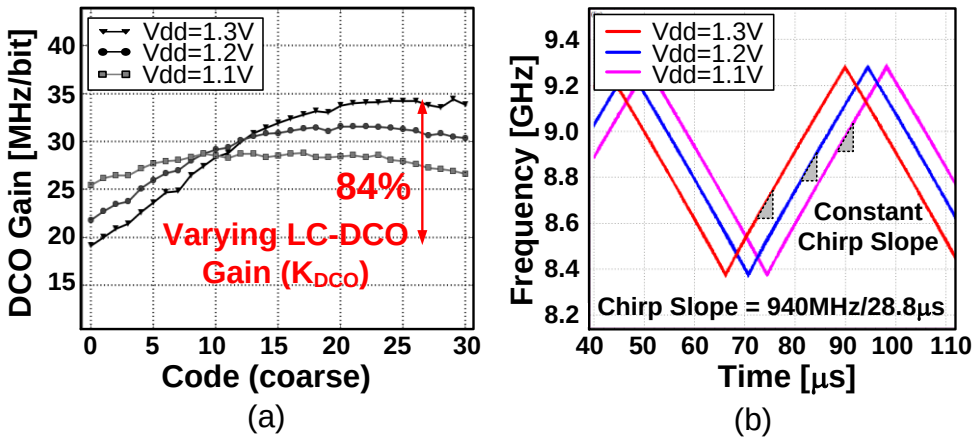


Fig. 6.27. (a) Varactor-based LC-DCO gain variation. (b) Constant chirp slope regardless of LC-DCO gain variation.

Fig. 6.27 demonstrates that even with a 84% change in the DCO gain caused by the supply voltage variation, the proposed calibration-free TPM with the polarity-alternating second-order DLF keeps the chirp slope constant.

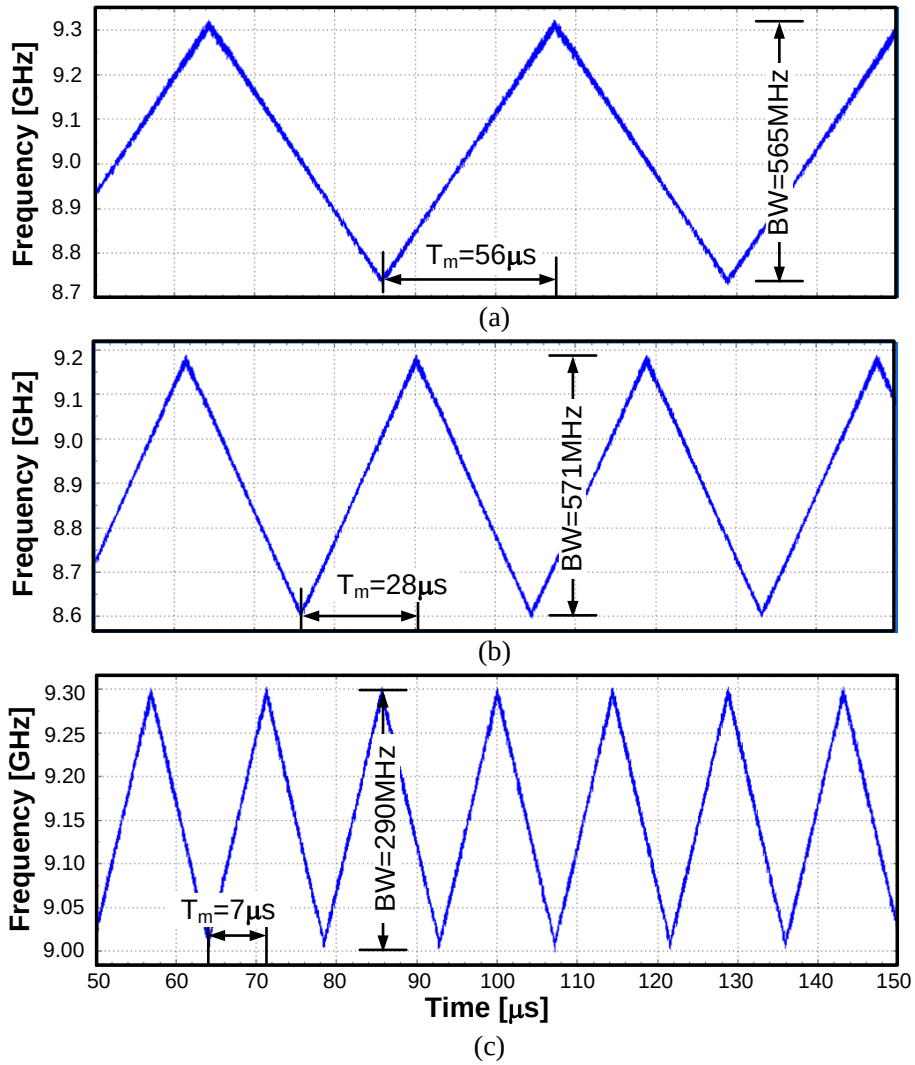
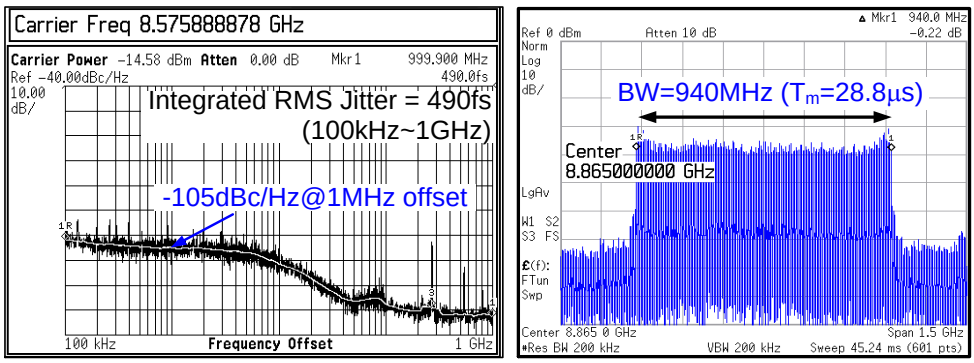


Fig. 6.28. Various chirp profile: (a) *BW*=565 MHz, T_m=56µs, (b) *BW*=571 MHz, T_m=28µs, and (c) *BW*=290 MHz, T_m=7µs.

Fig. 6. 28 shows the various chirp profile with different BW and T_m that are controlled by digital paremeters.



Phase Noise (Without Chirp) **Power Spectrum (With Chirp)**

(a) (b)

Fig. 6.29. (a) Measured PLL phase noise without chirp. (b) Measured power spectrum with chirp.

As shown in Fig. 6.29, the measured phase noise of the PLL clock without a chirp is -105-dBc/Hz at 1-MHz offset and -126.2-dBc/Hz at 40-MHz offset and the power spectrum of the PLL clock including the chirp with T_m=28.8μs shows a uniform spread of the spectral power from 8.395-GHz to 9.335-GHz.

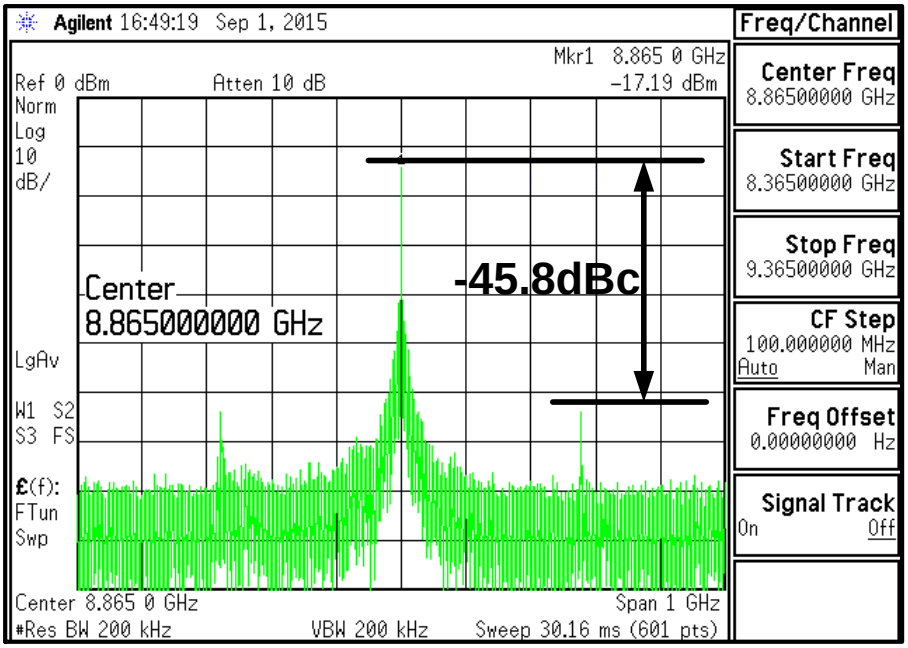
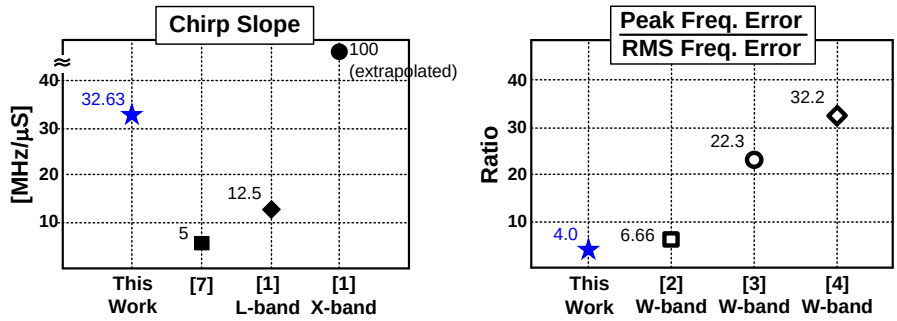


Fig. 6.30. Measured power spectrum without chirp.

Fig. 6.30 shows the measured reference spur of -45.8 dBc at 8.865 GHz.



	This Work	MTTS06 [35]	MTTS13 [30]	ISSCC10 [29]	ISSCC11 [31]	JSSC14 [32]
Application	Short-Range Radar (L-,X-band)			Long-Range Radar (W-band)		
FMCW Generation	ADPLL + TPM	External Source + VCO	External Source + PLL	Frac.-N PLL	Mixed-Mode	ADPLL + TPM
Frequency Range [GHz]	8.4 ~ 9.4	9.5 ~ 11.0	7.2 ~ 12.2	75.6 ~ 76.3	82.1 ~ 83.8	56.4 ~ 63.4
Chirp Bandwidth (*BW*)	956 MHz	50 MHz	125 MHz (L-band) 1000 MHz* (X-band)	700 MHz	1.5GHz	1220 MHz
Chirp Period (T_m)	5 ~ 220 μs	10 μs	10 μs*	0.6 ~ 3 ms	2 ~ 100 ms	0.21 ~ 4.1 ms
Chirp Slope [MHz/μs]	32.63 (940MHz/28.8μs)	5 (50MHz/10μs)	12.5 (125MHz/10μs) 100* (1GHz/10μs)	0.466 (700MHz/1.5ms)	1.5 (1.5GHz/1ms)	4.76 (1GHz/0.21ms)
Peak Freq. Error at TAP	7.6 MHz	N/A	N/A	2 MHz‡	4MHz‡	5.8 MHz‡
RMS Freq. Error†	1.9 MHz	N/A	3.088 MHz*	300 kHz	179 kHz	180 kHz
Power Consumption	14.8 mW	N/A	380 mW	73 mW	152 mW§	48 mW
Phase Noise @ 1 MHz offset	-105 dBc/Hz	N/A	-81.4 dBc/Hz	-85 dBc/Hz	-84 dBc/Hz	-90 dBc/Hz
Technology	65-nm CMOS	180-nm CMOS	250-nm BiCMOS	65-nm CMOS	65-nm CMOS	65-nm CMOS

*** Extrapolated value from divide-by-8 (L-band) clock measurement result (i.e. 125MHz/10 μs=12.5 at divide-by-8 clock),**
† Including turn-around point (TAP), ‡ Taken from the figure in papers, § Including buffer power consumption

Table 6.1. Performance comparison of the proposed FMCW chirp frequency synthesizer PLL with prior arts.

Table 6.1 compares the key performance metrics of the proposed FS-PLL with those of the other FMCW frequency synthesizers. The proposed chirp FS-PLL achieves the fast chirp slope of 32.63-MHz/μs while keeping the frequency error less than 1.9-MHz_{rms} at all times, which is equivalent to a 15.95-cm spatial resolution of the X-band radar. On the other hand, this work also exhibits the low ratio between the peak frequency error and rms frequency error, even comparing with the state-of-the-art FMCW frequency synthesizers for W-band radars [29],[31],[32].

6.6 Signal-to-Noise Ratio of Radar

In signal processing, a matched filter (MF) maximizes the output peak-signal-to-mean-noise ratio to maximize the detectability of a target [45]. The MF is obtained by correlating a known signal, or template, with an unknown signal to detect the presence of the template in the unknown signal. This operation is equivalent to convolving the unknown signal with a conjugated time-inverted version of the known signal, i.e., the impulse response of the MF is $h(t)=s^*(T-t)$. The MF is the optimal filter for maximizing the signal to noise ratio (*SNR*) when the input noise spectral density is uniform (additive white Gaussain noise). MFs are commonly used in radar signal processing, in which a known signal is transmitted, and the reflected (or received) signal is processed for detecting their difference between the transmitted and reflected signal [46].

In the MF receiver, the frequency response, $H(f)$, of the MF is

$$H(f) = A \cdot S^*(f) \cdot e^{-j2\pi f t_m} . \quad (6.3)$$

where t_m is the time at which the output of the MF is a maximum (generally equal to the duration of the signal). And, $s(t)$ is the received signal and $S(f)$ is the Fourier transform of $s(t)$ as

$$S(f) = \int_{-\infty}^{\infty} s(t) e^{-j2\pi ft} dt . \quad (6.4)$$

The amplitude and phase of the MF are

$$\begin{aligned} |H(f)| &= |S(f)| \\ \phi_{MF} &= -\phi_s(f) + 2\pi f t_m \end{aligned} . \quad (6.5)$$

The signal-to-noise ratio (*SNR*) of the MF receiver to be maximized

$$SNR \le \frac{\left|s_0(t)^2_{\max}\right|}{N} = \frac{\left|\int_{-\infty}^{\infty} S(f)H(f)e^{-j2\pi ft_m}df\right|^2}{\frac{N_0}{2}\int_{-\infty}^{\infty}\left|H(f)\right|^2 df} = \frac{\int_{-\infty}^{\infty}\left|S(f)\right|^2 df}{\frac{N_0}{2}} . \quad (6.6)$$

where N is the mean square noise power at MF output and N_0 is the input noise power per unit bandwidth.

Apply Parseval's theorem for the numerator of (6.6), the total energy of the received signal is

$$E = \int_{-\infty}^{\infty}\left|S(f)\right|^2 df = \int_{-\infty}^{\infty}\left|s(t)\right|^2 dt . \quad (6.7)$$

$$SNR_{peak} = \frac{\int_{-\infty}^{\infty}\left|S(f)\right|^2 df}{\frac{N_0}{2}} = \frac{2E}{N_0} \quad (6.8)$$

At the peak output, the *SNR* is the highest attainable, which is $2E/N_0$ as (6.8). The response is described by the autocorrelation function of the signal.

To guarantee the peak *SNR* of the MF receiver, it is necessary to convolve the received signal with exactly matched signal of the received signal. If nonlinearities in the convolved signal are existed, achievable SNR_{peak} can be decreased.

Chapter 7

Conclusion

In this thesis, A PVT-insensitive-bandwidth PLL and a chirp frequency synthesizer PLL without an explicit calibration or additional components are proposed.

The PVT-insensitive loop BW at a given frequency is achieved by the use of constant-gain TDC and constant-relative-gain DCO of which characteristics rely only on ratiometric designs. For instance, in the DCO with exponentially-sized switched-capacitor banks, the relative DCO gain is set by the capacitance ratio. Also, in the TDC with oversampling BB-PFDs, the gain is set by the phase spacing between the BB-PFDs, which is fixed in units of radians. The prototype PLL has been fabricated in a 28-nm CMOS technology. The measurement results demonstrated a nearly constant loop bandwidth across process, voltage, and temperature conditions.

The precise triangular frequency chirp without increased frequency errors at turn-around points is achieved by calibration-free TPM, second-order DLF with polarity-alternating frequency ramp estimator, and constant-gain TDC. The simple second-order DLF that tracks frequency ramp exactly can realize gain self-tracking for feed-forward modulation signal. In addition, thanks to the known polarity information from the phase modulator, the instant polarity alternation can make precise triangular chirp without any overshooting at turn-around points. The prototype PLL has

been fabricated in a 65-nm CMOS technology. The measurement results demonstrated the fast chirp slope with low frequency errors despite the nonlinear DCO gain, varying with PVT conditions.

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초 록

본 논문에서는 고정상대이득을 가지는 디지털제어발진기와 고정이득을 가지는 시간디지털변환기 및 간단한 디지털루프필터를 사용하여 추가적인 캘리브레이션(calibration) 및 회로요소 없이 공정, 전압, 온도에 상관없이 동작하는 고정밴드 위상동기루프(PLL)와 첩(chirp) 주파수생성기를 제안하였다.

첫째로 고정상대이득 디지털제어발진기(DCO)와 고정이득 시간디지털변환기(TDC) 및 간단한 디지털루프필터(DLF)를 사용하여 고정 루프밴드(loop bandwidth) 위상동기루프를 구현하였다. 공정, 전압, 온도에 상관없는 밴드 특성을 위해 비율기반설계(ratiometric design)를 적용하여 디지털제어발진기가 입력코드 변화에 대해 현재 주파수의 일정한 비율로만 변하도록 제작하였고, 시간디지털변환기가 입력 단위시간(UI)에 대해 고정된 탐지범위와 해상도를 가지도록 제작하였다. 이로 인해, 제안하는 위상동기루프는 추가적인 캘리브레이션 루프 없이도 공정, 전압, 온도 및 주파수에 상관없이 입력 주파수의 일정 부분에 해당하는 루프 밴드를 유지하였다. 28 나노 CMOS 공정으로 제작된 칩은 8.34~9.34 GHz 의 주파수 범위와 652 fs 의 RMS 지터를 가졌으며, 15.2 mW 의 전력을 소모하고 0.24 mm^2 의 면적을 차지하였다. 또한, 822 kHz±4.25 %의 고정된 위상고정루프 밴드를 유지하였다.

둘째로 X 밴드의 주파수변조연속파(FMCW) 이미징 레이더를 위해 정확한 삼각 주파수 변조 (triangular frequency chirp)을 수행할 수 있는 첩 주파수 생성을 위한 위상고정루프를 구현하였다. 위상 도메인 두점 변조 (two-

point modulation)와 고정이득 시간디지털변환기, 누적방향을 첩의 기울기에 따라 순간적으로 바꾸는 간단한 2 차 디지털루프필터를 사용하여, 제안하는 위상동기루프는 별도의 캘리브레이션이 없이도, 두점 변조를 통해 주파수 변조의 방향이 갑자기 바뀌는 지점에서도 주파수 에러 (frequency error)의 열화가 없는 빠른 변조 기울기(chirp slope)를 가진 삼각 주파수 변조를 구현하였다. 65 나노 CMOS 공정으로 제작된 칩은 8.9 GHz 중심주파수에서 940 MHz 밴드의 삼각 주파수 변조를 28 μs 의 시간 동안에 수행하였고, 이때 주파수 에러는 주파수 변조 방향이 바뀌는 지점을 모두 포함하여도 1.9 MHz_{rms} 이하로 측정되었다. 또한 이 칩은 14.8 mW 의 전력을 소모하였으며, 기존에 보고된 첩 주파수 생성기들과 비교하여 가장 빠른 32.63 MHz/μs 의 변조 기울기를 가졌다. 이는 주파수변조연속파 이미징 레이더의 거리 해상도를 15.95 cm 까지 낮출 수 있는 성능이다.

주요어 : 디지털 위상동기루프, 캘리브레이션, 고정 루프밴드, 시간디지털변환기, 디지털제어발진기, 첩주파수생성기, 두점변조, 레이더.

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