Ph.D. DISSERTATION

A STUDY ON LOW-PHASE-NOISE 77-GHZ CMOS TRANSMITTER FOR FMCW RADAR

저 위상잡음 77 GHz CMOS FMCW 레이더 송신기에 관한 연구

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공학박사 학위논문

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Abstract

This thesis presents design methodology and experimental verification of a low-phase-noise 77-GHz CMOS FMCW (Frequency Modulated Continuous Wave) radar transmitter. It is quite difficult to design a low-phase-noise signal generator at millimeter-wave frequencies in CMOS because gain of CMOS transistors is extremely low at those frequencies. When using a frequency multiplier, it is relatively advantageous to design a low-phase-noise signal source because a VCO can be designed at lower frequency band where gain of active devices is high. When using multiple stage frequency multipliers to achieve low-phase-noise performance, the operating frequency range can be reduced and DC power consumption can be increased. Therefore, in this thesis, two methods for realizing 77-GHz CMOS low-phase-noise signal source have been proposed.

One method is to combine a ×6 frequency multiplier and a 12.8-GHz FMCW signal generator. In this case, a VCO, an injection-locked VCO buffer, a ×3 frequency multiplier (tripler), and a ×2 frequency multiplier (doubler) constituting the 77-GHz signal generator are designed as a four-stage coupled injection-locked oscillator (ILO) chain which is oscillated and injected into the output signal of the preceding stage. The VCO used in the 12.8-GHz PLL (phase locked loop) was designed using linearized transconductance (LiT: Linearized Transconductance) technology

to have low phase noise characteristics and was designed to be simpler than the existing LiT VCO using a 3:2 transformer. Since the PLL is designed as the integer-N type, an external frequency modulated triangular reference signal must be injected into the phase frequency detector (PFD) of the PLL to generate the FMCW signal. The fabricated transmitter chip supports FMCW output signals in the 76.81-77.95 GHz band when supplied with the external reference triangular signal from 50.00 to 50.75 MHz. The RF output power is about 8.9 dBm and consumes 116.7 mW of DC power. The measured phase noise is -91.16 dBc/Hz at the 1-MHz offset of the 76.81-GHz carrier frequency, which is the lowest phase noise characteristic of the previously announced 77-GHz CMOS transmitter and transceiver. A transmitter module for 77-GHz radar performance measurement was fabricated by combining the transmitter chip with the on-chip feeder that can solve the millimeter-wave packaging problem.

The other is a method of combining a ×28 frequency multiplier and a 2.75-GHz FMCW signal generator. As in the previous method, the VCO, a ×7 multiplier, and two ×2 multipliers constituting the 77-GHz signal generator are each designed as a 4-stage ILO chain. The VCO used in the 2.75-GHz PLL is designed as a class-C type that improves the startup problem to have low-phase-noise characteristics. As in the previous case, an integer-N type PLL is used. The fabricated transmitter chip supports FMCW output signals in the 76.26-78.23 GHz band when supplied with the

external reference triangular signal from 42.55 to 43.65 MHz. The RF output power is about −18 dBm and consumes 195.4 mW of DC power. The measured phase noise is −93.64 dBc/Hz at the 1−MHz offset of the 78.13−GHz carrier frequency, which is even lower phase noise characteristic than the ×6 frequency multiplier based transmitter chip.

Keyword : 77−GHz, FMCW radar transmitter, frequency multiplier, low−phase−noise VCO, PLL

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Table of Contents

List of Figures

List of Tables

Chapter 1. Introduction

In the past, radar systems, which were primarily used only for military, aircraft, and scientific navigation purposes, have recently begun to be installed in automobiles with the development of cheap and small radar systems. The automotive radar system is not only used for safety purposes such as collision avoidance and blind spot detection but also is becoming popular in terms of convenience such as adaptive cruise control. Furthermore, it is becoming an indispensable element in the development of an “intelligent vehicle” capable of automatic driving in the future. Although laser radar for automobiles has been commercialized in the early 1980s, lasers are so sensitive to various weather conditions that millimeter-wave radars are now widely available. In chapter 1.1, types and applications of the automotive radar will be described briefly, and the concept of FMCW radar will be discussed in detail. And research strategies for developing low-phase-noise radar transmitter in CMOS have been discussed in chapter 1.2.

1.1. Types and Applications of Automotive Radars

RADAR is an abbreviation of RAdio Detection And Ranging. Its main function is detection of position or direction of object and measurement of distance or velocity. Among them, the distance and speed of the detected object are based on the measurement of the frequency shift due to the Doppler Effect, which includes the propagation speed of the radio wave, the propagation time, and the reflected or scattered radio wave respectively. The distance and velocity measurements of the radar using the above principle are based on (1) and (2).

$$R = \frac{c \cdot \Delta t}{2} \tag{1}$$

$$v = \frac{\lambda \cdot f_d}{\cos\theta} \tag{2}$$

In the above equation (1), c is the propagation speed in free space, and Δt is the time taken for the emitted radio wave to be reflected by the measured object and returned to the radar. In (2), f_d is the Doppler frequency shift, λ is the wavelength of the radiated wave, and θ is the angle between the radar and the measured object, which is the angle between the measurement direction of the radar and the moving direction of the measured object. f_d becomes larger when a higher frequency is used than when a lower frequency is used for measuring the velocity of a subject moving at the same speed. This means that it is easier to extract the Doppler frequency

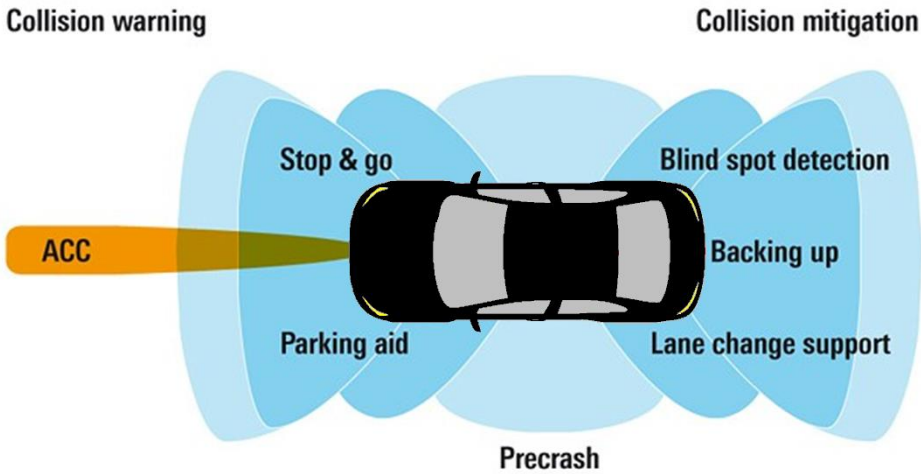

Fig. 1. ADAS function.

TABLE I. Radar classification according to detection distance

Radars	Freq. (GHz)	Modulation	Angle (Deg)	Distance (m)	Resolution (m)	Applications
LRR	77	FMCW	15	150~	0.5	ACC
MRR	77 / 77-81	FMCW / Pulse	40	~100	0.5	Stop&go, Cross traffic alert, Lane change
SRR	77-81	Pulse	80	~30	0.1	Collision avoidance, Blind spot detection, Parking aid

shift by using a relatively high frequency in the measurement of the speed. Therefore, automotive radars are used at frequencies higher than those used by other conventional electronic products such as 24, 77, and 79 GHz. In Europe, which is leading the automobile parts industry, the 77-GHz is mainly used as a medium-and long-range detection radar for 100 ~ 250m and 79-GHz is used as a short-range collision prevention radar for 10 ~ 20m.

Fig. 1. Shows various ADAS (Advanced Driver Assistance Systems) functions. The functions of ADAS include ACC (Adaptive Cruise Control), Stop & Go, parking aid, blind spot detection, backing up, lane change detection, and collision warning. Vehicle radars can be classified as LRR (Long Range Radar), MRR (Medium Range Radar), or SRR (Short Range Radar) depending on the detection range [Table. I]. The LRR detects long distances of more than 150m in the 77-GHz band and is mainly used for ACC. The MRR detects distances of several tens of meters and uses 77-GHz FMCW radar or 77~81-GHz pulse radar, mainly used for stop & go, cross traffic alert, and lane change support. The SRR detects short distances of less than 30m in the 77~81-GHz band and is used for collision avoidance, blind spot detection, and parking aid.

The 77-GHz FMCW radar used mainly for LRR or MRR is as follows. The basic radar configuration is shown in Fig. 2 [1]. An FMCW radar literally means a radar in which frequency-modulated signals are continuously transmitted. A typical signal waveform is shown in Fig. 3 [2]. The solid line indicates the transmission signal

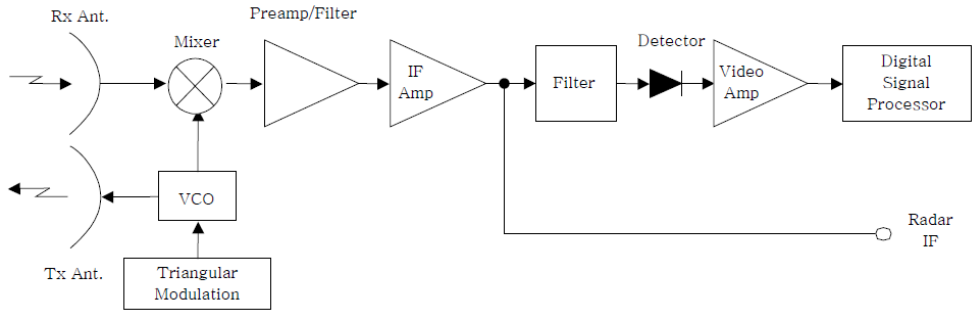

Fig. 2. General architecture of FMCW radar.

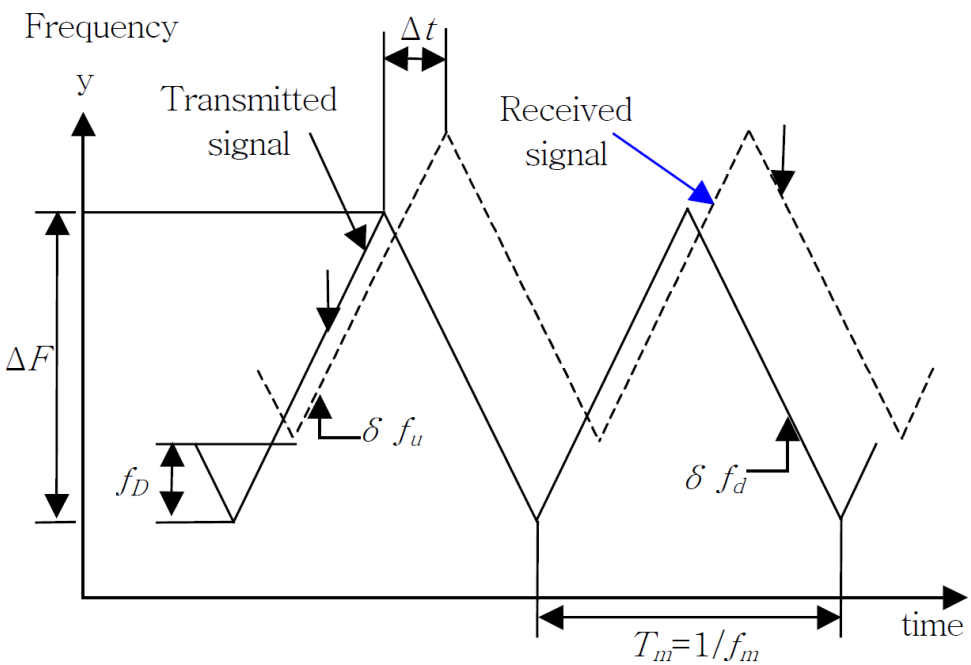

Fig. 3. Time-frequency waveform of conventional FMCW radar.

of the radar, and the dotted line indicates the reception signal in which the transmission signal is reflected or scattered back to the object to be measured. Distance and velocity measurements can be obtained using the delay time (Δt) and the Doppler frequency shift (f_D) of the received signal.

$$R = \frac{f_D \cdot c}{4 f_m \Delta F} \tag{3}$$

$$v = \frac{(f_D - \delta f_u)c}{2 f_0} \tag{4}$$

ΔF is the maximum frequency deviation, f_0 is the center frequency, and f_m is the modulation frequency.

1.2. Research Strategy

For the development of FMCW radar integrated circuit in CMOS for vehicles, it is necessary to establish the direction and strategy of this research. First, to determine the radar performance specification, the relationship between radar detection distance and radar SNR should be clarified. In the situation shown in Fig. 4, the radar equation is widely known as follows [3].

$$P_r = \frac{P_t G_t G_r \lambda^2 \sigma}{(4\pi)^3 R^4} \tag{5}$$

P_t is transmit power (W), P_r is received power (W), G_t is transmit antenna gain, G_r is receive antenna gain, σ is radar cross section (RCS, m^2), and R is distance to target. From (5), the relationship between the maximum detection distance (R_{max}) and the minimum detectable SNR (S/N_{min}) can be derived as follows.

$$R_{\max}^4 = \frac{P_t G_t G_r \lambda^2 \sigma}{(4\pi)^3 k T_0 B F_n (S/N)_{\min}} \tag{6}$$

When the minimum SNR is known as shown in equation (6), the maximum detection distance can be calculated. The minimum SNR is determined from the false alarm probability and the detection probability [4]. The graph of Fig. 5 shows the false alarm probability when the x-axis is the SNR and the y-axis is the detection probability. Generally, the SNR at the detection probability 99% and the false alarm probability 10^{-10} is determined as the minimum SNR, which is about 16 dB. Since the radar SNR

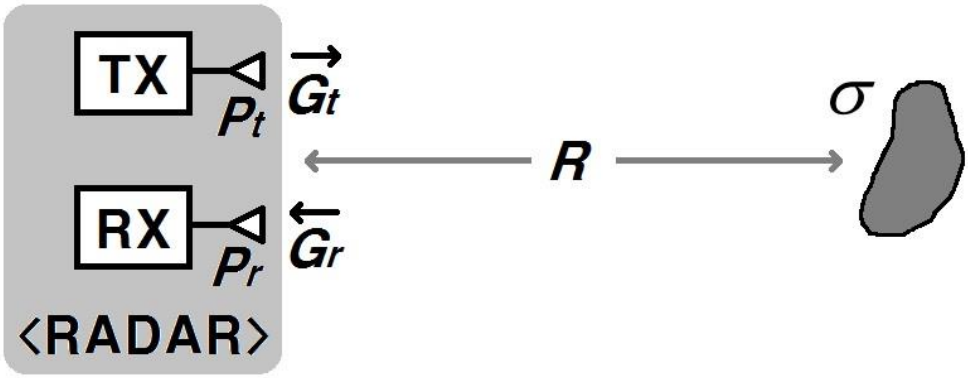

Fig. 4. Detecting target at a distance of R from the radar.

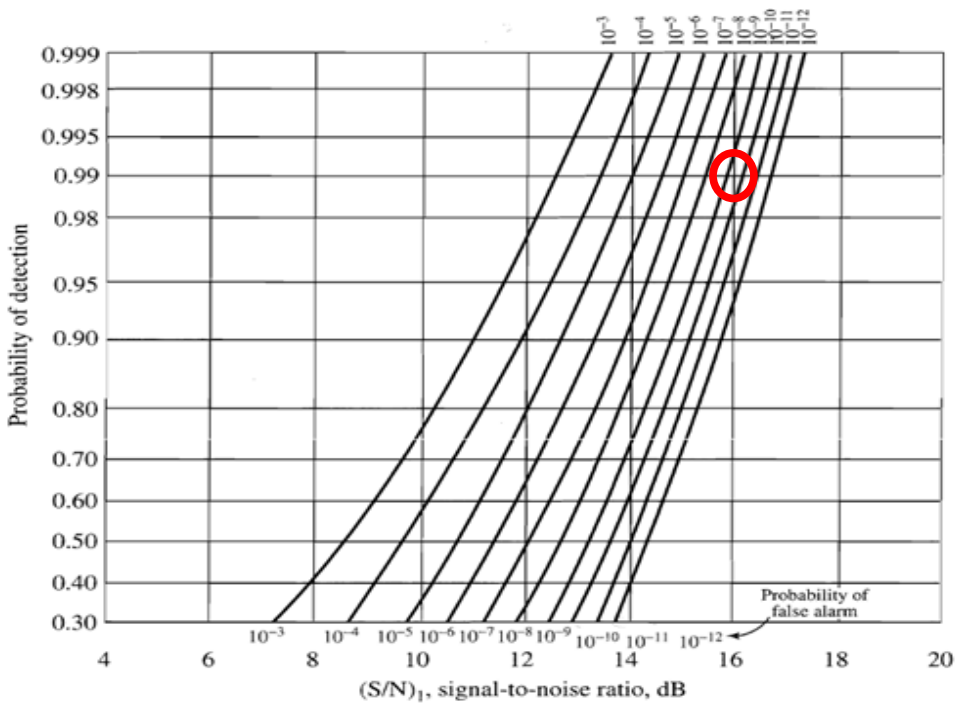

Fig. 5. Minimum SNR according to detection probability & false alarm probability.

determines the maximum detection distance of the radar, it is a measure of the sensitivity of the radar. One of the factors that greatly affect the SNR is the phase noise of the signal source. The phase noise of signal source directly determines the radar sensitivity as shown in Fig. 6. The reflected signal will be extremely low power and can be overshadowed by an oscillator with too much noise [5]. Therefore, designing a low-phase-noise FMCW radar is one of the most important ways to increase the

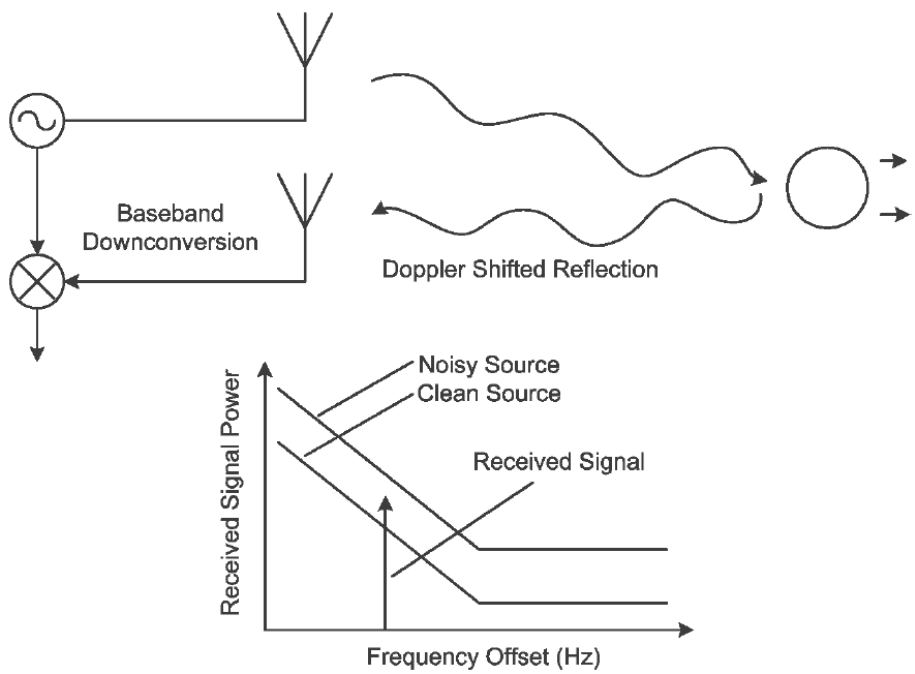

Fig. 6. A simplified Doppler shift radar system demonstrating the effects of phase noise on the downconverted Doppler shift.

maximum detection distance of a radar.

Fig. 7 shows process technology trend. In millimeter-wave frequencies, SiGe technologies have been widely used from the past due to high cut-off frequency and breakdown voltage [6], [7]. With the recent performance development of CMOS devices, CMOS can be applied to mm-wave radar systems [8]-[10]. Although CMOS radar systems have some advantages, such as low cost and high integration, the phase-noise performance should be improved further in order to compete with SiGe radar systems. Thus,

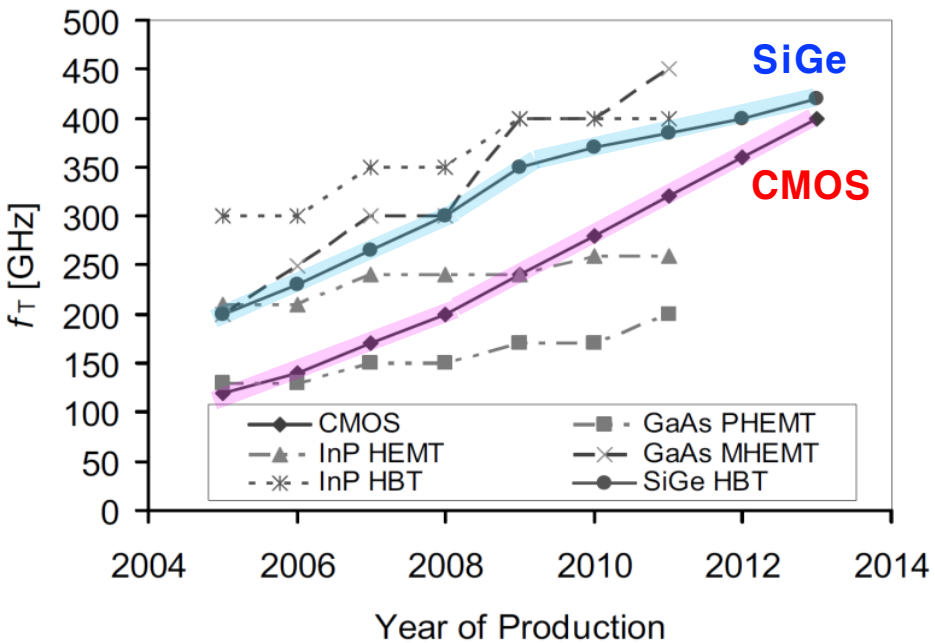

Fig. 7. Process technology trend.

achieving a low-phase-noise signal generator in CMOS has been a significant issue. Several approaches to designing a low-phase-noise 77-GHz FMCW signal generator are employed in this thesis. The first approach is to use a frequency multiplier. A VCO suffers from high phase noise due to poor transistor gain as well as the low quality factor of varactors at mm-wave frequencies. Therefore, despite consuming more DC power, combining a lower frequency VCO and a frequency multiplier can be a more appropriate solution than direct mm-wave oscillation for the mm-wave low-phase-noise performance [11]. Secondly, the proposed 77-GHz signal generator is designed with an injection-locked (IL) oscillator (ILO) chain, which is a powerful tool to realize low-phase-noise oscillators with good harmonic suppression at mm-wave frequencies [12]. Since the phase noise of the ILO chain is determined by the injected signal purity, the low frequency VCO should be designed to have low phase noise characteristics using the appropriate technique, which is the third approach. In this thesis, two versions of the 77-GHz signal source were presented, each of which was implemented using a $\times 6$ frequency multiplier and a $\times 28$ multiplier. Since it is important to design a VCO with low noise characteristics with the appropriate techniques at the frequency before being multiplied. A linearized transconductance (LiT) VCO at 12.8 GHz and a class-C VCO at 2.75 GHz were designed and improved with circuit ideas in this research.

Chapter 2. Frequency and Architecture Selection

Before designing a 77-GHz FMCW radar transmitter chip with a frequency multiplier, the most important thing to consider is determining the architecture and the frequency of the transmitter. When the 77-GHz signal generator including the VCO, the buffer and the frequency multiplier is designed as an ILO chain as in the previous study, the final output phase noise characteristics is determined by the phase noise characteristics of the first stage oscillator of the ILO chain. Therefore, it is necessary to set the frequency of the first stage oscillator and the multiplication factor (N) of the frequency multiplier, which are advantageous for low phase noise characteristics. Considering the system implementation issues such as the frequency locking ranges and DC power consumption of cascaded frequency multipliers, the appropriate number of frequency multiplier stages should be determined. In this research, thus, a ×6 frequency multiplier, which is a combination of ×3 multipliers and ×2 multipliers, and a ×28 multiplier that combines ×7 multipliers and two-stage ×2 multipliers have been developed in our group. A low-phase-noise 77-GHz signal generator should be designed by combining these two multipliers with a low-phase noise VCO at each pre-multiplication frequency.

In the relatively high 12.8-GHz frequency band, it is difficult to apply the class-C technique, known as providing the lowest phase

noise performance, because of the parasitic components, so the LiT VCO, suitable for low phase noise characteristics in that band, will be explained in chapter 2.1. In chapter 2.2, the class-C VCO will be described in detail as a suitable scheme for low-phase-noise VCO design in the 2.75-GHz band. In chapter 2.3, we will briefly explain what the ILO chain is and then use it to show the benefits of phase-noise characteristics when designing a 77-GHz signal generator. Finally, a summary will be covered in Chapter 2.4.

2.1. LiT VCO

It is widely known that phase noise in CMOS LC VCOs is fundamentally limited by the oscillation amplitude and the inherent device noise. A new approach based on transconductance linearization of the active devices, so called LiT (Linearized Transconductance) VCO, that increases the signal swing while reducing the active device noise contribution in LC VCOs in year

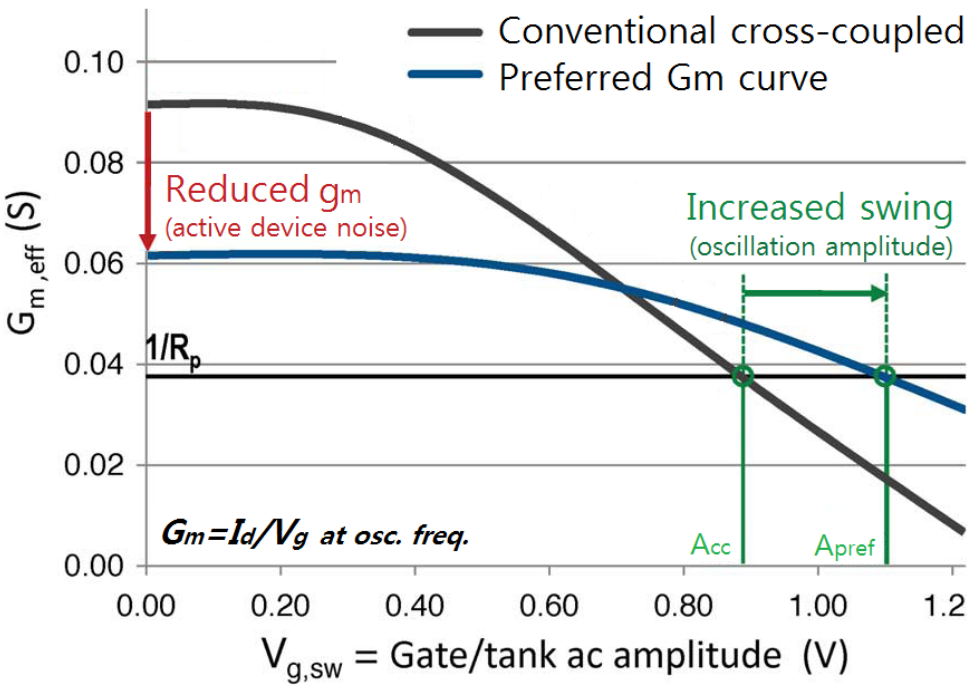

Fig. 8. G_m versus voltage swing showing a typical oscillator curve and a preferred curve for improved phase noise.

2013 [13]. The oscillation amplitude is usually limited by the non-linearity of the large signal transconductance (G_m). The effective transconductance ($G_{m,eff}$) versus gate ac voltage swing showing a typical oscillator curve and a preferred curve for improved phase noise is presented in Fig. 8. From these curves, two important observations can be seen. The first one is about the oscillation

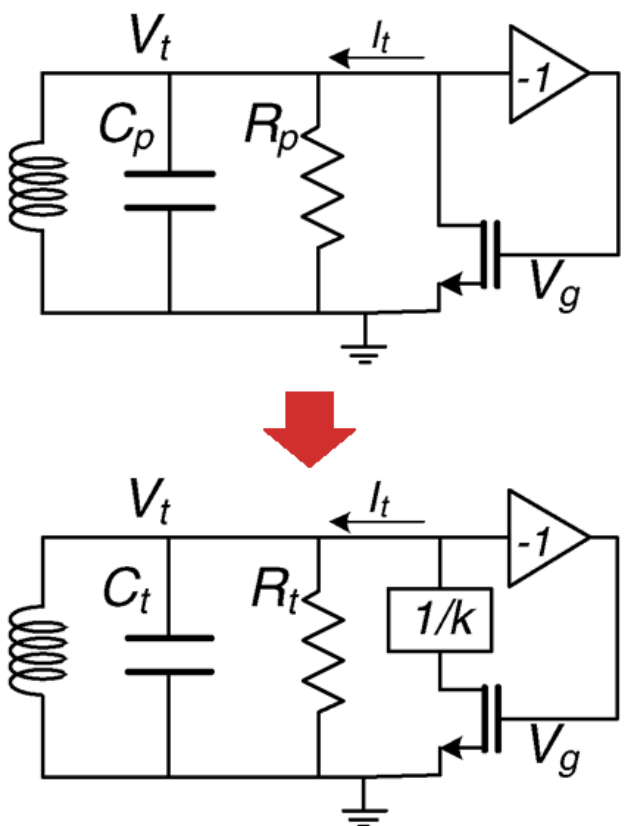

Fig. 9. Feedback concept for LiT using lower voltage swing on the drain node.

amplitude. As shown in the figure, the $G_{m,eff}$ drops with increasing oscillation amplitude. The equilibrium amplitude A_{cc} is reached when $G_mR_p=1$. The main source of nonlinearity is the transistor entering the triode region. The second one is the active device noise. Fig. 8 also shows the small-signal transconductance (g_m) corresponding to G_m for an infinitesimally small amplitude of oscillation. Note that this g_m determines the active device noise power at the oscillation zero crossings (when the oscillator's phase noise sensitivity is at its highest). As a result, with other factors remaining constant, the device g_m is a significant determinant of the VCO phase-noise performance. From these two observations, a more linear G_m curve (blue line in Fig. 8) realizes larger oscillation amplitude and lower active device noise, thereby improving SNR. Consequently, the phase noise characteristic of the VCO can be improved [13].

The conceptual feedback scheme in Fig. 9 can achieve the desired linearization because the drain node in the MOSFET is mainly responsible for large signal nonlinear device G_m. A portion of the tank/gate amplitude is fed to the drain, reducing swing at the drain. The result is a reduction in triode behavior that linearizes the G_m curve. This feedback scheme can be implemented using a capacitive divider as shown in Fig. 10 (a).

This LiT VCO solves two problems that worsen phase noise and shows improved phase noise performance. However, since the LC tank is connected to the gate node, a large-sized choke inductor is required at the drain node for VDD bias. Relatively complicated

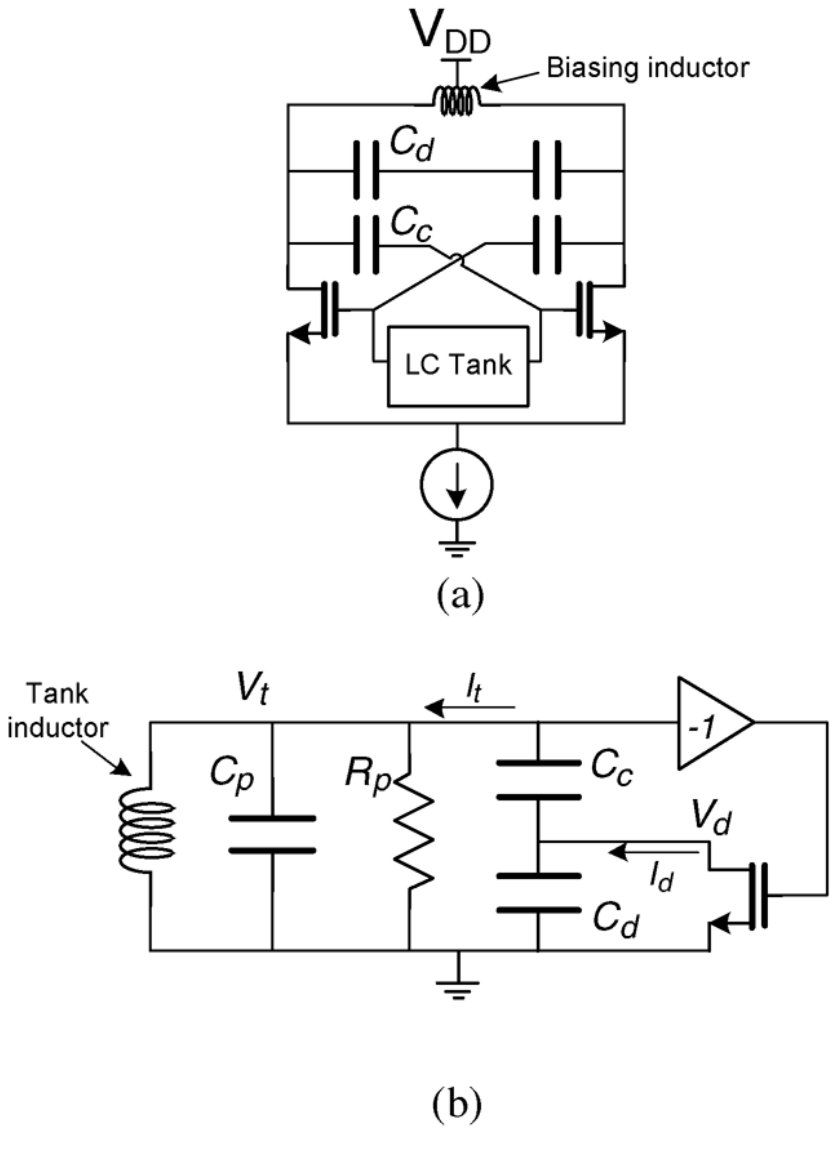

Fig. 10. LiT VCO: (a) full circuit and (b) half circuit

layout are also required because the feedback is formed by a complex capacitor divider network. Thus, an improved LiT VCO for solving these problems of existing LiT VCO has been proposed in this paper, and details can be found in chapter 3.1.

2.2. Class-C VCO

Since the publication of the first class-C VCO paper in 2008, numerous class-C VCO papers have been published because they have much better phase noise performance than conventional VCOs. Compared with an LC cross-coupled VCO, the class-C VCO provides better phase noise performance due to its low gate-bias

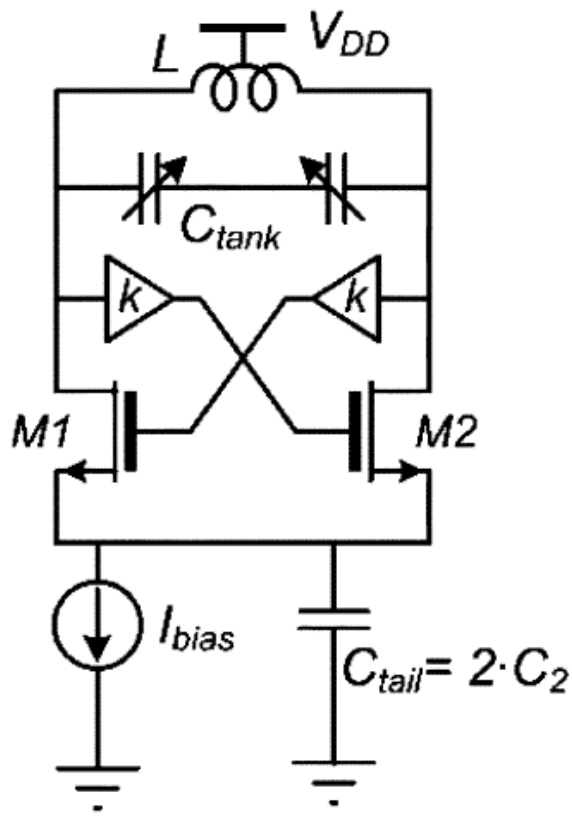

Fig. 11. Schematic of the class-C LC-tank oscillator.

voltage, which can be explained by impulse sensitivity function [14]. A schematic of the class-C LC-tank oscillator is shown in Fig. 11 [15]. For a class-C VCO (Fig. 11), the drain current of the switching transistors (M1/M2) is a pulse wave instead of a near rectangular wave in a conventional LC-tank VCO, as in Fig. 12. The class-C operation generates impulse-like fundamental drain current with much higher efficiency, resulting in much higher oscillation voltage amplitudes versus a given current consumption. Fig. 13 shows MOS current waveforms and amplitude of the

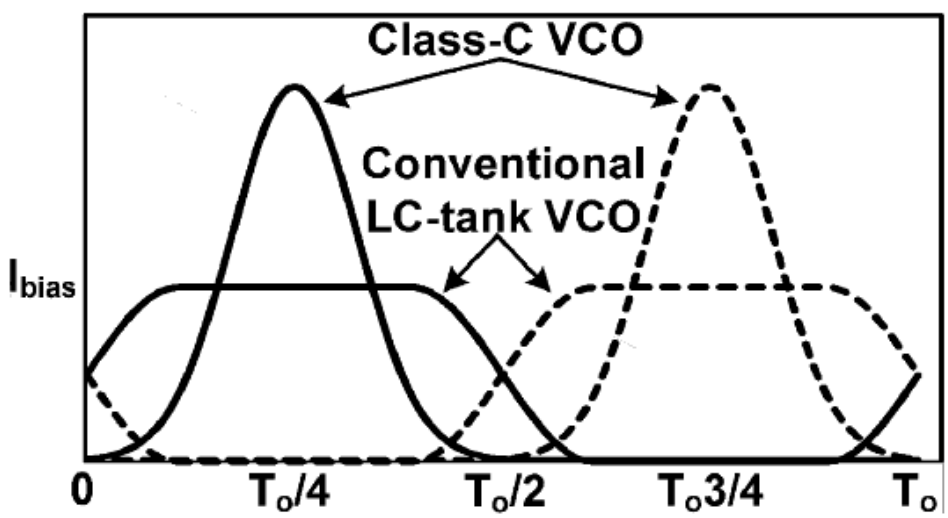

Fig. 12. Drain current of the FETs for conventional LC-tank VCOs and class-C VCOs.

fundamental current harmonic in the class-C oscillator (top), differential pair LC-tank oscillator (bottom). In a typical LC VCO, the transistor has a conduction angle of half of the oscillation period, and the drain current at this time has a square-like waveform with 50% duty. In the case of a class-C VCO, however, the transistor has a much smaller conduction angle than half the oscillation period due to the low gate bias voltage. The drain current has an impulse-

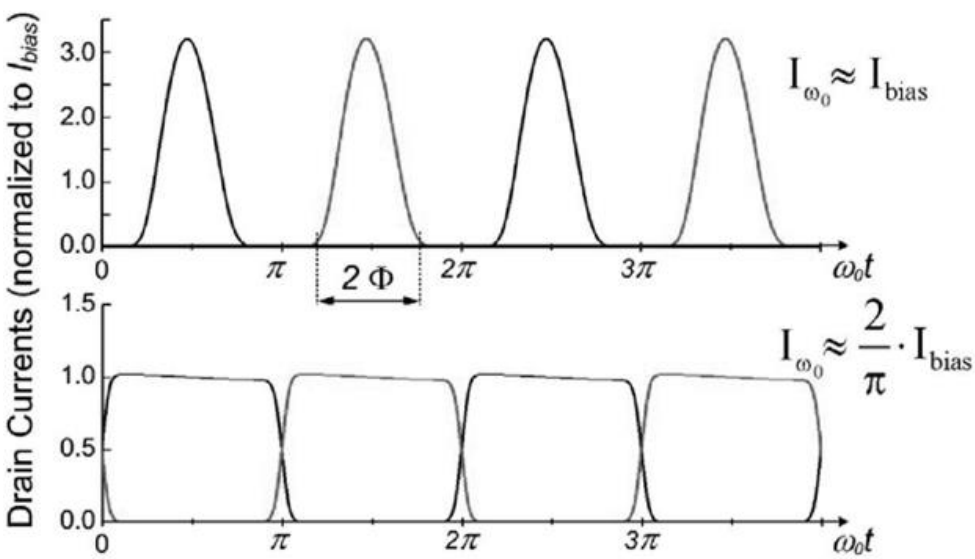

Fig. 13. MOS current waveforms and amplitude of the fundamental current harmonic in the class-C oscillator (top), differential pair LC-tank oscillator (bottom).

like waveform because the transistor is turned on only for a short time. As demonstrated in [16], ideal Class-C operation results in a 36% lower bias current, compared to the conventionally used Class-B oscillator, for the same oscillation amplitude and phase noise. This is because the conversion of bias current into fundamental current harmonic is more efficient in Class-C (with an ideal conversion factor α_C equal to 2) than in Class-B (ideal conversion factor $\alpha_B = 4/\pi$). Therefore, the theoretical phase noise improvement for the same current consumption, compared to the standard differential-pair LC-tank oscillator, is 3.9 dB.

Although the class-C VCO has an advantage of providing a very good phase noise performance, it is not suitable for a relatively high frequency application because it is difficult to realize a sharp impulse-like drain current waveform due to the parasitic capacitance. Therefore, in order to generate a 77-GHz signal with the class-C VCO, there is no other way to connect multiple frequency multipliers in series.

Also, since a class-C VCO has inevitable startup problems due to its low gate-bias voltage, there have been several attempts to achieve robust startup such as hybrid VCOs [16], [17], a dual-conduction VCO [18], an adaptive bias scheme [19] and an automatic startup loop [15]. However, the hybrid and dual-conduction topologies, which are secure approaches for robust startup, are not sure solutions in that a free-running auxiliary pair distorts the class-C waveform and degrades the steady-state

phase noise performance. A class-C VCO with the automatic startup loop shows good performance, but it has reliability issues because of its switching operation. An adaptive bias scheme is generally known as a way to easily get a robust startup, but there is a need for an improved scheme that can guarantee startup more reliably.

A method with lower phase noise characteristics (similar to an adaptive bias scheme) than hybrid or dual-core VCO, with improved startup (similar to a hybrid or dual core VCO) over adaptive bias scheme, has been proposed in this paper. More details will be covered in chapter 4.1.

2.3. Injection-Locked Oscillator Chain

The injection-locked (IL) oscillator is characterized in that, when an external signal having a frequency similar to that of the free oscillation frequency is injected, the oscillator synchronizes with the injected signal and outputs the same frequency as the injected frequency [20]. It is one way to make an oscillator that is injected and synchronized at the same frequency and has low phase noise characteristics, such as a signal injected at the desired frequency. There is a problem that it is difficult to fix the phase noise characteristic and the phase when designing the oscillator in the high frequency band. Thus, by designing the low-phase-noise VCO in the low frequency band (f_0) and synchronizing the high

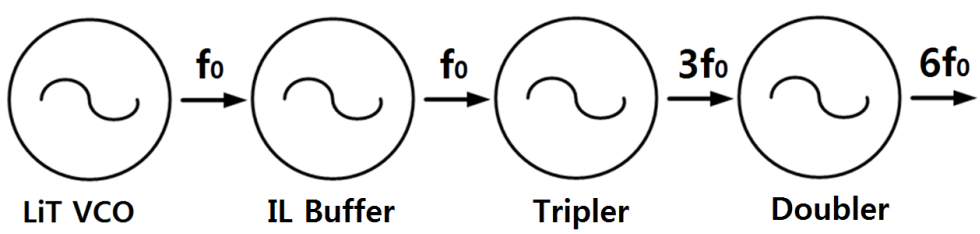

Fig. 14. A four-stage injection locked oscillator chain structure of the proposed 77-GHz signal generator with the ×6 frequency multiplier.

frequency oscillator with the injection lock as the harmonic component (n^{th}) of the VCO output signal, it is possible to design a high frequency ($n \times f_0$) signal generator with good phase noise characteristics.

Fig. 14 shows an example of a four-stage IL oscillator (ILO) chain structure of the proposed 77-GHz signal generator with the $\times 6$ frequency multiplier. Initially at frequency f_0, the LiT VCO generates a low-phase-noise signal that is injected into a free-running oscillator (IL buffer). The 3^{rd} harmonic component of the output signal of the IL buffer is injected into the freely oscillating tripler near the $3f_0$ and the tripler oscillation frequency is locked at exactly $3f_0$. Likewise, the 2^{nd} harmonic component of the tripler output signal (i.e., $6f_0$) is injected into the freely oscillating doubler

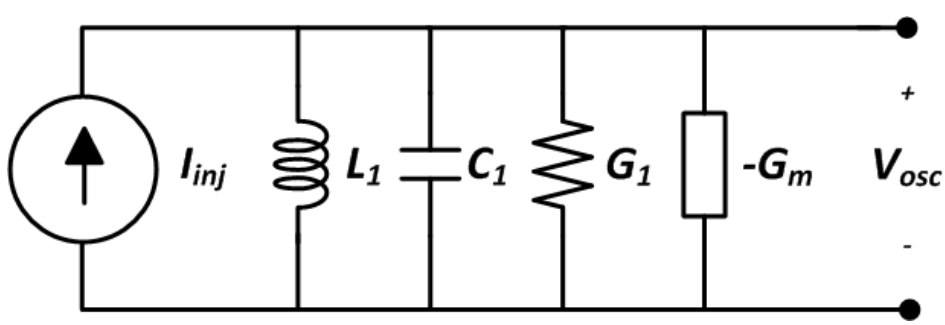

Fig. 15. Simple equivalent circuit of injection-locked oscillator load.

near the $6f_0$ and the doubler oscillation frequency is locked at exactly $6f_0$.

In order to analyze the phase noise characteristics of the injection locked oscillator in detail, an injection locked oscillator is shown as an equivalent model as shown in Fig 15 [21]. Fig 15 shows a simple one-port modeling of the resonant load when an external signal is applied and G1 is the loss of the resonant load. The circuit in the figure can be expressed simply by the equation (7) as follows.

$$C_1\frac{d^2V_{osc}}{dt^2}-(G_1-G_m)\frac{dV_{osc}}{dt}+\frac{1}{L_1}V_{osc}=\frac{dI_{inj}}{dt} \tag{7}$$

$I_{inj}(t)$ and $V_{osc}(t)$ can be expressed by the equations (8) and (9), respectively, and $V_A(t)$ is the amplitude of the output signal.

$$I_{inj}(t)=I_{inj,p}\cos w_{inj}t=Re\{I_{inj,p}\exp(jw_{inj}t)\} \tag{8}$$

$$V_{osc}(t)=V_A(t)\cos(w_{inj}t+\theta)=Re\{V_A(t)\exp(jw_{inj}t+j\theta)\} \tag{9}$$

Equations (8) and (9) can be substituted into (7) and the real and imaginary parts can be represented by expressions (10) and (11), respectively.

$$C_1\frac{d^2V_A}{dt^2}-C_1\left(w_{inj}+\frac{d\theta}{dt}\right)^2V_A+(G_1-G_m)\frac{dV_A}{dt}+\frac{1}{L_1}V_A = w_{inj}I_{imj,p}\sin\theta \tag{10}$$

$$2C_1\left(w_{inj}+\frac{d\theta}{dt}\right)\frac{dV_A}{dt}+C_1\frac{d^2\theta}{dt^2}V_A+(G_1-G_m)\left(w_{inj}+\frac{d\theta}{dt}\right)V = w_{inj}I_{imj,p}\cos\theta \tag{11}$$

Several assumptions were made to simplify this equation. The output signal moves slowly in very small amounts, the LC resonator load is $R_p=G^{-1}=QL_1w_0$, $w^2_{inj}-w^2_0=2w_0(w_0-w_{inj})$, and $w_{inj}=w_0$. Finally, assuming that the phase of the signal changes slowly, equations (8) and (9) can be simplified to equations (10) and (11).

$$\frac{d\theta}{dt}=w_0-w_{inj}-\frac{w_0I_{inj,p}}{2QI_{osc,p}}sin\theta \tag{12}$$

$$\frac{dV_A}{dt}+\frac{G_1-G_m}{2C_1}V_{env}=\frac{I_{inj,p}\cos\theta}{2C_1} \tag{13}$$

If the applied signal and the free oscillation signal are synchronized, we can express it as an equation (14).

$$\left(\frac{w_0-w_{inj}}{w_L}\right)^2+\left(\frac{G_1-G_m}{I_{inj,p}}V_{A,p}\right)^2=1,\ G_m=G_1-\frac{V_{A,p}}{I_{inj,p}} \tag{14}$$

In this case, if the injection lock oscillator is successfully locked, the LC resonator loss is reduced by $V_{A,p}/I_{inj,p}$ from the free oscillation state loss G1, so that the phase noise characteristic of

the injection lock oscillator is improved compared with that of a general oscillator. Intuitively, there is an effect of lowering the jitter accumulation in terms of time domain as the injection signal is synchronized with the oscillation signal at the zero crossing for every cycle.

It can be found out in Fig. 16 that when the external signal having low-phase-noise characteristic is injected into the oscillator having the high-phase-noise characteristic in the free oscillation state, it has a low-phase-noise characteristic of the injected external signal as shown in the figure when it is locked.

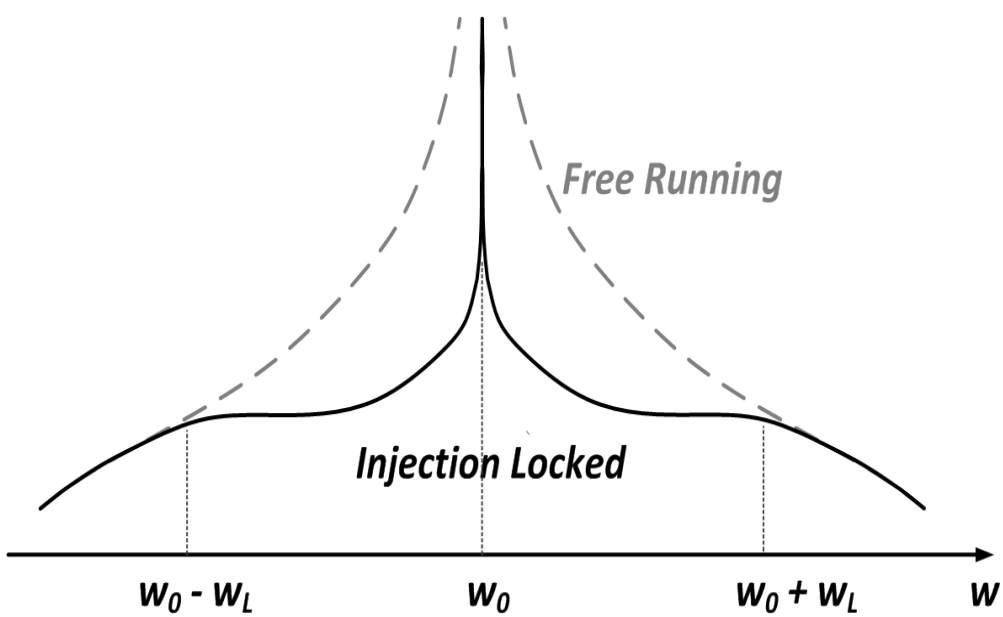

Fig. 16. Phase noise reduction by injection-lock technique.

2.4. Summary

In this thesis, in order to generate a 77-GHz low-phase-noise signal was significantly access in three ways. The first approach is to apply a frequency multiplier. At mm-wave frequencies, a VCO suffers from high phase noise due to poor transistor gain as well as the low quality factor of varactors. Therefore, despite consuming more DC power, combining a lower frequency VCO and a frequency multiplier can be a more appropriate solution than direct mm-wave oscillation for the mm-wave low-phase-noise performance. The second approach is to design a VCO with very low phase noise at low frequencies. In this paper, two versions of the 77-GHz signal generator were designed using a ×6 frequency multiplier and a ×28 multiplier, and in each case the problems of the existing LiT VCO and class-C VCO were improved. Finally, a third approach is to use the ILO chain. After designing an improved LiT, class-C VCO with very low phase noise characteristic at low frequencies, the harmonic component of this output signal was injected and locked to the corresponding high frequency oscillator. When constructing a multi-stage ILO chain, the frequency lock range is reduced and power consumption is increased. However, an automotive FMCW radar systems only require a narrow frequency band and battery capacity will be sufficient. Therefore, with the above three approaches, a low-phase-noise 77-GHz FMCW radar transmitter chip could be designed well.

Chapter 3. 77-GHz FMCW Radar Transmitter with 12.8-GHz PLL and ×6 Frequency Multiplier

At the beginning of Chapter 2, it was mentioned that there were two approaches to select frequency and architecture. One method (version 1) of them is to combine a ×6 frequency multiplier and a 12.8−GHz PLL. The block diagram of the proposed 77−GHz radar TX is shown in Fig. 17. It consists of a 77−GHz signal generator, a driver amplifier, a power amplifier and PLL blocks. Because the signal generator is implemented with the ILO chain without requiring gain buffers after each ILO, the DC power consumption and chip area can be decreased. Moreover, harmonic suppression, which is one of the main concerns of the multiplier−based system, can be improved by the ILO chain because each oscillator acts as a narrow band−pass filter. A PLL is composed of a current−mode logic (CML) divider, seven stages of true−single−phase−clock (TSPC) divider, a phase frequency detector (PFD), a charge pump (CP), and a loop filter.

In chapter 3.1, an improved LiT VCO design and PLL (phase locked loop) will be discussed in detail. The VCO used in the 12.8−GHz PLL was designed using LiT technology to have low−phase−noise characteristics and was designed to be simpler than the existing LiT VCO using a 3: 2 transformer. The other RF blocks

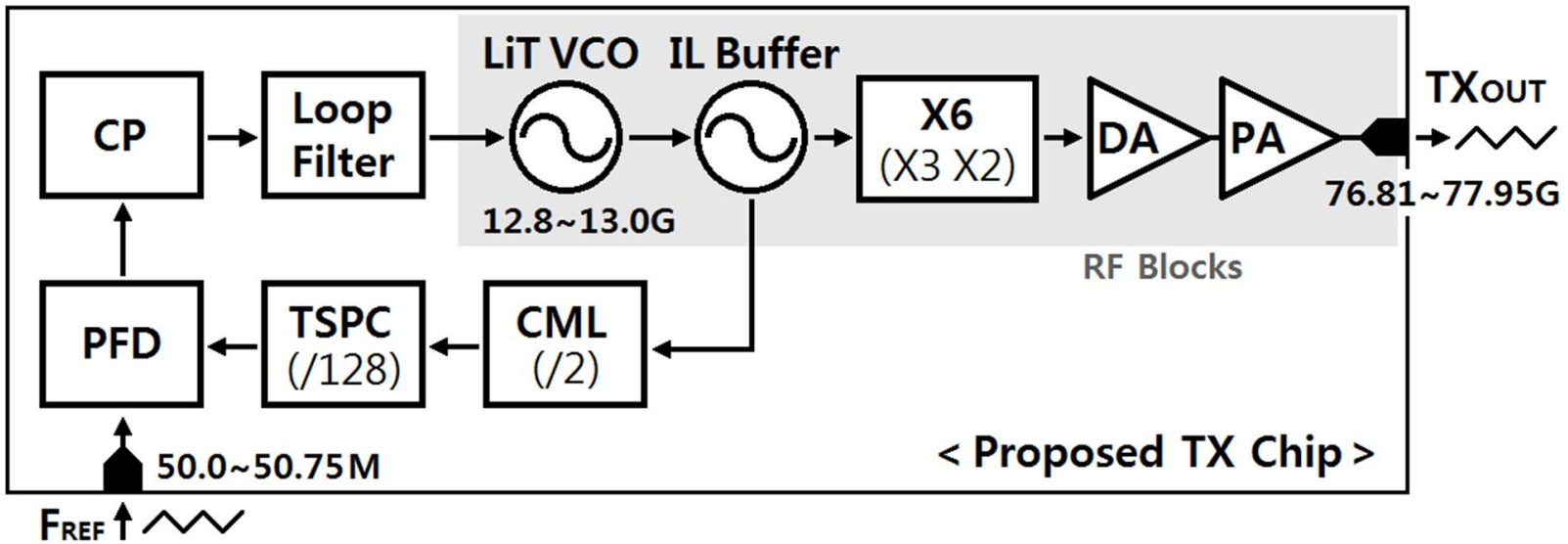

Fig. 17. Block diagram of the proposed 77−GHz TX chip.

that make up the transmitter chip except VCO, VCO buffer, and PLL blocks will be covered in chapter 3.2. The measurement results are shown in chapter 3.3, and finally the summary will be placed in chapter 3.4.

3.1. Proposed LiT VCO and PLL

Fig.18 shows the proposed LiT VCO schematics. It is well known that the phase noise characteristic of a VCO is fundamentally due to the oscillation amplitude limit and the inherent noise of the transistor itself. Recently, LiT technology has been developed to solve the above problems and improve the phase noise

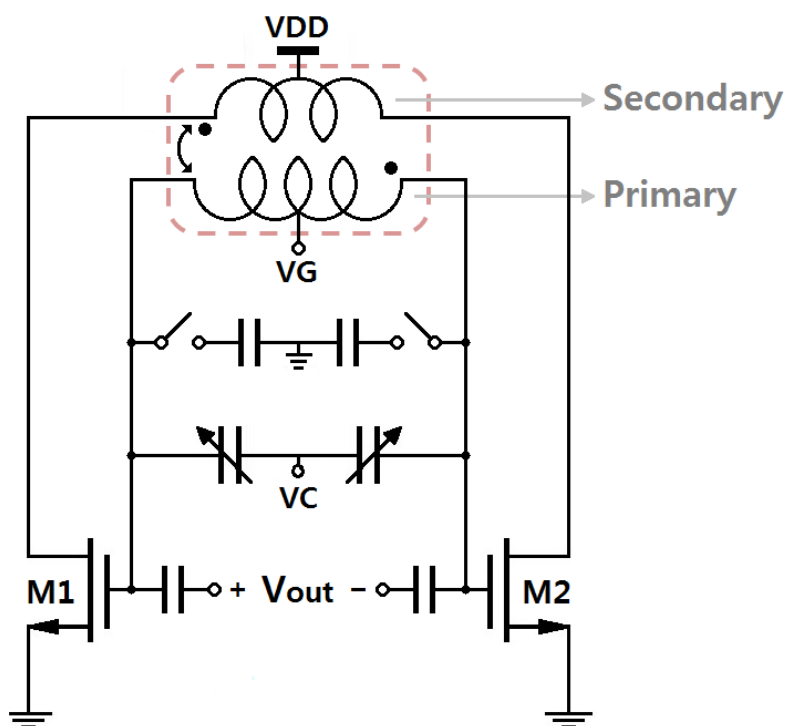

Fig. 18. Schematic of the proposed improved LiT VCO.

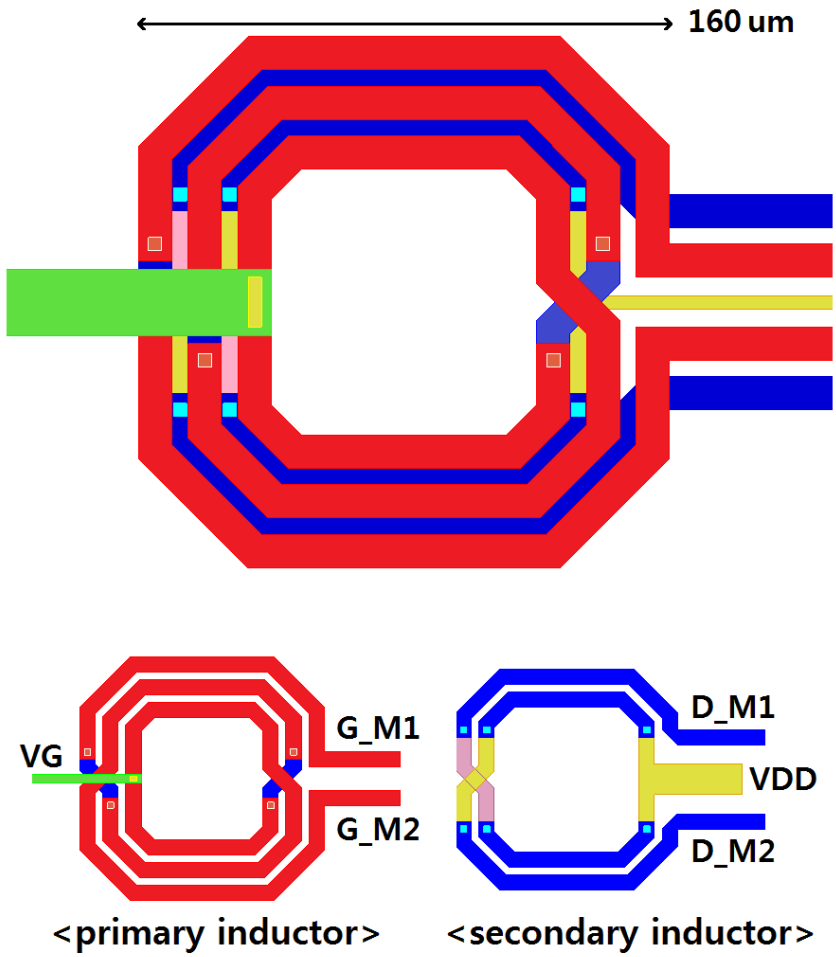

Fig. 19. Designed 3:2 transformer for the proposed LiT VCO.

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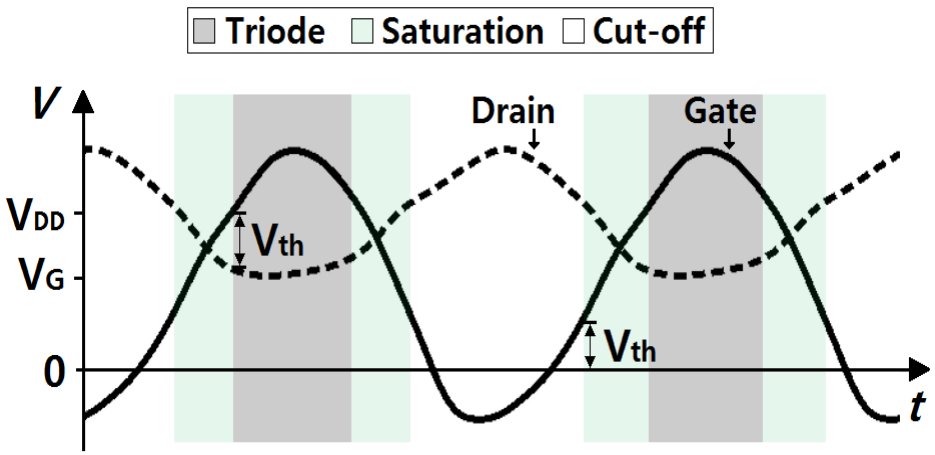
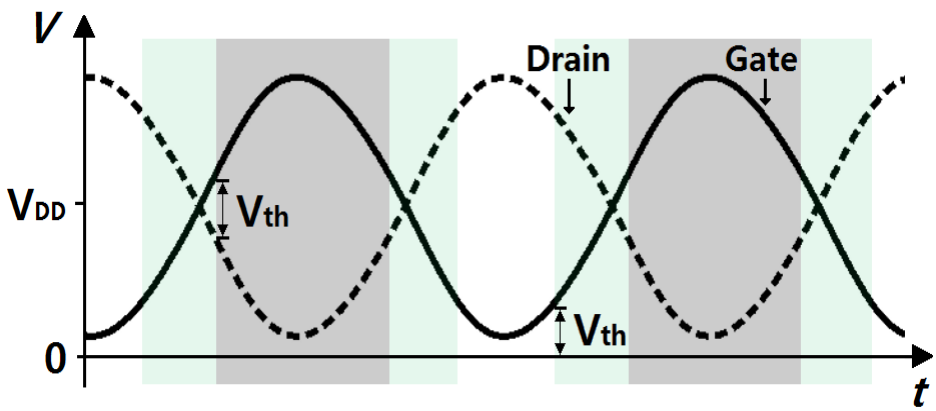
characteristic of VCO [13]. As described in Chapter 2.1, the LiT technology reduces noise in small signals and increases amplitude in large signals, resulting in good phase noise characteristics. Unlike conventional cross-coupling schemes, a feedback scheme in which the amplitude of the voltage waveform at the drain node of the VCO core transistor is less than the amplitude of the voltage waveform at the gate node should be used. The existing LiT VCO uses complex capacitor divider circuits to obtain this waveform and connects the LC resonator to the gate node of the core. Since the LC resonator is connected to the gate, a very large choke inductor, which appears to be open in AC, must be connected to supply the VDD voltage to the drain node. A complex capacitor divider circuit and a very large choke inductor are added to the VCO, resulting in chip area increase and layout complexity.

In order to solve the problems mentioned above, to replace the role of choke inductors of the LC resonator and the drain node connected to the capacitor divider circuit and the gate node with a simple and compact 3:2 transformer is proposed [31]. Fig. 18 shows a schematic of the proposed LiT VCO and Fig. 19 presents a designed 3:2 transformer for the proposed LiT VCO. The diameter of the outermost coil of the designed 3: 2 transformer primary inductor is 160 μm. The primary inductor with a turn number of three is connected to the gate node of the VCO core and the inductance measured by EM-simulation is 324 pH at 12.8-GHz. Secondary inductors with a turn number of 2 are connected to the



(a)



(b)

Fig. 20. (a) Simulated waveforms of a 3:2 transformer based LiT VCO, (b) Those of a conventional LC VCO.

drain node, and similarly the inductance is 147 pH at 12.8−GHz. Fig. 20 (a) shows a waveform that is suitable for LiT by connecting a primary turn−inductor with a turn number to the gate node and a secondary inductor with a small turn number to the drain node. Comparing Fig. 20 (a) and (b), it can be seen intuitively that the

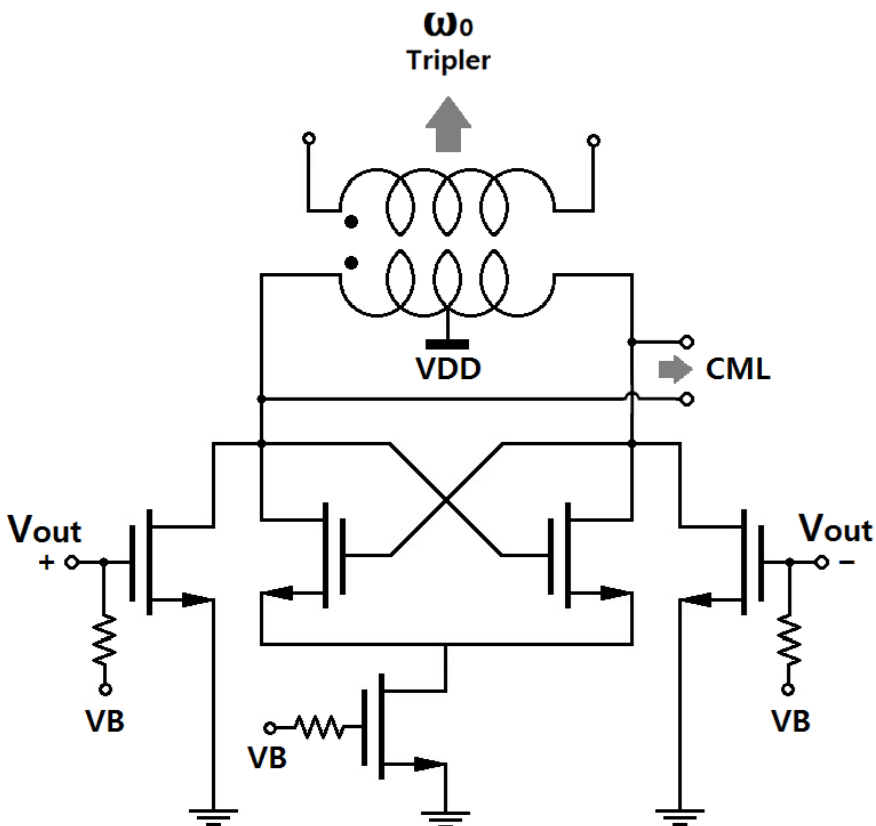


Fig. 21. Schematic of the injection−locked buffer.

general VCO is longer than the LiT VCO in the triode region, which is one of the main causes of VCO nonlinearity. Therefore, it can be concluded that the proposed LiT VCO can obtain improved phase noise characteristics.

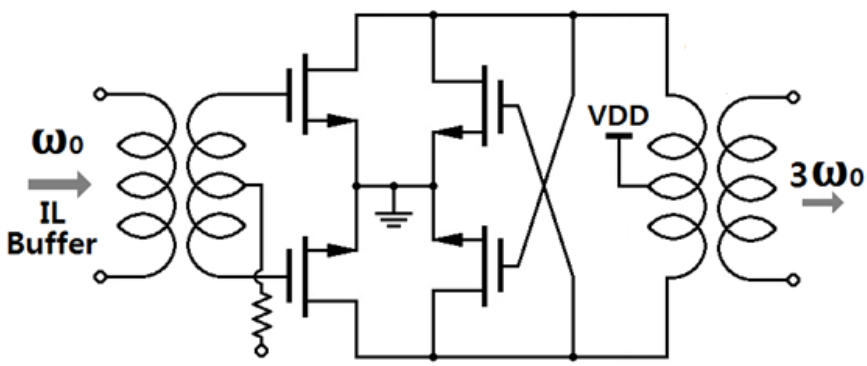
Since the output signal of the VCO must be transmitted to the CML frequency divider and the frequency multiplier of the PLL, respectively, a buffer that provides a large output power is needed. Therefore, a buffer is constructed using an injection-lock oscillator [22]. As shown in Fig. 21, the injection-lock buffer consists of small transistors acting as a buffer, a large cross-coupled transistors serving as a large output power, a current source, and a transformer which transfers the signal to the × 3 multiplier while being used as a load of an injection-locked oscillator. When the output signal of the VCO is injected into the buffer, the oscillation frequency of the buffer is locked by the oscillation frequency of the VCO when the buffer oscillates itself near 12.8-GHz.

In this paper, an integer N-type PLL is designed. The designed PLL consists of a CML divider, a TSPC divider, a PFD, a charge pump and a loop filter. The output signal of the VCO buffer enters the CML frequency divider. Because the CML frequency divider can operate at a relatively high speed without using the resonance structure requiring the inductor, the high frequency input signal of 12.8 GHz is divided into 6.4 GHz. The designed CML divider is commonly used and designed on the basis of a master-slave D flip-flop. The divided signal by CML divided into low-frequency

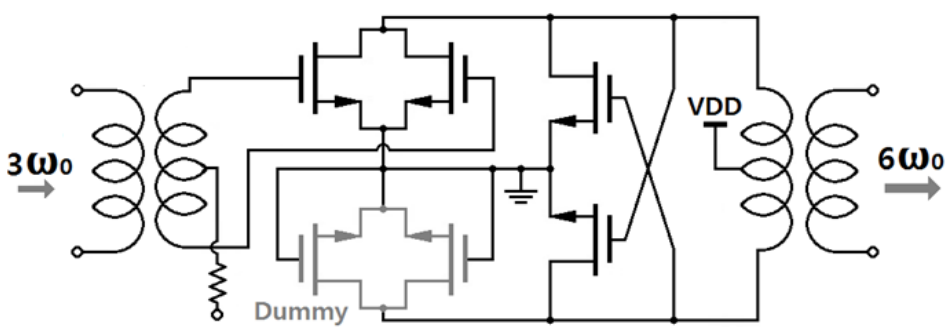
signals of about 50-MHz through the seven-stage TSPC divider. The PFD compares phase and frequency of the divided VCO output signal to those of a reference signal (F_{REF}). The loop bandwidth can be adjusted from 100 kHz to 1 MHz by controlling the CP bias current.

3.2. ×6 Multiplier and Power Amplifier

Fig. 22 is a schematic of a ×6 frequency multiplier. The proposed ×6 multiplier consists of a ×3 frequency multiplier (tripler) and a ×2 frequency multiplier (doubler) connected in series by using an injection-locked oscillator. In general, since the



(a)



(b)

Fig. 22. Schematic of (a) the frequency tripler and (b) the frequency doubler.

output power of the harmonic component exceeding the third order is small, the 2nd or 3rd harmonic component is often used for the frequency multiplier. In this design process, a multiplier using a 3rd harmonic component is used for the first stage, and next, a 2nd harmonic component is used for the second stage. Consequently, a frequency multiplier chain which is multiplied by 6 at a frequency of 12.8 GHz to 77 GHz is designed. The tripler is designed to inject the 3rd harmonic component generated from the VCO buffer into the self-oscillating tripler core near the triple frequency through the injection transistors [23]. The injection-locking range of the 3rd harmonic injection-lock oscillator can be expressed as an equation (15).

$$\left|3 \cdot \omega_{inj} - \omega_0\right| < \Delta\omega_{lock}$$

$$\Delta\omega_{lock} = \frac{\omega_0}{2Q} \cdot \frac{A_{3w_0,\,inj}}{A} \tag{15}$$

Q, ω_0, and A in the equation represent the Q-factor, the resonance frequency of the LC resonator of the oscillator, and the output voltage amplitude of the self-oscillating tripler, respectively. $A_{3wo,inj}$ represents the output voltage amplitude of the VCO buffer. It can be found out from equation (15) that if the Q-factor of the LC resonator of the tripler becomes large, the frequency lock range becomes narrow, so that the output frequency of the tripler cannot follow the frequency of the output oscillation signal of the VCO buffer. Also, the larger the frequency lock range, the greater the

frequency difference between the two signals for frequency synchronization, and thus the more stable circuit can be realized. Therefore, the tripler in this research was designed to ensure a proper frequency lock range. If the tripler is designed to resonate in a band similar to the three-times of output oscillation frequency of the VCO buffer and have an appropriate frequency lock range, then it is advantageous to obtain lower DC consumption voltage and higher RF output power than the amplifier type multiplier (not ILO chain) type do. In the case of a large-signal operation in which the oscillator oscillates in a frequency-synchronized state, the output voltage amplitude V_{out} of the tripler can be expressed by an equation (16).

$$V_{out} = \frac{2}{\pi} \cdot I_{bias} \cdot R_L \tag{16}$$

I_{bias} in equation (16) denotes a bias current switched between the differential stages of the tripler, and R_L denotes a substantial load resistance. If the tripler operates as an oscillator, the output voltage amplitude is determined by the bias current and the actual load resistance. And the loss of the LC resonator is compensated by the negative resistance end due to the cross-coupling pair, thereby obtaining a large output voltage amplitude. Thus, two multipliers can be connected directly without using a gain buffer.

A 38.5-GHz signal with a large output power and three times multiplication is passed through the transformer to the doubler. The doubler uses a method of injecting a signal by adding a push-push

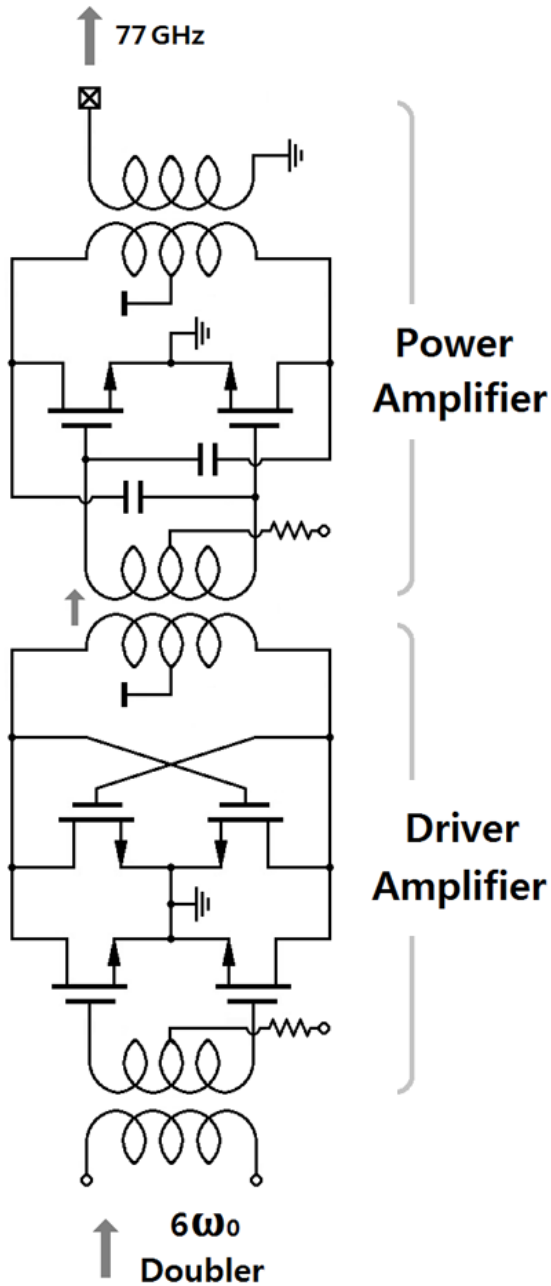
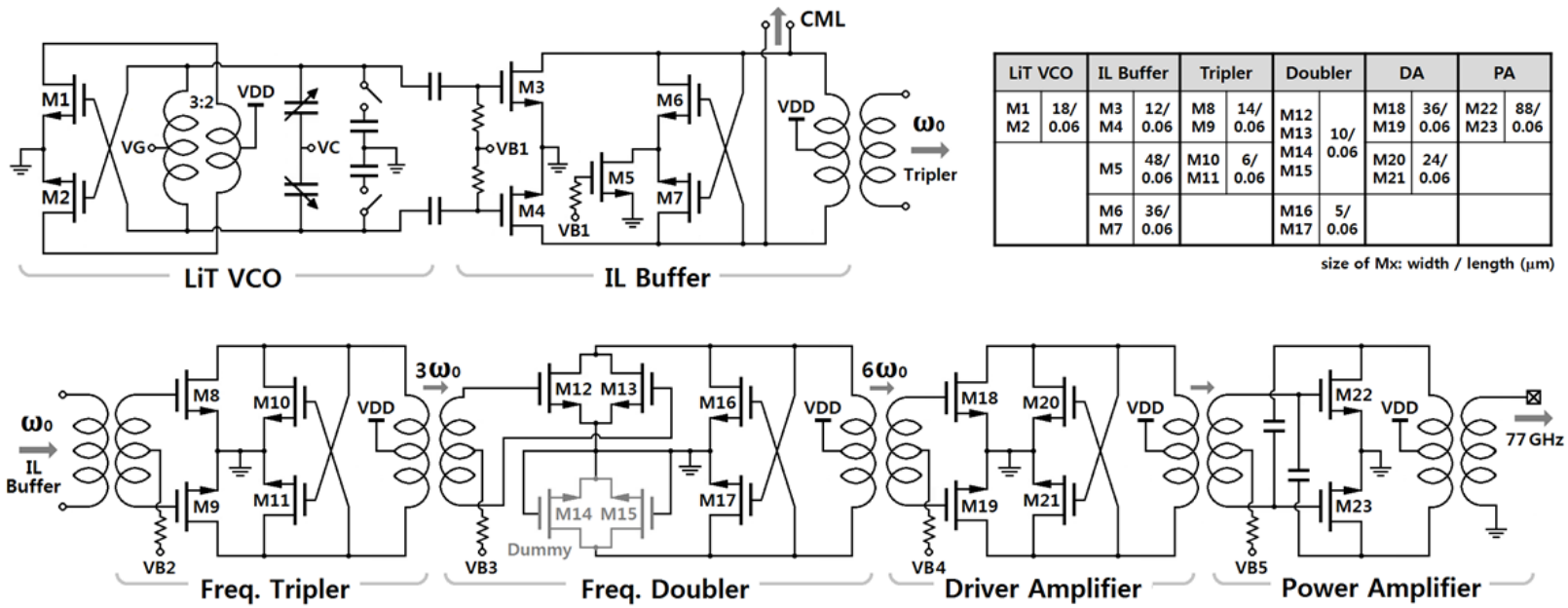


Fig. 23. Schematic of the power amplifier.

cell with a common source structure next to the cross-coupling pair structure. The push-push method is mainly used for a general frequency doubler because it can increase the 2^{nd} harmonic component and remove unwanted odd order components. Since the push-push cell is connected to only one side of the doubler core, a dummy cell is added to the other side to make the resonance load conditions the same. The 2^{nd} harmonic component generated from the push-push cell is injected into the doubler core oscillating freely at near 77-GHz. In order to set the frequency of the oscillator to 77-GHz accurately, both the passive element and the wiring layout of the active element were modeled through EM simulation.

Fig. 23 is a circuit schematic of a driver amplifier and a power amplifier designed to have a sufficiently large output power that the proposed transmitter is suitable for a 77-GHz automotive mid-range and long-range radar. The driver amplifier is designed with a high gain structure using a cross-coupled pair to achieve a large voltage swing with low power consumption [24]. The power amplifier is designed with a neutralization technique to neutralize the C_{gd} parasitic capacitors between the gate and drain nodes by adding capacitors between the drain and the gate in a differential manner in the cross-coupled structure [25]. The gain and stability of the power amplifier have been increased due to this technique. The total schematic of RF blocks is shown in Fig. 24.



LiT VCO		IL Buffer		Tripler		Doubler		DA		PA	
M1 M2	18/ 0.06	M3 M4	12/ 0.06	M8 M9	14/ 0.06	M12 M13 M14 M15	10/ 0.06	M18 M19	36/ 0.06	M22 M23	88/ 0.06
		M5	48/ 0.06	M10 M11	6/ 0.06			M20 M21	24/ 0.06		
		M6 M7	36/ 0.06			M16 M17	5/ 0.06				

size of Mx: width / length (μm)

Fig. 24. Total circuit schematic of RF blocks.

3.3. Measurement Results

3.3.1 LiT VCO Measurement Results

The proposed 13 GHz LiT VCO with the 3:2 transformer is fabricated in 65−nm RF CMOS process. Fig. 25 shows a chip micro−photograph of the proposed LiT VCO and IL buffer. The output frequency and phase noise are measured by an Agilent E4448A spectrum analyzer with RF and DC probing. The measured output frequency tuning ranges are 12.25 GHz ~ 12.86 GHz and 12.86 GHz ~ 13.52 GHz [Fig. 26]. The output power is approximately 7.2 dBm when the VCO core and the IL buffer consume 7.7 mW and 21.6 mW, respectively. The measured phase

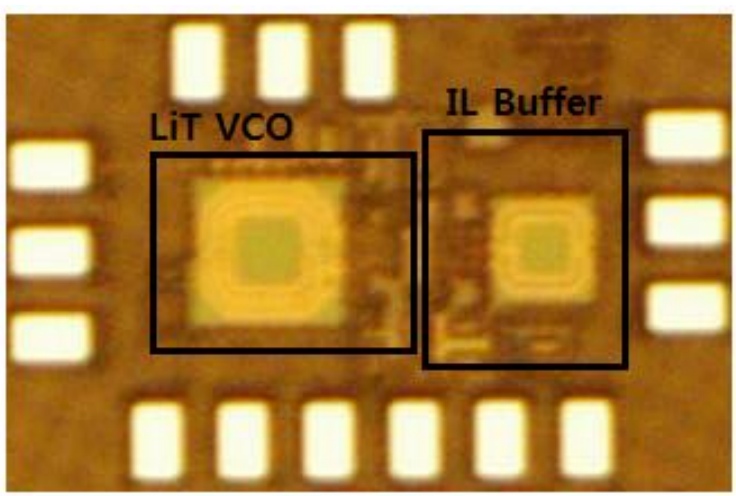


Fig. 25. Chip micro−photograph of the proposed LiT VCO and IL buffer.

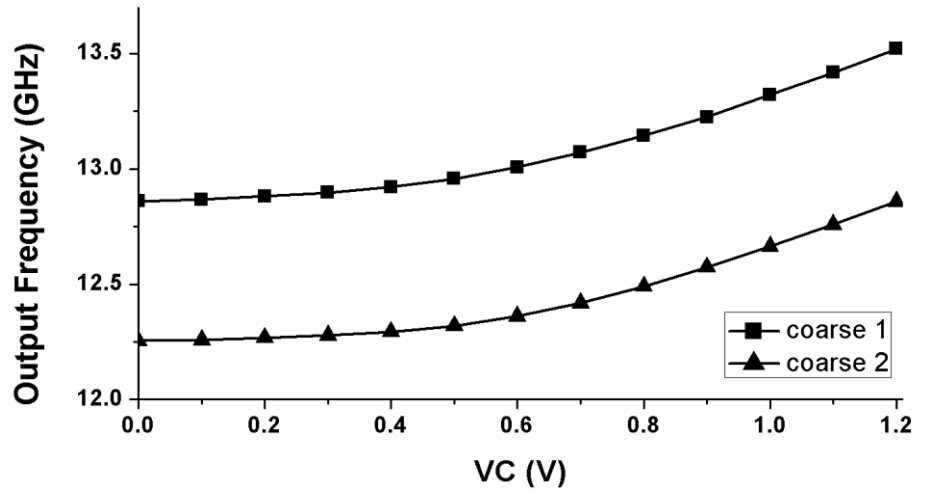


Fig. 26. Measured output frequency.

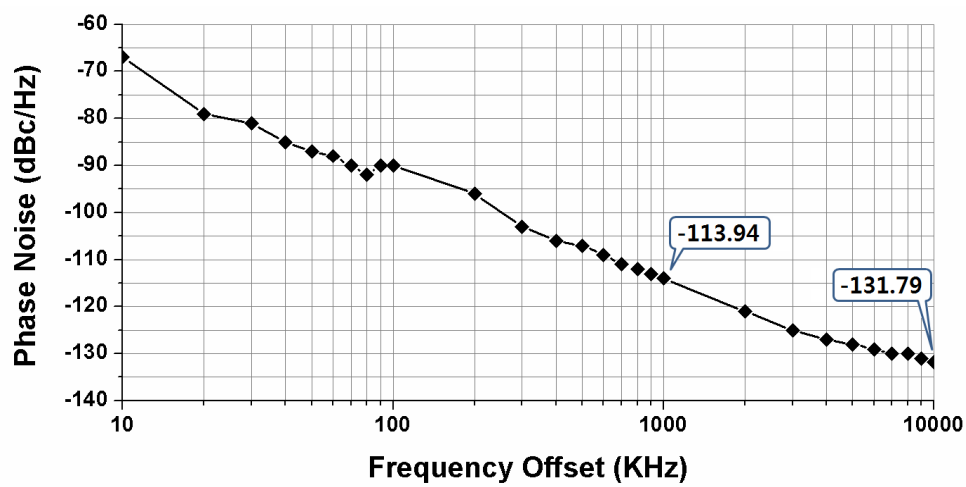


Fig. 27. Measured phase noise when carrier frequency is 13.2 GHz.

noise shows a good value of −113.94 dBc/Hz at 1 MHz offset frequency [Fig. 27]. Fig. 5 shows a micro−photograph of a chip. The chip size is 830 × 530 μm^2, including test pads. Table II highlights the details of the VCO performance. The FOM is determined as below.

$$FOM = -L(\Delta f) - 10\log\{(\Delta f / f_{osc})^2 \cdot P_{dc\_mW}\} \quad (14)$$

$L(\Delta f)$ is the phase noise, Δf is the offset frequency, f_{osc} is the oscillation frequency and P_{dc_mW} is the DC power consumption.

Table II. Performance of the proposed LiT VCO

Technology	65 nm RF CMOS
Tuning Range	Coarse 1: 12.25 ~ 12.86 GHz Coarse 2: 12.86 ~ 13.52 GHz
Phase Noise	-113.94 dBc/Hz @ 1MHz offset
Core DC power	7.7 mW
Buffer DC power	21.6 mW
Output power	7.2 dBm
Full-Chip Size	830 × 530 μm^2
FOM	187.48

3.3.2 77-GHz Transmitter (v1) Measurement Results

The proposed chip was fabricated using a 1−poly 8−metal, 65−nm CMOS process with a top copper metal thickness of 3 μm. Fig. 28 is a microphotograph of the manufactured transmitter chip for a 77−GHz automotive radar. The size of the designed chip is 1.38 × 0.79 mm^2 including the pad. PCB was fabricated for measurement as shown in Fig. 29. DC bias was applied through PCB line and RF output was measured by on−wafer probing using an RF probe capable of measuring up to 110−GHz. The 50−MHz triangular reference signal was applied to the chip on the PCB board using the SMA connector. Fig. 30 presents the equipment settings for measuring the W−band signal output. Since the Agilent E4448A spectrum analyzer cannot measure up to 77−GHz by itself, the output frequency spectrum and phase noise performance are measured by connecting the external mixer. The RF output power was measured using an Agilent N1914A power detector and the output power and output frequency spectrum were simultaneously verified using a −10 dB directional coupler at the output stage. The reference chirp signal was applied to the Agilent E8257D signal generator. The output spectrum measured in the above−mentioned experimental environment is shown in Fig. 31. It is the output spectrum screen when the PLL is locked and the reference signal is 50.1 MHz and the carrier frequency is 76.54 GHz which is 1536 times the reference signal. Because the horizontal axis of the

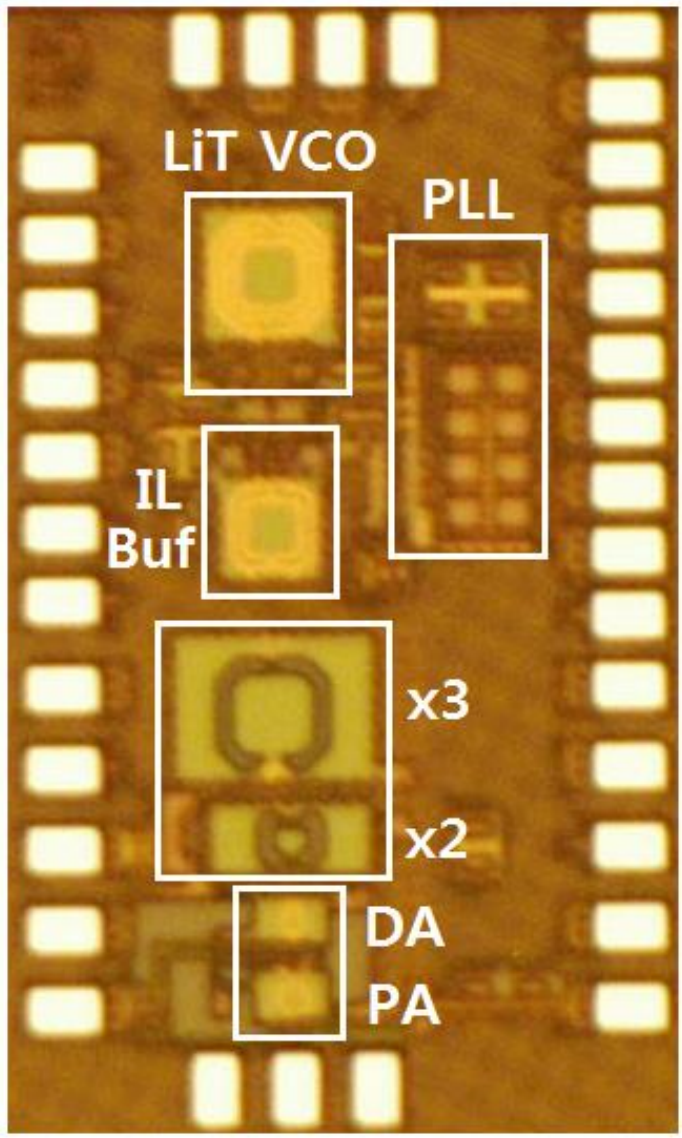


Fig. 28. A microphotograph of the transmitter chip.

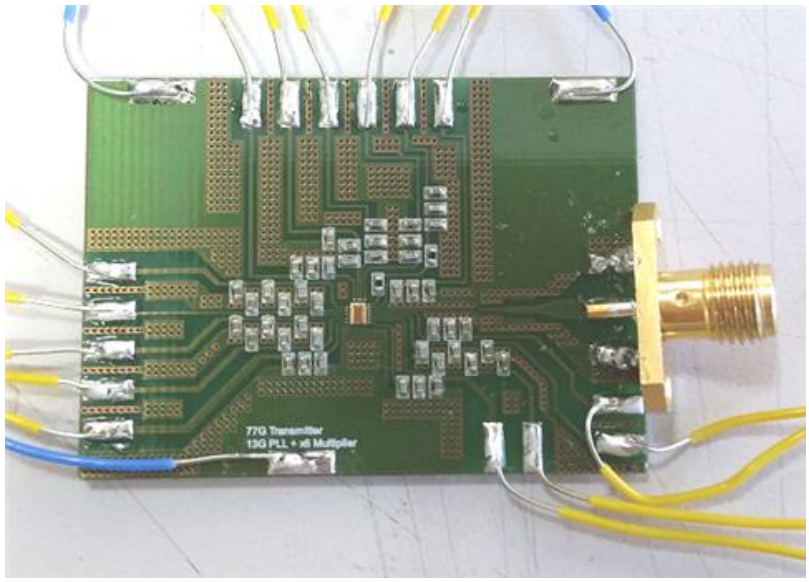


Fig. 29. A PCB to measure fabricated transmitter chip.

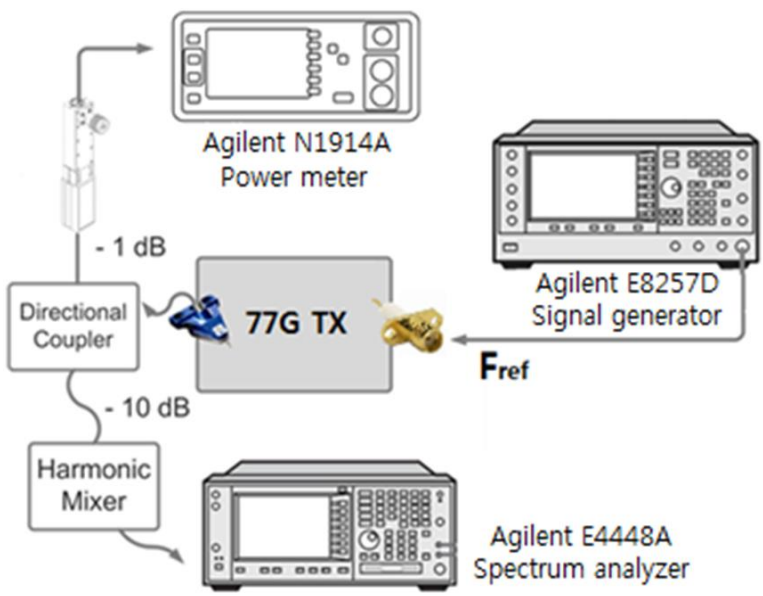


Fig. 30. An experimental environment.

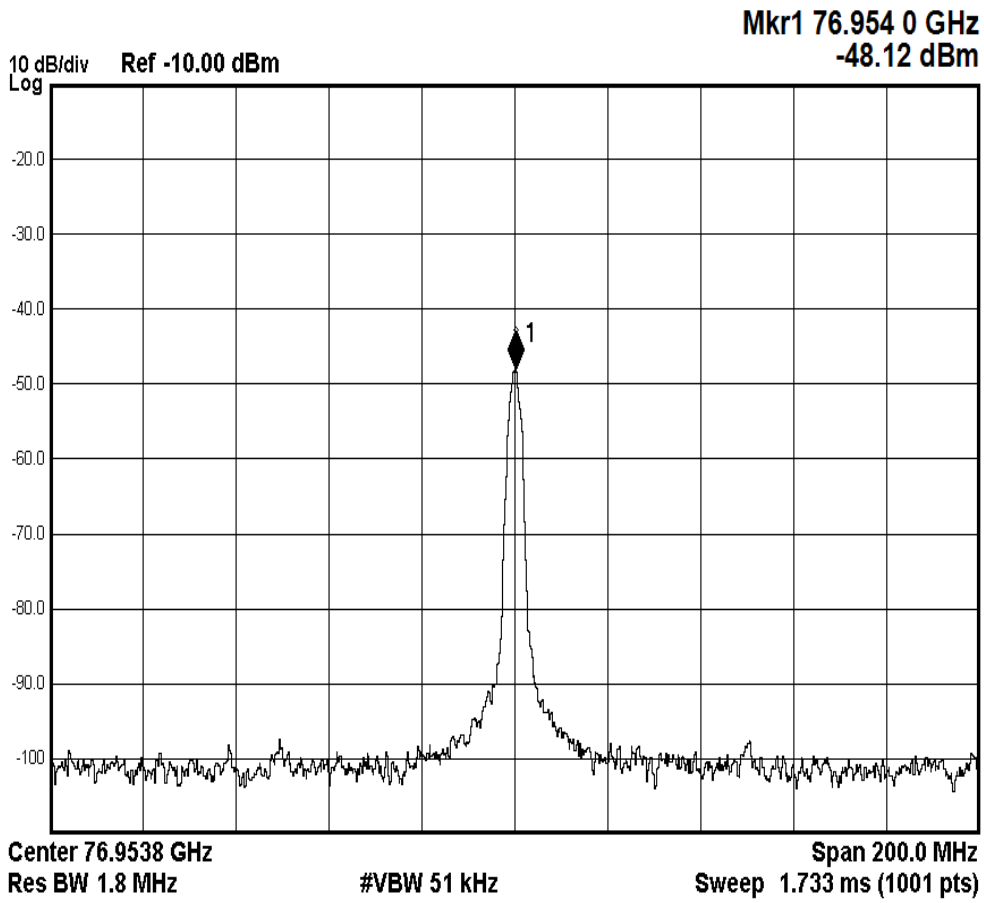


Fig. 31. A measured frequency spectrum.

screen is 200-MHz in total, it is 20-MHz per space in the horizontal direction. Since the output signal must pass through the RF probe, cable, external mixer, and -10 dB coupler until it reaches the spectrum analyzer, the output power shown in the spectrum analyzer is low due to these losses. The actual output power measured by the power detector and compensated for various losses and the output frequency seen by the spectrum analyzer are shown in Fig. 32. The output frequency range measured with the PLL locked to the reference signal is 76.81 ~ 77.95-GHz when the reference signal is 50.0 ~ 50.75-MHz. Output power was measured at 6 to 8.9 dBm in the lock range. Fig. 33 represents the measured phase noise characteristics when the transmitter output carrier frequency is 76.91-GHz. The measured phase noise value is -91.16 dBc / Hz at the 1-MHz frequency offset and -111.78 dBc / Hz at the 10-MHz frequency offset with the markers placed on the spectrum analyzer screen. Fig. 34 shows the output spread spectrum of the transmitter chip when changing the reference signal from 50.00-MHz to 50.75-MHz slowly (10 ms). In the figure, the proposed transmitter chip can cover the output triangular wave bandwidth of 1.1-GHz when the triangular wave reference signal is applied, which is twice as large as the minimum triangular wave bandwidth 600 MHz required for the 77-GHz FMCW radar for vehicles. Because fast sweep time of an external triangular chirp signal is required for the automotive FMCW radar application, the measured FMCW chirp bandwidth is lowered to 601 MHz with a fast

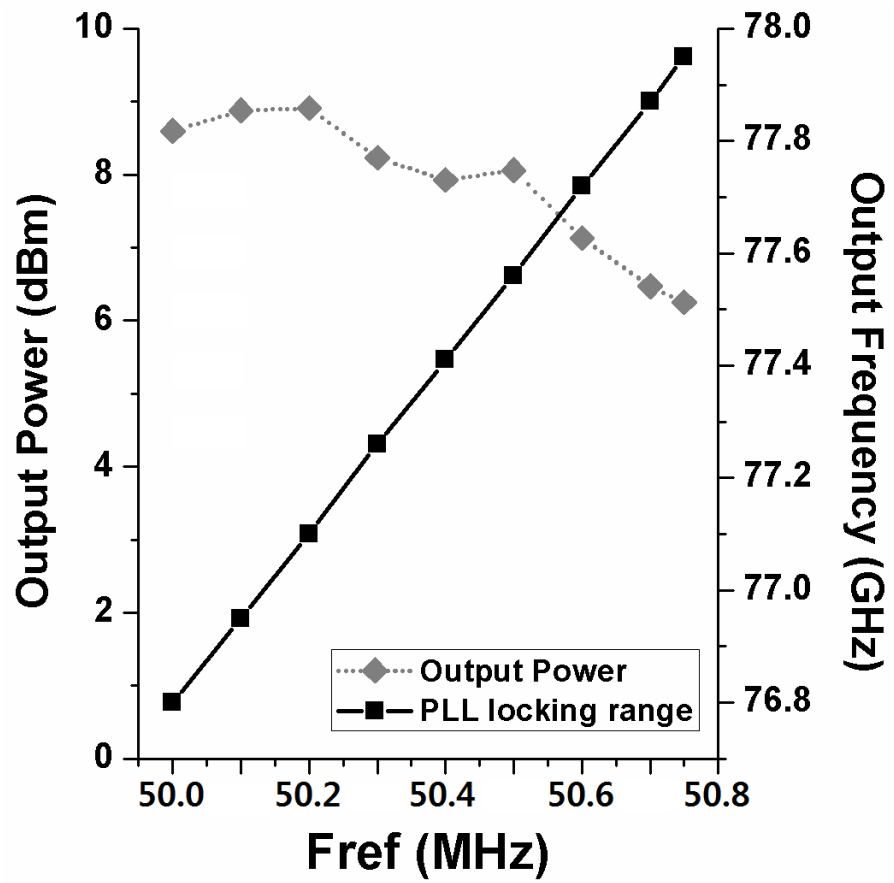
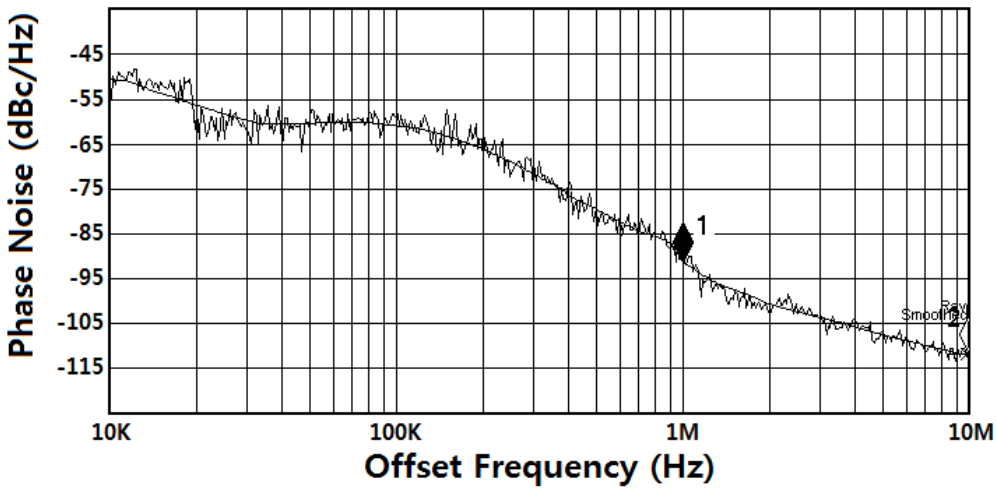
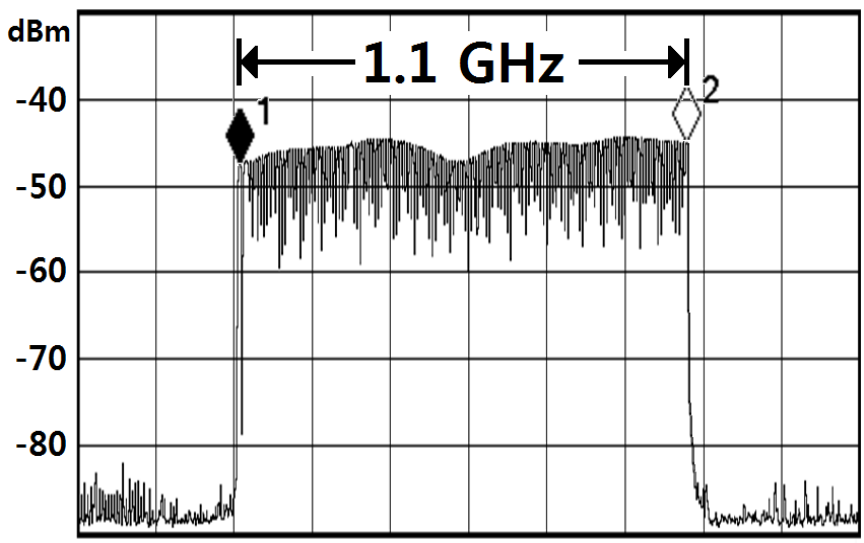


Fig. 32. Measured phase-locked output frequency and power.



MKR	MODE	TRC	X	Y	FUNCTION	FUNCTION WIDTH
1	N	2	1.00 MHz	-91.16 dBc/Hz		
2	N	2	10.0 MHz	-111.78 dBc/Hz		

Fig. 33. Measured phase-noise at 76.81-GHz carrier frequency.



MKR	MODE	TRC	SCL	X	Y
1	N	1	f	76.809 GHz	-47.390 dBm
2	N	1	f	77.950 GHz	-45.057 dBm

Fig. 34. Measured spread spectrum with 10-ms slow chirp reference signal.

1-ms sweep time, as shown in Fig. 35. The measured root-mean-square (rms) frequency error is approximately 490 KHz.). The 1st, 2nd, and 3rd harmonic output spectrum is presented in Fig. 36 (a) and the 4th and 5th harmonic components are shown in Fig. 36 (b).

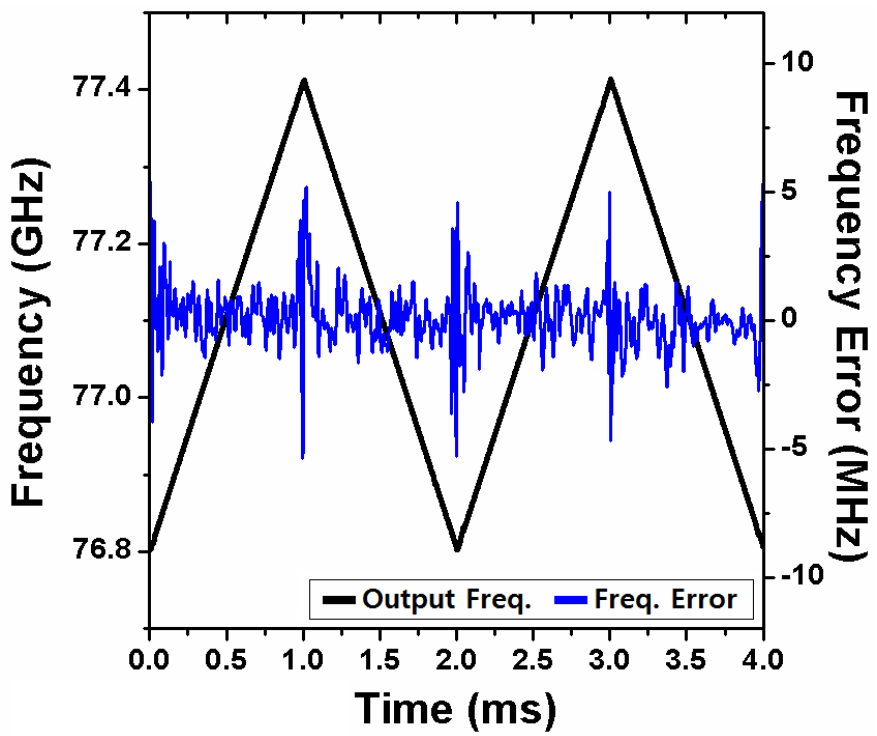
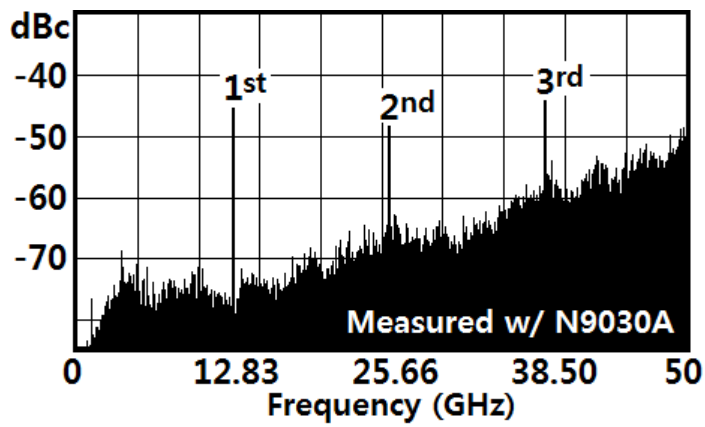
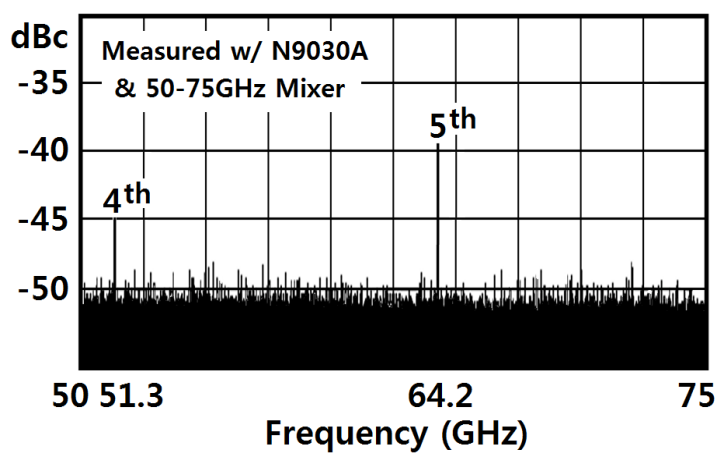


Fig. 35. FMCW profile and frequency error with 1-ms fast chirp reference signal.

Due to the ILOs, the undesired harmonic components are lowered below −39 dBc. Table III shows the performance comparison between the proposed paper and the recently published 77−GHz radar papers. Looking at the Table III in detail, the proposed radar transmitter chip is designed with the integer−N PLL, so it has a disadvantage that it needs a signal source that provides a triangular



(a)



(b)

Fig. 36. Output spectrums of the harmonics in (a) 0–50 GHz, (b) 50–75 GHz.

Table III. Comparison of RADAR Transmitters or Transceivers

	[6]	[7]	[8]	[9]	[10]	This work
Tech.	SiGe Bipolar	SiGe Bipolar	65nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS
Func. / PLL	TRX / Frac. N	TRX / –	TRX / Frac. N	TRX / Int. N	TX / Frac. N	TX / Int. N
Freq. (GHz)	68–93.6	75–79	75.6 –76.3	78.1 –78.8	76–81	76.81 –77.95
RMS Freq. Error (KHz)	N/A	N/A	< 300	N/A	970	490
×N	×1	×18	×1	×1	×2	×6
P_{out} (dBm)	7	6.2	5.1	−2.8	3	8.9
Phase Noise (dBc/Hz)	−88 @10K, −90 @1M	−105.3 * @1M	−85.33 @1M	−85 @1M	−83.43 @1M	−91.2 @1M
TX + PLL Pdiss (mW)	423	1125	243 (TRX)	406	320	116.7
Area (mm^2)	1.9 ×1.6	3 ×1.8	1 ×1.1	3.5 ×2	1.5 ×1.9	1.4 ×0.8

* 4.25−GHz external signal source (Agilent E8257D) is used.

chirp reference signal, but it shows the quite good performances. The proposed chip provides the lowest phase noise among 77-GHz CMOS radar transmitter chips developed so far, suitable frequency range for FMCW radar, and low DC power consumption.

3.4. Summary

In this paper, a 77-GHz FMCW radar transmitter chip was fabricated by constructing a PLL using a 12.8-GHz high-performance VCO and integrating it with a ×6 frequency multiplier and a power amplifier. In the millimeter-wave band, it is well known that it is more advantageous to design the oscillator in the lower frequency band than direct oscillation at the mm-wave band.

Therefore, in this research, a 77-GHz radar transmitter chip was fabricated by designing an oscillator at 12.8 GHz and injecting a 12.8-GHz signal into a PLL and a × 6 multiplier. The 12.8-GHz high-performance VCO is designed to maximize the amplitude of VCO and reduce the inherent noise by applying LiT technology. Although the existing LiT technology has the effect of improving the phase noise characteristic but there is a problem that the structure is complicated and the required area becomes large. In the method using the proposed 3:2 transformer, the above problems are solved simply while maintaining the performance improvement.

Among the RF blocks of the proposed chip, the VCO, IL VCO buffer, ×3 multiplier, and ×2 multiplier, which correspond to the signal generator that produces the 77-GHz signal, are all designed as oscillators. Both of them were designed to follow the initial signal source VCO using frequency locking and phase noise performance using injection-locking techniques. That is, the signal generator including the × 6 multiplier was designed with only four connected

injection locked oscillators without additional buffers or gain stages. In this way, it is possible to improve the phase noise characteristics and to reduce the DC power consumption and area, but the frequency lock range becomes small. However, since the 77-GHz FMCW radar is a narrow-band system with a required frequency band of about 500-MHz, it may not be affected by the disadvantages of the multiple-stage oscillator coupled with the injection lock.

The designed chip is fabricated in 65nm CMOS process and the chip size is 1.38 × 0.79 mm^2 including pad. The RF output was measured through a probe through a wafer, and the DC bias was applied via a bonding wire on the PCB. The measurement equipment used was an Agilent E4448A spectrum analyzer, an Agilent N1914A power detector, and an Agilent E8257D signal generator. The measured chip supports a locked output frequency of 76.81 to 77.95-GHz, which is 1536 times the reference signal when the slow chirp (10 ms) reference signal is 50.0 to 50.75-MHz. The measured FMCW chirp bandwidth with a fast 1-ms sweep time is lowered to 601 MHz. The maximum output power is 8.9 dBm and the DC power consumption is 116.7 mW. Because the phase noise characteristic, which is the most important performance indicator in the radar transmitter, provides the best phase noise characteristic among the papers published at -91.16 dBc/Hz at 1-MHz offset. Therefore, it can be confirmed that the proposed chip is a high-performance 77-GHz vehicle radar transmitter.

Chapter 4. 77-GHz FMCW Radar Transmitter with 2.75-GHz PLL and ×28 Frequency Multiplier

At the beginning of Chapter 2, it was mentioned that there were two approaches to select frequency and architecture. One method of them is to combine a ×6 frequency multiplier and a 12.8−GHz PLL, which is covered in chapter 3. The other method (version 2) is to combine a ×28 frequency multiplier and a 2.75−GHz PLL. The block diagram of the proposed 77−GHz radar TX is shown in Fig. 37. It consists of a 77−GHz signal generator (2.75−GHz VCO, ×7 multiplier, and two ×2 multipliers), a driver amplifier, a power amplifier and PLL blocks. The basic structure is similar to the transmitter discussed in chapter 3, but because the multiplication factor is increased to 28, the VCO could be designed at a lower frequency of 2.75 GHz. Thus, a class−C VCO, which is known to be the best in terms of phase noise, could be applied. In the case of the ×28 frequency multiplier, a ×7 multiplier and two doublers are cascaded. Similarly, the 77−GHz signal generator is configured in the form of an ILO chain.

In chapter 4.1, an improved class−C VCO design and PLL will be explained in detail. The class−C VCO used in the 2.75−GHz PLL was designed to have low−phase−noise characteristics and was designed to have faster and more robust startup than conventional

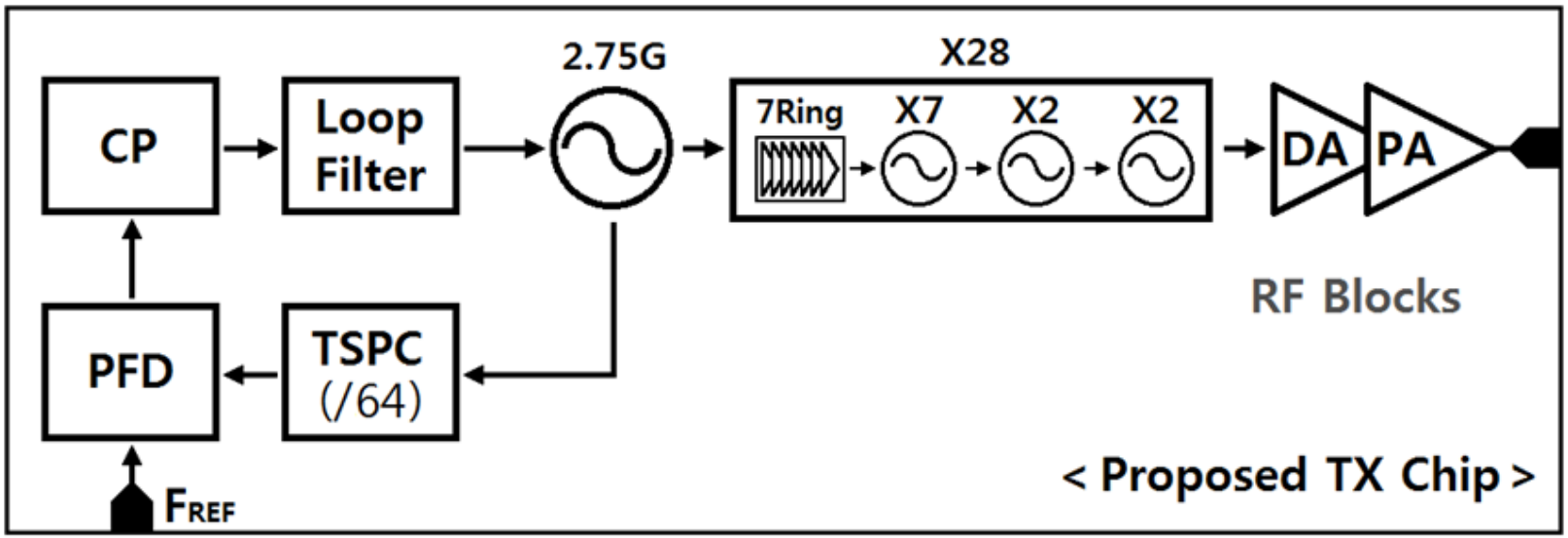


Fig. 37. Block diagram of the proposed 77−GHz TX chip.

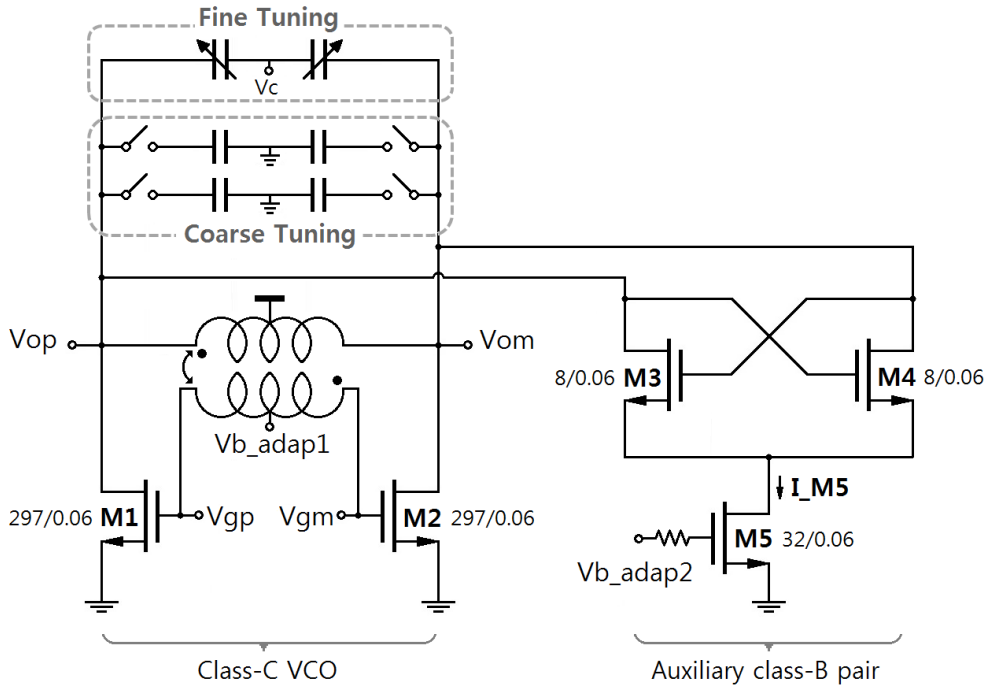
class-C VCOs. The other RF blocks such as a frequency multiplier and a power amplifier will be covered in chapter 4.2. The measurement results are shown in chapter 4.3, and the summary will be followed in chapter 4.4.

4.1. Proposed class-C VCO and PLL

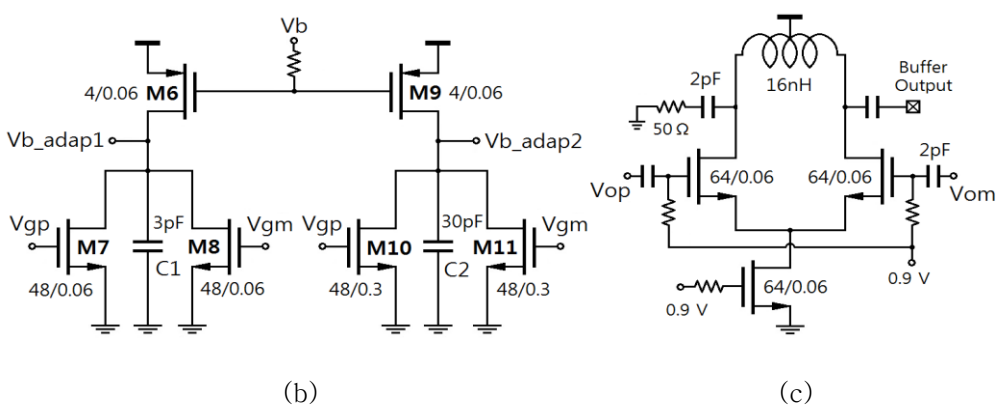
Class-C VCOs have been proposed steadily in recent years. Compared with an LC cross-coupled VCO, the class-C VCO provides better phase noise performance due to its low gate-bias voltage, which can be explained by impulse sensitivity function [14].

Given that a class-C VCO has inevitable startup problems due to its low gate-bias voltage, there have been several attempts to achieve robust startup such as hybrid VCOs [16], [17], a dual-conduction VCO [18], an adaptive bias scheme [19] and an automatic startup loop [15]. However, the hybrid and dual-conduction topologies, which are secure approaches for robust startup, are not sure solutions in that a free-running auxiliary pair distorts the class-C waveform and degrades the steady-state phase noise performance. A class-C VCO with the automatic startup loop shows good performance, but it has reliability issues because of its switching operation. An adaptive bias scheme is generally known as a way to easily get a robust startup, but there is a need for an improved scheme that can guarantee startup more reliably. To improve the startup beyond what an adaptive bias scheme can achieve a self-turn-off auxiliary Class-B pair that maintains low-phase-noise performance and mitigates the startup problem of class-C VCOs is proposed [32].

A schematic of the proposed class-C VCO with a self-turn-off auxiliary class-B pair is shown in Fig. 38(a). The gate bias voltage



(a)



(b) (c)

Fig. 38. Schematic of (a) the proposed class-C VCO with an auxiliary class-B pair, (b) the adaptive bias circuit, and (c) the output buffer.

of the main class-C pair (M1/M2) and that of the auxiliary class-B pair current source (M5) are generated by adaptive bias control circuits [Fig. 38(b)]. A bias network for class-C operation is simply realized by using the center-tapped secondary winding of a transformer, whose primary replaces the tank inductance [14]. The primary inductor has simulated inductance and quality factor (Q) at 2.5 GHz of 2.46 nH and 8.1, respectively, and the secondary

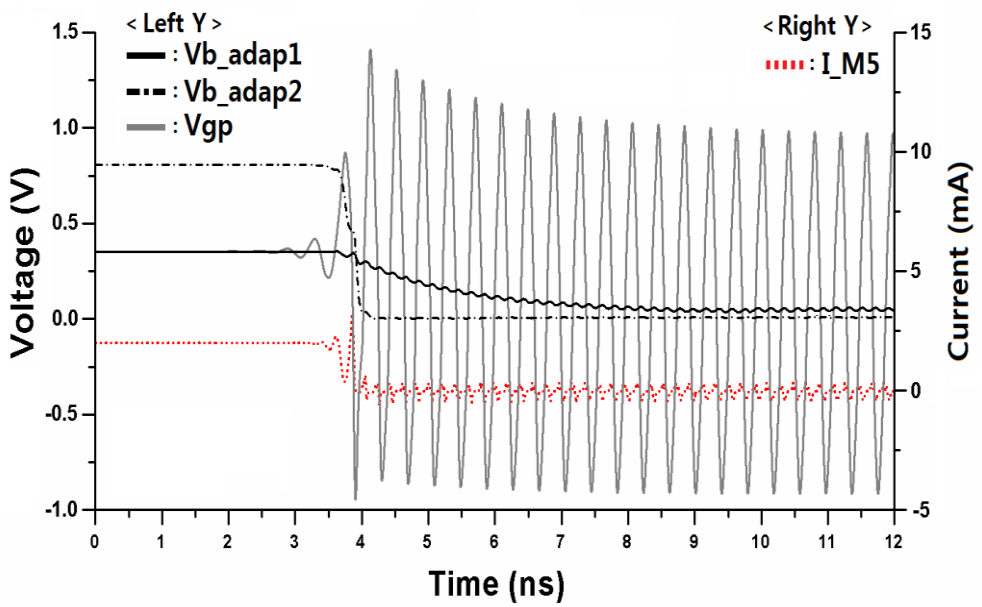


Fig. 39. Adaptive bias voltage waveform of the proposed VCO.

inductor has those of 1.66 nH and 6.4, respectively. The coupling coefficient of the transformer is 0.86 at 2.5 GHz.

In the adaptive bias control circuit, the gates of M7/M8 are, respectively, connected to those of M1/M2 to mirror the M1/ M2 currents. These currents are summed at the Vb_adap1 node and are compared with the M6 current. Then, the capacitor C1 converts the current difference to voltage. This voltage is fed back to the gate of M1/M2 through the center-tap of the transformer [19].

The transient waveforms of the class-C core and the adaptive bias circuit are shown in Fig. 39. The initial voltage and the slope of the Vb_adap1/Vb_adap2 graph are determined by the amount of current flowing in each bias circuit and by the sizes of C1 and C2. The initial voltage of Vb_adap1 is set to 0.32 V when Vb is 0.4 V to guarantee oscillation. With the increase in the voltage amplitude of the oscillator core (Vgp), the currents of the class-C core and the bias circuit are increased. This increased current of the bias circuit is integrated into C1 at the Vb_adap1 node and lowers the voltage of Vb_adap1 to nearly 0 V for class-C operation (the solid black line). The dashed black line in the graph shows the adaptive bias for self-turn-off operation. The gate of the current source (M5) is biased by 0.8 V to turn on M5 in an initial state and almost 0 V to turn it off in a steady-state. The simulated current of the auxiliary pair (the solid red line) in the initial state and the steady-state is 2 mA and nearly 0 mA, respectively. Therefore, the auxiliary class-B pair can provide an additional negative trans-conductance for fast

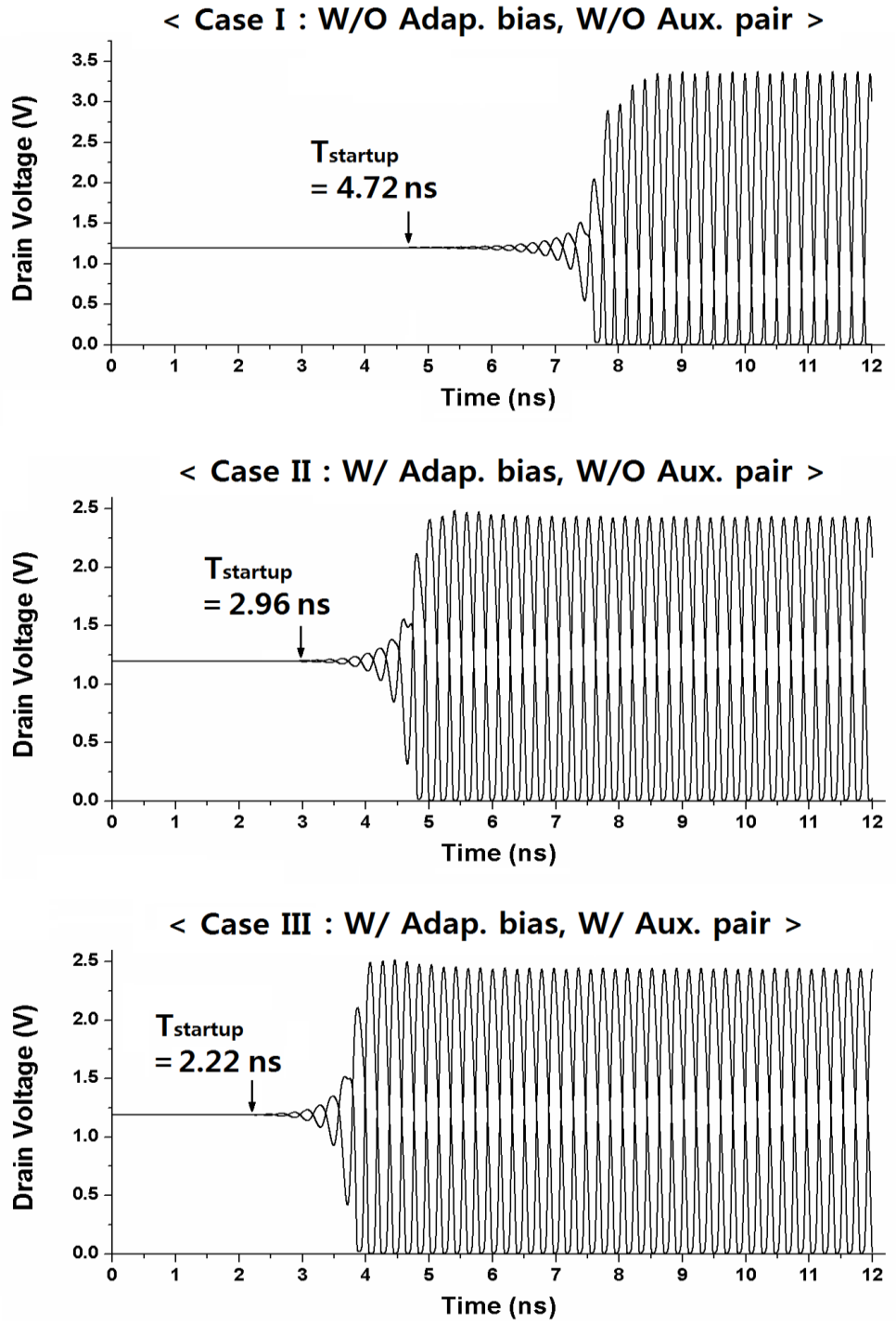


Fig. 40. Comparison of a class-C VCO startup by transient simulation.

startup before entering the steady-state and then it turns itself off (no DC power consumption) in the steady-state.

Transient simulation results that verify the fast startup are shown in Fig. 40. In this work, $T_{startup}$ is defined according to the time when the difference between positive and negative voltage swings reaches 5 mV for the first time. The gate bias voltage of the VCO in case I is 0.32 V which is the same as the initial voltage of Vb_adap1 for a fair comparison. The startup time of the adaptively biased class-C VCO with the auxiliary class-B pair (Case III) is 2.22 ns, which is faster than that of the adaptively biased class-C VCO without the auxiliary pair ($T_{startup}$ = 2.96 ns) as simulated in Case II and much faster than that of the general class-C VCO without a startup technique ($T_{startup}$ = 4.72 ns), as also simulated in Case I.

The simulated phase noise of each case is shown in Fig. 41. Because the gate bias of the class-C VCO core is decreased adaptively (Case II and III), the current waveform of the VCO is sharper than that of Case I which provides a longer conduction time [19]. Therefore, the phase noise of Case II and III is lower than that of Case I as much as approximately 3 dB in simulation. Unlike conventional hybrid or dual-conduction topologies, the phase noise performance in Case III is not degraded compared with Case II because the class-B auxiliary pair which distorts the impulse-like class-C current waveform turns itself off in steady-state automatically. To verify how much the proposed self-turn-off

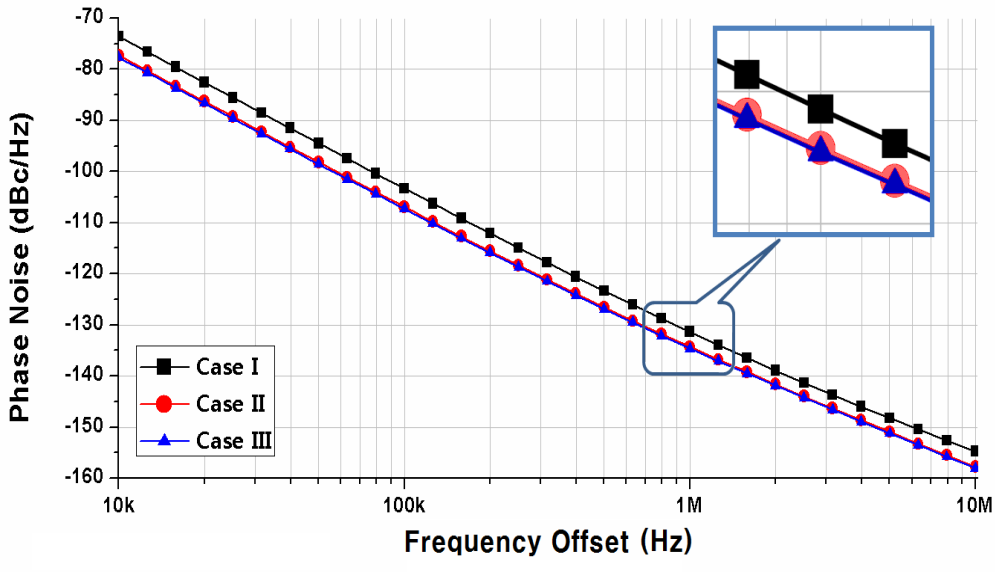


Fig. 41. Comparison of simulated phase noise of each case.

TABLE IV.
Comparison of Startup w/ & w/o the Self-Turn-Off Auxiliary Pair

w/o self-turn-off auxiliary pair		w/ self-turn-off auxiliary pair	
Core gate bias (V)	Tstartup (ns)	Core gate bias (V)	Tstartup (ns)
0.32	4.72	0.32	2.92
0.30	11.50	0.30	4.56
0.28	-	0.28	7.23
⋮	⋮	⋮	⋮
0.12	-	0.12	44.64
0.10	-	0.10	-

auxiliary class-B pair contributes to the robustness of startup, the startup simulation results according to each fixed gate bias of the main VCO core are shown in Table III. The minimum oscillation gate bias voltage with and without the proposed auxiliary pair is 0.12 V and 0.3 V, respectively. Thus, the self-turn-off auxiliary pair can guarantee oscillation when the initial voltage of the adaptive bias circuit is reduced by process variation or a mismatch of transistor models.

Judging from Figs. 40 and 41 and Table IV, the proposed adaptively biased class-C VCO with the self-turn-off auxiliary class-B pair provides fast and robust startup without any performance degradation, such as phase noise increase or additional DC power consumption in the steady-state.

As with the version of the transmitter mentioned in chapter 3, an integer N-type PLL is designed. The designed PLL consists of a TSPC divider, a PFD, a charge pump and a loop filter. The VCO output signal is divided into low-frequency signals of about 41-MHz through the six-stage TSPC divider. The PFD compares phase and frequency of the divided VCO output signal to those of a reference signal (F_{REF}). The loop bandwidth can be adjusted from 100 kHz to 1 MHz by controlling the CP bias current.

4.2. ×28 Multiplier and Power Amplifier

Harmonic amplification is commonly used for millimeter-wave frequency multipliers [26]. However, since amplification stages are required to enhance weak harmonic components, using a higher order harmonic component increases the burden on the system. As a result, unwanted frequency components require a filtering step. Therefore, in the transmitter chip of chapter 3, the frequency multiplier is designed using the ILO chain which does not need amplifier stages and can perform self-filtering. However, this is also not suitable for designing a frequency multiplier with high multiplication factor due to weak high-order harmonic power. If too many multiplier stages are connected in series, the frequency lock range will be reduced, power consumption and system complexity will increase, so a multiplier design with high multiplication factor is required.

Another way to multiply frequencies is to use multi-push technology [27]. Multi-push (N-push) technology eliminates unwanted harmonics by adding the desired harmonic components together in a structured manner, eliminating the need for additional amplifiers and filters. However, N-phase signal is required in the desired frequency and phase correction circuit [28].

Because N-push multipliers require N-phase signals with higher amplitudes at the desired harmonics to obtain sufficient output power, a ring oscillator composed of inverters can be a good

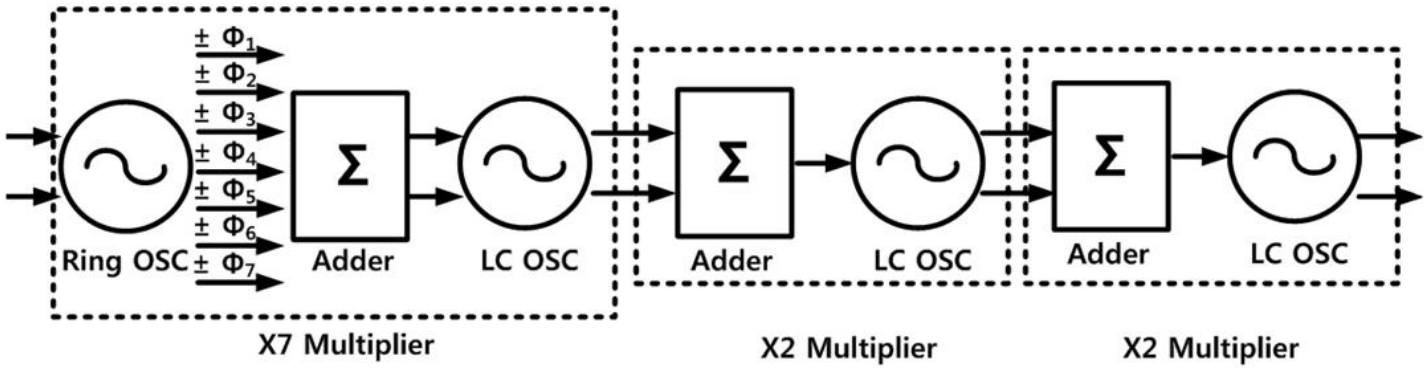
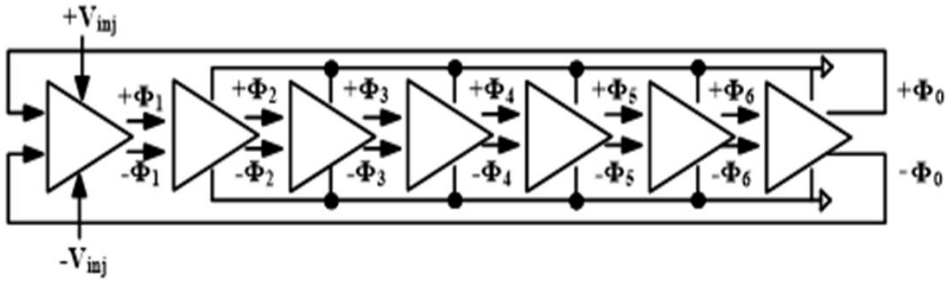


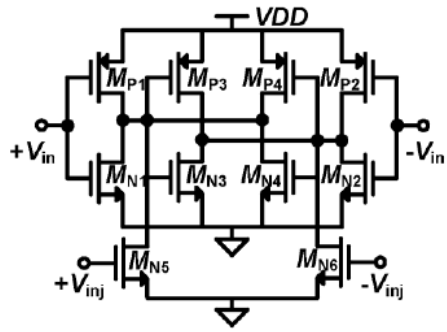
Fig. 42. Block diagram of the designed ×28 frequency multiplier.

candidate for generating phase signals with rich harmonic power. The ideal ring oscillator provides a square wave, so theoretically, all orders of the N-push multiplier can be implemented without degrading the amplitude. However, since the high-frequency harmonic signal is attenuated by the low-pass transfer characteristic, it is difficult to achieve sufficient harmonic power combination for a high order. Therefore in this thesis, a ×28 multiplier is implemented by putting two stages of doubler after 7-push multiplier as shown in Fig. 42. This frequency multiplier was designed by referring to previous work which designed 10 multiplier [29], [30].

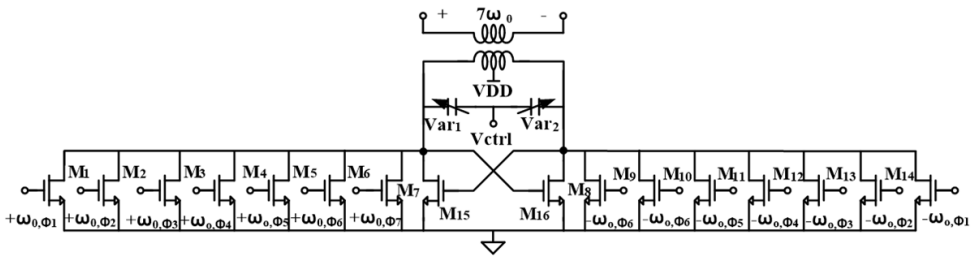
Fig. 43 is a circuit schematic of the designed 7-push frequency multiplier which consists of a 7-stage ring oscillator chain and adder. The 7-push multiplier requires the differential 7-stage ring oscillator with the rich 7-th harmonic component, but the large number of 7 results in more parasitic and bandwidth reduction which causes low harmonic power. The differential injection-locked ring oscillator with 7-stage inverters is used to generate 7-signals with 2pi/7 phase difference. The ring oscillator is locked by the low-phase-noise output signal of the proposed class-C VCO. Each output node of the ring cell is connected to the adder (class-AB CS amplifier). The class-AB transistors (M1-M14) and the cross-coupled transistors (M15, M16) share the output resonant load at $7w_0$. The 7^{th} harmonic is enhanced by the nonlinearity of the class-AB amplifiers and only the 7^{th} harmonic is amplified by the $7w_0$ LC



(a)



(b)



(c)

Fig. 43. (a) Block diagram of the 7-stage ring oscillator, (b) schematic of the ring cell, and (c) schematic of the adder and the oscillator ($7f_0$).

resonant load and cross-coupled pairs. In addition, unwanted harmonics that are not canceled due to phase and amplitude mismatches are filtered by the 7 w_0 LC resonant load.

The two-stage frequency doubler behind the 7-push multiplier is the same circuit mentioned in chapter 3 as shown in Fig. 44. The first stage doubler receives the 19.25-GHz signal, which is a 7-push multiplier output, and generates a second harmonic component,

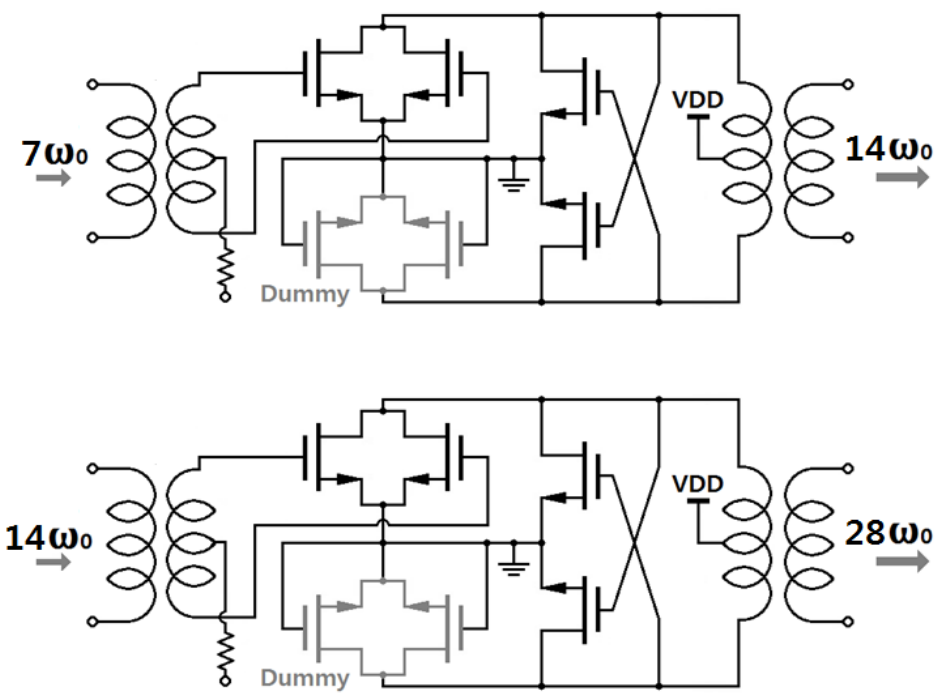


Fig. 44. Schematic of the two stage frequency doubler.

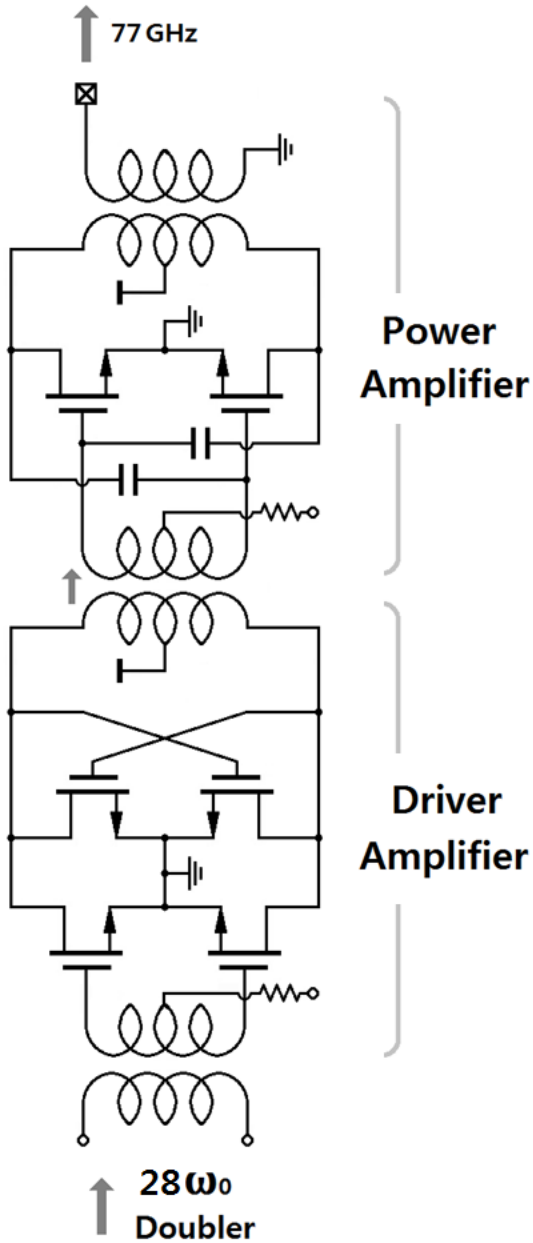


Fig. 45. Schematic of the power amplifier.

38.5 GHz, through the common-node cell. This signal is injected and locked into the first doubler core oscillating near 38.5 GHz. The second stage doubler receivers the 38.5-GHz signal and also generates its second harmonic component, 77 GHz, through the common-node cell. This signal is injected and locked into the second doubler core oscillating near 77 GHz. Thus, the 2.75-GHz signal from the improved class-C VCO based PLL is multiplied by 28 times to a 77-GHz signal.

The power amplifier was designed with the same structure as mentioned in chapter 3 and the transistor size was modified to suit the load conditions as shown in Fig. 45.

4.3. 77-GHz Transmitter Measurement Results

4.3.1 Class-C VCO Measurement Results

The proposed class-C VCO is fabricated via a standard 65-nm CMOS process. Fig. 46 shows a photograph of a chip. The total chip size is 720 × 1440 μm^2, including the test pads. The measured frequency tuning ranges are 2.30–2.36 GHz, 2.38 –2.44 GHz and 2.47–2.54 GHz and the measured output power is approximately 5.5 dBm when the output buffer consumes 16.8 mW at 1.2-V V_{DD} [Fig. 47]. The measured phase noise shows a feasible value of −132.41 dBc/Hz at a 1-MHz frequency offset [Fig. 48]. The DC power

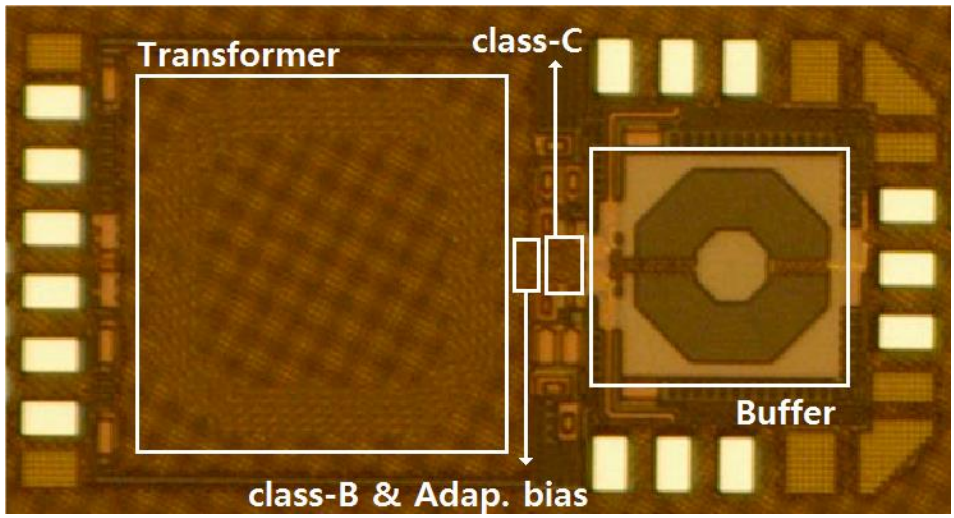


Fig. 46. Chip micro-photograph of the proposed class-C VCO.

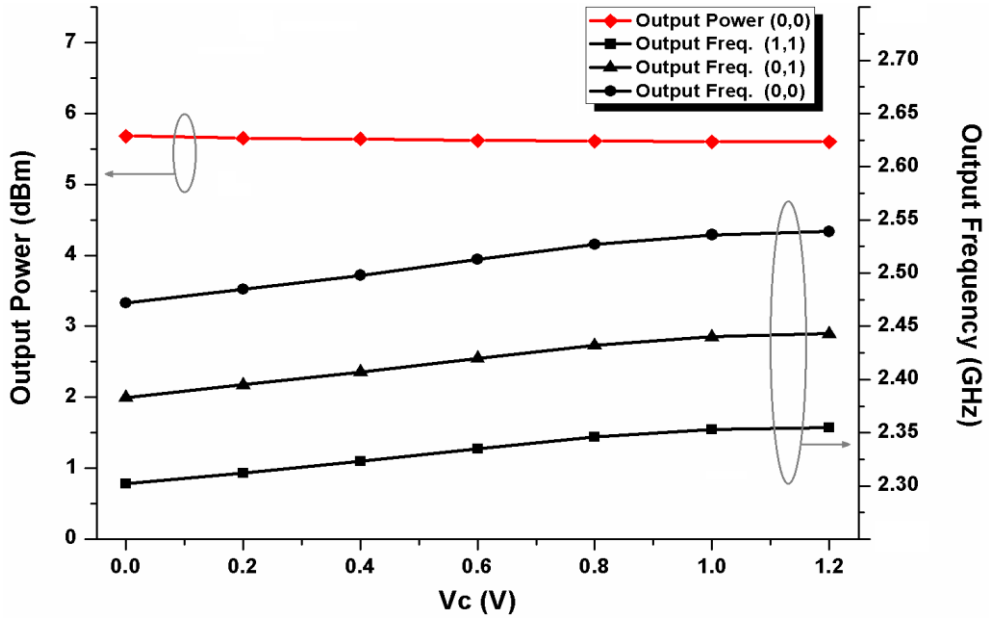


Fig. 47. Measured output frequency and output power.

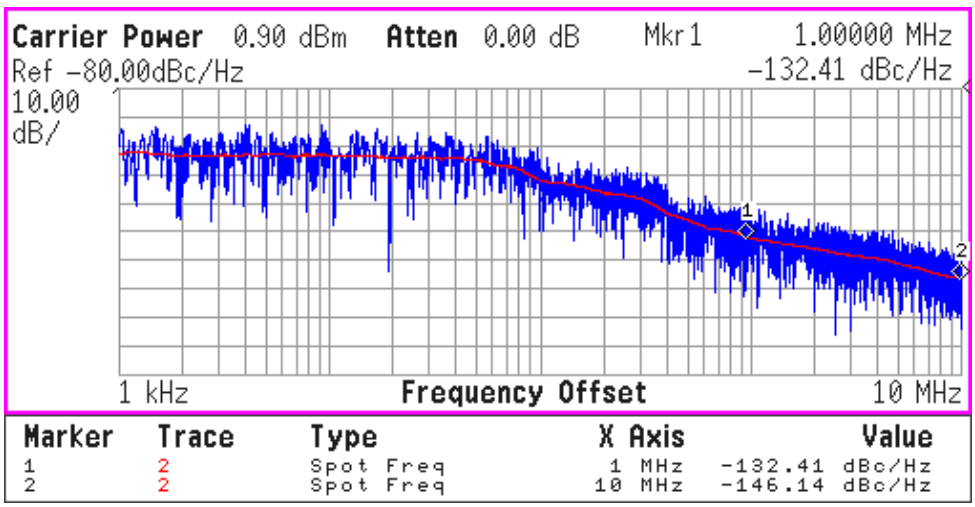


Fig. 48. Measured output frequency and output power.

consumption of the proposed VCO with the adaptive bias circuit is 6 mW at 1.2−V V_{DD}. Table V highlights the details of a performance comparison with recently published class−C VCOs.

Table V. Comparison of published CMOS class−C VCO

Ref.	Topology / Techniques for startup	Freq. (GHz)	PN (dBc/Hz)	Core Power (mW)	FOM	Proc. (nm)
[14]	Class-C / None	4.9	−130 @ 3M	1.3	196	130
[16]	Class-B/C / Aux. pair (free running)	6.7	−137 @ 2M	27	188	55
[17]	Class-AB/B / Aux. pair (free running)	13.15	−101.4 @ 1M	2.4	180	180
[18]	Class-C / Aux. pair (free running)	5.4	−113 @ 1M	0.63	190	180
[19]	Class-C / Adaptive bias	5.1	−116.65 @ 1M	0.86	192.3	90
[15]	Class-C / Automatic startup loop	3.1	−123 @ 1M	1.57	191	180
This work	Class-C / Adaptive bias & Aux. pair (self turn off)	2.46	−132.41 @ 1M	6	192.45	65

$$FOM = -L(\Delta f) - 10\log\{(\Delta f / f_{osc})^2 \cdot P_{dc\_mW}\}$$

4.3.2 77-GHz Transmitter (v2) Measurement Results

The proposed chip was fabricated using a 1−poly 8−metal, 65−nm CMOS process with a top copper metal thickness of 3 μm. Fig. 49 is a microphotograph of the manufactured transmitter chip for a 77−GHz automotive radar. The size of the designed chip is 2.0 × 0.86 mm^2 including the pad. PCB was fabricated for. DC bias was applied through PCB line and RF output was measured by on−wafer probing using an RF probe capable of measuring up to 110−GHz. The 43−MHz triangular reference signal was applied to the chip on the PCB board using the SMA connector. Since the Agilent E4448A spectrum analyzer cannot measure up to 77−GHz by itself, the output frequency spectrum and phase noise performance are measured by connecting the external mixer. The RF output power was measured using an Agilent N1914A power detector and the output power and output frequency spectrum were simultaneously verified using a −10 dB directional coupler at the output stage. The reference chirp signal was applied to the Agilent E8257D signal generator. The output spectrum measured in the above−mentioned experimental environment is shown in Fig. 50. It is the output frequency spectrum screen when the PLL is locked and the reference signal is 42.55 MHz and the carrier frequency is 76.24 GHz which is 1792 times the reference signal. Since the output signal must pass through the RF probe, cable, external mixer, and −10 dB coupler until it reaches the spectrum analyzer, the output

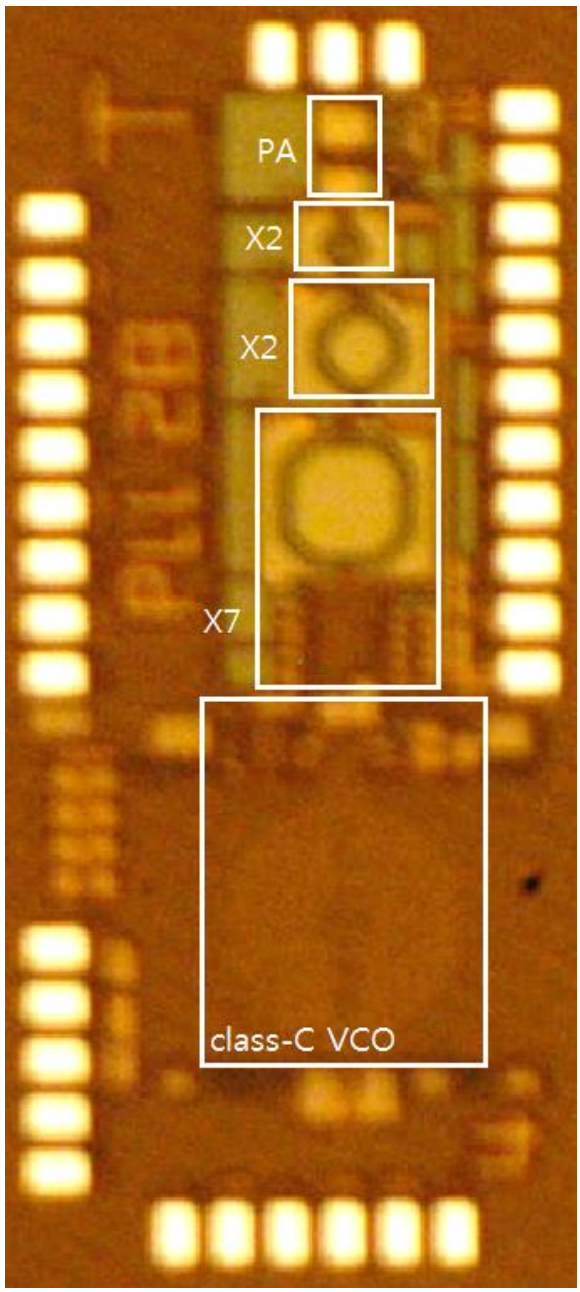


Fig. 49. A microphotograph of the transmitter chip.

power shown in the spectrum analyzer is low due to these losses. The output frequency seen by the spectrum analyzer is shown in Fig. 51. The output frequency range measured with the PLL locked to the reference signal is 76.24 ~ 78.13-GHz when the reference signal is 42.55 ~ 43.60-MHz. However, output power was measured at about -18 dBm in the lock range. This is because the second frequency doubler is not oscillated owing to the process

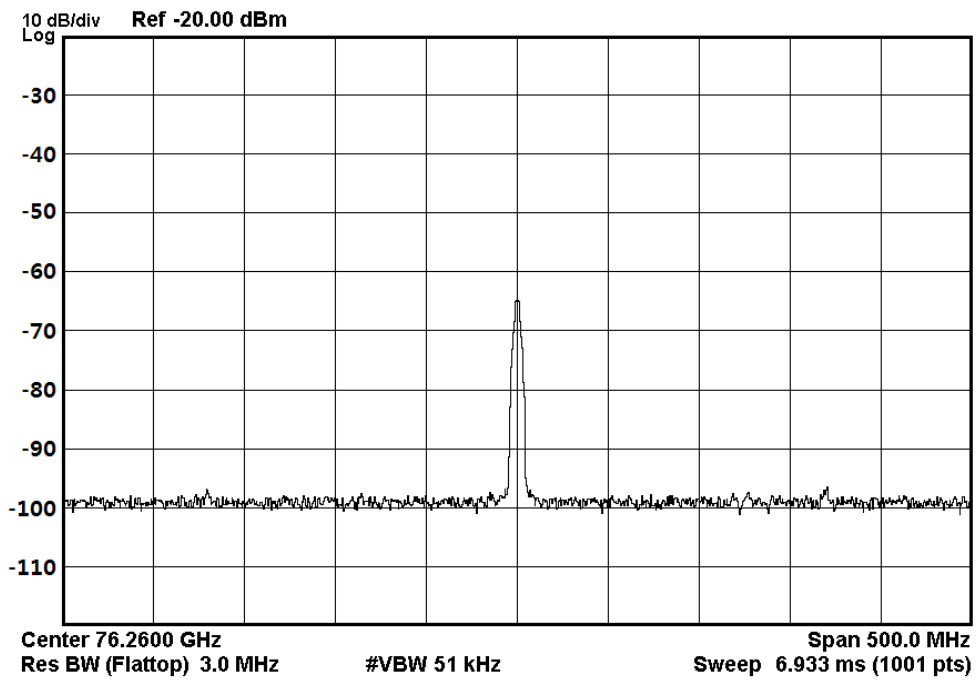


Fig. 50. Output frequency spectrum.

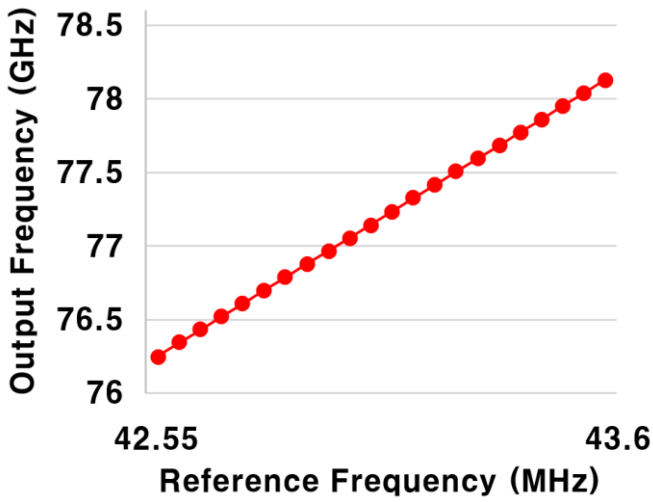


Fig. 51. Measured phase-locked output frequency.

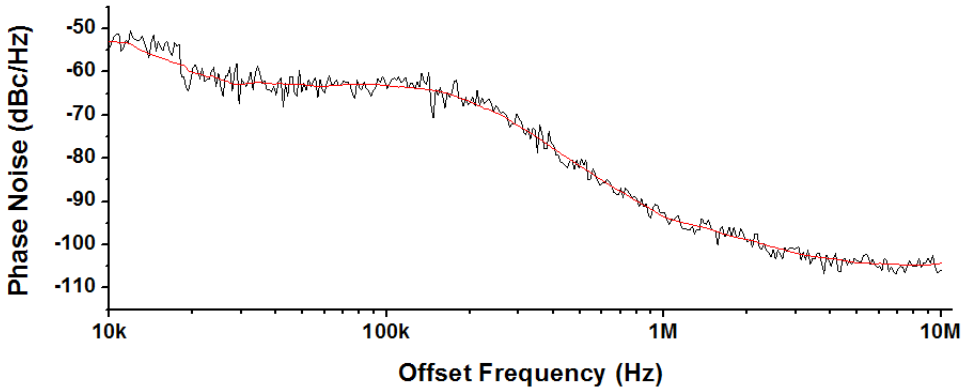


Fig. 52. Measured phase noise.

variation, and thus the PA does not supply enough input power. Fig. 52 represents the measured phase noise characteristics. The measured phase noise value is −93.64 dBc/Hz at the 1−MHz frequency offset and −104.37 dBc / Hz at the 10−MHz frequency offset with the markers placed on the spectrum analyzer screen. Fig. 53 shows phase noise performance according to the output frequency. It can be confirmed that it provides a low phase noise characteristic in the entire frequency band.

Table VI shows the performance comparison between the

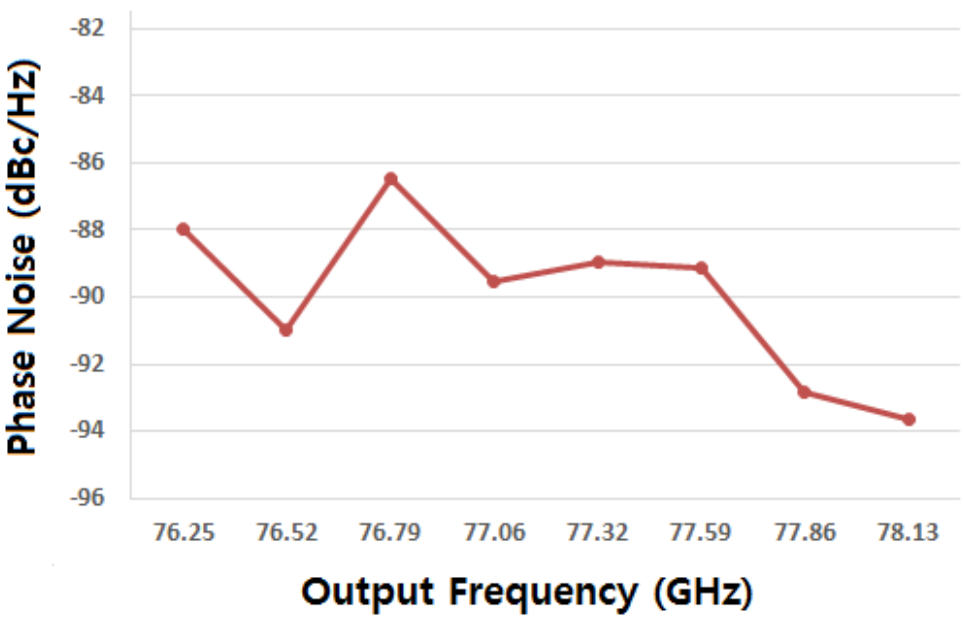


Fig. 53. Phase noise vs. output frequency.

proposed paper and the recently published 77-GHz radar papers. Looking at the table in detail, the proposed radar transmitter chip with 2.75-GHz PLL and ×28 multiplier is designed with the integer-N PLL, so it has a disadvantage that it needs a signal source that provides a triangular chirp reference signal, but it shows the quite good performances. The measured phase noise is -93.64 dBc/Hz at 1-MHz offset. The proposed chip provides the lowest phase noise at 1-MHz offset frequency among 77-GHz CMOS radar transmitter chips including the proposed ×6 multiplier-based transmitter chip, suitable frequency range for FMCW radar, and low DC power consumption.

Table VI. Comparison of RADAR Transmitters or Transceivers

	[6]	[7]	[8]	[9]	[10]	TX CH.3	This work
Tech.	SiGe Bipolar	SiGe Bipolar	65nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS
Func. / PLL	TRX / Frac. N	TRX / –	TRX / Frac. N	TRX / Int. N	TX / Frac. N	TX / Int. N	TX / Int. N
Freq. (GHz)	68–93.6	75–79	75.6 –76.3	78.1 –78.8	76–81	76.81 –77.95	76.26 –78.23
RMS Freq. Error (KHz)	N/A	N/A	< 300	N/A	970	490	–
×N	×1	×18	×1	×1	×2	×6	×28
P_{out} (dBm)	7	6.2	5.1	−2.8	3	8.9	−18
Phase Noise (dBc/Hz)	−88 @10K, −90 @1M	−105.3 * @1M	−85.33 @1M	−85 @1M	−83.43 @1M	−91.2 @1M	−93.64 @1M
TX+PLL Pdiss (mW)	423	1125	243 (TRX)	406	320	116.7	195 (w/o PA)
Area (mm^2)	1.9 ×1.6	3.0 ×1.8	1.0 ×1.1	3.5 ×2.0	1.5 ×1.9	1.4 ×0.8	2.0 ×0.86

* 4.25−GHz external signal source (Agilent E8257D) is used.

4.4. Summary

In the millimeter-wave band, it is well known that it is more advantageous to design the oscillator in the lower frequency band than direct oscillation at the mm-wave band. Therefore, in this research, a low-phase-noise 77-GHz transmitter chip was fabricated by designing a low-phase-noise oscillator at 2.75 GHz and injecting a 2.75-GHz signal into a PLL and a × 28 multiplier.

The 2.75-GHz high-performance VCO is designed to generate impulse-like current waveform by applying class-C operation. Although the existing class-C VCO has the greatest effect of improving the phase noise characteristic but there is an inevitable startup problem due to its low gate-bias voltage. There have been several attempts to achieve robust startup, but there is a need for an improved scheme that can guarantee startup more reliably. To improve the startup beyond what an adaptive bias scheme can achieve a self-turn-off auxiliary Class-B pair that maintains low-phase-noise performance and mitigates the startup problem of class-C VCOs is proposed in this paper.

Among the RF blocks of the proposed chip, the class-C VCO, 7-push multiplier, and two ×2 multipliers, which correspond to the signal generator that produces the 77-GHz signal, are all designed as oscillators. Both of them were designed to follow the initial signal source VCO using frequency locking and phase noise performance using injection-locking techniques. In this way, it is possible to

improve the phase noise characteristics and to reduce the DC power consumption and area, but the frequency lock range becomes small. However, since the 77-GHz FMCW radar is a narrow-band system with a required frequency band of about 500-MHz, it may not be affected by the disadvantages of the multiple-stage oscillator coupled with the injection lock.

The designed chip is fabricated in 65nm CMOS process and the chip size is 2.0 × 0.86 mm^2 including pad. The RF output was measured through a probe through a wafer, and the DC bias was applied via a bonding wire on the PCB. The measurement equipment used was an Agilent E4448A spectrum analyzer, an Agilent N1914A power detector, and an Agilent E8257D signal generator. The measured chip supports a locked output frequency of 76.26 to 78.23-GHz, which is 1792 times the reference signal when the reference signal is 42.55 to 43.60-MHz. The output power is about -18 dBm because the second doubler (77 GHz) seems not to oscillate and the input of the power amplifier is not sufficient. The DC power consumption is 116.7 mW. Since the phase noise characteristic, which is the most important performance indicator in the radar transmitter, provides the best phase noise characteristic among the papers published at -93.64 dBc/Hz at 1-MHz offset. This value is about 2.5 dB lower than the value of the transmitter chip (v1) mentioned in chapter 3. Therefore, it can be confirmed that the proposed chip is a high-performance 77-GHz vehicle radar transmitter.

Chapter 5. Conclusion

This thesis presents design methodology and experimental verification of a low-phase-noise 77-GHz CMOS FMCW (Frequency Modulated Continuous Wave) radar transmitter. When using a frequency multiplier, it is relatively advantageous to design a low-phase-noise signal source because a VCO can be designed at lower frequency band where gain of active devices is high. Therefore, in this thesis, two methods for realizing 77-GHz CMOS low-phase-noise signal source have been proposed.

One method is to combine a ×6 frequency multiplier and a 12.8-GHz PLL for FMCW signal generation. The VCO used in the PLL was designed with a newly proposed improved LiT VCO using a 3:2 transformer. The fabricated transmitter chip supports FMCW output signals in the 76.81-77.95 GHz band when supplied with the external reference triangular signal from 50.00 to 50.75 MHz. The RF output power is about 8.9 dBm and consumes 116.7 mW of DC power. The measured phase noise is -91.16 dBc/Hz at the 1-MHz offset of the 76.81-GHz carrier frequency, which is the lowest phase noise characteristic of the previously announced 77-GHz CMOS transmitter and transceiver.

The other is a method of combining a ×28 frequency multiplier and a 2.75-GHz PLL for FMCW signal generation. The improved

class-C VCO is proposed, which improves the startup problem to have low-phase-noise characteristics. The fabricated transmitter chip supports FMCW output signals in the 76.26-78.23 GHz band when supplied with the external reference triangular signal from 42.55 ~ 43.65 MHz. The RF output power is about -18 dBm and consumes 195.4 mW of DC power. The measured phase noise is -93.64 dBc/Hz at the 1-MHz offset of the 78.13-GHz carrier frequency, which is even lower phase noise characteristic than the ×6 frequency multiplier based transmitter chip.

So far two versions of the 77-GHz transmitter chip are designed with a frequency multiplier based structure, a low-phase noise VCO at low frequencies, and an ILO chain of signal generators. If the radar transmitters are designed in this way, it is expected that low-phase-noise 77-GHz signals can be generated. First, an excellent phase noise performance of -91.16 dBc/Hz at 1-MHz offset, which is the best performance among published papers, was achieved by a transmitter version with a ×6 multiplier and an improved 12.8-GHz LiT VCO. Next, phase noise performance of -93.64 dBc/Hz at 1-MHz offset, approximately 2.5 dB lower than the first version, was achieved by a transmitter version with a × 28 multiplier and an improved Class-V VCO.

In conclusion, the structure and the techniques that are expected to have low phase noise have been proposed, and it has been verified in this thesis that the best available phase noise performance is provided.

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Abstract

본 논문에서는 65nm CMOS 공정을 이용한 저 위상 잡음을 갖는 77-GHz 장거리 차량용 주파수 변조 연속파 (FMCW: Frequency Modulated Continuous Wave) 레이더용 송신기가 두 가지 버전으로 제안되었다. 일반적으로 밀리미터파 대역에서는 능동 소자의 이득이 매우 낮기 때문에 낮은 위상 잡음을 갖는 전압 제어 발진기 (VCO: Voltage Controlled Oscillator)를 제작하는 것은 어려움이 따른다. 주파수 체배기를 이용하는 경우, 체배 차수 (N) 분의 1 주파수에서 VCO와 위상 잠금 루프 (PLL: Phase Locked Loop)를 설계할 수 있기 때문에 낮은 위상 잡음을 갖도록 설계하기에 상대적으로 유리하다.

본 논문에서는 크게 두 가지 방법으로 송신기를 설계하였다. 하나는 77-GHz 대역에서 저 위상 잡음 송신기를 구현하기 위하여 상대적으로 낮은 주파수인 12.8-GHz 에서 동작하는 고성능 신호원을 설계하고, 이를 6 체배 하여 목표로 하는 77-GHz 대역의 송신기이고, 다른 하나는 더욱 낮은 주파수인 2.75-GHz 에서 동작하는 고성능 신호원을 설계하고, 이를 28 체배 하여 목표로 하는 77-GHz 대역의 송신기이다.

첫 번째 송신기의 경우, 77-GHz 신호발생기를 구성하는 VCO, VCO 버퍼, ×3 체배기, ×2 체배기는 각각 발진하며 앞 단의 출력 신호로 주입 잠금된 4 단의 연결된 주입 잠금 발진기로 설계되었다. 12.8-GHz PLL에 사용된 VCO는 저 위상 잡음 특성을 갖기 위해 선형화된 트랜스컨덕턴스 (LiT: Linearized Transconductance) 기술을 이용하였고, 3:2 변압기를 이용하여 기존의 LiT VCO 보다 단순한 구조로 설계되었다. 주파수 ×6 체배기는 일반적으로 주로 쓰이는 3차 조화 성분 주입-잠금 방식의 주파수 ×3 체배기와 push-push 방식의 ×2 체배기의 결합으로 구성되어있다. 6 체배된 77-GHz 신호는 드라이버 증폭기와 전력 증폭기를 거쳐 높은 RF 전력을 가지게 되어 중거리 혹은 장거리 차량용 레이더의 송신 신호로 사용 가능하게 된다. PLL은 정수 N 방식이 사용되

었으므로 77-GHz에서 FMCW 신호를 만들어 내려면 삼각파 형태의 레퍼런스 신호가 PLL의 위상 주파수감지기 (PFD: Phase Frequency Detector)에 주입되어야 한다. 제작된 송신기 칩은 50.00 ~ 50.75 MHz 의 레퍼런스 삼각파 신호가 공급될 때 76.81 ~ 77.95 GHz 대역의 FMCW 출력 신호를 지원한다. RF 출력 전력은 약 8.9 dBm 이고 116.7 mW의 DC 전력을 소모한다. 제작된 송신기의 위상 잡음은 76.81-GHz 캐리어 주파수의 1-MHz 오프셋에서 -91.16 dBc/Hz 이며, 이는 기 발표된 77-GHz CMOS 송, 수신기 논문들 중 가장 낮은 위상 잡음 특성이다.

두 번째 송신기의 경우, 주입 잠금으로 연결된 VCO, 7-푸쉬 체배기, 두 단의 ×2 체배기를 이용하여 77-GHz 신호를 발생시킨다. 2.75-GHz PLL에 사용된 VCO는 기존의 class-C VCO의 스타트업 문제를 성능 저하 없이 안정적으로 해결한 개선된 class-C VCO이다. 낮은 위상 잡음을 갖는 2.75-GHz 신호를 28체배하여 77-GHz 신호를 만들게 된다. PLL은 마찬가지로 정수 N 방식이 사용되었기 때문에 삼각파 레퍼런스 신호가 요구된다. 제작된 송신기 칩은 43.55 ~ 43.60 MHz 의 레퍼런스 삼각파 신호가 공급될 때 76.26 ~ 78.23-GHz 대역의 FMCW 출력 신호를 지원하고, 이는 레퍼런스 신호의 1792 배에 해당된다. RF 출력 전력은 두 번째 ×2 체배기의 발진 실패로 인해 전력 증폭기의 입력으로 충분한 전력이 전달되지 못하여 -18 dBm의 낮은 출력 전력이 측정되었고 195 mW의 DC 전력을 소모한다. 제작된 송신기의 위상 잡음은 1-MHz 오프셋에서 -93.64 dBc/Hz이며, 이는 기 발표된 논문들 뿐만 아니라 첫 번째 버전 송신기보다도 2.5 dB 가량 우수한 성능을 제공한다.

결론적으로, 본 논문에서는 좋은 위상 잡음 성능을 가질 것으로 예측되는, 주파수 체배기 기반 구조 및 낮은 대역 고성능 VCO 설계 기술들이 제안되었고, 우수한 위상 잡음 성능을 실험적으로 검증하였다.