Ph.D. Dissertation

A Study on Energy-Efficient Inductor Current Controls for Maximum Energy Delivery in Battery-free Buck Converter

무전원 벅 컨버터의 최대 에너지 전달을 위한 효율적인 인덕터 전류 제어에 관한 연구

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A Study on Energy-Efficient Inductor Current Controls for Maximum Energy Delivery in Battery-free Buck Converter

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Abstract

A discontinuous conduction mode (DCM) buck converter, which acts as a voltage regulator in battery-free applications, is proposed to maximize the energy delivery to the load system. In this work, we focus the energy loss problem during start-up and steady-state operation of the buck converter, which severely limits the energy delivery. Especially, the energy loss problem arises from the fact that there is no constant power source such as a battery and the only a small amount of energy harvested from the ambient energy sources is available. To address such energy loss problem, this dissertation proposes optimal inductor current control techniques at each operation to greatly reduce the energy losses. First, a switching-based stepwise capacitor charging scheme is presented that can charge the output capacitor with constant inductor current during start-up operation. By switching the inductor with gradually incrementing duty-cycle ratios in a stepwise fashion, the buck converter can make the inductor current a constant current source, which can greatly reduce the start-up energy loss compared to that in the conventional capacitor charging scheme with a voltage source. Second, a variable on-time (VOT) pulse-frequency-modulation (PFM) scheme is presented that can keep the peak inductor current constant during steady-state operation. By adaptively varying the on-time according to the operating voltage conditions of the buck converter, it can suppress the voltage ripple and improve the power efficiency even with a small output capacitor. Third, an adaptive off-time positioning zero-crossing detector (AOP-ZCD) is presented that can adaptively position the turn-off timing of the low-side switch close to the zero-

inductor-current timing by predicting the inductor current waveform without using a power-hungry continuous-time ZCD. To demonstrate the proposed design concepts, the prototype battery-free wireless remote switch including the piezoelectric energy harvester and the proposed buck converter was fabricated in a 250 nm high-voltage CMOS technology. It can harvest a total energy of 246 μJ from a single button press action of a 300-mm^2 lead magnesium niobate-lead titanate (PMN-PT) piezoelectric disc, and deliver more than 200 μJ to the load, which is sufficient to transmit a 4-byte-long message via 2.4-GHz wireless USB channel over a 10-m distance. If such battery-free application does not use the proposed buck converter, the energy losses incurred at the buck converter would be larger than the energy harvested, and therefore it cannot operate with a single button-pressing action. Furthermore, thanks to the proposed energy efficient buck converter, the battery-free wireless remote switch can be realized by using a cheaper PZT piezoelectric source, which can achieve a 10× cost reduction.

Keywords : Buck converter, battery-free application, switching-based stepwise capacitor charging, variable on-time, adaptive off-time positioning zero-crossing detector, piezoelectric, RF transmitter, battery-free wireless remote switch.

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Chapter 1

Introduction

1.1 Motivation

With active researches in energy harvesting system [1]–[4], there is a growing demand for battery-free applications [4], [26]–[28] such as wireless switches and sensors. While these applications utilize the energy existing in environment, for example kinetic motion [35], pressure [26]–[30], light [36] and differences in temperature [38], combining energy harvesters and ultra-low power wireless applications creates the battery-free solutions. Such battery-free applications can save maintenance and installation costs for use in buildings, smart home and industrial applications as well as for the Internet of Things (IoTs). However, the energy harvested from such ambient energy sources is limited and the large energy losses incurred during the system's operation make it difficult to supply enough energy to meet the

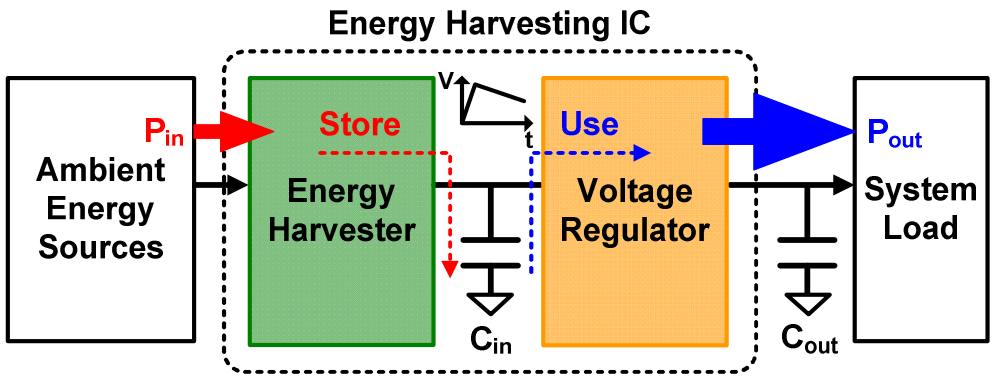

Fig. 1.1. Simple schematic of the battery-free application.

requirements for successful data transmission. This dissertation proposes an energy-efficient voltage regulator circuit and its optimal inductor current control techniques to deliver the largest possible energy while a small amount of energy harvested is available.

A simple schematic of the battery-free system is illustrated in Fig. 1.1. It consists of an ambient energy source, energy harvester, storage capacitor (C_{in}), voltage regulator and load system. When the ambient energy sources such as a solar cell, piezoelectric transducer and thermoelectric generator (TEG) generate the electric charge, the energy harvester collect this charge in C_{in}, instead of the battery. Since the generated power from the ambient energy sources (i.e, P_{in}) is smaller than the required power of the load system (i.e., P_{out}) in most cases, the energy should be collected in C_{in} during the sufficient time before operating the voltage regulator. After the enough energy is charged in C_{in}, the voltage regulator begins charging its output capacitor (C_{out}) to a desired output voltage using the energy stored in C_{in} (i.e., start-up operation), and then delivers this energy to the load (i.e., RF transmitter) at a

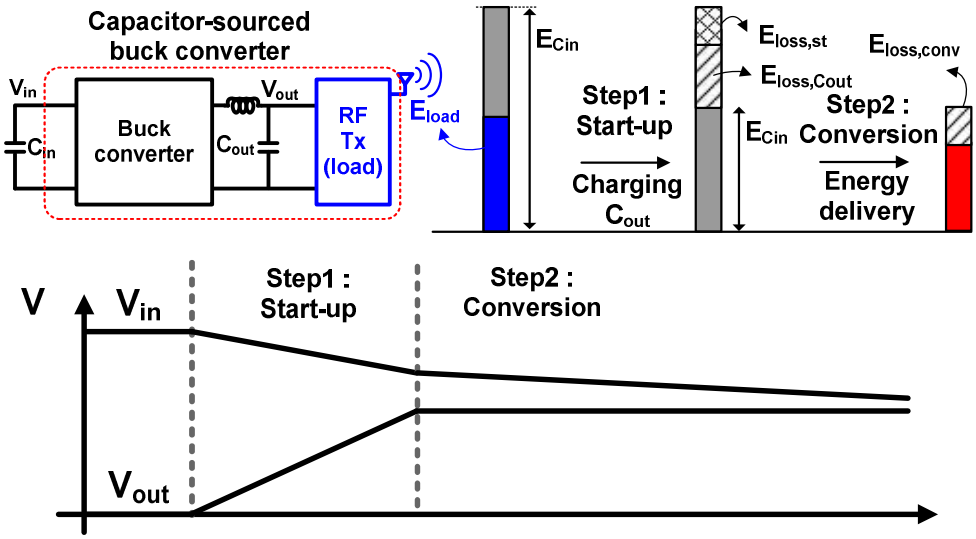

Fig. 1.2. Specific operation of the voltage regulator and its design issues in battery-free applications.

steady output voltage. In this study, we focus on the voltage regulator because its energy loss is dominant, thereby significantly limiting the energy delivery.

The challenges in designing such a voltage regulator arise from the energy losses incurred during the start-up operation with fully discharged output capacitor (C_{out}) and during the steady-state operation with the large quiescent current in control circuits. Fig. 1.2 illustrates the specific operation of the voltage regulator and its design issues in battery-free applications. Note that the small input capacitor (C_{in}) is required to collect the large energy with a high voltage in energy harvesting process [35], [40], which calls for the step-down buck converter topology as a voltage regulator to down-convert the voltage. First, the large energy is dissipated at start-up operation of the buck converter. Specifically, to charge C_{out} from zero to the desired

output

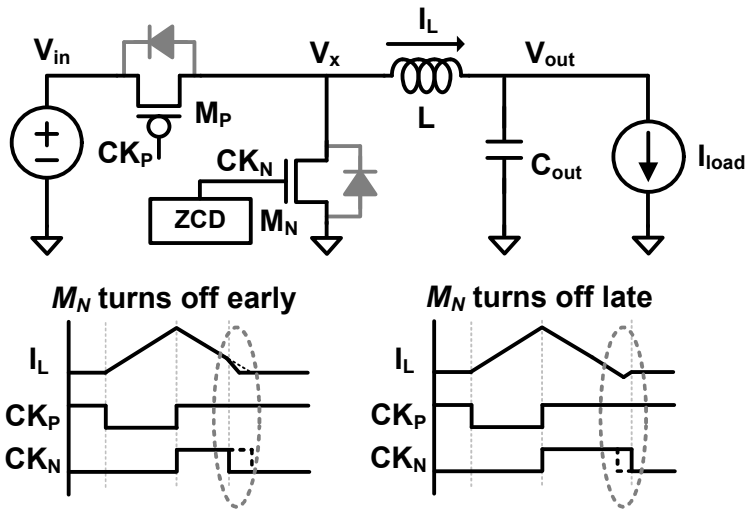

Fig. 1.3. Schematic of synchronous DCM buck converter and its key waveforms when M_N turns off early or late.

voltage (V_{out}), the capacitor charging loss is incurred, which contains two losses; one is the energy dissipation at the resistive component ($E_{loss,st}$) such as a switch, and the other is the stored energy in C_{out} (i.e. $E_{loss,Cout} = 0.5C_{out}V_{out}^2$). Second, the large energy loss ($E_{loss,conv}$) is also dissipated during steady-state operation. Specifically, to regulate V_{out} at a steady voltage, the large quiescent current of the buck converter's controller is incurred. Especially, the power efficiency of a discontinuous conduction mode (DCM) buck converter is mainly limited by the precision of its zero-crossing detector (ZCD), which controls and generates the timing signal to turn off the low-side switch M_N when the inductor current becomes zero. For instance, the timing error between the actual turn-off timing of M_N and the zero-inductor-current timing can incur a large power loss, either due to the body diode conduction when

M_N turns off too early or due to the inverse inductor current when M_N turns off too late, as shown in Fig. 1.3. To circumvent these losses, the ZCDs require high precision in detecting this timing error. However, the high-precision ZCDs employing a continuous-time comparator [4], [8]–[11] incur a large static power consumption (e.g., ~250 μW [4]) in operation.

1.2 Thesis Contribution and Organization

To address the aforementioned challenges in both start-up and steady-state operation, this dissertation proposes optimal inductor current control techniques for each operation.

First, in order to reduce the resistive loss ($E_{loss,st}$) at start-up operation, a switching-based stepwise charging technique [39] is proposed that can charge the capacitor with a current source; this can be realized by keeping the average inductor current constant and operating the buck converter in continuous conduction mode (CCM) with linearly incrementing duty-cycle ratios in a stepwise fashion.

Second, in order to minimize the required energy to charge the capacitor ($E_{loss,Cout}$) at start-up operation, a variable on-time pulse-frequency modulation (PFM) control [4] is proposed that can make use of a small C_{out} without degrading the steady-state performance such as voltage ripple and power efficiency; this can be realized by adaptively varying the on-time of PFM pulse with inversely proportional to the voltage difference between input and output (i.e., $T_{on} \sim 1/(V_{in} - V_{out})$), which can keep the peak inductor current constant.

Lastly, in order to reduce the controller loss ($E_{loss,conv}$) at steady-state operation, an adaptive off-time positioning ZCD (AOP-ZCD) is proposed, which is a sampling-based ZCD [1]–[3] with an adaptive off-time pulse generator that can achieve both high-precision in timing detection and low-power consumption in operation for wide ranges of input and output voltage conditions; this can be realized by the inductor current waveform prediction aided with the constant peak inductor current control.

This thesis is organized as follows. Chapter 2 describes the overall architecture of the proposed buck converter for battery-free applications. Specifically, the operation mode, overall architecture and building blocks of the proposed buck converter will be described. Chapter 3 provides the design concepts of the proposed optimal inductor current control techniques based on the detailed analysis. Specifically, energy savings from the switching-based start-up scheme [39], the variable on-time (VOT) PFM scheme [4] and the adaptive off-time positioning zero-crossing detector (AOP-ZCD) scheme will be described. Chapter 4 explains the detailed circuit implementation of the building blocks and shows their simulation results. Chapter 5 provides the measurement results of the proposed buck converter and Chapter 6 demonstrates the effectiveness of our approaches by applying the proposed buck converter to the battery-free wireless switch application.

Chapter 2

Operation Mode and Overall Architecture

After discussing the motivation and design issues of this work in Chapter 1, this chapter describes the operation mode and the overall architecture of the proposed buck converter for batter-free applications. The proposed buck converter employs both a continuous conduction mode (CCM) and discontinuous conduction mode (DCM) control schemes at each start-up and steady-state operation, respectively, to achieve maximum energy delivery. The principle of each control scheme will be discussed in detail in following sections.

2.1 Topology Selection

To down-convert the voltage, the step-down converter topology is required such as a buck converter or buck-boost converter as shown in Fig. 2.1. Considering that

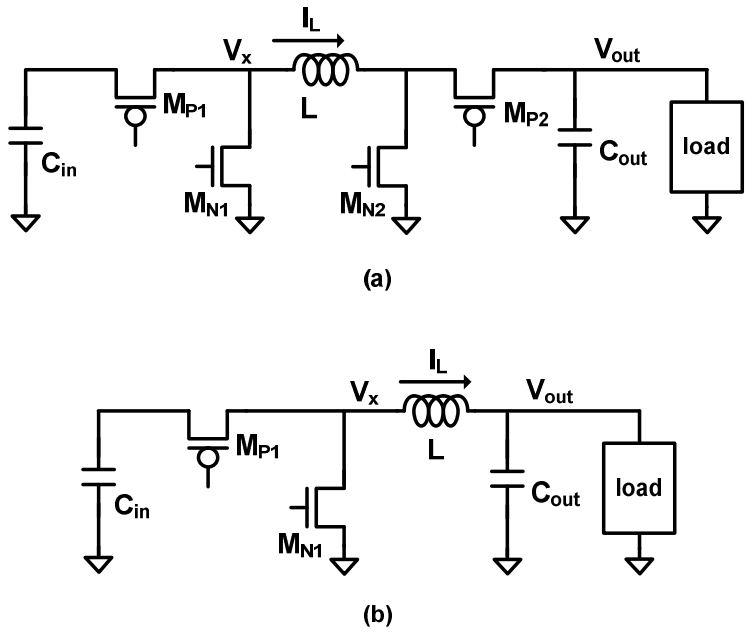

Fig. 2.1. Topology Comparison; (a) buck-boost, (b) buck.

the aim of the voltage regulator is delivering the maximum energy stored in the input capacitor to the load, the buck-boost topology could be preferable because it can operate even though the input voltage is lower than the output voltage, delivering more energy. However, this topology requires additional power switches M_{P2} and M_{N2} as shown in Fig. 2.1 (a), which incurs the larger conduction loss and switching loss. To reduce the conduction loss, the large-sized power switches are required; however, they occupy large silicon area. On the other hands, the simple buck topology as shown in Fig. 2.1 (b) does not require the additional power switches and hence this topology can achieve high efficiency and small silicon area. However, the buck topology can deliver the energy only when the input voltage is higher than the output voltage. Therefore, the rest of energy in the input capacitor could be wasted.

The topology chosen is the buck converter. Because the battery-free applications are realized by combining an energy harvester and ultra-low-power wireless application as described in Chapter 1.1, low supply voltages of the load systems (e.g., 1.0 V, 1.2 V) are used in practice. This means that the advantage of energy delivery in buck-boost topology is lost when the output voltage is low enough. Although the buck topology can deliver slightly smaller amount of energy, this topology can be more superior in ultra-low-power battery-free application because it can achieve high efficiency and reduce area.

2.2 Principle of Operation

The basic operation of the buck converter is stepping down the DC voltage efficiently by switching an inductor. In synchronous buck converter, two switches are used to control the inductor current and their switching signals determine the performance of the buck converter. Specifically, according to the duty-cycle ratios and switching frequency of switching signals, the performance such as current/voltage ripples and power efficiency can be changed and hence the optimal current controls should be analyzed first before designing. In buck converter, there are two operation modes; continuous conduction mode (CCM) and discontinuous conduction mode (DCM). Continuous inductor current mode is characterized by current flowing continuously in the inductor during the entire switching cycle in steady-state operation. Discontinuous inductor current mode is characterized by the inductor current being zero for a portion of the switching cycle. The two different modes will be discussed in this subsection.

2.2.1 Basic Operation in CCM

In continuous conduction mode, the buck power stage assumes two states per switching cycle. The ON state is when M_P turns on and M_N turns off. The OFF state is when M_P turns off and M_N turns on. The circuit diagram for each of the two states is shown in Fig 2.2. At ON state, the high-side switch turns on and the applied voltage across the inductor is the voltage difference between input and output (i.e., $V_L = V_{in} - V_{out}$) during DT, where D is a duty-cycle ratio of the switching signal ($0 < D < 1$) and T is a switching period. Because the voltage across the inductor V_L is a positive value, the inductor current increases with a slope of $(V_{in} - V_{out})/L$, where L is an inductance. At OFF state, the low-side switch turns on and the applied voltage across the inductor is the output voltage (i.e., $V_L = -V_{out}$) during $(1-D)\cdot T$. Because the voltage across the inductor V_L is a negative value, the inductor current decreases with a slope of $-V_{out}/L$. In steady-state operation, the amount of increase and decrease in inductor current should be same as expressed in (2.1). From this equation, we can find that the ratio between input and output voltage in CCM is proportional to the duty-cycle ratio.

$$\frac{V_{in}-V_{out}}{L}DT = \frac{V_{out}}{L}(1-D)T \quad \Rightarrow \frac{V_{out}}{V_{in}} = D \tag{2.1}$$

In other words, since the pulsed voltage V_x is filtered by a low-pass L/C filter to generate a DC voltage V_{out}, the average value of V_x equals to V_{out}. Ideally, if an inductor (L) and a capacitor (C_{out}) is large enough, a DC output voltage is generated and its voltage level varies with proportional to D.

However, because the inductance and capacitance values are finite, their non-

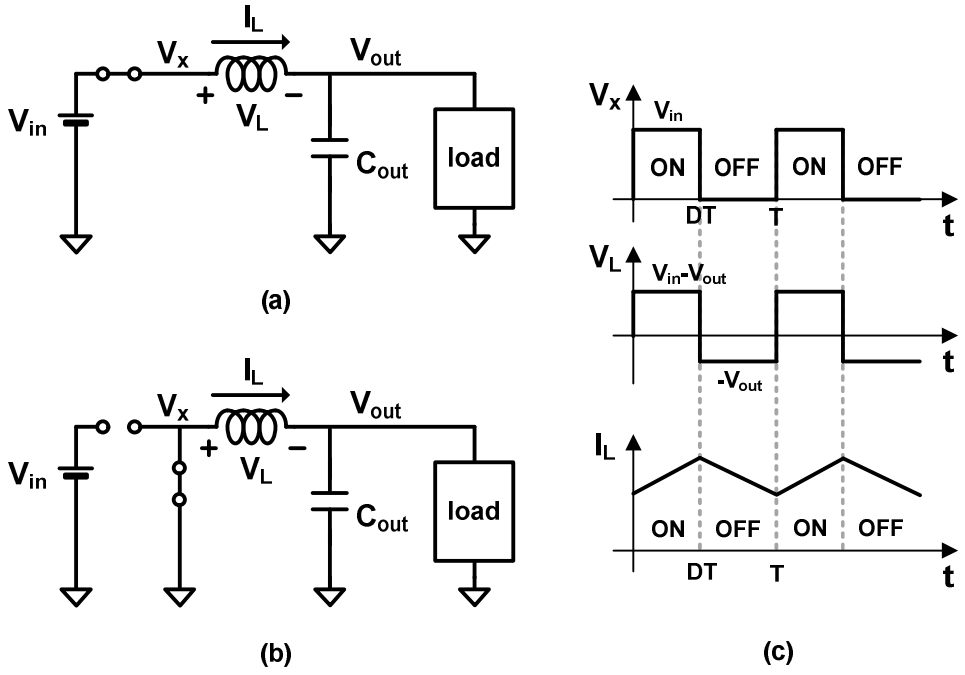

Fig. 2.2. Equivalent circuit diagrams of CCM buck converter at (a) ON state and (b) OFF state and its key waveforms.

idealities incur the current/voltage ripples. The maximum/minimum current $I_{\max}$ and $I_{\min}$ can be induced as (2.2), respectively, where I_{avg} is an average current (i.e., $I_{avg} = V_{out}/R_{load}$).

$$I_{max} = I_{avg} + \frac{V_{in} D(1-D)T}{2L}$$
$$I_{min} = I_{avg} - \frac{V_{in} D(1-D)T}{2L} \quad (2.2)$$

Therefore, the current ripple ($\Delta I_L = (I_{\max} - I_{\min})/2$) can be calculated. Since the AC component of the inductor current flows through the output capacitor, the capacitor

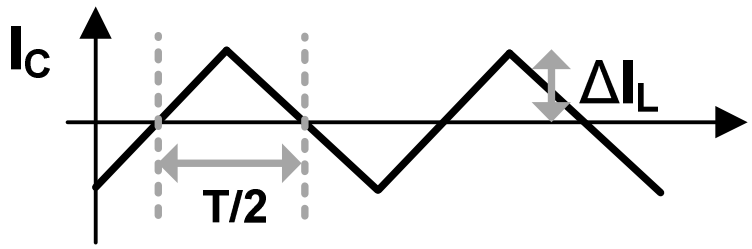

Fig. 2.3. Capacitor current waveform in steady-state operation.

current (I_c) can be plotted as shown in Fig. 2.3 and it generates the output voltage ripple (ΔV_{out}), which can be induced as (2.3).

$$\Delta V_{out} = \frac{1}{C} \cdot \Delta I_L \cdot \frac{T}{2} = \frac{V_{in}(1-D)D \cdot T^2}{8LC} \tag{2.3}$$

From (2.3), in order to minimize the voltage ripple, a fast switching frequency, a low input voltage, and large inductance and capacitance values are required.

2.2.2 Basic Operation in DCM

In discontinuous conduction mode, the buck power stage assumes three states per switching cycle as described in Fig.2.4. While the principle of operation of DCM buck converter almost same with that of the CCM buck converter as shown in Fig. 2.4 (a) and (b), there is an additional states (i.e., zero-inductor-current state) as described in Fig. 2.4 (c). When the high-side switch turns on, the inductor current increases with a slope of $(V_{in} - V_{out})/L$ and when the low-side switch turns on the inductor current decreases with a slope of $-V_{out}/L$ until the inductor current becomes zero. After this time, the stored charge in the output capacitor is transferred

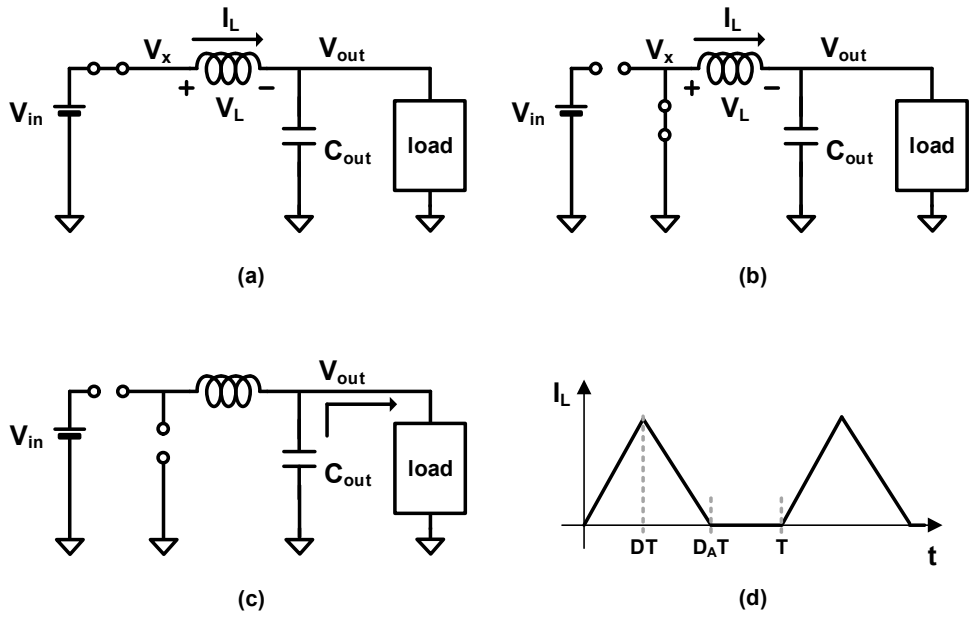

Fig. 2.4. Equivalent circuit diagrams of DCM buck converter and its key waveforms.

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to the load. In steady-state, the amount of increase and decrease in inductor current should be same as expressed in (2.4).

$$\frac{V_{in}-V_{out}}{L}DT=\frac{V_{out}}{L}(D_A-D)T \quad \Rightarrow \frac{V_{out}}{V_{in}}=\frac{D}{D_A} \tag{2.4}$$

Actually, the low-side switch turn-on time (i.e., $D_AT - DT$) is determined by the inductor peak current value and discharging slope.

$$D_AT-DT=\frac{I_{L,peak}\cdot L}{V_{out}} \tag{2.5}$$

From the fact that the charge transferred to the load in one switching cycle equals to the area of triangle of inductor current, D_A can be induced as (2.6).

$$D_A=\frac{2I_{load}}{I_{L,peak}} \tag{2.6}$$

From (2.5) and (2.6), D_A can be induced as function of switching period (T), inductance(L), duty-cycle ratio (D) and load current (I_{load}) as (2.7).

$$D_A=D+\frac{2I_{load}\cdot L}{D\cdot V_{in}\cdot T} \tag{2.7}$$

2.3 Operation Mode

To maximize the energy delivery, the proposed buck converter operates in CCM and DCM at start-up and steady-state operation, respectively. A simple block diagram of the proposed buck converter and its CCM/DCM controllers are illustrated in Fig. 2.5.

In start-up operation, the controller employs a pulse-width modulation (PWM) scheme to keep the average inductor current constant. The key principle of the start-up controller is that the energy is transferred from the input capacitor (C_{in}) to the output capacitor (C_{out}) by toggling the power switches (M_P and M_N) on and off multiple times, of which duty-cycle ratio linearly increments in a stepwise fashion. When the energy harvester collects the sufficient energy in C_{in}, the buck converter operates in the forward direction by turning on the high-side switch M_P and building up the positive inductor current that charges C_{out}. By linearly incrementing the duty-cycle ratio D from zero, the output voltage V_{out} increases linearly towards a desired voltage level, $V_{out} = D \cdot V_{in}$, which maintains the average inductor current constant.

After the charging C_{out} completes, the buck converter changes its operation mode in pulse-frequency-modulation (PFM) mode. The converter employs a PFM control scheme to regulate the output voltage, and to enhance the light-load efficiency by dynamically adjusting the switching frequency according to the load current. The key principles of the PFM control are that the on-time (T_{on}) of the high-side switching signal CK_P is adaptively scaled with inversely proportional to $V_{in} - V_{out}$ (i.e., $T_{on} \sim 1/(V_{in} - V_{out})$) and the off-time ($T_{off}$) of the low-side switching signal CK_N is also

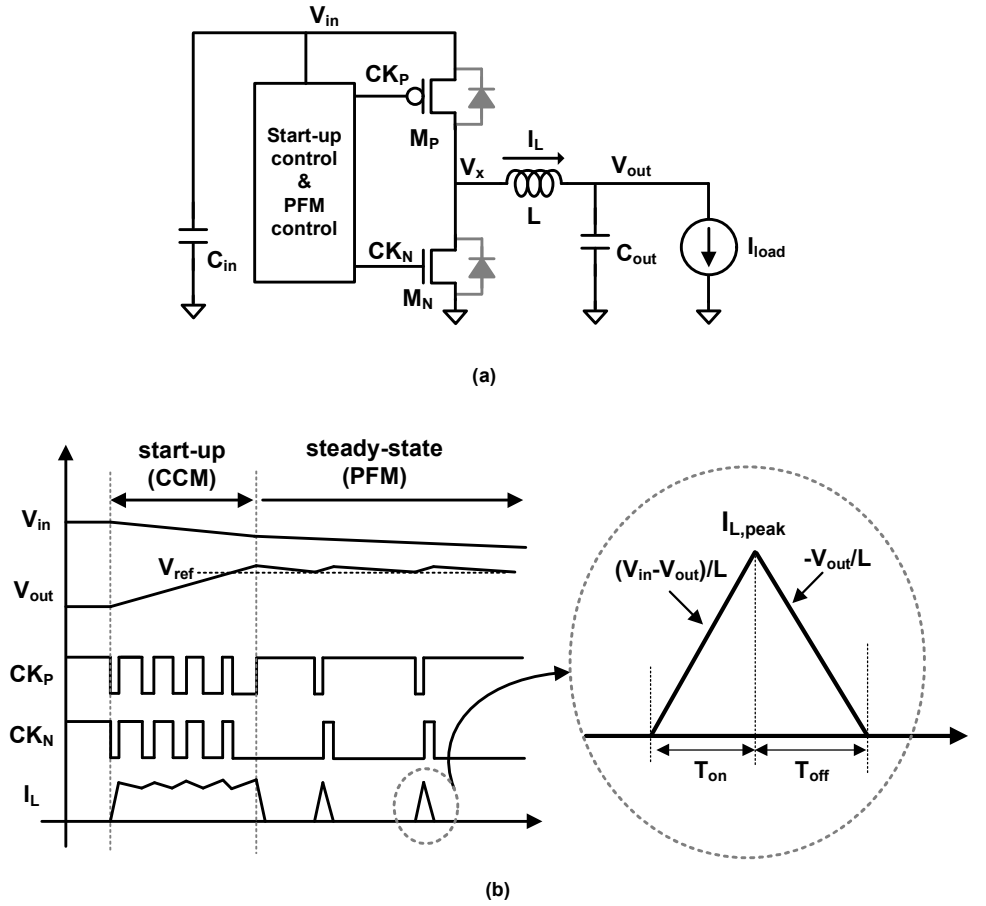


Fig. 2.5. (a) Simple block diagram of the buck converter and its controller, and (b) key operating waveforms.

adaptively scaled with inversely proportional to V_{out} (i.e., $T_{off} \sim 1/V_{out}$). The generated T_{on} can keep the inductor peak current constant regardless of V_{in} and V_{out} variation and the generated T_{off} can turn off M_N with the right timing by predicting the zero-inductor-current timing. The detailed design concepts of the proposed inductor current control techniques will be described in Chapter 3.

2.4 Overall Architecture

The overall architecture of the proposed buck converter is illustrated in Fig. 2.6. It is composed of a power stage of the buck converter, the switching-based stepwise charging scheme for start-up operation, the PFM control scheme including the variable on-time and adaptive off-time positioning ZCD, and the load system (i.e., 2.4-GHz WirelessUSB RF transceiver (CYRF8935)).

More specifically, during start-up, the switching-based stepwise charging scheme charges C_{out} with a constant inductor current, which is made by switching the buck converter with linearly incrementing the duty-cycle ratios. As shown in Fig. 2.6, it includes a voltage detector (VD), a duty-cycle controller (DCC), a digital pulse width modulator (DPWM), a non-overlap circuit and a 2:1 switched-capacitor (SC) converter. When the input capacitor (C_{in}) is charged to a desired voltage (e.g., 5 V) by an energy harvester, an enable signal (*en*) turns on a switch M_{en}. From this time, the input voltage V_{in} increases from zero to the capacitor voltage of C_{in} and then the proposed start-up controller begins to operate. When V_{in} reaches a predetermined voltage level (i.e., 2.8 V), a voltage detector (VD) generates a reset signal for the DCC, which generates pre-programmed 8-bit digital code (*DUTY_CTRL*). With this code, DPWM generates the pulse-width modulated signals (i.e., PWM_P and PWM_N) for both high-side and low-side switches (i.e., M_P and M_N). To prevent the significant power loss due to the crowbar current when both M_P and M_N turn on, the non-overlap circuit generate the dead time, where both M_P and M_N turn off. By linearly incrementing *DUTY_CTRL* from zero, the duty-cycle ratio (*D*) of the *PWM* clocks

also increase from zero; this can charge the output capacitor (C_{out}) linearly and stepwise, and can maintain the average inductor current constant. Note that a 2:1 switched-capacitor (SC) DC-DC converter is utilized to supply a lower voltage to the control circuits; the lower supply can greatly reduce the dynamic power consumption in control circuits.

The proposed PFM controller employs the variable on-time (VOT) pulse generator to keep the inductor peak current ($I_{L,peak}$) constant. When V_{out} reaches a desired output voltage that is determined by the output of a bandgap reference (BGR), an output sensing comparator (CMP) sets its output (V_{CMP}) low to high. This event enables the PFM controller and simultaneously disables the start-up controller to reduce the unnecessary power consumption. The VOT pulse generator generates the high-side switching signal CK_P, for which the pulse width (i.e., T_{on}) is set inversely proportional to $V_{in} - V_{out}$. Because the inductor current is charged from zero to $I_{L,peak}$ with a slope of $(V_{in} - V_{out})/L$ during T_{on}, the variable T_{on} can keep $I_{L,peak}$ constant for various V_{in} and V_{out} (i.e., $I_{L,peak} = (V_{in} - V_{out})/L \cdot T_{on} = const$).

To position the turn-off timing of M_N near the zero-inductor-current timing by predicting the inductor current waveform, the adaptive off-time positioning zero-crossing detector (AOP-ZCD) is proposed. When T_{on} ends, this event enables the AOP-ZCD, which is composed of an adaptive off-time (AOT) pulse generator and digital timing calibration loop. The AOT pulse generator generates the low-side switching signal CK_N, for which the pulse width (i.e., T_{off}) is set inversely proportional to V_{out} (i.e., $T_{off} \sim 1/V_{out}$). Because the inductor current is discharged from $I_{L,peak}$ to zero with a slope of $-V_{out}/L$ during T_{off}, the generated T_{off} can ideally turn off M_N when the inductor current reaches zero and the accurate zero-current switching

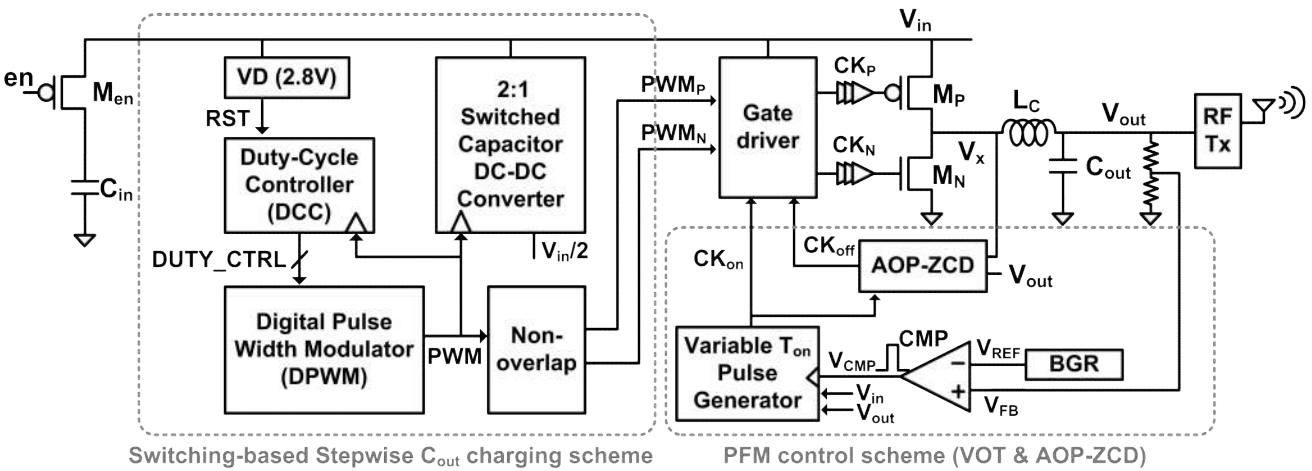


Fig. 2.6 Overall architecture of the proposed buck converter with a switching-based stepwise C_{out} charging scheme and a PFM control scheme including a variable on-time (VOT) pulse generator and an adaptive off-time positioning zero-crossing detector (AOP-ZCD).

(ZCS) timing of M_N can be predictable. However, the initially generated T_{off} is not enough to guarantee the precise ZCS operation because the timing error can be incurred by various non-ideal effects, such as process–voltage–temperature (PVT) variations, device mismatches, or series resistance of the power switches and inductor. To compensate for the residual timing error, a digital timing calibration loop in the AOP-ZCD adjusts the T_{off}.

Chapter 3

Optimal Inductor Current Controls for Maximum Energy Delivery

In Chapter 2, the operation mode and the overall architecture of the proposed buck converter were described. This chapter will discuss the optimal inductor current control techniques for maximum energy delivery in each start-up and steady-state operation in detail. Specifically, the previously-reported control schemes are described first, and then the proposed circuit techniques to reduce the energy losses introduced in Chapter 1 ($E_{loss,st}$, $E_{loss,Cout}$, $E_{loss,conv}$) for achieving the best performance will be explained based on the detailed analysis.

3.1 Constant Inductor Current Control with Switching-Based Stepwise Capacitor Charging Scheme

In this section, we describe the proposed start-up control scheme and its advantage compared to those of the previous ones. Before discussing the effectiveness of our approach, the previously reported capacitor charging schemes will be described first.

3.1.1 Conventional Charging Scheme with a Switch

In previous energy harvesting applications, a simple start-up switch [3], [35] was used to charge C_{out} as shown in Fig. 3.1 because they focused on the steady-state operation with a continuous energy source such as vibration or RF input, in which the steady-state power efficiency matters than the start-up energy loss. However, this method is not proper to the target application because the steady-state condition does not last long, which makes the transient energy loss during the start-up phase of the buck converter dominant. In this sub-section, we derive the start-up energy loss (i.e., $E_{loss,st} + E_{loss,Cout}$) when charging the capacitor with a switch to show that this scheme incurs the large energy loss at the switch.

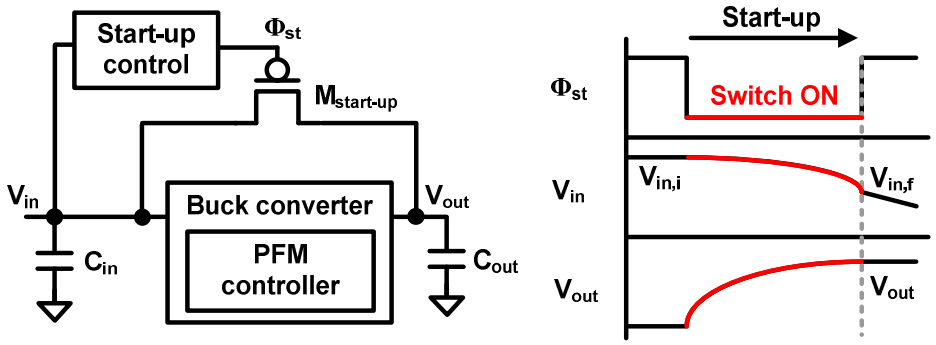


Fig. 3.1. Conventional start-up scheme with a simple switch $M_{\text{start-up}}$.

Its basic principle of charging C_{out} is the charge sharing between the input capacitor (C_{in}) and the output capacitor (C_{out}) by connecting them with a switch $M_{\text{start-up}}$. Since it charges C_{out} to V_{out} by directly connecting the voltage source (C_{in} can be considered as a voltage source), the large energy loss of $C_{\text{out}}V_{\text{out}}^2/2$ is incurred at the switch even if its resistance is an extremely low value.

More specifically, the total energy loss when the C_{in} is connected to the C_{out} with the $M_{\text{start-up}}$ can be derived as follows. Assuming that C_{out} is initially fully discharged and the initial voltage of the storage capacitor C_{in} is V_{in}, the final input voltage $V_{in,f}$ after charge sharing can be expressed as:

$$V_{in,f} = V_{in} - \frac{V_{out}C_{out}}{C_{in}} \tag{3.1}$$

Therefore, the energy usage of C_{in} during start-up operation (i.e. $E_{\text{loss,st}} + E_{\text{loss,Cout}}$) can be derived as (2):

$$E_{loss,st} + E_{loss,Cout} = \frac{1}{2}C_{in}(V_{in}^{\ 2} - V_{in,f}^{\ 2}) = V_{in}V_{out}C_{out} - \frac{V_{out}^{\ 2}C_{out}^{\ 2}}{2C_{in}} \tag{3.2}$$

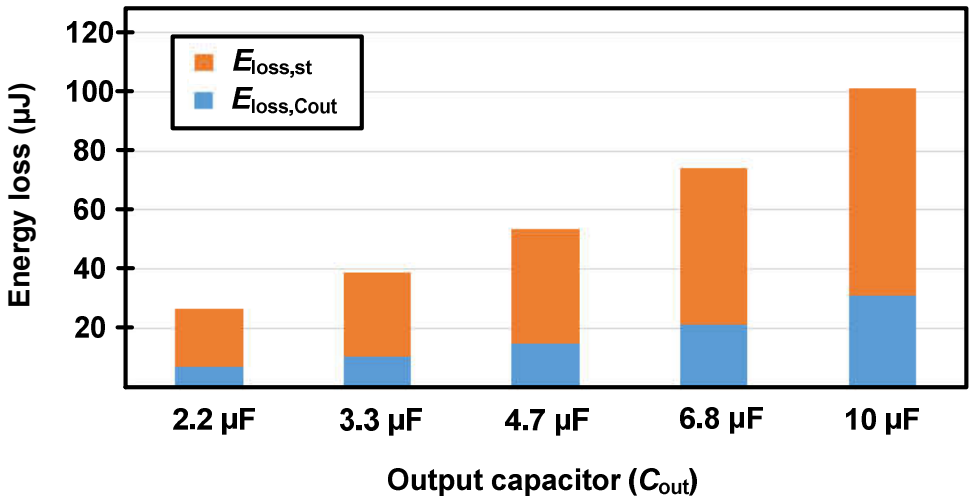


Fig. 3.2. Energy losses versus C_{out}.

Fig. 3.2 plots the energy losses in change with C_{out} from (3.2) with a 13.2-μF C_{in}, 5 V V_{in} and 2.5 V V_{out}. This figure shows that the large energy is lost at the switch and its loss increases as C_{out} increases. For instance, to charge a 2.2-μF C_{out} to V_{out}, 19.5-μJ energy is dissipated at the switch (i.e., $E_{loss,st}$), while 6.9-μJ energy is stored in C_{out} (i.e., $E_{loss,Cout}$). However, to charge a 10-μF C_{out} to V_{out}, 70.1-μJ energy is dissipated at the switch, while 31.3-μJ energy is stored in C_{out}. Considering that the energy stored in 13.2-μF C_{in} was 165 μJ, this charging scheme cannot be used in this application due to the excessively large energy loss incurred during charging C_{out}.

3.1.2 Adiabatic Stepwise Charging

The energy loss problem incurred when charging capacitor already existed in related fields. To reduce the resistive loss incurred at the switch, an capacitor charging technique called adiabatic switching has previously been researched for their energy efficient integrated circuits such as logic [45]–[47], SRAM [48] and clock driver networks [49], [50]. Specifically, adiabatic circuits use a stepwise charging method [41]–[44] that ideally dissipates no energy when the charging level moves between infinitesimal voltage levels as shown in Fig. 3.3. To charge the capacitor to the supply voltage V using the N-stepwise method, the intermediate reference voltages of the tank capacitors ($V_i = i \cdot V/N$) are connected to the load capacitor C in succession using the corresponding switches (T_1–T_N).

The effectiveness of adiabatic charging scheme is that charging the capacitor in N steps instead of a single step reduces the energy dissipation by a factor of N. To charge the capacitor C, each reference voltage level is connected to the capacitor in briefly in ascending order, until its voltage reaches the corresponding reference voltage level. While each reference voltage supply (i.e., voltage across tank capacitor) injects a charge to the capacitor, the energy loss at each switch (E_{TN}) can be expressed as:

$$E_{TN} = \frac{C(V_i - V_{i-1})^2}{2} = \frac{CV^2}{2N^2} \tag{3.3}$$

Therefore, the total energy loss at the switches (T_1–T_N) can be derived as:

$$E_{T1-TN} = E_{TN} \cdot N = \frac{CV^2}{2N} \tag{3.4}$$

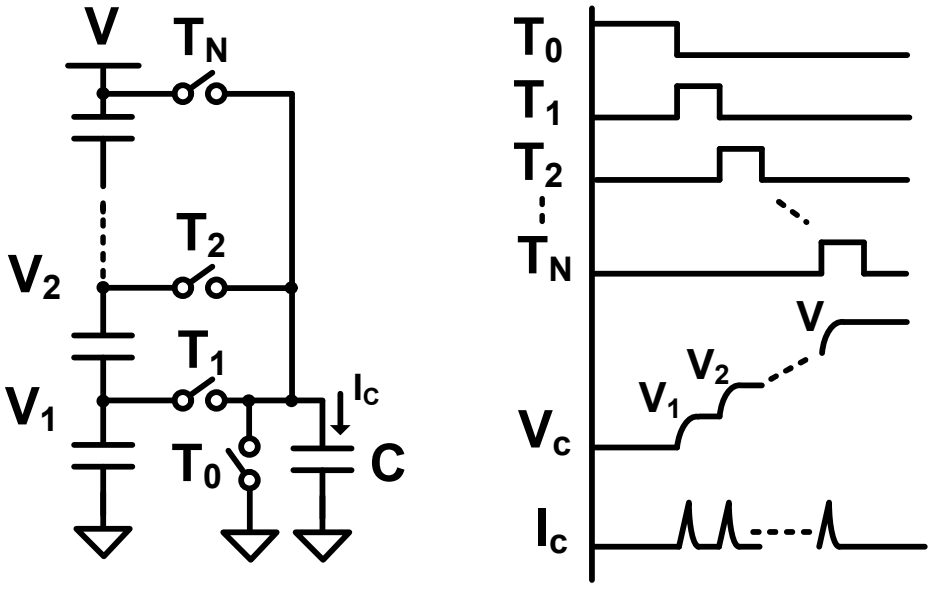


Fig. 3.3. Stepwise charging the capacitor with *N* tank capacitors.

Although this scheme can reduce the loss incurred at the switches, it is difficult to directly apply this technique to the battery-free applications because this method needs *N* additional tank capacitors to generate *N* step voltage levels, resulting in design complexity and increasing cost. Moreover, a large amount of energy is required to pre-charge *N* tank capacitors to their predetermined voltage levels.

3.1.3 Proposed Start-up Scheme

To efficiently charge C_{out} without incurring the loss at the start-up circuit (i.e., $E_{loss,st}$), the proposed start-up scheme [39] employs a current charging method as shown in Fig 3.4. Charging C_{out} with a current source can reduce $E_{loss,st}$ to zero ideally, while the required energy is only $E_{loss,cout}$ (i.e., $0.5C_{out}V_{out}^2$). Specifically, to realize the current source, the proposed start-up scheme directly uses the buck converter that can make the inductor current as a constant current source by switching the inductor. Note that $E_{loss,st}$ in the proposed scheme is the required energy to make the constant inductor current during the buck converter's start-up operation.

To reduce the $E_{loss,st}$, the proposed buck converter realizes the stepwise charging by digitally incrementing duty-cycle ratios in a stepwise fashion. Specifically, since the buck converter can generate an output voltage that is proportional to the duty-cycle ratio (D) (i.e. $V_{out} = DV_{in}$), N voltage levels can be generated without using the

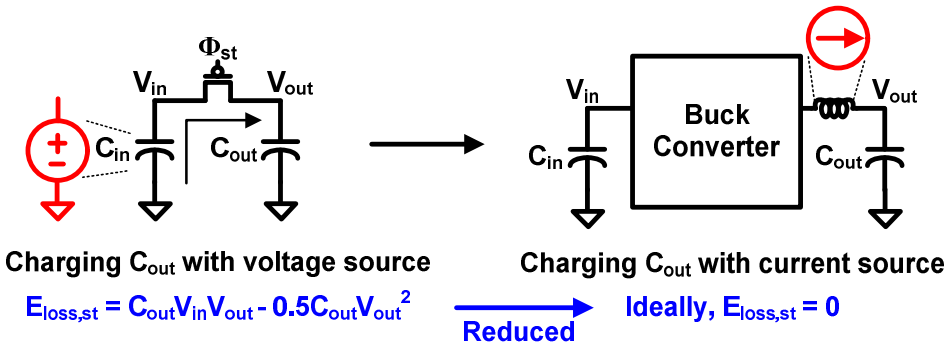


Fig. 3.4. Design concept of the proposed capacitor charging scheme with a current source.

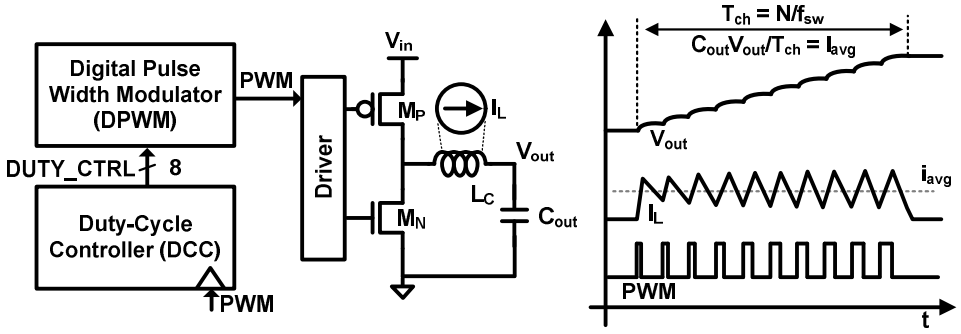


Fig. 3.5. Schematic of the switching-based stepwise capacitor scheme and its operating waveforms.

N pre-charged tank capacitors. By increasing V_{out} stepwise, the average inductor current can be kept constant and the $E_{loss,st}$ can be reduced by a factor of the number of stepwise voltage levels (N).

To control the duty-cycle ratio, the proposed start-up controller uses a digital pulse width modulator (DPWM) and duty-cycle controller (DCC), as shown in Fig. 3.5. The DPWM generates a pulse-width modulated (*PWM*) switching pulse to operate the buck converter in CCM and its duty-cycle ratio is digitally controlled by 8-bit *DUTY_CTRL* [7:0] from DCC. By linearly incrementing *DUTY_CTRL* [7:0], the buck converter can charge C_{out} to V_{out} in a stepwise fashion with the constant average inductor current.

To verify the effectiveness of this approach, the buck converter losses are derived. Fig. 3.6 illustrates the main buck converter losses during the start-up operation including the conduction and switching energy losses. First, the conduction loss (E_{cond}) is incurred at the resistive components such as the resistance of power switches (R_s) and inductor (R_L). During stepwise charging, the average inductor current (i_{avg}) can

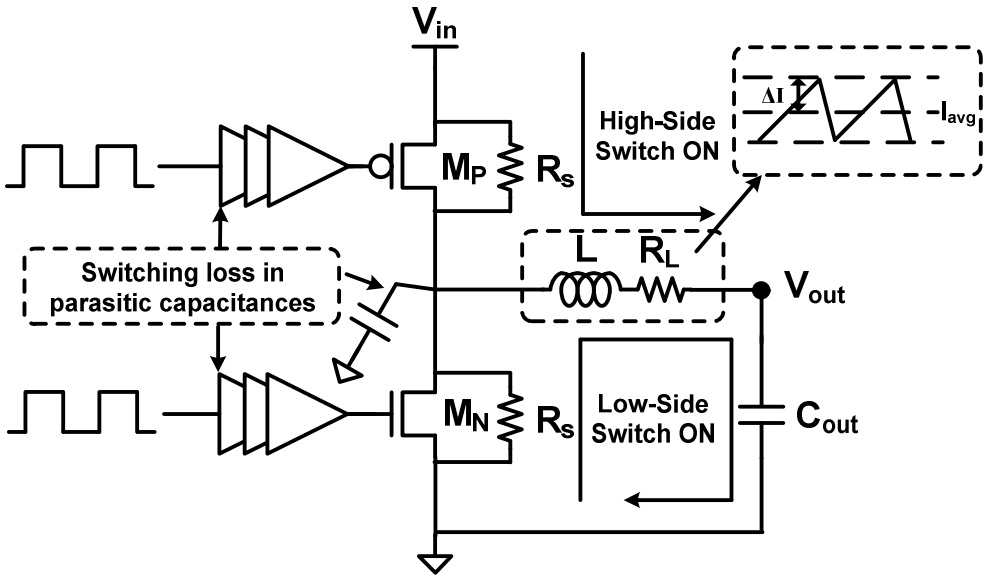


Fig. 3.6. Schematic of the loss components in the buck converter: R_s, R_L, and the parasitic capacitances in the switching nodes.

be maintained roughly constant due to the linearly increasing duty-cycle ratio, and its ripple current ($\Delta i[n]$) can be expressed as a function of the n-th duty-cycle ratio $D[n]$. Both i_{avg} and $\Delta i[n]$ can be expressed as (3.5) and (3.6), respectively,

$$i_{avg} = C_{out}\frac{dV_{out}}{dt} = \frac{C_{out}V_{out}}{T_{ch}} = \frac{C_{out}V_{out}f_{sw}}{N} \tag{3.5}$$

$$\Delta i[n] = \frac{V_{in}\cdot D[n]\cdot(1-D[n])}{L_C\cdot f_{sw}} \tag{3.6}$$

where T_{ch} is the charging time, f_{sw} is switching frequency of the *PWM* signal and L_C is the inductance. If the duty-cycle resolution is K, the n-th duty-cycle ratio $D[n]$ can be given by:

$$D[n] = n / K \quad (n = 1, 2, ..., N) \tag{3.7}$$

Note that the relationship between N and K is determined by the voltage conversion ratio, and hence the value of K can be expressed as:

$$K = \frac{NV_{in}}{V_{out}} \tag{3.8}$$

Assuming that transistors M_P and M_N have identical series on-resistances R_s and the inductor has a series resistance of R_L, and the total resistance in the current-delivering path is R (i.e., $R_s + R_L$), then the total conduction energy loss E_{cond} can be expressed as:

$$\begin{aligned} E_{cond} &= \frac{R}{f_{sw}} \sum_{n=1}^{N} (i_{avg}{}^2 + \frac{(\Delta i[n])^2}{12}) \\ &= \frac{RC_{out}{}^2 V_{out}{}^2 f_{sw}}{N} + \frac{RV_{in}{}^2}{12 L_C{}^2 f_{sw}{}^3} \sum_{n=1}^{N} (1 - \frac{n}{K})^2 (\frac{n}{K})^2 \end{aligned} \tag{3.9}$$

Note that from (3.9), assuming that E_{cond} is the dominant loss and f_{sw} is high enough to ensure that $\Delta i \cong 0$, then charging the capacitor over N steps instead of a single step can reduce the energy dissipation by a factor of N. Second, the switching loss E_{swit} is incurred in the internal parasitic capacitors in the switching nodes in the driver and power switches. Assuming that the sum of the internal capacitors is C_{int}, the dynamic energy loss E_{swit} can be expressed as:

$$E_{swit} = C_{int} V_{in}{}^2 f_{sw} (N / f_{sw}) = C_{int} V_{in}{}^2 N \tag{3.10}$$

While $E_{\text{loss,st}}$ is the sum of the energy losses derived in (3.9) and (3.10), we can find the optimal values of N and f_{sw} that can minimize the total energy loss for a given C_{out}. From the analysis, both E_{cond} and E_{swit} are highly dependent on the charging

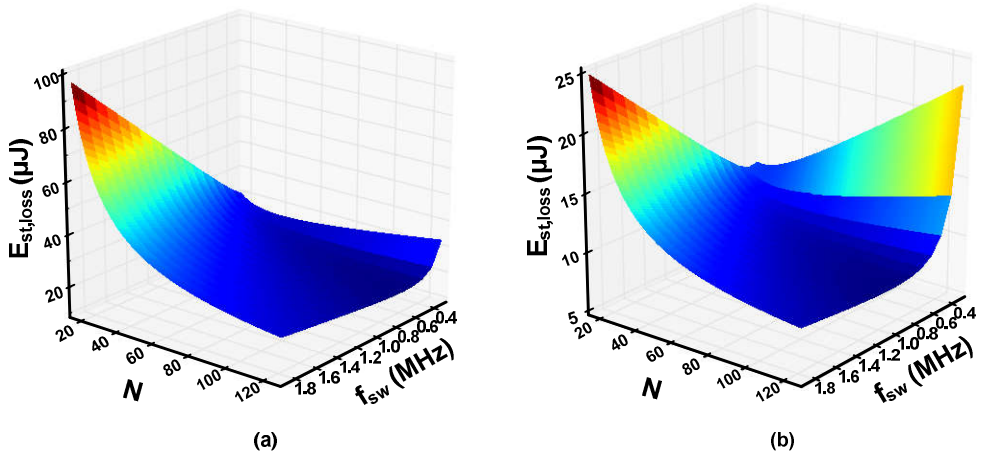


Fig. 3.7. Start-up energy loss ($E_{loss,st}$ + $E_{loss,Cout}$) in change with N and f_{sw}, when charging (a) 4.7-μF and (b) 2.2-μF capacitors.

time (i.e., $T_{ch} = N / f_{sw}$). Since i_{avg} is inversely proportional to T_{ch}, as given by (3.5), a large T_{ch} can reduce E_{cond}. However, a large T_{ch} incurs a large E_{swit} from (3.10). Fig. 3.7 illustrates the sum of the total energy loss in the buck converter ($E_{loss,st}$) and the stored energy in C_{out} ($E_{loss,Cout}$) with respect to changes in N and f_{sw} when charging a 4.7 μF and 2.2 μF C_{out}, respectively. To charge a 4.7-μF capacitor to 2.5 V, the action of switching the buck converter at 0.9 MHz and ramping the duty-cycle from 0 to ~50% over a 0.14-ms T_{ch} can maintain the start-up energy loss below 22 μJ, while the buck converter loss ($E_{loss,st}$) is only ~5.1 μJ (i.e., stored energy in 4.7-μF C_{out} ($E_{loss,Cout}$) is 14.7 μJ). From (3.5), we can find that the optimal inductor average current can be 84 mA in this case. In the same way, to charge a 2.2-μF capacitor to 2.5 V, the action of switching the buck converter at 1.2 MHz and ramping the duty-cycle from 0 to ~ 50% over a 0.11-ms T_{ch} can maintain the start-up energy loss below 10 μJ, while the buck converter loss ($E_{loss,st}$) is only ~1.7 μJ (i.e., stored energy in 2.2-μF C_{out} ($E_{loss,Cout}$) is 6.9 μJ). From (3.5), we can find that the optimal inductor

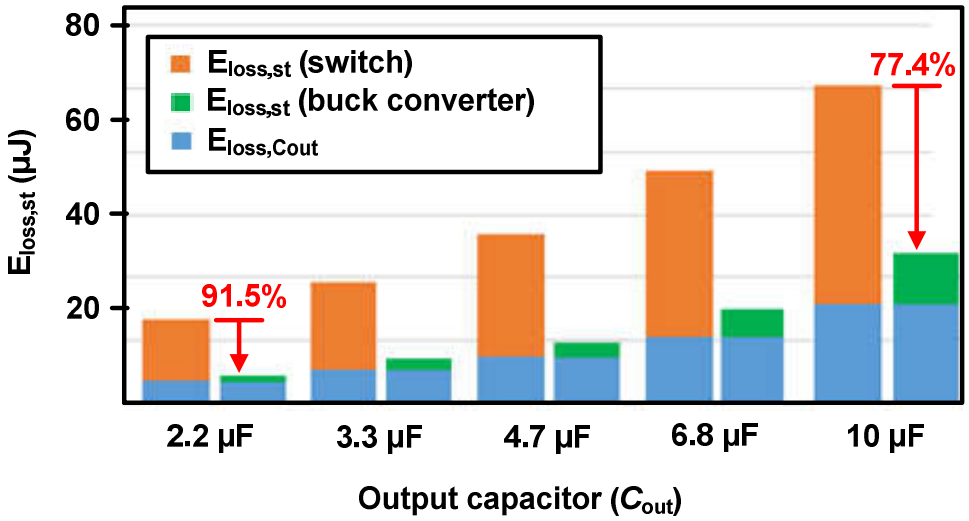


Fig. 3.8. $E_{loss,st}$ comparison between the conventional and the proposed start-up scheme.

average current can be 50 mA in this case. In both cases, the proposed start-up scheme can greatly reduce $E_{loss,st}$ compared to the conventional charging scheme with a switch.

Fig. 3.8 plots the comparison of the energy loss incurred at the start-up circuit $E_{loss,st}$ between the conventional (i.e., switch) and proposed (i.e., buck converter) schemes versus C_{out}, demonstrating the effectiveness of our approach. For instance, the proposed start-up scheme saves the energy by 91.5% at 2.2-μF case and by 77.4% at 10-μF case, respectively.

3.2 Constant Inductor Peak Current Control with Variable On-Time PFM Scheme

Although the proposed start-up scheme can reduce the $E_{loss,st}$, the PFM buck converter still calls for a large C_{out} to suppress the voltage ripples. Especially, because the input of the buck converter is a capacitor, its voltage decreases as the energy is delivered to the load, which demands for a larger C_{out} to achieve the voltage ripple within an acceptable range needed by the application over wide range of input voltage conditions. In this sub-section, the design concept of the variable on-time PFM scheme will be explained that enables the use of a small C_{out} to reduce $E_{loss,Cout}$, while maintaining small voltage ripples and high efficiency over wide range of input voltage conditions.

3.2.1 Basic Operation of PFM Buck Converter

The DCM buck converters are widely used in many emerging low-power applications, including energy harvesting systems [1]–[4], wearable devices [5], medical sensors [3], [6], and the Internet of Things (IoT) [4] because they can achieve high efficiency at light loads and can extend the battery life. Especially, the buck converter employs a pulse-frequency modulation (PFM) control can save the energy in light load condition by adjusting the switching frequency according to the load current.

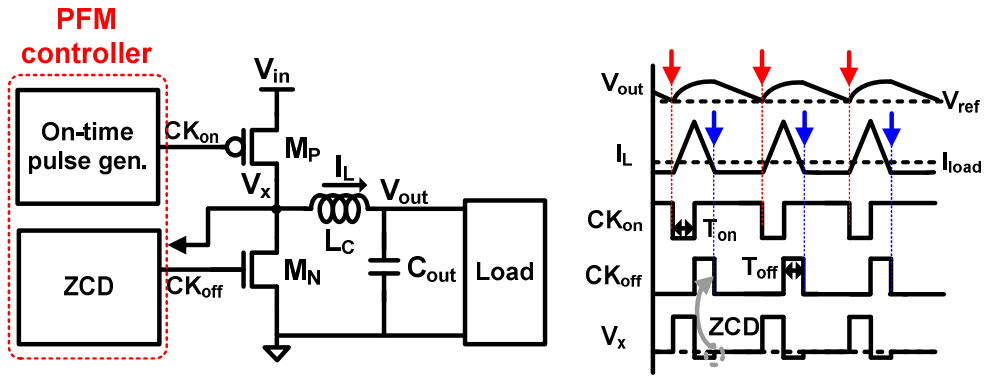


Fig. 3.9. Simple schematic of the buck converter with PFM control operating in DCM and its key waveforms.

The simple schematic of the buck converter with PFM control operating in DCM and its key waveforms are illustrated in Fig. 3.9. When the output voltage V_{out} becomes smaller than the reference voltage V_{ref}, an on-time pulse generator generates the high-side switching signal CK_{on}, of which the pulse width is T_{on}. During the on-time (T_{on}), the high-side power transistor (M_P) turns on and the inductor current increases with a slope of $(V_{\text{in}} - V_{\text{out}})/L$. When M_P turns off, simultaneously the low-side switching signal CK_{off} is generated, of which the pulse width is T_{off}. During the off-time (T_{off}), the low-side power transistor (M_N) turns on and the inductor current decreases with a slope of $-V_{\text{out}}/L$ until it reaches zero. At this time, the zero-current detector (ZCD) turns off M_N to prevent the reverse inductor current, which can incur the significant power loss. When both switches turn off, the stored charge in the output capacitor (C_{out}) is delivered to the load until V_{out} becomes smaller than V_{ref} again.

In the PFM controller, the on-time (T_{on}) determines the various key performance such as the inductor peak current ($I_{L,peak}$), the switching frequency (f_{sw}) and the volt-

age ripple (V_{ripple}). From the amount of increase in the inductor current (I_L) during the on-period (T_{on}), the inductor peak current can be derived as:

$$\frac{(V_{in} - V_{out})T_{on}}{L} = \frac{V_{out}T_{off}}{L} = I_{L,peak} \tag{3.11}$$

This equation shows that the inductor peak current is determined by the voltage difference between input and output and the on-time period. Note that the amount of the increase and decrease in the inductor current should be same in the PFM control from the fundamental inductor current balancing equation and hence the off-time is determined by the inductor peak current and output voltage from (3.11). The total charge (Q_{total}) stored in the inductor is the area under the inductor current waveform in one switching period, which can be express as:

$$Q_{total} = \frac{I_{L,peak}(T_{on} + T_{off})}{2} \tag{3.12}$$

Assuming that the power loss of the buck converter is zero (i.e., resistive components in current path assumed to zero) and it regulates the output voltage ideally (i.e., the zero-crossing timing of the inductor current is detected at the right timing), the charge transferred to the load can be expressed as (3.13), where T_{sw} is the switching period, which is determined by the load current (I_{load}).

$$Q_{total} = I_{load} \cdot T_{sw} \tag{3.13}$$

Since the total charge stored in the inductor is equal to the charge transferred to the load in one switching period (T_{sw}) from (3.13), the switching frequency (f_{sw}) can be derived as:

$$f_{sw} = \frac{2I_{load}}{I_{L,peak}(T_{on} + T_{off})} \tag{3.14}$$

During T_{on} and T_{off}, the total charge (Q_{total}) stored in the inductor is decomposed into the charge transferred to the load and temporarily stored in the output capacitor (i.e., Q_{cap}). Especially, Q_{cap} causes the voltage ripple (V_{ripple}). In other words, the area of $I_L - I_{load}$ (i.e., Q_{cap}) determines V_{ripple} and, it can be derived as:

$$V_{ripple} = \frac{(I_{L,peak} - I_{load})^2 (T_{on} + T_{off})}{2C_{out} I_{L,peak}} \tag{3.15}$$

Consequently, to ensure that the voltage ripple remains within an acceptable range needed by the application, the proper value of the on-time (T_{on}) should be selected.

3.2.2 Constant On-Time PFM Scheme

The constant T_{on} (COT) PFM scheme [14]–[17] have been widely used when the buck converter operates in the narrow ranges of input and output voltages. In other words, the optimal value of T_{on} can be a constant when the operating voltages are fixed. However, if the input supply varies under the COT control, both the inductor peak current value and the charge transferred to the load in each switching cycle can also vary, which results in producing a widely varying voltage ripple and an average value of the output voltage.

Especially, in the battery-free applications, the design challenges arise from the fact that the input supply voltage decreases as the charge in the input capacitor is delivered to the load. In other words, the decreasing input voltage incurs the widely varying inductor peak current because its slope during T_{on} is proportional to $V_{in} - V_{out}$ from (3.11). Fig. 3.10 (a) shows that the amount of charge transferred decreases as the input voltage decreases. This is due to the decrease of the inductor peak current from (3.12), which results in the fast switching frequency from (3.14) and defeats the power-saving advantage of the PFM control at a low V_{in}. To alleviate this problem, a possible way is to increase the value of the on-time from the start (i.e., larger T_{on}). By increasing T_{on}, a slow switching frequency at a low V_{in} can be achieved as shown in Fig. 3.10 (b). However, this larger T_{on} causes the high voltage ripple at a high V_{in} as shown in Fig. 3.10 (c). Therefore, the COT PFM scheme must use the large output capacitor (C_{out}) to suppress the voltage ripple at a high V_{in}, which is not proper to the battery-free application because the large C_{out} can incur the start-up energy loss as illustrated in Fig. 3.8.

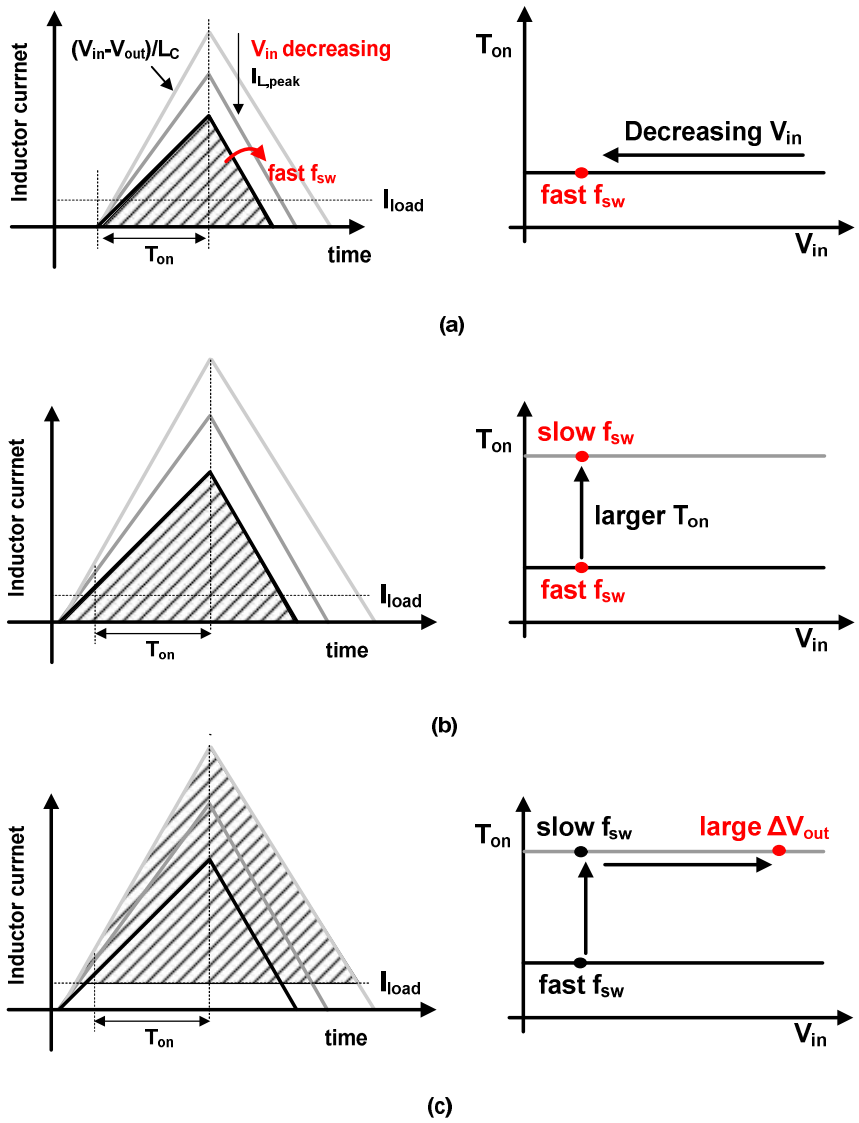


Fig. 3.10. Inductor current waveforms under constant on-time PFM scheme; (a) switching frequency increase at low V_{in}, (b) slow switching frequency with larger T_{on} at low V_{in} and (c) resulting large voltage ripple at high V_{in}.

3.2.3 Variable On-Time PFM Scheme

To address this problem, the variable on-time (VOT) PFM scheme is proposed that enables the use of a small C_{out}, while maintaining the small voltage ripple and the low switching frequency over wide ranges of input voltage conditions. Specifically, the VOT pulse generator keeps the inductor peak current ($I_{L,peak}$) by varying T_{on} inversely proportional to the $V_{in} - V_{out}$ as shown in Fig. 3.11 (a). At a high V_{in}, the VOT pulse generator generates a small T_{on}, which enables the use of a small C_{out} by reducing the worst case voltage ripple. In addition, the variable T_{on} increases as the input voltage decreases, which can improve the power efficiency by reducing the switching frequency at a low V_{in}. Consequently, under the VOT PFM control, the inductor peak current can be kept constant regardless of V_{in} variation by adaptively varying T_{on} as shown in Fig. 3.11 (b). Even for the various input and output voltages, by adaptively varying the on-time, the variation of the amount of charge transferred,

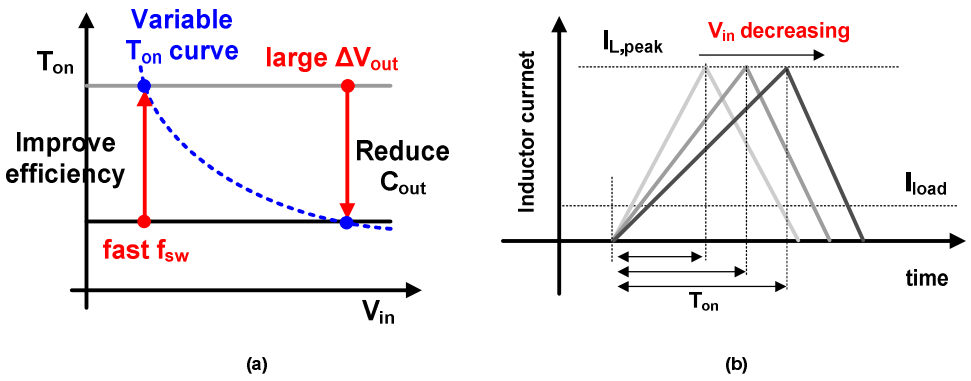


Fig. 3.11. Proposed variable T_{on} curve to reduce C_{out} and improve the power efficiency.

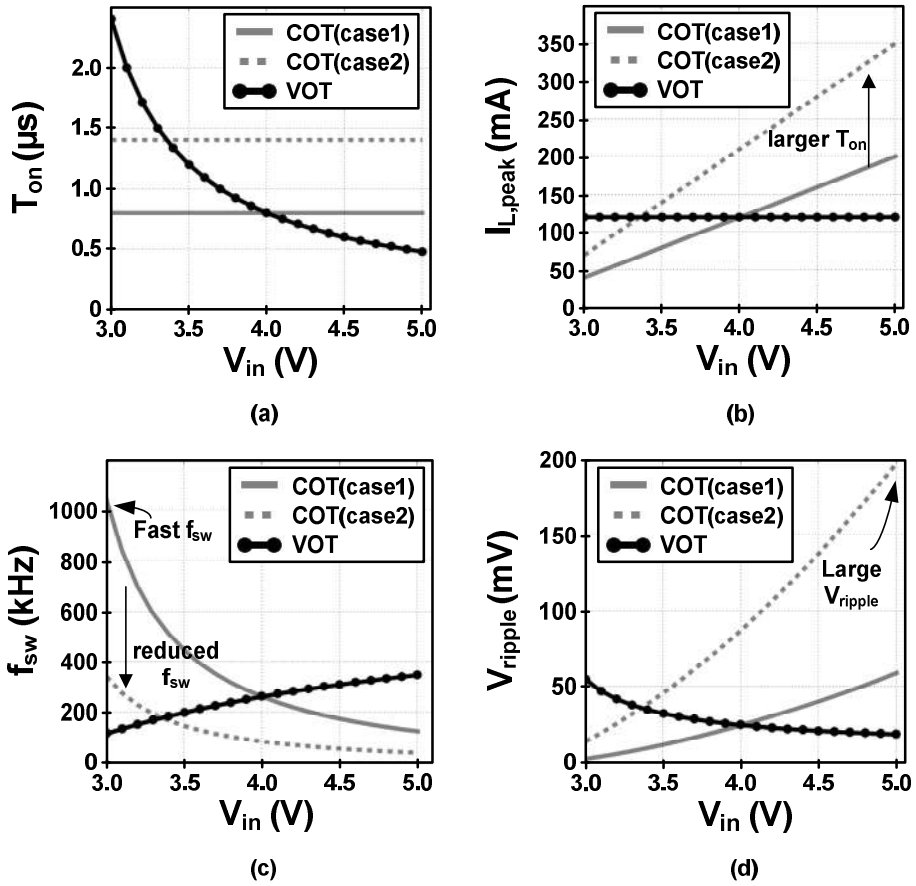


Fig. 3.12. Performance comparison between the variable T_{on} (VOT) and the constant T_{on} (COT); (a) T_{on} value, (b) inductor peak current ($I_{L,peak}$), (c) switching frequency (f_{sw}) and (d) voltage ripple (V_{ripple}).

which is the area of I_L, can be reduced and be kept fairly constant.

The performance comparison between the variable T_{on} (VOT) and the constant T_{on} (COT) controls are illustrated in Fig. 3.12. These figures are plotted based on the equations derived in Section 3.2.1 If T_{on} is a constant value, $I_{L,peak}$ can widely vary

with V_{in}; this can incur widely varying V_{ripple} and f_{sw} across the range of V_{in}. For instance, when T_{on} has a constant value of 800 ns (i.e., Case 1) with a 10-μH inductor, $I_{L,peak}$ is proportional to V_{in} and varies between 50 mA and 200 mA as V_{in} changes from 3 V to 5 V [see Fig. 3.12 (b)]. This means that it is difficult to operate the buck converter at a low V_{in} because the amount of charge that is transferred to the load during one switching period is dramatically reduced as V_{in} decreases. In addition, $I_{L,peak}$ at 3 V V_{in} is too small, thereby incurring a very high f_{sw} of 1 MHz, which degrades the light-load efficiency (see Fig. 3.12 (c)). Since both $I_{L,peak}$ and T_{off} decrease as V_{in} decreases, f_{sw} is inversely proportional to the square of V_{in} from (3.14). Therefore, a larger T_{on} is required to reduce f_{sw} (i.e., Case 2). For instance, the larger T_{on} of 1.4 μs can reduce f_{sw} to 350 kHz, but this causes an unnecessarily large $I_{L,peak}$ of 350 mA at 5 V V_{in}, thereby causing a large V_{ripple} of 200 mV (see Fig. 3.12 (d)). An alternative way to suppress V_{ripple} is to use a large C_{out}, but this incurs the large start-up loss as mentioned before.

On the other hands, the variable T_{on} (VOT) can reduce the worst case V_{ripple} and f_{sw}. Specifically, the variable T_{on} can maintain both $I_{L,peak}$ and T_{off} constant from (3.9). Since these two design parameters are fixed, the variation of f_{sw} and V_{ripple} according to V_{in} can be effectively reduced from (3.14) and (3.15) (see Fig. 3.12 (c) and (d)). As a result, the VOT PFM scheme can achieve a reduced worst-case V_{ripple} of 50 mV that makes it possible to enable the use of a small C_{out} (i.e., reducing $E_{loss,Cout}$), and a reduced worst-case f_{sw} of 400 kHz that improves the power efficiency.

3.3 Inductor Current Prediction with Adaptive Off-time Positioning ZCD (AOP-ZCD)

While the VOT pulse generator can improve the power efficiency by reducing the worst case switching frequency as described in 3.2.3, the controller power loss is still large because the continuous-time ZCDs consume the large static power. To reduce $E_{\text{loss,conv}}$ by minimizing the static power consumption of the zero-crossing detector, the adaptive off-time positioning ZCD is proposed that can predict the zero-inductor-current timing without using the power-hungry continuous-time comparator. In addition, it can achieve high resolution and fast-tracking time in its timing detection for wide ranges of input and output voltages.

3.3.1 Previous Sampling-Based ZCD

The energy loss problem due to the large quiescent current of the ZCD circuit in steady-state operation have previously been addressed by introducing sampling-based ZCDs [1]–[3]. Fig. 3.13 (a) and (b) compare the block diagrams of the continuous-time ZCD and the sampling-based ZCD. The continuous-time ZCD can accurately find the zero-inductor-current timing and generate the timing signal CK_N to turn off M_N for wide ranges of input and output voltages, but its comparator dissi-

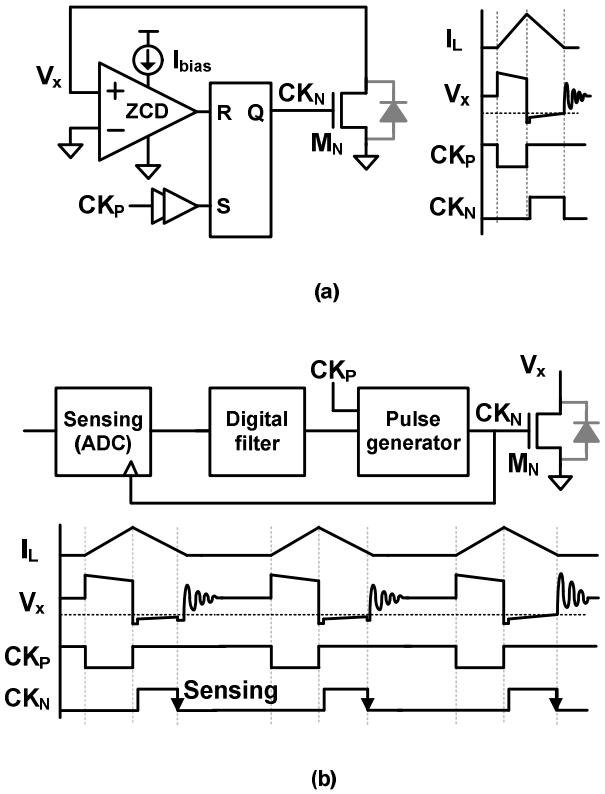


Fig. 3.13. Block diagram of (a) the continuous-time ZCD and (b) the sampling-based ZCD.

pates large static current (e.g., ~100 μA [4]) to achieve high precision. On the other hands, the sampling-based ZCD detects the zero-inductor-current timing by using a timing error detector such as a clocked comparator [2] and a successive approximation register analog-to-digital converter (SAR-ADC) [3]. Specifically, because it detects whether M_N turns off too early or late by sampling the inductor current direction only once per switching cycle, the static power consumption can be reduced. Depending on the polarity of the sampled inductor current direction, the ZCD then increases or decreases the digital filter output accordingly and eventually, it con-

verges to an appropriate value. Controlled by the digital filter output, a pulse generator can generate an appropriate timing signal for the accurate ZCS operation of M_N.

While the sampling-based ZCD can lower the power consumption by eliminating the continuous-time comparator, it cannot be applied to the battery-free applications because it cannot operate over wide ranges of input and output voltage conditions without degrading either timing resolution or its time to converge to the optimal ZCS timing. To cover such a wide range of voltage conditions, the sampling-based ZCD must have a wide calibration range of timing because the zero-inductor-current timing can widely vary according to the voltage conditions. To extend the calibration range, a possible way is either to increase the unit step size or to increase the number of steps. However, the former sacrifices the precision (i.e. coarse resolution), while the latter convergence time. Due to these tradeoffs, the previous sampling-based ZCDs were used with narrow ranges of input/output voltage conditions.

3.3.2 Proposed Adaptive Off-time Positioning ZCD

To achieve both high resolution and short convergence time over wide range input and output voltage conditions, the adaptive off-time positioning ZCD (AOP-ZCD) is proposed, which is a sampling-based ZCD with an adaptive off-time (AOT) pulse generator. The block diagram of the proposed AOT-ZCD including the AOT pulse generator and the timing calibration loop is illustrated in Fig. 3.14. While the on-time T_{on} was scaled with inversely proportional to the voltage difference between input and output (i.e., $T_{on} \sim 1/(V_{in} - V_{out})$) as discussed earlier, now the AOT pulse generator generates the off-time T_{off} scaled with inversely proportional to the output voltage (i.e., $T_{off} \sim 1/V_{out}$). Therefore, the AOT pulse generator can always position the initial turn-off timing of M_N close to the zero-inductor-current timing regardless of V_{in} variation from the fundamental inductor current balancing equation in (3.11). Since the initial timing error between the initial turn-off timing of M_N and the zero-inductor-current timing can be always kept small, the ZCD can have a narrow calibration range enough to compensate the residual timing error. Therefore, the timing calibration loop can converge quickly with high resolution.

However, the initially generated T_{off} by the AOT pulse generator is not enough to guarantee the precise ZCS operation because the timing error can be incurred by various non-ideal effects, such as process–voltage–temperature (PVT) variations, device mismatches, or series resistance of the power switches and inductor. To compensate for the residual timing error, the timing calibration loop adjusts the T_{off} controlled by the digital filter output. Specifically, this digital calibration loop operates in a bang-bang control mode, sampling the inductor current direction at the falling

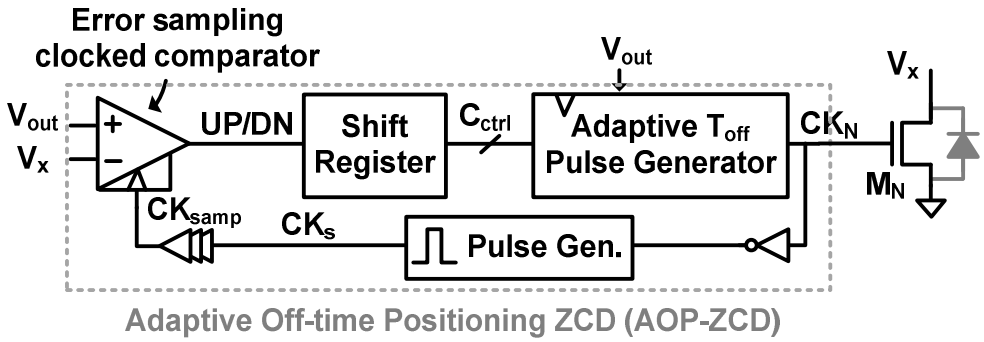


Fig. 3.14. Block diagram of the proposed AOT-ZCD.

edge of CK_N and incrementing or decrementing a 7-bit digital code C_{ctrl} based on the sample result *UP*/*DN*.

Chapter 4

Circuit Implementation

While the specific design concepts of the proposed inductor current controls were explained in Chapter 3, the detailed circuit implementation to realize the proposed control schemes will be described in this chapter.

4.1 Circuit Implementation of Switching-Based Stepwise Capacitor Charger

As shown in Fig. 2.2, the proposed switching-based stepwise capacitor charging scheme includes the voltage detector (VD), the digital pulse width modulator (DPWM), the duty-cycle controller (DCC) and 2:1 switched-capacitor DC-DC converter. In this section, their circuit implementation will be explained.

4.1.1 Voltage Detector (VD)

The voltage detector circuit is used as a power-on reset (POR) that detects the power applied to the buck converter and generates a reset impulse to place the DCC into an initial state. Since it operates only once at first, its static power consumption should be minimized. For this reason, the voltage detector circuit is implemented based on the subthreshold operation of transistor (i.e., leakage current-based design).

Fig. 4.1 (a) shows the schematic of the voltage detector (VD) circuit, where the number of series diodes determines the detection voltage level. When V_{in} reaches a predetermined level set by the forward voltage of the series-connected diodes, the V_x node switches from low to high and turns on M_2, which begins to discharge the pre-charged V_Y node to ground. Then, the latch formed by M_3 and M_4 makes a sharp transition to switch the output signal *rst* from low to high. The low-threshold devices M_5–M_8 operate in the subthreshold conduction mode, enabling the circuit to use the

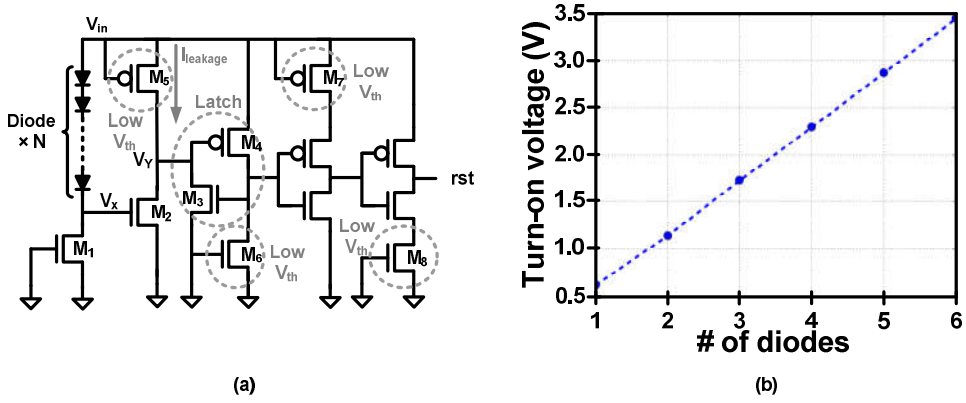


Fig. 4.1. (a) Schematic of the leakage-based voltage detector and (b) the simulation result of the detection voltage.

leakage current, thereby limiting the loss incurred by the crowbar current. Fig. 4.1 (b) shows the simulation result of the turn-on voltage as a function of the number of diodes connected in series. To detect 2.4 V, four diodes are used, which consume 12.4 nW.

4.1.2 Digital Pulse Width Modulator (DPWM)

The digital pulse width modulator (DPWM) is the key building block of the proposed switching-based stepwise capacitor charger that generates the pulse width modulated (PWM) signal, of which duty-cycle is controlled by DCC.

Fig. 4.2 (a) shows the circuit implementations of the proposed DPWM and the digitally-controlled capacitor array (DCCA), respectively. Fig. 4.2 (b) shows their operating waveforms. The DPWM is composed of two current-integrating stages, two crossing detectors, and an SR latch that form a relaxation oscillator. In the current-integrating stages, a constant current source I_{const} charges the digitally controlled on-chip capacitors C_1 and C_2 in alternating fashion. When the signals *PWM* and *PWMB* are reset to logic 1 and 0, then I_{const} charges C_1, and M_4 discharges C_2 to ground. When V_{C1} reaches the threshold voltage V_{th}, the crossing detector output switches to logic 1, and *PWM* and *PWMB* are switched to logic 0 and 1, respectively. This time, the current source I_{const} charges C_2, and M_2 discharges C_1 to ground, until the voltage on C_2 reaches V_{th}. Note that the on-time T_{on} and off-time T_{off} are set in the time it takes to charge capacitors C_1 and C_2 to the predetermined level (V_{th}), respectively. The switching period T_{sw} is equal to the sum of T_{on} and T_{off}, each of which is proportional to the capacitances C_1 and C_2, respectively, and expressed as:

$$T_{sw} = T_{on} + T_{off} = \frac{V_{th}}{I_{const}}(C_1 + C_2) \tag{4.1}$$

From (4.1), it can be seen that the duty-cycle ratio $D = T_{on}/T_{sw}$ can be set based on the ratio between C_1 and $C_1 + C_2$.

The proposed DPWM digitally controls the capacitances C_1 and C_2 via an 8-bit

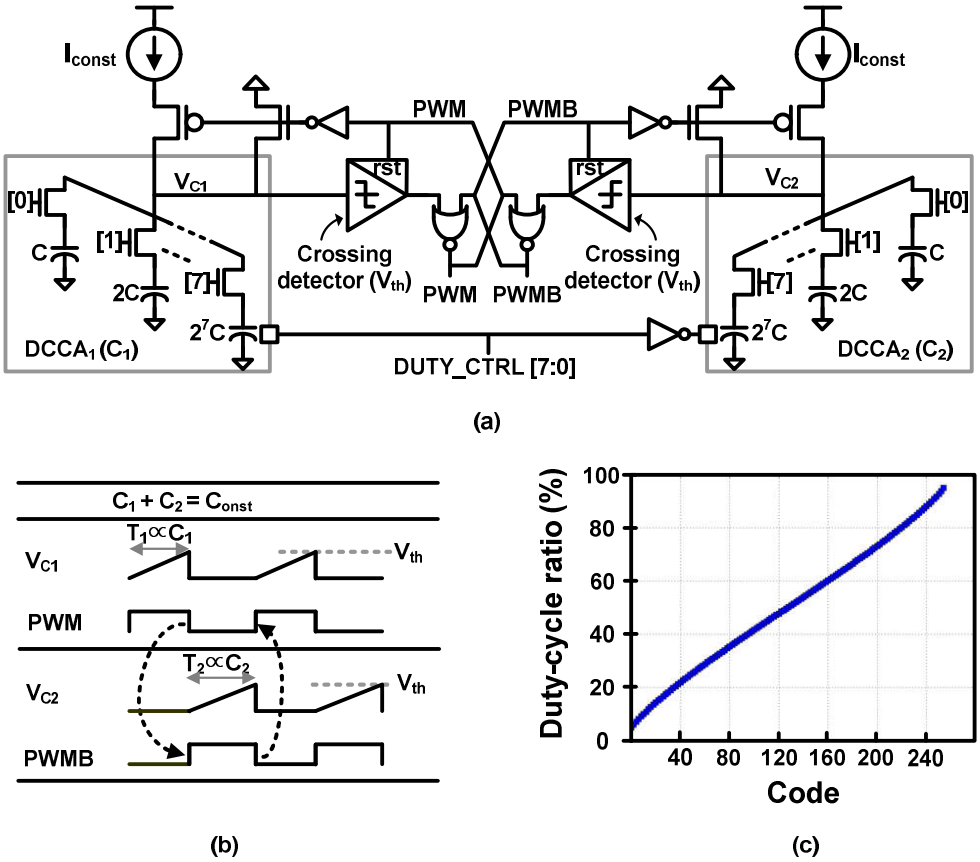


Fig. 4.2. (a) Circuit implementation of DPWM, (b) its key waveforms, and (c) simulation result of the duty-cycle ratio versus *DUTY_CTRL* [7:0].

digital code obtained from the set of digitally switchable binary-weighted capacitor arrays. To set the *PWM* output frequency, the digital codes controlling C_i and C_2 are changed in a complementary fashion to keep $C_1 + C_2$ constant at $(2^8-1)C$, where C is the unit capacitance. The minimum and maximum duty-cycle ratios, $D_{\min}$ and $D_{\max}$, are set by the parasitic capacitance C_{par} present at nodes V_{C1} and V_{C2}, respectively, as expressed in (4.2):

$$D_{\min} = \frac{C_{par}}{(2^8 - 1)C + 2C_{par}} \ , \ D_{\max} = \frac{(2^8 - 1)C + C_{par}}{(2^8 - 1)C + 2C_{par}} \qquad (4.2)$$

As can be seen from the simulation results in Fig. 4.2 (c), the duty-cycle ratio curve is linear with respect to the digital code, and the minimum and maximum duty-cycle ratios are 4% and 96%, respectively, by keeping the parasitic capacitance C_{par} sufficiently small compared to C_1 and C_2. Considering that the DPWM dissipates 60 μW, and it takes 0.11-ms T_{ch} to charge a 2.2-μF C_{out} to 2.5 V, this circuit consumes only 6.6 nJ of energy.

4.1.3 Programmable Duty-Cycle Controller (DCC)

The programmable duty-cycle controller (DCC) linearly increments or decrements the pulse-width of the *PWM* signal at a programmable rate by producing a programmable 8-bit digital code pattern *DUTY_CTRL*. Fig. 4.3 (a) shows the block diagram of the DCC. The DCC is essentially a programmable counter that consists of 7-bit and 8-bit digital counters and a digital comparator. The rate at which the count is incremented or decremented is set by the counting threshold N_{th}, which in turn sets the charging time T_{ch}.

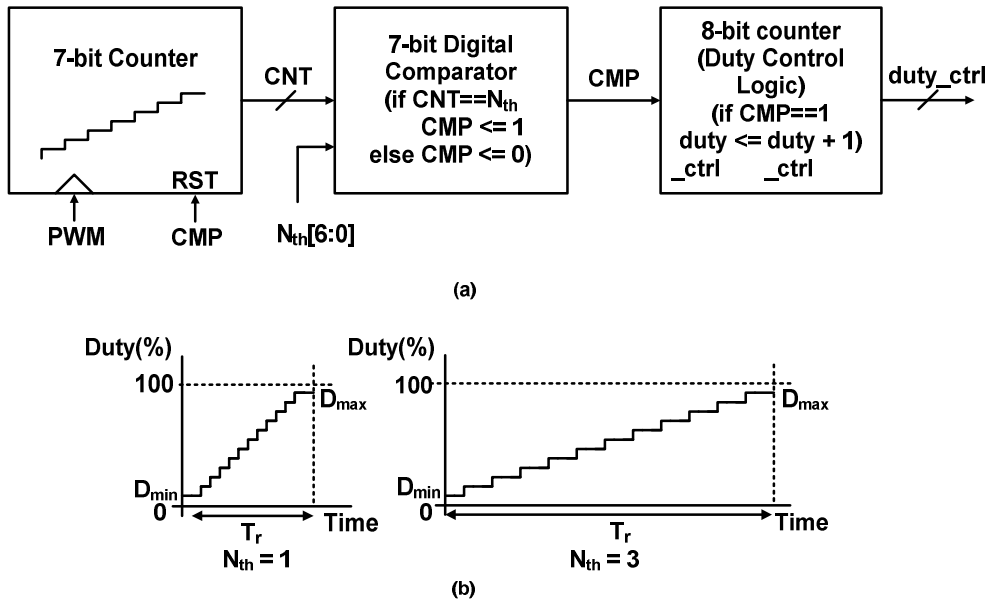


Fig. 4.3 (a) Block diagram of the programmable duty-cycle controller and (b) the example trajectory of the duty-cycle during the charging operation when $N_{th} = 1$ and $N_{th} = 3$.

The duty-cycle controller operates as follows. First, when the reset signal from VD is generated, the PWM clock is configured to have a minimum pulse width D_{min} and is fed into the 7-bit digital counter. The counter starts to count the number of positive edges of the clock. When the count CNT reaches the predetermined value of N_{th}, the comparator output CMP switches to logic 1 and *duty_ctrl* increments by 1. The counter is then reset to 0 and repeats the counting process. In this way, N_{th} sets the charging period T_{ch} (i.e., average inductor current) of the proposed start-up scheme. To illustrate this further, Fig. 4.3 (b) shows an example trajectory of the duty-cycle during the charging period.

4.1.4 Switched Capacitor (SC) Step-Down Converter

Fig. 4.4 describes the circuit implementation of the 2:1 switched-capacitor (SC) step-down converter and its key operating waveforms. The SC converter supplies a low DC voltage to the controller in order to reduce its dynamic power consumption. A switched-capacitor (SC) type converter was selected because the expected load power is very low at below 1 mW and precise regulation of the voltage is not critical.

The SC converter is composed of a frequency divider, a level-shifter, a non-overlapping pulse generator, and a SC converter power stage. The counter-based frequency divider divides the *PWM* clock frequency by 16 and generates a 50% duty-cycle clock *CLK*. The level-shifter converts *CLK* into a clock with a high-voltage swing *CLK_H*, and the non-overlapping pulse generator ensures that the complementary switching signals P_{sig} and N_{sig} have sufficient non-overlapping periods between them to avoid causing crowbar currents in the SC converter.

Fig. 4.5 shows a simplified schematic of the 2:1 SC converter implemented in this work. The converter stage has two power-train capacitors C_1 and C_2 and a flying

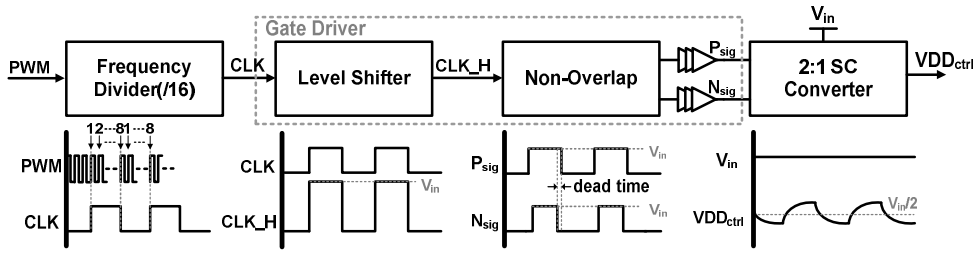


Fig. 4.4 Block diagram of 2:1 switched-capacitor (SC) step-down converter including the gate driver circuit and its key waveforms.

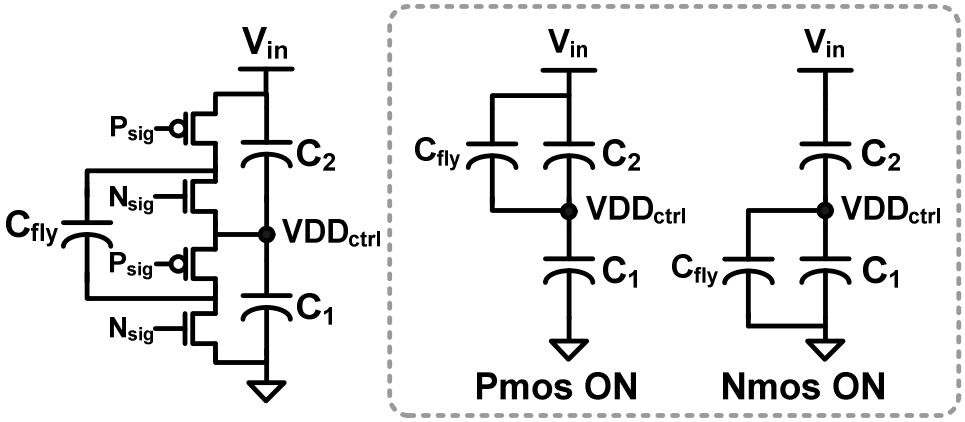


Fig. 4.5 Circuit implementation of the 2:1 switched-capacitor (SC) converter.

capacitor C_{fly}, which are all implemented using off-chip ceramic capacitors. When the input voltage is in the range of 3–5 V, the converter produces an output equal to half of the input voltage by periodically switching between the two capacitor configurations. When the PMOS power switches turn on, C_{fly} is charged from the battery. When the NMOS power switches turn on, C_{fly} transfers the charge to the output. The 2:1 SC converter as designed is over 90% efficient and only uses two 100-nF power train capacitors and a 50-nF flying capacitor.

4.2 Circuit Implementation of Variable On-Time Pulse Generator

The variable T_{on} can be realized with the time needed to charge the capacitor C from its zero reset state to a predetermined voltage V_{th} with a variable current source I_{on} (i.e., $T_{on} = C \cdot V_{th}/I_{on}$). To make T_{on} inversely proportional to $V_{in} - V_{out}$, the variable I_{on} should be scaled with proportional to $V_{in} - V_{out}$. Fig. 4.6 illustrates a simple block diagram of the VOT pulse generator and its timing diagram. When V_{out} becomes smaller than the reference voltage V_{ref}, an output voltage sensing comparator produces a pulse V_{CMP} and then its falling edge enables the T_{on} pulse generator by

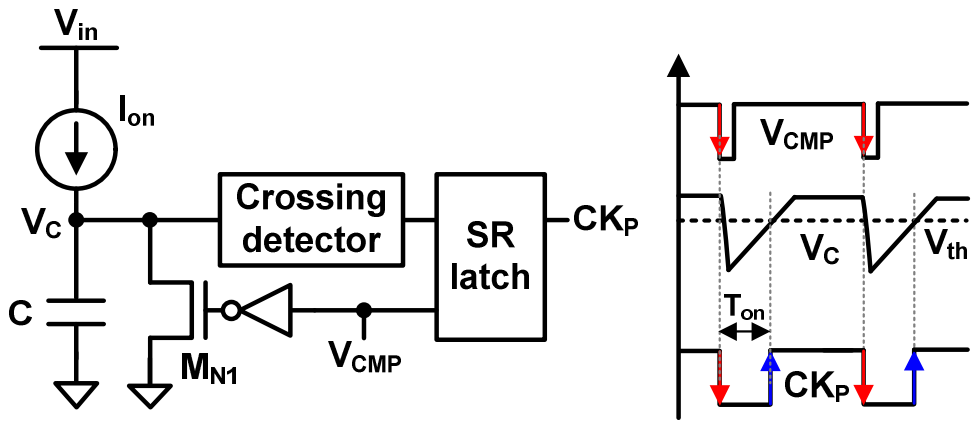


Fig. 4.6 Simple block diagram of the variable on-time (VOT) pulse generator and its key waveforms.

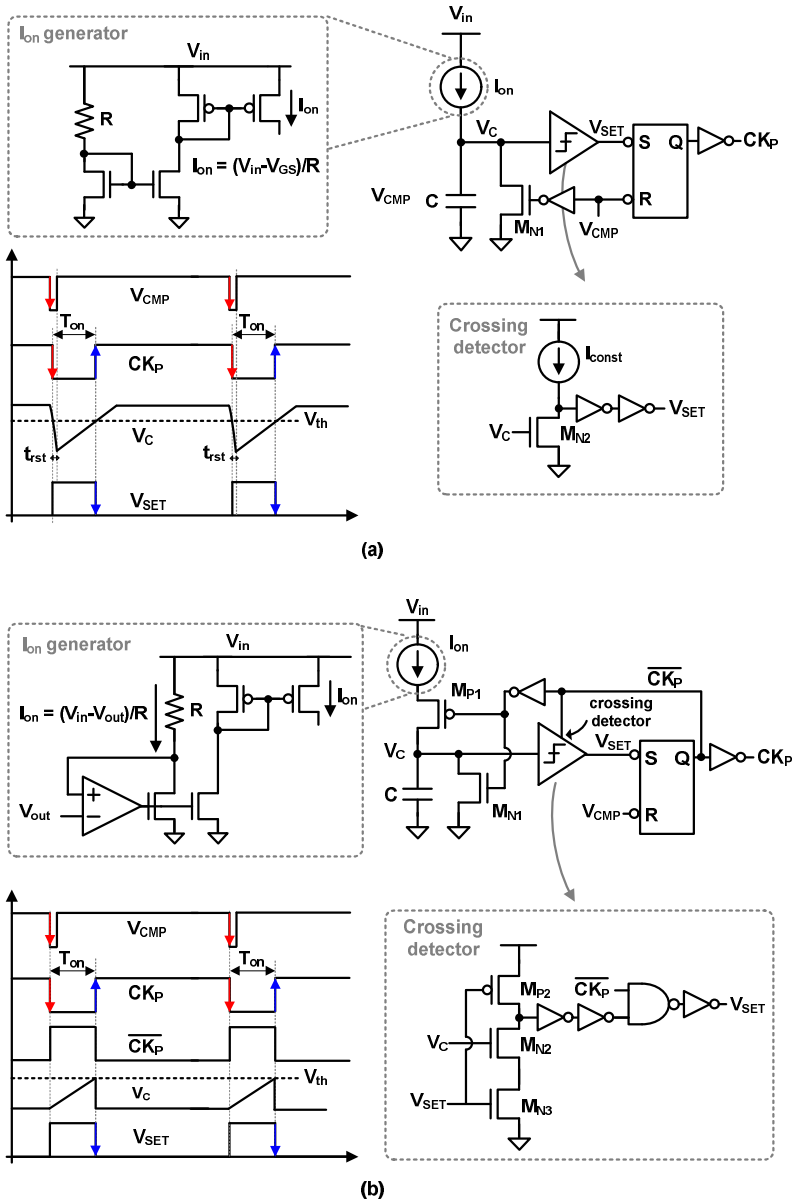


Fig. 4.7 Circuit implementations of (a) the previous VOT pulse generator and its key waveforms and (b) the proposed ones.

resetting CK_P to ground. This simultaneously turns on M_{N1} to discharge C to the zero reset state. After M_{N1} turns off, I_{on} starts to charge C. When the capacitor voltage V_C reaches the predetermined threshold voltage V_{th}, the crossing detector sets the rising edge of CK_P.

However, the previously-reported VOT pulse generators [8], [11] illustrated in Fig. 4.7 (a) had some design issues such as inaccurate T_{on} and large power consumption. Specifically, the variable I_{on} was scaled with proportional to the voltage difference between input and gate-to-source voltage (i.e., $V_{in} - V_{GS}$ [8]), while it was determined by the voltage across a sensing resistor R (i.e., $I_{on} = (V_{in} - V_{GS}) / R$). In addition, the reset time (t_{rst}) of the capacitor increased the T_{on} unnecessarily because V_C was reset right before charging operation. Hence, the generated T_{on} in previous VOT pulse generators was inaccurate, as expressed below:

$$T_{on} = \frac{RCV_{th}}{V_{in} - V_{GS}} + t_{rst} \tag{4.3}$$

Moreover, during the M_{N1} turn-on time while C is discharged and the M_{N2} turn-on time while V_C is higher than V_{th}, the current sources of I_{on} and I_{const} were directly connected to the ground (i.e., crowbar current) that consumes an unnecessary power.

The proposed VOT pulse generator illustrated in Fig. 4.7 (b) can address these issues by generating the accurate T_{on} with an additional op-amp in I_{on} generator and a proper reset timing of the capacitor, and by preventing the crowbar current with additional switches. Specifically, in the proposed I_{on} generator, the op-amp sets the voltage across the sensing resistor R to $V_{in} - V_{out}$, which allows Ion to be perfectly adjusted by $(V_{in} - V_{out})/R$. In addition, by feeding CK_P to M_{N1}, V_C can be reset right after when it reaches V_{th} and hence the reset time does not affect the T_{on}. By modify-

ing the I_{on} generator and changing the reset timing, the accurate T_{on} can be generated, as expressed below:

$$T_{on} = \frac{CV_{th}}{I_{on}} = \frac{RCV_{th}}{V_{in} - V_{out}} \tag{4.4}$$

Moreover, an additional M_{P1} controlled by CK_P can prevent the crowbar current of I_{on} by turning it on only when I_{on} charges C, and additional switches M_{P2} and M_{N3} in the crossing detector can reduce the crowbar current of I_{const} by preventing both switches from turning on simultaneously.

To verify the circuit performance, the proposed VOT pulse generator was simulated with a 570-kΩ on-chip resistor R and 7-pF on-chip metal–insulator–metal (MIM) capacitor C. Fig. 4.8 (a) plots the simulated T_{on} with both V_{in} and V_{out} changing. The dotted lines represent the ideal T_{on} curves from (4.4). The proposed circuit

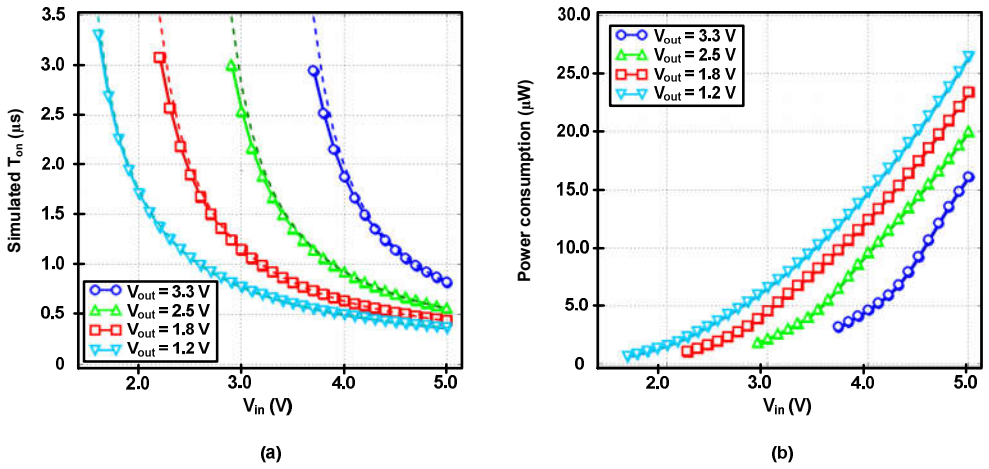


Fig. 4.8 Simulation results of the VOT pulse generator: (a) the simulated T_{on} and (b) its power consumption for various V_{in} and V_{out} conditions.

generated the accurate T_{on} that can keep $I_{L,peak}$ constant at $(V_{in} - V_{out}) \cdot T_{on}/L \cong 140$ mA under various V_{in} and V_{out} conditions. In addition, a low power consumption of less than 30 μW was achieved, as shown in Fig. 4.8 (b).

4.3 Circuit Implementation of Adaptive Off-time Positioning ZCD

As shown in Fig. 3.14, the proposed adaptive off-time positioning ZCD (AOP-ZCD) includes the adaptive off-time (AOT) pulse generator, the timing error detector and the shift-register. In this section, their circuit implementation will be explained.

4.3.1 Adaptive Off-Time (AOT) Pulse Generator

The AOT pulse generator can be implemented with the almost same principle as that of the VOT pulse generator. Fig. 4.9 illustrates the circuit implementation of the AOT pulse generator. To make the T_{off} inversely proportional to V_{out}, the adaptive current source I_{off} is scaled with proportional to V_{out} and hence the generated T_{off} can be expressed as:

$$T_{off} = \frac{CV_{th}}{I_{off}} = \frac{RCV_{th}}{V_{out}} \tag{4.5}$$

In addition, a digitally controlled capacitor array C_{off} is implemented to make T_{off} adjustable by the digital timing calibration loop. Its capacitance value is determined by the 7-bit digital code C_{ctrl}[6:0] as expressed in (4.6), where its initial capacitance value should be the same with C (i.e., 7 pF) in the VOT pulse generator to meet the requirement that the amount of increase and decrease in the inductor current during

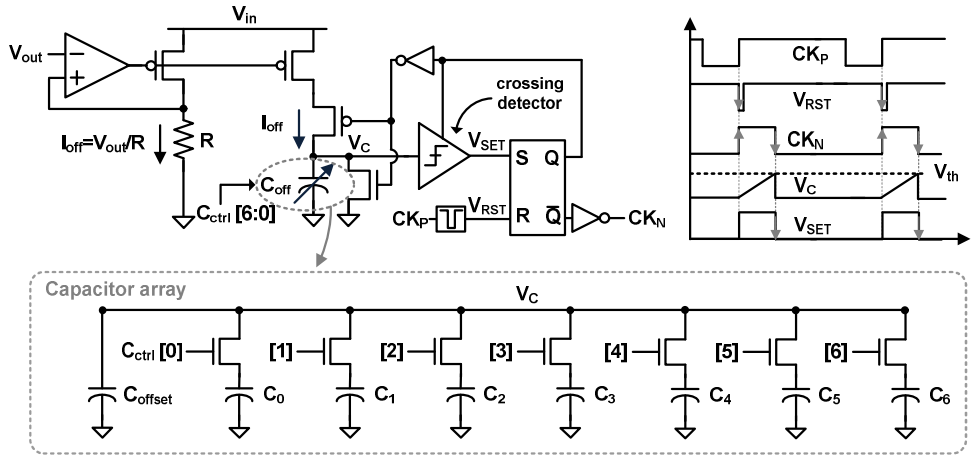


Fig. 4.9 Circuit implementation of the proposed AOT pulse generator and its key waveforms.

T_{on} and T_{off} must be same.

$$C_{off} = C_{offset} + C_{ctrl}[0]\cdot C_0 + C_{ctrl}[1]\cdot C_1 + \cdots + C_{ctrl}[6]\cdot C_6 \tag{4.6}$$

To verify the circuit performance such as the accuracy of T_{off}, the power consumption and the timing resolution, the AOT pulse generator was simulated with the same value of R (i.e., 570 kΩ) in that of the VOT pulse generator. However, the initial value of C_{off} was intentionally designed to be slightly smaller (i.e., 6.7 pF) than that of the VOT pulse generator (i.e., 7 pF) to avoid the significant power loss from the reverse inductor current when M_N turn off late. Fig. 4.10(a) plots the simulated T_{off} with both V_{in} and V_{out} changing. The dotted lines represent the ideal T_{off} curves for various output voltage conditions from (4.5). The simulated T_{off} curves matched well with them and were roughly constant. A low power consumption less than 18 μW was achieved, as shown in Fig. 4.10(b). Fig. 4.10(c) plots the simulated T_{off} with a changing V_{out} and the digital code C_{ctrl} [6:0] from 0 to 127. Each T_{off} curve in

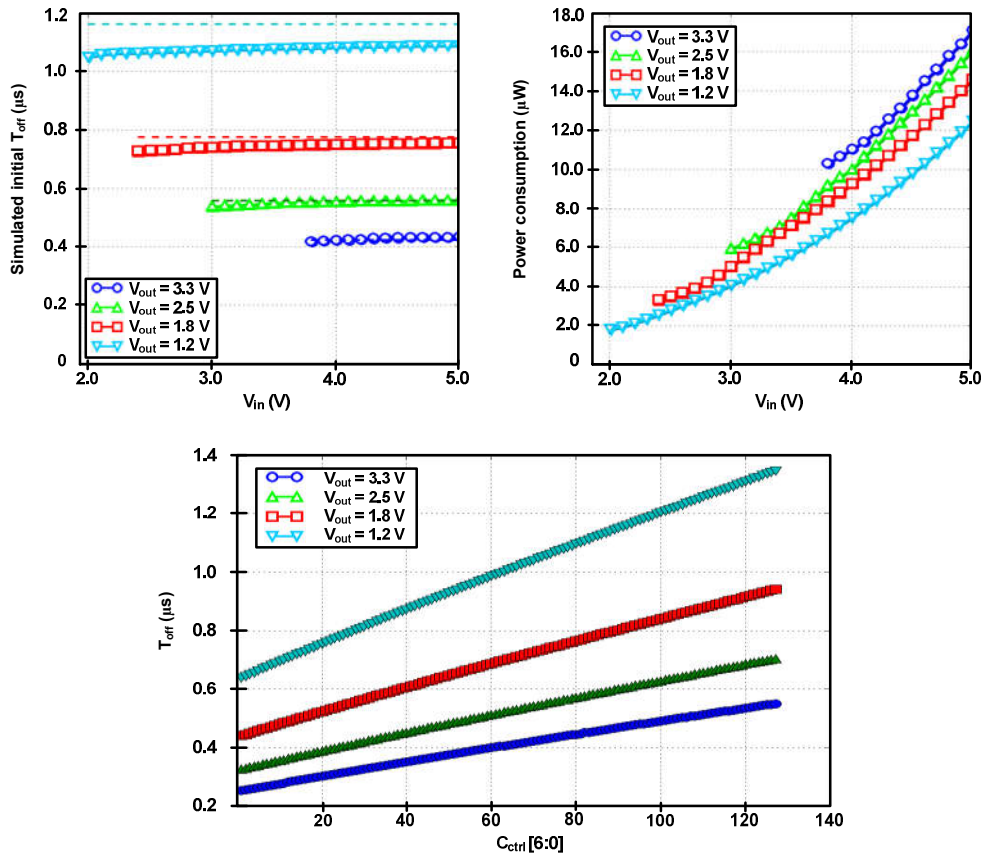


Fig. 4.10 Simulation results of the AOT pulse generator: (a) the simulated initial T_{off}, (b) its power consumption for various V_{in} and V_{out} conditions, and (c) the simulated T_{off} with a changing digital code C_{ctrl} [6:0].

creased linearly according to the digital code, where the slope represents the unit step size of the timing calibration. For instance, when V_{out} was 3.3 V, the minimum and maximum T_{off} were 0.25 µs at C_{ctrl} = 0 and 0.55 µs at C_{ctrl} = 127, respectively, and hence the step size was approximately 2.3 ns. Considering that the required T_{off} at 3.3 V V_{out} was approximately 420 ns, within 0.6% timing error can be achieved after the timing calibration. In addition, each resolution at V_{out} = 1.2 V, 1.8 V and 2.5

V was 5.5 ns, 3.9 ns and 2.9 ns, respectively. Despite such a fine resolution, the proposed AOP-ZCD can compensate for the initial timing error quickly thanks to the adaptive setting of initial T_{off} close to the accurate ZCS timing.

4.3.2 Timing Error Detector and Shift-Register

The timing error detector was implemented by using a clocked comparator and an auxiliary switch M_L, which determines whether to increase or decrease the ca-

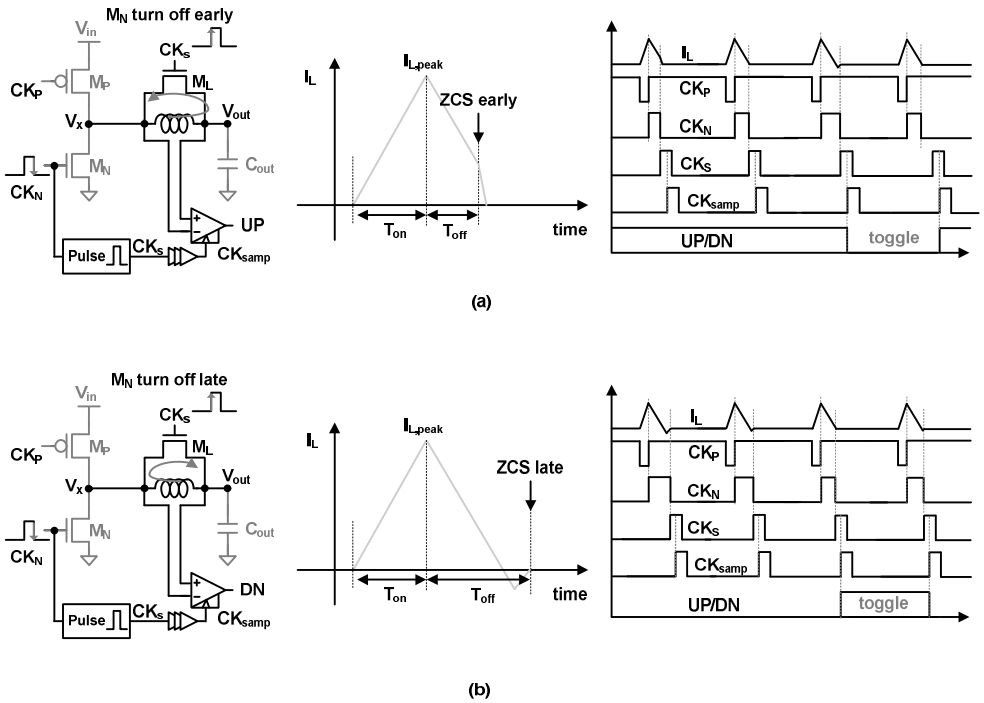


Fig. 4.11 Timing error detector and the timing calibration waveforms when (a) M_N turns off early (i.e., ZCS-early case) and (b) M_N turns off late (i.e., ZCS-late case).

pacitance value of C_{off} by sampling the inductor current direction [2] as shown in Fig. 4.11. At the negative edge of CK_N, M_N turns off, and simultaneously the positive edge of CK_S is generated, which turns on M_L. While both M_P and M_N are turned off, the inductor current flows through M_L. If M_N turns off early (i.e., ZCS-early case) as

shown in see Fig. 4.11(a), the positive inductor current flows through M_L, which makes V_{out} higher than V_x. On the other hands, if M_N turns off late (i.e., ZCS-late case) as shown in see Fig. 4.11(b), the negative inductor current flows through M_L, which makes V_{out} lower than V_x. The polarity of the voltage difference between V_{out} and V_x that represents the inductor current direction is sampled by the clocked comparator, which produces the 1-bit *UP*/*DN* signal.

The shift-register was digitally implemented with the 7-bit counter. For every switching cycle, the shift-register increments or decrements 1-bit based on the sampled result *UP*/*DN*. Eventually, the digital code C_{ctrl} [6:0] is converged to the appropriate value that corrects the timing error. Note that since the timing calibration loop operates in a bang-bang control mode, the *UP*/*DN* signal toggles in locking state.

Chapter 5

Measurement Results of Proposed Buck Converter

To demonstrate the proposed design concepts, a prototype buck converter IC was fabricated in 250-nm high-voltage (HV) CMOS technology. The die photograph of the proposed buck converter is shown in Fig. 5.1. The entire system occupied an effective area of 1.2 mm^2 including the power switches (M_P and M_N) and control circuits. The prototype IC was measured with an off-chip 10-µH inductor (L) and a 2.2-µF output capacitor (C_{out}). In this chapter, the measurement results will be shown and discussed.

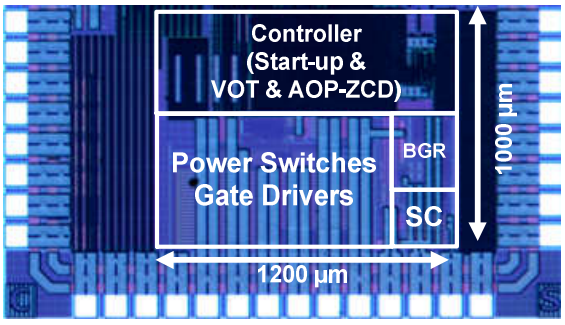


Fig. 5.1 Die photograph.

5.1 Measurement Results of Switching-Based Stepwise Capacitor Charger

The switching-based stepwise C_{out} charging scheme was measured with the various setting N_{th} in the DCC, which can control the charging time T_{ch}. This is because the charging time directly affects the losses incurred during start-up operation such as conduction and switching losses as discussed in subsection 3.3.3.

Fig. 5.2 plots the measured start-up energy loss (i.e., $E_{loss,st} + E_{loss,Cout}$) in change with T_{ch}, demonstrating the energy loss reduction in the proposed switching-based stepwise charging method. When charging 2.2-μF C_{out}, the optimal T_{ch} was 0.12 ms, at which the minimum energy loss of 9.4 μJ can be achieved. If T_{ch} is smaller than 0.12 ms, the average inductor current increases, which incurs a large conduction energy loss. If T_{ch} is larger than 0.12 ms, the number of switching cycle increases, which incurs a large switching energy loss. From the energy loss curve, it is more sensitive to the conduction energy loss. Considering that the required energy to charge 2.2-μF C_{out} to 2.5 V_{out} is 6.9 μJ, the energy loss incurred at the buck converter is only 2.5 μJ. In the same way, when charging 4.7-μF C_{out}, the optimal T_{ch} was 0.2 ms, at which the minimum energy loss of 22 μJ can be achieved. Considering that the required energy to charge 4.7-μF C_{out} to 2.5 V_{out} is 14.7 μJ, the energy loss incurred at the buck converter is only 7.3 μJ. Note that a small C_{out} of 2.2 μF can be used in this work thanks to the VOT pulse generator as described in subsection 3.2.3.

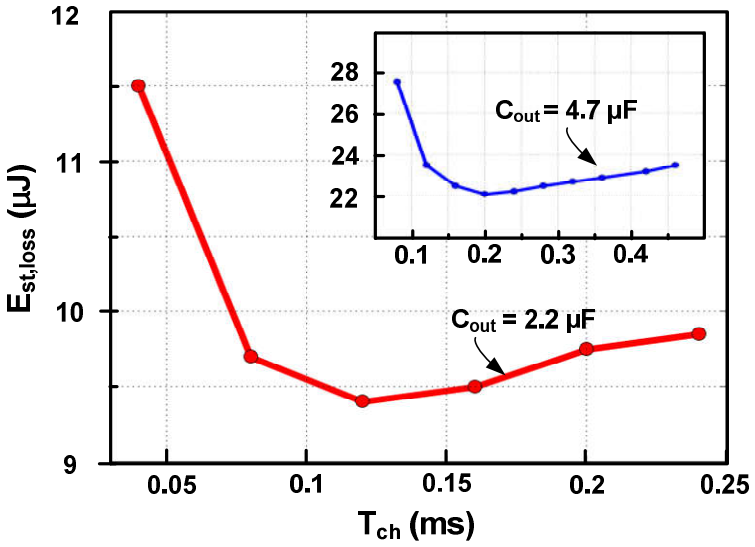


Fig. 5.2 Measured start-up energy loss in change with T_{ch}. when charging 2.2-μF C_{out} and 4.7-μF C_{out}.

Fig. 5.3 the measured key waveforms during the start-up operation, showing that the constant average inductor current charges 2.2-μF C_{out} in a stepwise fashion. The duty-cycle ratios of the switching signals CK_P and CK_N were gradually modulated to charge the capacitor to 2.5 V V_{out} in a linear and stepwise manner. By switching the buck converter at a high frequency of 1.6 MHz, the average inductor current was held constant during the charging time T_{ch}. At first, the inductor current was slightly higher than the average value of i_{avg}, because the initial value of the duty-cycle ratio was not zero. When V_{out} was matched with its corresponding duty-cycle ratio, the average inductor current maintained a constant value of 50 mA. After V_{out} reached

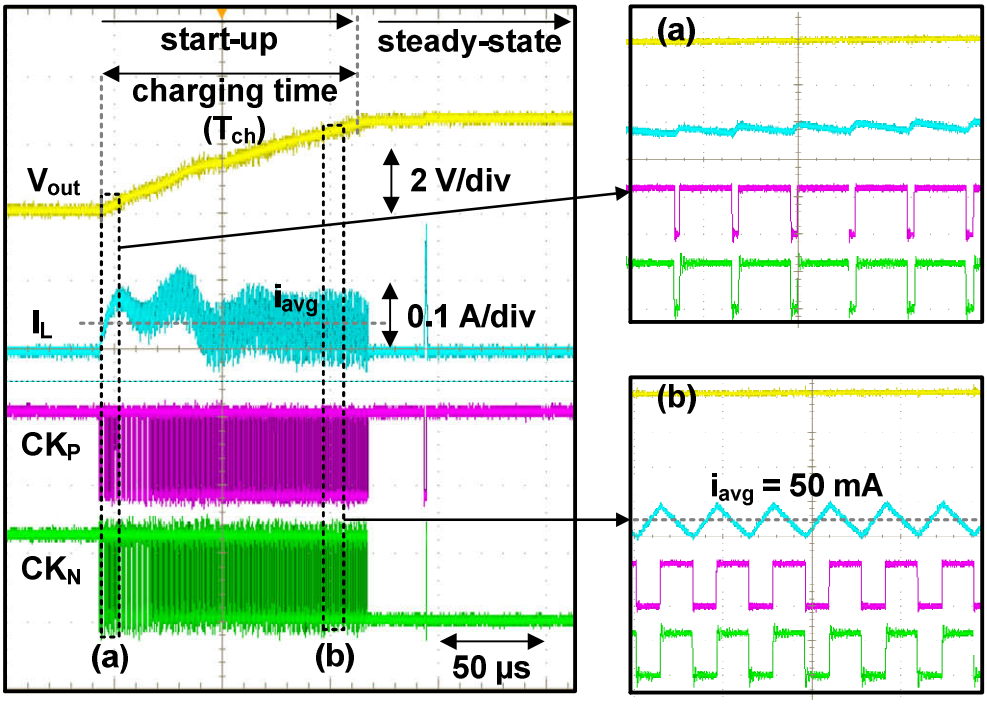


Fig. 5.3 Measured key waveforms during start-up operation.

the target output voltage of 2.5 V, the start-up circuits were disabled, and the buck converter began to operate in PFM mode.

5.2 Measurement Results of Steady-State Performance with VOT Pulse Generator and AOP-ZCD

The steady-state performance of the proposed buck converter was measured with various input and output voltages to demonstrate that the variable on-time (VOT) pulse generator can keep the inductor peak current constant and the adaptive off-time positioning ZCD (AOP-ZCD) can turn off the low-side switch when the inductor current becomes zero by predicting it, regardless of change in operating voltage conditions. The prototype buck converter IC was measured at input and output voltages ranging 2.5−5.0 V and 1.2−3.3 V, respectively.

Fig. 5.4 plots the measured on-time (T_{on}) of the VOT pulse generator over wide ranges of input and output voltage conditions. While the dotted lines represent the theoretical on-time curve from (4.4) that can maintain the inductor peak current constant, the measured points were well matched to them. In other words, the measured on-times are inversely proportional to the voltage difference between input and output voltage. To demonstrate the constant peak inductor current, the measured waveforms are shown in Fig. 5.5 by varying the input voltage from 3.5 V to 5.0 V at 2.5 V V_{out}. This figure shows that the peak inductor current can be kept constant at 140 mA by adaptively varying on-time from 1.3 μs to 0.5 μs.

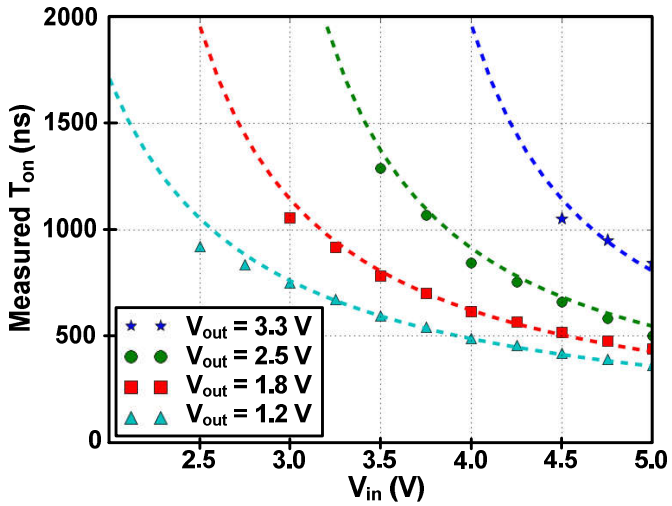


Fig. 5.4 Measurement of the generated on-time (T_{on}) from the variable on-time pulse generator over wide ranges of input and output voltage conditions.

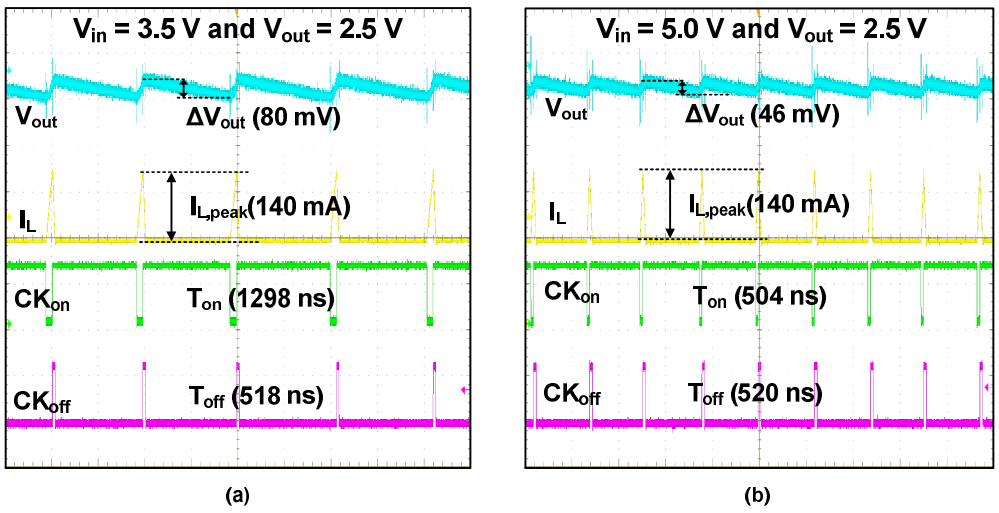


Fig. 5.5 Measured waveforms at difference input voltages (V_{in} = 3.5V, 5V) and at 2.5 V V_{out}.

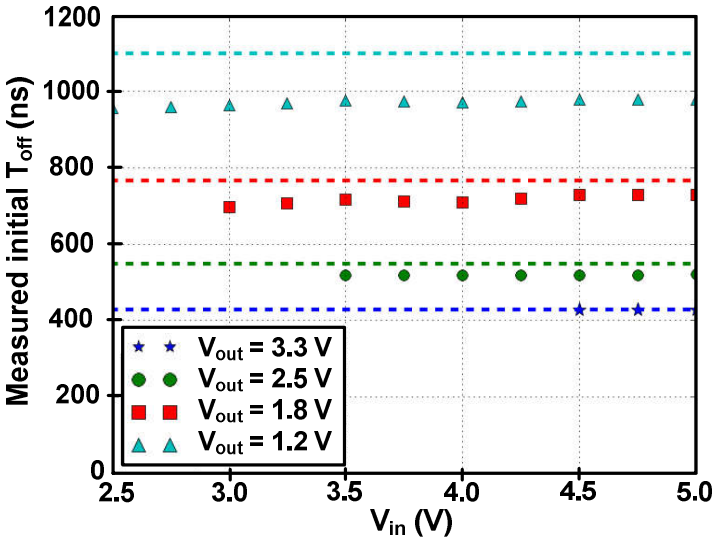


Fig. 5.6 Measurement of the generated off-time (T_{off}) from the adaptive off-time pulse generator over wide ranges of input and output voltage conditions.

Fig. 5.6 plots the measured off-time (T_{off}) of the AOT pulse generator over wide ranges of input and output voltage conditions. While the dotted lines represent the theoretical off-time curve for ZCS operation from (4.5), the measured points were well matched to them. Since the off-time is solely determined by V_{out} while the peak inductor current is maintained at a constant value, the measured off-time at each V_{out} case is a constant value. However, the measured points are slightly smaller than the theoretical values. In practice, the initial value of C_{off} in Fig. 4.9 was intentionally designed to be slightly smaller than 7 pF to avoid significant power loss from the reverse inductor current when M_N turn off late. As shown in Fig. 5.5, the T_{off} values are same at 0.5 μs regardless of change in V_{in}, showing the adaptive off-time positioning.

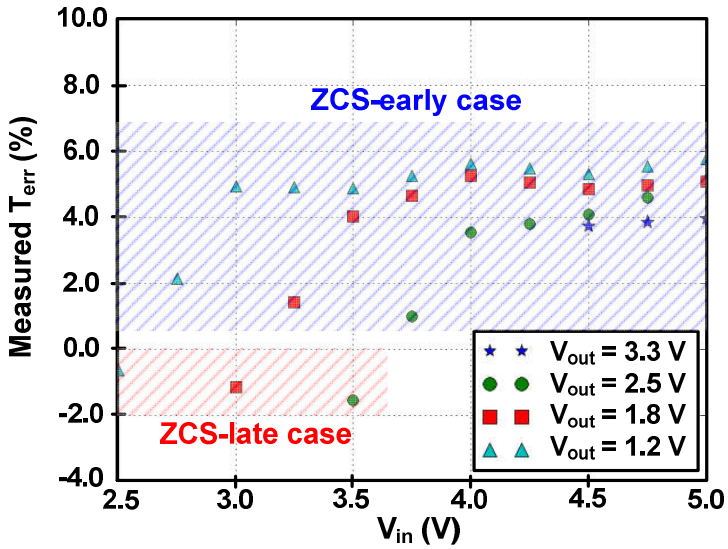


Fig. 5.7 Measured timing error (T_{err}) over wide ranges of input and output voltage conditions.

Fig. 5.7 plots the measured initial timing error (T_{err}) before timing calibration over wide ranges of input and output voltage conditions. The timing error can be expressed with the measured T_{off} before and after T_{err} calibration (i.e., T_{off_before} and T_{off_after}), respectively:

$$T_{err}(\%) = \frac{T_{off\_after} - T_{off\_before}}{T_{off\_before}} \cdot 100 \tag{5.1}$$

The positive and negative values of T_{err} represent the ZCS-early and ZCS-late cases, respectively. For various V_{in} and V_{out} values, the measured T_{err} (%) was always small value in the range of −2.0% to 6.0%. the worst-case T_{err} (%) in each case was 6% at V_{in} =5 V and V_{out} = 1.2 V and −2% at V_{in} =3.5 V and V_{out} = 2.5 V, respectively.

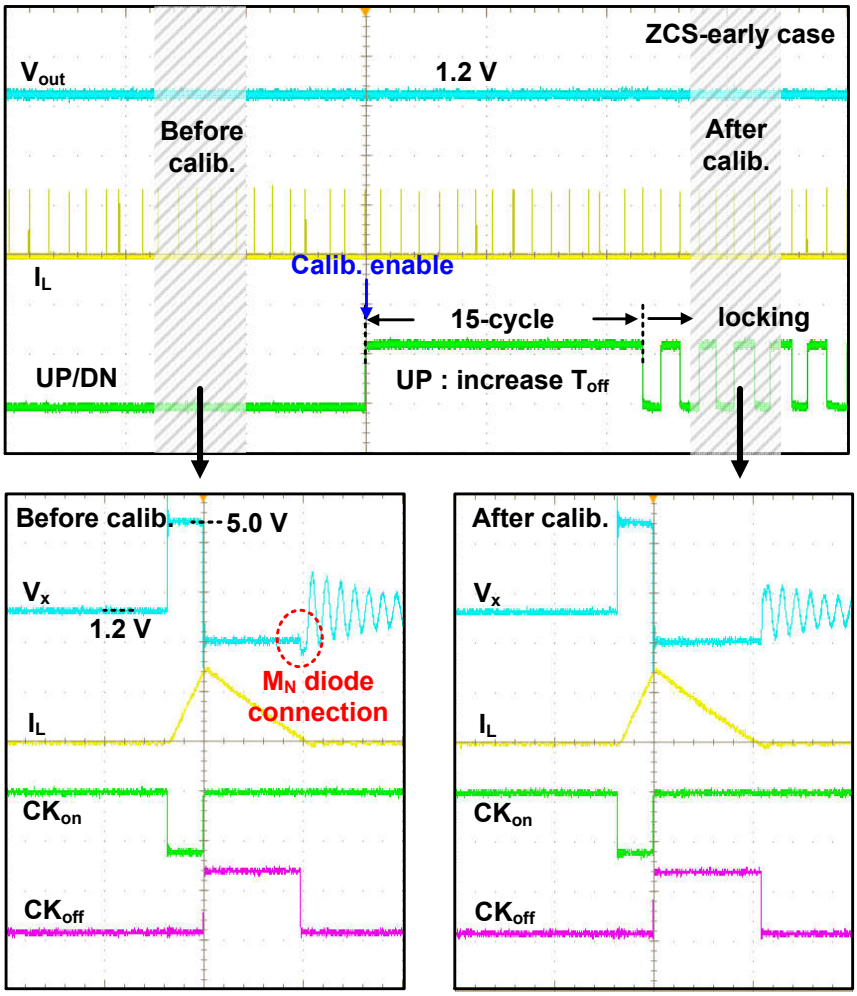


Fig. 5.8 Measured transient waveforms of T_{err} compensation for the worst ZCS-early case when converting 5.0 V to 1.2 V.

Fig. 5.8 and 5.9 show the transient waveforms of the T_{err} calibration at the worst ZCS-early and ZCS-late cases, demonstrating that the proposed AOP-ZCD can achieve the fast convergence time even with high resolution. Before calibration in the ZCS-early case (see Fig. 5.8), when both the high-side and low-side power

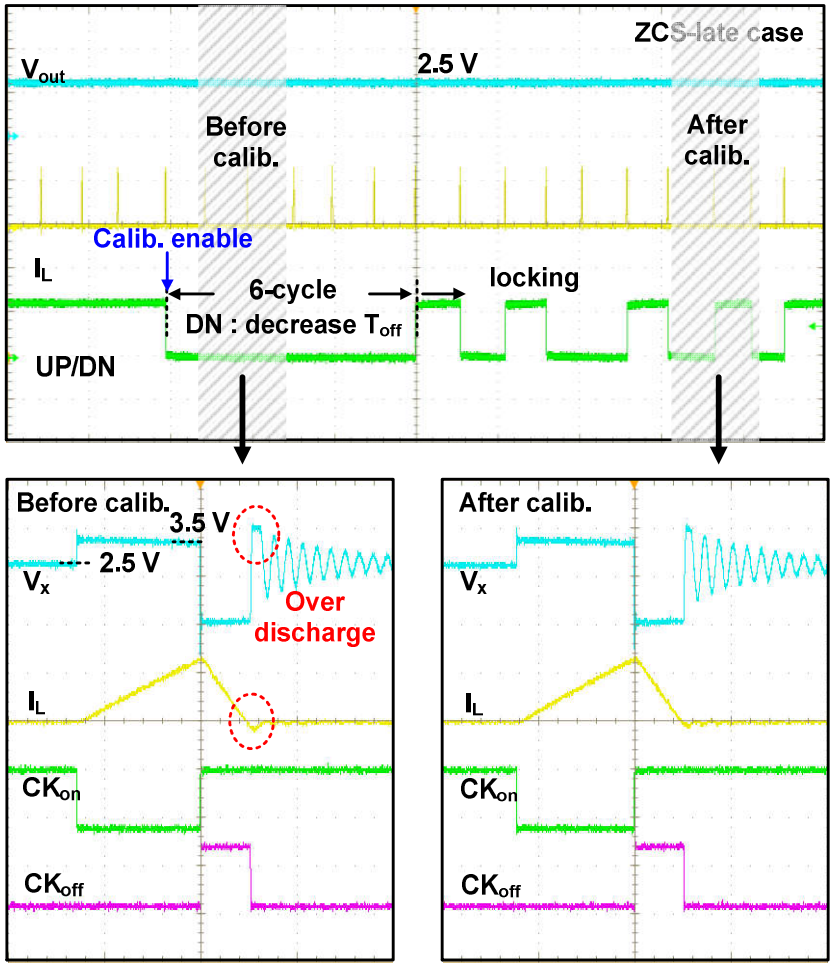


Fig. 5.9 Measured transient waveforms of T_{err} compensation for the worst ZCS-late case when converting 3.5 V to 2.5 V.

switches M_P and M_N were turned off, the positive inductor current flowed through the body diode of M_N that incurred the loss. To compensate for this T_{err}, the clocked comparator produced the *UP* signal to increase T_{off} over 15 switching cycles with 4.4 ns resolution. After calibration, M_N turned off at the right timing that eliminates its

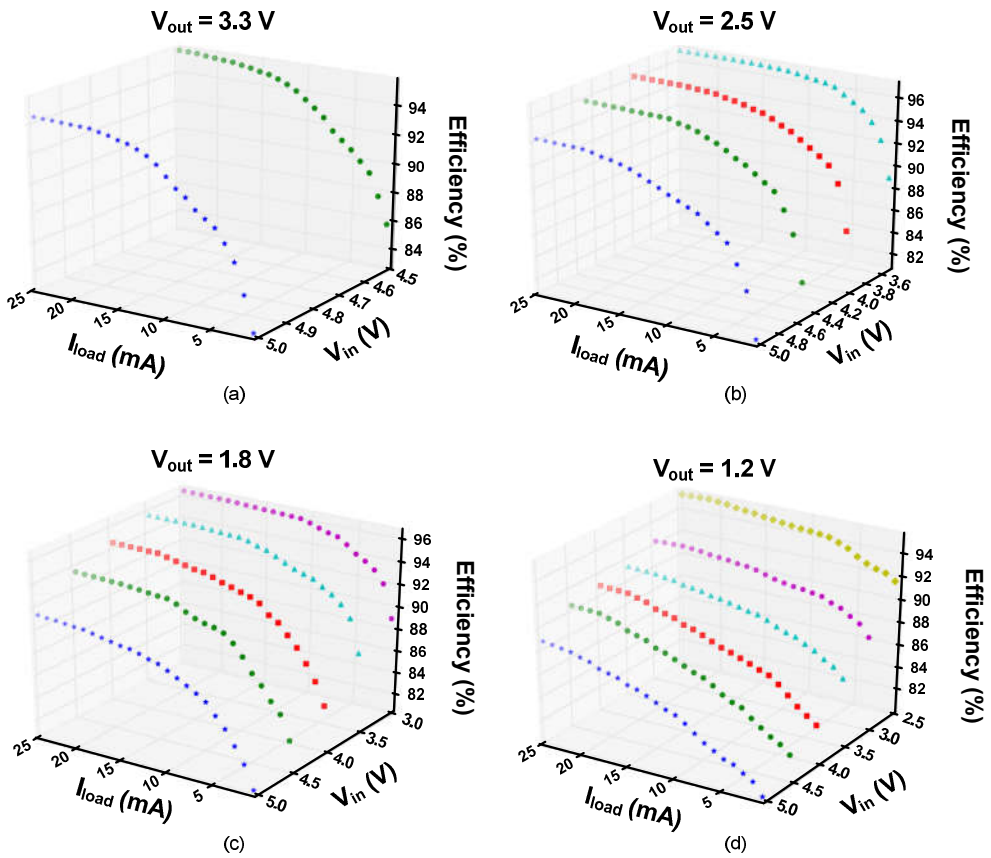


Fig. 5.10 Measured power efficiency at the steady state for various load currents I_{load}, V_{in}, and V_{out}: (a) V_{out} = 3.3 V, (b) V_{out} = 2.5 V, (c) V_{out} = 1.8 V, (d) V_{out} = 1.2 V.

body diode conduction. When the calibration ended, the binary signal *UP*/*DN* toggled repeatedly. Before calibration in the ZCS-late case (see Fig. 5.9), the negative inductor current incurred the power loss. To compensate for this T_{err}, the clocked comparator produced the *DN* signal to decrease T_{off} over six switching cycles with 2 ns resolution. After calibration, M_N turned off at the right timing that eliminates the flow of a reverse current.

Fig. 5.10 plots the measured power efficiencies, showing that the designed DCM buck converter achieves the high efficiencies over wide ranges of input voltage and output voltage conditions. While the PFM control has the advantage of reducing the switching power loss by dynamically adjusting the switching frequency according to I_{load}, the proposed AOP-ZCD can further enhance the power efficiency. Compared to the power consumption of continuous-time ZCDs (i.e., ~100 μW [4]), the proposed AOP-ZCD dra matically reduced the power consumption and dissipates only 1–18 μW. In addition, compared to previous sampling-based ZCDs, the AOP-ZCD achieved high power efficiencies for various V_{in} and V_{out} values. The prototype buck converter IC achieved a 96% peak efficiency at I_{load} = 25 mA, V_{in} = 3.5 V, and V_{out} =

TABLE 5.1

PERFORMANCE COMPARISON WITH PRIOR WORKS

	Yang [4]	Wu [11]	Chen [2]	This work
Technology	0.25-μm CMOS technology	0.18-μm CMOS technology	0.18-μm CMOS technology	0.25-μm CMOS technology
Operating mode	DCM (PFM)	DCM (PFM)	AM/DCM/CCM	DCM (PFM)
Input voltage (V_{in})	3.0–5.0 V	0.22–1.3 V	0.55–1.0 V	2.5–5.0 V
Output voltage (V_{out})	2.5 V	1.8 V	0.35–0.5 V	1.2–3.3 V
External inductor (L)	10 μH	4.7 μH	4.7 μH	10 μH
External capacitor (C_{out})	2.2 μF	N/A	4.7 μF	2.2 μF
ZCD type	Continuous time	Continuous time	Sampling-based	Sampling-based
I_{load}	1–25 mA	1–50 mA	100 nA–20 mA	1–25 mA
Peak efficiency	92 % @ I_{load} = 25 mA	90.6 % @ I_{load} = 50 mA	92 % @ I_{load} = 6 mA	96 % @ I_{load} = 25 mA
Efficiency @ 1 mA I_{load}	73.2 %	N/A	81 %	88 %
EEF @ 1 mA I_{load}	2.4 %	N/A	14.5 %	18.8 %

2.5 V and more than 80% at the 1–25 mA load condition.

Table I compares the performance with that of recently presented DCM converters. Although the previous works achieved high peak power efficiencies of over 90% at each optimal condition, their results were measured under their maximum load condition, at which the effect of efficiency degradation due to the controller power loss is relatively small. Therefore, we compare the power efficiencies at more light load condition (e.g., 1 mA I_{load}). In addition, we benchmarked an efficiency enhancement factor (EEF) [19] that represents the power efficiency benefit of a buck converter over that of a linear regulator for fair comparison because their input and output voltages are different each other. This is expressed below:

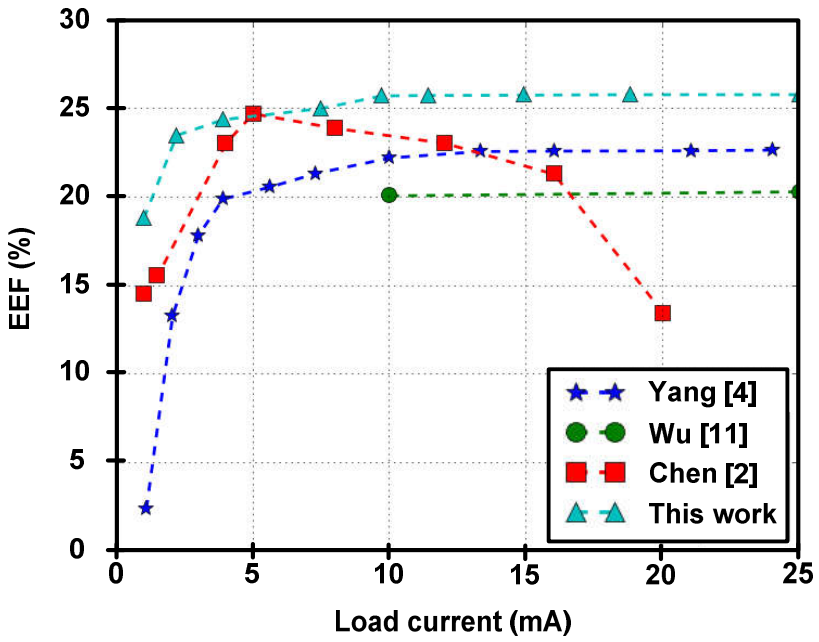


Fig. 5.11 Efficiency Enhancement Factor (EEF) comparison.

$$EEF = 1 - \frac{\eta_{lin}}{\eta_{buck}}\Bigg|_{k_{buck}} \tag{5.2}$$

where η_{buck} and η_{lin} are the power efficiencies of the buck converter and the ideal linear regulator, respectively, at the same voltage conversion ratio k_{buck}. Fig. 16 plots the comparison of the EEF. Because the continuous-time ZCD [3] has high power consumption, EEF was the lowest among them at 1 mA I_{load}. On the other hands, the Ref. [2] that used the sampling-based ZCD can achieve a higher EEF value of 14.5 % at 1 mA I_{load}. Our buck converter exhibited the highest EEF among them (i.e., EEF = 18.8% at 1 mA I_{load} and 25.8 % at 25mA I_{load} when converting 3.5 V to 2.5 V).

Chapter 6

Realization of Battery-free Wireless Remote Switch

In this chapter, the realization of battery-free wireless remote switch (BWS), which is a wireless remote controller that can operate without batteries [26]–[29], is presented. Such BWSs reduce the need to install wiring within buildings, or reduce the costs of periodically recharging or replacing batteries. To supply the energy instead of battery, a disc-type piezoelectric (PE) transducer is used that can generate the energy from the button-pressing actions of users. Especially, the energy benefit will be highlighted when the proposed buck converter applied to the BWS, which is demonstrated by the measurement results.

6.1 Key Building Blocks of Battery-free Wireless Remote Switch

Basically, the key building blocks consisting the battery-free wireless switch (BWS) are a piezoelectric (PE) device, an energy harvester, a voltage regulator and a RF transmitter as illustrated in Fig. 6.1. When a disc-type PE source [5] is pressed, it generates the electrical energy in a form of bipolar current I_{PZ}. The energy harvester, which includes a rectifier circuit, collects this energy in storage capacitor C_{in}. Next, the buck converter begins charging output capacitor C_{out} to the desired output voltage V_{out} using the energy stored in C_{in} (i.e, start-up), and then delivers this energy to the load at a steady V_{out}. To demonstrate the energy benefits when applying the proposed buck converter, a piezoelectric-based power management solution for BWS was realized by using a 300-mm^2 lead magnesium niobate-lead titanate (PMN-PT) piezoelectric disc and a 2.4-GHz WirelessUSB RF transceiver (CYRF8935) that transmits a 4-byte message to control a target device (e.g., lighting).

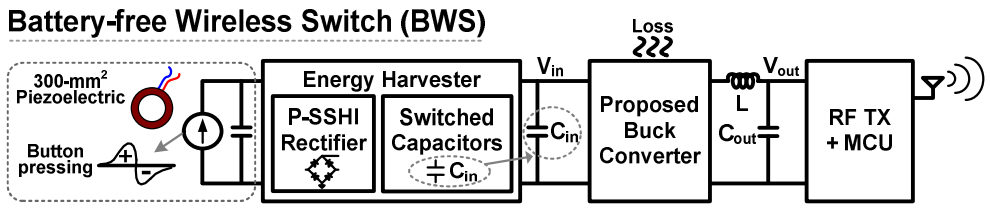


Fig. 6.1 Key building blocks of the battery-free wireless remote switch (BWS).

6.2 Piezoelectric Energy Harvester with P-SSHI Rectifier

While various rectifier circuits as a piezoelectric energy harvester have previously been reported in literature [32]–[35], a rectifier based on synchronized switch harvesting on inductor (SSHI) technique is employed to maximize the amount of energy harvested. Specifically, the rectifier with a switch S_1 and an inductor L_H, called P-SSHI rectifier [32]–[33], is used to minimize a C_{PZ} discharging loss when the AC current I_{PZ} is inverted from positive to negative [32]. To rectify the single-pulsed AC current I_{PZ}, the FBR is required (see Fig. 6.2 (a)); however, this incurs a large loss at C_{PZ} when I_{PZ} changes in polarity. This is because the negative I_{PZ} is not

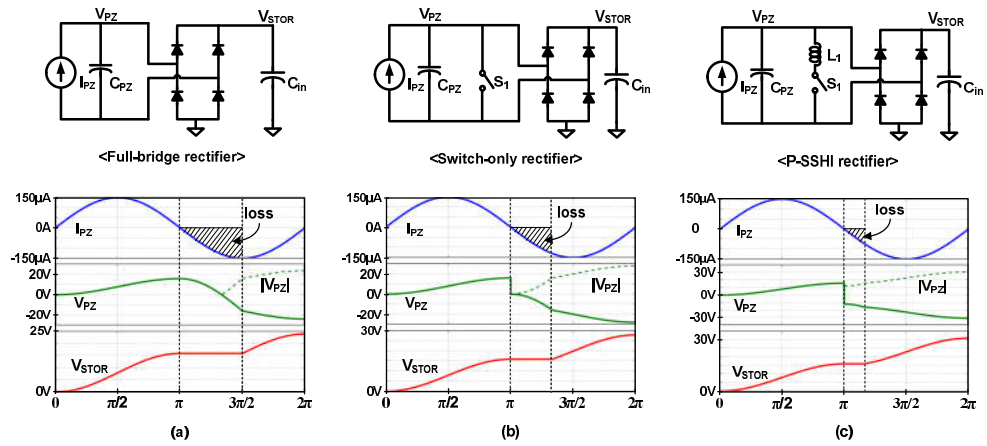


Fig. 6.2 Three examples of piezoelectric energy-harvesting circuits and their key waveforms: (a) FBR, (b) switch-only rectifier (SOR), and (c) P-SSHI rectifier.

used for charging C_{in}, but for discharging the remaining charge in C_{PZ} instead. To minimize this loss, the switch-only rectifier (SOR) [30] that discharges V_{PZ} to ground by switch S_1 (see Fig. 6.2 (b)) and the P-SSHIR that flips V_{PZ} to a negative voltage using an inductor (L_H) (see Fig. 6.2 (c)) are both good candidate circuits to reduce this energy loss.

6.2.1 Analysis on Single-Pulsed Energy Harvesting

In this subsection, we derive the optimal conditions for the energy harvester that are required to harvest the maximum amount of energy from the single-pulsed energy that arrives from the PE source pressed by a user. All three rectifier topologies presented in Fig. 6.2 can be analyzed simultaneously by assuming the presence of an arbitrary voltage changer, as shown in Fig. 6.3. That is, this arbitrary voltage changer can change the voltage V_{PZ} across C_{PZ} when the polarity of I_{PZ} is inverted as:

$$V_{PZ}(t+) = \gamma \cdot V_{PZ}(t-) \tag{6.1}$$

where $t-$ and $t+$ represent the times before and after I_{PZ} is inverted, respectively, and γ is the "flipping coefficient" ($-1 \leq \gamma \leq 1$). For instance, the FBR case has a γ value of 1 because this topology does not have any additional circuit to change V_{PZ}. In the SOR case, $\gamma = 0$ because V_{PZ} is connected to ground through a switch. In the P-SSHIR case, $\gamma = -1$ because an ideal L_H–C_{PZ} resonance circuit can invert V_{PZ} to $-V_{PZ}$.

By using this general rectifier topology, we can derive the total harvested energy when only a single pulse of energy is available. In this analysis, the initial voltage of both capacitors C_{PZ} and C_{in} is assumed to be zero. In addition, the sinusoidal current

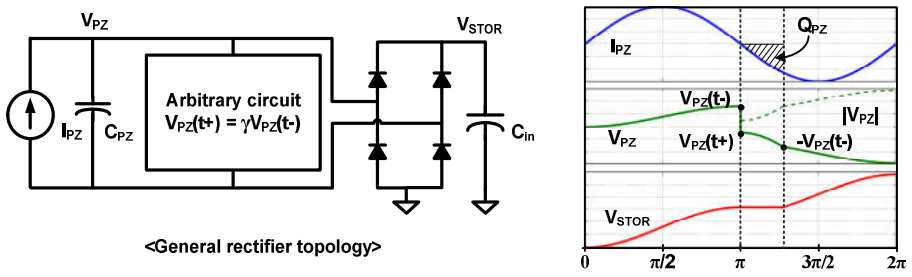


Fig. 6.3 General rectifier topology with an arbitrary voltage changer.

I_{PZ} is assumed to be $I_{PZ}(t) = I_{PZ} \sin\omega t$ for time T, where $\omega = 2\pi/T$ and T is the period in which the PE source is excited. Note that the actual I_{PZ} waveform is not perfectly sinusoidal (the measured waveform will be presented in section 6.3), but is assumed to derive and compare the harvested energy according to the values of γ and C_{in}. During the first-half period, the positive I_{PZ} charges both C_{PZ} and C_{in}; hence, the accumulated voltage $V_{PZ}(t-)$ can be expressed as:

$$V_{PZ}(t-) = \frac{\int_0^{T/2} (I_{PZ} \sin\omega t)dt}{C_{PZ} + C_{in}} = \frac{2I_{PZ}}{\omega(C_{PZ} + C_{in})} \tag{6.2}$$

When I_{PZ} begins to change in polarity, the arbitrary voltage changer changes V_{PZ} as:

$$V_{PZ}(t+) = \gamma V_{PZ}(t-) = \frac{2\gamma I_{PZ}}{\omega(C_{PZ} + C_{in})}, \text{ where } -1 \le \gamma \le 1 \tag{6.3}$$

If $V_{PZ}(t-)$ is not perfectly inverted to $-V_{PZ}(t-)$ (i.e., $\gamma \neq -1$), then I_{PZ} starts to discharge C_{PZ} alone until $V_{PZ}(t+)$ reaches $-V_{PZ}(t-)$, while the voltage across C_S is maintained at $V_{PZ}(t-)$. The amount of charge Q_{PZ} required to discharge C_{PZ} to $-V_{PZ}(t-)$ can be calculated as:

$$Q_{PZ} = C_{PZ}(V_{PZ}(t+) - (-V_{PZ}(t-))) = \frac{2(1+\gamma)I_{PZ}C_{PZ}}{\omega(C_{PZ} + C_{in})} \tag{6.4}$$

After C_{PZ} is discharged to $-V_{PZ}(t-)$, the other pair of diodes in the rectifier turn on and then I_{PZ} resumes charging both C_{PZ} and C_{in} again. When charging is completed, the final voltage of V_{STOR} across C_{in} can be calculated as:

$$V_{STOR} = V_{PZ}(t-) + \frac{\int_{T/2}^{T} |I_{PZ}(t)|\,dt - Q_{PZ}}{C_{PZ} + C_{in}} = \frac{2I_{PZ}((1-\gamma)C_{PZ} + 2C_{in})}{\omega(C_{PZ} + C_{in})^2} \tag{6.5}$$

A general expression for the total harvested energy E_{STOR} stored in C_{PZ} and C_{in} from a single pulse of energy can be derived as a function of C_{in}/C_{PZ} in (6.6).

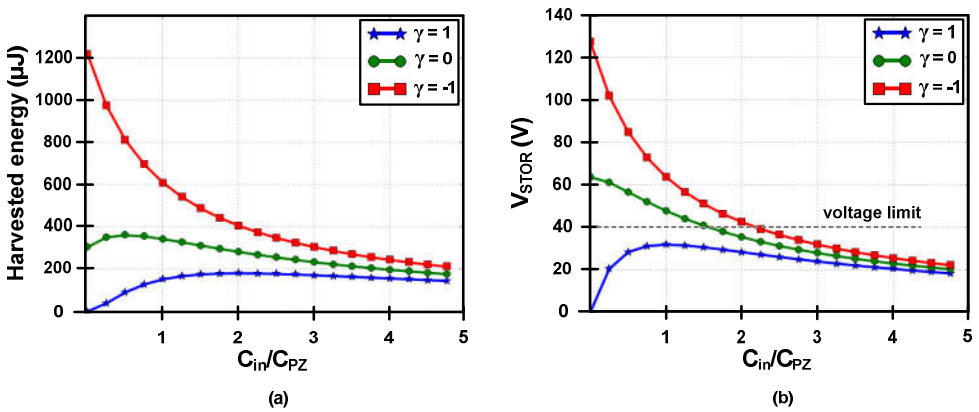


Fig. 6.4 (a) Theoretical harvesting energy, and (b) post-harvesting-voltage V_{STOR} according to the value of flipping coefficient (γ) and the capacitor ratio C_{in}/C_{PZ} of example topologies of an FBR ($\gamma = 1$), SOR ($\gamma = 0$), P-SSHIR ($\gamma = -1$).

$$E_{STOR} = \frac{1}{2}(C_{PZ} + C_{in})V_{STOR}^{\ 2} = \frac{2I_{PZ}^{\ 2}}{\omega^2 C_{PZ}} \frac{(1-\gamma+2C_{in}/C_{PZ})^2}{(1+C_{in}/C_{PZ})^3} \tag{6.6}$$

Fig. 6.4 (a) plots E_{STOR} versus γ and C_{in}/C_{PZ} with a disc-type 300-mm^2 PE source that has an internal capacitance C_{PZ} of 150 nF and a peak current I_{PZ} of 150 μA. Theoretically, the maximum achievable energies are approximately 180 μJ at $C_{in} = 2C_{PZ}$ in the FBR ($\gamma = 1$) case, 360 μJ at $C_{in} = 0.5C_{PZ}$ in the SOR ($\gamma = 0$) case and 1200 μJ at $C_{in} = 0$ in the P-SSHIR ($\gamma = -1$) case, respectively. However, each optimal loading produces an excessively high voltage, while the allowable voltage limit is 40 V in the given CMOS process. For instance, the final voltages in both the SOR and P-SSHIR cases are approximately 56 V and 128 V, respectively (see Fig. 6.4 (b)). While the P-SSHIR can harvest the highest energy among these three circuits, we use $C_{in} = 2.4C_{PZ}$ while considering the acceptable voltage range, and the maximum theoretical energy is approximately 350 μJ.

6.2.2 Proposed Piezoelectric Energy Harvester

Although the aforementioned rectifier circuits can achieve the maximum energy harvested under each set of optimal conditions, the final voltage of V_{STOR} can be too high for the subsequent buck converter to use directly. This imposes a large burden on the subsequent buck converter, causing a high voltage conversion ratio, thereby reducing the energy delivery. However, if V_{STOR} is limited to a low voltage (e.g. 5 V) by using a large C_{in}, the amount of energy harvested is dramatically reduced.

To alleviate this tradeoff between maximum energy extracted and the final voltage, the proposed energy harvester employs a 6:1 series-parallel switched-capacitor (SC) converter with a P-SSHIR as shown in Fig. 6.5. At first, all of the switches are turned off, and the six capacitors C_{S1}–C_{S6} are initially aligned in series through diodes, which provides an effective capacitance of $C_S/6$ if it is assumed that all storage capacitors have the same value of C_S. When the PE button is pressed, the positive I_{PZ} begins charging both C_{PZ} and the series-connected C_{S1}–C_{S6} (see Fig. 6.5 (a)). When I_{PZ} is inverted, the switch S_I turns on to invert the voltage across C_{PZ} by forming the L_H–C_{PZ} resonant circuit (see Fig. 6.5 (b)). Then, the other pair of diodes in the rectifier turns on and the negative I_{PZ} resumes charging the capacitors (see Fig. 6.5 (c)). By activating the switches that re-align the storage capacitors in parallel, the 6:1 SC converter efficiently down-converts the resulting voltage V_{STOR} (see Fig. 6.5 (d)).

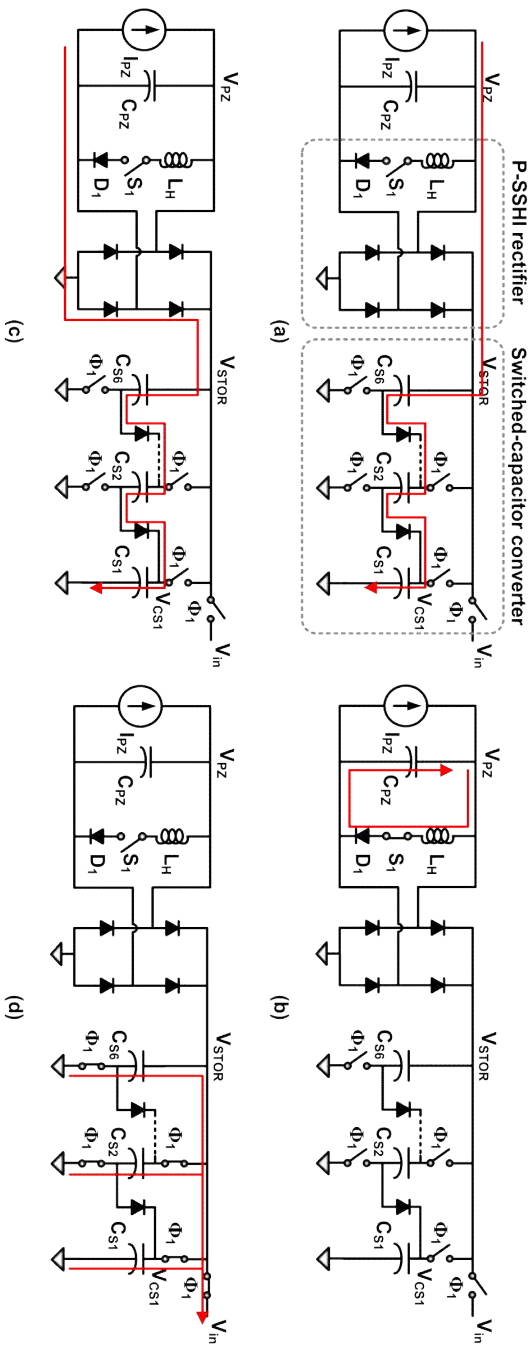


Fig. 6.5 Operation principle of the proposed energy harvester, combining a P-SSHIR and a 6:1 SC converter.

6.2.3 Circuit Implementation

All of the components for the energy harvesting circuit, including the switches and timing control circuit, are integrated into a single chip, except for the passive components, such as the inductor and storage capacitors. A detailed schematic of the circuit implementation is shown in Fig. 6.6. The circuit uses a 470-μH inductor for the P-SSHIR and six 2.2-μF capacitors for the 6:1 SC converter. To tolerate high source-to-drain voltages, which can typically exceed 30 V, all of the switches and diodes in the P-SSHIR and 6:1 SC converter circuits are designed using 40 V HV transistors, of which the gate-source voltage allows 5 V, and on-chip HV Schottky diodes. Pull-up resistors are used to protect each gate node in the HV-PMOS switch, and maintain the voltage difference between the gate and source at < 5 V when the HV-NMOS switch is turned on. A diode D_1 is in series with switch S_1 in order to prevent a subsequent flipping action. Since voltage flipping only occurs once due to the action of a single button-press, diode D_1 can replace the zero-current sensing circuit to turn off the switch S_1 in [6], thereby reducing the complexity of the design and saving energy. In addition, since the stored energy in the lowermost capacitor

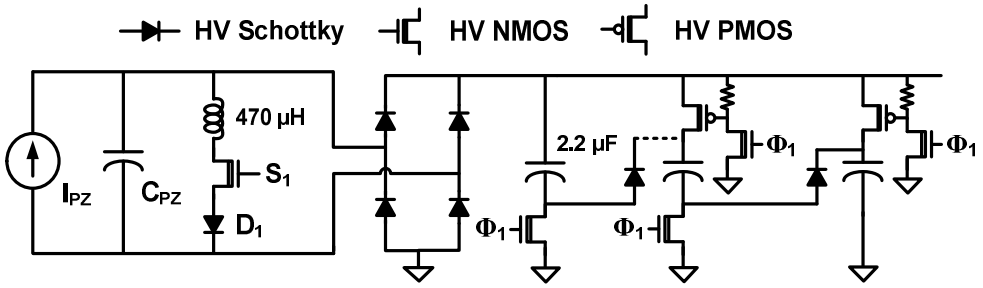


Fig. 6.6 Detailed circuit implementation of the proposed harvesting circuit.

C_{S1} in the SC converter is used as a power source for the control circuits, the control circuits are designed using 5 V transistors.

To activate S_1 and the parallel connection switches with each accurate timing, it is necessary to detect V_{CS1} across C_{S1}. The timing control circuit and the voltage waveform of V_{CS1} are depicted in Fig. 6.7. When the voltage V_{CS1} reaches 0.6 V under the positive I_{PZ}, the voltage detector VD_1 generates an enable signal *EN* that activates a comparator CMP and an oscillator OSC. When V_{CS1} peaks at the inversion of I_{PZ}, the sensing circuit monitors the first peak point of V_{CS1} and then generates S_1 by comparing V_{CS1} with the delayed version V_{del}. When V_{CS1} reaches 3.5 V under the negative I_{PZ}, the voltage detector VD_2 turns on CMP again. When V_{CS1} peaks after I_{PZ} has completed charging, the timing control circuit detects the second peak point of V_{CS1} and generates Φ_1. Note that the voltage detector circuit was described in subsection 4.1.1. To implement VD_1 and VD_2, one diode and six diodes are used, respectively.

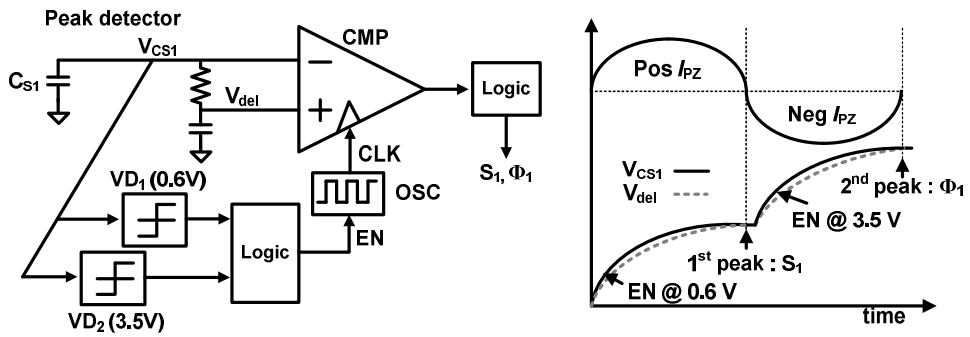


Fig. 6.7 Timing control circuit including a clocked comparator, an oscillator, and two voltage-level detectors.

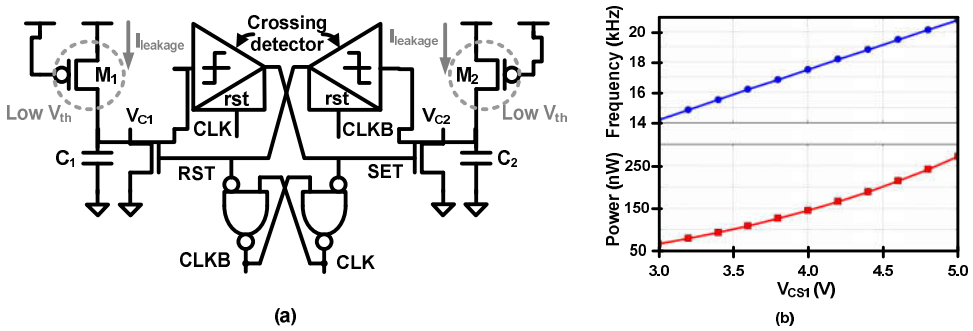


Fig. 6.8 (a) Schematic of ultra-low-power relaxation oscillator and (b) simulation result of frequency and power consumption.

Fig. 6.8 (a) illustrates the ultra-low-power relaxation OSC [38]. A leakage current source I_{leak} by M_1 and M_2 operating in the subthreshold region charges the on-chip capacitors C_1 and C_2 in an alternating fashion. Once I_{leak} charges C_1 to the threshold voltage V_{th}, the output of the corresponding crossing detector is set to a high value that resets C_2 to ground, and sets *CLK* and *CLKB* to high and low, respectively. In the same way, I_{leak} begins charging C_2 to V_{th}, which sets *CLKB* to high, and *CLK* to low. The period of *CLK* is set by the sum of the number of times needed to charge capacitors C_1 and C_2; hence, the frequency of *CLK* can be expressed as:

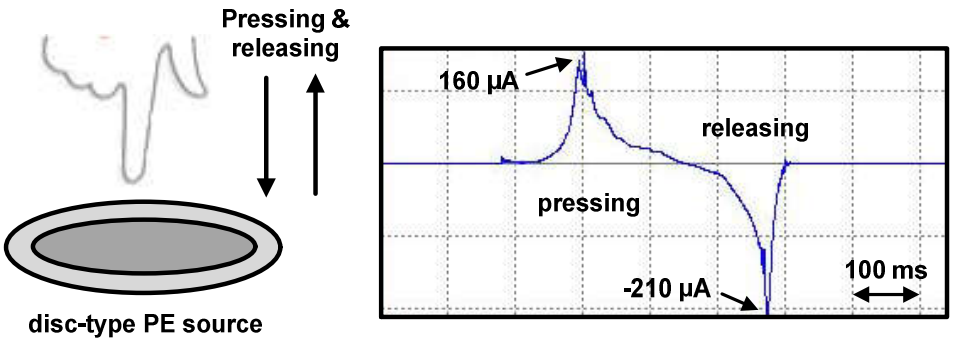
$$f_{sw} = \frac{I_{leak}}{2V_{th}C}, \text{ where } C_1 = C_2 = C \tag{6.6}$$

The simulation result in Fig. 6.8 (b) shows that the OSC can provide a 21-kHz clock signal with 270-nW power consumption at V_{CS1} = 5 V.

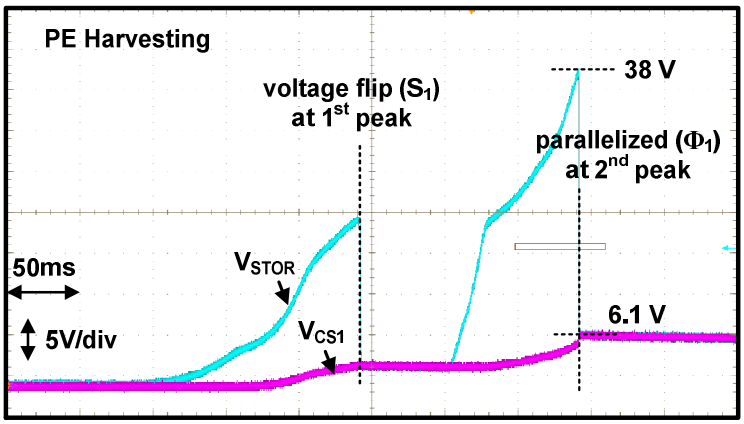
6.3 Measurement Results of Battery-free Wireless Switch

Fig. 6.9 (a) illustrates the disc-type piezoelectric source and shows the measured I_{PZ} when the 300-mm^2 PMN-PT piezoelectric (PE) disc button was pressed and released. In contrast to a stick-type PE source [6], the disc-type PE button does not output a decaying sinusoidal current because its movement is suppressed after the button is released. Since the pressing action is performed by a human, the length of time during which the PE source is excited can vary, and was in the range of approximately 300–400 ms. A bipolar AC current I_{PZ} was generated and the measured positive and negative peak values were 160 μA and -210 μA, respectively.

Fig. 6.9 (b) illustrates the measured voltage waveforms of V_{STOR} and V_{CS1} at the uppermost and lowermost capacitors in the 6:1 SC converter, respectively, showing the timing detections for harvesting the maximum amount of energy and the down-converted voltage of 6.1 V. The timing circuit of the PE harvester can detect the first and second peaks of V_{CS1} to invert the voltage across C_{PZ} to a negative value by S_1 and to parallelize the 6:1 SC converter by $\Phi 1$, respectively. When six 2.2-μF capacitors (C_{S1}–C_{S6}) are used, the PE harvester can charge the series-connected capacitors to 38 V and down-convert voltage to 6.1 V by changing its configuration in parallel, respectively. Since five HV Schottky diodes were required to connect the six storage capacitors in series, this caused an additional voltage drop of approximately 1.5 V, which then caused the down-converted voltage to be slightly smaller than V_{STOR}



(a)



(b)

Fig. 6.9 (a) Measured I_{PZ} when a 300-mm^2 PMN-PT piezoelectric disc button is pressed and released by a user, and (b) measured voltage waveforms.

divided by 6 (i.e. 6.3 V). The measured energy harvested was 246 μJ.

Fig. 6.10 shows the energy flows and losses while the buck converter delivers the energy stored in capacitor to the load. This figure compares the energy losses such as $E_{loss,st}$, $E_{loss,Cout}$ and $E_{loss,conv}$ of the proposed buck converter with those of the con

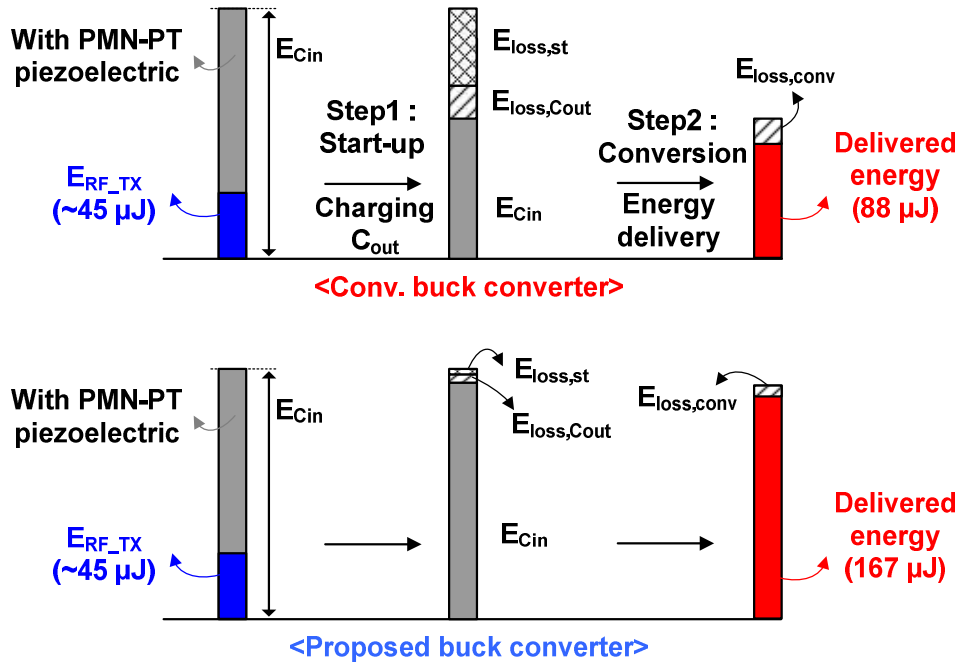


Fig. 6.10 Energy flows and losses during start-up and conversion operation of the (a) conventional and (b) proposed buck converter.

ventional buck converter to show the energy benefits of the proposed buck converter. The conventional one considered in this comparison uses a simple start-up switch ($M_{\text{start-up}}$) [3], [35] for start-up operation, and a constant on-time PFM control [2], [14] and a continuous-time analog ZCD for steady-state operation. Both buck converters can deliver the enough energy over 45 μJ to operate the RF transmitter. This is because the PMN-PT piezoelectric disc can generate a large energy, but it is costly. In addition, the proposed PE energy harvester can maximize the energy harvested of 246 μJ. However, the energy losses such as $E_{\text{loss,st}}$, $E_{\text{loss,cout}}$ and $E_{\text{loss,conv}}$ were 53 μJ,

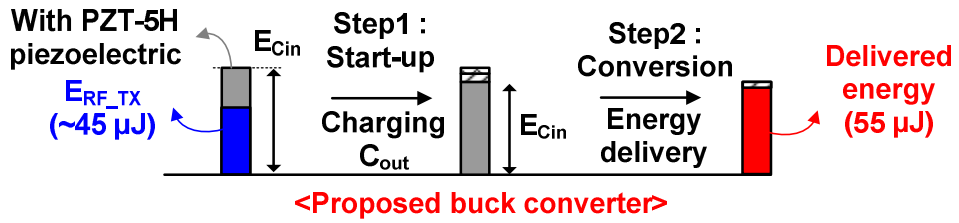


Fig. 6.11 Energy flows and losses during start-up and conversion operation of the proposed buck converter with PZT-5H piezoelectric disc.

21 μJ and 23 μJ, respectively, in the conventional buck converter. On the other hands, their values were 2.5 μJ, 6.9 μJ and 12.6 μJ, respectively, in the proposed buck converter. Considering that the rest of energy after start-up operation in the proposed buck converter is much larger than that in the conventional one, the conversion energy loss $E_{loss,conv}$ of 12.6 μJ in the proposed buck converter is a greatly reduced value. In other words, if the same energy with the conventional case would be transferred to the load, only 7.8 μJ would be incurred. As a result, the total energy loss of the proposed buck converter can be reduced over 4×, which allows that the BWS application can use a cheaper PE disc such as PZT-5H. Note that a PZT-5H was $5-cost while the PMN-PT was $50-cost.

Fig. 6.11 illustrates the energy flows and losses when using a PZT-5H PE disc. The proposed buck converter can deliver the enough energy of 55 μJ to the RF transmitter while the available energy stored in C_{in} was 68 μJ. Fig. 6.12 illustrates the measured key waveforms of the buck converter when the RF transmitter was operating in active mode. After the charging process completes in the harvesting stage, which took approximately 300 ms, the buck converter began charging C_{out} to

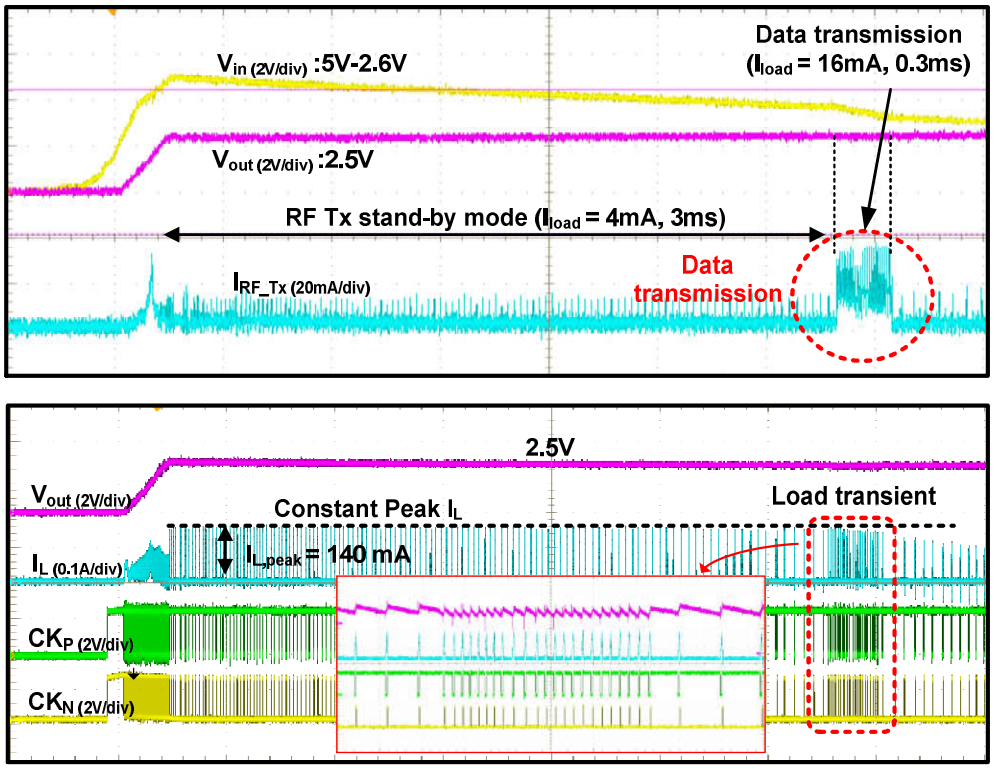


Fig. 6.12 Measured waveforms for RF transmitter operating in active mode with PZT-5H.

2.5 V V_{out} during the 0.12 ms long start-up period. Once V_{out} reached 2.5 V, the buck converter began operating in PFM mode to deliver a steady 2.5 V output, while I_{load} abruptly changed from 4 to 16 mA during data transmission. The CYRF8935 Wireless USB transmitter consumed 4 mA during the 3 ms long stand-by period and 16 mA during the following 0.3 ms period when transmitting on/off messages to the target device (e.g., lighting), and consuming a total energy of 45 μJ for data transmission.

Chapter 7

Conclusion

This work proposes energy-efficient inductor current controls of the buck converter to maximize the energy delivery in battery-free applications. Minimizing the energy losses incurred during start-up and steady-state operations of the buck converter is crucial because there is no constant power source in the target applications. To address this problem, three inductor current control techniques have been presented that can greatly reduce the energy losses by minimizing the unnecessary energy consumption.

Chapter 3 described the proposed design concepts in detail based on the analysis. In start-up operation, the switching-based stepwise capacitor charging scheme was employed to keep the average inductor current constant. By using the constant current source and by charging the capacitor in a stepwise fashion, the loss incurred at the start-up circuit can be greatly reduced. In addition, the variable on-time PFM scheme was employed to keep the peak inductor current constant at steady-state operation. By adaptively varying the on-time as the input voltage decreases, it can keep the voltage ripple small within an acceptable range needed by the application over wide ranges of input voltage conditions even with a small output capacitor and improve the power efficiency by reducing the switching frequency. Finally, the adap-

tive off-time positioning zero-crossing detector (AOP-ZCD) was employed to predict the inductor current waveform and then adaptively position the turn-off timing of the low-side switch in the vicinity of the zero-inductor-current timing without using a power-hungry continuous-time ZCD.

While Chapter 4 presented the detailed circuit implementation for realizing the proposed circuit techniques, Chapter 5 demonstrated the performance of the prototype buck converter fabricated in 250 nm CMOS technology. To charge a 2.2-μF output capacitor to 2.5 V, the action of switching the buck converter at 1.6 MHz and ramping the duty-cycle from 0 to ~50% over a 0.12-ms T_{ch} can maintain the start-up energy loss below 10 μJ. In addition, it achieved a peak efficiency of 96% at 25 mA load, over 80% efficiency for 1–25 mA load, and efficiency enhancement factor (EEF) of 25.8% at 25 mA load, which is the highest EEF reported to date.

By using the proposed buck converter, the battery-free wireless remote switch (BWS) was realized in Chapter 6. To supply the energy instead of battery, a disc-type piezoelectric (PE) transducer was used that can generate the energy from the button-pressing actions of users. Thanks to the proposed energy-efficient buck converter, the prototype BWS can have energy benefit, which allows to transmit a 4-byte-long message via 2.4-GHz wireless USB channel over a 10-m distance even with a low cost 300-mm^2 PZT-5H piezoelectric disc.

Finally, the proposed inductor current control methods can be applied not only to battery-free application but also to various other applications such as wearable devices, medical sensors, and the Internet of Things (IoT) because it can always achieve high efficiency for wide ranges of input / output voltage.

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초 록

배터리가 없는 어플리케이션에서 에너지를 최대한 로드 시스템으로 전달하기 위해 벅 컨버터 전압 레귤레이터를 제안한다. 본 연구에서는 에너지 전달을 제한하는 벅 컨버터의 초기 구동 및 정상상태 동작에서 발생하는 에너지를 최소화 하는 것을 목표로 한다. 특히, 배터리 같은 일정한 파워 공급원이 없고, 오직 주위의 에너지로부터 적은 에너지를 수확하여 동작해야 하기 때문에, 에너지 부족 문제는 매우 심각하다. 이런 문제를 해결하기 위해서, 본 논문은 각각의 동작에서 발생하는 에너지 손실을 줄이기 위해 최적화된 인덕터 전류 제어 방식들을 제안한다. 첫 번째는, 스위칭 기법을 이용한 단계적 캐패시터 충전 방식으로, 벅 컨버터가 초기 구동할 때 인덕터의 평균 전류 값을 일정하게 만들어준다. 인덕터를 스위칭하여, 인덕터 전류를 일정한 전류원으로 만드는 방식으로, 이를 이용해 캐패시터를 단계적으로 충전하면 회로에서 발생하는 많은 에너지 손실을 줄일 수 있다. 두 번째는, 펄스 주파수 변조 (PFM) 방식에서 온타임을 동작하는 전압에 따라 변화시키는 방법으로, 벅 컨버터가 정상 상태에서 구동할 때 인덕터 최대 값을 일정하게 만들어준다. 이를 통해 작은 출력 캐패시터를 가지고도 출력 전압 리플을 줄일 수 있을 뿐만 아니라, 효율을 증가시킬 수 있다. 세 번째는, 기존의 파워를 많이 소비하는 영전류 검출회로 (ZCD) 를 사용하지 않고도, 인덕터 전류의 파형을 예측하여, 영전류 시점에 스위치를 꺼주는 방식으로, 벅컨버터가 정상 상태로 동작할 때 제어회로에서 소비하는 파워 소모를 효과적으로 줄일 수 있다. 제안하는 전류 제어 방식의 효과를 확인하기 위해, 250 나노 CMOS 공정으로 무전원 무선 스위치 칩을 제작하였다. 스위치 버튼을 누르는 힘을 이용해 PMN-

PT 압전소자가 에너지를 발생시키고, 그 중 246 μJ 에너지를 수확하였으며, 제안하는 벅 컨버터를 이용해 200 μJ 이상의 에너지를 로드로 전달하였다. 이 에너지를 이용해 2.4-GHz wireless USB channel 을 통해 4-bype 메시지를 성공적으로 전달 할 수 있었다. 만약 이 어플리케이션이 제안하는 벅 컨버터를 사용하지 않았다면, 수확한 에너지는 대부분 전달하는 회로에서 손실되고 말았을 것이며, 한 번 스위치 버튼을 누르는 동작으로는 시스템에 충분한 에너지가 전달 되지 않았을 것이다. 즉, 제안하는 벅 컨버터를 사용함으로써 에너지 손실을 최소화 함으로써, 기존에 사용하는 비싼 PMN-PT 압전소자를 쓰지 않고, 값이 10 배 싼 PZT-5H 소자를 사용해도 구현 가능함을 확인 하였다.

주요어 : 벅 컨버터, 무전원 어플리케이션, 스위칭 방식을 이용한 단계적 캐패시터 충전, 온타임 변환, 오프타임을 적응적으로 위치시키는 영전류 검출회로, 무선 송신기, 무전원 무선 스위치.

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