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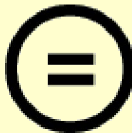

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공학박사 학위논문

Design and Fabrication of Highly Stable Oxide TFT Shift-Register Employing the Current Sensing Feedback System

전류 센싱 피드백 시스템을 이용한 고안정성 산화물 **TFT** 쉬프트 레지스터의 설계 및 제작

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Abstracts

Design and Fabrication of Highly Stable Oxide TFT Shift-Register Employing the Current Sensing Feedback System

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Integration of shift registers on the glass panel allows the display to be thinner, lighter, and cheaper to produce, thanks to the reduction of the number of ICs for scanning horizontal lines. Circuits of the shift register employing n-type thin film transistors (TFTs), such as hydrogenated amorphous silicon (a-Si:H) and oxide TFTs, have been reported. Recently, oxide TFTs attract much attention due to their high mobility (5~10 $cm^2/V\cdot s$) compared with that of a-Si:H TFT (0.8$cm^2/V\cdot s$). However, oxide TFTs often suffer from severe degradation of the threshold voltage (V_{TH}) against the temperature and electrical stress.

In this paper, in order to compensate the instability of oxide TFTs in the shift register, an oxide TFT with double gates, which can control V_{TH} by varying the top gate bias (V_{TG}) is adopted. The top gate of the double-gate TFT can be

fabricated in the same process for the pixel IZO (Indium Zinc Oxide) so that an additional process only for the top gate is not required. Adequate V_{TG} is provided timely, adaptively to the gate of the oxide TFTs to stabilize the threshold voltage.

The fabrication result shows that the proposed shift register using V_{TG} set at an adapted value become stable at 100℃ whereas the conventional one is mal-functioning.

The optimum V_{TG} varies from product to product and changes continuously over the lifetime of the display. Therefore, the feedback driving system suitable for the proposed shift register is required to search the optimum V_{TG}. The system has two main functions; the first is to sense the current of shift register and the second is the searching algorithm for finding the optimum V_{TG}. When the transistors are degraded by an external stress, the current of the whole shift registers is changed. The information about the V_{TH} degradation in the shift register can be gathered via current sensing circuit. The sensed current is integrated to generate the output and is forwarded to an ADC. The binary-converted current of shift register is processed by the proposed algorithm in the digital domain for obtaining an optimum V_{TG} and then the result is converted back to analog to generate V_{TG}. The IC implementing such functions is fabricated in a 0.18 μm BCDMOS process. When the shift register current is measured on the conventional system with increasing temperature up to 80°C, it is increased to more than 10 times than that at the room temperature. However, the proposed feedback system keeps a highly stable (<13%) current level of shift register up to 80°C with an optimized V_{TG}.

Keywords: oxide thin film transistor, shift register, feedback system, V_{TH} compensation

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Chapter 1 Introduction

The TFTs employing the oxide material, such as IGZO, have attracted considerable attentions as promising devices for the active area for AMLCD and AMOLED. The electrical characteristics and stability of the oxide-based TFTs are not only superior to those of the a-Si:H TFTs, but also much more uniform than the poly-Si TFTs. In high-end display applications such as ultra high-resolution, frameless monitor and long battery life tablet, most of the oxide-based TFTs are inherently depletion-mode devices rather than the widely used enhancement-mode devices. It is well known that a design of driving circuits which employ a depletion-mode device is rather difficult. Therefore, the design of driving circuits employing the oxide-based TFTs may be a very important factor in order to commercialize the oxide-based TFTs. Furthermore, TFTs are degraded in operating condition. These issues limit the usage of oxide TFT in real application. Nevertheless, high mobility and low leakage current, inherent advantages of oxide TFT, are the required characteristics in the high-end display applications.

1.1 Background

Flat panel displays (FPDs) such as active-matrix liquid crystal display (AMLCD) [1], active-matrix organic light-emitting diode (AMOLED) [2], plasma display panel (PDP) [3] have been developed extensively over the last decade [4]. Among FPDs candidates, AMLCD is widely used due to its thinness, light-weight, low power requirement, and cost-effectiveness. AMLCD is produced in many different sizes and applications such as smart-phone, digital camera, tablet PC, notebook PC, computer monitor and TV.

Although AMLCD technology has been developed, the inherent drawback of the liquid crystal material, slow response time, causes the residual image and motion blur problem of f fast moving images. High operation frequencies such as 120 and 240 Hz suppress these problems [5], [6]. Also, there are many advanced technologies in AMLCD such as ultrahigh definition (UHD), 3-dimension (3D) and On-cell/In-cell touch which require faster response time. Therefore, the electrical characteristics of thin-film transistors (TFTs) are important factors in ultrahigh-resolution and high-frame-rate display.

Recently, AMOLED has attracted a considerable attention due to its wider viewing-angle, faster response-time, more vivid colors, lightweight, and low power-consumption in comparison with AMLCD. The AMOLED mainly occupies the smart-phone and mobile device market.

In AMOLED, the image quality is directly proportional to the characteristics of TFTs because the luminance of OLED linearly increases with the current controlled by TFT. It should be noted that the basic pixel circuit in AMOLED could be operated with only 2 transistors and 1 capacitance. However, the drawbacks of TFTs such as non-uniformity and poor electrical stability should be

compensated [7]-[12].

There are many material candidates for AMLCD and AMOLED including hydrogenated amorphous-silicon (a-Si:H) TFTs and low temperature polycrystalline-silicon (LTPS) TFTs. a-Si:H TFTs are very suitable for large area applications due to its low-cost, low temperature processing, and better uniformity over large area substrates. They are widely used as a switching device of pixel elements in AMLCD. They have been widely used in commercial applications. It could be produced with below 400℃ process which is comparable to low price glass substrate [13]-[15]. Drastic improvement in the driving technology and the electrical performance of a-Si:H TFTs makes it possible not only to switch pixels but also to integrate the shift register [16]-[25]. However, a-Si:H TFTs have drawbacks such as low field-effect mobility (<1 $cm^2/V\cdot s$), instabilities with respect to bias stressing [26] and light exposure [27]. The growth of high-end commercial market with ultrahigh-resolution (UD), high-frame-rate (>240Hz), and sizes larger than 70 inches require a higher electrical performance from TFTs. At least 3 $cm^2/V\cdot s$ of field-effect mobility is required to satisfy such demands [28], a condition not so easy to achieve by modifying the conventional amorphous silicon material. Also, the threshold voltage of a-Si:H TFTs is easily increased or decreased when the gate bias is applied. The charge trapping and defect state creation are considered main mechanisms of instabilities of a-Si:H TFTs [26], [27], [29]-[31]. It is well known that the SiNx, which is widely used as a gate insulator, has a high density of trap sites. When the gate bias was applied at the a-Si:H TFTs, the electron charges are trapped at the SiNx gate insulator or at SiNx/a-Si:H interface [32]. When the positive bias is applied at a-Si:H TFTs, the defect states could be generated at a-Si:H layer or at SiNx/a-Si:H interface [33]. Almost all extra electron carriers generated by gate bias in channel region are accumulated in tail state of conduction band which has

weak Si-Si bonds.

On the other hand, LTPS TFTs are widely used to drive AMOLED because they exhibit a more sufficient and stable current supply into the OLED than the a-Si TFTs. Since the poly-Si TFTs could be made as both NMOS and PMOS TFTs, the CMOS circuit could be designed [34]-[36]. As a result, the peripheral driver circuits of flat panel display could be integrated at glass substrate without additional integrated chip. The poly-Si TFTs can exhibit electron mobility in excess of 50 $cm^2/V\cdot s$, and they are much more stable than the a-Si:H TFTs. However, large area application has been proven to be difficult, and the relatively high thermal budget makes poly-Si unsuitable for flexible substrates. It is suffered from current non-uniformity at large area caused by inherent fluctuation of laser energy density. Because each laser pulse generated during crystallization of amorphous silicon has different energy density, and the spot size of laser is very small, the electrical characteristics of the poly-Si are not uniform. The many compensation circuits in AMOLED have been proposed in order to compensate for the current non-uniformity of the poly-Si TFTs. The production cost of the poly-Si TFTs is relatively high due to expensive laser equipment.

Recently, the oxide-based TFTs, such as ZnO, InGaZnO (IGZO), HfInZnO (HIZO), ZnSnO (ZTO), ZnInO (ZIO), and ZnInSnO (ZITO), have drawn interest as promising alternatives to pixel elements of FPD [37]-[54]. The electrical characteristics and stability of the oxide-base TFTs are superior to those of the a-Si:H TFTs, and at the same time, their uniformity is much better than that of poly-Si TFTs. The field-effect mobility of the oxide-based TFTs is about 10 $cm^2/V\cdot s$, a value not too small to drive AMLCD with ultrahigh-resolution and high-frame-rate or AMOLED. In addition, oxide semiconductor materials have an amorphous phase in general, which shows uniform electrical properties even

with a large-area substrate and is strongly advantageous for the display applications. The production process of the oxide-based TFTs are compatible to that of the a-Si:H TFTs. In the integrated shift register structure, oxide-based shift register is superior in terms of bezel width compared to a-Si:H TFT based circuit. Due to the higher mobility of oxide based TFT than that of a-Si:H based TFT, the size of TFT shift register in bezel area of display panel is dramatically reduced when the display panel adopts the oxide based TFT. The low-leakage current of oxide-based TFT is also a superior characteristic for mobile or tablet application, for it allows a long battery-life. One of the methods to lower the panel power consumption is reducing the refresh rate of panel driving from 60Hz to 30Hz or even less. In the blank time of low frequency driving, which is the time period between panel refresh times as Figure 1.1, pixel data should be maintained to avoid display picture degradation. The low leakage characteristic of oxide TFTs enables them to maintain the pixel data even though the frequency of panel refresh is as low as 1Hz or less.

On the other hand, the stability of the oxide-based TFTs, especially under light illumination [55]-[61], should be improved in order to apply at practical application of FPD as shown in Figure 1.1

In this study, the feedback system is proposed to compensate for the oxide-based TFTs degradation which is the V_{TH} shift characteristic caused by the operating temperature and electrical bias stress in an operating condition.

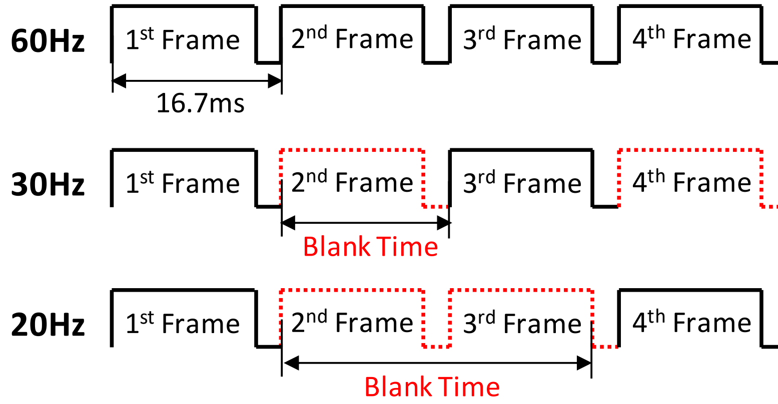


Figure 1.1 Low frequency driving of Display

1.2 Outline

In this paper, a new driving system is proposed for shift register circuits employing oxide TFTs. The proposed system includes a circuit for sensing the current consumption, a feedback control system to supply the adjusted top gate voltage, and a software algorithm for searching the optimal top gate bias voltage. The system regulates the current consumption of the shift register within the desired value by adjusting V_{TH} above zero through the top gate, thereby producing stable gate driving signals against process fluctuations and circumstances of extreme temperature.

Chapter 2 will provide technological background for early works, especially the circuit design of the shift register. How they used the conventional technologies to integrate shift register on the glass substrate will be reviewed. As using oxide based TFT and N type driving circuit it will cover a wide range of recent works facilitating system integration e.

Chapter 3 will present the new shift register of oxide TFT employing the double gate TFT structure to compensate for the degradation of TFTs. It includes the design and verification of a new shift register circuit, using the simulation and experimental method.

Chapter 4 will show the system architecture using current feedback system to compensate for the TFTs degradation. The current sensing circuit is designed and fabricated by 0.18μm BCDMOS process. It will discuss the system configuration, which is composed of three driving circuits and one algorithm block, respectively..

Chapter 5 is the summary of this thesis.

Chapter 2 Review of oxide-based TFT device and N-type TFT circuit design

Recently, oxide-based thin film transistor (TFT) has attracted much interest due to its higher mobiliy (～5 to 50 $cm^2/V \cdot s$), low temperature processing, and transparency, compared to a-Si:H TFTs. Oxide-based TFTs can be utilized as a backplane for high-performance AMLCD and the key element for an emerging AMOLED display technology. It is well known that TFTs for the display application need to stay in a stable condition while operating under the continuous exposure to illumination.

On the other hand, most of the oxide-based semiconductor materials are n-type due to the existence of intrinsic donors. Therefore, all driving circuits with the oxide-based TFTs should be designed by employing only n-type TFTs. is the same strategy applies for the integrated circuits using a-Si:H TFTs which was fabricated by only n-type TFTs.

2.1 Overview

2.1.1 Characteristics of Oxide TFT

As the flat panel display pursues in high-resolution, large-size and high-speed refresh rate, the key electrical characteristics of TFT such as mobility, stability, and uniformity become a critical issue. Due to the defects in a-Si:H TFTs or non-uniformity of polycrystalline-Si TFT, ZnO-based TFTs have been extensively studied [62, 63]. These TFTs have gained as much attention because they not only were transparent but also exhibited electron mobility (μ) of 0.3–2.5 $cm^2/V\cdot s$ and I_{ON}/I_{OFF} ratio of ~ 10^7. After these characteristics were revealed, various research group have focused on the study of an oxide-based TFT to improve the performance of oxide TFTs.

Several advantages of Oxide-based TFT in display applications are as follows:

1) Field-effect mobility in the range of 5 to > 50 $cm^2/V\cdot s$, a value about ten times greater than that of a-Si:H

2) An amorphous crystal structure for better uniformity and easier manufacturing compared with poly-crystalline silicon

3) low-temperature processing which is suitable for flexible substrates

It should be noted that Nomura et al. suggested using a complex $InGaO_3(ZnO)_5$(or IGZO) single-crystalline semiconductor layer in a TFT [63]. Also, the explosive attention about the application of amorphous multi-component oxides as channel layers in TFTs can be enabled after Nomura's report. Several combinations of cations, such as IZO [64], [65] and IGZO [66]-[68] which is the most widely explored ones, would be assessed. With the continuous improvement seen in these devices, it is now common to obtain remarkable

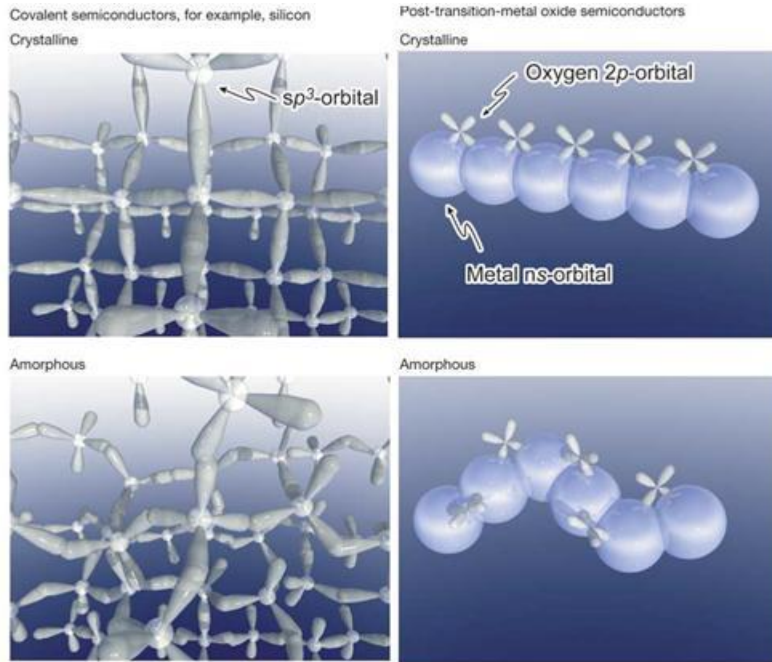
electrical properties, such as mobility above 10 $cm^2/V\cdot s$, I_{ON}/I_{OFF} ratio exceeding 10^7 and sub-threshold swing of 0.20 V/dec, with the indium-based semiconductors. In particular, a-IGZO is the most widely used semiconductor oxide materials [41]. Oxide-based semiconductor channel layers can be formed by sputtering at a temperature of 300 °C or lower [69, 70]. One of the important parameters is the oxygen concentration because oxygen vacancies are the major source of free carriers. As oxygen partial pressure increases, the transfer curve is positively shifted [71]. By optimizing oxygen content, highly mobile (46 cm^2/Vs) and high performing (SS = 0.54 V/decade, $V_{th} \approx 0$ V) devices can be obtained [72].Most of the oxide-based semiconductor materials are n-type due to the existence of intrinsic donors. Therefore, all driving circuits with the oxide-based TFTs should be designed by employing only n-type TFTs.

ZnO TFT exhibited high mobility near 20 cm^2/Vs with room temperature deposition[73], but relatively high gate voltage was required. Higher electrical conductivity (10^{-3} Ω^{-1} cm^{-1} to 10^{-2} Ω^{-1} cm^{-1}) of oxide semiconductor than that of a-Si:H attributes to the oxygen vacancies, cation interstitials, and substitutional/interstitial hydrogen, acting as shallow donors [74]. TCOs have a high carrier concentration (10^{18} cm^{-3} to 10^{21} cm^{-3}) because of these donors. However, polycrystalline structure causing non-uniformity problem, and the difficulty to fabricate were drawbacks of ZnO TFTs.

In 2004, Nomura et al. reported a TFT adopting amorphous oxide semiconductor deposited at room temperature, IGZO, which demonstrated high-mobility (μ ~ 8.3 cm2/Vs) and low off-current [41]. Contrary to silicon-based TFTs, IGZO TFTs have high filed-effect mobility even though they are amorphous because of the electronic orbital structure of IGZO. As shown in Figure 2.1, a conducting path for free electrons is formed by the direct overlap between neighboring metal s orbitals. The conduction band of IGZO is mainly formed by the overlap of In 5s

orbitals. Due to the spherical symmetry of the 5s orbitals, as shown in Figure 2.1, the semiconductor is insensitive to structural deformation, allowing IGZO to have high mobility even in the amorphous phase.

Therefore, IGZO TFTs have been considered as a promising material for display products due to its high performance and good uniformity. Thus, in the past decade, display prototype adopting the oxide-based TFT has been demonstrated as shown in Figure 2.2. UHD 240Hz with 70 inch LCD TV has been successfully proven to operate and display an image with oxide-based TFT.



(a) (b)

Figure 2.1 Schematic orbital drawings for the carrier transport paths in crystalline and amorphous semiconductors: (a) Covalent semiconductors, (b) Amorphous oxide semiconductors [41].

Figure 2.2 Prototype 70’’ IGZO ultra definition LCD TV (Ref. DisplaySearch)

2.2 Oxide-based TFT

2.2.1 Electrical characteristics of oxide-based TFT

The carrier transport of oxide semiconductors may be attributed to the overlapping of s-orbital and the ordering of metal atoms [75]. These carrier transport properties are unique to oxide semiconductors and are not seen in covalent amorphous semiconductors such as a-Si:H as shown in Figure 2.1 [41]. The oxide semiconductor materials are divided into three main categories, ZnO, IGZO and others including ZTO, ITO, IZO and IZTO. Among these categories, IGZO is most widely used for the key component of the backplane for LCD and OLED.

The effect of IGZO composition on the TFTs electrical properties has been reported by Iwasaki et al. [68] and by Barquinha et al. [76].

Transfer characteristics are presented in Figure 2.3 for different combination of compounds, being the trends of μ_{FE} and V_{ON} with composition shown in Figure 2.4.

As shown in Figure 2.3 and 2.4, ZnO seems to be the best binary compound for oxide TFT application. Most of the oxide-based TFTs are inherently a depletion-mode device rather than the widely used enhancement-mode device due to large electron concentrations [77]–[82]. An enhancement-mode oxide-based TFT could be fabricated by controlling some fabrication parameters. As the oxygen partial pressure increases, the threshold voltage of the oxide-based TFTs is shifted in a positive direction [83]. For non-passivated IGZO TFTs with different $\%O_2$, 0.4 % and 10.0 %, the films with $\%O_2$=10.0 % have a lower density of oxygen vacancies, which are known to be the main source of free carriers in oxide semiconductors. Also, a threshold voltage is shifted in a positive

direction as the active layer thickness decreases [84] by the decrease of carrier concentration.

In the display application, the composition of the IGZO is very important because the flat panel display needs long term stability and higher electrical performance, such as high current driving capability.

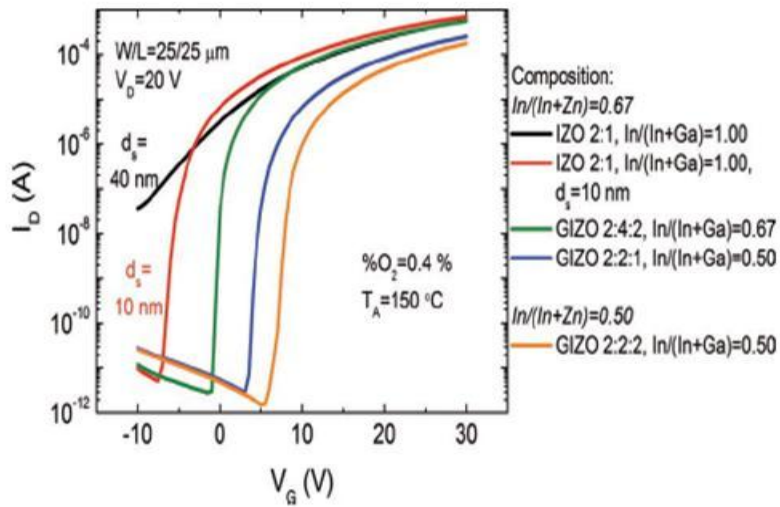
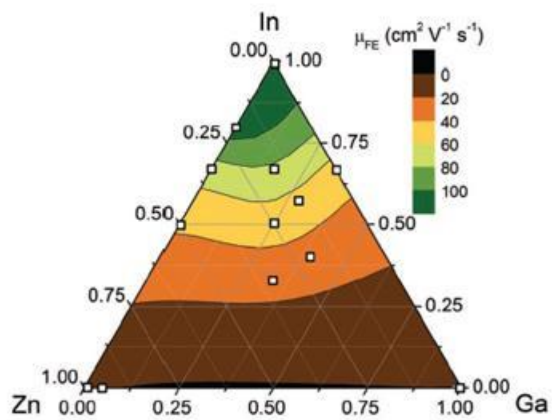


Figure 2.3 Effect of oxide semiconductor target composition on the transfer characteristics of TFTs annealed at 150 °C: ternary and quaternary compounds. The effect of decreasing d_s from 40 to 10 nm for IZO 2:1 is also shown [76].



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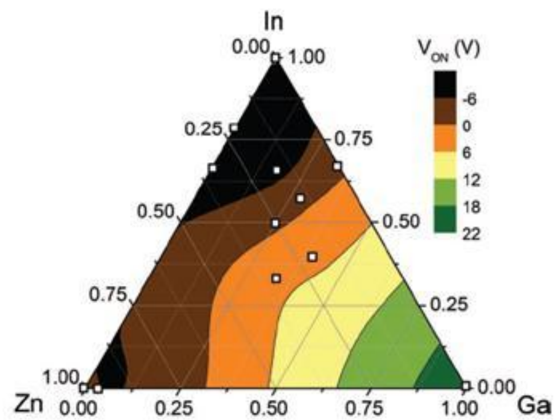


(b)

Figure 2.4 (a) μ_{FE} and (b) V_{ON} obtained for TFTs with different oxide semiconductor compositions in the indium-gallium-zinc oxide system. Devices annealed at 150 °C, with%O_2 = 0.4% [76].

2.2.2 Stability of oxide-based TFT

It is well known that oxide based TFTs have a good stability in darkness, but, under the light,, and negative bias stress, the stability issues are still remaining . It should be noted that TFTs in display panel are mostly turned off during their operation and exposure to light. Under negative gate bias stress with light illumination, V_{th} shifts in a negative direction considerably. Therefore, the stability under the negative bias illumination stress is crucial.

Based on the understanding of a-Si:H TFTs [26], [27], it can be expected that light illumination and bias stressing may cause instabilities such as charge trapping and defect creation in the amorphous oxide-based TFTs in the gate dielectric or at the oxide semiconductors/dielectric interface. Positive bias stressing has usually been tested for AMOLED applications, because TFT must supply a stable current during the entire operating time. In general, oxide semiconductors have n-type characteristics, so turning off the device requires applying negative voltage at the gate. It is well known that the turn-off period of switching TFT in the LCD driving scheme is over 99%, and the turn-on period is less than 1%. For example, the pixel turn-on time is calculated to be (1/1080*60=15.4us), and the turn off time is simply calculated to be (1079/1080*60=16651us) for FHD (1920*1080) resolution operated at 60Hz (16666us). Gate turn-on duty is 1/1080, so most of operating time is exposed to the turn off time. Severe negative shift in threshold voltage of oxide-based TFT has been reported during negative bias illumination stress [57], [85], [86].

Figure 2.5 shows the transfer characteristics of oxide-based TFT with various intensities and wavelengths [57].

Figure 2.6 shows the schematic diagram of energy band, which explains the photo-desorption of oxygen molecules into the ambient atmosphere [87]. Figure

2.7 demonstrates that the photo-induced hole trapping can cause the degradation of oxide-based TFT. Jeong et al. reported the environmental effects such as oxygen and water molecules activity on the oxide-based TFTs[61]. As shown in Figure 2.8, a suitable passivation layer is essential to improving the long-term reliability of oxide TFTs. Without a passivation layer in IGZO TFTs, the effect of the photo desorption of oxygen molecules and subgap state at IGZO back surface cannot be excluded. To understand the effect of light on IGZO, the passivation layer must prevent the effect of ambient atmosphere and reduce the sub-gap state at the IGZO back surface.

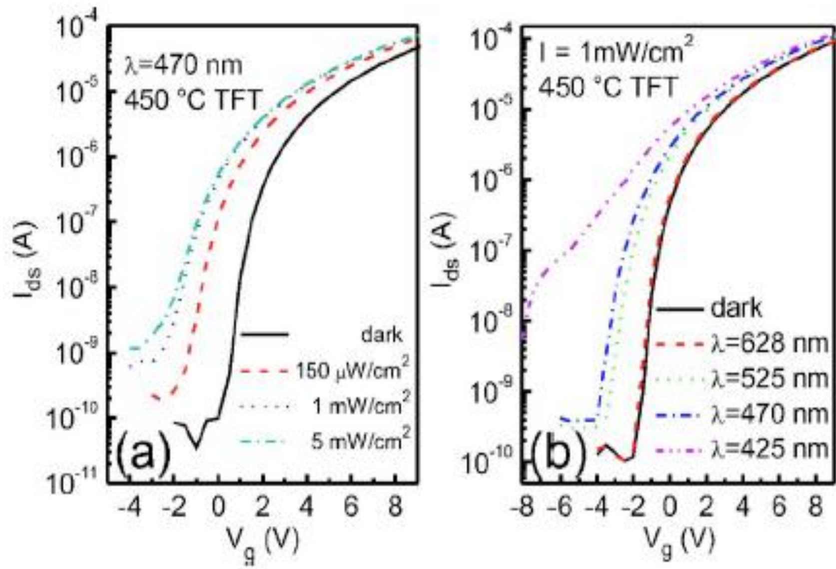


Figure 2.5 Transfer characteristics of TFT with ZTO channel deposited at 450 °C. (a) For different intensities at λ=470 nm. (b) For different wavelengths at I=1 mW/cm² [57].

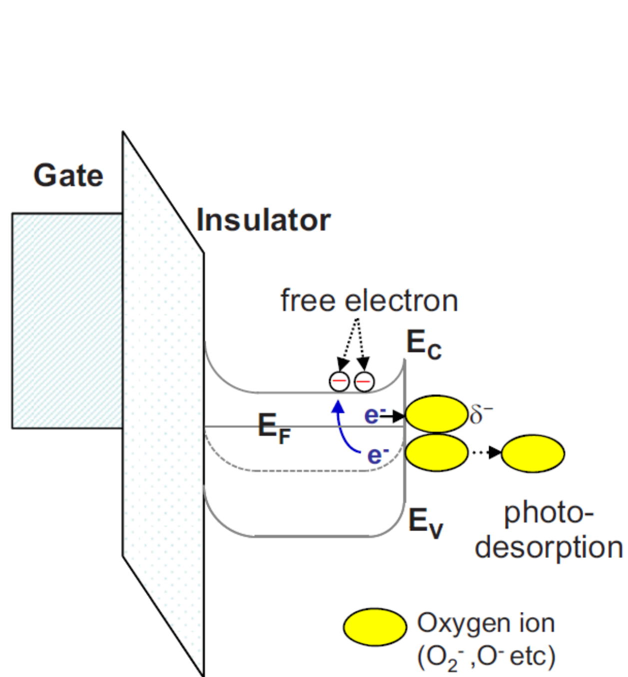


Figure 2.6 Schematic energy band diagram showing the photo-desorption of oxygen molecules into the ambient atmosphere for the un-passivated device under the application of NBS. [87]

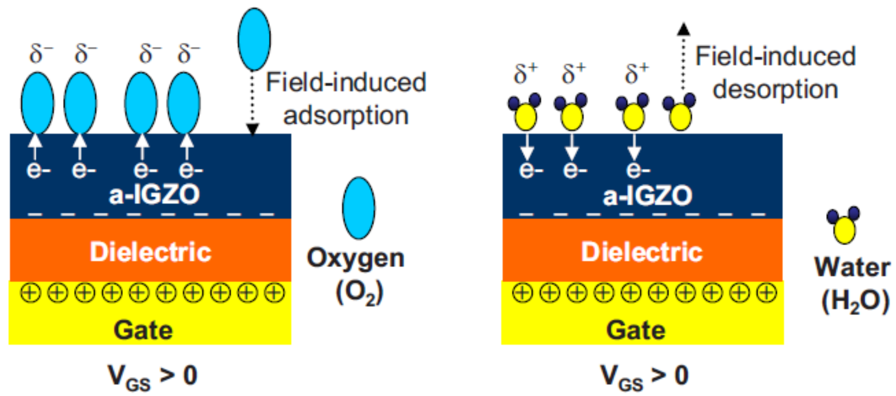


Figure 2.7 Schematic showing the electric-field-induced adsorption of oxygen molecules from the ambient atmosphere under the application of positive bias stress (left). Schematic showing the electric-field-induced desorption of water molecules into the ambient atmosphere under positive bias stress (right) [61].

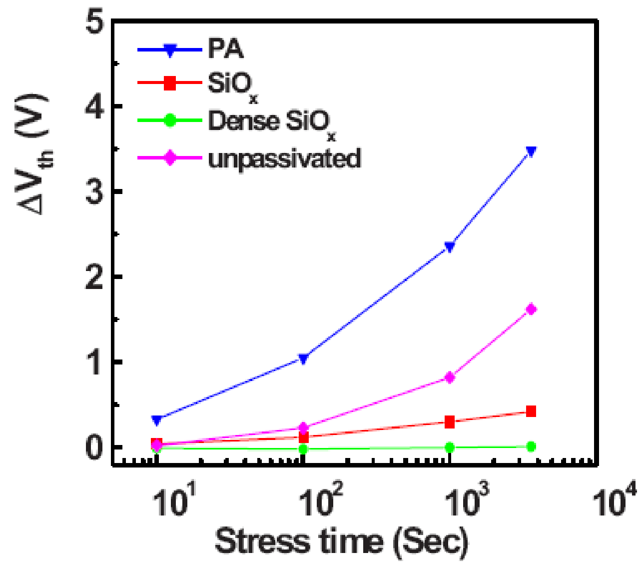


Figure 2.8 Vth shit dependence on the gate bias stresses. For comparison, the effect of the gate bias stress on the unpassivated oxide transistor was also included [61].

2.3 NMOS driving circuit

2.3.1 Bootstrapping driving circuit

It should be noted that the output voltage of push-pull CMOS inverter has the best performance because CMOS inverter can output without any threshold voltage loss. Its output voltage swings from VDD to ground. The static power dissipation of the CMOS inverter is practically zero, and the inverter can be sized to give equal sourcing and sinking capabilities. When the inverter circuit consists of only N-type TFT, the output of inverter can suffer a loss of output voltage due to threshold voltage loss. The inverter shown in Figure 2.9(a) is an NMOS-only inverter. The inverters shown in Figure 2.9(b) and (c) use a PMOS load, which isis generally the most useful in logic gates with a large number of inputs.

For the oxide-based display technology, all driving circuits should be designed by employing n-type TFTs due to the absence of practical p-type TFTs. It should be noted that oxide based TFT can be made by n-type TFT due to its intrinsic carrier property. Figure 2.10 exhibits the modified NMOS inverter [88]. The bootstrapping concept for elevating the output voltage up to VDD was reported. When an input is logically high, M1 is on, and the output decreases to approximately resistively divided voltage.

When an input transitions from high to low, M4 is used as a capacitor. The bootstrapping concept uses the capacitive coupling. The capacitive coupling results in an increase in the gate potential above VDD, allowing M2 to be fully turned on. Without bootstrapping, the M2 gate is tied to VDD, and the output is limited to VDD-V_{THN}. If the gate of M2 is bootstrapped, then M2 fully turns on, and the output reaches VDD. However, it cannot swing down to ground level as shown in Figure 2.10. Furthermore, M2 is always turned on, so the power

consumption will be a problem.

The bootstrapping concept in this circuit is very useful in designing only n-type TFT circuit that compensates for the pull up.

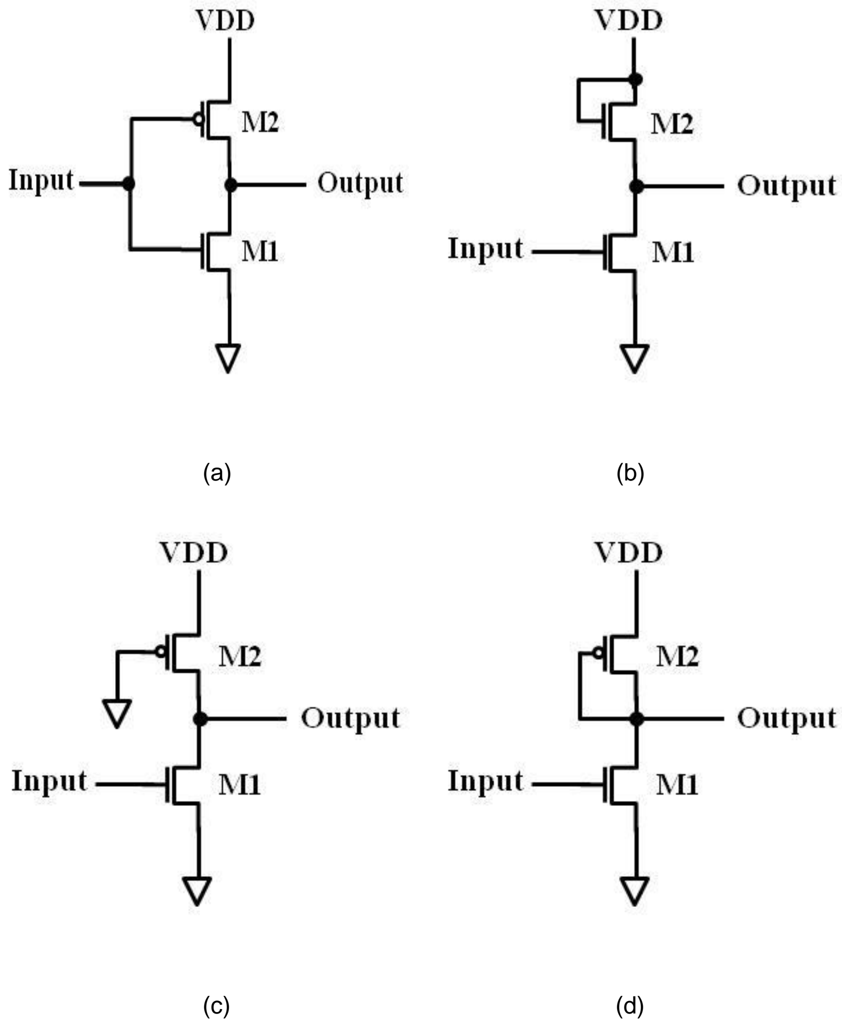
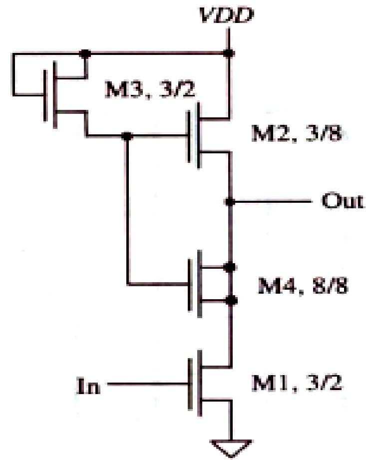
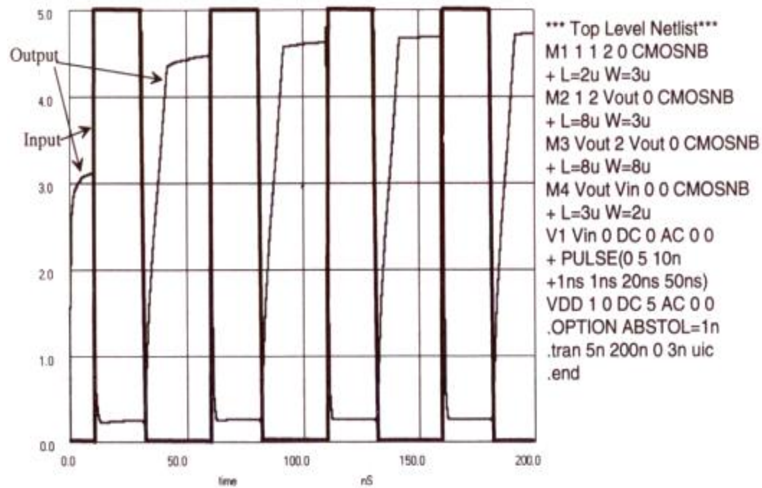


Figure 2.9 Various inverter configurations. (a) CMOS inverter, (b) NMOS-only inverter, (c) and (d) Inverter with a p-channel load [88].



(a)



(b)

Figure 2.10 (a) Bootstrapped NMOS inverter and (b) its simulation results [88].

2.3.2 Shift register with n-type TFT

Nowadays, most of display products include the integrated shift register on the panel because it can reduce the cost of external IC chip. Integrating the shift register employing a-Si:H TFTs as well as poly-Si TFTs is necessary in AMLCD and AMOLED [16]-[25].

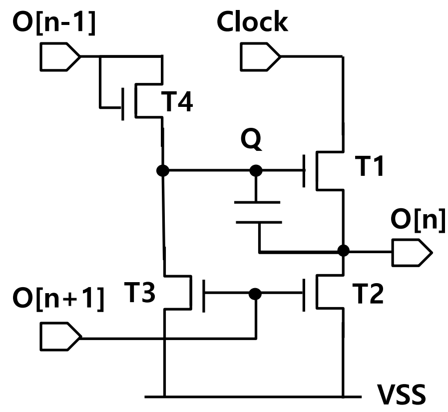
Figure 2.11 shows the schematic and the timing chart of the conventional shift register with only n-type TFTs. This circuit demonstrates the bootstrapping concept. The operation mechanism of the conventional shift register is as follows.

Stage 1: When T4 is turned on by the previous output pulse O[n-1], Q-node is charged to a high-voltage for bootstrapping.

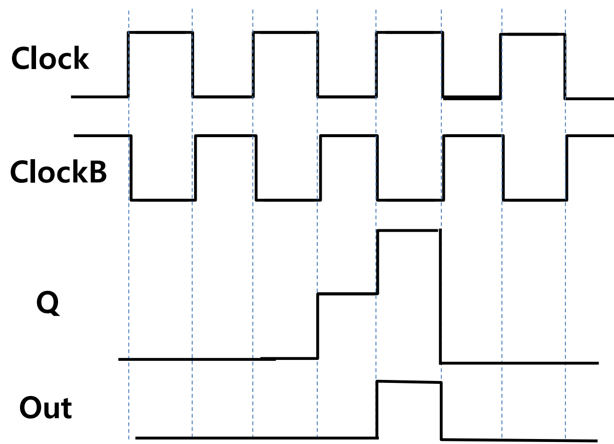
Stage 2: When the clock signal of a high-voltage is applied to the drain of T1, a Q-node is bootstrapped by the capacitances of T1. Therefore, the output pulses O[n] are generated through T1, which is fully turned on.

Stage 3: After the output pulse is generated, Q-node should be discharged to VSS when the output pulse of O[n+1] turns on T3. T3 is turned on so that the voltage of a Q-node stays low. Also, the output pulse of O[n+1] turns on T2 so that the gate-output voltage is kept at VSS.

This circuit was a very classical approach to integrating the scanning circuit on the glass panel. However, this circuit cannot be integrated on the panel due to the ripple voltage caused by the parasitic capacitance of T1. The clock voltage is always operated by AC signals (Von and VSS), so the ripple voltage caused by the parasitic capacitance of T1 will result in the abnormal operation of scanning circuit.



(a)



(b)

Figure 2.11 (a) Bootstrapped NMOS shift-register and (b) its timing diagram.

Therefore, various efforts to compensate for the ripple voltage in the scanning circuit had been reported. [89, 90] Figure 2.12 shows that the ripple compensated for the scanning circuit by using an additional TFT to clear the ripple voltage. It is well known that both the gate and output node of the driving TFT should be kept at low voltage level during the turn off timing of the shift register. When these nodes are increased during the turn off timing, the output pulse state is abnormal and the display will fail to produce image. The ripple voltage is controlled by TFT7 and TFT9 as shown in Figure 2.12. TFT7 and 9 are turned on and off by the inverter circuit. The inverter circuit can be composed of TFT3, TFT4, TFT5 and TFT6. When the clock voltage (CLK2) is high, TFT6 produces high voltage so that TFT7 and TFT9 are turned on, resetting gate and output node of the driving TFT (TFT8). The inverter output should be at low voltage level during the turn on period so that the Q node (the gate nod of TFT8) is connected to the gate node of TFT4 and 5. This circuit can be operated by the following procedure. At first, the previous output pulse is transferred into the Q node via TFT1. After that, the clock bias connected to TFT8 increases from Voff to Von in order to turn Q node to 2Von by bootstrapping. Bootstrapping can be executed by capacitance C1. The value of C1 should be carefully selected. When the value of C1 increases, the ripple voltage would decrease due to smaller capacitive coupling. However, value of C1 too large can prevent bootstrapping voltage and result in suppression of the turn on TFT8 voltage

Therefore, C1 value should be carefully designed. After bootstrapping, the reset pulse from the next stage and the clock bar (CLK1) can discharge Q-node and output node, respectively.

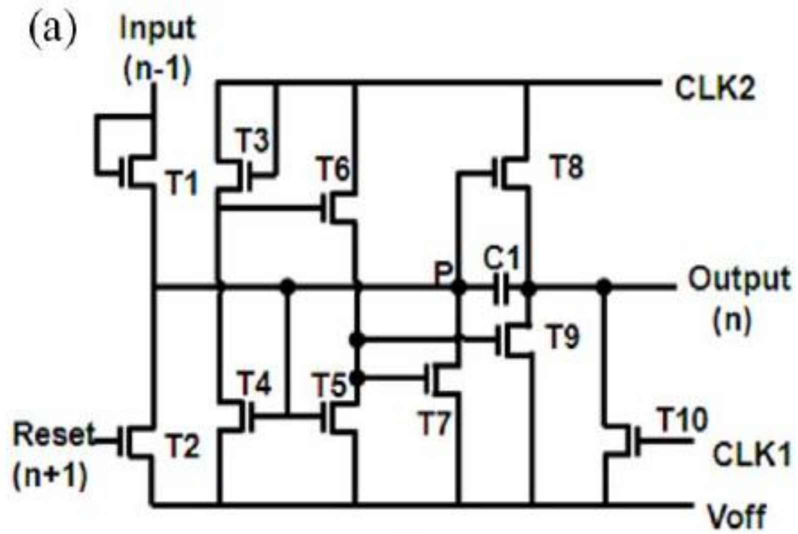


Figure 2.12 Ripple suppressed shift-register designed by only N-type TFT[89].

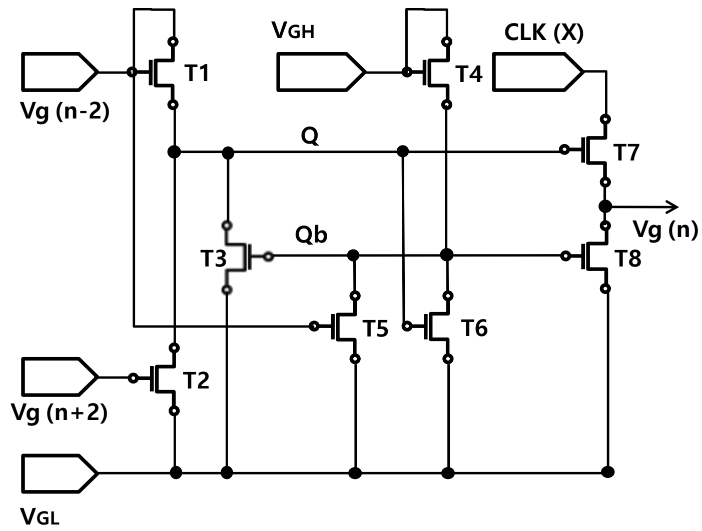
Figure 2.13 shows the schematic and the timing chart of another conventional shift register with only n-type TFTs. The operation mechanism of the conventional shift register is as follows.

Stage 1: When T1 is turned on by the output pulse of Vg(n-2) in the previous stage, a Q-node is charged to a high-voltage. At the same time, the voltage of Qb-node turns low (V_{GL}) because T5 is turned on by a Q-node of a high-voltage.

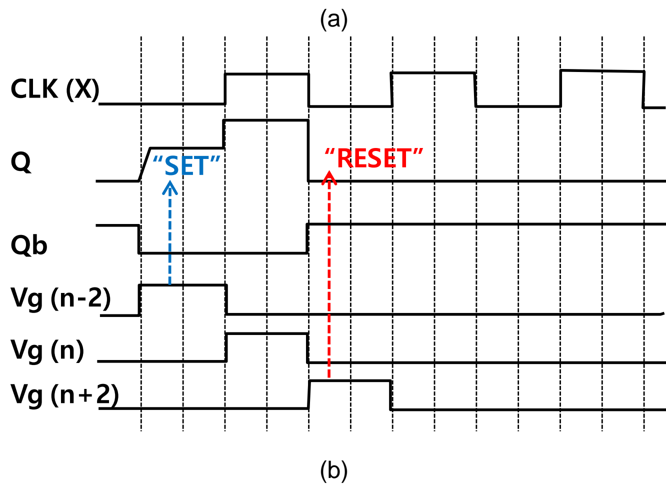
Stage 2: When CLK(x) of a high-voltage is applied to the drain of T7, a Q-node is bootstrapped by the parasitic capacitances of T7. Therefore, the output pulses [Vg(n)] are generated through T6, which is fully turned on.

Stage 3: After the output pulse is generated, a Q-node is discharged to VGL when T2 is turned on by the output pulse of Vg(n+2). T3 is turned on so that the voltage of a Q-node maintains a low voltage.

As shown in these two conventional shift registers, the operation mechanisms almost the same. The controllability of both Q and output node is the key property for highly stable shift-register.



(a)



(b)

Figure 2.13 (a) Schematic and (b) timing chart of the conventional shift register with only n-type TFTs.

However, the turn off biasing was already kept as zero voltage because both output nodes of gate and TFT8 are kept at an identical value. Especially, depletion-mode IGZO TFTs may suffer leakage in the current of TFT8. Therefore, some reports also propose the negative turn off biasing scheme as shown in Figure 2.14 [90]. The reported shift register has been designed by employing two low-voltage-level power signals with which a negative voltage can be applied to the gate–source voltage (Vgs) of depletion-mode a-IGZO TFTs.

Figure 2.14 shows the schematic and timing chart of the shift register for the negative turn off biasing [90]. As shown in Figure 2.14, the output sections of the shift register are classified into two parts. The output pulse of part(A) in the present (n) stage is supplied to node "I" by T1c. The gate of T2 is connected to the output node of the part (A) in the next (n+2) stage. During the generation period of an output pulse [period "(2)"], Vg (n−2), Vc(n−2), and Vc(n + 2) are kept at VGL, VGL1, and VGL1, respectively. The value of VGL1 is less than that of VGL. Therefore, the Vgs of T1a, T1b, and T2 become negative during an output pulse generation. It should be noted that when Vgs of T1a and T1b are negative, the leakage current is dramatically decreased.

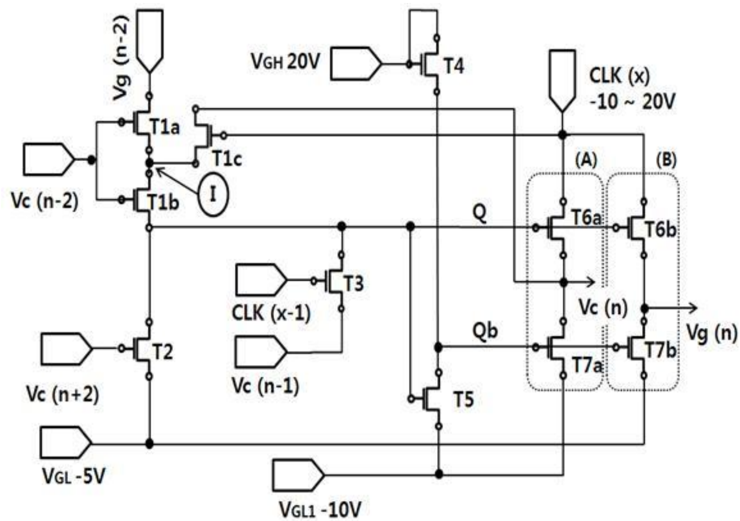
The circuit operation of the shift register is as follows.

Stage 1: When the output pulse of Vc(n-2) turns on T1a and T1b, the output pulse of Vg(n-2) pre-charges a Q- to a high-voltage . The voltage of Qb-node turns low (VGL1) because a Q-node of a high-voltage turns on T5 .

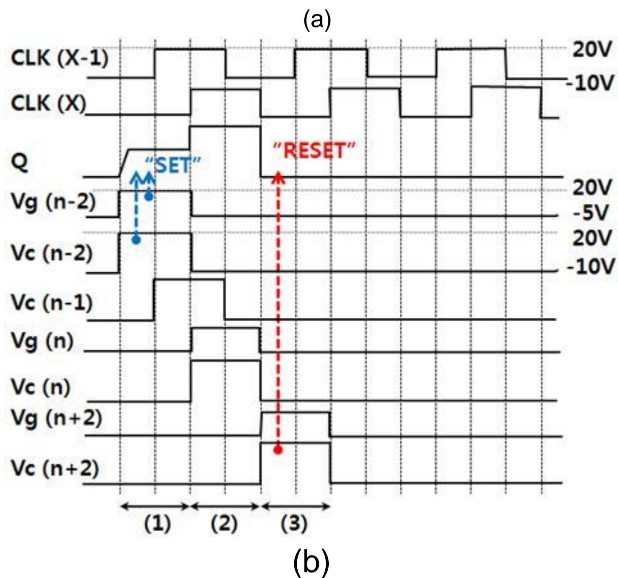
Stage 2: When CLK(x) of a high-voltage is inserted to the drain of T6a and T6b, a Q-node is bootstrapped by the parasitic capacitances of T6a and T6b. An additional bootstrapped capacitance is also possible. Therefore, the output pulses [Vc(n) and Vg(n)] are generated through fully turned on T6a and T6b, respectively.

Stage 3: The output pulse of Vc(n) in the present (n)stage is supplied to node "I" by T1c. During the generation period of an output pulse, Vg(n − 2), Vc(n − 2), and Vc(n + 2) are kept at VGL, VGL1, and VGL1, respectively. The Vgs of T1a, T1b, and T2 become negative during the output pulse generation.

Stage 4: After the output pulse is generated, a Q-node is discharged to VGL when T2 is turned on by the output pulse of Vc(n+2). T3 is turned on periodically by CLK(x-1) so that the voltage of a Q-node maintains a low voltage.



(a)



(b)

Figure 2.14 (a) Schematic and (b) timing chart of the shift register employing the turn off biasing [90].

Chapter 3 Proposed Oxide TFT Shift Register

In a shift register employing oxide TFTs, abnormal gate output was observed due to V_{TH} shift in a negative direction. In this thesis, V_{TH} of double gate TFT is controlled by top gate bias in order to compensate for the V_{TH} shift caused by ambient temperature, electrical stress and process fluctuation. This chapter proposes the shift register structure adopting double gate TFT. At first, device characteristics of double gate TFT are discussed to find out if the double gate TFT is suitable for the shift register. Secondly, simulation of conventional shift register circuit was analyzed to understand the malfunction mechanism. Then, a new shift register adopting double gate TFT is proposed and verified through simulation.

3.1 Overview

A double gate TFT is a well known device structure which has top gate electrode in addition to the inverted-staggered TFT as shown in Figure 3.1. When top and bottom gates are connected, and the same voltage is applied, on-current of double gate TFT increases. It has been reported that the current 2.4 times greater was observed at V_{GS} = 20 V when 150 nm thick passivation layer is used as a top gate insulator [91]. On the other hand, when a top gate voltage is applied independent of a bottom gate, V_{TH} changes according to the top gate-to-source voltage (V_{TS}) [92]. It means that the top gate can control the V_{TH} which shifts according to ambient temperature, electrical stress and process fluctuation. In this thesis, the double gate TFT is applied to the shift register to improve the circuit stability. In this chapter, characteristics of double gate TFT and a design of shift register circuit are described.

3.2 Characteristic of Double Gate TFT

Firstly, conventional and double gate TFT were fabricated and compared to find out if the double gate TFT is suitable for an integrated circuit. The double gate TFT can be fabricated with no additional mask and process because the pixel electrode can be used as a top gate electrode in display. Titanium and copper were deposited by DC sputtering on a glass substrate as the gate metal. SiO_2 gate insulator layer 200 nm thick was deposited by plasma enhanced chemical vapor deposition (PECVD) and the 40 nm thick active layer by sputtering. After the active island was patterned, the 250 nm thick source and drain electrodes (Cu) were deposited by sputtering. ITO top gate electrode was deposited after SiO_2 passivation layer was deposited. Figure 3.2 shows the transfer curves of fabricated single and double gate TFTs. The channel width and length of the device were 340 μm and 4.9 μm, respectively. An Agilent B1500A semiconductor parameter analyzer was used to measure the values. The transfer curves were measured at V_{DS} = 10 V, using single sweep which starts from V_{GS} = -20 to 20 V with an interval of 0.2 V. V_{TH}, mobility, and sub-threshold slope (SS) at V_{TS} = 0V are listed in Table 3.1.

V_{TH} and SS of double gate TFT were similar to those of single gate TFT. V_{TH} of single and double gate TFT were -0.58 and -0.53 V, and SS were 0.39 and 0.40 A/dec, respectively. SS was not significantly influenced by V_{TS}. V_{TH} was extracted by the constant current method at 1 nA. However, the mobility of double gate TFT was 3.58 cm^2/Vs which is only 52% of 6.94 cm^2/Vs of single gate TFT. In double gate TFT, not only bottom gate but also top gate controls the IGZO channel [92]. The equivalent circuit is shown in Figure 3.3. When top gate is connected to bottom gate or biased by the high value of V_{TS}, an additional electron channel is induced at back channel, and the on-current is increased. On

the contrary, negative V_{TS} or V_{TS} lower than V_{GS} would disturb a bottom gate inducing channel, and the extracted mobility of double gate TFT would be smaller than single gate TFT. This mobility characteristic should be considered when the double gate TFT substitutes for the single gate TFT in the circuit. In the integrated shift register, mobility is a critical factor for driving TFT which has to charge the gate load during several or tens of microseconds. However, as for switching TFTs, mobility is less important than V_{TH}.

When V_{TS} changes from -5 to 5 V, parallel shift of transfer curve was observed. Figure 3.4 shows that V_{TH} is shifted linearly with a slope of -1.25V/V by V_{TS}. The slope decreases when the thickness of top gate insulator increases.

Negative shift of V_{TH} causes the increase of leakage current, while positive shift lowers an on-current level and does not produce a signal. Negative shift is usually observed at an initial state because it is caused by an increase in ambient temperature and process fluctuation. Positive shift is caused by the electrical stress in the circuit operation. A TFT large enough can prevent malfunction caused by positive shift only when V_{TH} at initial condition is not negative. This is because the negative V_{TH} with a large TFT increases leakage current of the circuit. Therefore, V_{TH} compensation for the negative shift is very important in improving circuit stability and increasing yield.

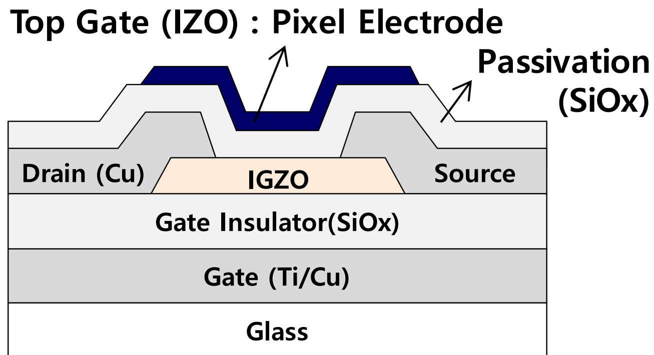
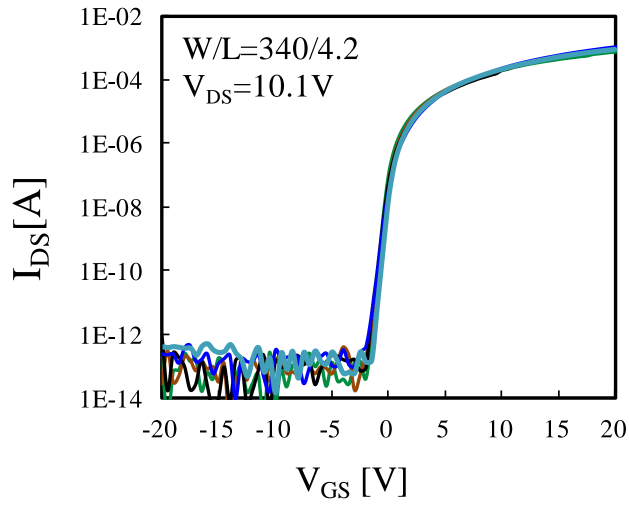
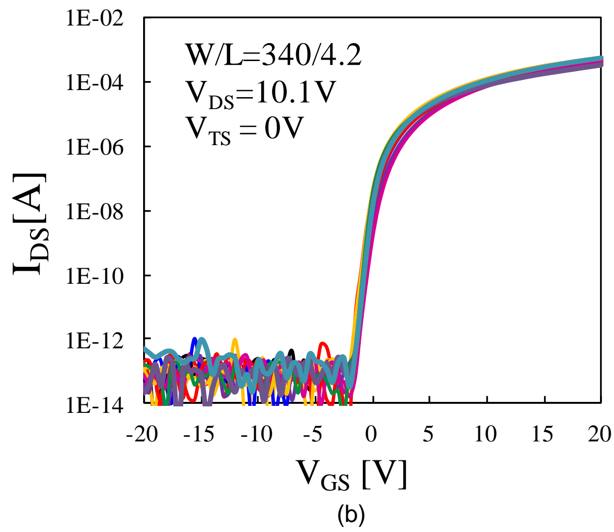


Figure 3.1 Cross-section of top gate IGZO TFTs.



(a)



(b)

Figure 3.2 Transfer curve of (a) single and (b) double gate TFT.

Table 3.1 Characteristics of single and double gate TFTs.

	Single Gate	Double Gate (V_{TS} = 0 V)
V_{TH} (@1nA)	-0.58	-0.53
Mobility (cm^2/Vs)	6.94	3.58
SS(10pA)	0.39	0.40

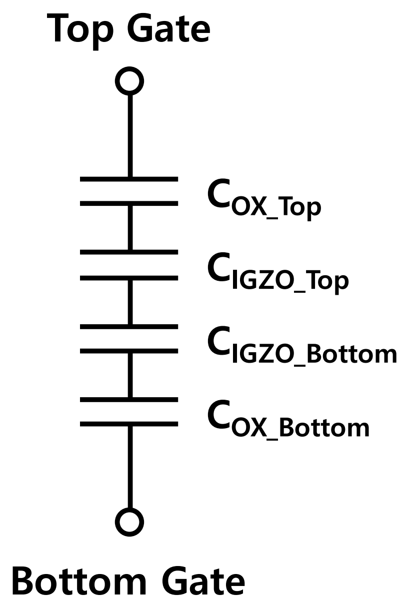
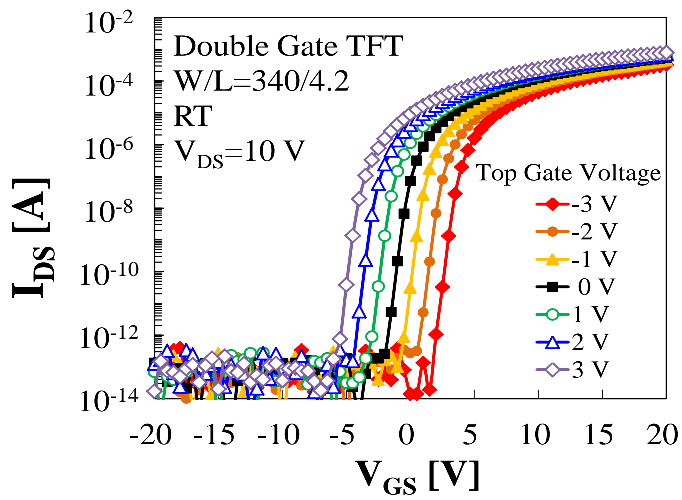
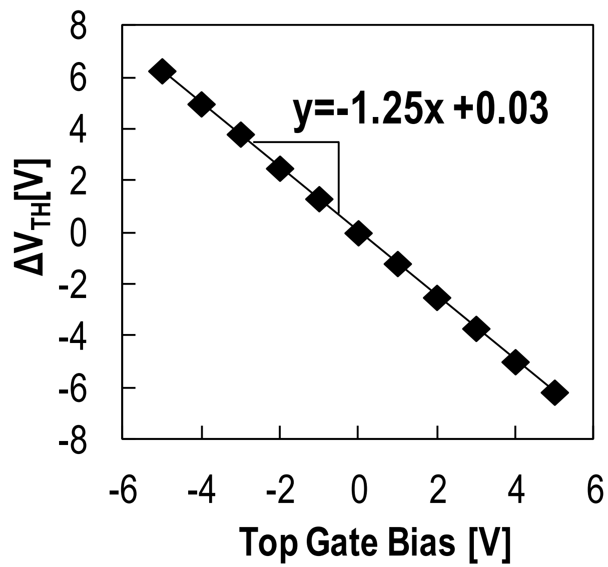


Figure 3.3 Equivalent capacitor circuit of double gate TFT [92].



(a)



(b)

Figure 3.4 (a) Transfer curve and V_{TH} change of double gate TFT according to V_{TS}.

3.3 Design of New shift register

3.3.1 Simulation Result of Conventional shift register

Before adopting the double gate TFT to a circuit, a simulation of conventional shift register circuit (Figure 3.5 [93]) was analyzed to find out which TFTs cause malfunction with a negative V_{TH} shift. In this circuit, an unit stage uses one clock signal: odd and even stages are connected to CKV and CKVB, respectively. CKV and CKVB are the clock signals for the shift register which are produced by power management IC (PMIC) using high and low DC voltages, V_{ON} and V_{SS2}. Figure 3.5 shows the odd stage circuit. When the signal from the previous stage (CR[N-1]) charges gate node of T1 (Q-node) through T4, T1 is turned on and bootstrapped by CKV. During this interval, CKV passes through T1 and T15, and thus the gate output signal (G_{OUT}) and the carry signal to the next stage (CR[N]) are produced. At first, Q-node is charged by the STVP signal from T-con which is a start signal of 1 frame. Then, Q-node, G_{OUT}, CR node are discharged when CR[N+1] turns on T9, 2, 17. The timing of those signals is listed in Figure 3.6. Other TFTs are present to keep the voltage of G_{OUT} low. T12, 7, 8, and 13 are Inverter with CKV source and CR[N] input. When CKV is high, Q-node, G_{OUT}, and CR node are supposed to be coupled up by CKV. However, the inverter output turns on T10, 3, and 11 at the time of CKV high so that CKV ripple can be discharged immediately. The inverter output is low only when CR[N] is high enough for Q-node charging. In this circuit, T1 is turned off by $V_{GS} = V_{SS2} - V_{SS1}$ ($V_{SS1} > V_{SS2}$), Therefore, a margin of negative V_{TH} shift for T1 is $V_{SS2} - V_{SS1} + V_{TH}$.

The SPICE model parameters were extracted by measuring the fabricated IGZO TFTs and are listed in Appendix A. The voltages are -11 V for V_{SS1}, -14 V for V_{SS2}, and -14V, -10 V with 27.36 kHz (for CKV and CKVB). When ΔV_{TH} is -1.8V, G_{OUT} is

distorted, and next stages cannot produce a signal. The results are also shown in Figure 3.6. Even though T11 discharges the CR node, the ripple is observed because T15 passed CKV due to a negative value of V_{TH}. This ripple turns on T9 and discharges Q-node. Therefore, T1 cannot produce G_{OUT} and CR for the next stage.

When V_{TH} is negatively shifted, TFTs are slightly turned on at V_{GS}=0V. It causes the increase of not only leakage current but also CKV coupled ripple because CKV passes through negatively shifted TFT. The ripple turns on TFT severely. This phenomenon can be observed as a gate output distortion and an increase of power consumption of the shift register. Figure 3.7 shows simulation result of power consumption of T4, T15, Inverter and other TFTs. The power consumption of T15 and inverter significantly increased with V_{TH} shift. In T15, power consumption increases with passing CKV signal. For the inverter, CKV-to-V_{SS2} leakage current is increased by negative V_{TH} shift. From the result, it was found that V_{TH} compensation of T15 and the inverter is quite effective in improving the stability of the circuit.

Power consumption is an important factor in V_{TH} compensation because it is one of the methods to measure the instability of the shift register. Before the gate output distortion occurs, V_{TH} compensation with a proper value should be followed by monitoring power consumption.

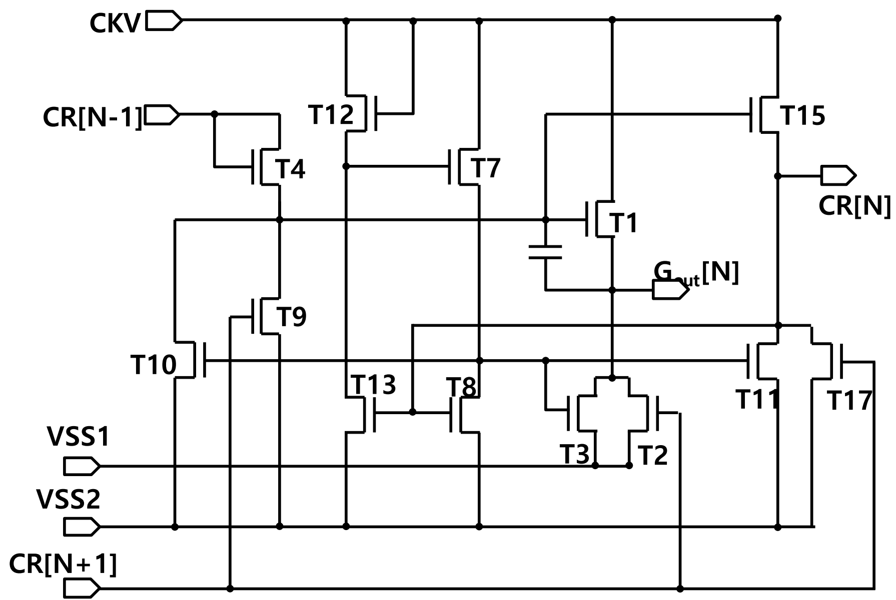


Figure 3.5 Conventional shift register circuit structure [93].

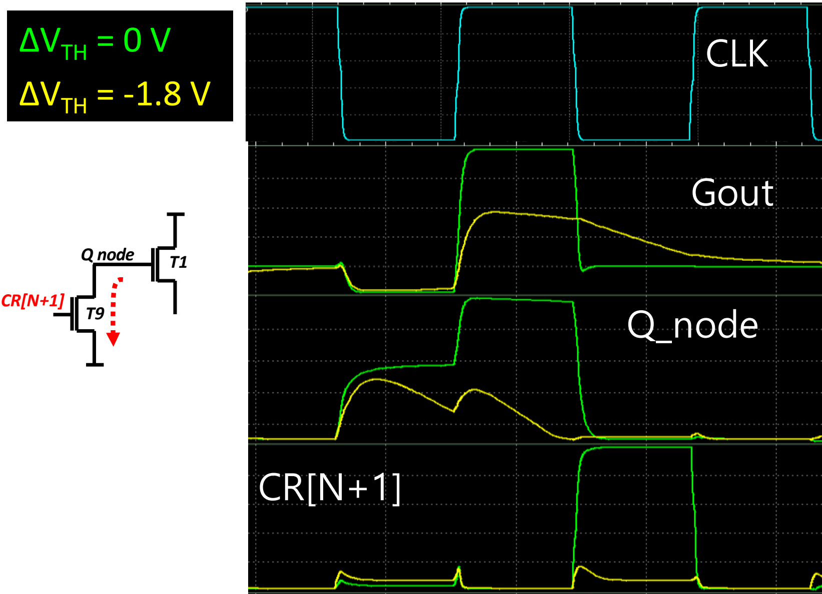


Figure 3.6 Simulation result of conventional shift register circuit.

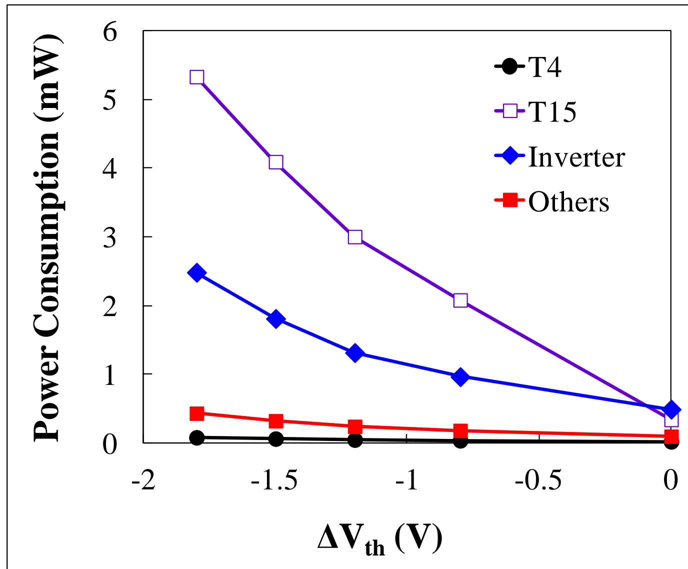


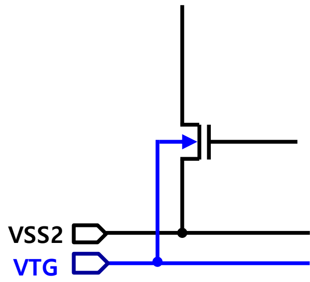
Figure 3.7 Simulation result of power consumption of each circuit block.

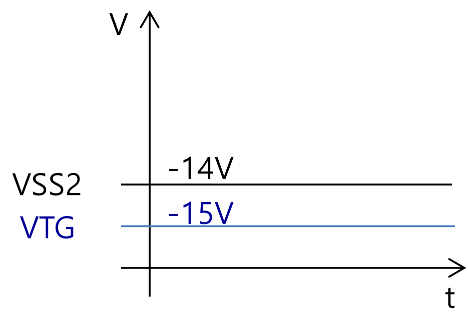
3.3.2 New shift register using Double Gate TFT

In double gate TFT, V_{TH} decreases when the top gate is larger than the source voltage and increases when the top gate is smaller than the source voltage. When the source node of TFT is connected to a DC voltage source such as V_{SS1} and V_{SS2}, top gate can be applied to an additional DC line. For example, if V_{TS}=-1 V is required, top gate (V_{TG}) 1V lower than V_{SS2} should be applied as shown in Figure 3.8. On the other hand, top gate bias has to be changed at the transition of source node to keep V_{TS} the same. An example of this case is shown in Figure 3.9. In the shift register circuit, CKV signal passes through TFT to produce G_{OUT} or CR signals. When T1 or T15 is turned on, source node will increase from -14 V to 10 V. If a constant top gate bias is applied to T15, V_{TS} decreases from -1 V to -25 V. It means that ΔV_{TH} increases to 25x1.25 V from 1x1.25V. In this condition, signal is not produced because TFT cannot be turned on. To avoid over-compensating, top gate bias must be changed at the transition of source node. In the shift register circuit, G_{OUT} and CR signals are created line by line. Therefore, a function that changes the top gate voltage should be added to the unit circuit. A circuit structure in Figure 3.10 is designed to change the top gate node of T15 line by line. The top gate node of T15 is connected to CKV by turning on T30. As a result, V_{TS} is 0 V when the source node of TFT is changed. Then, V_{TG} can be kept after T15 turns off. If V_{TS} equals 0 V, the top gate cannot compensate for the negative V_{TH} shift. However, negative V_{TH} shift facilitates transferring CKV to CR node with an increasing TFT current. Thus, the circuit in Figure 3.10 can be applied to the shift register employing double gate TFT.

Figure 3.11 is the proposed shift register circuit, and Figure 3.12 is the operational timing diagram. As discussed in 3.3.1, T15 and the inverter should be substituted with a double gate TFT. In the inverter, the amount of leakage

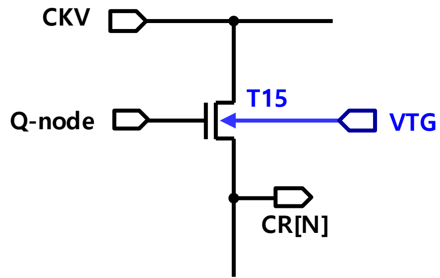
current can be decreased by V_{TH} compensation of pull-down TFT only because it blocks the current flow. Thus, only T8 and 13 are replaced with the double gate TFT. In this case, the source nodes of both TFTs are connected to V_{SS2}, so V_{TG} is directly connected to the top gate node. On the other hand, additional TFTs, T30 and T31, are required to adopt double gate TFT to T15. T30 increases the top gate of T15 with Q-node charge, and T31 keeps it at V_{TG} with an inverter output. When T30 is turned on, T31 is also opened with $V_{GS} = V_{SS2}-V_{TG}$. Therefore, the size of T31 should be small compared to T30. In this study, T30 is 3 times the size of T31.





Always VTS = -1 V

Figure 3.8 Circuit structure and timing diagram when double gate TFT is applied to where source node of TFT is connected to DC voltage source.



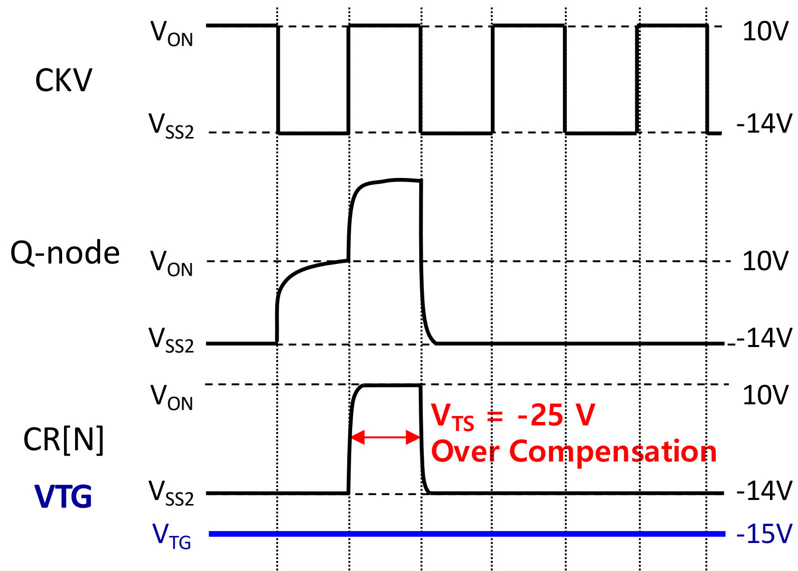


Figure 3.9 Example of when the source of TFT is changed.

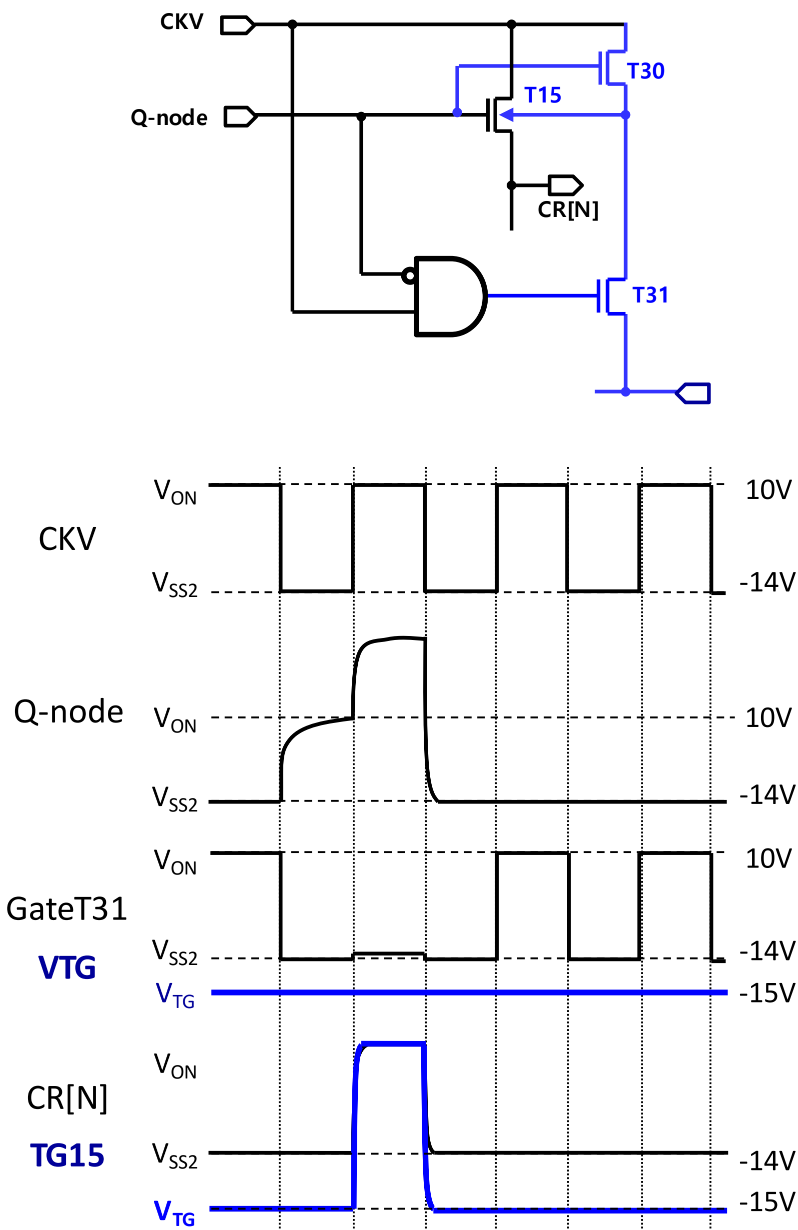


Figure 3.10 Circuit structure and timing diagram of double gate TFT whose top gate voltage is changed with a change in source node.

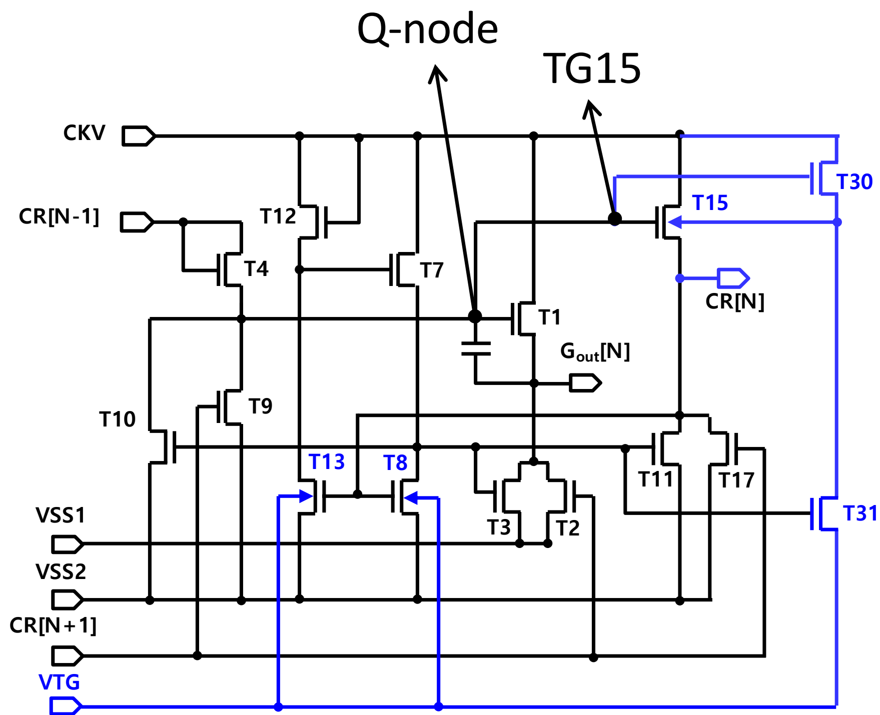


Figure 3.11 Proposed shift register circuit structure.

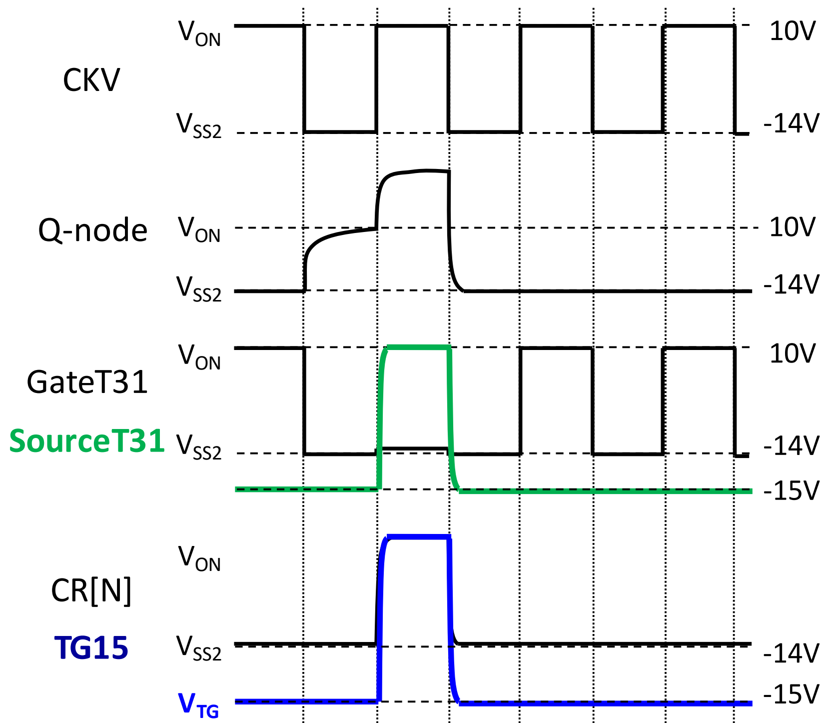


Figure 3.12 Timing diagram of a proposed shift register.

3.3.3 Simulation Modeling of Double Gate TFT

To verify the proposed shift register with spice simulation, device model of double gate TFT is required. However, conventional TFT models are not suitable for double gate TFT because conventional 4-terminal element is for drain, gate, source, and substrate electrode which is directly contact to semiconductor without insulator. In double gate TFT, there is insulator layer between active layer and top gate. Electron channel is induced at top gate side by positive bias and negative bias affects the electrical field of bottom gate with causing V_{TH} increase. On the other hand, conventional 4-terminal element like MOSFET has completely different device mechanism. According to substrate bias, V_{TH} is changed like double gate TFT. However, there is a current flow through the substrate.

From the experimental results, it was found that V_{TH} is linearly change with the ratio of -1.25 V/V depending on V_{TS}. If double gate TFTs replaces with the TFTs whose source node is connected to DC voltage, only V_{TH} parameter in the library should be modified. During circuit simulation, V_{TS} of double gate TFT is constant. However, when top gate bias and V_{TS} is changed during circuit operation, V_{TH} of device library cannot be modified in simulation progress. The device model applying the V_{TH} change during the simulation progress is required.

V_{TH} change depending on V_{TS} means the parallel shift of transfer curve according to V_{TS} as shown in Figure 3.14. It also means that there is additional gate bias as much as $-1.25\times V_{TS}$ to conventional TFT. From this, the voltage-controlled voltage source is used in double gate TFT model. As shown in Figure 3.14, $1.25\times V_{TS}$ is additionally applied to gate node of TFT.

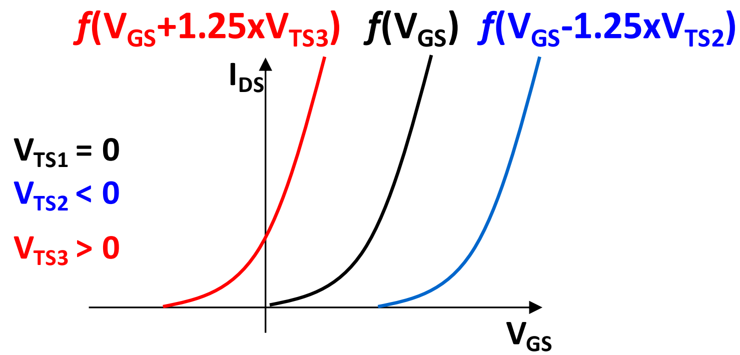


Figure 3.13 Schematic of V_{TH} shift according to top gate-to-source voltage (V_{TS}) in double gate TFT.

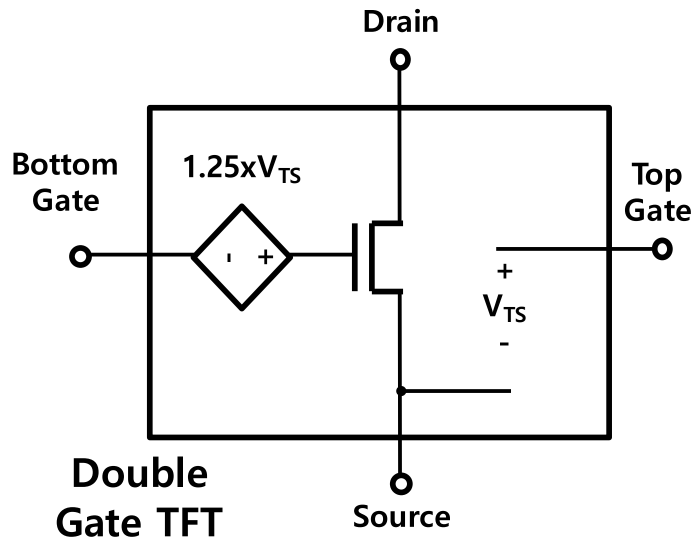


Figure 3.14 Schematic of double gate TFT model for spice simulation.

3.3.4 Simulation and Experimental Result

Using double gate TFT model in 3.3.3, simulation of the proposed shift register was performed. To compensate V_{TH} shift, $V_{TS} = \Delta V_{TH}$ /-1.25 was applied. Figure 3.15 shows that the proposed shift register is more stable than the conventional in the same negative V_{TH} shift condition, ΔV_{TH} = -1.8 V. In conventional shift register, G_{OUT} showed abnormal shape or kept low voltage in the middle of active frame time. Although there is small distortion in G_{OUT} in the proposed one, it is enough to turn on pixel TFTs. This is because CR ripple from CKV decreases with the V_{TH} compensation of T15. In the proposed circuit, the ripple of CR barely increases under negative V_{TH} shift, while it increases as much as turning-on T9 in the conventional one. In the circuit, T30 pull-up top gate bias of T15 at CR transition to create normal CR output and T31 pull-down to VTG to compensate T15 negative shift. Simulation result of top gate of T15 is also shown in Figure 3.15. Top gate bias is V_{ON} when Q-node turns on T30 and CKV is transferred. Under ΔV_{TH} =0 V it keeps V_{ON} during gate on time, while it decreases due to slightly turned-on T31 (V_{ON} is DC voltage from DC/DC and CKV is generated using V_{ON} and V_{SS2}). This could be another leakage path in circuit, so that width of T30 and T31 should be as small as possible. When CR[N] is discharged by CR[N+1], top gate node is not completely pulled down because both T30 and 31 is turned off. During the falling time of Q-node, top gate is discharged through CKV transition to low voltage. Then, T31 pull down top gate node to V_{TG} with inverter output. Inverter output is high when CKV is high and CR is low.

IGZO TFT shift register employing double gate TFT was fabricated. The channel widths of TFTs are 700 μm (for T1), 120 μm (for T4), 10 μm (for T8), 20 μm (for T13), 160 μm (for T15), 30 μm (for T30) and 10 μm (for T31), respectively. The channel lengths of all TFTs are 4.6 μm. Capacitance of T1 is 1.6pF.

Figure 3.16 (a) and (b) shows the optical images of the conventional and proposed shift register circuit. There are three input signals, CKV, CKVB, and STVP and three power sources, VSS1, VSS2 and VTG to operate the shift register. STVP is a start signal, which charges Q-node through T4 at the first stage. Input signals are -14 to 10 V, and VSS1 and VSS2 are -11 and -14 V, respectively. Through PMIC, a digital clock is level-shifted to CKV, CKVB, STVP using V_{ON} = 10 V and V_{SS2} = -14 V. Block diagram of shift register system is shown in Figure 3.17. Shift register stages are connected alternatively to CKV and CKVB.

From the G_{OUT} results in Figure 3.18 and Figure 3.19, it is found that the conventional and proposed shift register circuits are successfully fabricated. The results were measured at room temperature and V_{TG} was -14V which is same with V_{SS2}. As discussed in 3.3.1, power consumption is the important factor to compensate V_{TH} because the increase of power consumption is observed before G_{OUT} is distorted. Figure 3.20 is the result of current dissipation of shift register according to V_{TG}. These are average current values which are dissipated from V_{ON}, V_{SS1}, V_{SS2}, and V_{TG}, respectively. As V_{TG} increases more than near V_{SS2}, V_{ON}-to-V_{SS2} current increases due to V_{TH} decrease, so that V_{ON} current increases. When V_{TG} decreases, the leakage current in the additional 2T, T30 and 31, increases,. Therefore, V_{ON} current increases with V_{ON}-to-V_{TG} current although V_{ON}-to-V_{SS2} current is decreased by V_{TH} increases. During this experiment, the distortion of G_{OUT} was not observed. However, current increase of circuit may cause the degradation of TFT, so that the optimum V_{TG} having minimum V_{ON} current should be applied. Figure 3.21 shows the I_{VON}-V_{TG} characteristics of five samples. Even though these were deposited by the same process condition, optimum V_{TG} varies in different samples due to the process fluctuation. In addition, the optimum V_{TG} will be shifted with V_{TH} change by temperature or electrical stress. The optimum V_{TG} varies from product to product and changes continuously during display

driving. Therefore, driving system suitable for the proposed shift register is required to search optimum V_{TG} in real time.

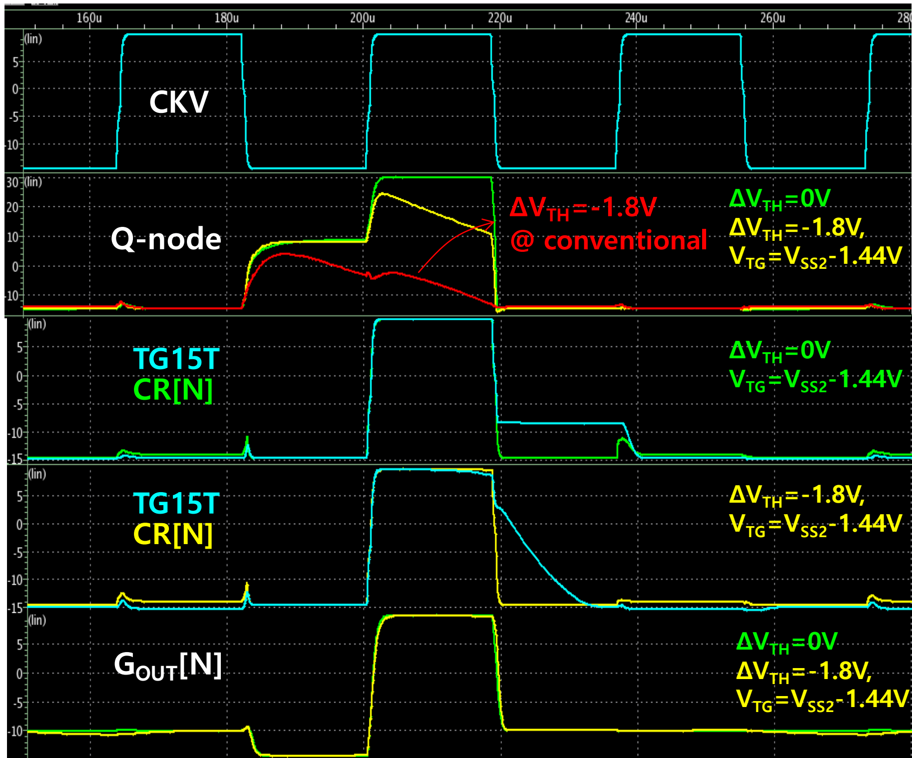


Figure 3.15 Simulation result of proposed shift register circuit.

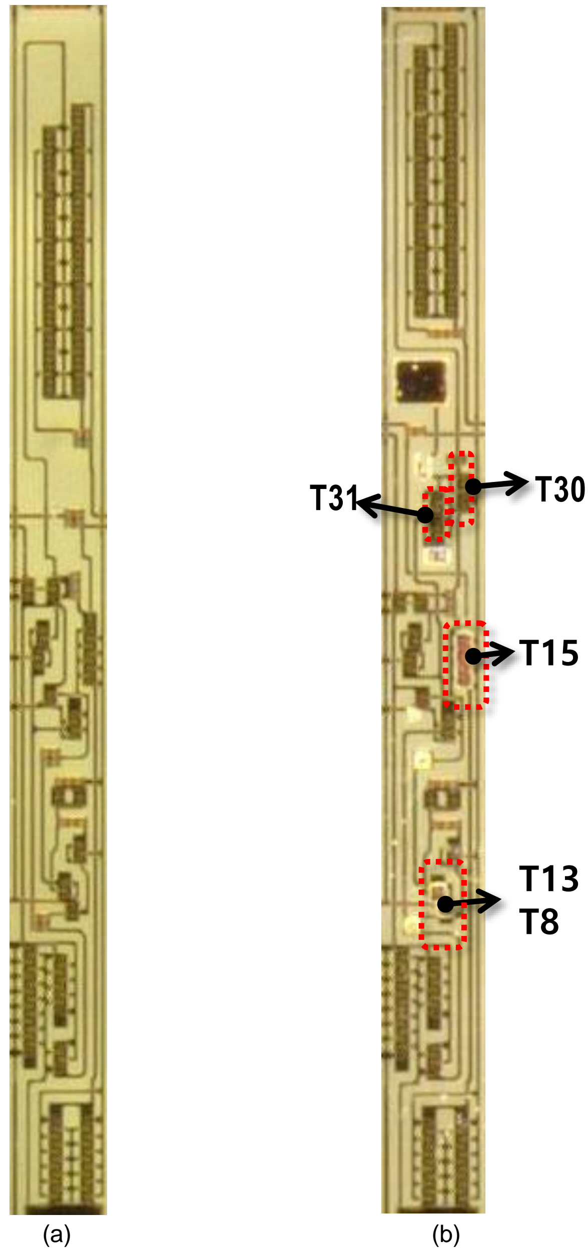


Figure 3.16 Optical image of fabricated (a) conventional and (b) proposed shift register

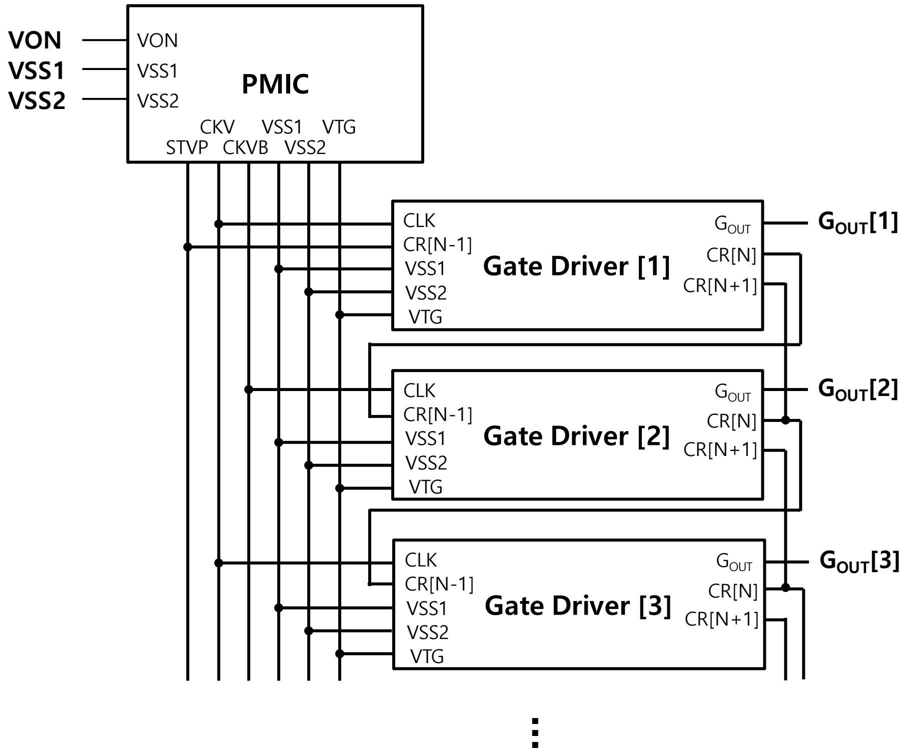


Figure 3.17 Block diagram of shift register system.

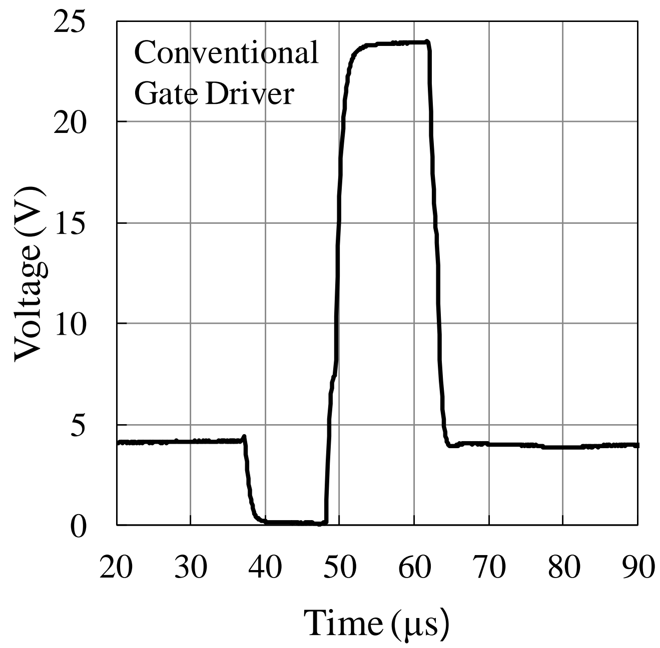


Figure 3.18 Experimental result of conventional shift register output.

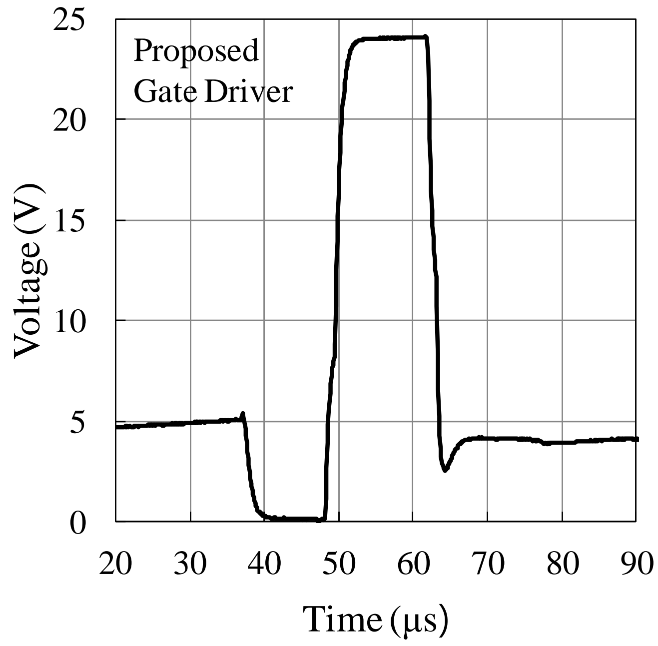


Figure 3.19 Experimental result of proposed shift register output.

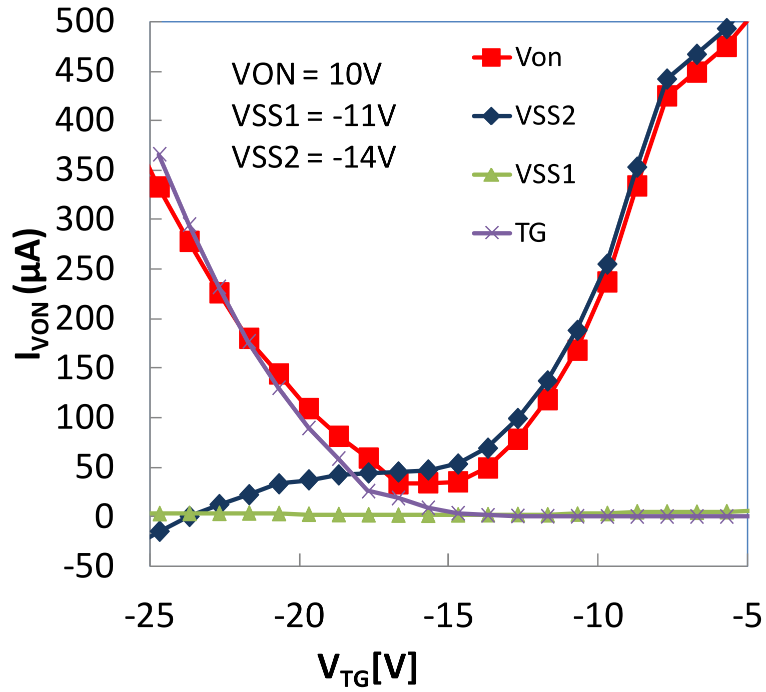


Figure 3.20 Current of voltage source of proposed shift register according to top gate voltage (V_{TG})

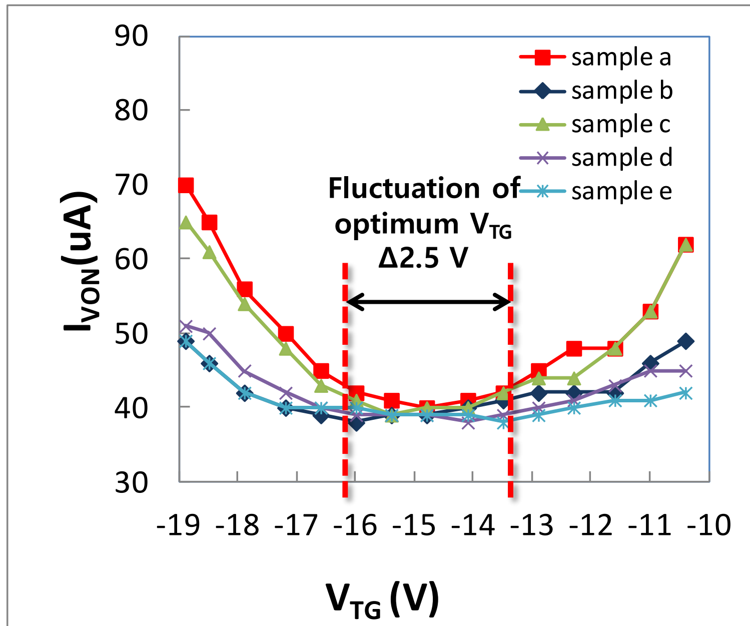


Figure 3.21 Fluctuation of optimum V_{TG}.

Chapter 4 Real Time Current-Sensing Feedback Compensation System

In order to drive the conventional shift register, a level shifter, digital circuits such as timing controller, and DC power sources such as V_{ON} and V_{SS} are required. The level shifter converts the voltage levels in the digital clock domain to analog levels suitable for the shift register employing double-gate TFTs.

In this chapter, real-time current sensing feedback system is designed and verified to improve both stability and power consumption of the shift register. The optimum V_{TG} can be varied by the product to product so that an optimal point searching (OPS) algorithm is proposed to decide the top gate voltage which can minimize the current of the shift register. An optimized top gate voltage is obtained by monitoring the current consumption of the shift register. Then, the adjusted top gate voltage (V_{TG}) using the proposed optimizing algorithm is applied to integrated shift register.

4.1 Overview

In this chapter, optimum V_{TG} varies in different samples about 2.5V due to the process fluctuation even though the samples are deposited under the same process condition. In addition, the optimum V_{TG} is shifted with the V_{TH} change by an elevated temperature or an electrical stress. In other words, the optimum V_{TG} varies from product to product and changes continuously over the lifetime of the display. Therefore, the feedback driving system suitable for the proposed shift register is required to search the optimum V_{TG} for the minimum the current of shift register. The system has two main functions; the first is to sense the current of shift register and the second is the searching algorithm for finding the optimum V_{TG}, as shown in Figure 4.1.

Now, the driving architecture of the feedback system will be considered. Driving circuit is composed of 3-driving circuit and 1-algorithm blocks. Figure 4.2 shows an overall flow of driving architecture. 3-driving circuit blocks are current sensor, AD Converter, and DA converter. Each circuit was also optimized for power consumption and accuracy. And, an optimizing algorithm block was made up of a digital circuit. First, the information about the degradation of the shift register can be sensed by the current of the shift register. In this step, the sensed current is converted to analog voltage level. Second, ADC block converts this voltage to 8-bit digital value for algorithm processing. Next, in algorithm block, to minimize the current of shift register, an optimal digital value is descried using searching algorithm processing. After data processing, in the last step, the optimal top-gate analog voltage value is produced by current steering type DA converter. Depending on the condition of shift register, period of the feedback compensation can be programmed. In this chapter, the analog block for feedback circuit and digital block for searching algorithm will be discussed in detail.

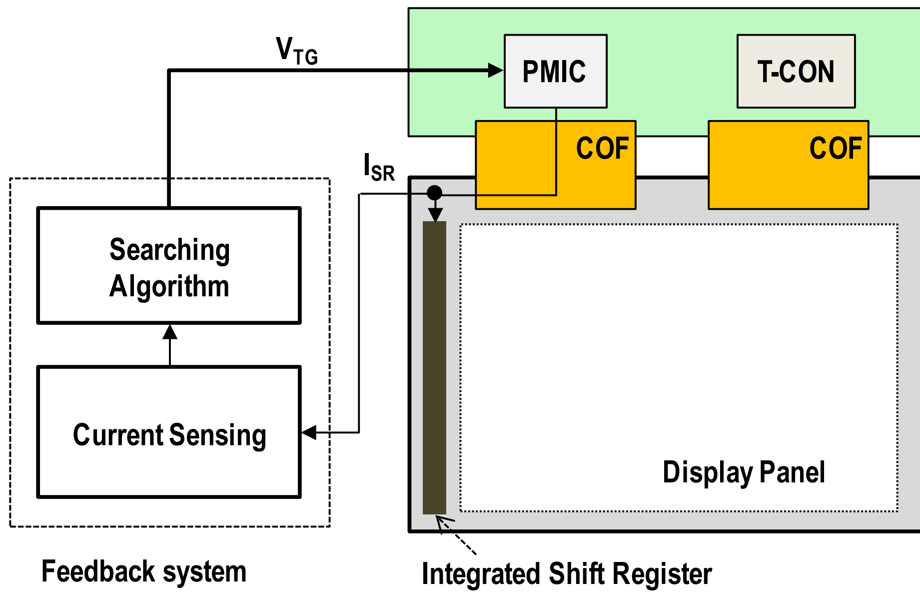
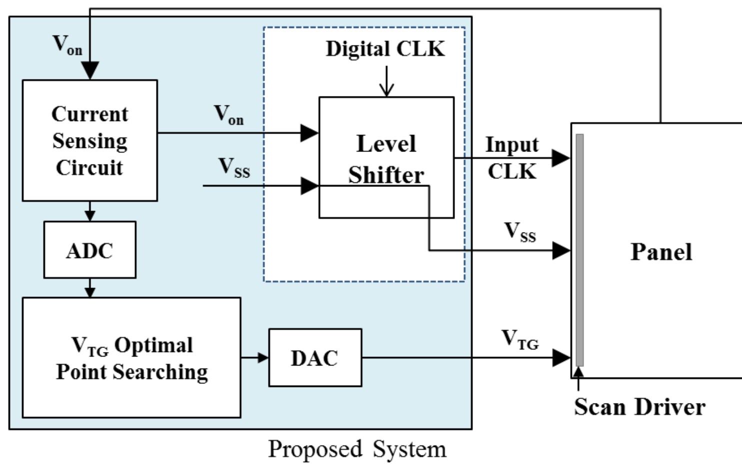


Figure 4.1 Proposed current sensing feedback system.

4.2 System Architecture

Figure 4.2 shows the concept block diagram of shift register degradation compensation using double gate TFT. It consists of shift register, current sensing circuit, ADC, optimal point searching algorithm and DAC. To compensate the degradation of the shift register, proposed system gathers current level at Von voltage which is gate bias voltage of active TFTs. The shift register of display panel needs the high level gate voltage to operate the active TFT in saturation region and this high level voltage(I_{VON}) is supplied from PMIC. If the TFTs of shift register are degraded by external environment stress such as electrical bias or thermal stress, the current of Von (I_{VON}) will be changed. Therefore, the current is sensed at Von voltage from PMIC as depicted in Figure 4.3 (a). The current information of Von will be used for reference data to determine top gate voltage in order to compensate V_{TH} shift of the shift register which uses double gate TFTs. And gathered current information is converted to digital value in the ADC step for algorithm processing later. In optimal point searching algorithm step, algorithm finds the V_{TG} which keep the output waveform of shift register stable even if shift register's TFT was degraded. Finally, chosen optimal top gate bias is applied to shift register through digital analog converter.

Figure 4.3 (b) shows the block diagram of one chip IC implementing such functions in real time.



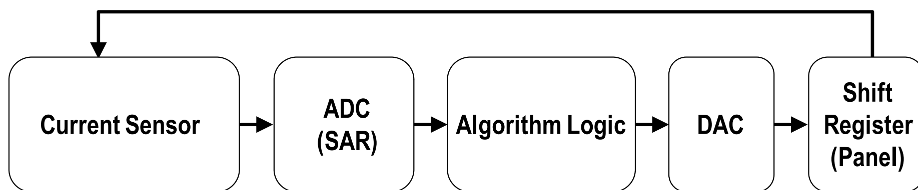
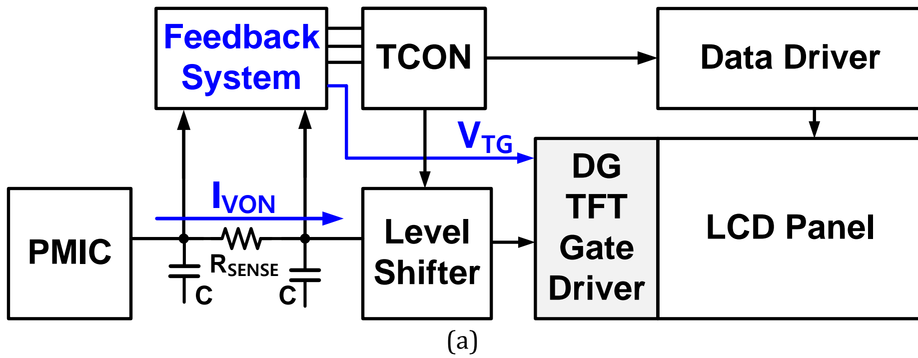
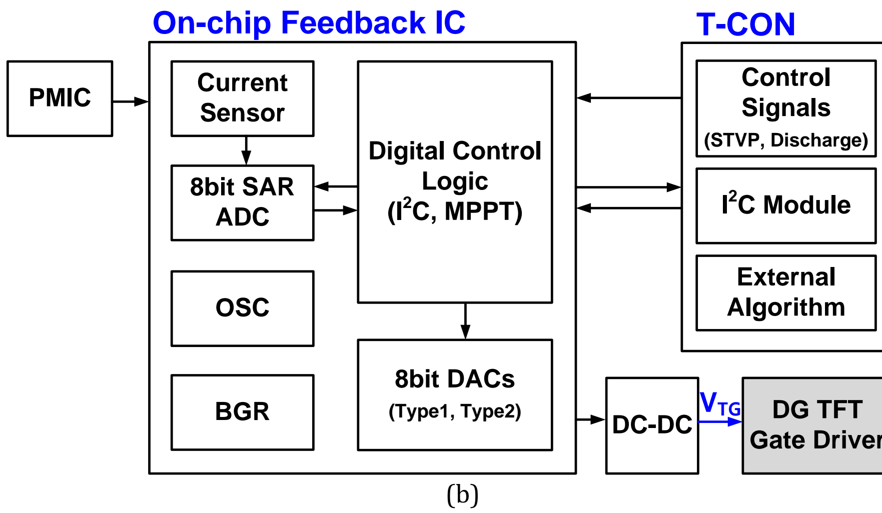


Figure 4.2 The proposed system architecture and flow chart.



(a)



(b)

Figure 4.3 Current sensing between PMIC and level shifter and concept diagram of the one chip feedback IC.

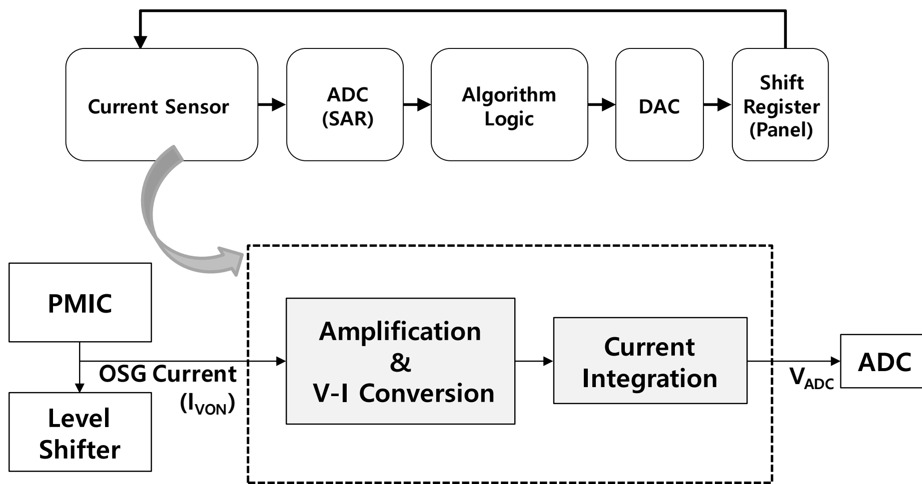
4.3 Circuit Design

4.3.1 Current Sensing Block

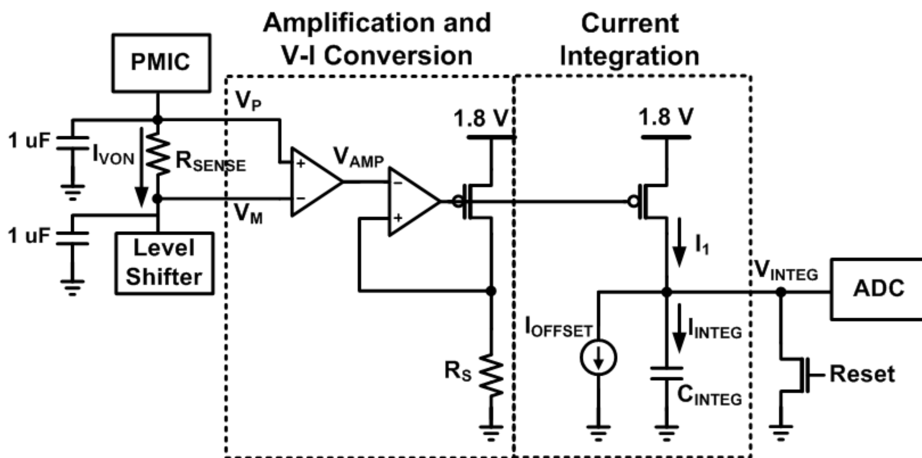
First step for compensating shift register is the current sensing when circuits operate. It should be noted that when V_{th} of shift register is negatively shifted due to the elevated temperature, the current of shift register would be increased so that sensing shift register current is the criteria for the performance of shift register. Current sensing block performs 3 kinds of function which is current monitoring, current integration and conversion to voltage value. Figure 4.4 (a) shows the flow chart of current sensing function.

Figure 4.4 (b) explains the detailed current sensing circuit. First, current sensor and amplification block detects total current which is consumed in shift register. The current is mirrored via sensing resistor (R_{SENSE}) which is located between power generation and shift register (level shifter). In the current integration block, the sensed current is integrated by C_{INT} to generate V_{INT} as the output when the *Reset* signal goes to low and is forwarded to an ADC. At that time, using integration driving method, the immunity against system noise can be obtained. R_{SENSE} and C_{INTEG} are designed two type mode, such as an on-chip and off-chip. The binary-converted current of the shift register is processed by the proposed algorithm in the digital domain for obtaining an optimum V_{TG} and then the result is converted back to analog to generate V_{TG}.

The proposed current sensing circuit is modeled and simulated using H-Spice simulator. The two kinds of differential amplifiers are used. One is N-type, another is P-type. In case of N-type amplifier, common input voltage is 1V, common output voltage is 0.4V, gain is 40. In case of P-type amplifier, common input voltage is 0.4V, common output voltage is 1V, gain is 40.



(a)



(b)

Figure 4.4 Diagram and circuits of current sensing block.

In Figure 4.4(b), R_{SENSE}, R_S and C_{INTEG} are made by discrete chips in printed circuit board (PCB) to ensure flexibility of current sensing feedback system. So, we have to set parameters of discrete off-chips.

First of all, current consumption of OSG TEG should be estimated. OSG current (I_{VON}) of TEG which is composed of 16 stages is normally 500μA in room temperature. And next, RSENSE and Op-AMP gain determine V_{AMP} values. For examples, R_{SENSE}=200ohm and OP-AMP gain=40,

$$V_{DIFF} = 500\mu A \times 200ohm = 100mV$$

$$V_P - V_N = V_{DIFF} \times \left(\frac{1}{10}\right) = 10mV \text{ (for amp common mode level)}$$

$$V_{AMP} = V_{COMMON} + V_{P-N} \times OP - AMP\ gain = 0.4 + 10mV \times 40 = 0.8V$$

And next, minimum and maximum value of C_{INTEG} should be calculated for PCB design. In case of C_{INTEG_MAX},

$$\text{ADC minimum resolution} = \text{ADC input range} \div 2^{\text{data bit}} = \frac{0.8V}{256} = 3.125mV$$

$$\Delta V_{INTEG} \geq 3.125mV \text{ for ADC minimum resolution}$$

$$\Delta V_{INTEG} \left(= \frac{\Delta IINTEG \times t}{C_{INTEG_{MAX}}}\right) \geq 3.125mV, \qquad \text{at } \Delta I_{VON} = 10\mu A$$

$$C_{INETEG_MAX} \leq \frac{\Delta I_{INTEG} \times t}{0.003125} = \frac{1 \times 10^{-4} \times \Delta I_{VON} \times R_S}{0.03125} = 32nF$$

In case of C_{INTEG_MIN},

$$I_{INTEG} \times t = C_{INTEG_{MIN}} \times \Delta V \text{ at } V_{INTEG_{MAX}}$$

$$\Delta V_{INTEG} \leq 0.8V \text{ for ADC input range}$$

$$\frac{I_{INTEG} \times t}{0.8} \leq C_{INTEG_{MIN}}$$

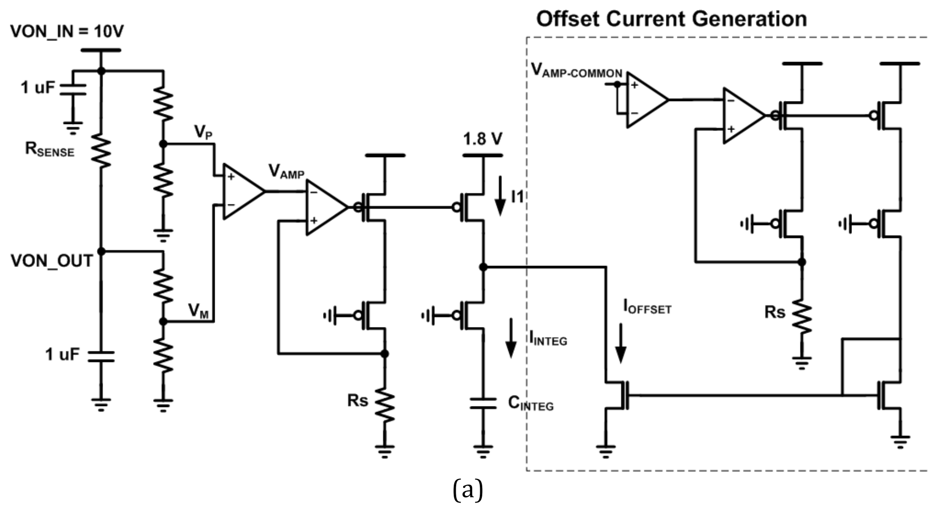
$$\text{At } I_{INTEG_{MAX}} = 32.5\mu A \text{ and } t = 0.5ms, \frac{I_{INTEG} \times t}{0.8} \leq C_{INTEG_{MIN}} = 20nF$$

$$\therefore\ 20nF(Min.) \leq C_{INTEG} \leq 32nF(Max.)$$

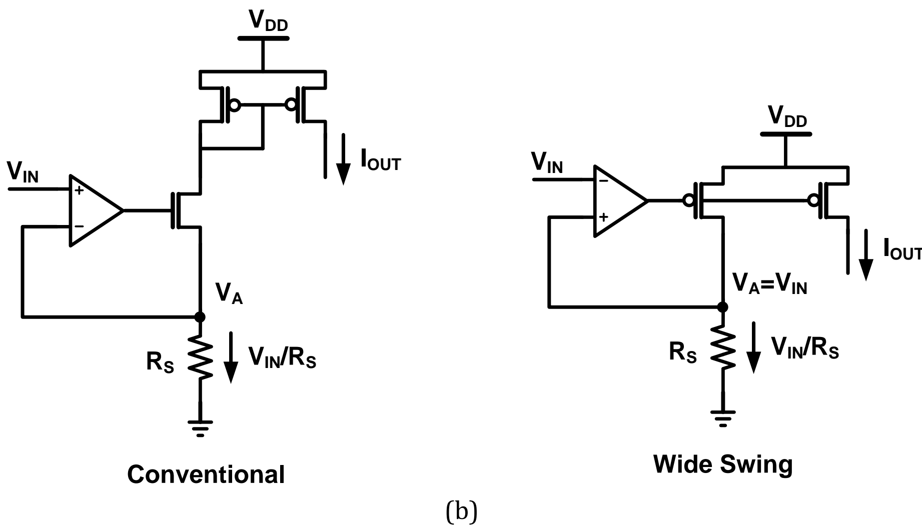
The offset compensation circuit is proposed for removing offset current of sensing circuit and to achieve high accuracy by utilizing duplication method. It is designed for enhancing robustness against the fabrication process variation, and temperature variation. It consists of voltage-dividing resistor, integrating capacitor as shown in Figure 4.5 (a). It is designed that common mode input voltage range of amplifier is 1V.

In addition, the low pass filter is formed by to smooth R_{SENSE} and capacitors on V_{ON_IN} and V_{ON_OUT} to smooth the ripple current waveform at Von. V_{ON_IN} is DC voltage from PMIC and V_{ON_OUT} is input of the level shifter. The ripple current waveform at V_{ON} is caused by the transition of CKV signal and must be smoothed by the low pass filter formed by R_{SENSE} and capacitors on V_{ON_IN} and V_{ON_OUT}.

Figure 4.5 (b) shows the operational trans-conductance amplifier (OTA) and this circuits perform a V-I converter. It is used to make sure of linearity and immunity of current sensing block. In this structure, output current is proportional to Vin/Rs value. First block of Figure 4.5 (b) circuit is conventional scheme based on OTA and voltage swing on V_A is V_{DD}-(V_{th1} + $V_{DS,sat1}$). This conventional OTA circuit is highly linear and has high input impedance but it needs voltage headroom. Second block of Figure 4.5 (b) shows wide swing approach, voltage swing level on Va is $V_{DD} - V_{DS,sat1}$ but there is possibility for T1 to go into the triode state which causes the non linearity. After amplification and V-I conversion using OTA circuit, current integration is processed. Current of OTA is mirrored to integration node which consists of integration capacitor and reset transistor using P-type current mirror circuit. A voltage of integration node is connected to input of AD converter.



(a)



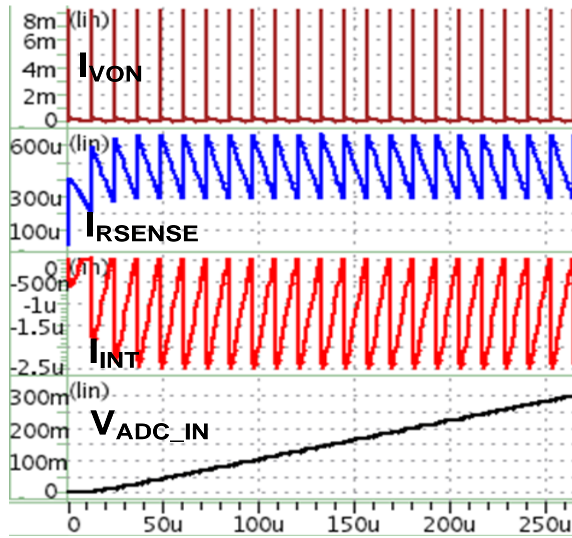
(b)

Figure 4.5 Offset cancellation circuit of the current sensing block and OTA V-I schemes: conventional stage & wide-swing approach.

Transient simulation is conducted under the condition which is R_{SENSE} is 10ohm, temperature is 25°C, integration capacitance is 100pF and top gate voltage is -15.7V. And the simulation result is shown in Figure 4.6 (a). The ripple of current waveform (I_VON) is caused by the transition of CKV signal. In order to make sure of stable current level, the ripple of current should be compensated. So, the capacitors are added to between VON_IN and R_{SENSE}, R_{SENSE} and level shifter for smoothing current ripple. And using offset current cancellation circuit, system accuracy can be enhanced. Using integration capacitor, integrated voltage becomes the output of current sensing block and is delivered to input of ADC block. Figure 4.6 (b) shows the timing of current sensing circuit and ADC block.

Figure 4.7 shows the simulation results for sensing resistor. Input current is modeled based on double gate TFT's characteristic as shown in Figure 4.7(a). According to top gate bias, current on Von is varied. 3 plots in Figure 4.7(b) indicate the integrated voltage level depending on sensing register values; 5, 10, 15ohm at temperature 25℃. To make sure of a wide output voltage range more than 0.5V for the input of AD converter, it is recommended to get a sensing resistor larger than 50 ohm.

Additionally, the output integrated voltage according to temperature is simulated. Input current model which is same with sensing register simulation is chosen. The integrated voltage level is simulated depending on temperature; 25,60,80℃ at sensing register values which is 10 ohm. When the temperature is 80℃, integration voltage range is shifted to lower level as 30mV level than that of 25℃. Wide voltage range of ADC can have immunity against temperature. So, input range of ADC should be designed to make sure of the margin of integration voltage variation depending on temperature.



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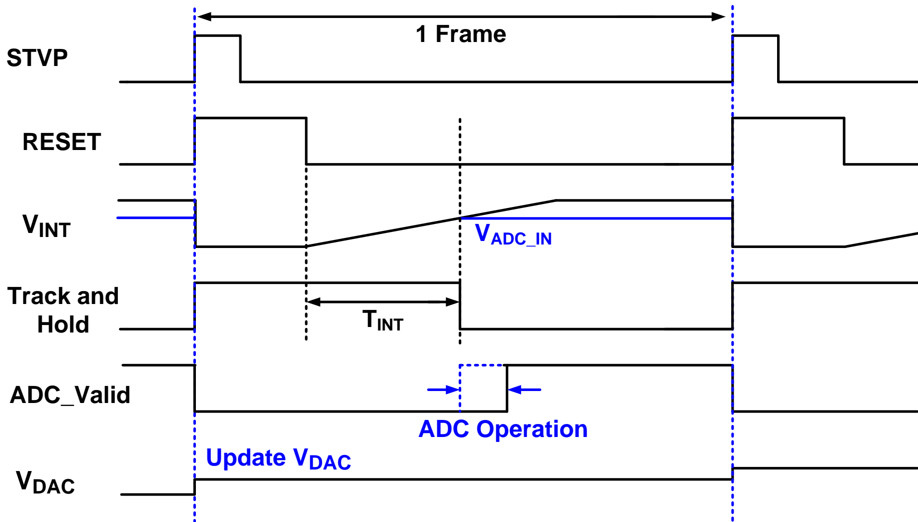

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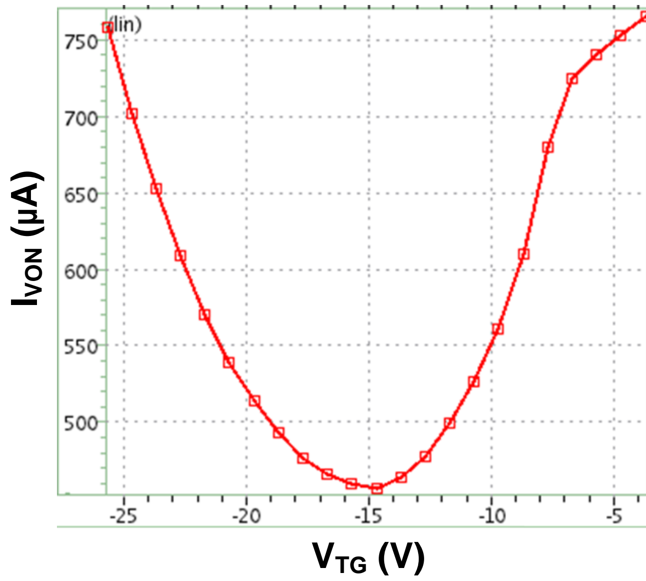
Figure 4.6 Transient simulation results of current sensing block and timing diagram.



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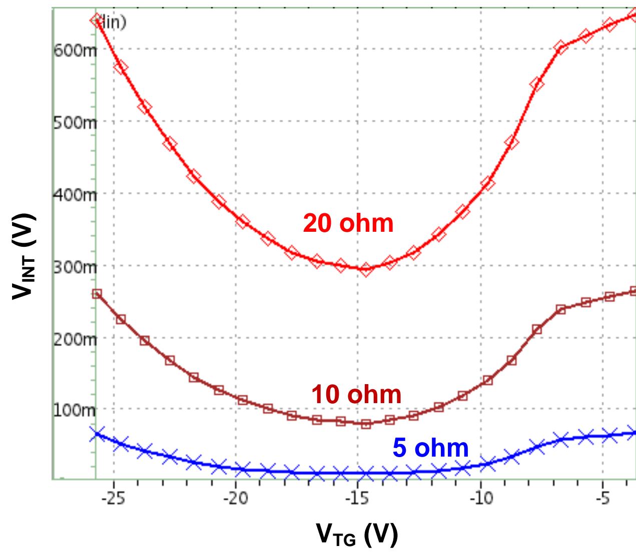

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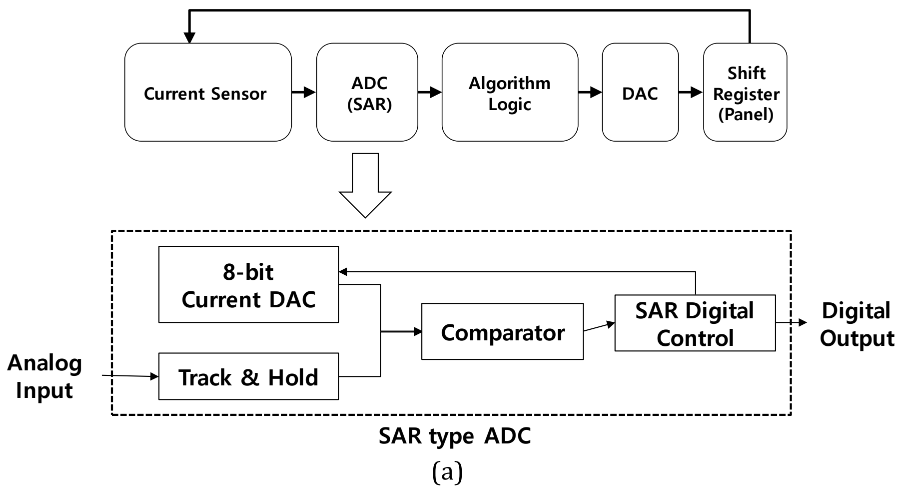
Figure 4.7 Input current model and simulation results depending on sensing resistor values.

4.3.2 ADC/DAC Block

Successive Approximation Register (SAR) type AD Converter is adopted to convert current value gathered from sensing circuit to N-bit digital value for algorithm processing as shown in Figure 4.8 (a). SAR ADC consists of DAC, comparator and track & hold. This AD converter has many advantages, such as high accuracy, small area and low power consumption. The operation of ADC can be explained 3 steps. Firstly, during the sampling period, analog input voltage is held by "Track & Hold circuit block". Second input voltage is compared to the reference voltage in comparator, and finally the register and control logic block in SAR generates new reference data depends on comparator result.

Figure 4.8 (b) describes the detailed block diagram of AD converter system. ADC resolution is 8bit for high accuracy system and input range is 0.0V to 0.8V in 1.8V power supply condition. After "Track & Hold", the input of ADC and reference voltage from current DAC is compared. Depending on the comparison outcome, it eliminates half of the range. One clock cycle is needed per one conversion. It requires N clock cycles for N-bit (speed degradation). SAR type ADC is hardware efficient structure. For example, even though the bit depth of system increases 8 to 10, the hardware of ADC does not need to be increased. But it has a disadvantage in terms of time consuming point of view. When the bit depth of system increases from 8 to 10, the processing time of ADC increases proportionally, that is, from 8 cycles to 10cyles. In addition, Binary conversion method such as SAR type ADC is quite sensitive to errors. When the error happens in MSB data comparison process, it can bring about fatal error and can't reduce the error structurally. This type of ADC has a trade-off relationship between high sampling rate and high resolution. Considering the purpose of the system, the 8-bit resolution of the sensing feedback system is designed.



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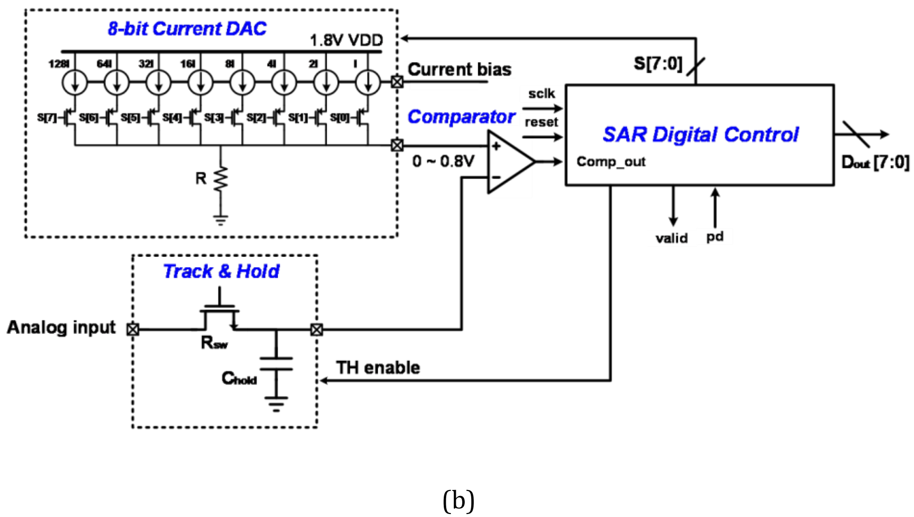


(b)

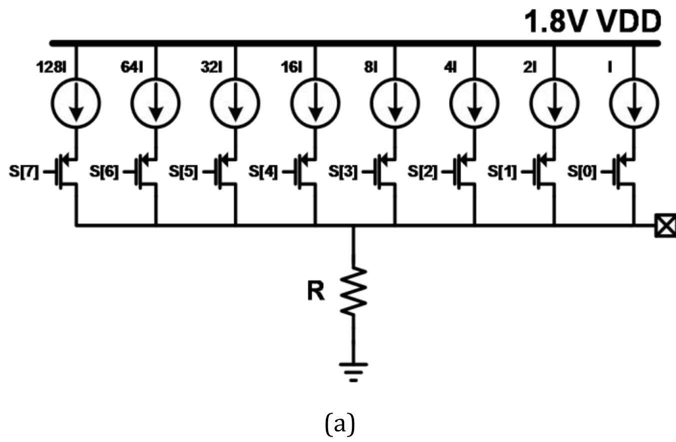
Figure 4.8 Block diagram of SAR type AD Converter.

The operation of SAR type ADC is based on finite state machine and decides the bit value from most significant bit (MSB) to least significant bit (LSB). The operation of binary successive approximation in SAR ADC is simulated.

8bit current DA converter as shown Figure 4.9 (a) is simulated with monolithic code increase input condition and temperature split from 25℃ ~ 100℃. Noise is ultimately limited by the thermal noise generated by passive components such as resistors. It expected that there is trade off relationship between power consumption and temperature variation. And it also expected that there will be process variation issues.

Figure 4.9 (b) shows the simulation result of AD converter system when analog input varies from 0.0V to 0.8V. 8bit current DA converter is adopted for AD converter. Resistor(R) is determined to 5.3 Kohm in current DAC circuit. Estimated power consumption is 271.8 μW.

When the comparator type is selected, several parameters must be the considered while selecting a suitable comparator. For example, while in general comparators are fast, their circuits are not immune to the classic speed-power tradeoff. High speed comparators use transistors with larger aspect ratios and hence also consume more power. By only turning on a comparator at certain intervals, higher accuracy and lower power can be achieved with a dynamic comparator structure, also called a lathed comparator. From a low power point, detailed comparator which is integrated in the current sensing circuit is designed as PMOS type dynamic latched comparator structure.



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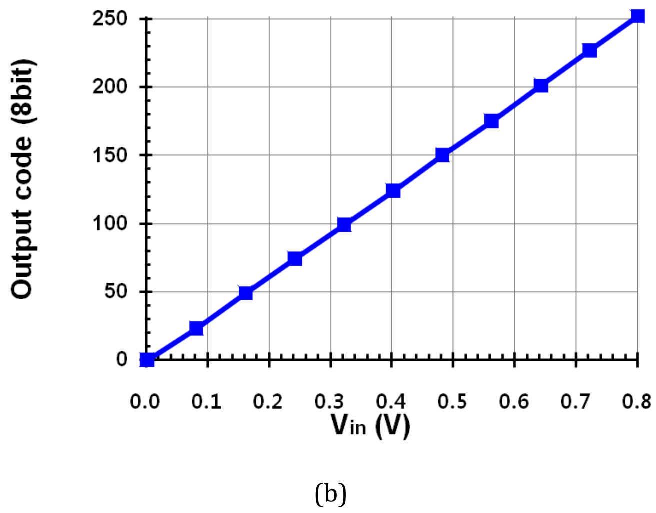

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Figure 4.9 Current DA converter in SAR ADC and Input and output graph of SAR ADC.

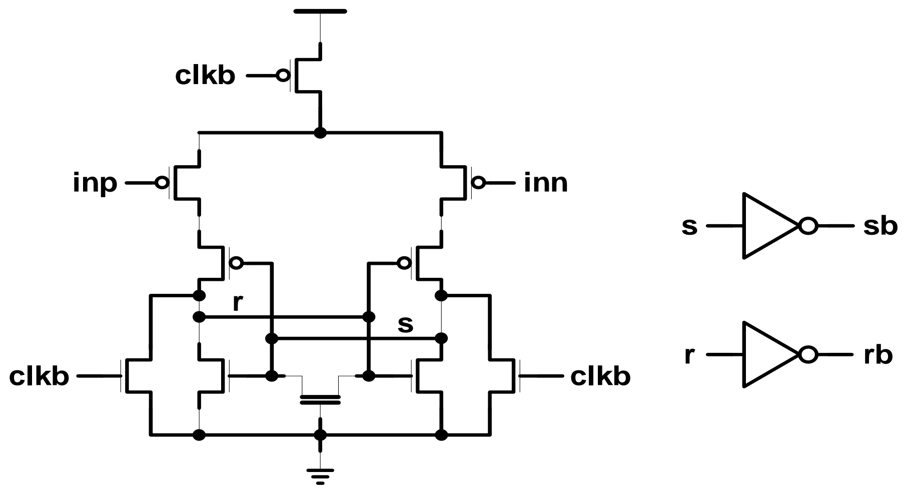


Figure 4.10 Comparator circuit of SAR ADC.

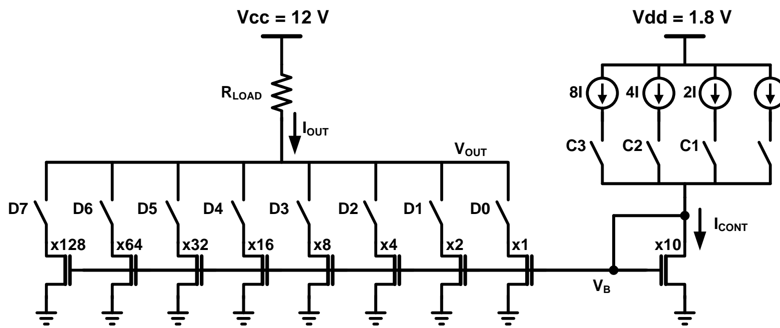


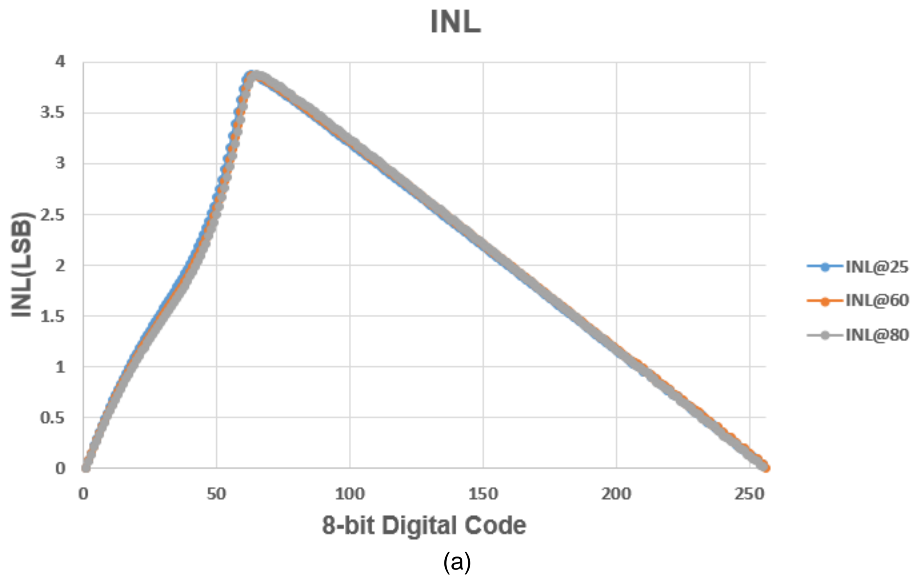
Figure 4.11 Current steering DA converter.

Current steering DA converter is proposed for shift register feedback compensation system. DAC is very important to system performance. The most important characteristics of these devices are resolution, monotonicity and dynamic range. There are important device parameters, such as Differential nonlinearity (DNL), Integral nonlinearity (INL) and thermal noise immunity.

In proposed system, the DAC has 10V dynamic range, 8bit resolution and it designed for low power consumption. And bias voltage generator is adopted to compensate resistor process variation. When load resistor is 62 kohm, maximum output current (I_{OUT}) is estimated to 163uA. Detailed DA converter circuit is shown Figure 4.11. Bias voltage generator can compensate resistor process variation. DAC output of this system has 10V dynamic range, when R_load is 62kΩ and maximum I_{OUT} is 163 μA.

Current steering DA converter is simulated. When input digital code is varied from 0 to 255, Output voltage changed 0V to 12V. So, dynamic range is more than 10V. Figure 4.12 shows simulation result of DA converter depending on temperature.

Reliability of current steering DA converter is also simulated and estimated. Figure 4.12(a) shows, maximum INL is estimated to 3.87 LSB at 25℃, 60℃, 80℃. INL shows how much the DAC transfer characteristic deviated from an ideal one. That is, the ideal characteristic is usually a straight line. INL shows how much the actual voltage at a given code value differs from that line, in LSBs. Maximum DNL is simulated -0.122 LSB, -0.123 LSB and -0.129 LSB at 25℃, 60℃, and 80℃ respectively. Figure 4.12(b) shows DNL simulation result. DNL shows how much two adjacent code analog values deviate from the ideal 1LSB step.



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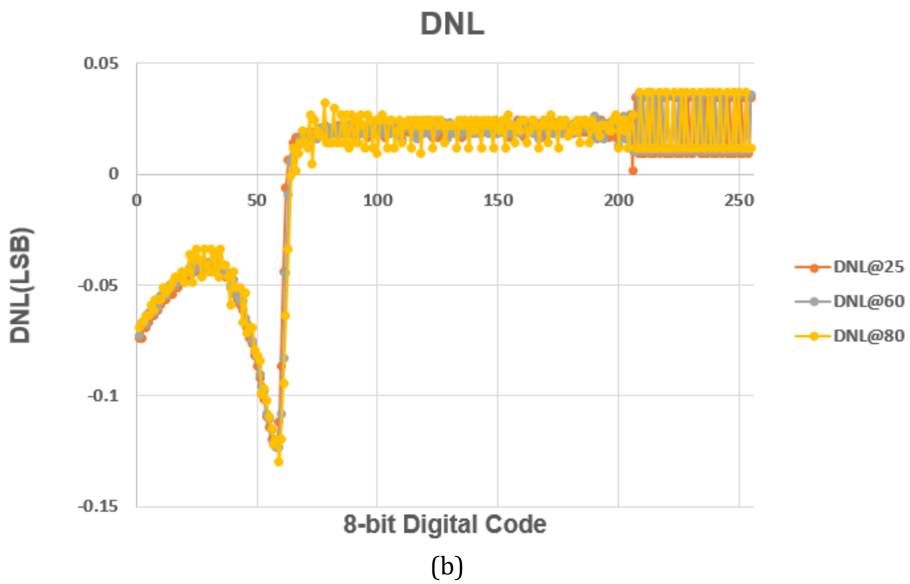


(b)

Figure 4.12 INL/DNL simulation result of DAC depending on temperature.

As mentioned before, passive components such as resisters, capacitors are easy to generate thermal noise and degrade the performance of DAC. Thermal noise in an ideal resistor is approximately white noise, meaning that the power spectral density is nearly constant throughout the frequency spectrum. But, when limited the finite bandwidth, thermal noise has a nearly Gaussian amplitude distribution. In aspect of noise immunity such as thermal, current steering DA converter type 2 is also suggested additionally. It uses control bias voltage and use off chip resistor. Current steering architecture is generally used for high resolution applications. This is because they are better suited low power consumption compared to other architectures, and easy integration in standard digital CMOS technologies which are cheaper. The current steering DAC architecture can be implemented using either binary weighted or thermometer-coded implementations. However, to improve the overall performance, a combination of both architectures is recommended. In proposed system, binary weighted structure is only adopted.

The design goal was 10V dynamic range and 8bit resolution and low power consumption. When R_load is 62kohm, maximum current output (Iout) is expected up to 163.019uA. And maximum power consumption is estimated 2.308mW

Current steering DAC's (Type 2) is simulated. Current range is from 41nA ~ 11.8uA at default setting. Initial condition of bias circuit is that C3 = 0(on), C2 = 1(off), C1 = 1(off), C0 = 1(off).

In DAC circuit, it is important to consider maximum steering current and output node resistor value. It can determine DAC output voltage range. Table 3.1 shows an optimized resistor value depending on maximum current level. The default value of Code is "0111", so default value of resistor is 62kohm.

Table 4.1 Recommendation of resistor value depending on maximum output current.

Code	I_cur (μA)	MAX_I_out (μA)	R (kohm)
1111	-	-	-
1110	0.8	20.6	490.0
1101	1.6	40.9	247.0
1100	2.4	61.3	165.0
1011	3.2	81.6	124.0
1010	4.0	102.0	99.0
1001	4.8	122.6	82.0
1000	5.5	142.7	71.0
0111	6.3	163.0	62.0
0110	7.1	183.1	55.0
0101	7.9	203.4	49.6
0100	8.7	223.5	45.0
0011	9.5	243.9	41.0
0010	10.3	263.9	38.0
0001	11.0	284.0	35.6
0000	11.8	303.9	33.0

In the proposed current sensing feedback system, a stable bias voltage generator circuit should be designed. A band-gap voltage reference circuit as shown in Figure 4.13 is adopted and designed for on-chip bias which is 0.7V and 1.1V level. A band-gap voltage reference is a temperature independent voltage reference circuit widely used in integrated circuits. It produces a constant voltage regardless of power supply variations, temperature changes and circuit loading form a device. It commonly has an output voltage around 1.25V. The voltage difference between two diodes, operated at different current densities, is used to generate a proportional to absolute temperature (PTAT) current in a first resistor. The critical issue in design of band-gap references is power efficiency and size of circuit. As a band-gap reference is generally based on BJT devices and resistors, the total size of circuit could be large and therefore expensive for IC design. Moreover, this type of circuit might consume a lot of power to reach to the desired noise and precision specification.

In case of the bandgap voltage reference in the proposed system, it has only ±1.1% deviation about 1.1V output level in severe condition which is ±10% power(Vdd) Split and 30~80 degrees Celsius range as shown in Figure 4.14. It has only ±0.7% deviation about 0.7V output level in severe condition which is ±10% power(Vdd) Split and 30~80 degrees Celsius range as shown in Figure 4.14.

Oscillation is the repetitive variation, typically in time, of some measure about a central value or between two or more different states. An electronic oscillator is an electronic circuit that produces a periodic, oscillating electronic signal, often a sine wave or a square wave. It converts DC from a power supply to an AC signal. It is widely used in many electronic devices. In oscillator circuit of the proposed system as shown in Figure 4.15, its frequency which range is from 1Hz to 11.8MHz can be controlled by the digital logic.

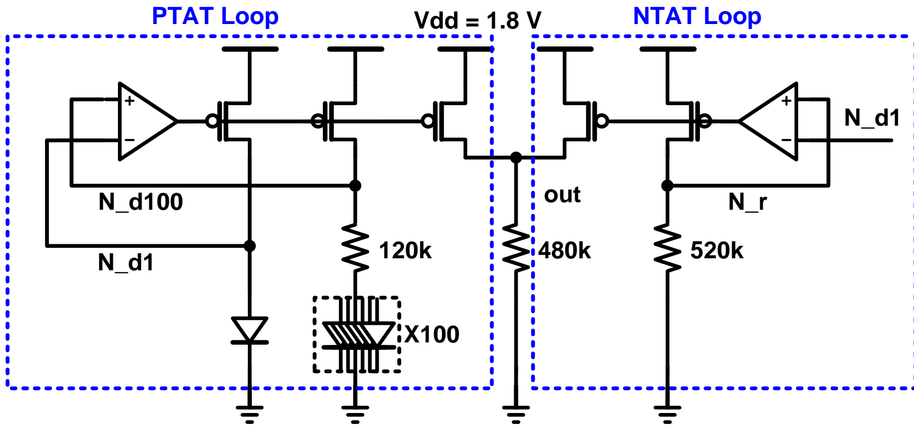


Figure 4.13 Bandgap reference (BGR) circuit.

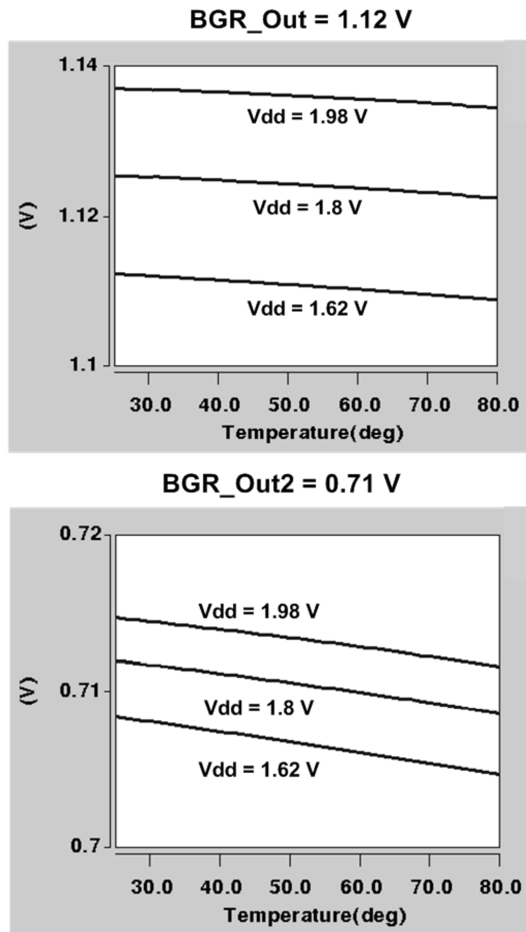


Figure 4.14 Temperature simulation of BGR_Out1/2.

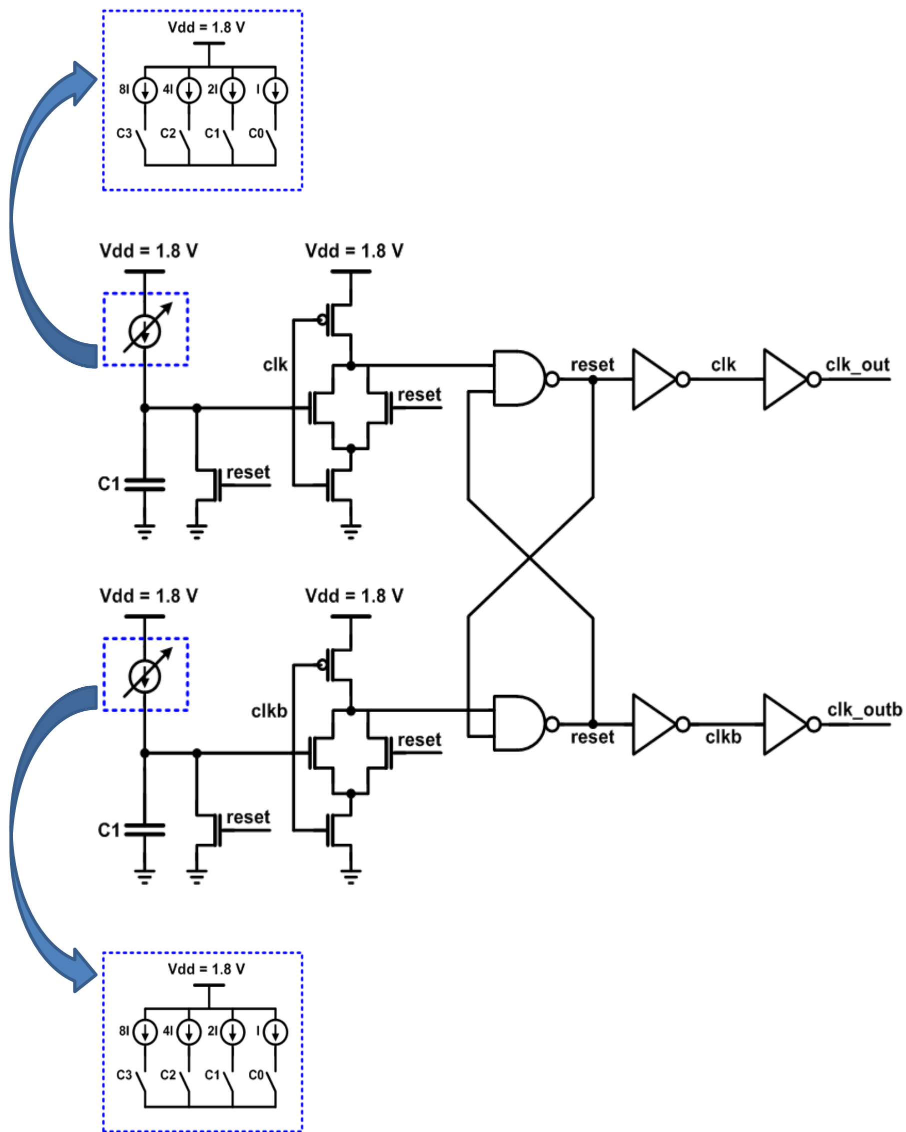


Figure 4.15 Diagram of internal oscillator circuits.

Using sensing resistor between PMIC and level shifter in the proposed real-time current sensing feedback system, current on the target device is sensed and made minimum current level which is adjusted by top gate bias using double gate TFT.

Using measurement data, I_{VON} is modeled to design current sensor circuits by Hspice simulator. Current model is varied depending on temperature variation. When the temperature is increased from 25℃ to 60℃, current level increase 200uA at top gate bias of -5V. Therefore, Searching stable condition for shift register is important. And optimal value of top gate bias is -15V level. The range of DAC output level of the system is set -10 to -20V with ±5V from optimal point.

In Figure 4.16, current sensing operation and ADC processing are simulated. It is synchronized by STVP which is a vertical sync signal of display module. When "Discharge" signal goes to "Low", it means RESET function is done and current integration is started. V_{INT} is the output of current sensing circuits. When V_{TRACK_HOLD} goes from "High" to "Low", ADC processing is started. When ADC_Valid is goes from "Low" to "High", ADC processing is done. And a digital code as ADC output is transmitted to algorithm digital block. After the processing of algorithm block, output of the algorithm is transmitted to DAC block and V_{DAC_OUT} as output of DAC becomes top gate bias.

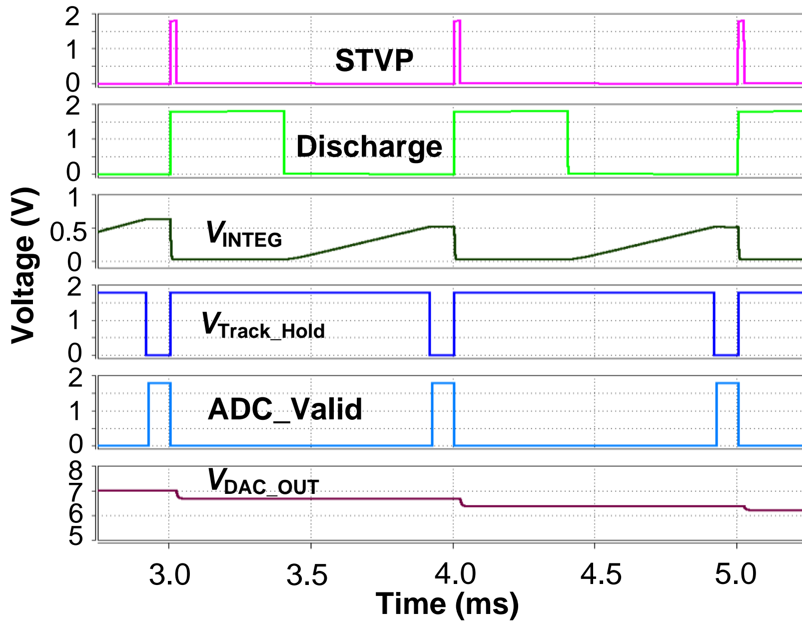


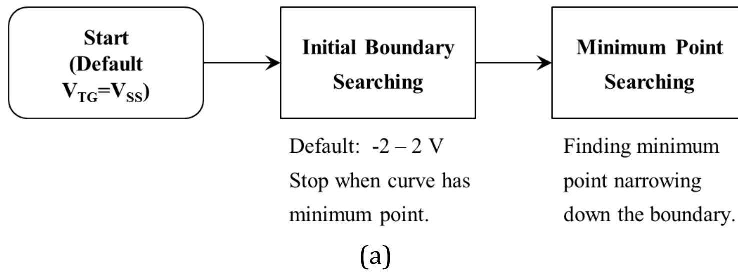
Figure 4.16 Transient simulation of current feedback system.

4.4 Optimum Point Searching Algorithm

An optimal point searching (OPS) algorithm is proposed to decide the top gate voltage. An optimized top gate voltage is obtained by monitoring the current consumption of the shift register. An analog-to-digital convertor (ADC) converts the sensed value and the feedback voltage level is computed in the algorithm part. Then, the adjusted top gate voltage (V_{TG}) in the double-gate TFTs is applied through a digital-to-analog convertor (DAC).

The proposed system includes a searching algorithm, which returns an optimum V_{TG} according to the detected current value. The Oxide TFTs are sensitive not only to electrical and temperature stress but also to the process fluctuation. The current consumption differs from glass to glass and the oxide TFT ages as the operation time is increased. In other words, a look-up table for compensation is valid only for a certain condition. The table data should be dynamically changed when V_{TH} is shifted by the electrical stress, temperature stress, and process fluctuation. Therefore, a proper searching algorithm is required to locate the optimized V_{TG} under all operating conditions. Figure 4.17(a) shows a simplified block diagram of the proposed searching algorithm. It is designed to find the V_{TG} that induces a minimum current consumption. Among the various techniques for finding the minimum value, a golden section search method is adopted due to its fast process time.

In Figure 4.17(b), it shows the Flow chart of optimum point searching algorithm. It is largely classified into three blocks which are initial boundary condition and escape condition and target searching condition.



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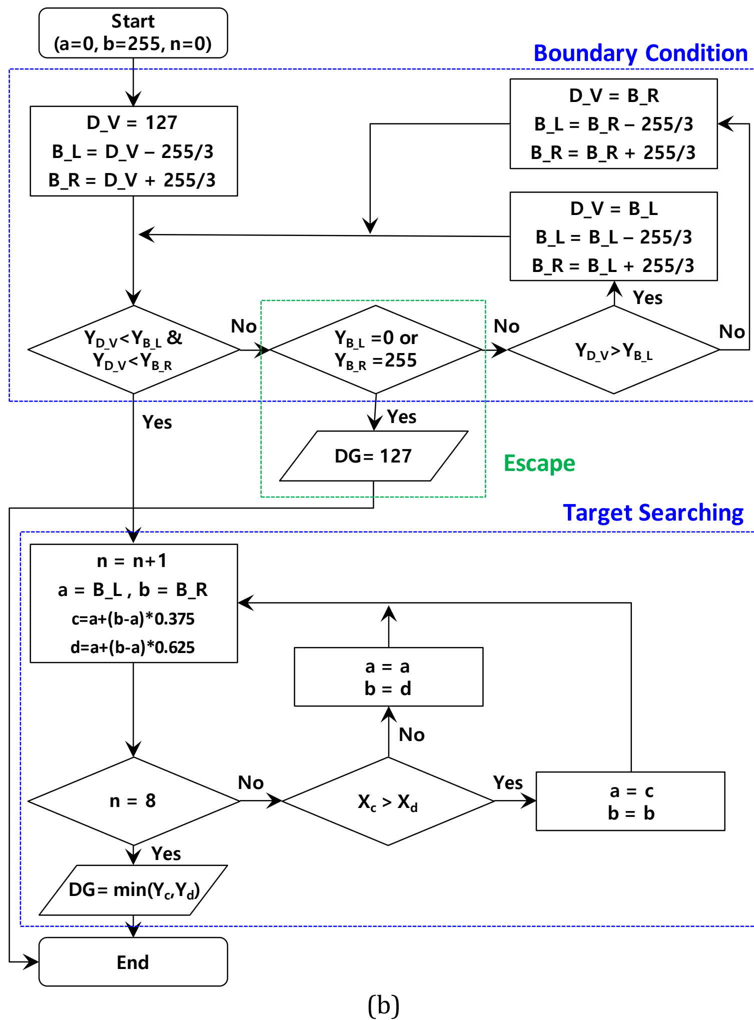


(b)

Figure 4.17 Block diagram of compensation algorithm and Algorithm flow chart of proposed algorithm.

An optimal point searching (OPS) algorithm employs a golden section-searching method for searching the optimum V_{TG}. The algorithm can be divided into two steps, an initial boundary searching and the final target searching.

In the first step, a search for an initial boundary range is performed. A narrow range is initially tried since starting from an extremely high or low V_{TG} might incur stress to the oxide TFT in the shift register, which can cause distortion at the output signal. V_{TG} is initially set as V_{SS} and the default initial boundary range is -2 V to 2 V. Although V_{TG} can be varied up to 10V, the upper bound of only 4 V is found enough based on the measured data.

Next, sensing results at the boundary and at the center are compared to find out if there is a minimum within the selected range as shown in Figure 4.18. When the sensing results exhibit an increasing or decreasing function, the boundary range should be shifted. It can be sure that an optimum value exists within the boundary range if the sensing current vs. V_{TG} curve is a concave function such as quadratic. In the next step, the target minimum value is searched inside the boundaries as shown in Figure 4.19. The boundary is narrowed down further by comparing two sensing results at the points away from the upper and lower boundaries by (1-g)×(width of boundary), where g is the golden ratio ($g \cong 0.625$). An optimum V_{TG} can be obtained by iterating the above process 8 times in an 8-bit data resolution.

$$6 \geq 256 \times g^{n}$$

Figure 4.20 shows the simulation result of optimal point searching algorithm. After 8 iteration of comparison process, it finds the optimal point of top gate bias in the shift register

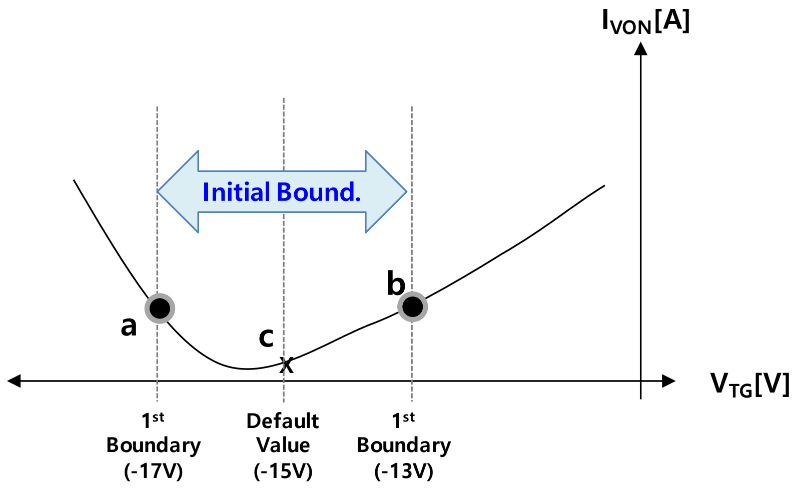
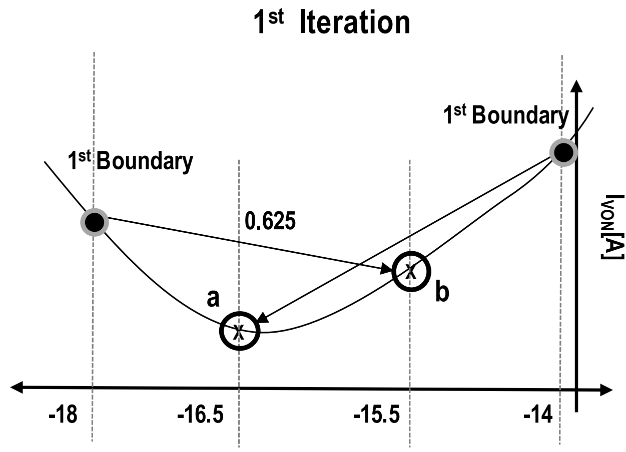


Figure 4.18 Searching for an initial boundary range.



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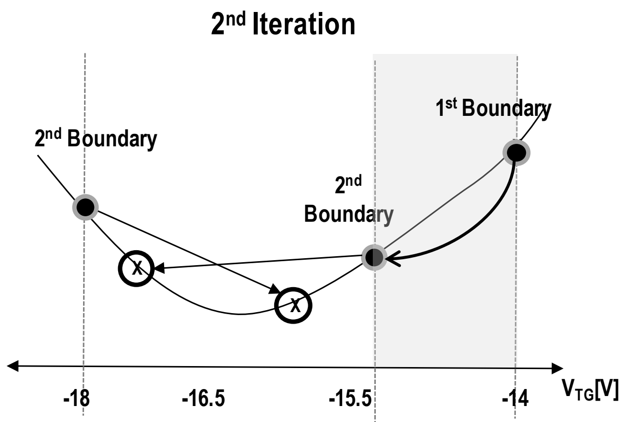

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Figure 4.19 Finding the minimum value inside the boundary range.

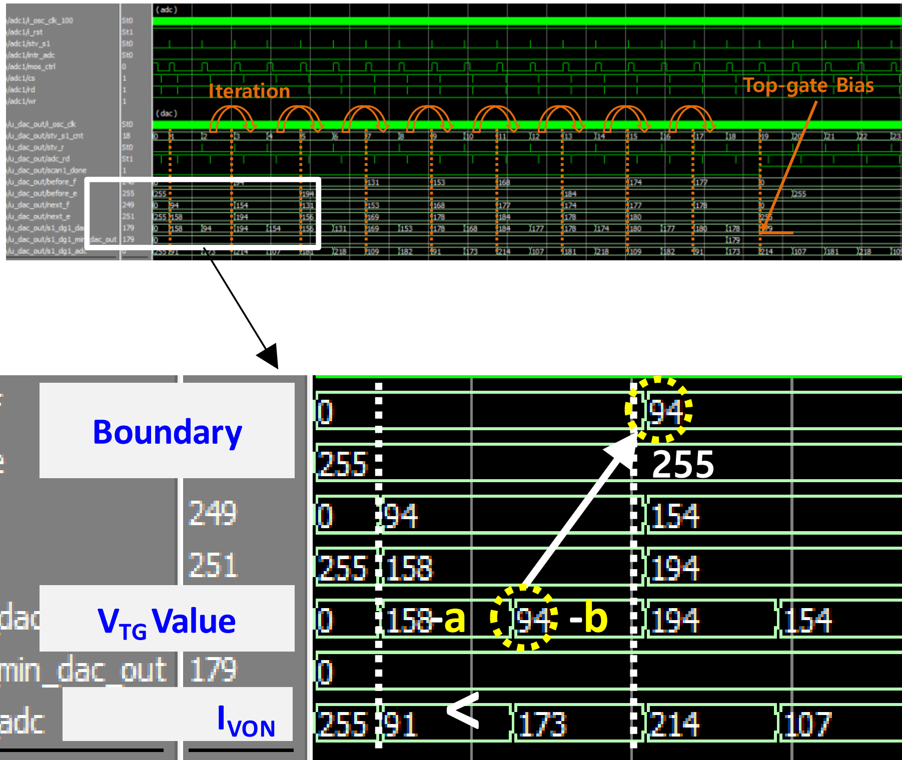


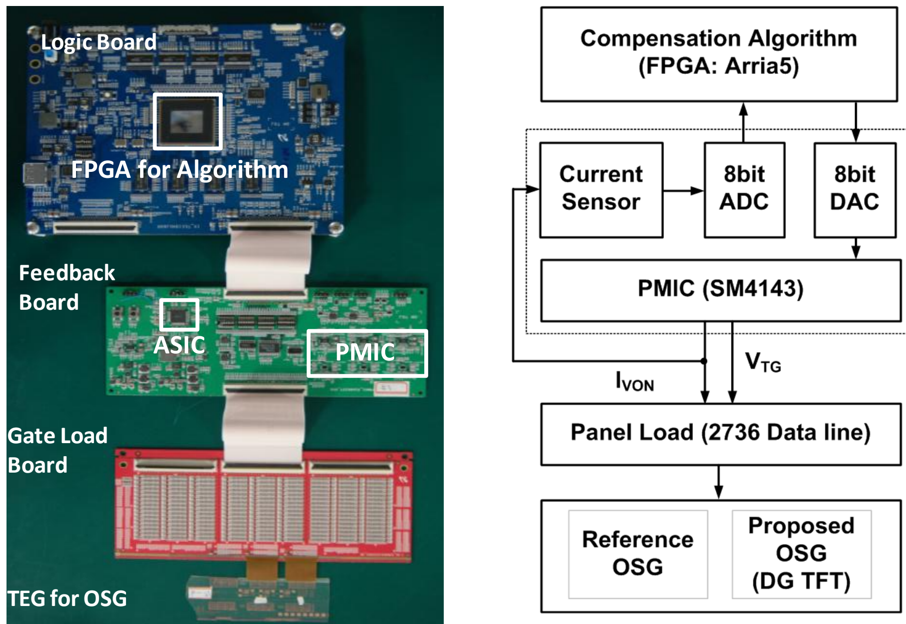
Figure 4.20 Simulation results of optimal point searching algorithm operation using Modelsim.

4.5 System Verification

To verify the overall function of the proposed system, a prototype system has been built using current feedback sensing IC and FPGA IC, as shown in. The key parameters of t_{WAIT} and t_{INTEG} are 5.33ms and 1.33ms, respectively. Using an 8-bit successive approximation ADC, a conversion time t_{CONV} of 0.2ms is required and added to the overall timing. Figure 4.21(a) is the layout of PCB of feedback circuits.

A 16-stage shift register prototype has been fabricated by employing the inverted staggered etch-back oxide TFTs. The fabricated double-gate TFTs demonstrate a linear shift in V_{TH} with a slope of -1.23 V/V by the top gate-to-source voltage. V_{TH} of the oxide TFTs shifts in the negative direction when the ambient temperature is increased. The average current of the 16-stage shift register is measured as V_{TG} is varied. When V_{TG} changes from -10 to 10V, I_{VON} shows a shape of a valley. It exhibits the minimum when V_{TG} is -15V. V_{TG} of -15 V corresponds to V_{SS} of the system, i.e., 0 V. Thus, demonstration of a highly stable gate output voltage is in order with a properly designed feedback system, which compensates the negative V_{TH} shift. Figure 4.21(b) shows the verification of the shift register circuits operation.

After an OPS processing in the digital domain, the optimum value is located and the DA converter generates V_{TG}. The change of V_{DAC_OUT} (V_{TG}) executed by the OPS algorithm is revealed by in-situ monitoring of the current sensing. The measured results confirm that the top-gate bias for the minimum current of the shift register is stabilized within 16 frames, i.e., 256 ms.



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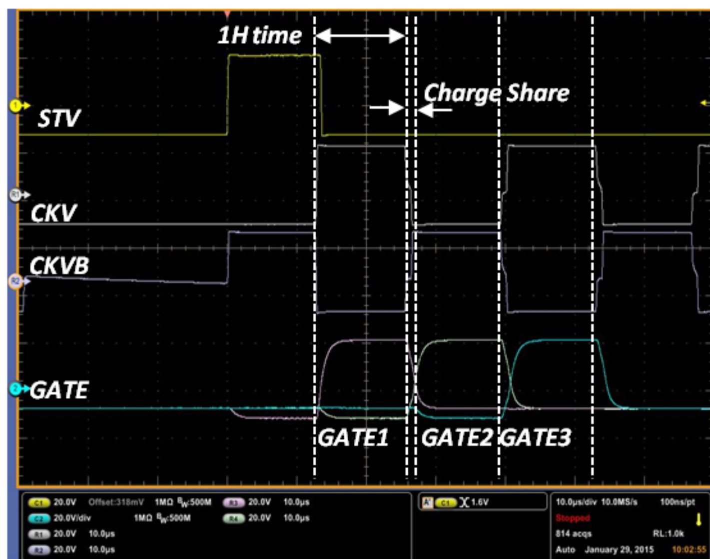

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Figure 4.21 Photograph of an external feedback compensation system and signal waveform of shift register circuit operation.

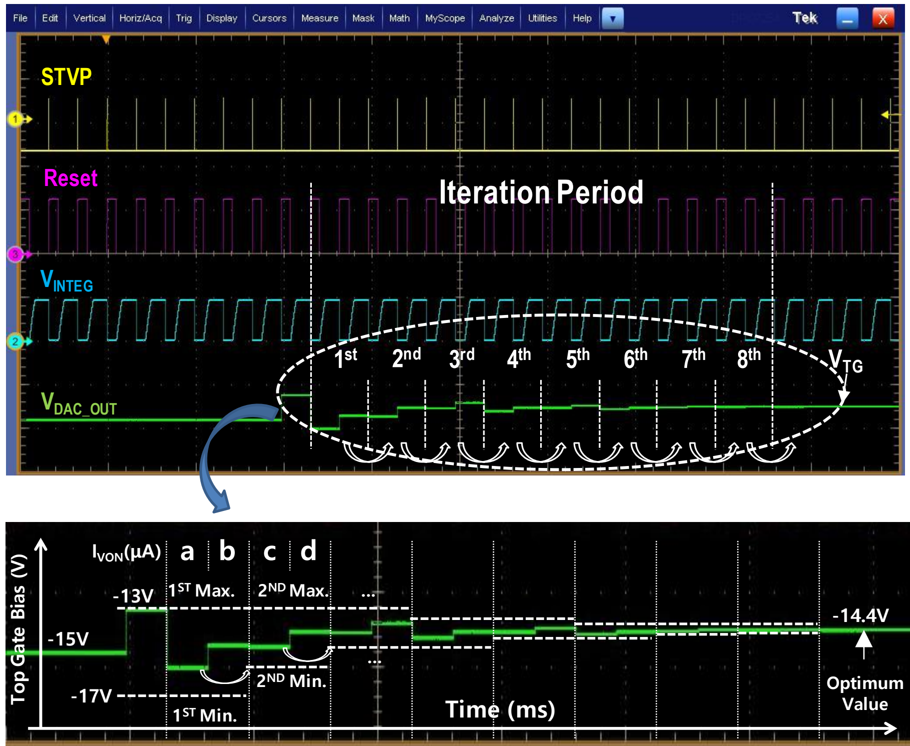
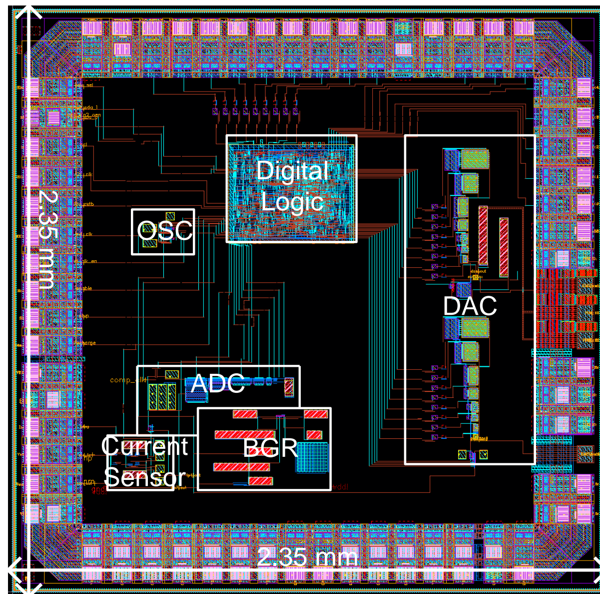


Figure 4.22 Experimental results of system operation



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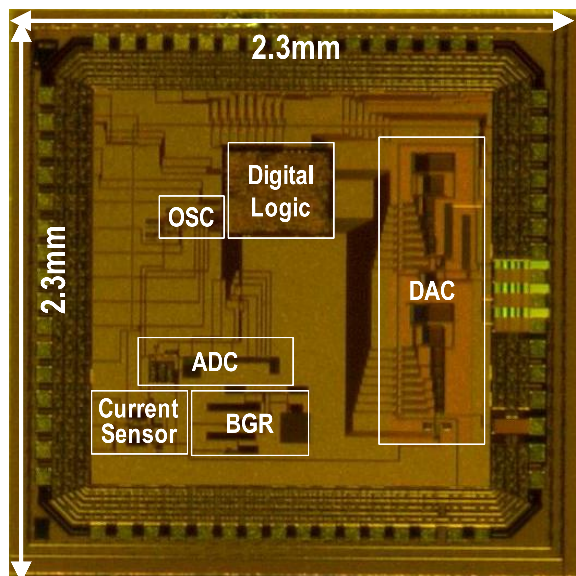


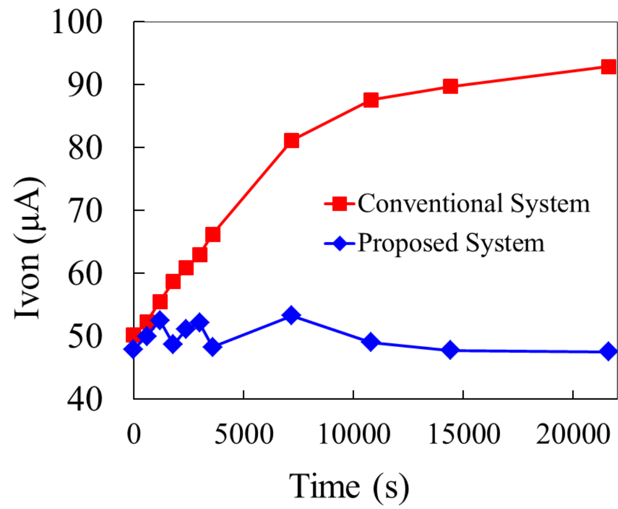
(b)

Figure 4.23 Layout and photograph of the proposed feedback sensing IC.

The real-time current sensing feedback system is successfully designed and fabricated for stabilizing the operation of oxide TFTs-based shift registers over PVT variations and stress. By sensing and integrating the current of the whole shift registers from the display panel, and by applying an optimal point searching algorithm, a stable operation up to 80°C was demonstrated which would not be possible otherwise.

When the current of shift register is measured on the conventional system with increasing temperature up to 80°C, it is increased to more than 10 times than that at the room temperature. However, the proposed feedback system keeps a highly stable (<13%) current up to 80°C with an optimized V_{TG}. Figure 4.24 show the time evolution of power consumption at 60°C. A power of 1.15mW at the initial state changes to 2.14mW after 21,600s in the conventional system whereas the proposed system recorded a stable power consumption of1.15±0.08mW. The sensed current level is significantly low (~102μA) since only 16 stages are used in the shift register, which implies that the fluctuation caused by noise is relatively large. Although there is a fluctuation of about 7% in the compensated power consumption, it does not influence the on/off levels of the gate output. From the measured results, it is confirmed that the proposed system compensates the time-variant V_{TH} shift and improves the performance of the shift register significantly.

When I_{SR} is measured on the conventional system with increasing temperature up to 80°C, I_{SR} is increased to more than 10 times than that at the room temperature. However, the proposed feedback system keeps a highly stable (<13%) I_{SR} up to 80°C with an optimized V_{TG} as shown in Figure 4.25.



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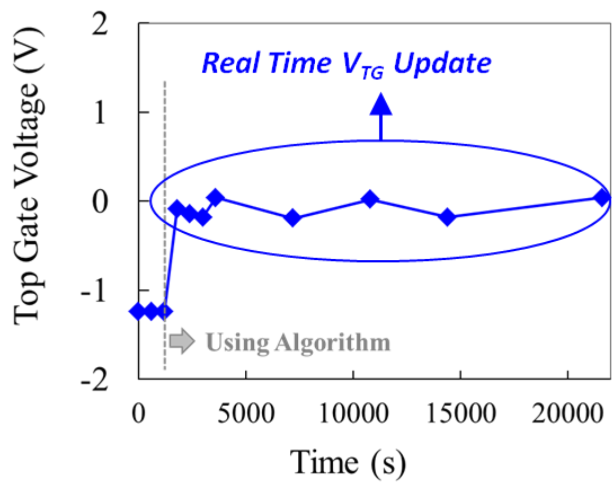

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Figure 4.24 Time evolution of power consumption and top gate voltage (V_{TG}) at 60 °C

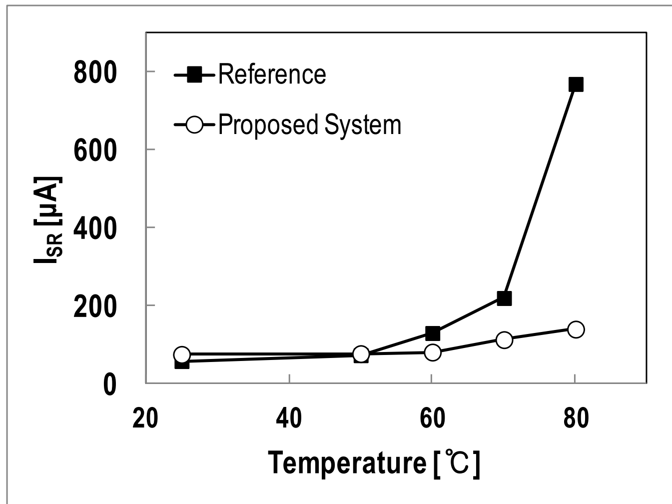

Figure 4.25 The variation of shift register current (I_{SR}) depending on the operating temperature.

Table 4.2 Voltage range of feedback system depending on PMIC current.

DAC Output	PMIC Current	ADC Input	ADC Output		V_{DG}
(8 bit)	(μA)	(V)	(HEX)	(DEC)	(V)
0	543.7	0.272	D0	208	-10
15	526.7	0.263	C7	199	-10.6
31	511.3	0.256	C3	195	-11.2
47	497.5	0.249	BB	187	-11.9
63	485.4	0.243	B8	184	-12.5
79	475.7	0.238	B2	178	-13.1
95	468.6	0.234	B0	176	-13.7
111	463.5	0.232	AE	174	-14.4
127	461.9	0.231	AD	173	-15
143	462.5	0.231	B0	176	-15.6
159	464.8	0.232	B3	179	-16.2
175	469.2	0.235	B4	180	-16.9
191	475.1	0.238	B7	183	-17.5
207	482.8	0.241	B8	184	-18.1
223	488.1	0.244	BA	186	-18.5
239	487.7	0.244	BB	187	-18.5
255	487.4	0.244	BB	187	-18.5

Table 4.3 Pin description of the proposed feedback sensing IC.

Pin Name	Pin Function	# of Pin	Typ.
VDD_12	12V Power for DAC	2	12
VDD_5	5V Power for DAC	3	5
VDD	1.8 V Power for Core Analog and Digital circuits	7	1.8
VDD_33	3.3 V Power for I2C and Digital Interface	4	3.3
GND	Common GND	16	0
Von_in	I_{VON} sensing (Sensing resistor plus node)	1	1.2
Von_out	I_{VON} sensing (Sensing resistor minus node)	1	1.2
Enable	Compensaion Enable(Negative Reset, when 0 reset, 1 operation)	1	3.3
STVP	Timing sync signal	1	3.3
Discharge	Current Mirror Dischage, H: Discharge, L: Integration	1	3.3
DAC_in[7:0]	Parallel DAC inputs for the external algorithm	8	3.3
SDA_sel	I^2C environment setting signal	1	0 or 3.3
SDA	I^2C Protocol signal	1	3.3
SCL	I^2C Protocol signal	1	3.3
I2C_CLK	I2C clock (frequency 48 MHz)	1	3.3
I2C_RSTB	I^2C negative reset signal (when=0, reset)	1	3.3
EXT_CLK	Reserve in case OSC doesn't work	1	3.3
EXT_CLK_EN	Enable external clock	1	3.3
Integ	Current integration node (Ext. capacitor needed)	1	-
ADC_valid	Signal after ADC result updated	1	3.3
ADC_out[7:0]	ADC outputs for the external algorithm	8	3.3
DAC_out	DAC output voltage	1	-
DAC_out2	DAC2 output voltage (Ext. resistor needed)	1	-
	Total number of pins	64	

Table 4.4 Register description of the proposed feedback sensing IC.

R/W	Register number	Bits	Internal register name	Initial value	description
W	0	[7:0]	MPPT_compare	0000_0010	A reference value to decide either coarse or fine step
W	1	[7:0]	DAC_in_i2c	0000_1111	DAC inputs from I2C using external algorithm
W	2	[7:0]	DAC_coarse_step	0000_0100	DAC coarse output step
W	3	[7:0]	DAC_fine_step	0000_0010	DAC fine output step
W	4	[7:0]	DAC_max_boundary	1111_1100	DAC output maximum boundary
W	5	[7:0]	DAC_min_boundary	0000_0100	DAC output minimum boundary
W	6	[1:0]	ext_en	0	Algorithm mode selection
		[2]	DAC_sel	0	when 0, DAC use (default). when 1, DAC_2 use
		[3]	No use	0	No use
		[7:4]	integ_time [3:0]	0	-
W	7	[7:0]	integ_time [11:4]	0010_0000	default 512 period
W	8	[3:0]	osc_frequency[3:0]	0	OSC frequency control, 0000 : slowest, 1111: fastest
		[7:4]	DAC2 current control[3:0]	111	PMOS input, 0000 largest, 0000 smallest current
R	9	[7:0]	adc_mask	variable value	mask for binary search in SAR ADC
R	0A	[7:0]	adc_dac	variable value	Values of the DAC used in SAR ADC
R	0B	[7:0]	dac_out	1000_0000	DAC_output value
R	0C	[1:0]	adc_state	variable value	representing current state in the ADC operation
		[3:2]	mppt_state	variable value	representing current state in the MPPT algorithm
		[4]	dac_gain	variable value	After comparing MPPT output value, DAC_gain becomes "0" or "1".
		[5]	perturbation	variable value	Determine the direction of perturbation: Increase or Decrease.
		[7:6]	No use = 00	0 (Fixed)	-

Chapter 5 Summary

Recently, IGZO TFTs have been gained much attention as promising devices for the active area for AMLCD and AMOLED. Low leakage current of IGZO TFTs can drive the panel at the extreme low frame frequency, such as 1Hz.

In high-end display applications such as ultra high-resolution (UHD), frameless monitor and long battery life tablet, most of the oxide-based TFTs are inherently a depletion-mode device rather that the widely used enhancement-mode device. It should be noted that a design of driving circuits which employ a depletion-mode device is rather difficult to obtain highly stable operation.

In this thesis, a new oxide shift-register using the double gate structure is proposed for highly stable operation in accordance with the temperature and process variation such as V_{TH} shift. In order to search the optimum double gate bias, a current sensing feedback driving system is designed and proved by the 0.18μm BCDMOS process. By sensing and integrating the current of the whole

shift registers from the display panel, and by applying an optimal point searching algorithm, a stable operation up to 80°C was demonstrated which would not be possible otherwise. The compensation algorithm in the system obtains an optimized bias level by maintaining minimum current dissipation. A stable gate output in the proposed system has been verified up to 100°C by adjusting the top gate bias, while the gate output of the conventional system deteriorates at 80°C and above. The proposed system offers a long-term, suitable operation for devices employing shift registers with oxide TFTs that are prone to a negative V_{TH} shift under various environmental variations.

Appendix A SPICE models

A.1 IGZO TFT model parameter

```
 *******************************
*          IGZO TFT model          *
*******************************
.MODEL ntft nTFT (+level = 35        tox = 2.4e-7        +alphasa = 0.6
+def0 = 0.6         +delta = 5          +el = 0.35          +emu=0.06
+eps = 11           +epsi = 7.4         +gamma = 0.4        +gmin = 1e23
+iol = 3e-14        +kasat = 0.006      +kss = 6            +kvt = -0.036
+lambda = 0.006     +m = 2.5            +muband = 0.0006
+rdx = 0            +rsx = 0            +sigma0 = 1e-20     +v0 = 0.12
+vaa = 7.5e3        +vd니 = 20          +vfb = -3           vgsl = 20
+vmin = 0.3         +vt0 = 3.8          +cgdo = 0.2e-12     +cgso = 0.2e-12)
```

A.2 Double gate TFT Model

```
.SUBCKT    DG_UNIT    Drain    Gate    Source    TG

M1    Drain Gate_T15 Source ntft w=wd l=ld

E1    Gate_T15 Gate TG Source 1.25

.ends    DG_UNIT
```

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초 록

최근 디스플레이 산업에서 주목 받고 있는 산화물 박막 트랜지스터(TFT)는 비정질 실리콘 TFT 대비 높은 이동도 특성으로 초고해상도(≥4Kx2K) 및 고속프레임(≥240Hz) 동영상 재생이 가능하고 낮은 off 전류 특성으로 저속프레임(≤30) 정지 영상 재생을 통한 저소비 전력 디스플레이가 가능하다는 장점을 갖고 있다. 그러나 산화물 TFT는 온도, 습도 및 전기적 스트레스를 가했을 때 문턱전압이 이동한다. 액정디스플레이의 경우 픽셀회로에서 사용되는 TFT는 on-off 전압 마진이 크지만 쉬프트레지스터의 경우 게이트-소스 전압(V_{GS})이 0 V 이상에서 turn-on, 이하에서 turn-off 조건이기 때문에 문턱전압 이동에 민감하다.

본 논문은 산화물 TFT를 이용한 쉬프트레지스터의 온도 및 전기적 안정성을 높이기 위한 문턱전압 제어가 가능한 쉬프트레지스터 회로 및 실시간 피드백 보상이 가능한 구동 시스템에 대한 연구이다.

쉬프트레지스터 회로는 상부 게이트 전압(V_{TG})에 따라 문턱전압이 변화하는 더블게이트 TFT를 적용하여 문턱전압 열화 보상이 가능하도록 디자인하였다. 기존 회로에서 문턱전압이 감소함에 따라 발생하는 문제를 분석하여 취약한 부분에만 더블게이트 TFT를 대체 적용하고 소스 단자가 DC인 TFT의 경우에는 상부 게이트에 DC를 인가하고 신호를 전달하는 TFT의 경우에는 TFT turn-on 시 높은 전압이 인가되어 신호 전달이 극대화 되도록 설계 하였다. 쉬프트레지스터를 100°C에서 동작시켰을 때 기존 회로의 경우 게이트 출력 파형이 왜곡된 것에 반해 최적 V_{TG}전압을 인가한 제안된 회로에서는 안정적으로 동작하는 것을 시뮬레이션 및 실험을 통해

확인하였다.

그러나, 동일한 공정조건에서 제작된 회로임에도 불구하고 공정 산포에 의해 초기 문턱전압에 산포가 존재하고 열화 조건에 따라 문턱전압의 이동 정도가 다르기 때문에 패널마다 V_{TG} 최적값이 변화하는 문제가 존재한다. 그렇기 때문에 제안된 쉬프트레지스터로 문턱전압을 보상하기 위해서는 실시간으로 최적 V_{TG}를 인가할 수 있는 구동 시스템이 필요하다. 회로를 구성하는 TFT의 문턱전압 변화는 소비전류의 변화로 나타나기 때문에 본 연구에서는 쉬프트레지스터의 소비전류를 센싱하여 열화 정도를 파악하고 최적점을 찾는 알고리즘을 통해 최적 V_{TG}를 인가하는 시스템을 설계하였다. 시스템은 전류를 센싱하는 회로 및 센싱 회로를 디지털로 변환하는 ADC, 최적점을 검색하는 디지털 회로, 디지털 값을 아날로그 V_{TG} 전압으로 변환하는 DAC 등으로 구성되어 있고 0.18 μm BCDMOS 공정을 통해 IC로 제작하여 그 기능을 검증하였다. 실험 결과 기존 쉬프트레지스터의 경우 80°C 에서 소비전류가 10배 이상 증가한 것에 반해 제안된 피드백 회로 시스템에서는 소비전류가 13% 이하로 안정적으로 동작하는 것을 확인하였다.

본 연구에서는 실시간으로 쉬프트레지스터 전류를 센싱하여 문턱전압 열화를 피드백 보상을 하는 시스템 및 쉬프트레지스터 회로를 제안 및 제작함으로써 그 안정성을 검증하였다.

주요어: 산화물 박막 트랜지스터, 쉬프트레지스터, 피드백 시스템, 문턱전압 보상

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