Ph.D. DISSERTATION

Implementation of Synaptic Plasticity and Learning functions using Si-based Charge Trap Memory

실리콘 기반의 전하 트랩 메모리를 이용한 시냅스의 가소성 및 학습 기능 구현

BY

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COLLEGE OF ENGINEERING
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이 논문을 공학박사 학위논문으로 제출함

2016 년 8 월

서울대학교 대학원

전기컴퓨터공학부

이 명 선

이명선의 공학박사 학위논문을 인준함

2016 년 8 월

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ABSTRACT

The development of an energy efficient and highly integrated electronic synapse is an important step in the effort to mimic the adaptive learning and memory in a biological neural network. Recently, several types of two-terminal memristors have been proposed to emulate biologically inspired synaptic functions using various components such as atomic switches, phase-change memory (PCM), and resistive switching devices. However, these two terminal devices require one select device per cell in a cell array to imitate a synapse-neuron network. Moreover, they need to be improved in terms of reliability, repeatability and processing complexity.

In this thesis, we propose a new silicon-based charge trap memory device with an $Al_2O_3/HfO_2/Si_3N_4$ (A/H/N) gate stack to realize the imitation of memory features in a biological synapse. In a fabricated capacitor having the proposed gate stack, short-term plasticity (STP) and long-term potentiation (LTP) properties with their transition are demonstrated, which are similar to the behavior of biological synapses.

A single charge trapping layer (Si_3N_4) on silicon interface induces fast charge loss by trap-assisted tunneling (TAT) or direct tunneling. In addition, there is no remarkable pulse interval dependence when repeated input pulses are

applied, in which the pulse amplitude and width are same. However, more frequent input pulses leads to larger current changes with longer retention property when HfO_2 layer is inserted on Si_3N_4 layer as a second charge trapping layer. It is originated from the deep trap level (E_T) in HfO_2 layer leading to a transition into long-term memory. Lastly, we proposed a pair of pre- and post-synaptic spike scheme for the synaptic device and STDP property was demonstrated from experimental data.

This suggested architecture has remarkable advantages, including high uniformity over a large area, excellent reliability, the use of CMOS-compatible materials, and easy integration with CMOS circuits.

Keywords: Charge trap memory, Synapse, Short-term plasticity (STP), Long-term potentiation (LTP), $Al_2O_3/HfO_2/Si_3N_4$ (A/H/N), gate stack

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CONTENTS

Chapter 1

Introduction

1. 1 Motivation

Recently, several types of two-terminal memristors have been proposed to emulate biologically inspired synaptic functions using various components such as atomic switches, phase-change memory (PCM), and resistive switching devices [1]-[7]. Among these components, some show not only a nonvolatile memory feature with a gradual conductance change but also synaptic or biological memory functions with transition behavior. Examples include Ag_2S, WO_x, Ta_2O_5 and α-InGaZnO, which are not controlled by the charge but by ion migration or movement of the oxygen vacancies [4]-[7]. However, these two terminal devices require one select device per cell in a cell array to imitate a synapse-neuron network. Moreover, they need to be improved in terms of reliability, repeatability and processing complexity. Some authors have reported the synapse devices using three-terminal memories, such as SONOS-type flash memories and ferroelectric-gate FETs [8], [9]. However, the synapse devices have only nonvolatile characteristics. It is possible to implement incremental conductance changes with them while they cannot be used to implement short-

term plasticity and long-term potentiation.

Therefore, it is necessary for a synaptic device to have high reliability and low-power consumption with short- and long-term memory applications. Thus, we propose a new silicon-based memory device with an $Al_2O_3/HfO_2/Si_3N_4$ (A/H/N) gate stack to realize the imitation of memory features in a biological synapse. In this stack, two different charge trap layers are used for short-term plasticity (STP), and long-term potentiation (LTP) wtih their conversion properties. One have a short retention property and the other one should have long-term memory characteristic with deep trap level.

1. 2 Major factors influencing retention properties

One of the serious obstacles to scaling of flash-memory devices is tunnel-oxide thickness reduction due to the trade-off relationship between program/erase speed and retention. A thin tunnel oxide causes faster program/erase speed but leads to degradation of the data retention property, whereas a thick tunnel oxide ensures a good retention property but brings about slow operation speed. As tunnel-oxide scales down, a higher electric field is applied for the same gate voltage. This reinforces a write/erase stressing effect on the tunnel oxide, causing

the generation of defects and traps in the gate stack. It is well known that such defects in the tunnel oxide induce trap-assisted tunneling current, which significantly affects the retention property. This effect is called stress-induced leakage current (SILC) [16], and results in major reliability concern, especially for floating gate-type flash-memory devices due to non-localization of stores charges. It can easily lead to oxide breakdown and is also increased dramatically for thinner oxides.

In many material system, these when two dissimilar materials are in contact, electronic states caused dangling bonds or other imperfections occur at the interface. In the SiO_2/Si system, these states can be passivated with hydrogen; the resulting density of the interface states very low. However, the direct contact of the high-k material/Si interface still requires more advanced passivation method for practical implementation. If these states are not fully passivated, they can act as traps for charged carriers, resulting in undesirable transistor characteristics such as hysteresis, wide distribution of the threshold, and reduction of channel mobility. Therefore, a proper passivation process is required to use high-k barrier-

engineered materials for the tunnel oxide.

The use of high-k dielectric layer for blocking oxide can improve the program/erase speed by decreasing the gate stack EOT value. Another advantage of high-k dielectrics for blocking oxide is decreased back tunneling current by electron during erase operation. Al_2O_3 is considered to be a leading candidate as an alternative blocking oxide layer. The dielectric constant of Al_2O_3 (~8.8) is higher than that of SiO_2 (3.9) and it has a large band gap (8.7 eV), conduction band offset (2.8 eV) as compared to silicon. Many research results commonly show that the properties of the Si_3N_4/Al_2O_3 interface involve a path of electron detrapping and they play a crucial role in the program/erase and retention mechanism. For decreasing defective bonds or traps density of the Al_2O_3 bulk, a passivation method of the Al_2O_3 blocking layer has also been investigated. Chang et al. reported that high-pressure fluorine annealing at 400 °C on a $Pt/Al_2O_3/Si_3N_4/SiO_2/Si$ (MANOS) memory device replaced Al-O bonds with Al-F bonds in the Al_2O_3 blocking layer, which led to improvement of the blocking efficiency of the MANOS devices [17]. The revealed that fluorine incorporation into ONA

stacks improved electrical performance in such areas as leakage current at a high field, erase speed, endurance characteristics, and even charge loss rate by thermal emission.

1. 3 Si_3N_4 and HfO_2 for charge trap layers

Although the conventional Si_3N_4 trap layer is the most common and well known charge-trap layer, having a relatively deep trap energy level that provides good data retention, it is expected that there is a thickness scaling limitation in the Si_3N_4 trap layer. Scaling of the Si_3N_4 trap layer below a thickness of 4 nm leads to increased charge loss in the data retention states and a small memory window [18]. Therefore, for further scaling of the charge trap layer, other high-k materials with an even deeper trap energy level, other high-k materials with an even deeper trap energy level should be used for future flash applications. Adopting a high-k dielectric as a charge-trap layer can be an effective approach for scaling operation voltage to reduce power consumption and chip size. A high-k trap layer reduces the electrical thickness of the flash memory cell stack. Consequently, voltage drop

across the high-k trap layer could be reduced while voltage drop across the tunnel oxide is increased. Accordingly, operation voltage is scaled down and program/erase speed is increased at the same time. To further reduce operation voltage, reduction of charge trap layer EOT is unavoidable, because severe reduction of bottom and top oxide thickness may cause degradation of data retention properties.

Ideally, high-k dielectric materials are attractive candidates for the charge trap layer in flash memory devices due to the characteristic of deep trap energy levels, which decreases the tunneling current through the tunnel oxide and blocking oxide in the retention state. In addition, use of a high-k dielectric for storage nodes can increase physical thickness, which in turn increases the number of traps and therefore enhances the memory window in the dielectric while keeping the same EOT of the dielectric stacks. Therefore, a high program/erase speed and longer data retention time can be expected when employing a high-k as the storage layer.

One of promising candidates for high-k charge storage dielectrics is HfO_2. Ultrathin HfO_2 trap layer with a thickness of 2 nm could store almost the same

charges as a Si_3N_4 layer with a thickness of 7 nm in a MHOS structure [19]. MNOS memory exhibits almost no memory window when the nitride thickness is thinner than 4 nm. On the other hand, the memory window of the MHOS capacitor does not diminish suddenly even if the HfO_2 trap layer continuously decreases. This is because the charge-trap phenomenon in trapping layers is different; in other words, the HfO_2 layer has better bulk charge-trapping characteristics than Si_3N_4 layer. HfO_2 has much shallower charge trap (0.5-0.96 eV) than the other charge-trapping materials, such as Si_3N_4 (~1.39 eV) and Al_2O_3 (~2.35 eV) [20]. As a result, trapped charge in HfO_2 are easily detrapped and lost via tunneling. Although as-deposited amorphous HfO_2 formed by electron-beam evaporation has deeper charge traps (~2.45 eV), the trap energy decreases drastically to ~0.96 eV after undergoing 600-900 °C annealing process.

1. 4 Design of gate stack for synaptic device

The Short-term plasticity (STP) is a temporary potentiation of neural connections, and lasts for a few minutes or less while the long-term potentiation

(LTP) should be maintain the strengthened state for a long time (from hours to years). Besides, STP can be converted to LTP through repeated rehearsals, which involves a physical change in the structure of neurons. Thus, short-term and long-term memory should coexist in a synaptic device for the emulation of synaptic behavior. The poor retention property can be implemented by ultra-thin or without tunnel layer and high interface traps between silicon and the gate stack interface. On the other hand, a charge storage layer having deep trap level can have better retention property. A use of high-k dielectric can improve the power consumption and program/erase speed. If these mentioned factor are properly combined in multilayer gate stack, a new synaptic device can be made for neuromorphic applications.

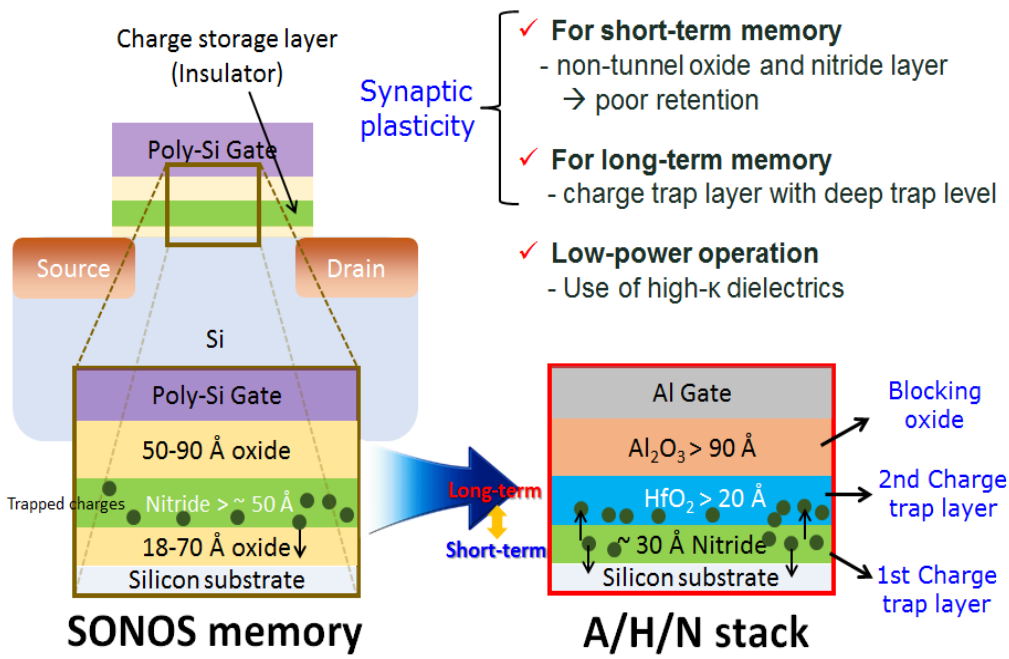


Fig. 1.4. 1 Design of synaptic device

1. 5 Thesis Organization

This thesis is organized as follows. Chapter 1 provides motivation of this thesis including an overview of issues in SONOS type memory device. Chapter 2 consists of a fabrication process of a capacitor consisting of A/H/N stack with Al gate, and their capacitance-voltage (*C*-*V*) and capacitance (*C*-*t*) characteristics. Trapped charge variations depending on iterative pulse conditions are compared with biological synaptic behavior. From experimental data, short-term plasticity (STP) and long-term potentiation (LTP) are demonstrated. In Chapter 3, analysis

of charge transport and trapping mechanism with *I-V* measurements and fitting of the curves for the A/H/N stack. The transient characteristics are represented for O/N stack to investigate properties of a single charge storage layer (Si_3N_4). Scaled A/H/N stack also is also studied with a comparison A/N stack with different pulse conditions. Lastly, we demonstrated spike-time-dependent plasticity (STDP) with gradual potentiation/depression properties for the proposed device. Chapter 4 is conclusions of this dissertation. Analysis of interface trap was tried using charge pumping method in Appendix section.

Chapter 2

$Al_2O_3/HfO_3/Si_3N_4$ (A/H/N) gate stack

2. 1 Introduction

High-κ charge trapping layer in poly-Si/SiO_2/Si_3N_4/SiO_2/Si (SONOS) type memory structure is of increasing interest for charge storage non-volatile memory (NVM) device applications [21-27]. Silicon nitride (Si_3N_4) charge trapping layers in a poly-Si/SiO_2/Si_3N_4/SiO_2/Si (SONOS) memory structure have been studied extensively with poor retention and scaling issue [28]. The high-κ film as a charge trapping layer should be used in the SONOS structure to improve the program/erase speed, vertical scaling and charge retention characteristics. To further improve the vertical scaling and charge retention characteristics of non-volatile memory devices, the high-κ materials with a large barrier height, such as Al_2O_3 films, are interesting alternatives as a blocking oxide [29]. To obtain high-performance non-volatile memory devices, a high work function metal gate electrode in a metal/Al_2O_3/HfO_2/SiO_2/Si (MAHOS) memory structure has been studied for a new generation of memory technology. Therefore, we also used

high-κ dielectrics properly for the proposed gate stack to imitate synaptic behavior.

2. 2 Fabrication process of a capacitor

The fabricated device consists of an Al gate electrode and an A/H/N gate stack formed on a p-type Si (100) wafer. The first step in the implementation of the structure is to form an n^+ region with As^+ ions and annealing so as to supply electrons effectively to the gate stack while the device is being programmed. Before the deposition of the nitride layer (~ 3 nm) by low pressure chemical vapor deposition (LPCVD), the wafer was treated with diluted hydrofluoric acid to remove the native oxide. Then, HfO_2 (~ 10 nm) and Al_2O_3 (~ 12 nm) layers were formed by atomic layer deposition (ALD) at 350 ˚C. An Al layer (~ 200 nm) was deposited and patterned by a wet etching process for the formation of the top electrode. The area of the square Al electrode is approximately 100 × 100 μm2. The capacitance-voltage (*C*-*V*) and capacitance-time (*C*-*t*) measurements were performed at different temperatures using an HP 4280 CV meter and an Agilent 81110A pulse pattern generator. The frequency and small-signal

amplitude for the measurements are 1 MHz and 30 mV, respectively. The DC bias and pulse voltages were applied to the Al top electrode, and the silicon substrate and the n^+ region were electrically grounded during all of the measurements.

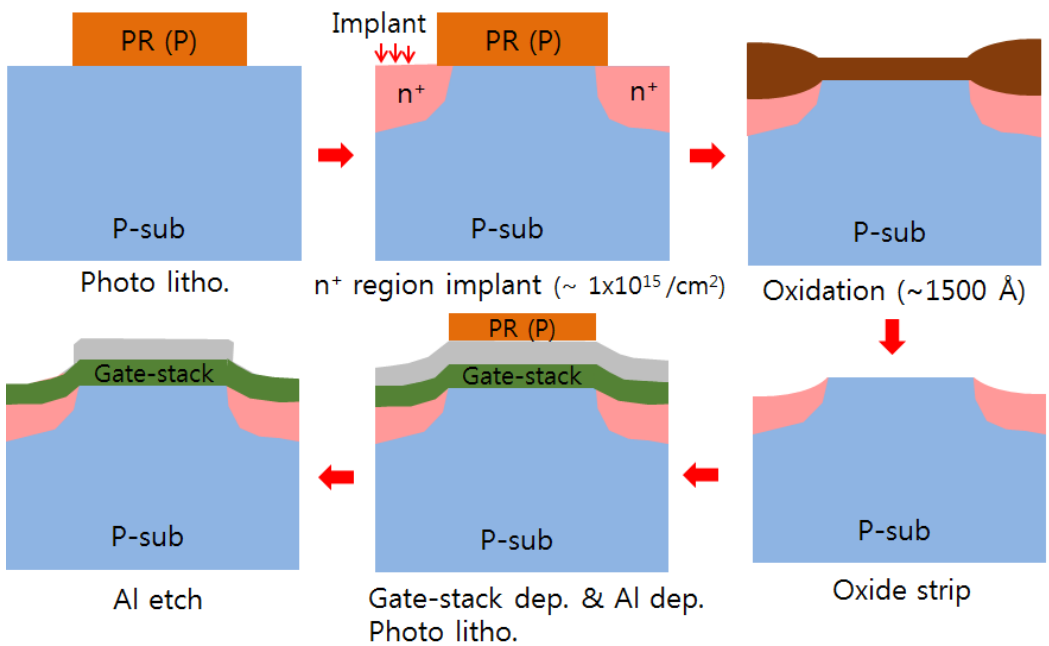


Fig. 2.1 Fabrication process flow of a capacitor

2. 3 Measurement setup

The area of the square Al electrode is approximately 100 × 100 μm^2. The capacitance-voltage (*C*-*V*) and capacitance-time (*C*-*t*) measurements were performed at different temperatures using an HP 4280 CV meter and an Agilent 81110A pulse pattern generator. The frequency and small-signal amplitude for the measurements are 1 MHz and 30 mV, respectively. The DC bias and pulse voltages were applied to the Al top electrode, and the silicon substrate and the n+ region were electrically grounded during all of the measurements.

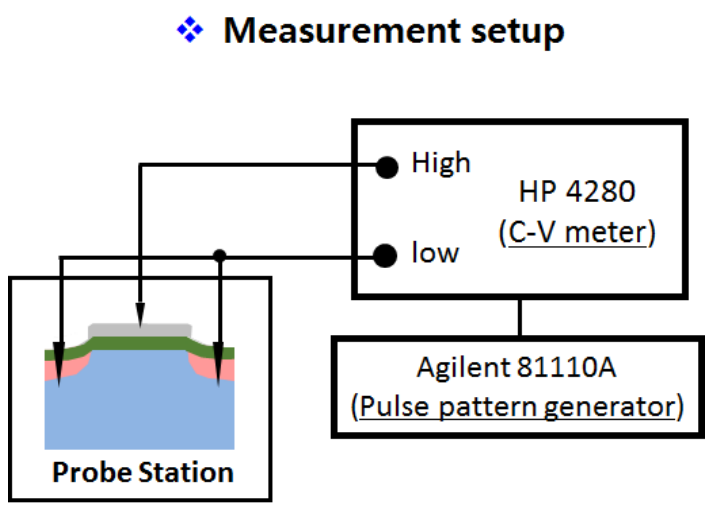


Fig. 2.2 Schematic image of measurement setup

2. 4 *C-V* characteristics

Figure 2.3(a) shows a cross-sectional TEM image of a device with an Al electrode (top), an A/H/N gate stack, and a Si substrate (bottom). The energy band diagram of the gate stack is shown in Fig. 2.3(b), where it is important to note that there is no tunnel oxide layer, as is common in general gate stacks for charge-trap flash memory types such as SONOS-type memory. Nitride film is usually used as a charge trapping layer formed on the tunnel oxide layer for nonvolatile memory applications. However, the nitride layer in this work is directly formed on the Si substrate, leading to poor retention properties. An HfO_2 layer has not only been suggested as a tunneling or blocking oxide layer given that it is a high-κ dielectric material. It has been also suggested as a charge-trapping layer for the implementation of charge trap flash memory [11], [12]. With a high-κ dielectric layer as a secondary charge-trapping layer, the effective oxide thickness and the operation voltage for charge trapping could be effectively reduced.

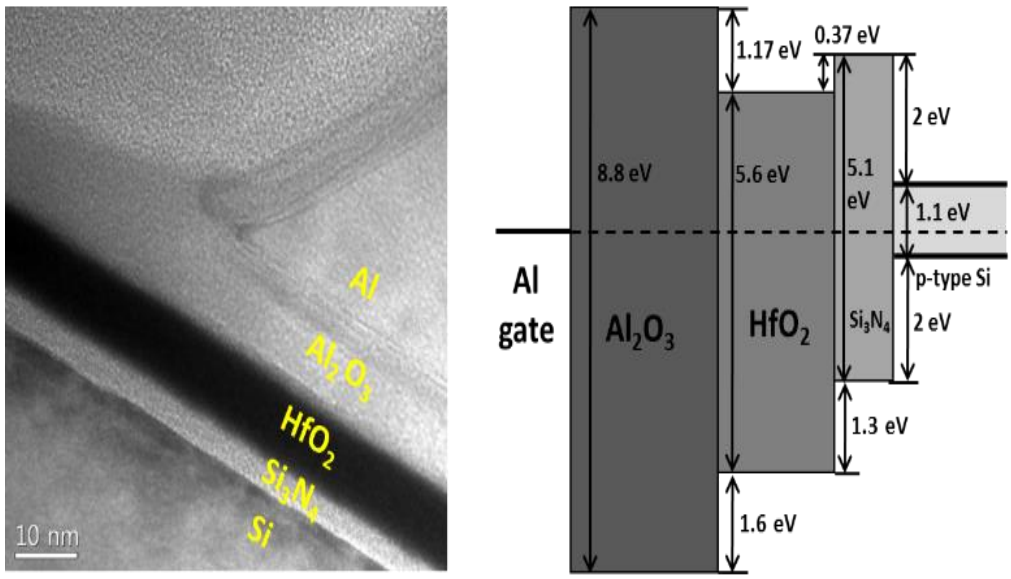
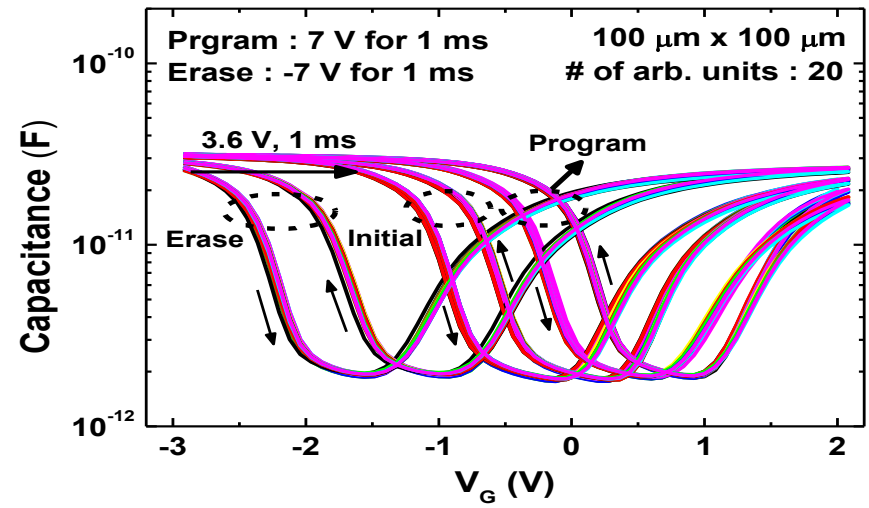
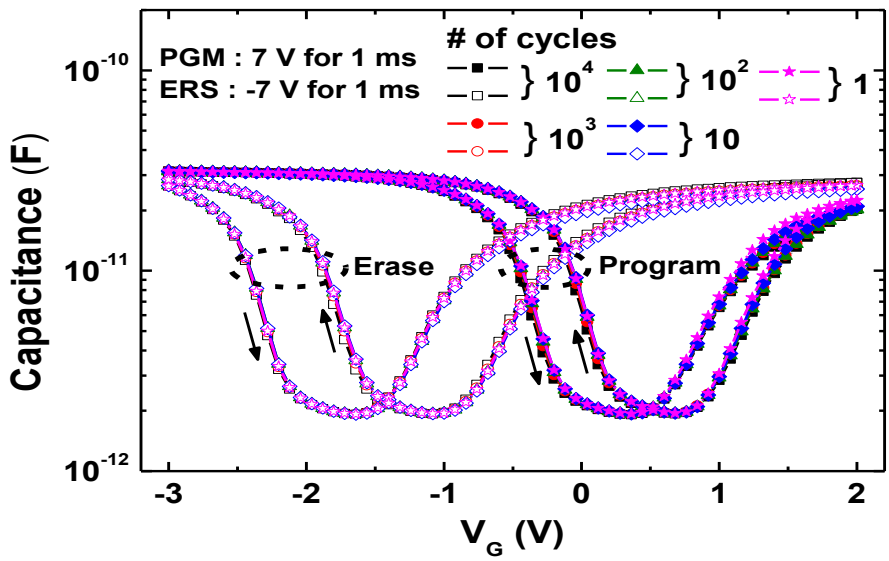


Fig. 2.3 . (a) Cross-sectional TEM image and (b) energy band diagram of a Si (bottom)/Si_3N_4/HfO_2/Al_2O_3/Al (top) cell

Figure 2.4 (a) presents the C-V characteristics of arbitrary cells (100 × 100 μm2) measured with a voltage double sweep from -3 to 2 V. They show hysteresis behavior, which indicates that electrons are easily trapped at the interface states between the nitride layer and the Si substrate and in the nitride layer during the measurement. Reproducible program and erase properties are also clearly observable. A voltage pulse of 7 V for 1 ms causes about a shift of 1.5 V from the



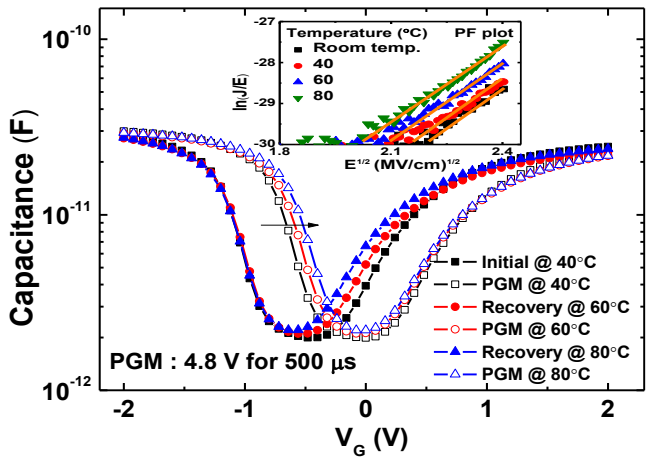
(a)



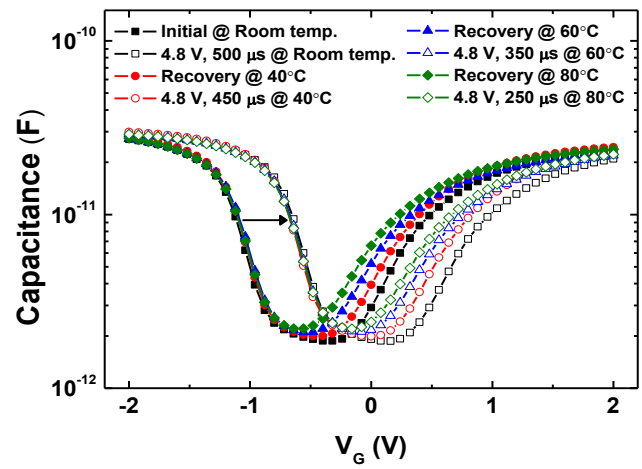
(b)

Fig. 2.4 (a) Capacitance-voltage (C-V) curves in 20 arbitrary cells (100 μm × 100 μm) with program (7 V for 1ms) and erase (-7 V for 1ms) characteristics. 3.6 V for 1 ms was applied after the erase operation to restore the charge of the measured device to nearly its almost initial state. (b) P/E cycling endurance of a cell capacitor.

curve at the initial state. Then, the erase operation is successively performed by a voltage pulse of -7 V for 1 ms, leading to a program/erase window of about 2 V. The device state can be put back into its almost initial state by applying 3.6 V for 1ms. Figure 2.4(b) shows the 10k cycling endurance of the capacitor at room temperature, showing excellent endurance properties with nearly consistent *C*-*V* curves.



(a)



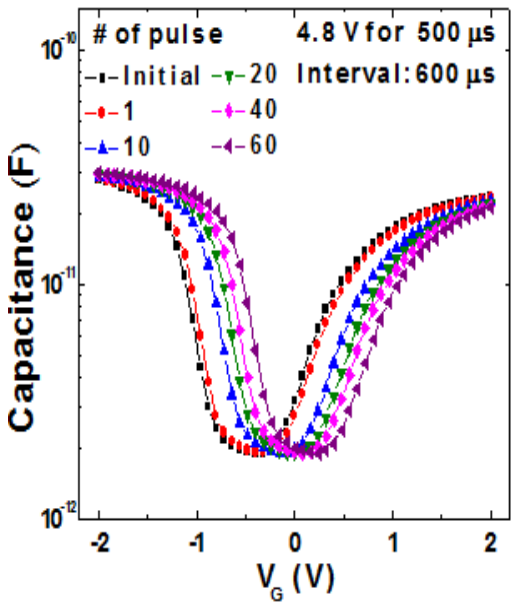
(b)

Fig. 2.5 (a) C-V characteristics immediately after applying 4.8 V for 500 μs at different temperatures (40, 60 and 80 ℃). The inset of Fig. 3(a) shows the ln(J/E)-$E^{1/2}$ characteristics of the proposed stack for PF emission at different temperatures. (b) *C-V* properties soon after the capacitor is programmed at 4.8 V for different pulse widths at different temperatures, showing nearly the same flatband voltage (V_{fb}) shifts (~0.43 V).

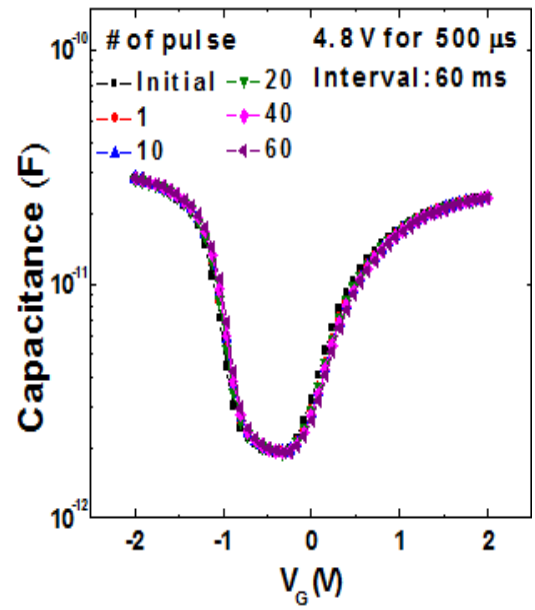
2. 5 Transient properties with *C-t* measurements

Figure 2.5(a) shows the C-V characteristics immediately after the application of 4.8 V for 500 μs at different temperatures (40, 60 and 80 ℃) was performed immediately after the device was programmed at 4.8 V for 500 μs. Because the dominant current transport mechanism is not Fowler-Nordheim (FN) tunneling but instead Poole-Frenkel (PF) conduction, as shown in the inset of Fig. 2.5(a), the program characteristics differ depending on the temperature. However, Fig. 2.5(b) demonstrates that the program speed can be controlled by adjusting the programming pulse width when the pulse amplitude (4.8 V) is fixed at different temperatures. Nearly the same flatband voltage (V_{fb}) shifts (~0.43 V) are successively achieved for all of the performed program conditions.

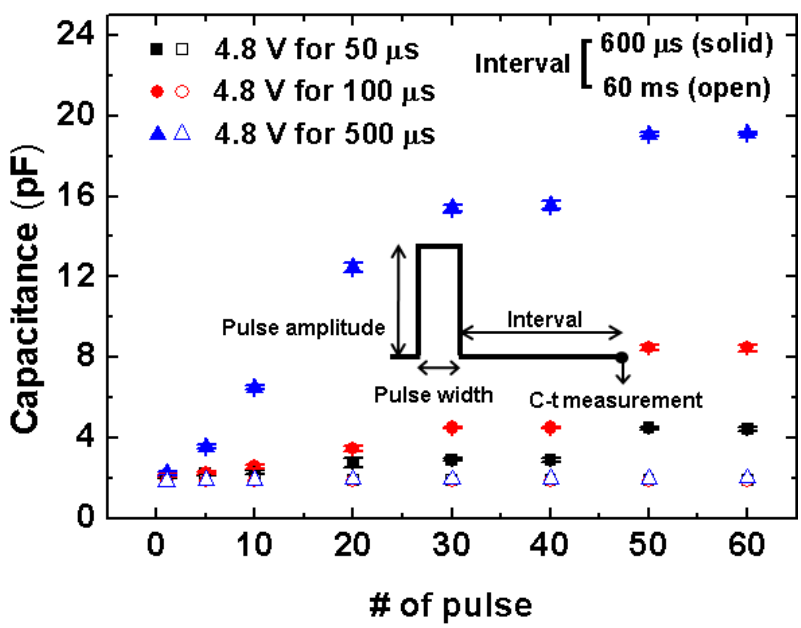
C-V measurements were carried out immediately after the application of consecutive programming pulses (4.8 V for 500 μs) with different time intervals (600 μs and 60 ms) between adjacent pulses, as shown Figs. 2.6(a) and (b). When the time interval is 600 μs, the *C-V* curves gradually shift to the right direction, indicating the stacked layers are gradually charged.


# of pulse
4.8 V for 500 μs
Initial
20
Interval: 600 μs
1
40
10
60
Capacitance (F)
10^{-10}
10^{-11}
10^{-12}
-2
-1
0
1
2
V_G (V)

(a)


# of pulse
4.8 V for 500 μs
Initial
20
Interval: 60 ms
1
40
10
60
Capacitance (F)
10^{-10}
10^{-11}
10^{-12}
-2
-1
0
1
2
V_G (V)

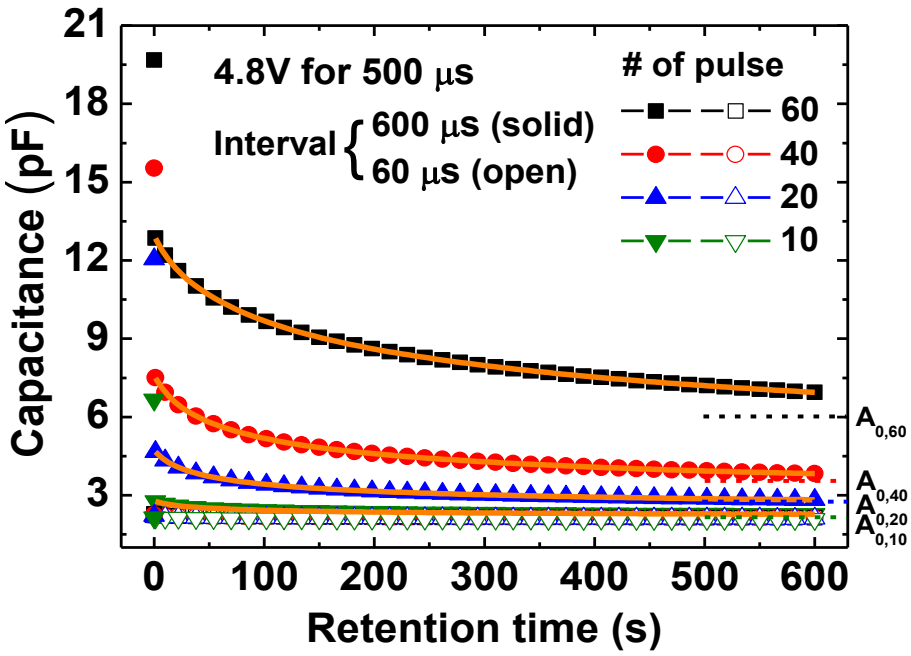
(b)


4.8 V for 50 μs
4.8 V for 100 μs
4.8 V for 500 μs
Interval
600 μs (solid)
60 ms (open)
Capacitance (pF)
0
4
8
12
16
20
24
Pulse amplitude
Interval
Pulse width
C-t measurement
0
10
20
30
40
50
60
# of pulse

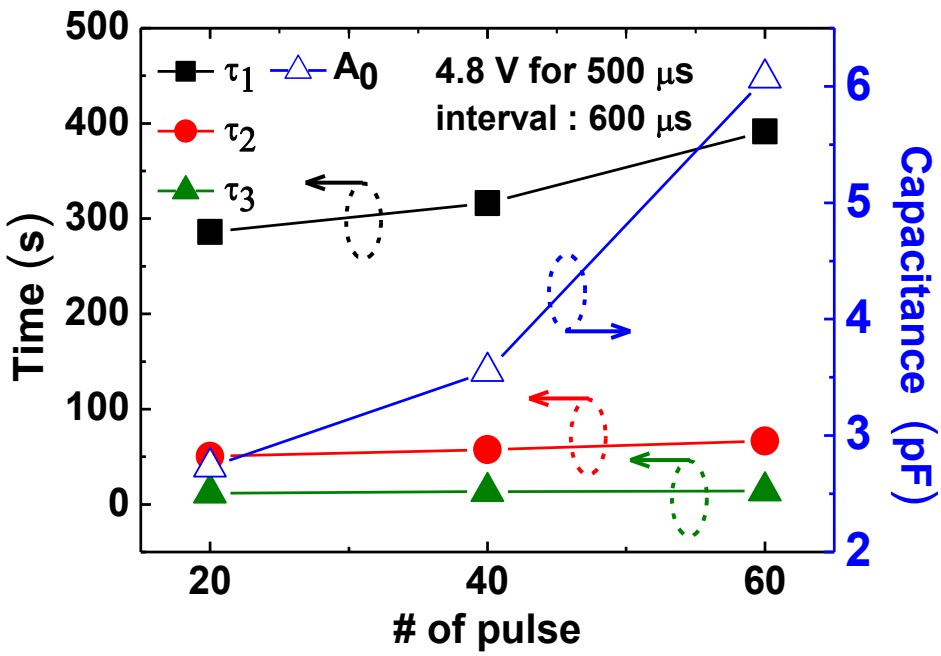
(c)

Fig. 2.6 *C-V* characteristics of the gate stack depending on the number of applied programming pulses (4.8 V for 500 μs) with time intervals of (a) 600 μs and (b) 60 ms between the pulses. (c) Capacitance change characteristics after consecutive program pulses with different pulse widths and time intervals and the applied voltage pulse profile (inset) for the capacitance-time (*C-t*) measurements. Solid marks and error bars for the interval of 600 μs represent the mean and standard deviation (SD), respectively, from measured data in about 100 samples

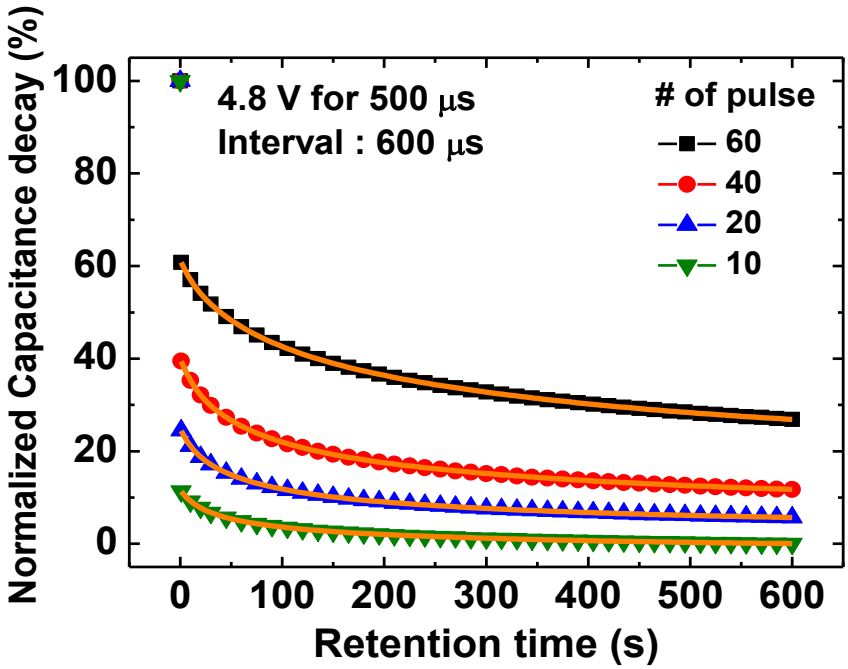
However, there are no remarkable changes for the program condition with the relatively long time interval (60 ms), as shown in Fig. 2.6(b). Thus, these results imply the injected charge after the program operation is easily discharged within about 60 ms. This characteristic can be utilized for STP under the program condition. Using the measurement method shown in the inset of Fig. 2.6(c), we can observe capacitance changes at the read bias depending on the pulse widths and time intervals. This manifests more accurate charge variations in the A/H/N dielectric stack compared to the C-V measurement after the operation of the program, as shown in Fig. 2.6(a) and (b).


4.8V for 500 μs
Interval { 600 μs (solid)
60 μs (open)
# of pulse
60
40
20
10
Capacitance (pF)
Retention time (s)
A0,60
A0,40
A0,20
A0,10

(a)


τ1
τ2
τ3
A0
4.8 V for 500 μs
interval : 600 μs
Time (s)
Capacitance (pF)
# of pulse

(b)



(c)

Fig. 2.7 (a) Retention characteristics of the gate stack after applying repeated pulses of 4.8 V for 500 μs with the time intervals of 600 μs and 60 ms at a gate voltage of -0.2 V. The third-order decay fits [i.e., $A_0 + A_1\exp(-t/\tau_1) + A_2\exp(-t/\tau_2) + A_3\exp(-t/\tau_3)$] for the pulse interval of 600 μs are also plotted with solid lines except for the first dots measured after the time intervals from the final stimulation in each condition. The other symbols are the data measured after 1 s from the falling edge of the final stimulation pulse. (b) Changes in the characteristic time constants (τ_1, τ_2, τ_3) and synaptic weight (A_0) in accordance with the number of stimulations (20 to 60). (c) Normalized decay properties when repeated input pulses (4.8 V for 600 μs) are applied with a time interval of 600 μs to the device depending on the number of stimulations.

In the following section, we demonstrate a STP to LTP transition and a synaptic strength-enhancing effect in the proposed stack upon consecutive stimulations through *C-t* measurements. The device states were nearly identical to the initial state according to the measured device shown in Fig. 2.6. A read voltage of -0.2 V was applied to minimize disturbance on the charge variation of the device for the measurements shown in Fig. 2.6(c). An increase in the capacitance during the *C-t* measurement indicates an electron injection from the substrate to the gate stack in the measurement condition. Because there is no tunnel oxide layer below the nitride layer, the trapped charge is spontaneously detrapped to the substrate easily after the application of a voltage pulse. Thus, when the time interval between the stimulation is relatively long (60 ms), there are no significant changes in the capacitances, even after applying repeated pulses with a long width (4.8 V for 500 μs) as many as 60 times. However, more frequent stimulations lead to a gradual increase in the capacitance despite the spontaneous charge loss, as the time interval between the stimulation pulses is not long enough for the injected charge to detrap and return to its initial state, resulting in a net capacitance

increase.

STP and LTP can be classified according to the memory retention characteristics. STP is momentarily sustained by repeating the same stimulus, whereas LTP, in spite of the presence of spontaneous discharging, can be maintained for a far longer period of time without subsequent stimulations. The conversion from STP to LTP is also accomplished through iterative rehearsals, which is analogous to biological synaptic behavior in which the strength of a synaptic connection is dependent on the time interval between the stimulations [13]. Figure 2.7(a) shows the charge retention properties for 600 s after applying consecutive input pulses of 4.8 V for 500 μs with time intervals of 600 μs and 60 ms. The trapped charge over time decays rapidly at the beginning, after which the decay rate declines. In addition, when the number of stimulations is increased, the charge decay rate slows down and the increased capacitance value is sustained for a longer time. Consequently, the proposed stack shows a significant improvement in the retention time which is strongly related to the stimulation rate and the number of pulses. The short-lived charge loss can be attributed to the trapped

charge at the near Si/Si_3N_4 interface, while the long-lasting retention characteristic likely originated from the charge trapped at the HfO_2/Si_3N_4 interface or HfO_2 bulk layer [14]. We think that the transition from STP to LTP starts when the injected charge is trapped deep inside the nitride layer, the HfO_2/Si_3N_4 interface, and/or HfO_2 bulk layer. In addition, the decay lines of the *C-t* curves do not show a simple first-order stretched exponential decay fit {i.e., $A_0\exp[(-t/\tau_1)^{\beta}]$} in Fig. 2.7(a). The long-lasting retention characteristic has three different slopes [i.e., $A_0 + A_1\exp(-t/\tau_1) + A_2\exp(-t/\tau_2) + A_3\exp(-t/\tau_3)$] in the measured *C-t* curves [the solid lines in Fig. 2.7(a)], which indicates more than a single dominant type of trap [15]. In addition, the characteristic time constants (τ_1, τ_2, τ_3) and synaptic weights (A_0) increase gradually as the number of rehearsals is increased, as potted in Fig. 2.7(b), which indicates that LTP is enhanced. Specifically, the fitting parameter of A_0 in Fig. 2.7(a) indicates a long-lived factor for LTP. The relative decay rate is also alleviated by increasing the input pulses, as shown in Fig. 2.7(c). Phenomena similar to these results have also been observed in other synaptic devices [7]-[9].

In order to examine the reliability of our stack structure at a high temperature

for LTP, the retention properties were investigated. In Fig. 2.8, the retention measurements were carried out for the proposed stack at 80 ℃ after applying 60 pulses of 4.8 V for 250 µs with a time interval of 600 µs. Here, the program condition was intentionally determined for the same charge injection performed by applying 4.8 V for 500 µs at room temperature. Although there is some charge loss for 5000 s, the remaining charge is sufficient to serve as LTP, and longer lasting memory can be implemented if the number of stimulations is increased. It should be noted that the gate stack in this work can easily be implemented in FETs, where we can detect the drain current with time instead of using the capacitance.

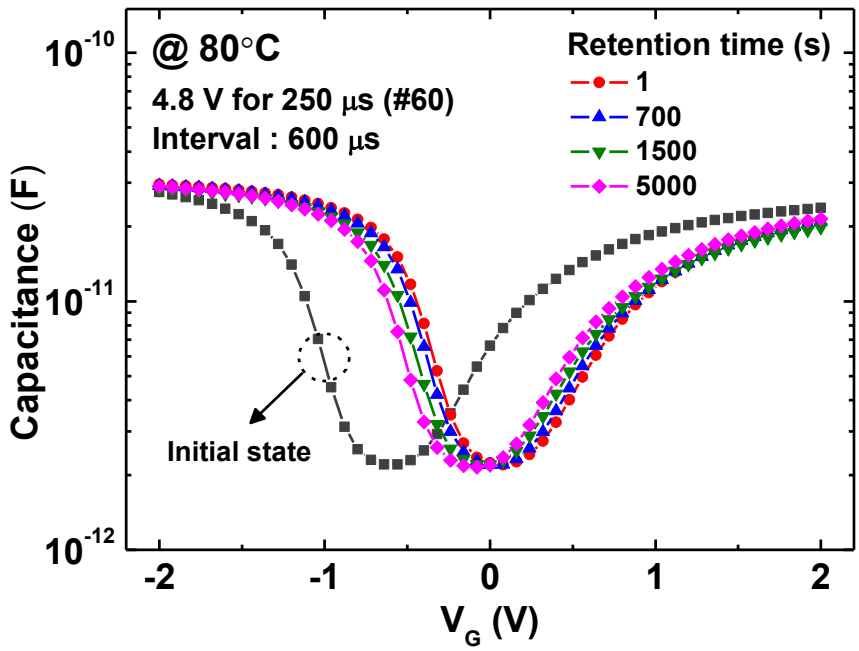


Fig. 2.8. Retention characteristics of the gate stack after programming with consecutive 60 pulses of 4.8 V for 250 μs with the time interval of 600 μs at 80 ℃.

Chapter 3

Analysis of charge trapping and retention mechanism

3. 1 Introduction

In this chapter, charge trapping characteristics of thin LPCVD Si_3N_4, atomic-layer deposited HfO_2 films with Al_2O_3 as a blocking oxide and Al metal gate on p-Si substrates in the MAHNS memory structure have been investigated. We suggest a model for electron-trapping phenomena and charge transport mechanism. The model suggests that electron trapping is caused by contributions from two different processes: fast transient resonant trapping of the injected channel electrons near the Si_3N_4/Si interface and electron hopping between the traps or trap assisted tunneling, which is responsible for the long lasting V_t shift when the consecutive input pulses are frequent with long pulse width. Analysis of each of these electron-trapping processes, which can be separated based on their different characteristic times according to the trap positions in the gates gate stack. This

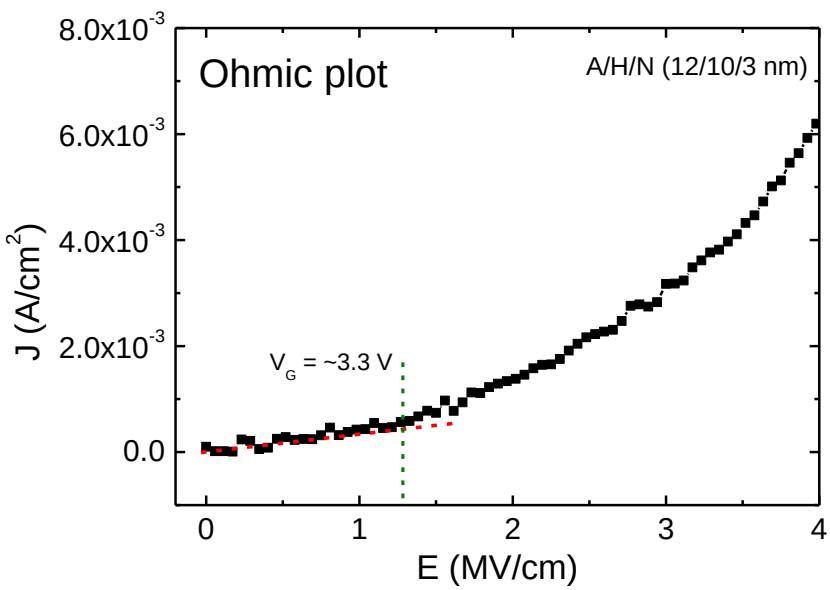
also provides insight into the origin of STP and LTP with their transition effect.

3. 2 Measurement and Discussion

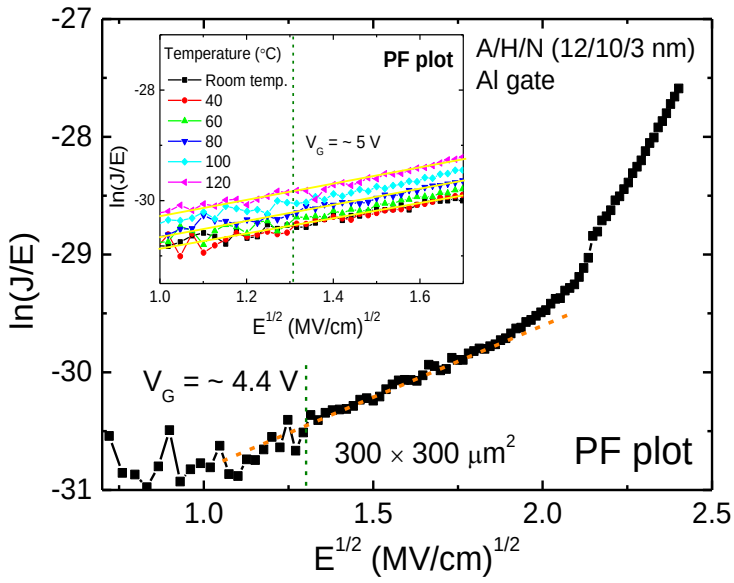
The I_g-V_g measurements are carried out by Agilent B1500 semiconductor parameter analyzer for investigating the current transport mechanism of A/H/N (12/10/3 nm) gate stack. Fig. 3.1 show ohmic, poole-frenkel (PF) and Fowler-Nordheim (F-N) tunneling fitting plots depending on intensity of the electric field in I_g-V_g curve. When the electric field is relatively low, the I_g-V_g curve shows the ohmic property. As the electric field is higher, the transport mechanism changes from PF emission to F-N tunneling, which is consistent with the current transport characteristics in Metal/high-k dielectrics/Si (MIS) capacitors (Si_3N_4, HfO_2, Al_2O_3) [30-32].

We also proposed possible energy diagram schemes for charge trapping and retention mode when electrons are trapped in S_3N_4 or HfO_2 layers in A/H/N stack as shown in Fig. 3.2 and 3.3, respectively. When the gate bias is applied, the channel electrons can be trapped into nitride or HfO_2 by tunneling or PF conduction mechanism. Since there is no tunneling barrier from Si substrate to the two charge storage layers, electrons can be easily trapped in trap sites in nitride or HfO_2 layers. Also, the high interface trap density between nitride and the Si

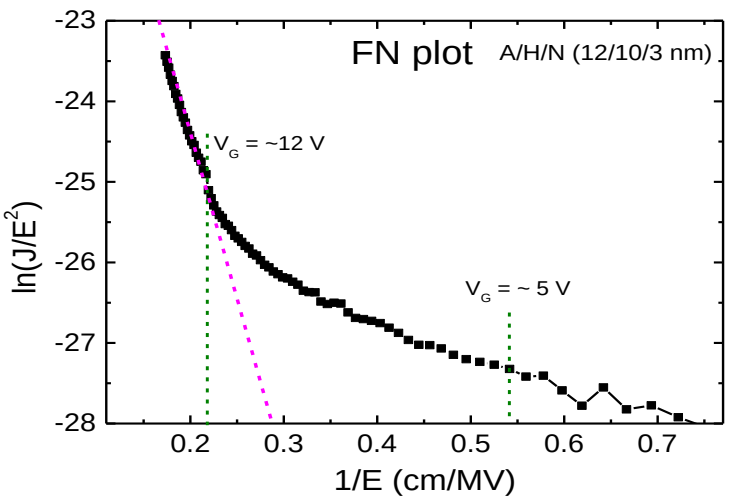
substrate induce trap-assisted tunneling (TAT) and the charge trapping efficiency can be enhanced even in the relatively low gate bias. Generally, interface trap density between silicon and high-k materials such as Si_3N_4, Al_2O_3, HfO_2 is higher than thermally grown SiO_2. Stoichiometric silicon nitride (Si_3N_4) has an intrinsic tensile stress of about 910 Mpa at room temperature. If it is applied in direct contact to silicon, this intrinsic tensile stress can result in a high mechanical stress in the underlying silicon. On the other hand, charge loss of the gate stack is relatively serious because no tunneling barrier exists between Si substrate and the charge storage layers. The trapped charge near Si/Si_3N_4 interface is mainly emitted by tunneling (direct tunneling or TAT).



(a)



(b)



(c)

Fig. 3.1 (a) Ohmic plot in the region of low electric field, (b) PF emission plot for medium electric field region and (c) F-N tunneling plot in the high gate bias condition. The inset of (b) represents the *I-V* curves at different temperatures.

A thermal excitation can be dominant for the trapped electrons located deep inside the gate stack especially in HfO_2 as depicted in Fig. 3.3.

Charge trapping into the trap centers is controlled by a trap energy distribution, doping concentration and bias conditions, which define a carrier quasi Fermi-level location inside a semiconductor band gap. It dynamically changes due to a carrier capture or emission by or from a trap. The trap capture cross-section is an important parameter that defines the charge-trapping dynamics and the carrier recombination rate through a trap. The effective trap time constant (the time required for a single-trapping or de-trapping event) can be estimated as

$$\tau_{trap} = \frac{1}{N_t v_{th} \sigma}$$

where N_t is the trap concentration, v_{th} is the thermal velocity and σ is the trap capture cross-section [33]. The trap capture cross section of nitride is relatively smaller than that of HfO_2 as shown in table 3.1, which is a more dominant factor for the trap occupation compared to the trap densities difference between them [34-40]. We can estimate that the electron trapping event occur more easily in nitride layer compared to HfO_2.

In the retention mode, the four terminals (gate, source, drain, substrate) are

grounded. The trapped charge loss mainly occurs by four process which are trap-to-band tunneling, trap-to-trap tunneling, band-to-tunneling and thermal excitation [41, 42]. Trapped charge near the silicon surface are emitted to the silicon conduction band or Si/ Si_3N_4 interface states by trap-to-band and trap-to-trap tunneling processes. Holes from the silicon valence band can be injected into nitride traps by band-to-trap tunneling due to the internal electric field. The trapped electrons in the shallow trap level from nitride or HfO_2 are thermally emitted to the conduction band, which is followed by drift conduction and tunneling to the silicon substrate. However, the traps in the deep level states cannot be easily emitted by the thermal excitation. The related physical equations are followed.

(1) Band-to-trap tunneling

$$\tau_{B-T}(x) = \tau_{B-T_0} e^{\alpha^{h}_{ox} x_{OT}} e^{\alpha_n{}^{h} x} \quad (\tau_{T-B_0} = 10^{-12} \sim 10^{-13}\,\mathrm{s})$$

$$\alpha^{h}_{ox} = \frac{2\sqrt{2qm^{*}_{ox,h}\phi^{h}_{1}}}{\hbar},$$

$$\alpha^{h}_{n} = \frac{2\sqrt{2m^{*}_{n,h}(E_{GN} - E_{TD})}}{n\hbar}$$

(2) Trap-to-trap tunneling

$$\tau_{T-T}(x) = \tau_{T-T_0} e^{2\eta_{ox} x_{OT}} e^{2\eta_n x}$$

$$\tau_{T-T_0} = \frac{m^*_{ox,e}{}^2 x_{OT}\left(1+\frac{1}{2\eta_{ox}x_{OT}}\right)}{2\pi^2\eta_{Si}\hbar^3\overline{D_{it}}},$$

$$\eta_{ox} = \frac{\sqrt{2m^*_{ox,e}(q\phi^e_2 + E_{TD})}}{\hbar},$$

$$\eta_n = \frac{\sqrt{2m^*_{n,e}E_{TD}}}{\hbar},$$

$$\eta_{Si} = \frac{\sqrt{2m^*_{Si,e}(E_{TD} - q(\phi^e_1 - \phi^e_2))}}{\hbar}$$

(3) Trap-to-band tunneling

$$\frac{1}{e^-_{nt}} \equiv \tau_{T-B}(x) = \tau_{T-B_0} e^{\alpha^e_{ox}{}^h x_{OT}} e^{\alpha_n{}^e x},$$

$$\alpha^e_{ox} = \frac{2\sqrt{2m^*_{ox,e}(q\phi^e_2 + E_{TA})}}{\hbar},$$

$$\alpha^e_n = \frac{2\sqrt{2m^*_{n,e}E_{TA}}}{\hbar}$$

(4) Thermal excitation

$$\tau_{th} = \frac{1}{AT^2 e^{-\frac{E_{TA}}{k_B T}}} = \frac{1}{e^-_{ntho} e^{-\frac{E_{TA}}{k_B T}}},$$

$$A = 2\sigma_n\sqrt{\frac{3k_B}{m^*_{n,e}}}\left(\frac{2\pi m^*_{n,e}k_B}{h^2}\right)^{3/2}$$

From these relationships, tunneling components for retention properties are strongly dependent on the distance (X_{OT}) from the silicon surface in the A/H/N stack. On the other hand, the thermal emission component is related to the trap energy level (E_T) which is independent on the spatial position of trapped charge. When repeated pulses are applied to gate, electrons are continuously injected to the gate stack from the silicon channel while the discharge of the trapped charge also occurs especially by tunneling process. Most of injected charges are trapped in nitride layer but some electrons can be trapped in HfO_2 layers as the input pulse are consecutively applied to the gate. Actually, the value of the capture cross section for nitride is larger than HfO_2, which can lead to the electron trapping efficiency as shown in Table. 3.1. Thus, the injected electrons are mainly captured in the nitride trapes but they are easily deptrapped by tunneling components, which cause short-term plasticity (STP) characteristic. As the number of program pulses increases, the part of injection carriers can be captured in HfO_2 layer and trap-to-trap tunneling also enhances the charge trapping into deep inside of the gate stack. The defect energy band in HfO_2 is deeper from the conduction band

edge compared to nitride. Therefore, it can be explained that charge loss is dominant for consecutive stimulation with a long time interval while frequent stimulation help charge trapping in HfO2 layer, which can make an implementation of long-term potentiation (LTP).

Carrier	Material	Effective mass	N_t [cm^{-3}]	σ_T [cm^2]	E_T [eV]
Electron	Nitride	$0.36m_0$	Gaussian, 3.5×10^{19}	1×10^{-13}	1.5 (from CB)
Hole	Nitride	$0.38m_0$	Uniform, 1×10^{19}	1×10^{-13}	2.5 (from VB)
Electron	HfO_2	$0.18m_0$	Uniform, 4.5×10^{19}	1×10^{-14}	1.4-2.7 (from CB)
Hole	HfO_2	$0.2m_0$	Uniform, 7×10^{18}	1×10^{-14}	2.6-3.4 (from VB)

Table 3.1 Main physical parameters for nitride and HfO_2

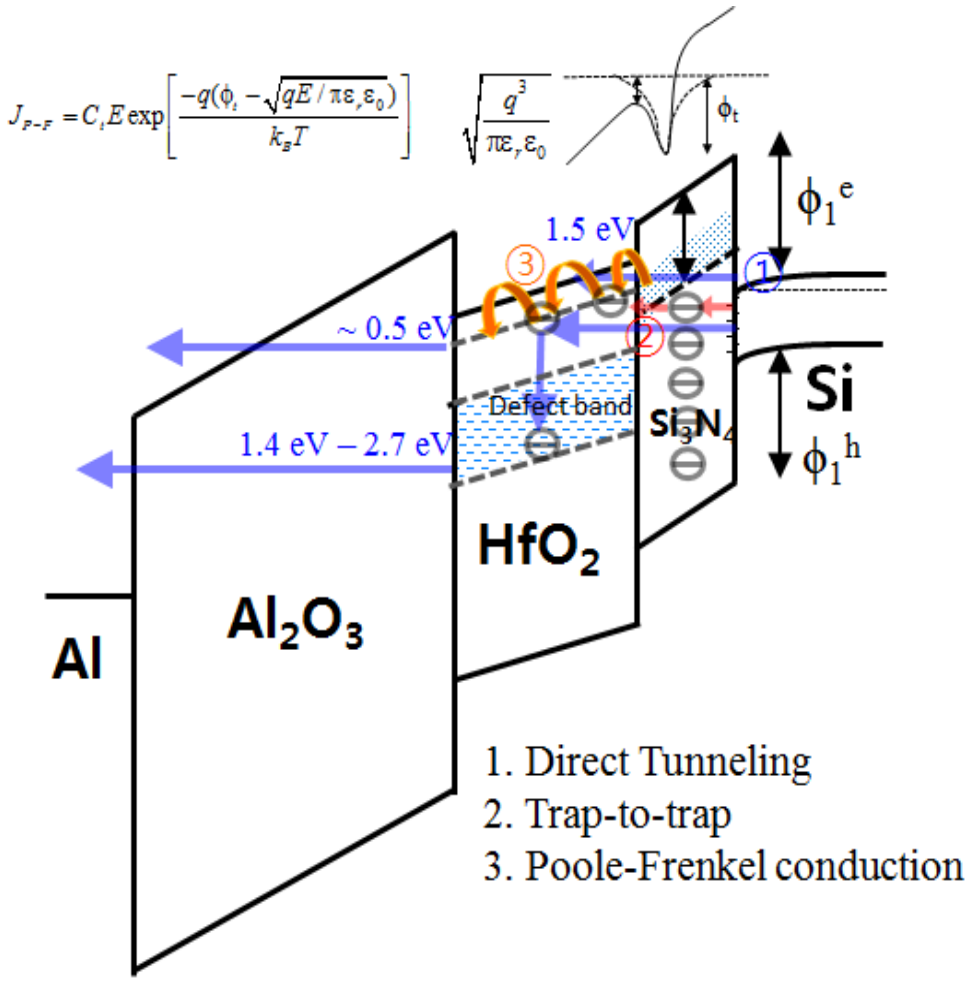


Fig. 3.2 Schematic of the energy band diagram with the proposed electron trapping processes when a positive bias is applied to the gate.

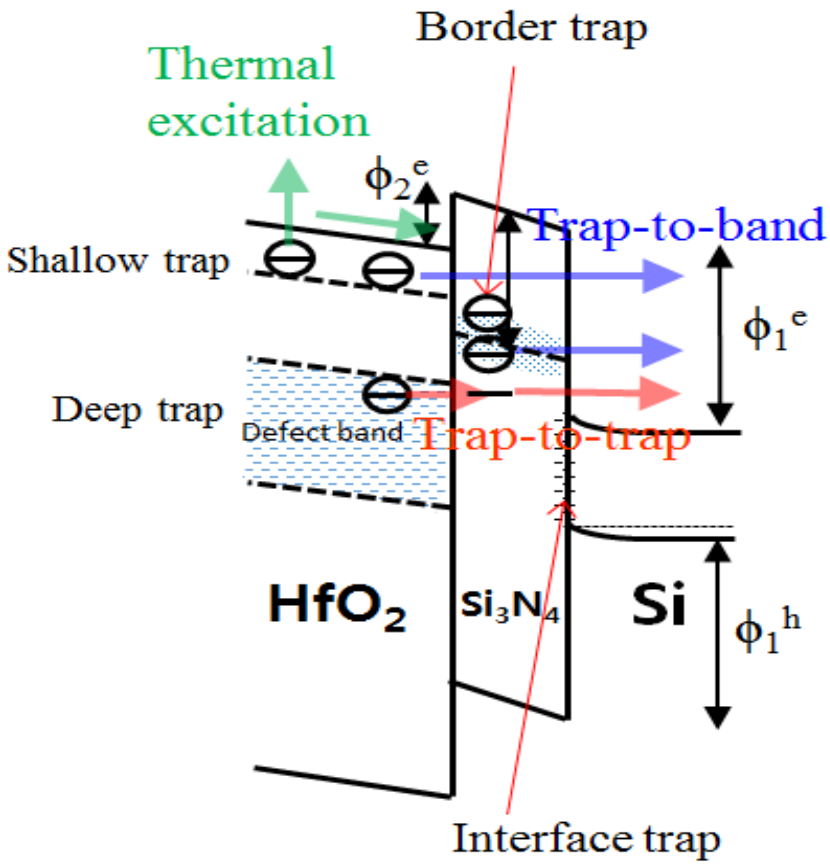


Fig. 3.3 Schematic of the energy band diagram for the electron emission in the retention mode

Chapter 4

Synaptic characteristics in a FET device

4. 1 Fabrication process of a FET device

N-type FET devices with different gate stacks were fabricated using the conventional CMOS process technology. The pad oxide (SiO_2) (～120 Å) was thermally grown on 6 inch p-type silicon wafers, followed by the deposition of Si_3N_4 (~1600 Å) using LPCVD process. Before these steps, the standard RCA cleaning (SPM, SC1, SC2) was carried out for silicon wafers. The active area was patterned with dry etching with a photolithography process. Then, local oxidation of silicon (LOCOS) was grown by wet oxidation process at 1000 ℃ in which the field implantation was performed in advance. A channel and source/drain implantation were carried out before the deposition of gates stacks since high-κ dielectrics are easily influenced by high temperature thermal process such as an annealing for the dopant activation. Before the deposition of the first layer of the gate stack (Si_3N_4), 100:1 DHF dipping was carried out for the elimination of a native oxide. Then, High-κ gate dielectric stack (HfO_2, Al_2O_3) or oxide layer were

deposited by atomic layer deposition technique. After that, a metal gate electrode was deposited using physical vapor deposition (PVD) method. Finally, the gate metal was patterned using lithography and dry etching technologies. The key fabrication process is shown with a schematic diagram in Fig. 4.1. LOCOS is well formed as can be seen in Fig. 4. 2.

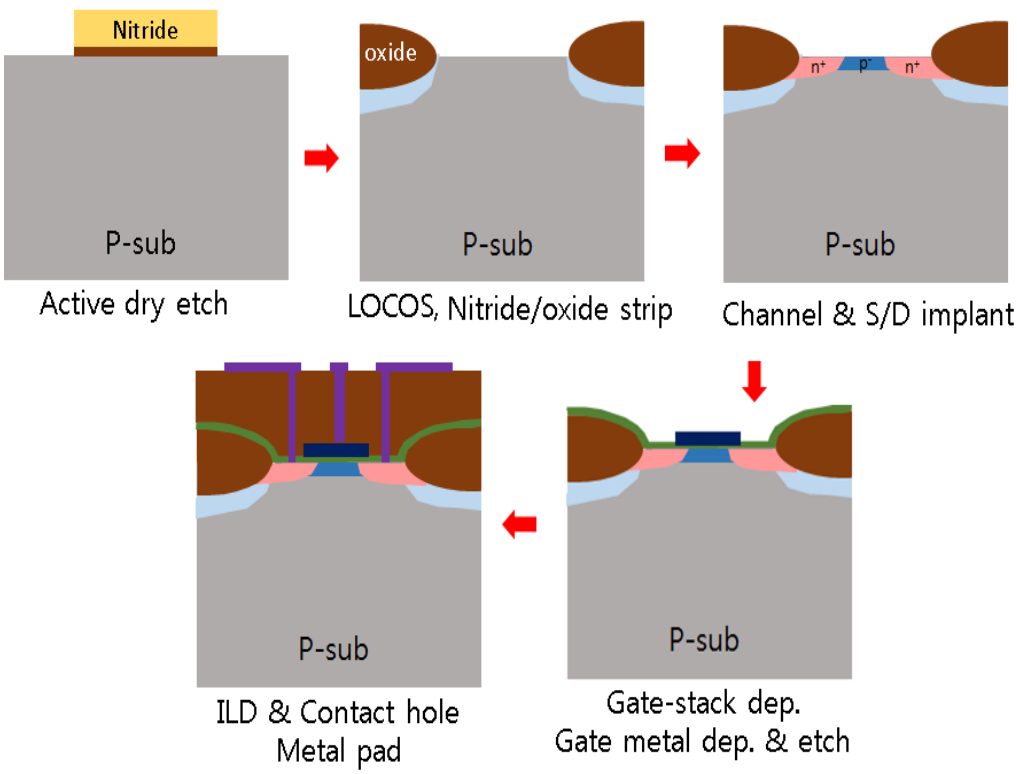
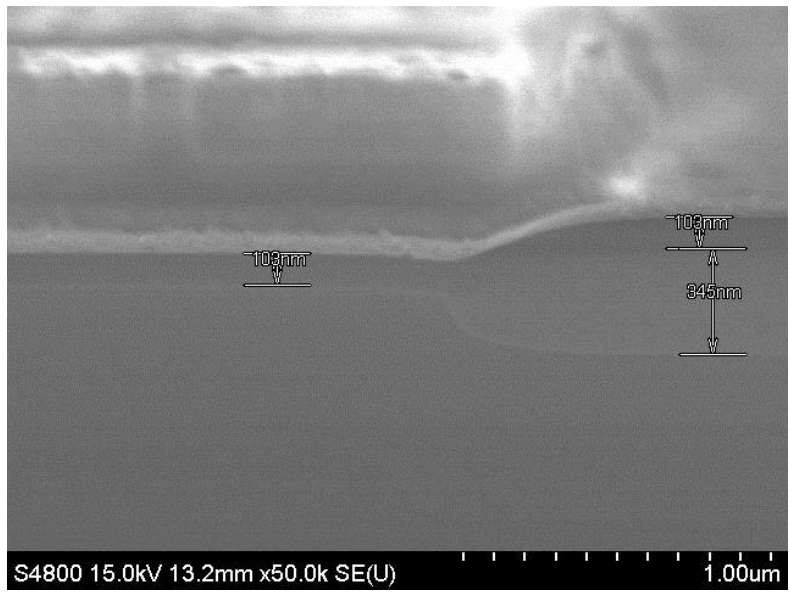
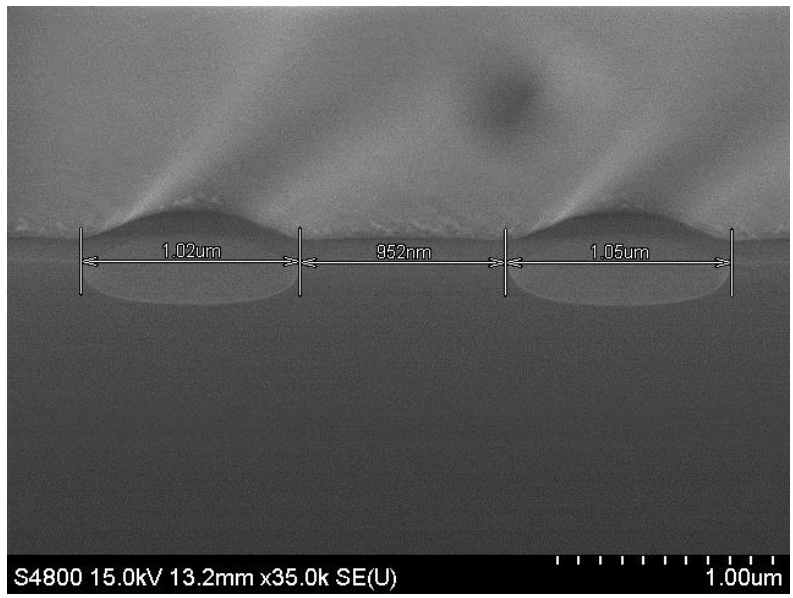


Fig. 4.1 Schematic of key process for a FET device



(a)



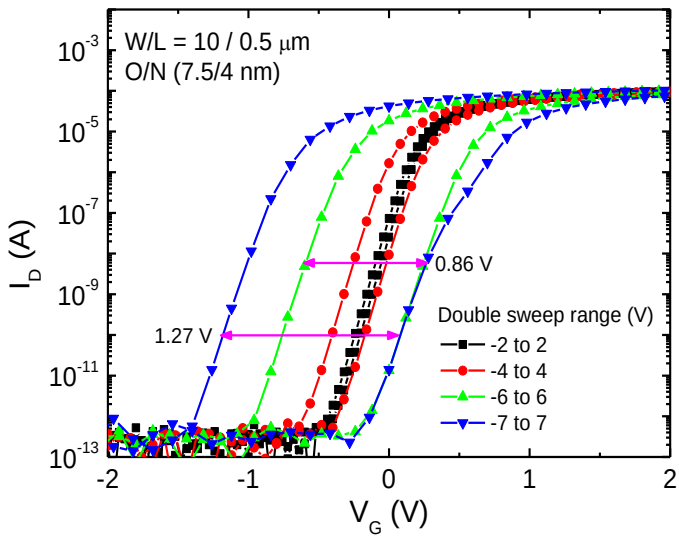
(b)

Fig. 4.2 SEM images of LOCOS region. Bird's beak length is ~ 200 nm.

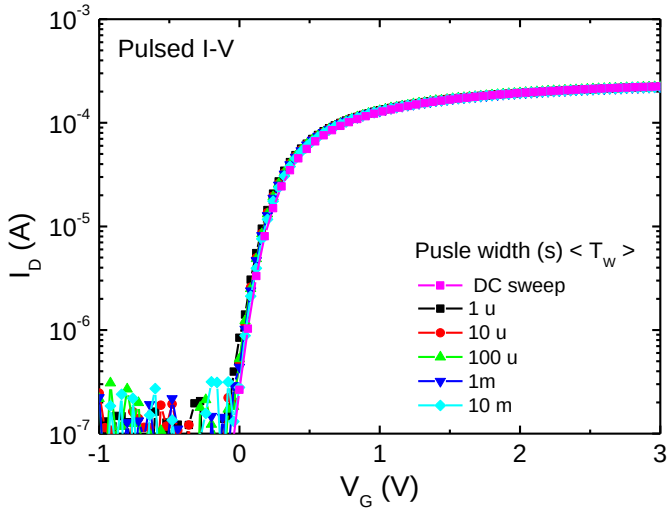
4. 2 Characteristics of SiO_2/Si_3N_4 (O/N) stack

To investigate nitride layer properties except HfO_2 as a charge storage layer, we prepared two FET devices having SiO_2/Nitride (O/N) gate stacks with different nitride thicknesses (~4, ~6 nm). Firstly, silicon nitride (Si_3N_4) layer was deposited by LPCVD process at 750 ℃. Then, the blocking oxide (~ 7.5 nm) is grown by thermal oxidation at 850 ℃. TiN metal gate was used for the O/N gate stack.

Figure 4.3 shows I_D-V_G characteristics of the fabricated device with DC measurement and pulsed *I*-*V* technique. Basically, hysteresis behavior is observed owing to the interface states between nitride and silicon substrate as shown in Fig. 4.3 (a). As the sweep range increases, hysteresis phenomenon becomes more serious and ΔV_{th} is about 1.27 V in the case of -7 to 7 V. This hysteresis comes from electron trapping and detrapping during the measurement. When the measurement time is reduced for read operation by pulsed *I*-*V* measurement, the charge trapping can be reduced as depicted in Fig. 4.3 (b). Figure 4.4 represents transient I_D properties after applying 5 V for different pulse widths. A read voltage



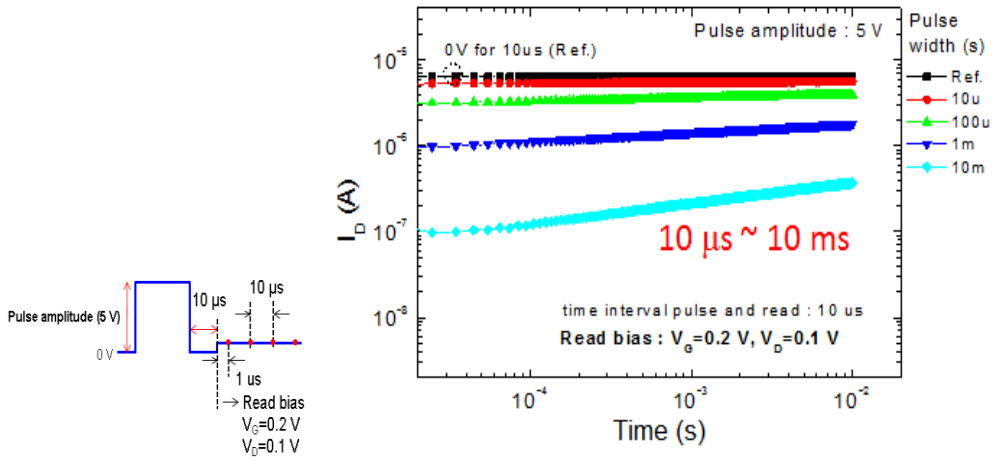
(a)



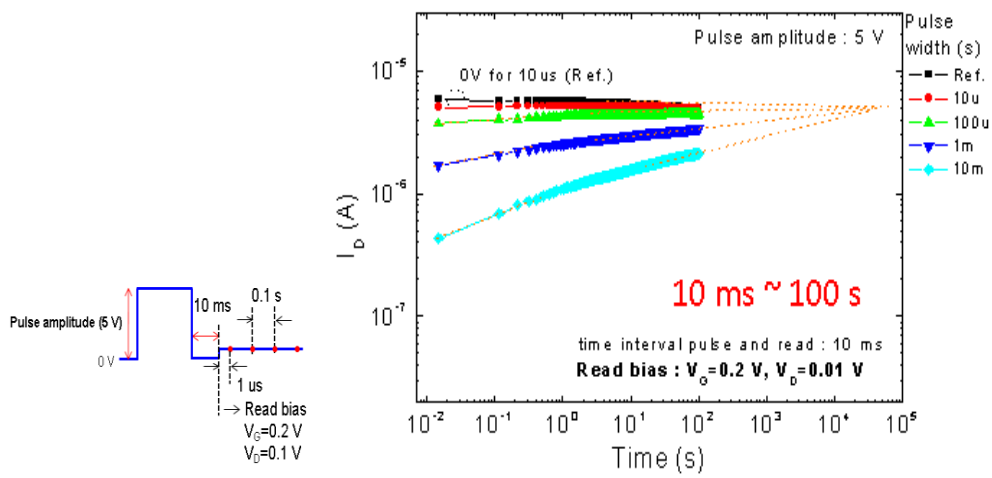
(b)

Fig. 4.3 (a) I_D-V_G characteristics with hysteresis behavior (DC double sweep)

(b) Pulsed I_D-V_G curves



(a)



(b)

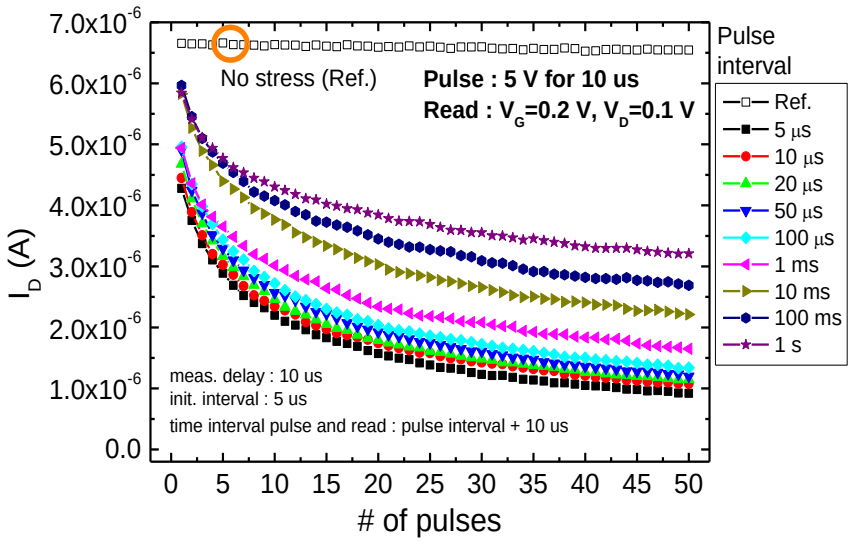
Fig. 4.4 Retention properties after applying a pulse (5 V) as a parameter of pulse width

of 0.2 V is applied and its influence to the I_D transient is negligible as shown in Fig. 4.4 (a) and (b). In these figures, fast decay curves are observed and long pulse width leads to better retention characteristic with a larger current change. In this case, tunneling process is a dominant retention mechanism since there is no tunneling oxide and the thickness of nitride is thin. When input pulses are applied repeatedly, I_D current changes gradually as shown in Fig. 4.5. Here, charge loss occurs simultaneously with charge trapping under repeated stimulation. Because charge decay is more serious for longer interval time, the I_D variation increases as the pulse time interval becomes short. When the pulse width is larger, drain current variation is large even for the small number of pulses as compared between Fig. 4.5 (a) and (b). In addition, when the number of stimulations is increased, the charge decay rate slows down and the changes of drain current values arer relatively decreased.

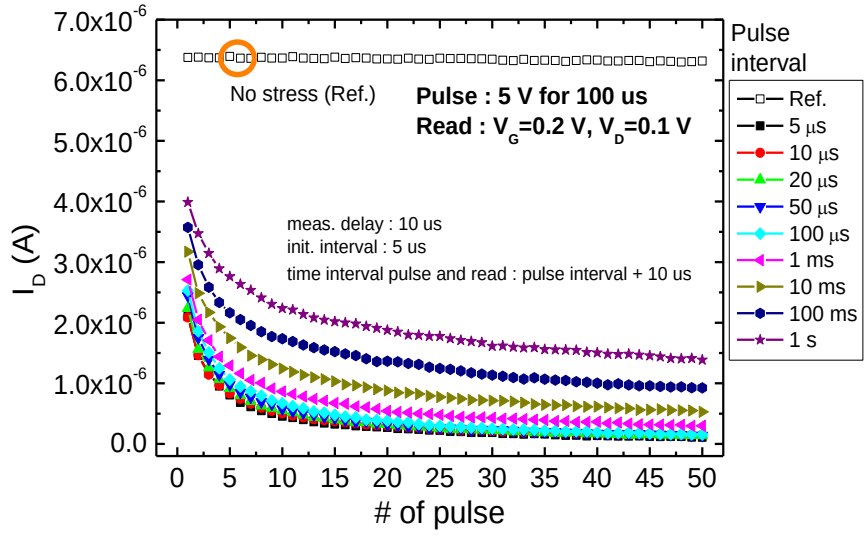
Figure. 4.6 shows retention characteristics with different pulse number, pulse interval time and input pulse conditions. As shown in Fig, 4.6 (a) and (b), the increased pulse width induces larger charges. When negative bias is applied,

accumulated holes in the silicon substrate are trapped into the nitride layer. The trapped holes are also easily emitted for a short time as shown in Fig. 4.6 (c). Time interval dependence can be seen for the three input conditions for short period of time while the decay curves are nearly same after about 1 s. When stimulation pulses are repeatedly applied, more electrons are captured but charge loss happens spontaneously. An internal electric field helps electron detrapping process for a short period of time, which makes the current decay differences for the different time interval conditions. When the remained electrons are similar in the retention mode for different intervals, charge loss rate are nearly same as shown in Fig. 4.6.

Consequently, the retention characteristics of the O/N stack indicates that nitride layer shows short-lived memory properties. However, there is no a time interval dependence and transition characteristic from STP to LTP even when many frequent consecutive pulses are applied to the device. The transient properties for a thicker nitride layer (~ 6 nm) in O/N stack also show similar phenomena as depicted in Fig. 4.7.

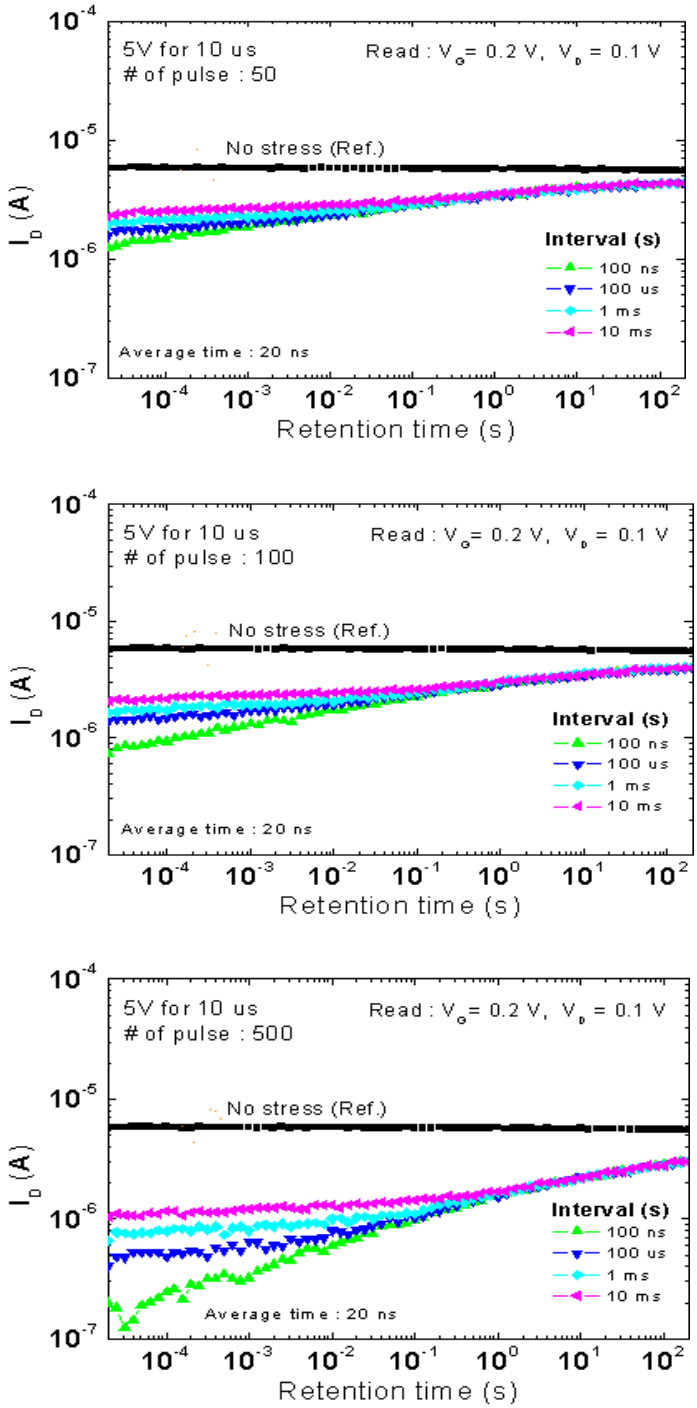


(a)

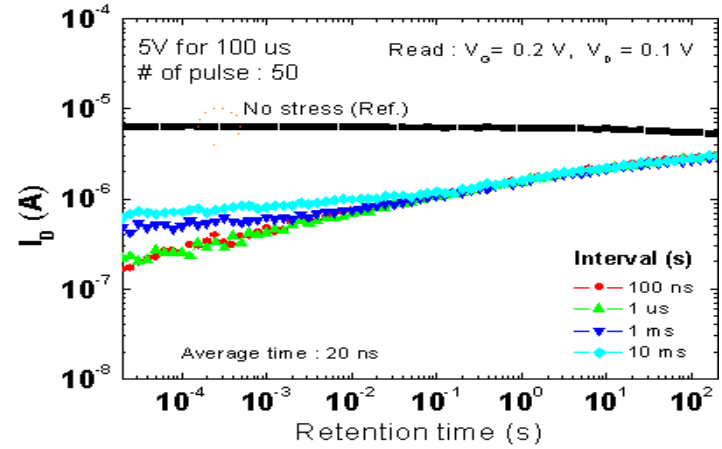


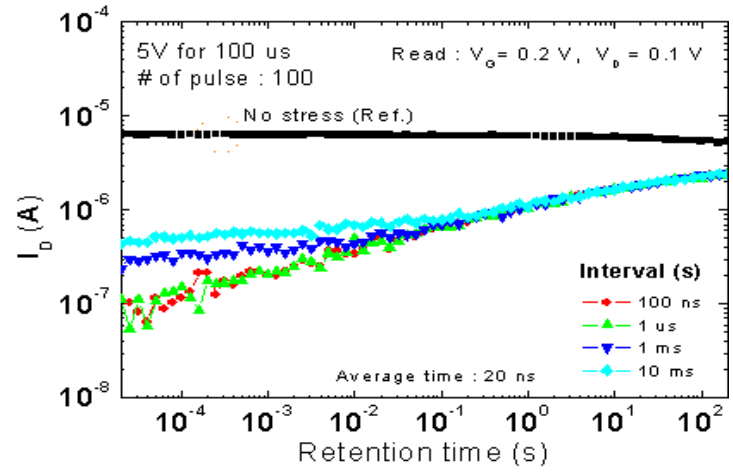
(b)

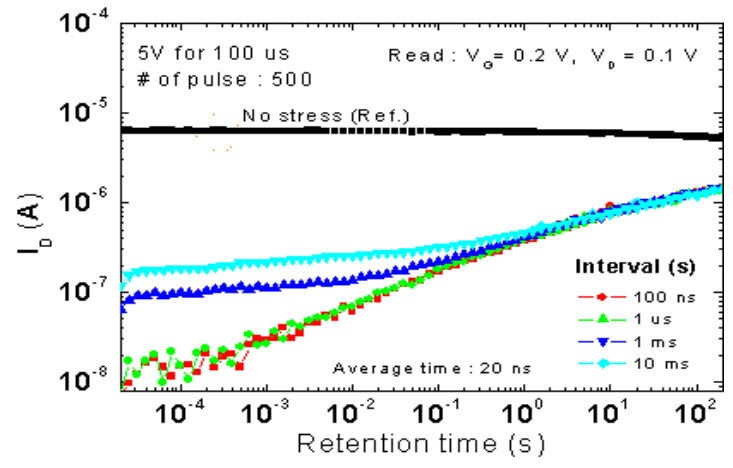
Fig. 4.5 Transient I_D properties of the O/N (7.5/4 nm) stack depending on the number of applied pulses as a parameter of time intervals.


5V for 10 us
# of pulse : 50
Read : V_G= 0.2 V, V_D = 0.1 V
No stress (Ref.)
Interval (s)
100 ns
100 us
1 ms
10 ms
Average time : 20 ns
I_D (A)
Retention time (s)
5V for 10 us
# of pulse : 100
Read : V_G= 0.2 V, V_D = 0.1 V
No stress (Ref.)
Interval (s)
100 ns
100 us
1 ms
10 ms
Average time : 20 ns
I_D (A)
Retention time (s)
5V for 10 us
# of pulse : 500
Read : V_G= 0.2 V, V_D = 0.1 V
No stress (Ref.)
Interval (s)
100 ns
100 us
1 ms
10 ms
Average time : 20 ns
I_D (A)
Retention time (s)

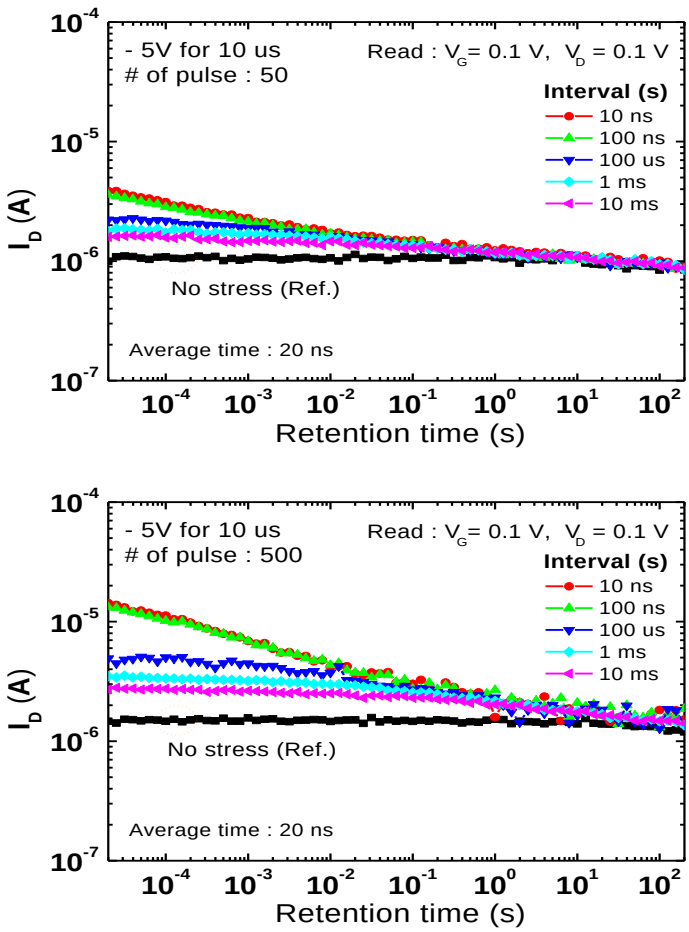
(a)


5V for 100 us
# of pulse : 50
Read : V_G= 0.2 V, V_D = 0.1 V
No stress (Ref.)
Interval (s)
100 ns
1 us
1 ms
10 ms
Average time : 20 ns
I_D (A)
Retention time (s)


5V for 100 us
# of pulse : 100
Read : V_G= 0.2 V, V_D = 0.1 V
No stress (Ref.)
Interval (s)
100 ns
1 us
1 ms
10 ms
Average time : 20 ns
I_D (A)
Retention time (s)

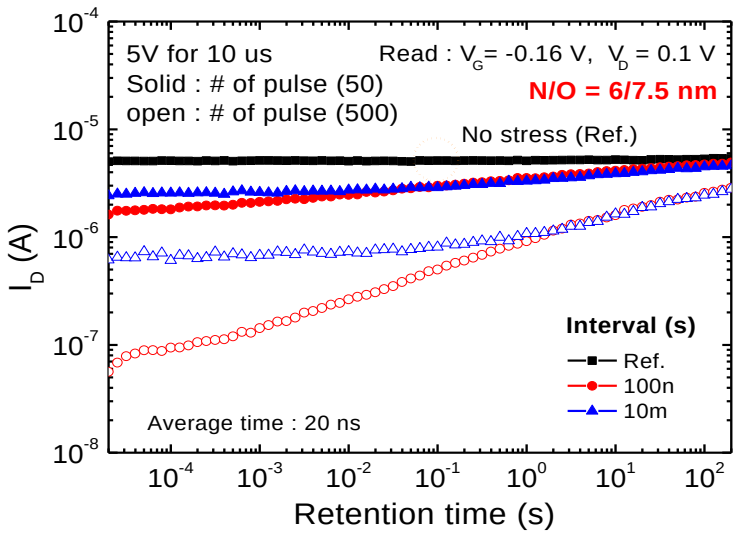

5V for 100 us
# of pulse : 500
Read : V_G= 0.2 V, V_D = 0.1 V
No stress (Ref.)
Interval (s)
100 ns
1 us
1 ms
10 ms
Average time : 20 ns
I_D (A)
Retention time (s)

(b)

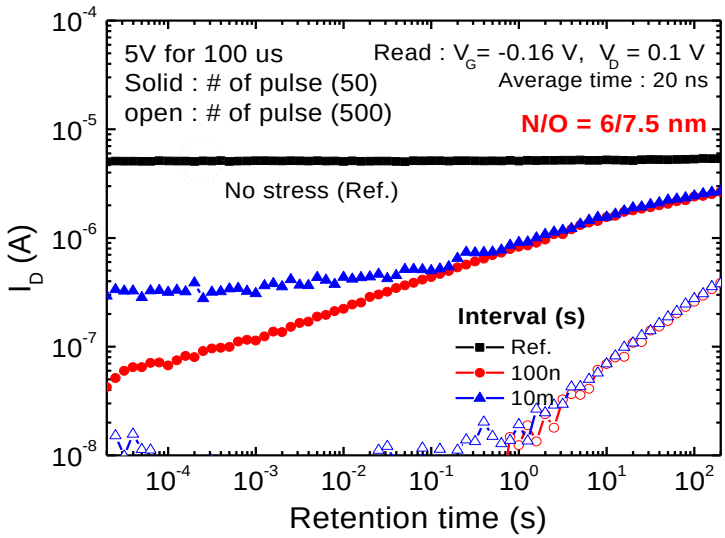


(c)

Fig. 4.6 Retention properties with different pulse conditions which are (a) 5 V for 10 us, (b) 5 V for 100 us and (c) -5 V for 10 us.



(a)



(b)

Fig. 4.7 Retention properties for O/N (7.5/6 nm) stack

4. 3 Scaling of A/H/N gate stack

As mentioned in chapter 1, a scaling of gate stack is important for the next generation of memory technology because it leads to achieve low-power operation. The low-power dissipation is also critical for an implementation of neuromorphic system. In this point of view, we made the proposed A/H/N (12/10/3 nm) gate stack scaled down to A/H/N (9/5/2.6 nm) stack.

The cross-sectional transmission electron microscopy (TEM) image of

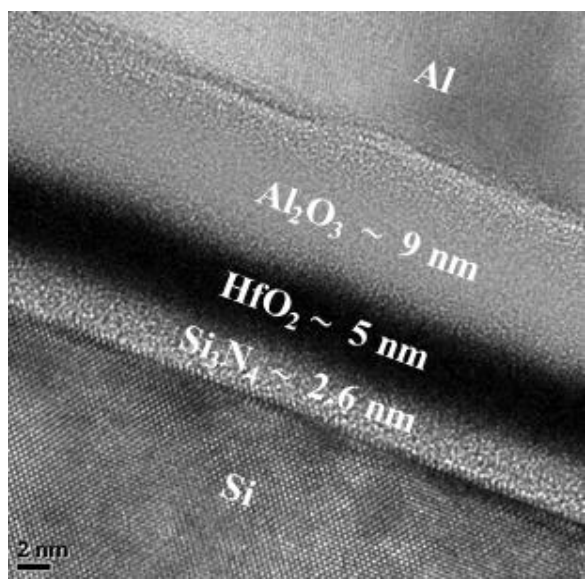


Fig. 4.8 Cross sectional TEM image for A/H/N(9/5/2.6 nm) stack

A/H/N (9/5/2.6 nm) stack is shown in Fig. 4.8.The LPCVD nitride layer was formed immediately after 100:1 DHF dipping for the direct contact formation between silicon substrate and nitride. HfO_2 and Al_2O_3 layer are deposited sequentially by atomic layer deposition (ALD), which is followed by Al deposition with PVD process. During the deposition of the gate stack, we prepared another device having A/N (9/2.6 nm) stack for comparison.

Figure 4.9 shows I_D-V_G curves for the fabricated FET devices with A/H/N (9/5/2.6 nm) and A/N (9/2.6 nm) where similar hysteresis behavior is observed (ΔV_T = ~ 0.3 V). This is originated from Si/Si_3N_4 interface in common. When read operation is carried out for monitoring drain current decay in a retention mode, the read bias can influence the original charge loss of the gate stack. Thus, we proposed a low-stress retention measurement scheme as shown in Fig. 4.10 where the read bias is only applied for a short period of time (10 μs) at each measurement point. We performed transient measurements using the suggested measurement method with different stimulation conditions for a comparison of A/H/N (9/5/2.6 nm) and A/N (9/2.6 nm) stacks. 5 V for 100 μs is applied for

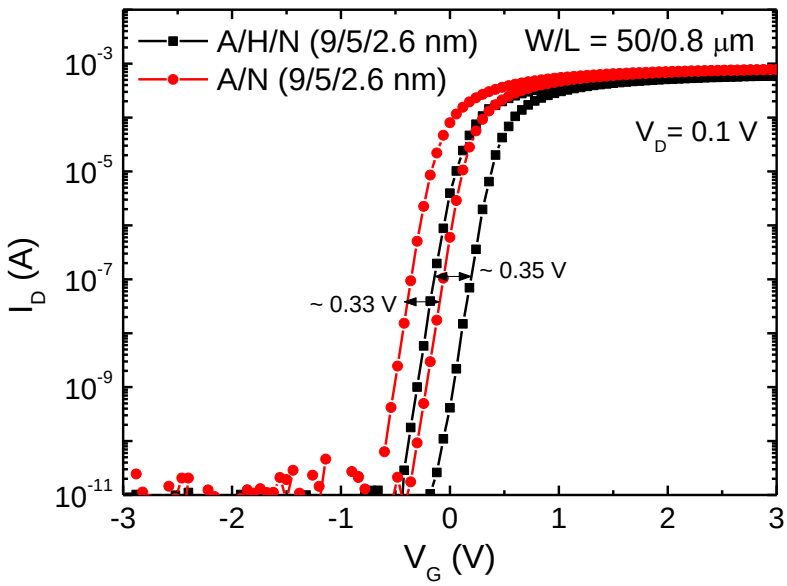


Fig. 4.9 I_D-V_G characteristics for A/H/N (9/6/2.6 nm) and A/N (9/6 nm) stacks

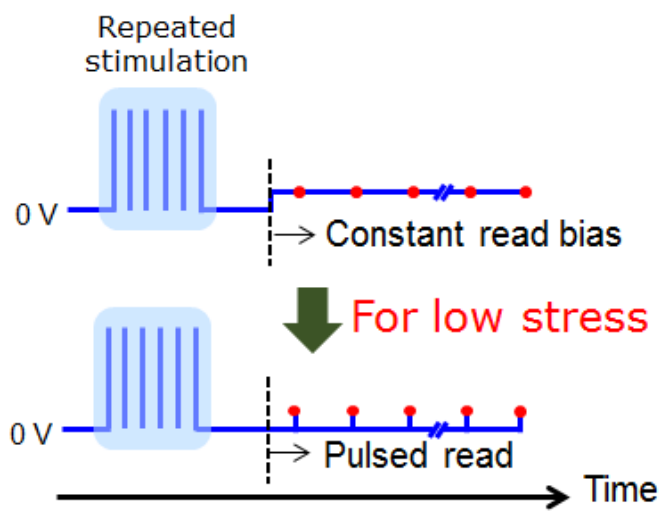


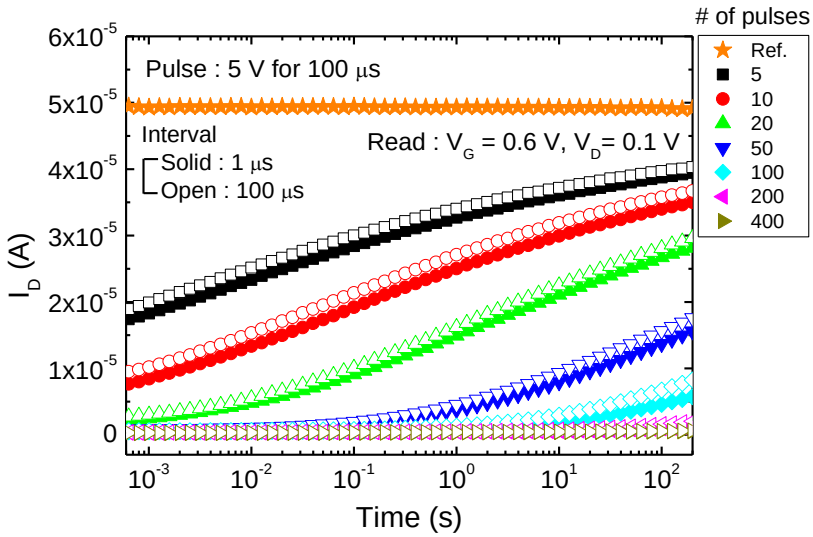
Fig. 4.10 Measurement scheme for low-stress transient characteristics

A/H/N (9/5/2.6 nm) but the pulse amplitude is 4.1 V for A/N (9/2.6 nm) with consideration for the same electric field at nitride layer (~ 4 MV/cm). Here, it is noted that the dielectric constants for Al_2O_3, HfO_2 and Si_3N_4 are ~ 8.8, ~ 17 and ~ 7, respectively. As the number of pulses increases, I_D is gradually decreased with charge loss versus time in both of two stacks as shown in Fig. 4.11 (a) and (b). However, the A/H/N stack shows that the transient curves are different depending on interval time while there is no interval dependence for the A/N stack. When the same number of pulses are applied to the gate stacks, retention time (time required to recover into the reference I_D value) of the A/H/N is relatively longer than the A/N as well. This is because some injected electrons can not only trapped in Si_3N_4 but also HfO_2 for the A/H/N stack as iterative gate pulses are applied. Here, the trapped charge in HfO_2 is expected to have longer retention characteristic due to the deep trap levels (1.4 ~ 2.7 eV) and the farther spatial distance from the silicon substrate as elucidated in chapter 3.2. The A/H/N stack was measured for monitoring the recovery characteristics after applying gate pulses with more different input conditions as shown in Fig 4.11

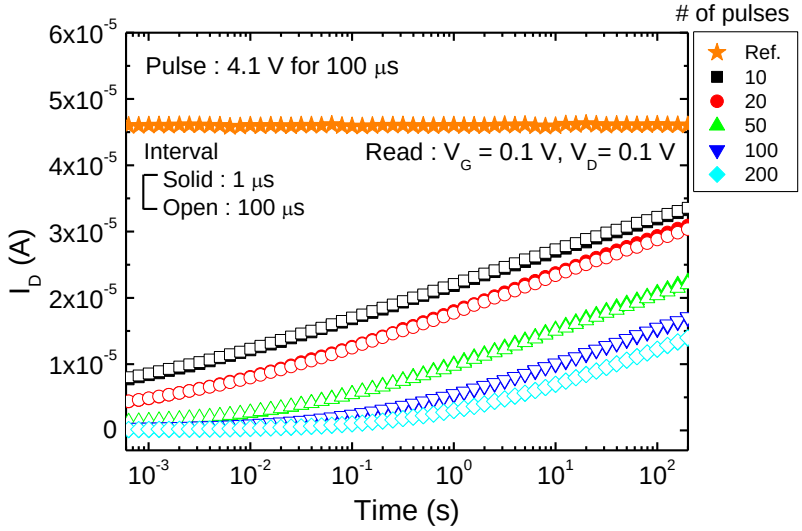
and Fig. 4.12. 4.5 V and 5 V of pulse amplitudes are applied to Fig. 4. 11 and Fig. 4.12, respectively. The pulse intervals are 1 μs, 100 μs and 10 ms. When interval time is relatively longer, more charge loss is followed during the stress operation and the recovery time to the reference state will be shorter. When the pulse width is 500 μs, the pulse interval dependence almost disappears since the long pulse duration make the position of the trapped charge relatively deeper in the gate stack as can be seen in Fig. 4.11 (c) and Fig. 4.12 (d). Consequently, it is necessary to find the proper input condition to achieve an implementation of a desired synaptic transient performance showing time interval dependence.

Lastly, retention measurements of the device at room temperature and 60 ° C were carried out to examine long-term memory characteristics for up to 10^4 s as depicted in Fig 4.13. Iterative pulses are applied with 5 V for 100 μs with a pulse interval of 1 μs. When the number of the input pulses is 200 at room temperature, the recovery rate of I_D transient curve to the reference state suddenly becomes higher from about 10^2 s. There is no remarkable decay changes for more repeated stimulation conditions even at a higher temperature of

60 °C as plotted with open symbols in Fig. 4.13. Therefore, it can be speculated that as the increase of the input pulses give rise to an enhanced long-lived retention property, which is a gradual LTP transition property originally from STP. Higher-amplitude and longer-duration pulses cause a larger change in the device conductance by trapped charge in the gate stack. The suggested structure of the gate stack (A/H/N) is a basic structure for mimicking synaptic behavior in biological system. We expect that the performance of short-term or long-term memories can be improved as a synaptic device for a desired operation conditions by band-engineering.

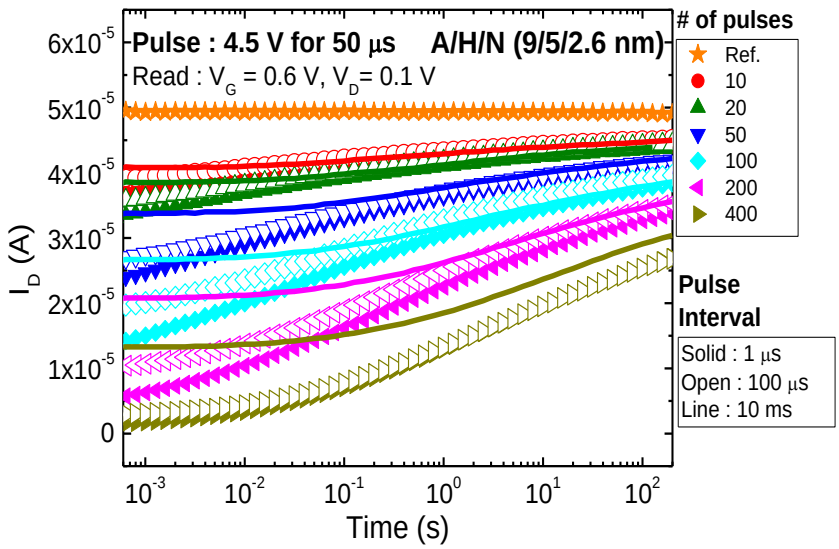


(a)

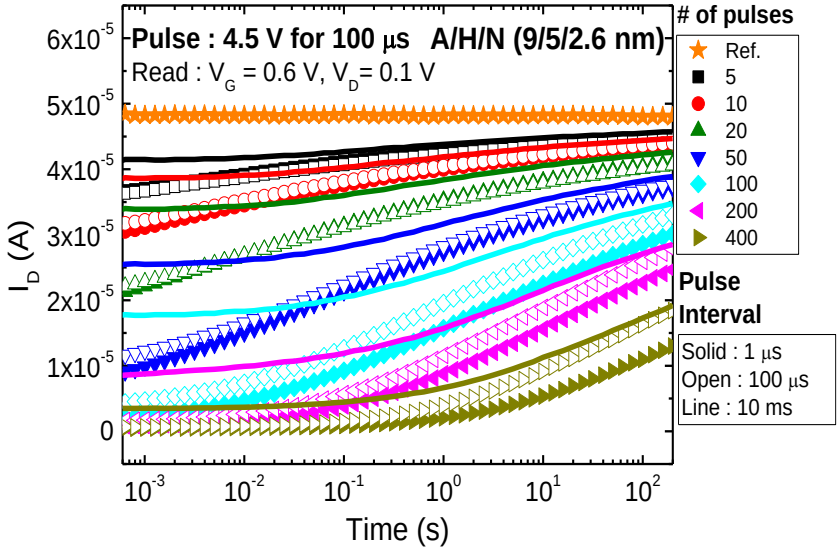


(b)

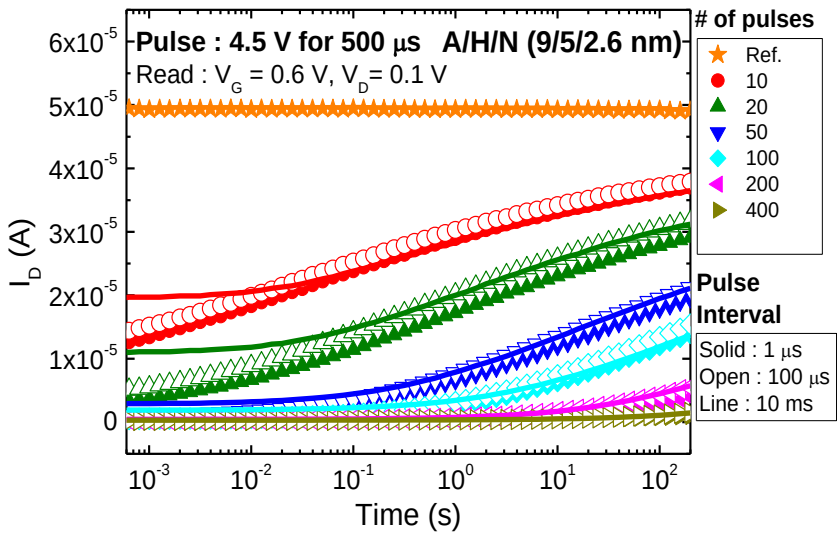
Fig. 4.11 Retention properties for (a) A/H/N and (b) A/N stack at a same electric filed depending on the number of pulses


Pulse : 4.5 V for 50 μs A/H/N (9/5/2.6 nm)
Read : V_G = 0.6 V, V_D = 0.1 V
I_D (A)
Time (s)
# of pulses
Ref.
10
20
50
100
200
400
Pulse Interval
Solid : 1 μs
Open : 100 μs
Line : 10 ms

(a)

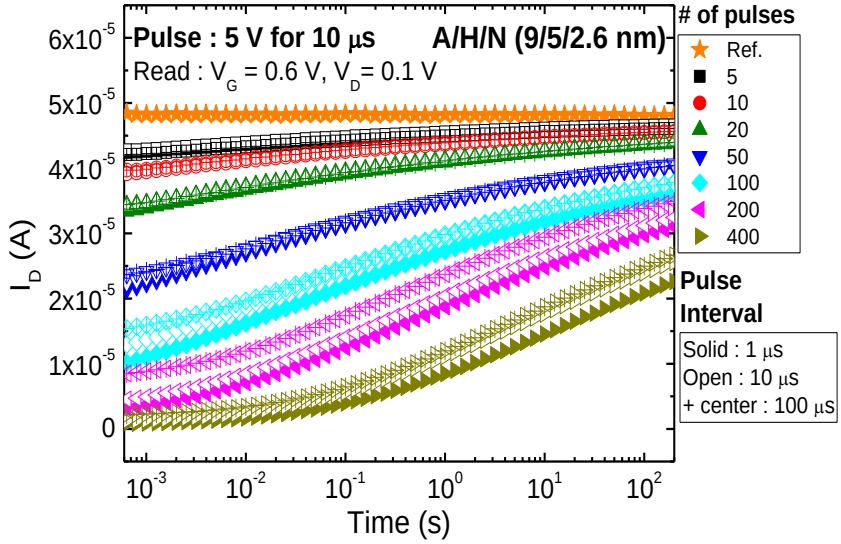

Pulse : 4.5 V for 100 μs A/H/N (9/5/2.6 nm)
Read : V_G = 0.6 V, V_D = 0.1 V
I_D (A)
Time (s)
# of pulses
Ref.
5
10
20
50
100
200
400
Pulse Interval
Solid : 1 μs
Open : 100 μs
Line : 10 ms

(b)

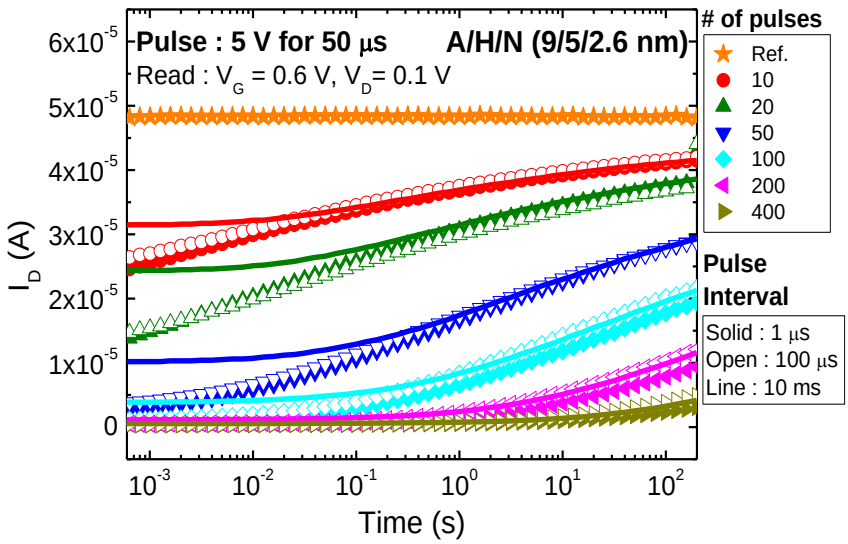


(c)

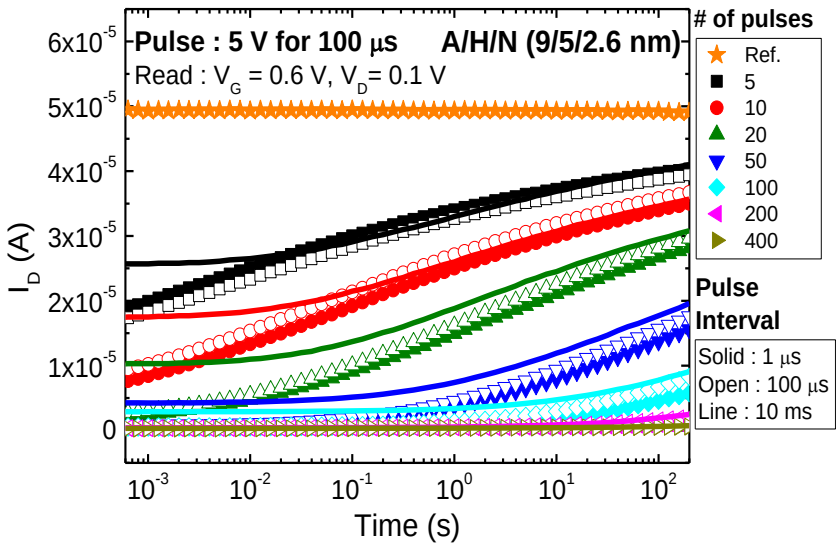
Fig. 4.11 Retention properties with different pulse conditions ((a) 4.5 V for 50 μs, (b) 4.5 V for 100 μs, (c) 4.5 V for 500 μs)



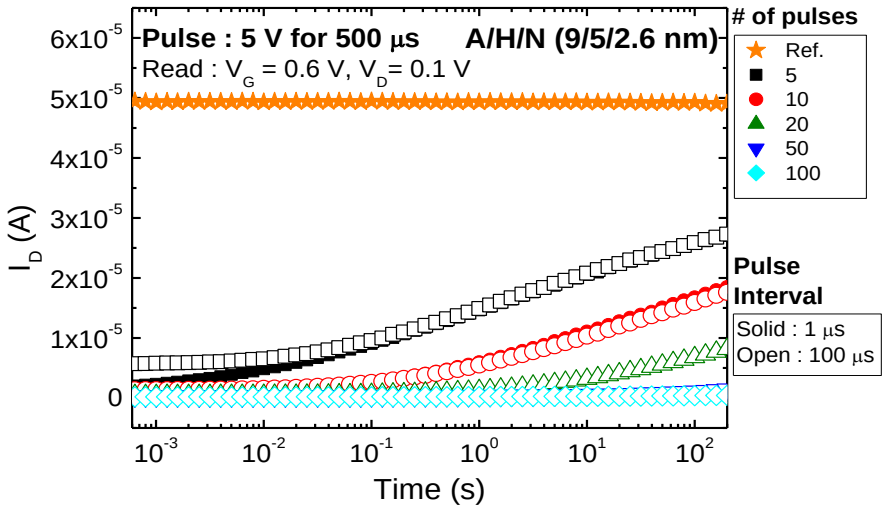
(a)


Pulse : 5 V for 50 μs
A/H/N (9/5/2.6 nm)
Read : V_G = 0.6 V, V_D = 0.1 V
I_D (A)
Time (s)
# of pulses
Ref.
10
20
50
100
200
400
Pulse Interval
Solid : 1 μs
Open : 100 μs
Line : 10 ms

(b)


Pulse : 5 V for 100 μs
A/H/N (9/5/2.6 nm)
Read : V_G = 0.6 V, V_D = 0.1 V
I_D (A)
Time (s)
# of pulses
Ref.
5
10
20
50
100
200
400
Pulse Interval
Solid : 1 μs
Open : 100 μs
Line : 10 ms

(c)



(d)

Fig. 4.12 Retention properties with different pulse conditions ((a) 5 V for 10 μs, (b) 5 V for 50 μs, (c) 5 V for 100 μs, (d) 5 V for 500 μs)

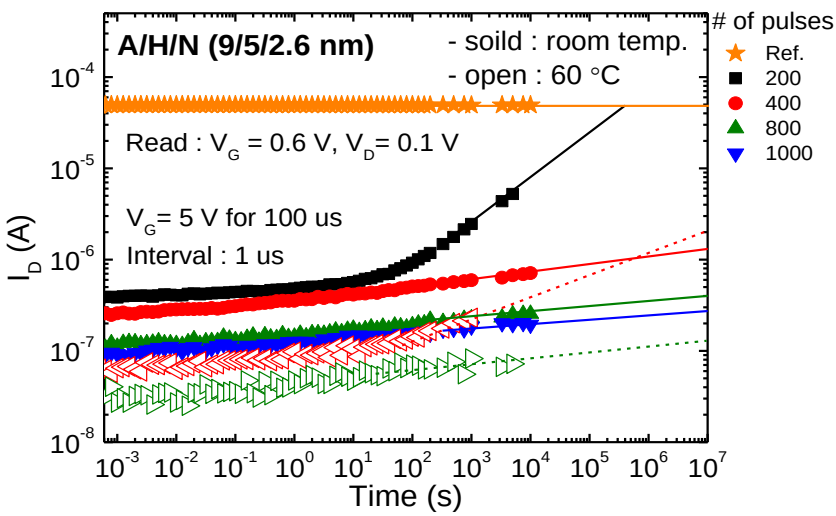


Fig. 4.13 Retention characteristics for A/H/N (9/5/2.6 nm) stack after stimulation with consecutive pulses of 5 V for 100 μs with the time interval of 100 μs at room temperature and 60 ℃.

4. 4 Spike-timing-dependent plasticity (STDP)

Synaptic plasticity is believed to have relationship with learning and memory of the biological brain [43]. In the late 1990s, a form of Hebbian learning, spike-timing-dependent plasticity (STDP), which concentrates on the temporal order of spikes, emerged as a new concept in cellular learning [44], [45]. According to an asymmetric type of STDP, Bi and Poo discovered initially in hippocampus, the synaptic weight can be modified depending on the temporal correlation of pre- and post-synaptic spikes. If a pre-synaptic spike precedes a post-synaptic spike, the synaptic weight increases while the synapse weight decreases for the reverse temporal order. The percentage of synaptic weight changes is determined by the value of timing difference between pre- and post-spikes. In other words, a smaller spike timing difference results in a larger increase or decrease of the synaptic weight. There are different types of STDP forms showing different synaptic weight modifications according to the pre- and post-spike timing and their order including the asymmetric type [46], [47].

A silicon channel conductivity of the FET device having A/H/N (9/5/2.6

nm) can be increased or decreased by consecutive potentiating or depressing pulses as shown in Fig 4. 14 where input pulses of 5 V for 100 μs are initially applied 400 times with 1 μs of time interval for a long-term memory state. We assumed an increase and decrease of I_D indicates a depression and potentiation, respectively. In Fig 4. 14, 10 consecutive potentiation pulses are applied with 2.4 V for 100 μs, followed by 10 different depression pulses, which is repeated 5 times. To observe the I_D changes, read pulses with amplitudes of 0.7 V were used for gate bias after each single pulse. Reliable and repeatable I_D change curves are observed.

Figure. 4.15 shows a measurement scheme with a synaptic spike shape for an implementation of STDP. A pair of pre- and post-synaptic spikes (V^+/V^- =+3 /-4 V) are applied to the gate and silicon substrate of the device, respectively as shown in Fig 4. 15 (a). A spike pulse shape is designed as Fig. 4. 15 (b) which is different from a biological spike form. The used spike have shorter pulse duration (100 μs) while the amplitude is much higher compared to a biological spike (+ 30 mV, - 90 mV). The potential difference between pre- and post-spikes

are different according to the spike order and timing as demonstrated in Fig. 4. 15 (c). When the time interval is long enough to have no overlapping time between pre- and post-spikes, it is negligible for the influence of the spikes to the device. Experimental asymmetric STDP data (Fig. 4.16 (b)) from the synaptic FET are similar to the data from Bi and Poo (Fig. 4.16 (a)). The STDP plot in Fig. 4. 16 (b) can be an example and the STDP forms can be controlled by modifying the input pulse scheme.

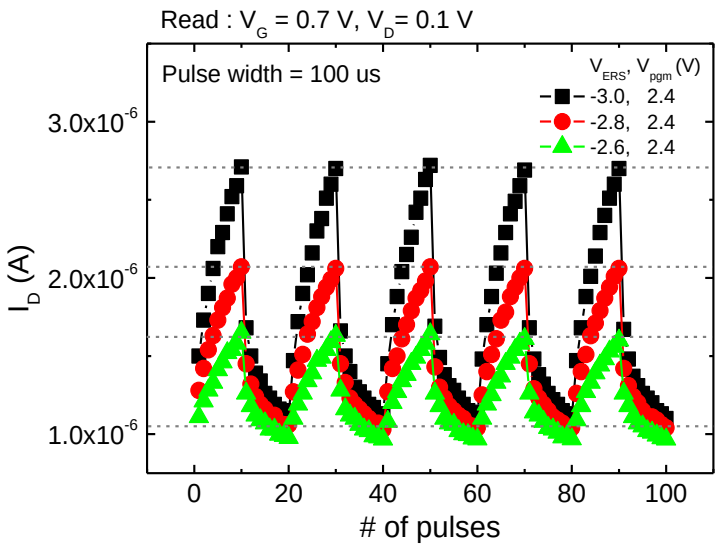


Fig. 4.14 I_D changes with consecutive application of potentiation and depression pulses depending on the applied pulse number

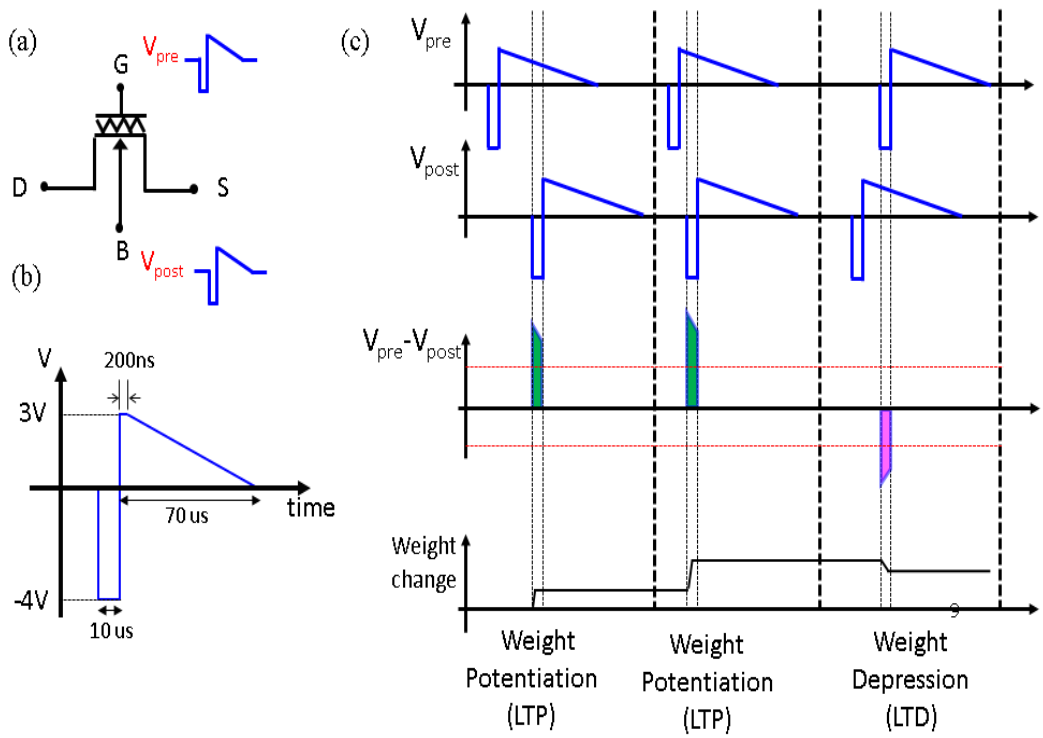
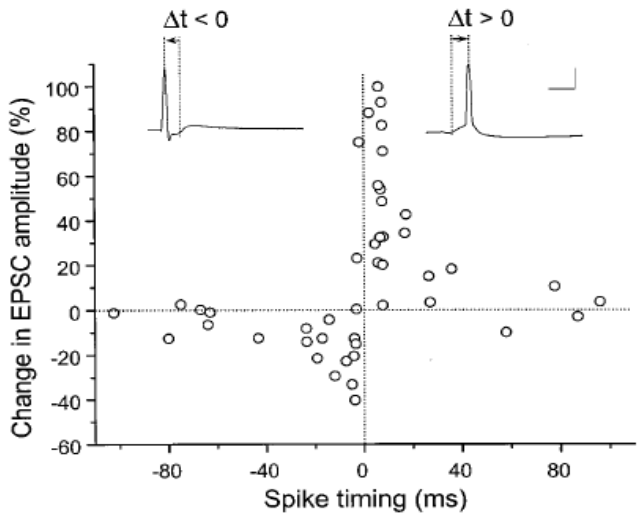
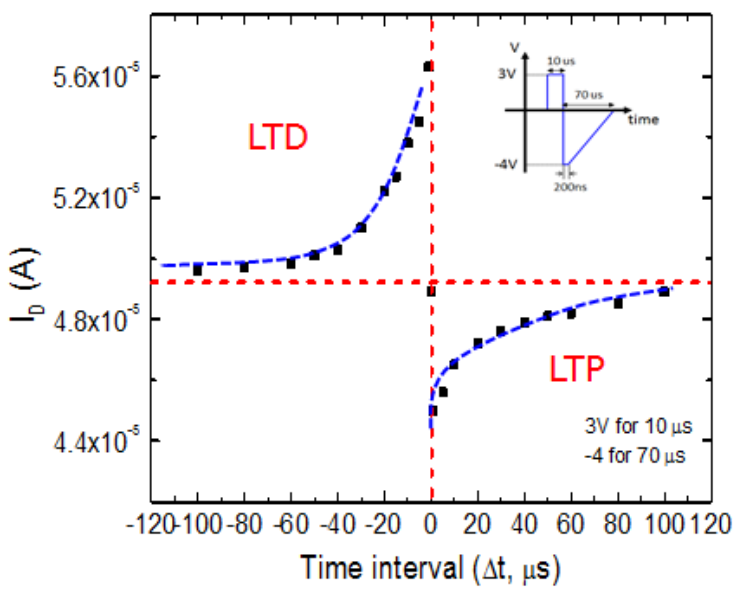


Fig. 4.15 (a) A pair of pre- and post-synaptic pulses for the synaptic device. The pre- and post-spikes are applied to the gate and substrate, respectively. (b) Input spike waveform in which negative bias region is rectangular and positive bias region is triangular. (c) Pre- and post-synaptic spikes for an implementation of STDP.



(a)



(b)

Fig. 4.15 (a) Biological STDP characteristics from Bi and Poo [44]. (c) Experimental results for STDP with our synaptic FET device

Chapter 5

Conclusion

In this thesis, $Al_2O_3/HfO_2/Si_3N_4$ gate stack were proposed and it is applied to the fabricated capacitor. STP and LTP with their conversion characteristics were explored in the proposed capacitor through *C-V* and *C-t* measurements in an efforts to imitate synaptic plasticity, for the first time. The competing effect of memory loss and memory strengthening was observed upon the application of repeated stimulations. To understand charge transport and retention mechanism in detail, we suggested the possible models with energy band diagrams. When a gate stack only have a single storage layer as O/N stack, it shows STP characteristic. The scales N/H/A stack also shows synaptic behavior with lower power dissipation.

We experimentally demonstrated behavior analogous synaptic behavior with the proposed gate stack architecture. This proposed charge controlled gate stack has great potential for use with silicon-based neuromorphic applications.

Appendix

Spatial trap distribution near silicon interface

A.1 Introduction

Conventional Charge pumping technique is originally proposed in 1969 which can determine substrate/gate dielectric interface state density (D_{it}), the energy distribution within the Si bandgap, capture cross sections for electrons and holes. By varying the charge pumping frequency, this technique also allows to characterize bulk defects close to the interface [49], and traps in nitride layers separated from the substrate by a thin SiO_2 layer [50, 51]. Recently, charge pumping was used in a similar way for characterizing HfO_2 bulk traps in SiO_2/HfO_2 stacks [52-54]. M. B. Zahid et.al further develop the applicability of the variable frequency charge pumping technique by independently controlling the pulse low and high level timings. This allows us to more clearly separate the traps in the interfacial SiO_2 from the traps in the HfO_2 and observe the creation

of new traps in both constituent layers.

Figure A.1 illustrates the connections for a device under test (DUT) with measurement system and the energy band diagrams during the charge pumping measurements. Source and Drain terminals are tied together or slightly reverse biased. The time varying gate pulse is of sufficient amplitude for the surface under the gate to be driven in into inversion and accumulation. The charge pumping current is measured at the substrate, at the source/drain tied together, or at the source and drain separately. When the gate voltage changes from positive to negative or vice versa, the surface changes between inversion and accumulation. During accumulation, some of the majority carriers provided by the body are trapped on interfaces states. During the rising edge of the gate pulse, the mobile majority carriers are collected rapidly from the accumulation layer by the body, and then the trapped majority carriers recombine with the minority carriers provided by the source and drain. Similarly, during the falling edge of the gate pulse, when the gate surface is pulsed from inversion to accumulation, the trapped minority carriers recombine with majority carriers.

In a voltage base sweep, the amplitude and period of the pulse are fixed while sweeping the pulse base voltage (Fig. A.2 (a)). At each base voltage, body current can be measured and plotted against base voltage. The interface trap density (*N*it) can be extracted as this equation:

$$N_{it} = \frac{I_{cp}}{qfA}$$

where I_{cp} is the measured charge-pumping current, q is the fundamental electronic charge, *A* is the device area, and *f* is the frequency.

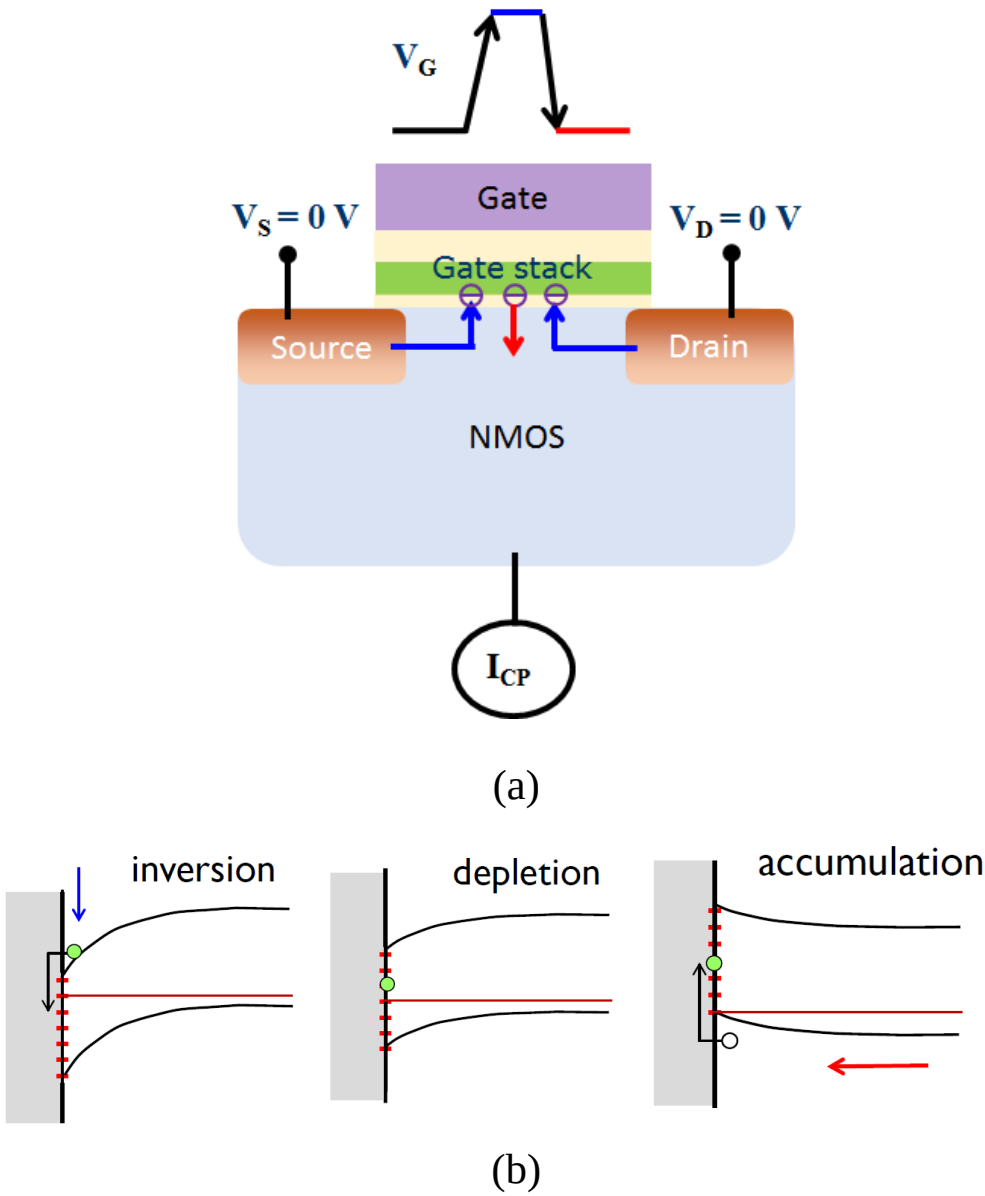


Fig. A.1 (b) Connections for a NMOS device under test (DUT) with semiconductor parameter analyzer and (b) Energy bands for charge pumping measurements

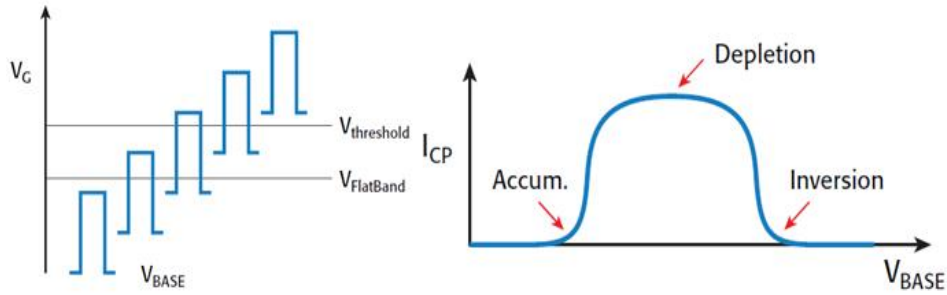
A.2 Measurement results and discussion

In conventional charge pumping theory, extracted D_{it} is interpreted as interface state density. However, border traps can also respond to the gate pulse at low frequency. In particular, when HfO_2 is separated from the substrate by very thin SiO_2 as the bottom dielectrics, traps in the HfO_2 can be sensed. In order to measure the interface states, charge pumping measurement was carried out with a constant duty cycle at a different frequencies.

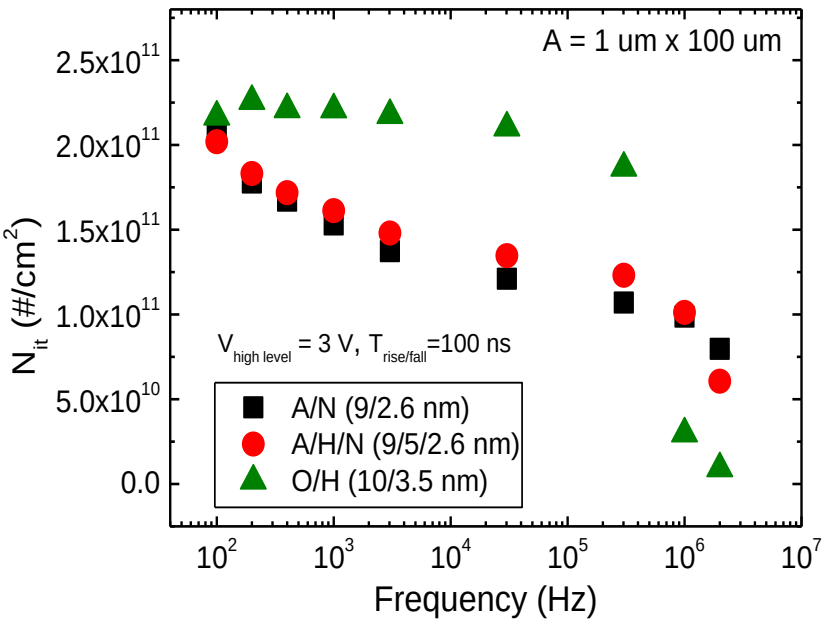
We performed the charge pumping measurements for A/H/N, A/N and O/H gate stacks to compare Si/SiN_4 and Si/HfO_2 interfaces. The pulse amplitude is 3 V and, t_{rise} and t_{fall} are 100 ns. When extracted N_{it} are compared between A/H/N and A/N stacks, the data are similar, which indicates that traps in HfO_2 do not be sensed [52]. The trap density of nitride is a bit higher in the bulk layer to the interface. On the other hand, the trap density in HfO_2/Si interface is higher than Si/SiN_4 interface at high frequency regime, which means there are more trap sites near silicon surface.

M. B. Zahid et. al proposed a Variable T_{charge}-$T_{discharge}$ Charge Pumping

(VT^2CP) where an independent control of charging and discharging time allows more clear separation of traps two different dielectrics [55]. We applied this technique for A/H/N gate stack to investigate the spatial trap distribution as shown in Fig. A. 3. A gate pulse with fixed t_{charge} and $t_{discharge}$ is applied for a base level sweeping from -2 to 5 V. Then $t_{discharge}$ is increased while t_{charge} remains unchanged and a new base level sweep is taken. The pulse amplitude is 3 V and, t_{rise} and t_{fall} are 100 ns. The base level sweeps was done with a different t_{charge} (1 μs to 5 ms) and $t_{discharge}$ varying from 5 μs to 800 μs. Two separated linear fits are observed in both Fig. A. 3 (b) and (c), which should be not originated from HfO_2/nitride interface but only nitride layer. Therefore, we could not obtain the trap spatial distribution in nitride/HfO_2 interface by VT^2CP technique. It is necessary to investigate another trap spatial analysis technique for the thick gate stacks.

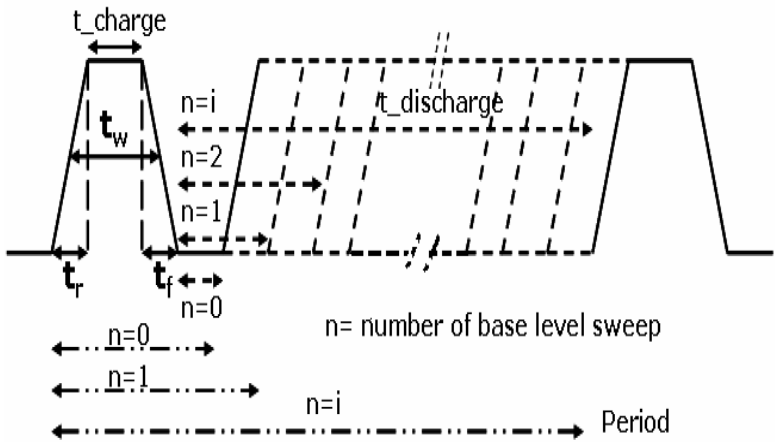


(a)

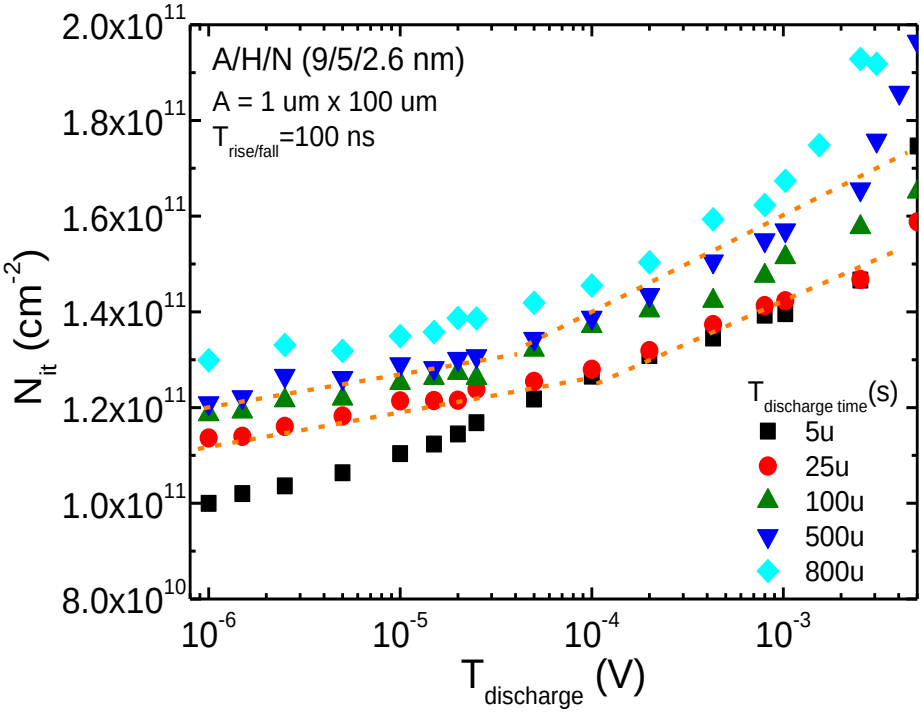


(b)

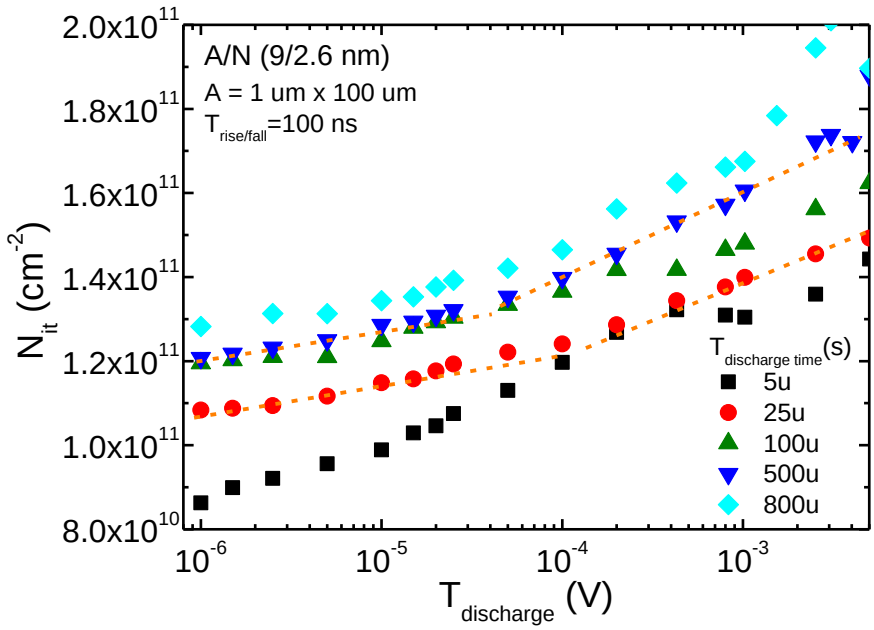
Fig. A.2 (a) Connections for a NMOS device under test (DUT) with semiconductor parameter analyzer and (b) Energy bands for charge pumping measurements


t_charge
t_discharge
t_w
n=i
n=2
n=1
n=0
t_r
t_f
n= number of base level sweep
n=0
n=1
n=i
Period

(a)


A/H/N (9/5/2.6 nm)
A = 1 um x 100 um
$T_{rise/fall}$=100 ns
$T_{discharge\ time}$(s)
5u
25u
100u
500u
800u
N_{it} (cm^{-2})
$T_{discharge}$ (V)
$2.0x10^{11}$
$1.8x10^{11}$
$1.6x10^{11}$
$1.4x10^{11}$
$1.2x10^{11}$
$1.0x10^{11}$
$8.0x10^{10}$
10^{-6}
10^{-5}
10^{-4}
10^{-3}

(b)



(c)

Fig. A.3 (a) VT^2CP measurement scheme and the extracted *N*it for (b) A/H/N and

(c) A/N stacks

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2. S. Yu, Y. Wu, R. Jeyasingh, D. Kuzum, and H.-S. P. Wong "An electronic synapse device based on metal oxide resistive switching memory for neuromorphic computation", *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2729 -2737, 2011

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List of Publications

International Journal

[1] **Myoung-Sun Lee,** Sung-Min Joe, Jang-Gn Yun, Hyung-Cheol Shin, Byung-Gook Park, Sang-Sik Park, and Jong-Ho Lee, "A Subthreshold Slope and Low-frequency Noise Characteristics in Charge Trap Flash Memories with Gate-All-Around and Planar Structure," *Journal of Semiconductor Technology and Science*, vol.12, no.3, Sep 2012.

[2] **Myoung-Sun Lee**, Byung-Gook Park, Il Hwan Cho and Jong-Ho Lee, "Characteristics of Elliptical Gate-All-Around SONOS Nanowire With Effective Circular Radius," *IEEE Eletron Device Lett*, vol. 33, no. 11, Nov 2012.

[3] **Myoung-Sun Lee**, Ju-Wan Lee, Change-Hee Kim, Byung-Gook Park and Jong-Ho Lee "Implementation of Short-Term Plasticity and Long-Term

Potentiation in a Synapse Using Si-Based Type of Charge-Trap Memory," *IEEE Trans. Electron Devices*, vol. 62, no. 2, 2015..

International Conference

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초 록

에너지 효율적인 고집적 전자 시냅스의 개발은 생물학적 신경망에서의 적응 학습 및 기억을 모방하기 위한 중요한 부분이다. 최근 2 단자 멤리스터, 즉 여러 종류의 원자 스위치, 상 변화 메모리 (PCM), 및 저항 스위칭 소자 등은 생물학적 시냅스의 기능을 모방하기 위해 제안되었다. 그러나, 이러한 두 단자 소자는 시냅스 신경 네트워크를 모방하는 셀 어레이에서 셀 당 하나의 선택 소자를 필요로 한다. 또한, 이들은 신뢰성, 재현성 및 공정 복잡성 측면에서 개선 할 필요가 있다.

본 논문에서는 생물학적 시냅스 메모리 기능의 모방하기 위해 Al_2O_3 /HfO_2/Si_3N_4 (A/H/N) 게이트 스택, 즉 새로운 실리콘 기반의 전하 트랩 메모리 장치를 제안한다. 제안된 게이트 스택을 갖는 캐패시터을 간단한 공정을 통해 제작하고, 단기 가소성 (STP) 및 장기 강화 (LTP) 성질 및 그들간의 전이되는 전기적 특성을 통해 생물학적 시냅스의 동작과 유사함을 증명하였다.

이 터널 절연막이 없는 얇은 질화막 층에서는 수 분 이내에서 빠른 전하 손실을 나타낸다. 또한, 반복하여 입력되는 동일한 펄스가 인가될 경우, 펄스 간격 의존성이 없다. 그러나, HfO_2 층을 Si_3N_4 층 위에 삽입할 경우 펄스간의 시간 차이에 따른 의존성이 존재한다. 이는 장기 메모리로 전환되는 것을 유도하는 HfO_2와 층의 깊은 트랩 레벨 (E_T)에 기인한다. 한편, 상기 게이트 스택의 I_G-V_G 측정을 하고, 전하의 전송 및 트래핑 특성을 이해하기 위해 이를 분석하고, 설명이 가능한 모델을 제시하였다. 마지막으로 전시냅스와 후시냅스에 인가되는 펄스 형

태를 제시하고 측정을 통해 STDP 특성을 확인하였다.

이 제안 된 구조는 넓은 영역에 걸쳐 높은 균일성, 우수한 신뢰성, CMOS 호환되는 재료를 사용하고, CMOS 회로와 융합하여 적용할 수 있는 장점을 갖는다.

주요어 : 전하 트랩 메모리, 시냅스, 단기 소성 (STP), 장기 증강 (LTP), Al_2O_3/ HfO_2 /Si_3N_4 (A/H /N), 게이트 스택

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