Ph.D. DISSERTATION

Vertical Tunnel Field-Effect Transistors with Tunnel-Direction Perpendicular to the Channel for Low Power Operation

저전력 동작을 위하여 채널에 직각인 터널방향과 수직형 구조를 가지는 터널 전계효과 트랜지스터

BY

JANG HYUN KIM

AUGUST 2016

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지도교수 박병국

이 논문을 공학박사 학위논문으로 제출함

2016 년 08 월

서울대학교 대학원

전기 컴퓨터 공학부

김장현

김장현의 공학박사 학위논문을 인준함

2016 년 08 월

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Abstract

In this work, Tunnel Field-Effect Transistors (TFETs) with a novel structure will be proposed as a substituting devices which can implement steeper switching than the conventional MOSFETs do in low power operation. It is experimentally demonstrated that applying a vertical structure with a perpendicular tunnel to the channel can achieve an operation of high electrical performance and it can be integrated in a bulk Si substrate.

First of all, Si and SiGe TFETs with a planar structure are fabricated and measured to extract model parameters. From the measured results, the parameters of band-to-band tunnel (BTBT) model, which can be used to simulate TFETs accurate are calibrated. In this regard, Synopsys Sentaurus Device will be used for this purpose.

Then, based on the simulation of planar TFETs, the proposed devices will be presented as the vertical TFETs with the perpendicular tunnel junction based on the bulk Si substrate. The perpendicular tunnel junction and the large tunnel area are employed on the source side to achieve a steep subthreshold swing (SS) and high ON-current (I_{ON}), which can lead to TFET's outstanding performance. Moreover, the I_{ON} can be increased easily by adjusting a height of overlap region between a source and a gate. Although, the TFETs show good electrical performance, there is a hump phenomenon in transfer curve.

In order to suppress the hump phenomenon in the transfer curves, the hump behavior in the proposed device should be investigated. After investigating it, the hump behavior is found to be originated from the two different tunnel regions. Moreover their threshold voltages originated from different tunnel show different values. In order to improve the electrical performance, a capping layer which can be made by gradual doping is inserted on the source. Then, the hump behavior can be expected to decrease.

Finally, the proposed TFETs will be fabricated on the bulk Si substrate. A thin intrinsic Si is epitaxially grown on the source region which forms the perpendicular tunnel junction to the channel, resulting in abrupt band bending. The fabricated the proposed TFETs show 17 mV/dec minimum subthreshold swing (SS) and 10^4 ON/OFF current ratio (I_{ON}/I_{OFF}) for sub-0.7 V gate overdrive. In addition, SS is maintained less than 60 mV/dec while a drain current increases from complete OFF-state (10^{-13}) to more than two orders of magnitude (10^{-11}).

In conclusion, the proposed device are fabricated successfully. From this study, it is demonstrated that the proposed TFETs will be one of the most promising candidate for a next-generation low-power device.

Keywords: band-to-band tunnel, tunnel field-effect transistor, vertical structure, TFET, low power device, perpendicular tunnel, subthreshold swing, Si substrate

Student Number: 2009-30956

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Chapter 1

Introduction

1.1 Power issues on CMOS technologies

During the last few decades, semiconductor devices and systems have been utilized and exploded. The miniaturization of semiconductor brings more features on chips and functionality at the lower cost. However a semiconductor industry is facing a serious obstacle. Although scale-down of the semiconductor has allowed a dramatic improvement, a power dissipation per unit area has been also equally increased [1]. In detail, a static power and a dynamic power have been considered as two principal sources of the power dissipation (Eq. 1.1). One of power dissipation is the static power. Whenever transistors are turned on or off, the static power is sustained from current that leaks through the transistors. The other is the dynamic power, which occurs from the repeated capacitance charge and discharge (Fig. 1.1). In the past, the dynamic power had been fo-

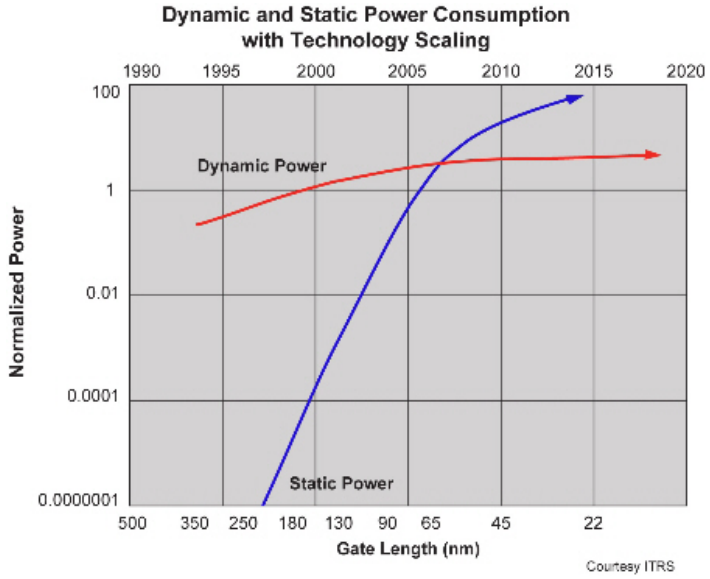


Figure 1.1 A power dissipation with the static power and the dynamic power (Courtesy: ITRS)

cused on a major source of the power consumption, and it has been controlled by scale-down of transistors and supply voltage. The dynamic power is proportional to the square of the supply voltage. Recently, however, the scale-downed transistors have aggravated the leakage current, so the static power begins to dominate the power consumption. The following equation defines overall power consumption as the sum of the dynamic and static power:

$$P = ACV^2 f + VI_{leak} \tag{1.1}$$

where A is the fraction of gates actively switching and C is the total capacitance

load. The first term is the dynamic power lost from charging and discharging the load capacitors. The second term means the static power lost due to leakage current. In the Eq. 1.2, the leakage current (I_{leak}) shows dependency on threshold voltage and supply voltage:

$$I_{leak} = KWe^{\frac{-V_T}{nV_0}}(1 - e\frac{-V_{DD}}{V_0}) \tag{1.2}$$

K and n are experimentally derived, W is the gate width, and V_0 in the exponents is the thermal voltage. At room temperature, V_0 is about 25 mV. Eq. 1.2 suggests two methods to reduce I_{leak}. The first solution is to shrink the supply voltage (V_{DD}) or to turn off the device. Second, increasing the threshold voltage will be another solution for the negative term in the Eq. 1.2.

In the most recent decade, however, the gate overdrive voltage (V_{DD}-V_T) has not been reduced proportionately with the transistor size (Fig. 1.2). Therefore, as the number and density of transistors on a chip have increased, the peak power density has also increased dramatically.

1.2 Tunnel Field Effect Transistors

In the previous section, the power dissipation has been mentioned. Many research groups have studied developing novel devices which can be operated in very low power [4]-[5]. Among these devices, the TFETs have been studied extensively due to outstanding subthreshold characteristics and capability for the

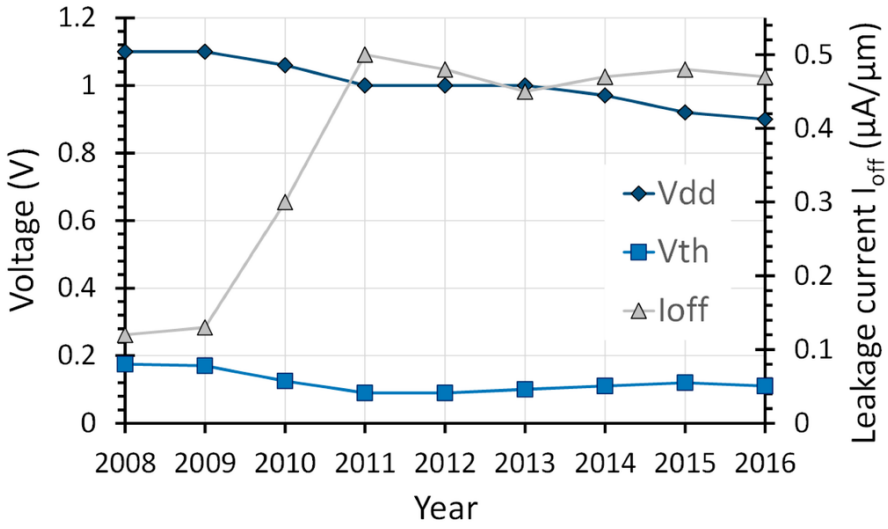


Figure 1.2 Trends for MOSFETs threshold voltage (V_T), operating voltage (V_{DD}), and corresponding transistor OFF-state leakage (I_{OFF}) [2].

low-power operation [6]-[10]. In the case of MOSFETs, which are conventionally used in almost every circuit (Fig 1.3(a)), there exists theoretical limit of 60 mV/dec subthreshold swing (SS) at room temperature (RT) because their carrier injection is based on thermionic emission (Eq.1.3) (Fig. 1.3(b)) [11]-[12].

$$SS = (\frac{dI_D}{dlogV_G})^{-1} = (1 + \frac{C_{DEP}}{C_{OX}})(\frac{kT}{q}ln10) \tag{1.3}$$

Considering operation of the TFETs which has opposite doping types with a source and a drain (Fig.1.3(b)), it has no theoretical limit by the thermionic carrier injection. Fig. 1.3(d) shows a energy band diagram to illustrate a tunnel process. When the TFETs are applied with V_G, electrons in the source transfer

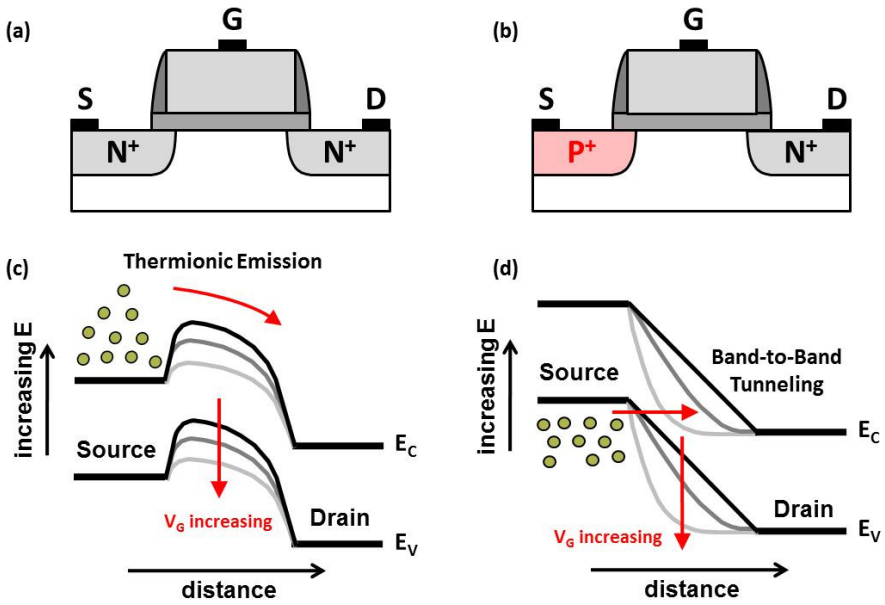


Figure 1.3 Schematic cross-sectional view of (a) MOSFETs and (b) TFETs. (c) The operation of a MOSFETs are based on the thermionic emission. (d) The operation of a TFETs are based on BTBT [3].

to the channel due to band banding. The tunnel process has been proposed as a current conduction mechanism. This is because the TFETs have weak dependence on the Boltzmann distribution and the BTBT dominates the carrier injection that can be switched more abruptly than the thermionic injection [13]-[14]. Thus, a SS can be scaled down to sub-60 mV/dec at RT. The transistors using this mechanism is ideal in that abrupt switching behavior which, in principle, allows V_{DD}-V_T to be scaled down aggressively while maintaining high I_{ON} (Fig. 1.4).

1.3 Issue for TFETs

The TFETs have been studied extensively due to remarkable low SS and capability for the low-power operation. However, the experimental demonstrations of TFETs have considerable discrepancy compared with the theoretical studies to satisfy the required performance. An issue for the fabricated TFETs is on their poor electrical performances; low ON-current (I_{ON}) and large SS, which are mainly attributed to the poor BTBT rate. In order to enhance the BTBT rate, the TFETs with double gate (DG) or gate-all-around structure are considered as a promising candidate due to the high controllability of gate on channel. And the abrupt junction between source and channel should be made. Then, the dopant profile has better abrupt junction. Moreover, it needs to employ hetero-junction technology such as silicon-germanium (SiGe), germanium (Ge), germanium-tin (GeSn), and III-V compound materials [15]-[16].

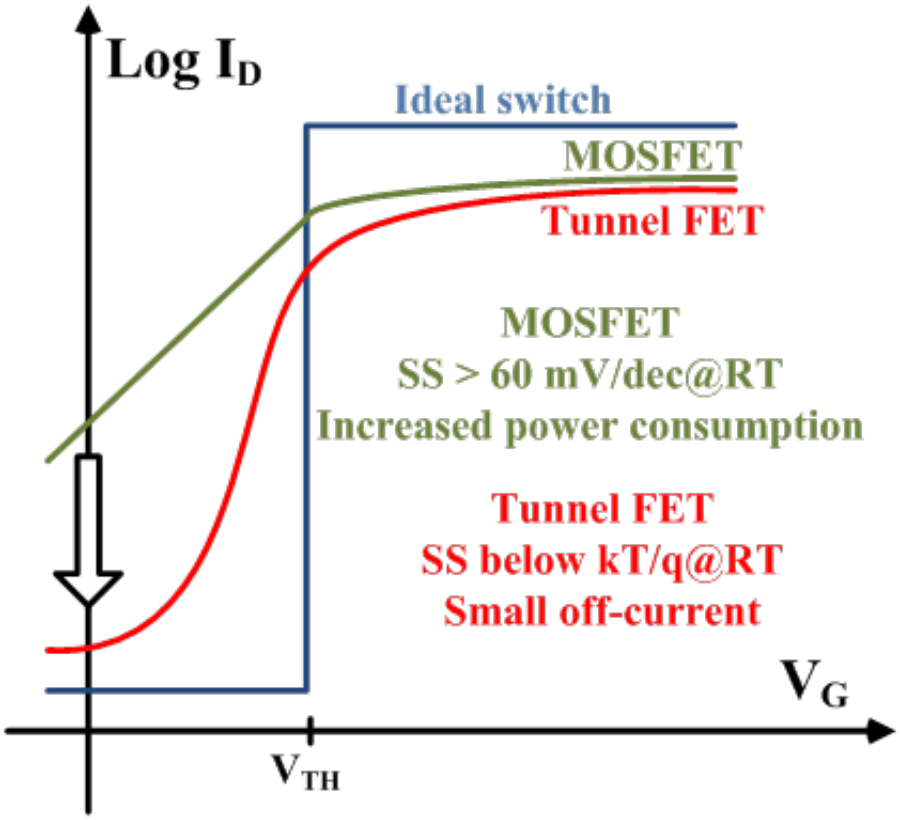


Figure 1.4 The switching properties of MOSFETs and TFETs.

The other issue is that the TFETs are the devices with a floating body. Since the source and drain in the TFETs have opposite doping types to make a p-i-n junction, the TFETs should be fabricated on a Silicon on insulator (SOI) substrate which is totally incompatible to CMOS process. Those devices, however, inevitably face self-heating effect and high fabrication cost. Moreover, in order to co-integrate with the MOSFETs with a bulk substrate, the TFETs should be fabricated without the SOI wafer.

1.4 Propose of the Target Device

In the previous section, the low power operation has been emphasized. In the MOSFET devices which have been utilized as industrial standard devices, the SS had been fundamentally limited to 60 mV/dec due to carrier injection that obey the Boltzmann statistics. As a result, a novel switch with entirely different carrier injection mechanism needs to be investigated. In the previous section, the several disadvantages of the TFETs were addressed. In many papers, the ON-current for the TFETs has been demonstrated to be quite below ITRS requirements [2]. Several studies showed dramatically improved I_{ON}/I_{OFF} ratio and highly boosted ON-current utilizing novel structure for gate controllability and material for band-gap engineering. However, as the ITRS Roadmap, the ON-current and OFF-current are suggested with 0.6 mA and 10 pA in LSTP(Low Standby Power) category. Considering characteristics of TFETs, the proposed TFETs are aimed to achieve performances in terms of SS and I_{ON}/I_{OFF} ratio

Table 1.1 ITRS specs referred to year 2020 for multi-gate transistors.

Device	Low Standby Power	Low Operation Power	High Power
V_{DD} [V]	0.67	0.53	0.68
I_{ON} [nA/μm]	0.01	5	100
I_{OFF} [mA/μm]	0.6	0.78	1.96

(sub 60 mV/dec SS and 10^4 I_{OFF}/I_{OFF} for sub-0.7 V gate overdrive) (Table 1.1). In order to meet the requirement of the ITRS, the ON-current of the TFETs should be boosted. In order to satisfy the current requirement, several technologies have been suggested in this paper.

Firstly, the TFETs are adapted to a high-κ gate dielectric. Then, the ON-current will be enhanced due to the high density of gate electric field. Moreover, the most important advantage TFETs has is the TFETs have low OFF-current. Therefore, employing the high-κ dielectric which contribute to boost the ON-current is an essential technology for the TFETs.

Secondly, as many papers have reported, the ON-current in the TFETs is determined with a tunnel width between source and channel [10]. A design for BTBT perpendicular to the channel direction (vertical BTBT) has two effects on the TFETs. One of the effects is the channel thickness limits to tunnel width. It is expected to enhance ON-current by adopting the thin tunnel width formed by an epitaxy. The other effect is that a tunnel junction area is increased by adjusting the gate and source overlaps.

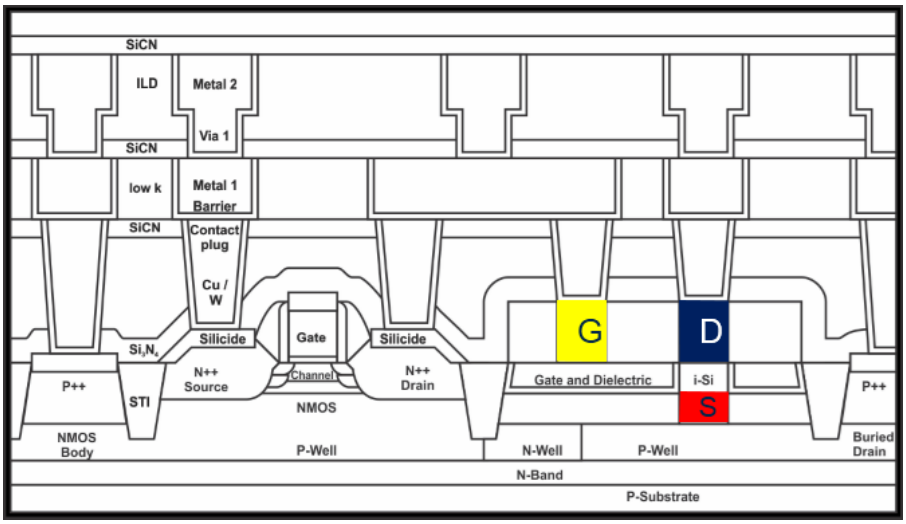


Figure 1.5 Cross sectional view of the MOSFETs and TFETs. Considering co-integration within bulk substrate, the TFETs with vertical structure are highly efficient.

Finally, a vertical structure is applied. The biggest merit of the vertical structure is that the channel can be isolated without silicon-on-insulator (SOI) substrate. Therefore, by using the vertical structure, the TFETs and MOSFETs can be integrated in the same bulk substrate. (Fig. 1.5).

1.5 Thesis outline

This dissertation is to propose and implement a novel TFETs. Especially, it is important to present highly improved electrical performances including low SS and high I_{ON}. All of the performance and process have been predicted by Technology Computer-Aided Design (TCAD) simulation with reliable model

parameters. Then the proposed TFETs have been verified with measured results.

In Chapter 2, planar Si and SiGe TFETs are fabricated as a reference device. By using these device, basic characteristics of the TFETs are confirmed. Then, electrical characteristics are analyzed and calibrated with the BTBT model. The model parameter of BTBT based on Kane's formulation is fitted with measured data. The BTBT model parameters used by the device simulation in this dissertation (Sentaurus Device) are utilized to design novel devices and then used for a optimization study.

Chapter 3 presents novel TFETs design. The proposed TFETs have feature for vertical structure with BTBT perpendicular to the channel. The perpendicular BTBT is employed to achieve low SS and enhance the tunnel current. Additionally, the vertical structure TFETs have advantages for the integration with high density. Then, the electrical performance and side effect are confirmed before the proposed TFETs are fabricated.

Chapter 4 examines the proposed devices. A total process of the fabrication is explained with details. Then, electrical performance is measured and compared with that of other groups. Finally, the proposed TFETs are analyzed and discussed to increase electrical performance.

Chapter 5 has conclusions of this paper and suggestions for future works to enhance performance.

Chapter 2

Planar Si & SiGe TFET

In this chapter, Si and SiGe TFETs with planar structure are fabricated and measured to extract model parameters. Although TCAD simulation tool reflects real physics and has accurate material characteristics which are well-estimated, the TFETs, simulated with the BTBT model, needs to be calibrated. After the model calibration, from the extracted model parameter, performance of the proposed device will be estimated and predicted.

2.1 Device fabrication

In order to prepare the planar TFETs as a reference, the TFETs had been fabricated on SOI wafer with CMOS compatibility. Fig. 2.1 illustrates a cross-sectional view of the fabricated TFETs and key processes. First, an active region was defined on 100 nm thickness. Then, gate dielectric was formed by dry

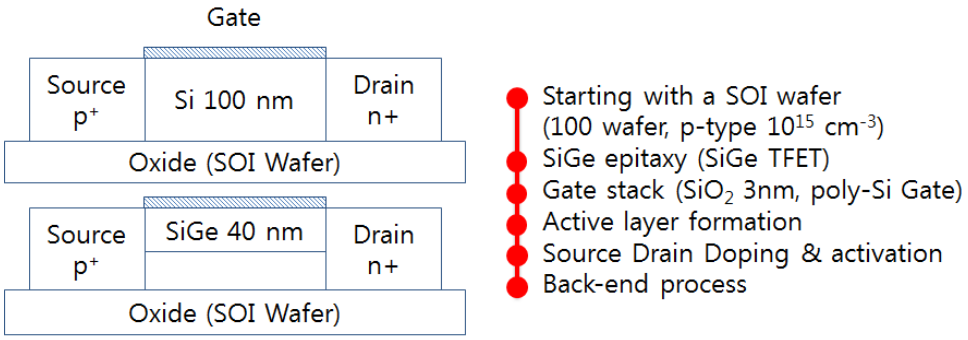


Figure 2.1 Schematic diagram and process flow for the Si and SiGe TFETs.

oxidation. The dry oxidation of 800 °C was performed during 30 sec. Then, a gate electrode was deposited with a poly-Si. The gate electrode was defined by photo-lithography and dry etch. Note that all of the pattens in this fabrication process were defined by i-line photo-lithography where the limit of the pattern size was 0.25 μm. A source and a drain regions were doped with BF_2^+ (8 x 10^{14} cm^{-3}, 10 keV, 7° tilt) and arsenic (8 x $10^{14} cm^{-3}$, 10 keV, 7° tilt), respectively. In order to activate the dopant, rapid thermal annealing (RTA) process of 900 °C was performed during 5 sec. Finally, inter-layer dielectric (ILD) was formed with tetra-ethyl-ortho-silicate (TEOS) oxide by PECVD process and metal layers (Ti/TiN/Al/TiN stacks) were deposited by physical vapor deposition (PVD) process to make a contact. Then, current and capacitance were measured by using the HP 4156 C semiconductor parameter analyzer and HP 4284 A precision LCR meter, respectively. The detailed process and recipe were described in Appendix section 2.5.

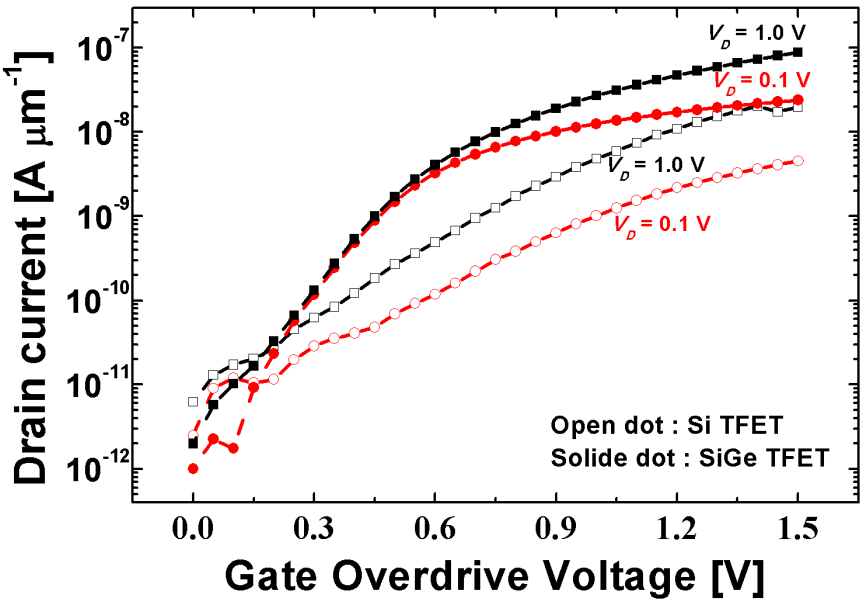


Figure 2.2 Measured I_D–V_G characteristics of planar-TFETs device with Si and SiGe substrate. The devices with SiGe TFETs show better current drivability than Si TFETs.

2.2 Measured Results

Fig. 2.2 shows the transfer characteristics of the fabricated Si TFETs and SiGe TFETs at 0.1 and 1.0 V drain voltages (V_D). Measured TFETs have channel length and width of 400 nm and 400 nm respectively. The performance can be further improved by band-gap engineered TFETs with SiGe. In the Si and SiGe TFETs, the devices exhibit average slope of 415 and 165 mV/dec over one order of magnitude of I_D at $V_D = 0.1$ V respectively. The I_{ON}/I_{OFF} ratio reaches 10^4 at $V_D = 0.1$ V and $V_G = 1.0$ V. Due to the small energy band of SiGe TFETs,

the subthreshold swing (SS) and I_{ON} are much better than that of Si TFETs. More specifically, the I_{ON} is about 10 times higher than that of Si TFETs. However, the SS is still above 60 mV/dec known as the limit of MOSFETs. The reason of degraded performance is the large tunnel resistance between source and channel. Note that, for the device using tunnel mechanism, broad doping gradient degrades gate modulation of the band-bending. Hence, to increase the tunnel current, the tunnel resistance should be reduced. Before proposing novel device, the dopant profile from the source to the channel should be identified to compare performances exactly as a reference. In order to confirm the source dopant profile, a secondary ion mass spectrometry (SIMS) is performed at the test sample which is fabricated with the same implantation and RTA processes. Fig 2.3. shows SIMS profile of boron and the dopant profile has 20 nm/dec slope.

Fig. 2.4 shows the output characteristics of Si and SiGe TFETs. The SiGe TFETs have larger current drivability than that of Si TFETs. Drive current of n-type SiGe TFETs is increased more 10 times more than that of Si TFET devices. Interestingly, the measured results show that a super-linear onset is definitely shown in the Si TFETs. When a large V_G and a very small V_D are applied, the phenomena is observed whereas the super-linear onset cannot be observed in any other bias condition. In the appendix chapter, the super-linear onset is investigated more detailedly.

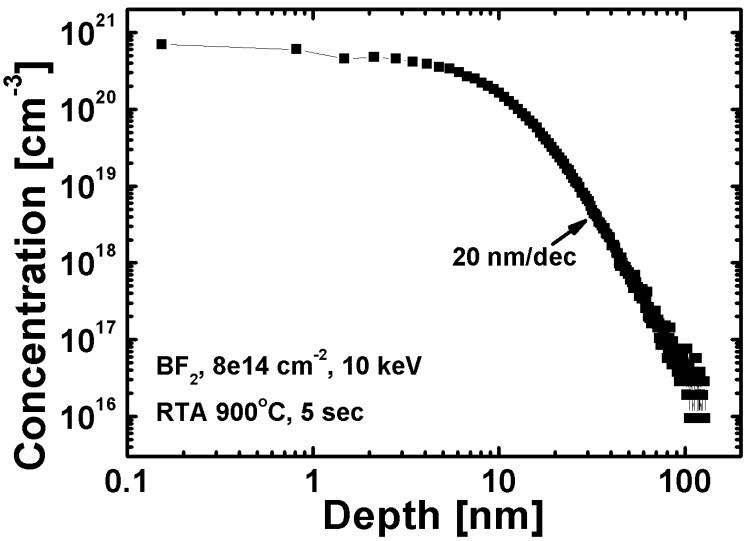


Figure 2.3 Boron concentration profile from surface to bulk direction using SIMS.

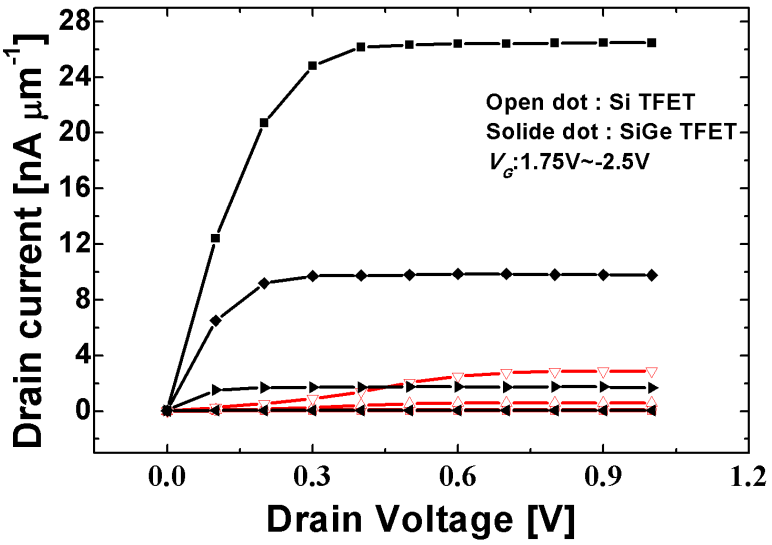


Figure 2.4 Measured output characteristics of n-type Si and SiGe TFETs.

2.3 BTBT model calibrations

In the previous section, the TFETs with planar structure were fabricated as a reference device for extracting tunnel parameters. In order to study and confirm the proposed device performance, the planar TFETs were used for calibrating band-to-band tunnel (BTBT) model. This calibration is validated as the reference for all the devices evaluated in the following chapters. Note that, gate leakage and contact resistance are not considered. Additionally the used models are followed: Fermi statistics, drift-diffusion carrier transport, band-gap narrowing and Shockley-Read-Hall (SRH) recombination models. The calibrated BTBT generation rates G per unit volume in this model are defined as

$$G = A(\frac{F}{F_0})^P exp(-\frac{B}{F}) \tag{2.1}$$

where F_0 = 1 V/m and P = 2.5. F is electric field. A is prefactor and B is exponential factor. The parameters of A and B are based on the Kane's model. For current fitting, simulation is performed based on experimental results of the fabricated TFETs. Fig. 2.5 shows the simulation results and measured results at V_D of 1.0 V with Si and SiGe TFETs. The simulation results for these parameters clearly show an excellent match with the experimental results (Table 2.1).

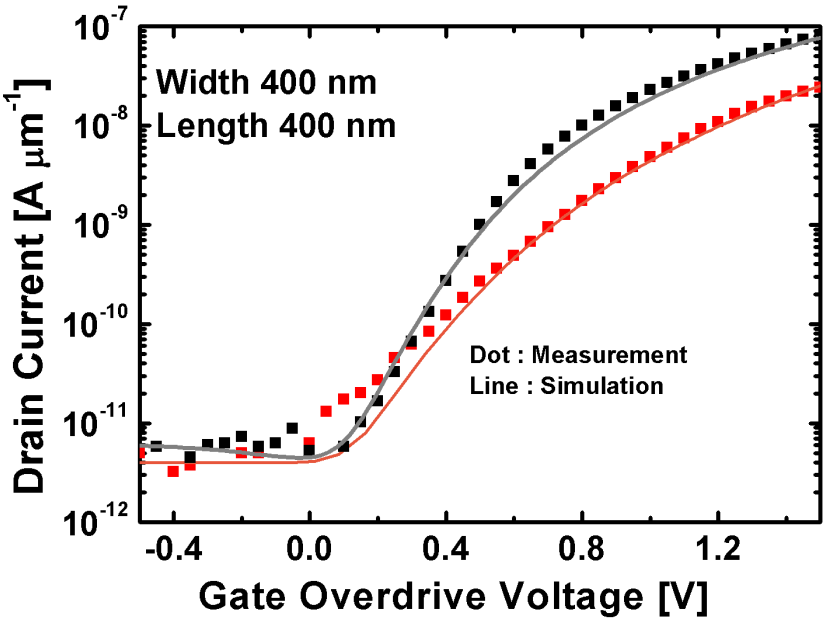


Figure 2.5 Parameter calibration curves with simulation and measurement results of TFETs.

Table 2.1 Simulated device parameters for the BTBT.

parameter	Si	SiGe	Unit
A	4 x 10^{14}	3 x 10^{16}	$cm^{-1}s^{-1}$
B	9 x 10^{6}	7 x 10^{5}	V/cm

2.4 Summary

In this chapter, the planar SiGe TFETs are fabricated and analyzed before implementing proposed TFETs. Based on the fabricated planar TFETs, the performance of the device has been evaluated and compared. Compared with Si TFETs, the SiGe TFETs show improved performance due to the small band-gap. As a reference device, the Si and SiGe TFETs are applied and calibrated to the tunnel models with a device simulation.

2.5 Appendix: Process Flow

Recipe

1. Wet station

Process name	Temp	Chemical	Time	QDR	Equipment
SC1 B Bath	80℃	NH4OH:H2O2:D.I=1:1:5	600s	360s	Wet station
SC2 A Bath	80℃	HCl : H2O2 : D.I=1:1:5	600s	360s	
HF C Bath	Room Temp	HF : DI = 1 : 100	30s	360s	
SPM	120℃	H2SO4 : H2O2 = 4 : 1	600s	360s	
PR Strip	120℃	H2SO4 : H2O2 = 4 : 1	600s	360s	

2. Photolithgraphy

Bottom material	PR	Coating		Exposure	Equipment
		RPM / sec	Rcp. / Coat No	msec / focus	
Si, SiNx, SiO2	SS03A9	4500 / 35	17 / 80(w/o EBR)	320 / -1.5	Nikon i-liner
TiN	SS03A9	4000 / 35	17 / 80(w/o EBR)	320 / -1.5	

3. Epitaxy

Process name	Temp	Gas	Epi rate	ETC	Equipment
SiGe	600	pre-clean [180 sec, SF6 5ccm, H2 347 sccm]	2.68 Å/sec		Eureka 2000
		pre-clean [60 sec, Cl2 10 sccm, H2 70 sccm]			
		[Si2H4 15 sccm, GeH4 45 sccm]			
Si	750	[Si2H6 50sccm]	1.28 Å/sec		
SiGe(Boron)	670	H 20sccm 184sec, SiH4 20 sccm, GeH4 60 sccm 184 sec, B2H6 1.6 sccm, 30torr	7.4 Å/sec		
Si(intrinsic)	720	20H,50SiH4,30torr,356sec	2.8 Å/sec		
Si(phospours)	720	20H,50SiH4,127/127/7.3 PH3,30torr,183sec	1.38 Å/sec		
Si(Boron)	640	20H,50SiH4,116.59/116.59/8.34B2H6	2.72 Å/sec		

4. Etch

Process name	Temp	Gas	Etch rate	ETC	Equipment
Si etch	RT	HBr 20 sccm, O2 1sccm, 2mT, He 9800 Torr	33.2 Å/sec	Power (T/B) 900/80 W	STS
SiO2 etch	RT	CHF3 25 sccm, CF4 5 sccm, Ar 70 sccm	50 Å/sec		P-5000
SiNx etch	RT	CHF3 15 sccm, CF4 10 sccm, Ar 30 sccm	50 Å/sec		

5. Deposition

Process name	Temp	Gas	Deposition rate	ETC	Equipment
SiNx	785	DCS: 30sccm, NH3:100sccm, 200mTorr	40 Å/min		SHF-150L
Poly-Si	630	SiH4 : 60sccm, 150mTorr	100 Å/min		
TEOS	380	TEOS 700 sccm, 9mTorr, O2 700 sccm	70 Å/sec		P-5000
TiN	200	Ar 15 sccm, N2 85 sccm	11.62 Å/sec	Power 5kW	Endura
Ti	200	Ar 58 sccm	18.29 Å/sec	Power 2kW	
Al	200	Ar 30 sccm	125 Å/sec	Power 6kW	

Planar TFET

Seq-No	*Process Name*	*Process Specification*
10	LASER MARKER	SOI wafer and bulk wafer (test)
	Marking wafer number in backside	
20	W13A(WA-13,C1-6)SPM-CLEANING	
	Initial cleaning	
30	W5A(WA-5,C1-6) SC-1,2 CLEANING	
	RCA cleaning, HF dip	
40	CMOS FURNACE Ⅱ - WET OXIDATION	SoI thinning process
	Oxidation for thinning 1000A +/-10% Thickness checked by ellipsometer	
50	PR TRACK	
	PR coating, develop	
60	NIKON STEPPER	Active layer pattern
	Active photo [Reticle : ACT]	
70	CMOS ICP POLY ETCHER	Active etch
	Trench etch 1000A +/-10%, E/R check a-step and **SEM**	
80	CMOS PR ASHER	
	PR ashing	
90	WET STATION WA-2 SPM PR STRIP	
	PR strip	
100	W13A(WA-13,C1-6)SPM-CLEANING	
	Pre Furnace cleaning for gate oxidation, HF dip	
110	W5A(WA-5,C1-6) SC-1,2 CLEANING	
	RCA cleaning, HF dip	
120	CMOS FURNACE Ⅱ - DRY OXIDATION	Gate dielectric oxidation
	Oxidation for thinning 30A +/-5% Thickness checked by ellipsometer	
130	LPCVD Ⅲ CMOS Poly Si(직접)	Gate doposition
	Gate p-Si depo 2000A +/-10%, THK at nanospec	
140	PR TRACK	
	PR coating, develop	
150	NIKON STEPPER	
	Gate photo [Reticle : PLY]	
160	CMOS ICP POLY ETCHER	Gate etch
	Gate etch, 2000A 20% over, E/R check, pattern test	
170	CMOS PR ASHER	
	PR ashing	
180	WET STATION WA-2 SPM PR STRIP	
	PR strip	
190	PR TRACK	
	PR coating, develop	
200	NIKON STEPPER	
	Drain photo [Reticle : NSD]	

210	Medium Ion Implanter	Gate and Drain doping
	N-side, As+, 10KeV, 8E14, Tilt 7	
220	CMOS PR ASHER	
	PR ashing	
230	PR TRACK	
	PR coating, develop	
240	NIKON STEPPER	
	Source photo [Reticle : PSD]	
250	Medium Ion Implanter	Source doping
	P-well, BF2+, 10KeV, 8E14, Tilt 7	
260	CMOS PR ASHER	
	PR ashing	
270	WET STATION WA-2 SPM PR STRIP	
	PR strip	
280	RTP(C1-4)	Dopant activation
	Activation 1050C, 10sec	
290	P5000 4호기 TEOS DEPOSITION	
	ILD TEOS dep 4000A +/-10%, T17 THK ellipso	
300	PR TRACK	
	PR coating, develop	
310	NIKON STEPPER	Contact hole pattern
	Source photo [Reticle : CNT]	
320	P5000-IV SIO/SIN ETCH	Contact etch
	Spacer SiO2 etch 4000A just etch, E/R check	
330	CMOS PR ASHER	
	PR ashing	
340	WET STATION WA-2 SPM PR STRIP	
	PR strip	
350	W13C(WA13C,C1-6)50:1BHF CLEANING(NO ME	
	Pre metal cleaning	
360	Ti Dep,(CMOS,Endura system)	Contact gap fill
	Barrier metal Ti depo 300A	
370	TiN Dep,(CMOS,Endura system)	
	Barrier metal TiN depo 300A	
380	Al Dep,(CMOS,Endura system)	
	Al depo 4000A	
390	TiN Dep,(CMOS,Endura system)	AR coating
	AR metal TiN depo 300A	
400	PR TRACK	
	PR coating, develop	

410	NIKON STEPPER	Metal pad pattern
	MT1(Metal1) photo [Reticle : metal1]	
420	P5000-Ⅲ AL ETCH & 텅스텐 ETCH	
	MT1 etch 4900A target 30% over, remain ILD THK check	
430	P5000-Ⅲ PR ASHING	
	PR ashing	
440	WET STATION(WS10C.C1-2) PR STRIP	
	PR solvent strip	

Chapter 3

Simulation of the Proposed TFETs

In this chapter, novel devices are presented as vertical structure TFETs with perpendicular tunnel junction to gate. In the reported paper which introduced L-shaped TFETs, a thin Si layer enabled perpendicular tunnel to occur and a large tunnel area was employed on the source to achieve steep subthreshold swing (SS) and high on-current, which could lead to TFET's outstanding performance [17]. In the proposed device, the thin Si layer and vertical structure in a bulk substrate are combined. The proposed TFETs devices demonstrate S.S of 32 mV/decade averaged over five decades and an ON-current (I_{ON}) > 10^{-5} A/μm. Moreover, the I_{ON} can be increased easily by adjusting the height of source. However, since a hump phenomenon in the transfer curves occurred, the hump behavior in the proposed device should be investigated. After inves-

tigating it, the hump behavior is found to be originated from the two different tunnel regions. In order to remove the hump, its behavior can be suppressed by using a capping layer which can be made by gradual doping.

3.1 Introduction

In this chapter, the novel devices are proposed and simulated for a vertical type TFETs which utilizes hetero-junction and thin Si layer which is formed by Selective Epitaxy Growth (SEG) on the source side to improve ON-current (I_{ON}) and to reduce SS values. The SEG layer can utilize perpendicular tunnel to the channel. Moreover, with vertical structure, the I_{ON} of the proposed TFETs can be enhanced by adjusting the height of source. However, the hump phenomenon appeared in the transfer curves. Thus, the hump phenomena should be analyzed and proposed by simple method to reduce the hump current.

3.2 Device structure and Fabrication Method

Fig. 3.1 shows the cross-sectional view of the simulated vertical structure TFETs One of the important advantages of the proposed device is that the proposed device can be fabricated on a p-type (boron con. $10^{15}cm^{-3}$) bulk Si wafer. The p-i-n layers is formed by epitaxial growth. The p-type source which has a low band-gap material ($Si_{0.7}Ge_{0.3}$) is doped with boron 1 x $10^{20}cm^{-3}$ (N_S). On top of the source, a n-type layer are deposited. The doping concentrations of intrinsic layer and n-type layer are boron $10^{15}cm^{-3}$ (N_I) and arsenic 1 x $10^{19}cm^{-3}$

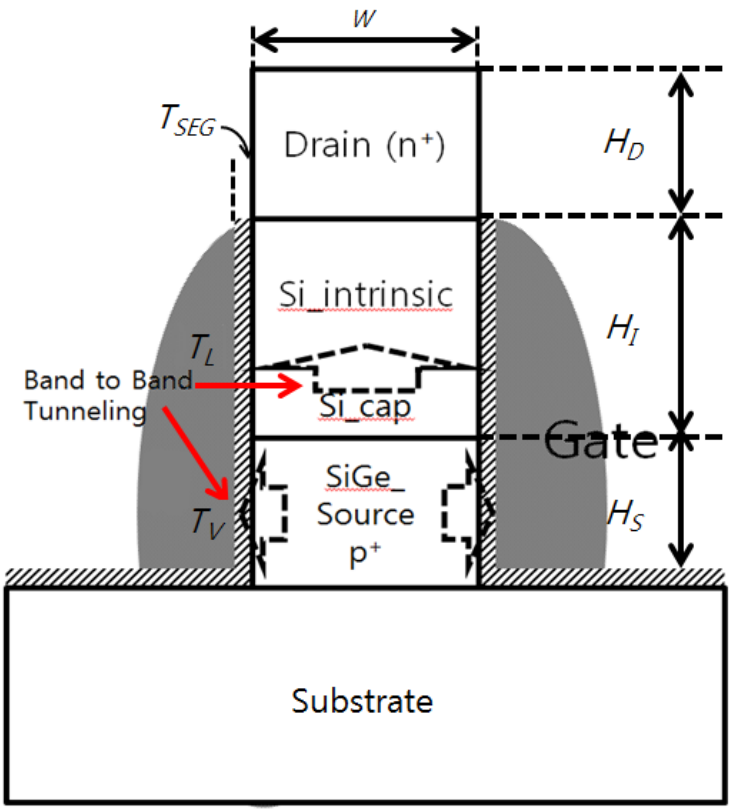


Figure 3.1 Schematic view of a vertical structure TFETs with perpendicular tunnel junction to channel. The source material is SiGe. Due to the SEG layer, the tunnel junction is formed on source region.

(N_D) respectively. Between the intrinsic layer and the source layer, the capping layer is located. The capping layer can be made by growing gradual doping layer or thermal treatment after p-i-n layers etching. The thickness of capping layer is 20 nm and doping level is changed from $10^{20}cm^{-3}$ to $10^{15}cm^{-3}$ gradually. The p-i-n layers are defined as 20 nm thick. To obtain low SS value and large on-current, SEG is performed by depositing a Si layer on the etched the p-i-n layers. By the SEG layer, it is possible the perpendicular tunnel to the channel. After the active formation, gate dielectric is deposited as 1 nm of SiO_2. Then TiN is deposited as a gate electrode (work function 4.3 eV). The TiN gate is defined by sidewall spacer technology. Simulation conditions are summarized in Table 3.1. The key processes of device fabrication are depicted in Fig. 3.2. The utilized device simulation tool is Sentaurus [18]. For accurate calculation of the BTBT, a non-local tunnel model is used.

3.3 Simulation Results and Discussion

Fig. 3.3 shows the energy band diagrams of the conventional planar TFETs and the proposed TFETs with various gate biases. In the case of the conventional TFETs, tunnel width (W_t) is gradually changed depending on the gate bias because the W_t is strongly related to depletion width between source and channel as can be seen in Fig. 3.3(a). However, the proposed TFETs have limited maximum W_t, which is the same as the length of SEG layer (T_{SEG}) as shown in Fig. 3.3(b). According to the BTBT theory, the I_{ON} of TFETs is proportional

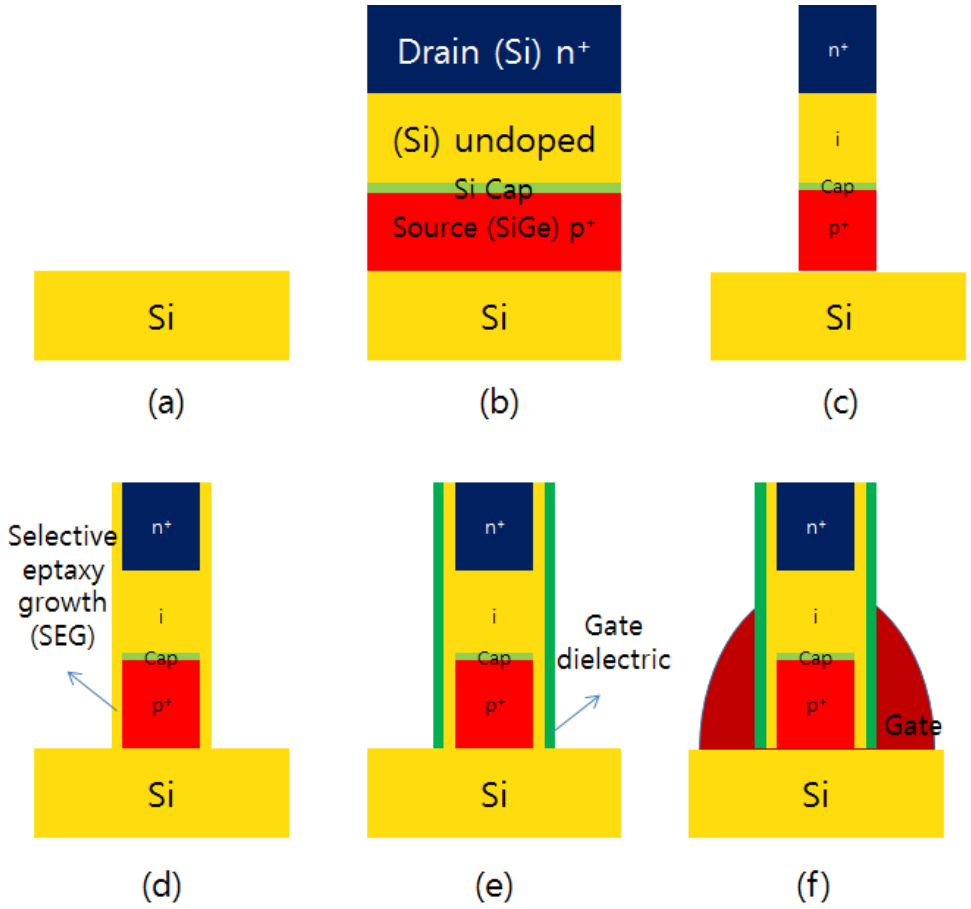


Figure 3.2 Key fabrication steps. (a) Starting with a Si bulk wafer. (b) Growing the p-i-n epitaxial layers with in-situ doping. (c) Patterning and Etching the p-i-n layers (d) growing the channel layer with SEG (e) Depositing gate dielectric (f) Forming a metal gate side wall spacer

Table 3.1 Simulated device parameters for the proposed TFETs.

V_{DD}	1.5 V
Height of drain (H_D)	50 nm
Height of intrinsic Si (H_I)	50 nm
Height of drain (H_S)	50 nm
Drain doping conc. (N_D)	n-type 10^{19} cm^{-3}
Channel doping conc. (N_I)	p-type 10^{15} cm^{-3}
Source doping conc. (N_S)	p-type 10^{20} cm^{-3}
Thickness of SEG (T_{SEG})	5 nm
Width (W)	50 nm
Effective oxide thick. (T_{ox})	1 nm

to $(1/W_t)\exp(-W_t)$. Therefore, high I_{ON} is attainable in the proposed TFETs. Furthermore, as W_t decreases, the ON-OFF transition of TFETs becomes more abrupt and its SS gets lowered. To confirm effect of the perpendicular tunnel junction in the vertical TFETs, the proposed devices should be further simulated. Fig. 3.4(a) shows transfer curves of the conventional TFETs and proposed TFETs. With perpendicular tunnel junction to the channel, the vertical TFETs show high I_{ON}. In particular, the proposed TFETs shows flat current saturation compared with the planar TFETs. In detail, the perpendicular tunnel has almost constant tunnel width by formed the SEG layer when the gate bias is applied. In the contrary, when the same gate bias is applied, lateral tunnel is increased gradually because the tunnel width is decreased steadily. The height of source is proportional to the ON-current because the length of tunnel junction is equal to the sum of fin width (W) + source height (H_S). Therefore ON-current of the device can be enhanced by increasing of the source height (Fig. 3.4(b)). In addition, it has been observed in the process that the transfer curve shows hump behavior. This unique behavior is originated from the SEG region and p-i-n region, which means that there are two tunnel junctions orthogonally whose threshold voltages are different. Thus, it is necessary to analyze the effects of the tunnel independently. In order to analyze the hump behavior, BTBT rates are confirmed when the gate region is applied at 0.5 V and 1.5 V respectively. When the gate bias is 0.5 V, BTBT is observed at the junction between the p-type layer and the intrinsic layer as shown Fig. 3.4. It

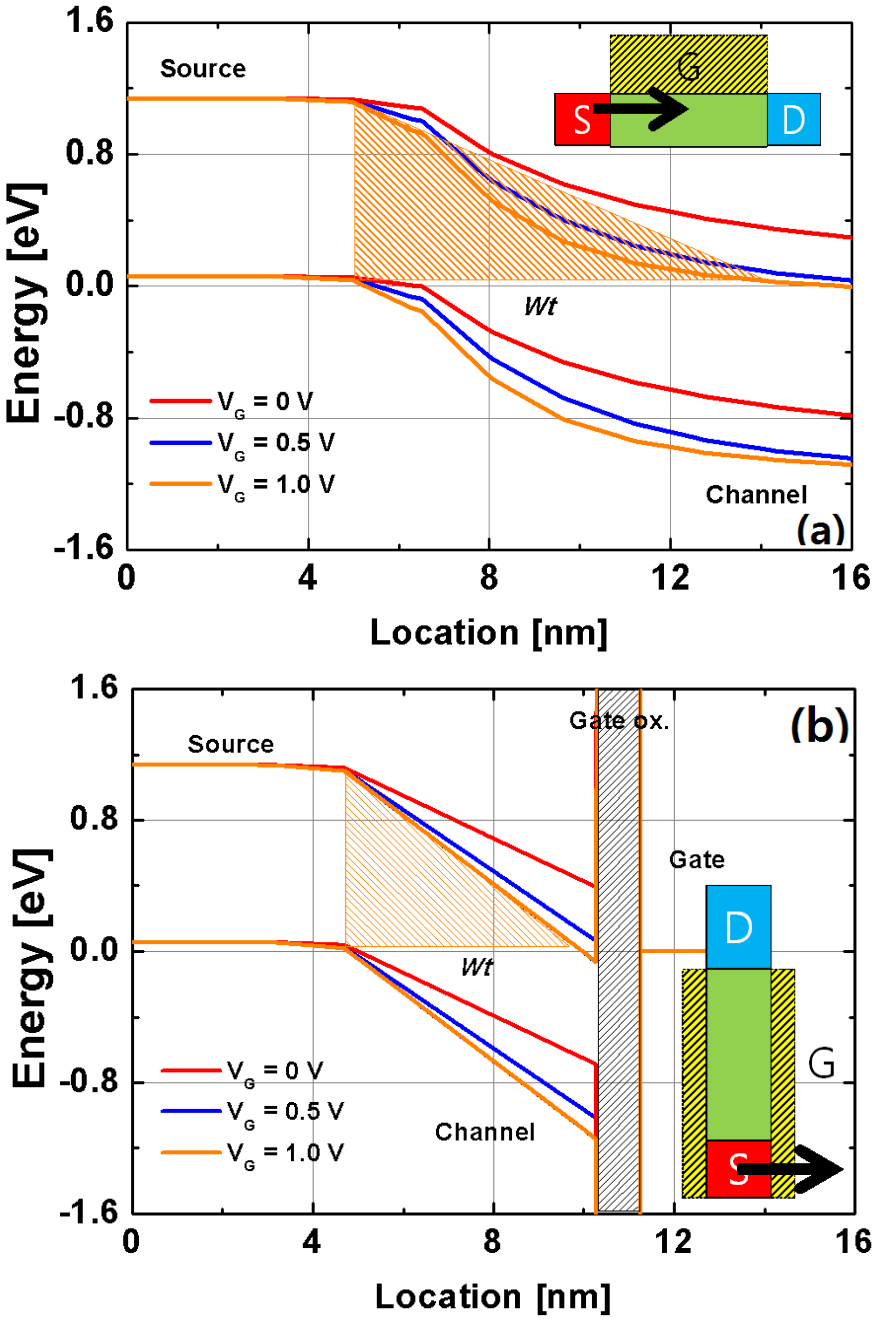


Figure 3.3 Simulated energy band diagram changes as a function of gate voltage in (a) Conventional planar TFETs and in (b) the proposed TFETs.

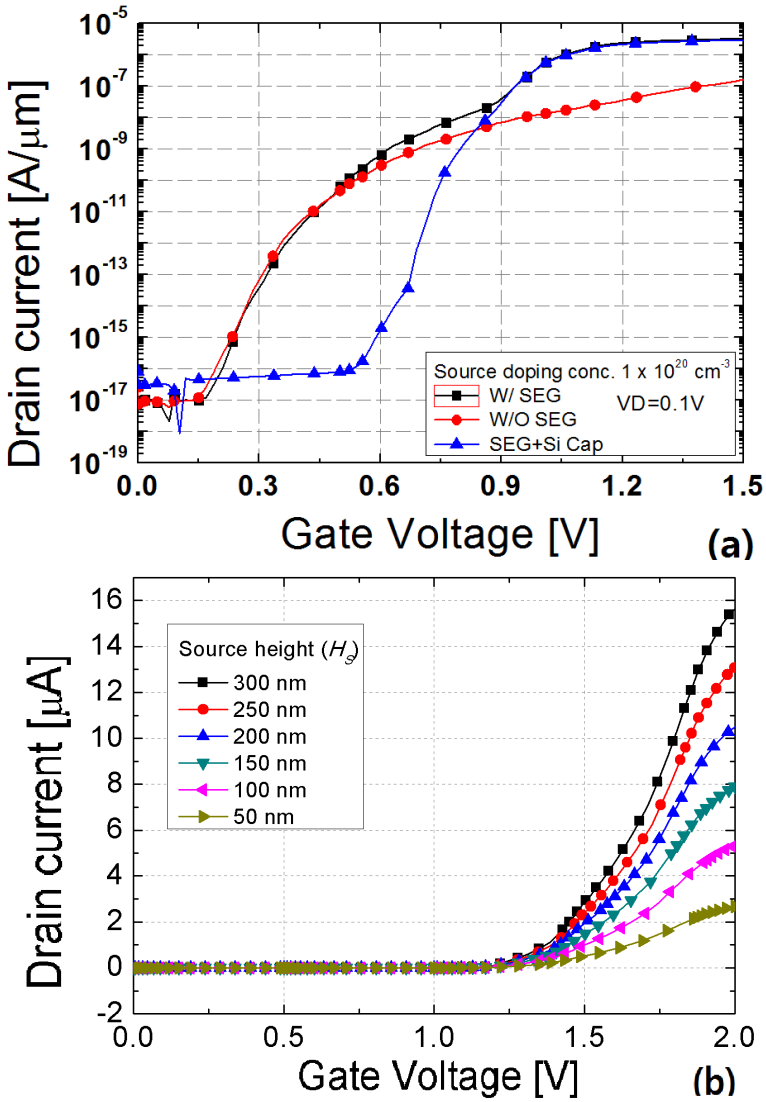


Figure 3.4 (a) I_D–V_D characteristic of a vertical structure TFETs devices with SEG layer and without SEG layer. The device with SEG layer shows hump phenomena. (b) I_D–V_D characteristics of a vertical structure TFETs device depending on various heights of source.

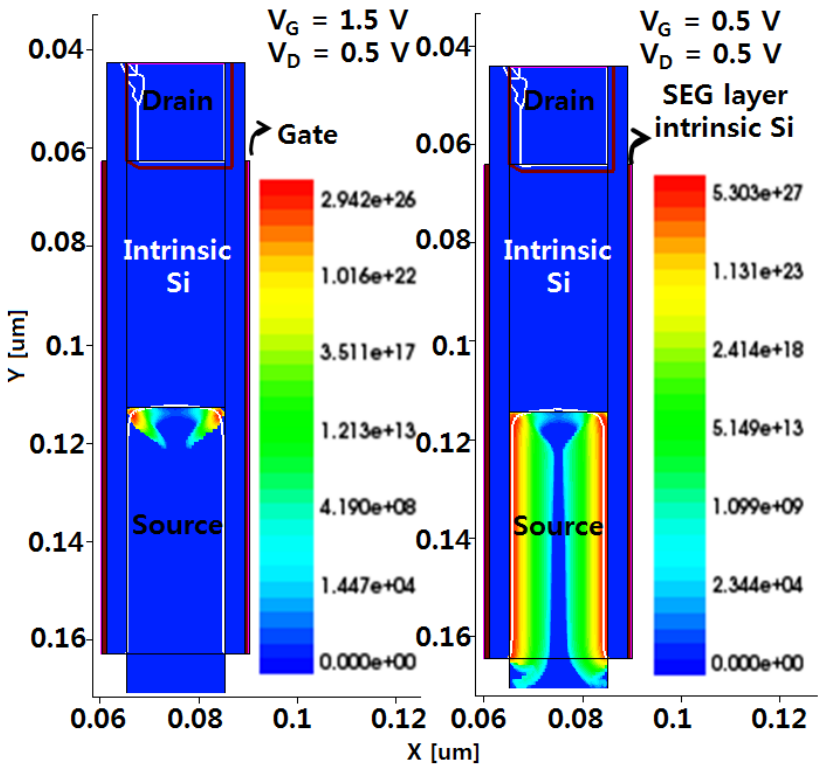


Figure 3.5 Band to band tunnel rate. The dominant tunnel region changed by applied gate voltage.

means that, at the low gate bias, BTBT at the junction between p-type layer and intrinsic layer (T_V) can contribute to the current. However, when the gate bias is 1.5 V, the BTBT rate at the junction between p-type layer and SEG layer (T_V) is increased more than that of T_L. As a result, the transfer curve of the TFETs with SEG layer is the superposition of two tunnel components from T_L and T_V (Fig. 3.1). In order to reduce the hump behavior, the current from T_L should be reduced or the threshold voltage of the T_L component should be shifted to positive direction than that from the T_V component. Therefore, the gradual doping layer at the junction between intrinsic layer and source layer is proposed as shown in the Fig. 3.1. By inserting gradual doping layer, the thickness of SEG layer is increased. In other words, electron tunnel can occur with a very low probability when the valence band of source and conduction band of the junction are aligned. Fig. 3.4(a) shows the transfer curves of the TFETs with Si capping layer. In the transfer curve, the hump behavior is not observed. Moreover, the on-current is maintained at the same level in spite of the inserted Si capping layer and the proposed structure shows a record-low SS of 32 mV/decade from 10^{-15} A/μm to 10^{-10}A/μm.

3.4 Summary of Simulation

In this chapter, vertical structure TFETs with perpendicular tunnel junction to gate was demonstrated by the simulation. For the proposed device, the hump effects of vertical type TFETs have been discussed. Based on the TCAD sim-

ulation results, it has been found that the hump effects are originated from the different tunnel regions which are connected perpendicularly. For further improvements of the proposed TFETs, the Si capping layer is proposed and its effectiveness is confirmed. The proposed structure shows a record-low SS of 32 mV/decade and $I_{ON} > 10^{-5}$ A/μm.

Chapter 4

Fabrication of the Proposed TFETs

In this chapter, the proposed TFETs are fabricated on a bulk Si substrate with perpendicular tunnel junction to gate for the first time. A thin intrinsic Si used as a perpendicular tunnel layer is epitaxially grown on the source region, resulting in an abrupt band bending at the tunnel junction. The fabricated TFETs show 17 mV/dec point-to-pint minimum subthreshold swing (SS) and 10^4 ON/OFF current ratio (I_{ON}/I_{OFF}) for sub-0.7 V gate overdrive. In addition, SS is maintained less than 60 mV/dec while drain current increases from the complete OFF-state (10^{-13}) to more than two orders of magnitude (10^{-11}).

4.1 Introduction

In this chapter, the proposed TFETs are demonstrated to overcome above-mentioned problems. The double gate and SEG layer with perpendicular tunnel to the channel are formed to reduce tunnel resistance and to achieve low SS. The proposed TFETs show minimum SS of 17 mV/decade and the high ON/OFF current ratio (I_{ON}/I_{OFF}) of 10^4. Furthermore, it can be simply co-integrated with MOSFETs on bulk Si by using well established standard CMOS processes.

4.2 Device Structure and Fabrication Method

The fabrication process of proposed devices was depicted in Fig. 4.1(a). Starting with p-type (10^{15} cm^{-3} boron doped) bulk Si wafer, active region was defined by 300 nm-thick local oxidation of silicon (LOCOS). Three layers were epitaxially grown on the active region in sequence: 100 nm-thick p-type source, 175 nm-thick p-type channel and 50 nm-thick n-type drain (Fig. 4.2(a) and 4.2(b)). The grown layers are confirmed by selected area electron diffraction (SAED). Fig. 4.3(a) and 4.3(b) showed that the preferred crystal growth direction of Si and SiGe. Each doping concentration is 5 x 10^{19} cm^{-3}, 1 x 10^{17} cm^{-3} and 1 x 10^{20} cm^{-3}, respectively. The dopant profile is shown in Fig. 4.4. Here, it should be noted that the n-type region is gradually doped because it determines the ambipolar current. After the epitaxial growth, the active layers were patterned with i-line photo-lithography and dry-etched with reactive ion etch (RIE) to form the vertical p-i-n structure whose dimensions were 1 x 0.5 μm^2 (Fig. 4.5).

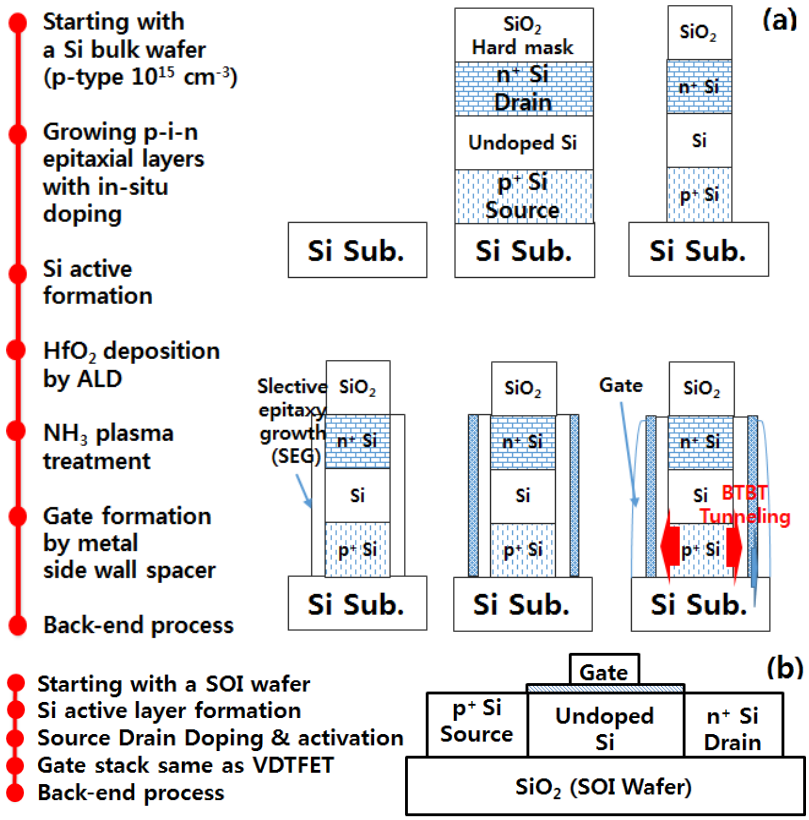


Figure 4.1 (a) Schematic diagram and process flow for the proposed TFETs. Between the intrinsic Si layers and the source regions, the tunnel junctions are formed. (b) Schematic diagram and process flow for conventional TFETs.

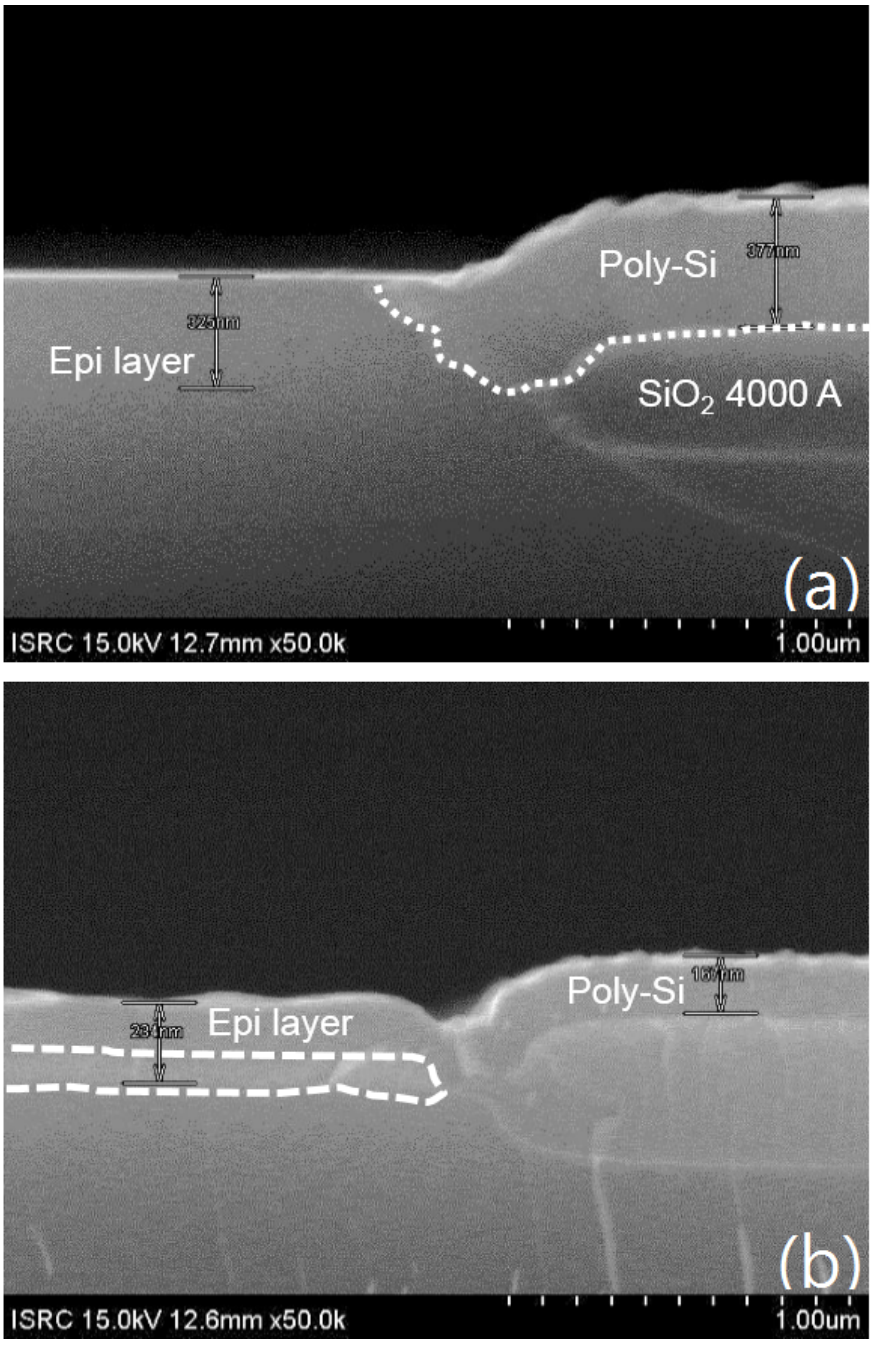


Figure 4.2 TEM image about epitaxy layer(a) Si source (b) SiGe source.

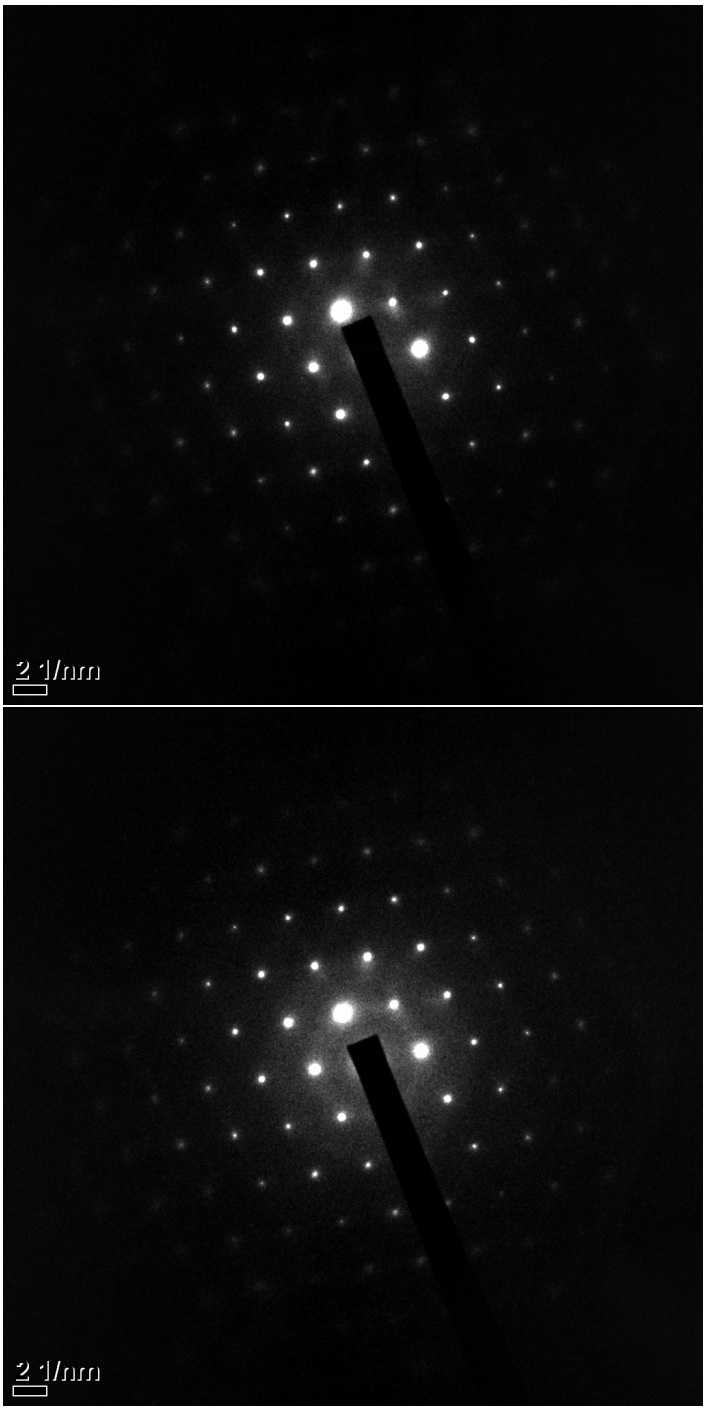


Figure 4.3 The selected-area electron diffraction analysis of(a) Si (b) SiGe.

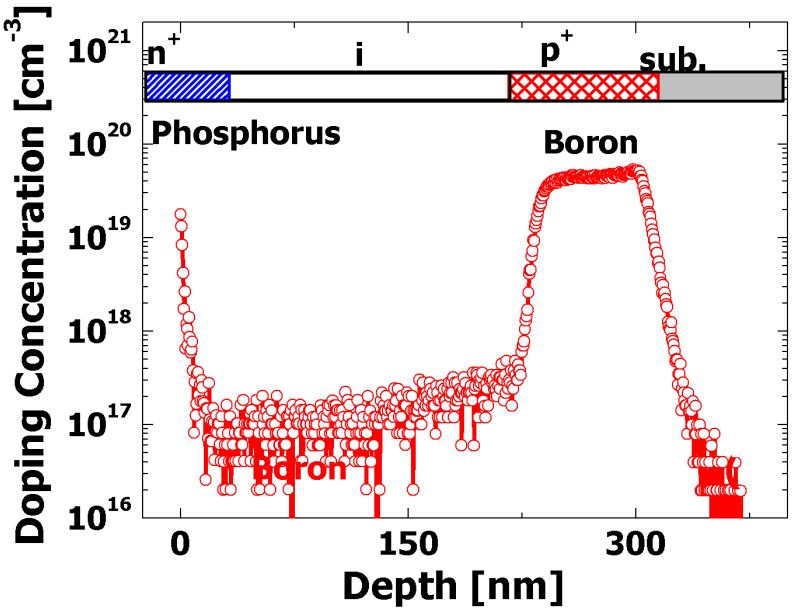


Figure 4.4 SIMS profile indicating phosphorus and boron concentration vs. depth. The dopants are doped by in-situ method when the Si layers are grown.

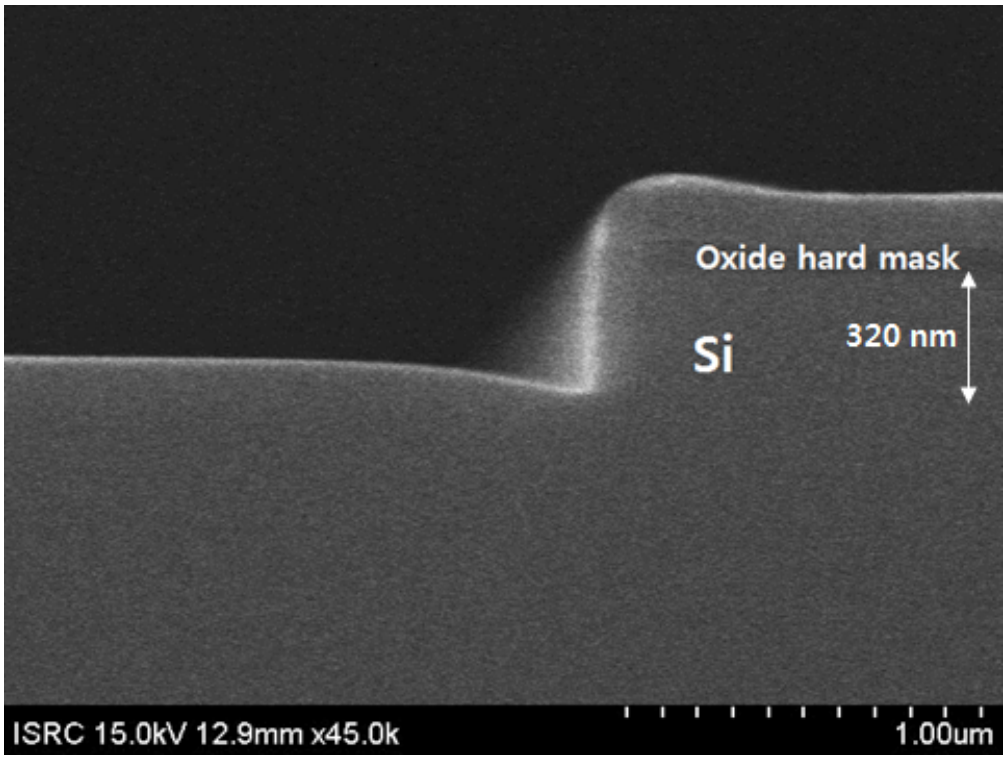


Figure 4.5 SEM image of active patterning with RIE process.

A thin intrinsic Si layer was grown on the side of source by selective epitaxial growth (SEG) at 670 °C to form the perpendicular tunnel junction between the source and the thin Si layer. The SEG layer with 13 nm thickness was successfully grown. HfO_2 of 5 nm thickness was deposited as a gate dielectric. The deposition process is performed by atomic layer deposition (ALD) process. The effective oxide thickness of the HfO_2 layer was 1.7 nm. Then, NH_3 plasma treatment was performed to form an HfON interfacial layer on the Si surface for better interface and higher permittivity than SiO_2[19]. In the Fig. 4.6(a), the cross-sectional TEM image are shown that the HfO_2 and interfacial layer

formed and the thickness of HfO_2 is 5 nm. And the Auger electron spectroscopy (AES) showed that a nitrogen is distributed in the HfO_2 and Si interface (Fig. 4.6(b)). Fig. 4.7 confirms that hysteresis, gate leakage current, and Effective Oxide Thickness (EOT) are all reduced due to the better interface and higher permittivity by the NH_3 plasma treatment (Current and capacitance were measured by using the HP 4156 C semiconductor and parameter analyzer and HP 4284 A precision LCR meter, respectively). Subsequently, TiN was deposited by sputtering process as a gate-metal (work function 4.58 eV) as shown in the high resolution transmission electron microscopy (HRTEM) image (Fig. 4.8). Finally, inter-layer dielectric (ILD) was formed with tetra-ethyl-ortho-silicate (TEOS) oxide by PECVD process and metal layers (Ti/TiN/Al/TiN stacks) were deposited by physical vapor deposition (PVD) process to make contact. In order to prepare control samples, planar TFETs had been fabricated by the process sequence of Fig. 4.1(b). First, active region was defined on 30 nm thickness of SOI substrate. The size of the active region is the same as that of the proposed TFETs Source and drain were formed by implantation. The source and the drain regions were doped with boron (5 x 10^{19} cm^{-3}) and arsenic (5 x 10^{19} cm^{-3}), respectively. In order to activate the dopants, rapid thermal annealing (RTA) process of 850 °C was performed during 30 sec. After the source and drain formation, the other steps were performed with the proposed TFETs. With the same material and thickness of gate stacks, the conventional planar TFETs and the proposed TFETs were compared.

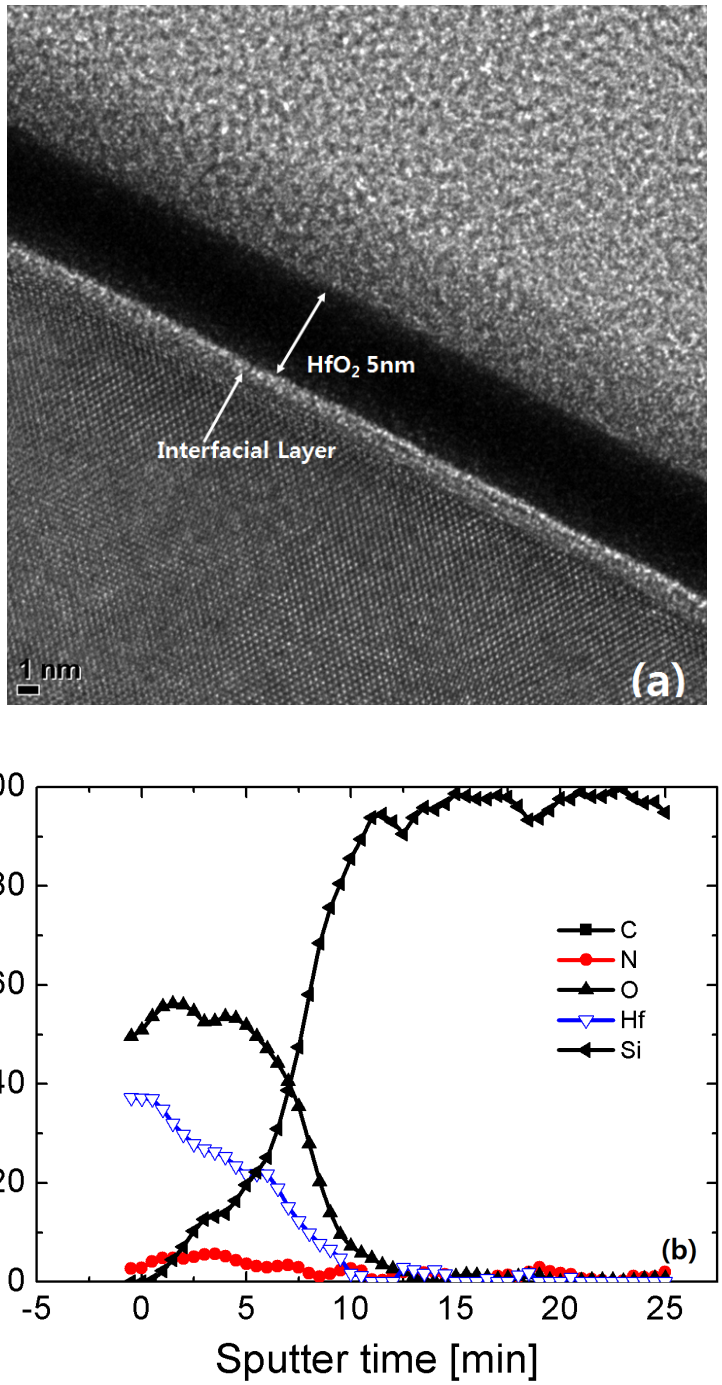


Figure 4.6 (a) Cross-sectional TEM image of a 5nm- HfO_2 film grown by ALD (b) AES depth profiles of HfO_2 films after NH_3 plasma treatment.

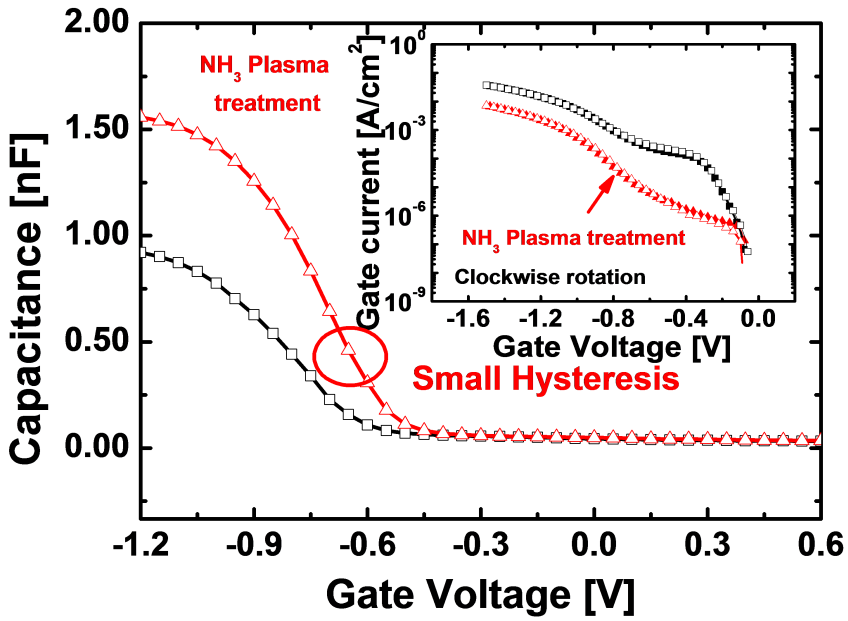


Figure 4.7 Measured hysteresis C–V curves of MOS capacitors with high-κ/metal gate stacks. The inset shows gate leakage current.

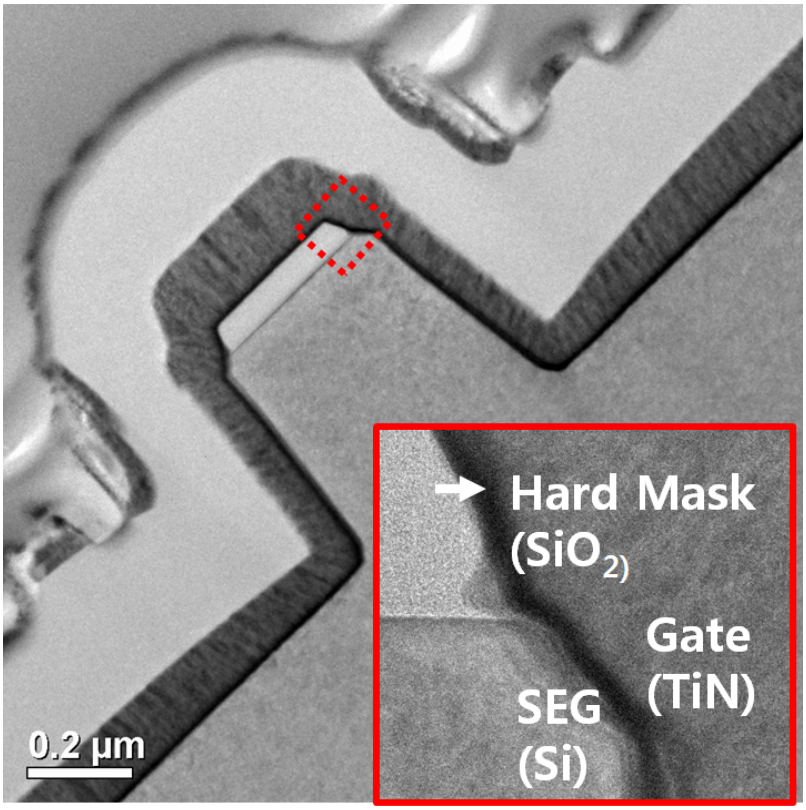


Figure 4.8 Cross-sectional HRTEM image which demonstrates fin structure. The thin epitaxially grown Si layer has 13 nm thickness.

4.3 Experimental results

In order to investigate the effects of the thin Si layer on the source in the proposed TFETs, TCAD simulations are performed with Synopsys SentaurusTM. Fig. 4.10(a) shows the transfer characteristics of the conventional TFETs and the proposed TFETs at 0.1 and 1.0 V drain voltages (V_D). Fig. 4.10(b) shows the output characteristics measured at various gate voltages. All the TFETs have 1 x 0.5 μm^2 active area and the proposed TFETs have the T_{SEG} of 13 nm. The turn-ON voltage ($V_{Turn-ON}$) is defined as the V_G where BTBT starts to occur. As compared to the conventional TFETs, the proposed TFETs show the outstanding performances such as low SS and large I_{ON}. The minimum SS value is 17 mV/dec and the I_{ON}/I_{OFF} ratio of 10^4 is obtained. The SS value is extracted at V_D of 0.1 V. Control groups consist of proposed Si TFETs and planar SiGe TFETs. The SS property of the proposed device is improved due to narrow band-gap. The I_{ON} enhances 1.8 times more than that of Si control group. Fig. 4.11 shows the subthreshold swing of the proposed TFETs with Si source as a function of drain current measured by forward and reverse sweeps. The results indicate that the quality of gate dielectric is so high that the difference between the forward and reverse sweeps is negligible and the proposed TFETs can have SS $<$ 60 mV/dec in a wide range of the drain current regardless of the forward and reverse sweeps. On the other hand, the the subthreshold swing of the proposed TFETs with SiGe source as a function of drain current show degraded performance due to the high I_{OFF} (Fig. 4.12). In terms of the

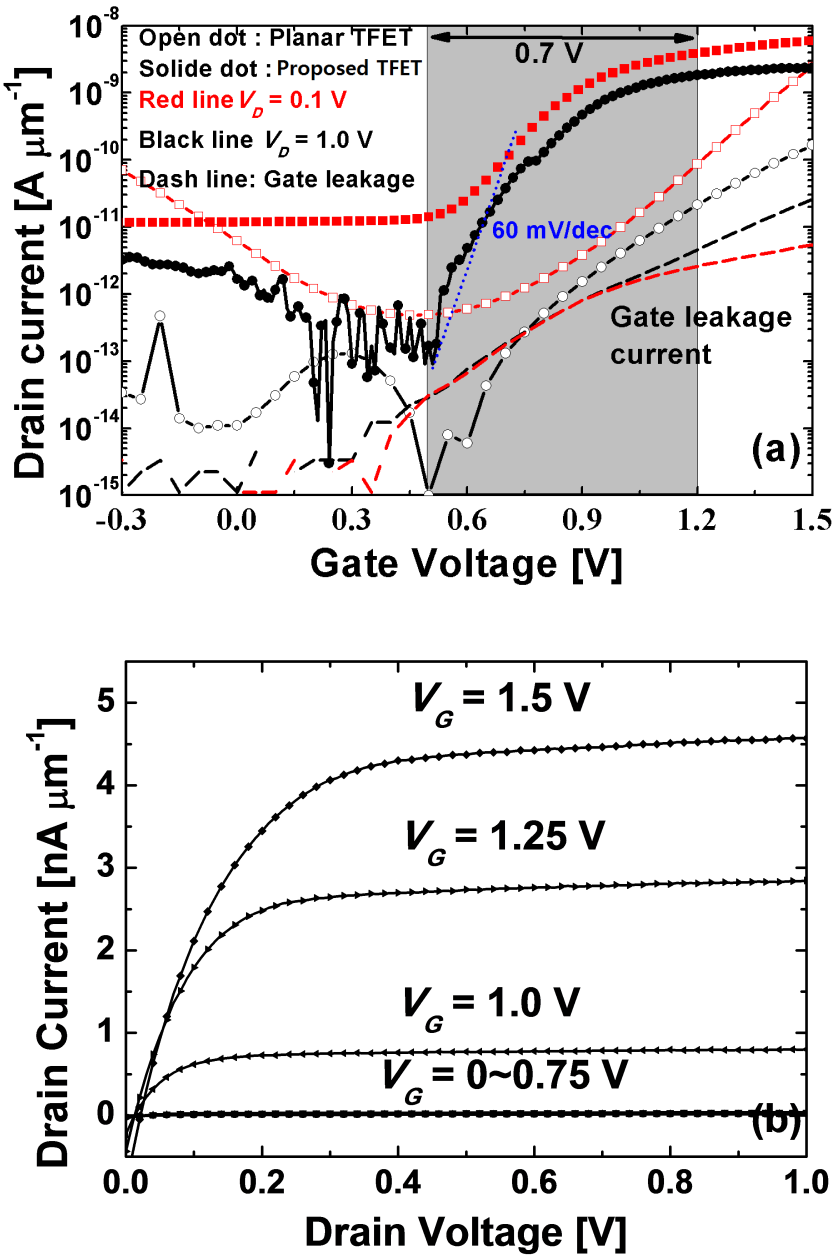


Figure 4.9 (a) Transfer characteristics of the proposed TFETs and conventional planar TFETs. (b) Output characteristics of proposed TFETs measured at various gate voltages.

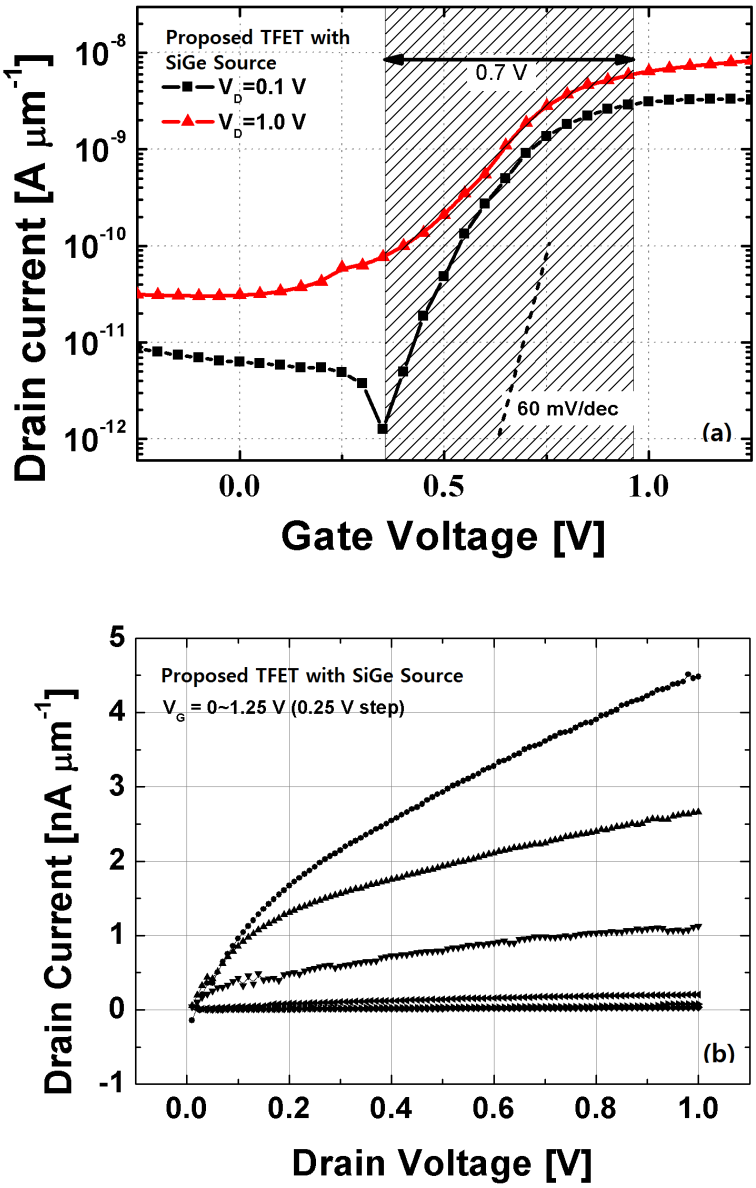


Figure 4.10 (a) Transfer characteristic of the proposed TFETs with SiGe source. (b) Output characteristic of the proposed TFETs measured at various gate voltages.

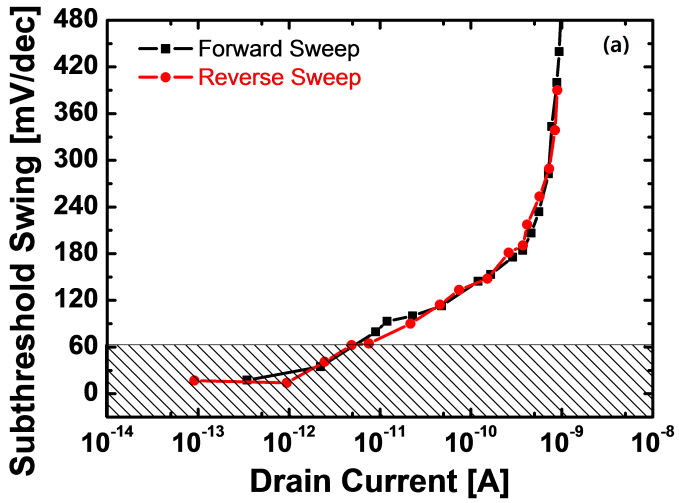


Figure 4.11 SS of the proposed TFETs with Si source as a function of drain current measured by forward and reverse sweeps. The the proposed TFETs show steep SS below 20 mV/dec in both forward and reverse sweeps.

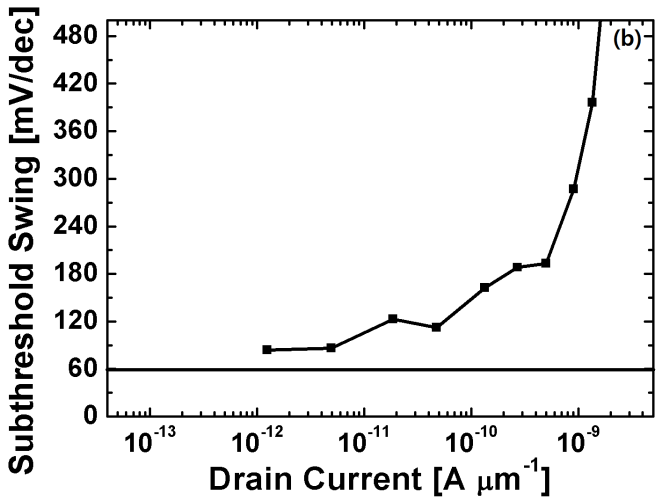


Figure 4.12 SS of the proposed TFETs with SiGe source as a function of drain current.

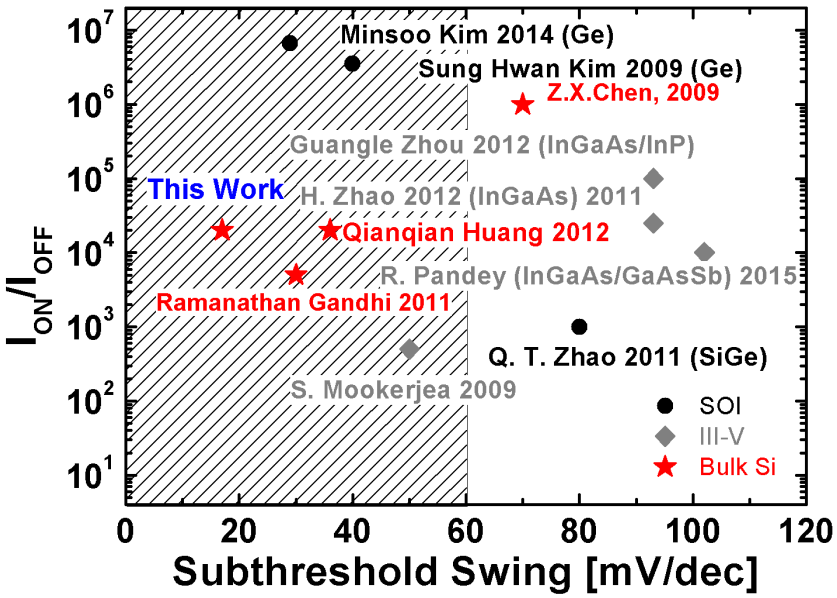


Figure 4.13 Performance comparison of TFETs. I_{ON}/I_{OFF} of TFETs as a function of subthreshold swing.

comparison of TFETs performances, the absolute value of I_{ON} may not be a good indicator because many TFETs with III-V compound semiconductor show high I_{OFF} despite of high I_{ON} [20]-[21]. Thus, the I_{ON}/I_{OFF} ratio should be used as the indicator of the performance comparison to consider both ON and OFF-states. To compare the performance of the proposed TFETs to those of other TFETs, the I_{ON}/I_{OFF} ratios of the TFETs are extracted as a function of subthreshold swing as shown in Fig. 4.13 [20]-[29]. All of the I_{ON}/I_{OFF} values are extracted as a function of minimum SS value when the gate overdrive

voltage of 0.7 V is applied to the devices. Compared with other bulk Si based TFETs, the proposed TFETs show the remarkable performance in terms of minimum SS and I_{ON}/I_{OFF} ratio. The further direction of this study will be to enhance the electrical performance of the proposed TFETs by optimizing the device parameters and applying the advanced techniques such as the stress engineering and the use of materials with a various band-gap.

4.4 Discussion

In the previous section, the performance of the proposed TFETs is measured and compared with that of other groups. Although the performance of the proposed TFETs shows better values than that of conventional TFETs, the fabricated TFETs do not still satisfy industrial demand. Therefore, in this section, the proposed TFETs are analyzed to confirm the cause of degraded performance.

4.4.1 High OFF leakage current

As mentioned before, TFETs are a promising device due to its low OFF current. As compared to the conventional TFETs, the proposed TFETs show the high I_{OFF} at negative V_G (Fig. 4.9(a)). In order to confirm the cause of high leakage current, the transfer curves with various drain pad sizes are shown in the Fig. 4.14. At the 0 V of V_G, the current levels depend on the contact size and source material. The drain pad is defined to form contact. The current level is

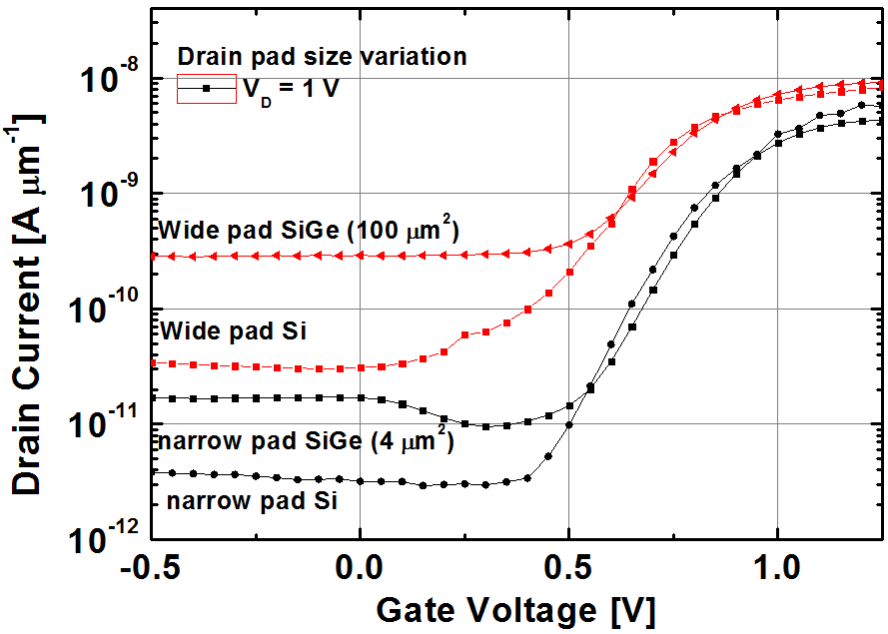


Figure 4.14 Transfer curves with various contact size. The I_{OFF} is depend on the pad size.

proportional to the drain pad size. In order to verify the path in the proposed TFETs, the cross-sectional SEM image is shown in Fig. 4.15(a) where drain pad is. In the SEM image, it is confirmed that the source is formed at the bottom of drain pad. As p-i-n layers are formed in one process with in-situ doping, the drain pad has p-i-n structure which is parasitic diode in the proposed TFETs. Therefore, as the drain bias applied, reverse diode current is formed in the drain pad (Fig. 4.15(b)). In order to minimize the reverse diode current, the epitaxy process which is performed to grow p-i-n layers, needs more patterning and etch process to eliminate the source under the drain pad.

4.4.2 Short channel effect

In the Fig. 4.10 (b), the measured output characteristics show that the current is increased with V_D. Fig. 4.10(b) shows that the performance of the proposed TFETs with SiGe source depends on the channel length. Note that, many papers have reported that there is little gate-length dependence [30]. According to the paper, the drain bias has little influence on tunnel junction [31]. As the channel length decreases, the lateral electric field is induced at the tunnel junction by the drain voltage which increases BTBT to occur at a smaller gate voltage. As a result, the influence of the gate voltage is diminished, SS becomes less steep and I_{ON}/I_{OFF} decreases. In order to confirm the short channel effect in the proposed TFETs, TCAD simulation is performed. The parameters of simulation are the same with the simulation which is performed in the chapter 3. Fig. 4. 16 shows that at the the case of channel length below 40 nm, the short

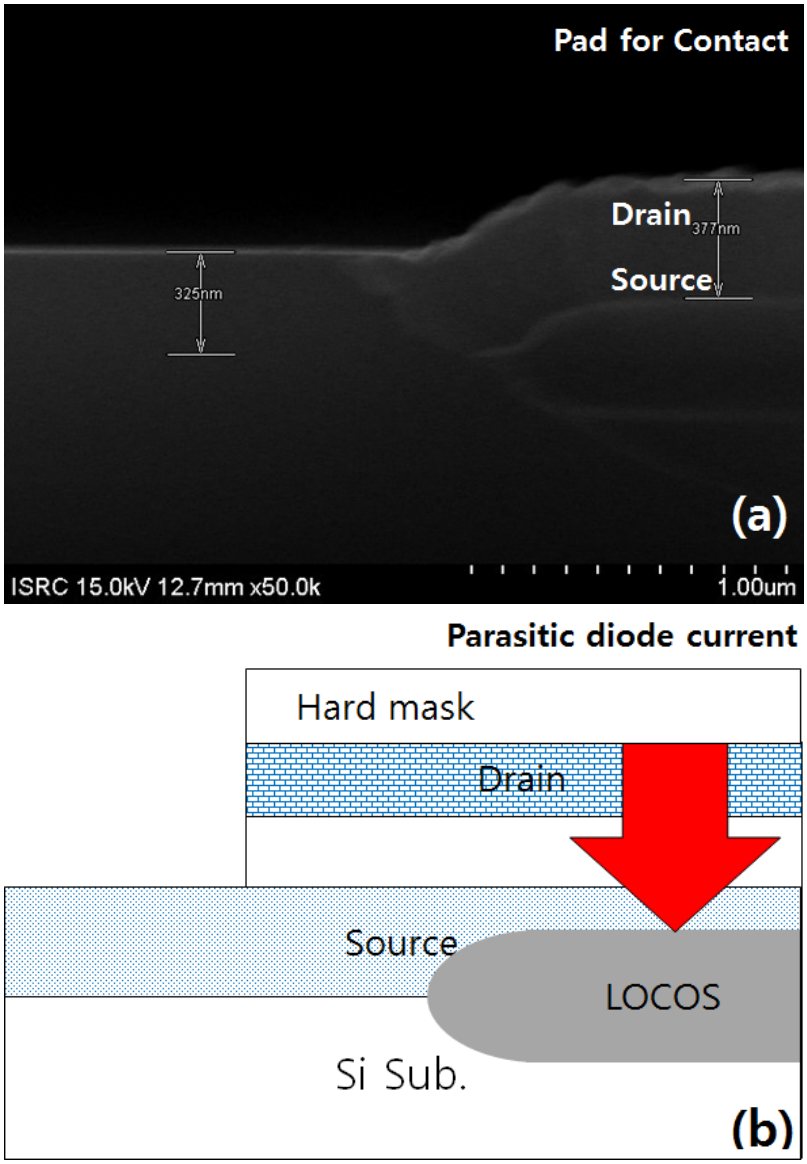


Figure 4.15 (a)Cross-sectional image of drain pad, (b)Illustration of parasitic diode current in drain pad

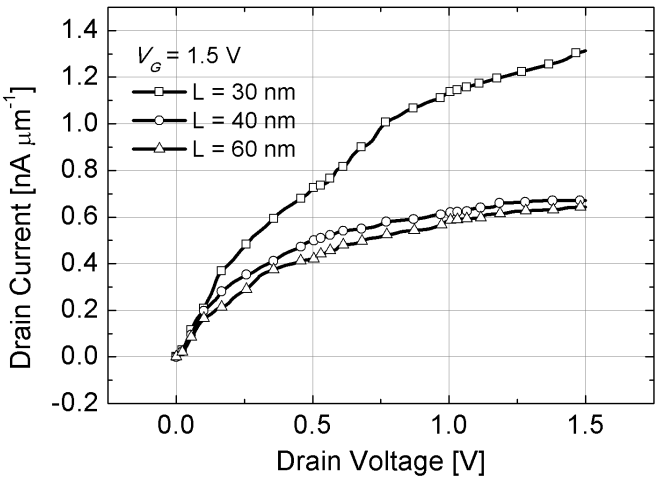


Figure 4.16 Output characteristic of the proposed TFETs simulated with various channel length.

channel effect is confirmed. It means that, in the short channel device, BTBT at the junction between p-type layer and intrinsic layer (T_V) can contribute to the current (Fig. 4.1). As a result, the current of the proposed TFETs is the superposition of two tunnel components from T_L and T_V. In order to reduce this short channel effect, the current from T_L should be reduced or the threshold voltage of the T_L component shifted to the positive direction.

4.4.3 Current Saturation by Drain

In the conventional TFETs, when the negative gate bias modulates channel potential, the tunnel current flows at the channel-drain. This tunnel current called by ambipolar current is shown in the TFETs as unique characteristics.

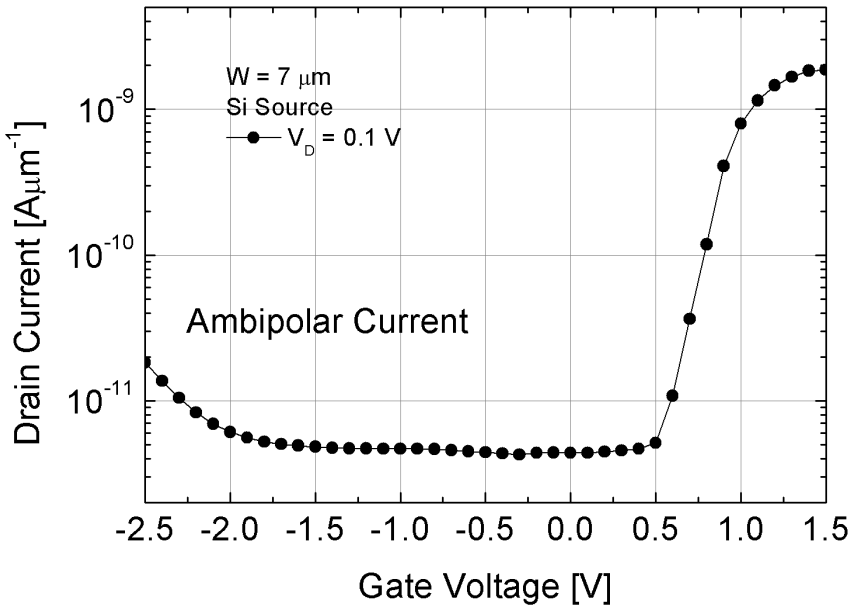


Figure 4.17 Transfer curves of the proposed TFETs. In the plot, the ambipolar characteristics are confirmed at -2.5 V of V_G.

In the transfer curves in the proposed TFETs, the ambipolar characteristics are not observable compared with the conventional TFETs (Fig. 4.9(a)). In order to confirm the ambipolar current, a high gate bias is applied with 1.0 V of V_D. At the -2.5 V of V_G, the ambipolar current is verified. In the the proposed TFETs, the ambipolar current is significantly suppressed. The suppression of ambipolar current is for the insufficient dopant activation. Although SIMS profile shows high dopant concentration in the drain region, the dopants are not activated due to the lack of process temperature. In order to confirm the

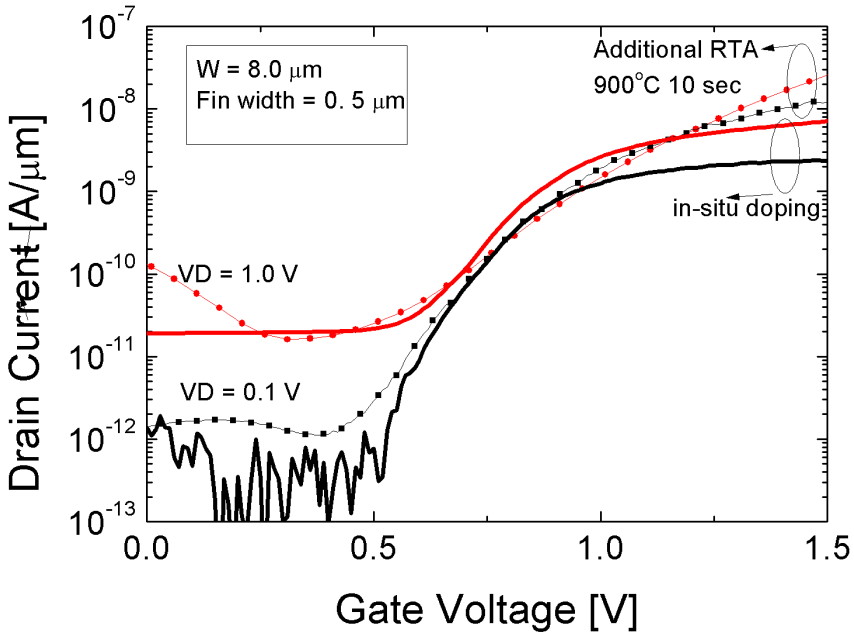


Figure 4.18 Transfer curve of the proposed TFETs with additional RTA process.

insufficient dopant activation, additional RTA process is performed with the proposed TFETs. The condition of RTA process is 900 °C and 10 sec. In the Fig. 4. 18, the transfer curves with RTA process shows higher current than that of unprocessed proposed TFETs. Moreover, the ambipolar current is also enhanced. Due to the low effective doping level, the resistance of drain contact is relatively high. In the Fig. 4.14 the I_{ON} depends on the pad size. From the result, it is confirmed that the current of the proposed TFETs is limited by the high contact resistance. It can explain the little difference between the proposed TFETs of Si and SiGe. The difference of I_{ON} between Si and SiGe the proposed TFETs is only 1.65 times. Compared with the conventional TFETs, there is little enhancement of the current despite the idea utilizing the proposed structure. Consequently, the source of the proposed TFETs is formed by epitaxy in the low temperature process.

4.4.4 Process Optimization

Compared with ITRS roadmap, the measured transfer curves show small amount of current. One of the most important obstacles for implementing the high performance of TFETs is the small current drivability. Fig. 4.18 shows that the performance of the proposed TFETs by TCAD simulation. The I_{ON} is fitted by measured data. Then, the thickness of SEG layer is adjusted. As thickness of the SEG layer decreased, the I_{ON} is increased dramatically. As a result, the tunnel width is determined by thickness of SEG layer. From optimizing the physical dimension, the current drivability is expected to improve.

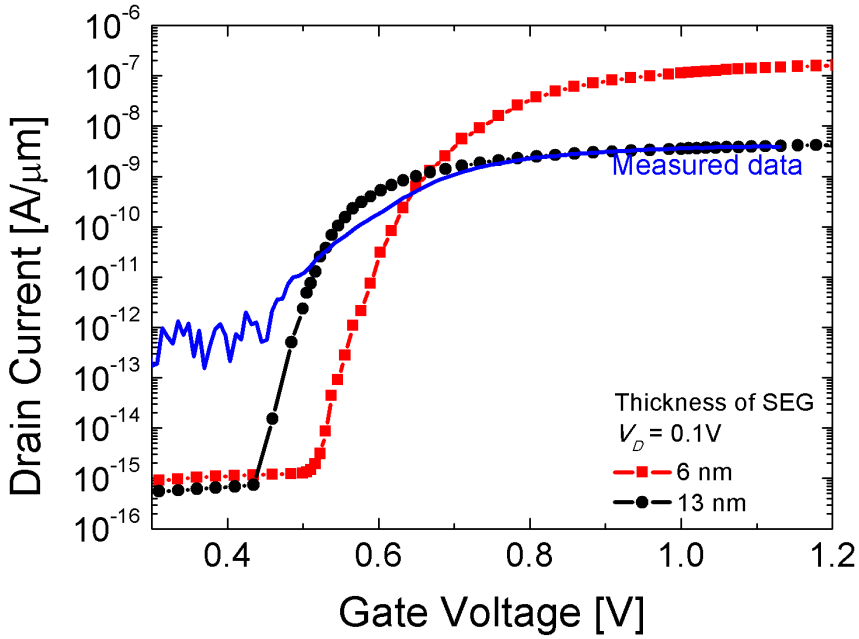


Figure 4.19 Transfer curves of the proposed TFETs and simulated TFETs. In the plot, the simulation results show effects of thickness of the SEG layer.

4.5 Summary

In conclusion, a vertical structure TFETs with the perpendicular tunnel to the channel on the bulk Si substrate have been fabricated successfully. To the best of our knowledge, our results are the first reported data for TFETs with the perpendicular tunnel junction to channel. The vertical structure is applied due to excellent carrier tunnel controllability and integration on bulk Si. Moreover, the perpendicular tunnel junction is formed through the epitaxial growth to achieve low SS by a steep band bending near the tunnel junction. Consequently, the proposed TFETs demonstrate remarkable performances in terms of SS and I_{ON}/I_{OFF} ratio (17 mV/dec minimum SS and 10^4 I_{OFF}/I_{OFF} for sub-0.7 V gate overdrive).

4.6 Appendix: Process Flow

Note that, the recipe of each steps is the same with the section 2.5 Appendix. Only time in etch process and deposition process are different to be adapted for the proposed TFETs. Therefore in this section, the total process sequence is depicted.

Process flow for HKMG Planar TFETs

Seq. No	*Process Name*	*Process Specification*
10	LASER MARKER	SOI wafer and bulk wafer (test)
	Marking wafer number in backside	
20	W13A(WA-13,C1-6)SPM-CLEANING	
	Initial cleaning	
30	W5A(WA-5,C1-6) SC-1,2 CLEANING	
	RCA cleaning, HF dip	
40	CMOS FURNACE II - WET OXIDATION	SOI thinning process
	Oxidation for thinning 1000A +/-10%, Tickness checked by ellipsometer	
50	WET STATION WA-3 BHF 7:1	Oxide strip
	Buffer oxide strip 1000A, sheet off check	
60	PR TRACK	
	PR coating, develop	
70	NIKON STEPPER	Active layer pattern
	Active photo [Reticle : ACT]	
80	CMOS ICP POLY ETCHER	Active etch
	Activce etch 500A +/-10%, thk. check a-step and SEM	
90	CMOS PR ASHER	
	PR ashing O2 plasma	
100	WET STATION WA-2 SPM PR STRIP	
	PR strip	
110	PR TRACK	Source pattern (open)
	PR coating, develop	
120	NIKON STEPPER	
	Active photo [Reticle : PSD]	
130	Medium Ion Implanter	Source doping
	P-type, B+, 10keV, 3E14, Tilt 7	
140	CMOS PR ASHER	
	PR ashing O2 plasma	
150	WET STATION WA-2 SPM PR STRIP	
	PR strip	
160	PR TRACK	
	PR coating, develop	
170	NIKON STEPPER	Drain pattern (open)
	Active photo [Reticle : NSD]	
180	Medium Ion Implanter	Drain doping
	N-type, As+, 10keV, 3E14, Tilt 7	
190	CMOS PR ASHER	
	PR ashing O2 plasma	
200	WET STATION WA-2 SPM PR STRIP	
	PR strip	
210	RTA	Dopant activation
	Dopant activation, 900C, 10sec, N2 100 sccm	

Seq. No	*Process Name*	*Process Specification*
220	W13A(WA-13,C1-6)SPM-CLEANING	
	predep. cleaning	
230	W5A(WA-5,C1-6) SC-1,2 CLEANING	
	RCA cleaning, HF dip	
240	HfO2 depposition	Gate dielectric deposition
	50A +/-5%, thk. check ellipsometer & C-V measurement	
250	TiN Dep,(CMOS,Endura system)	Gate deposition
	Gate layer TiN depo 1500A	
260	PR TRACK	
	PR coating, develop	
270	NIKON STEPPER	Gate pattern
	Active photo [Reticle : PSD]	
280	P-5000 Metal ETCH	Gate etch
	Gate etch 1500A target, thk. check a-step & SEM	
290	CMOS PR ASHER	
	PR ashing O2 plasma	
300	WET STATION WS-10 Solvent PR STRIP	Cleaning PR residual
	PR strip	
310	P5000 TEOS DEPOSITION	ILD deposition
	ILD SiO2 4000A +/-10%, thk. at ellipsometer	
320	PR TRACK	
	PR coating, develop	
330	NIKON STEPPER	Contact hole pattern
	Contact photo [Reticle : CNT]	
340	P5000 SIO/SIN ETCH	Contact etch
	Contact etch 4000A target 20% over.	
350	CMOS PR ASHER	
	PR ashing O2 plasma	
360	WET STATION WS-10 Solvent PR STRIP	Cleaning PR residual
	PR strip	
370	WET STATION WA-1 CLEANING(BHF 50:1)	
	Pre metal cleaning, 20sec	
380	Ti Dep,(CMOS,Endura system)	Contact gap fill
	Adhision metal Ti depo 300A	
390	TiN Dep,(CMOS,Endura system)	
	Barrier metal TiN depo 300A	
400	Al Dep,(CMOS,Endura system)	
	Al depo 4000A, No void check at CD-SEM	
410	TiN Dep,(CMOS,Endura system)	AR coating
	AR metal TiN depo 300A	
420	PR TRACK	
	PR coating, develop	

Seq. No	*Process Name*	*Process Specification*
430	NIKON STEPPER	Metal pad pattern
	MT(Metal) photo [Reticle : metal]	
450	P5000 AL ETCH	Pad etch
	MT etch 4900A target 30% over, remain ILD THK check	
460	CMOS PR ASHER	
	PR ashing O2 plasma	
470	WET STATION(WS10C.C1-2) PR STRIP	
	PR solvent strip	

Process flow for the proposed TFETs

Seq-No	*Process Name*	*Process Specification*
10	LASER MARKER	SOI wafer and bulk wafer (test)
	Marking wafer number in backside	
20	W13A(WA-13,C1-6)SPM-CLEANING	
	Initial cleaning	
30	W5A(WA-5,C1-6) SC-1,2 CLEANING	
	RCA cleaning, HF dip	
40	CMOS FURNACE II - DRY OXIDATION	Buffer oxidation for LOCOS
	Oxidation for thinning 100A +/-5% Thickness checked by ellipsometer	
50	LPCVD III CMOS SiNx	SiNx doposition
	SiNx depo 1000A +/-10%, THK at nanospec	
60	PR TRACK	
	PR coating, develop	
70	NIKON STEPPER	Active layer pattern
	Active photo [Reticle : ACT]	
80	P5000-IV SIO/SIN ETCH	SiNx etch
	SiNx etch 1000A just etch, E/R check	
90	CMOS PR ASHER	
	PR ashing	
100	WET STATION WA-2 SPM PR STRIP	
	PR strip	
110	W13A(WA-13,C1-6)SPM-CLEANING	
	Initial cleaning	
120	W5A(WA-5,C1-6) SC-1,2 CLEANING	
	RCA cleaning, HF dip	
130	CMOS FURNACE II - WET OXIDATION	LOCOS oxidation
	Oxidation for thinning 4000A +/-10% Thickness checked by ellipsometer	
140	WET STATION WA-2 SiNx STRIP	SiNx etch
	SiNx strip, Hf dip	
150	Epitaxy	p-i-n layers epi
160	P5000 4호기 TEOS DEPOSITION	Hard mask dep
	ILD TEOS dep 1000A +/-10%, T17 THK ellipso	
170	PR TRACK	
	PR coating, develop	
180	NIKON STEPPER	Active layer pattern
	Active photo [Reticle : ACT]	
190	P5000-IV SIO/SIN ETCH	Hard mask etch
	Spacer SiO2 etch 1000A just etch, E/R check	
200	CMOS ICP POLY ETCHER	Active etch
	Trench etch 3200A +/-10%, E/R check a-step and **SEM**	

210	CMOS PR ASHER	
	PR ashing	
220	WET STATION WA-2 SPM PR STRIP	
	PR strip	
230	W13A(WA-13,C1-6)SPM-CLEANING	
	Pre gate dielectric dep. cleaning, HF dip	
240	W5A(WA-5,C1-6) SC-1,2 CLEANING	
	RCA cleaning, HF dip	
250	HfO2 dep	
	5 nm, checked by ellipso	
260	TiN Dep,(CMOS,Endura system)	
	Gate metal TiN depo 1500A	
270	PR TRACK	
	PR coating, develop	
280	NIKON STEPPER	Gate patten
	MT1(Metal1) photo [Reticle : metal1]	
290	P5000-Ⅲ ETCH	Gate etch
	Gate etch 1500A target 10% over	
300	P5000-Ⅲ PR ASHING	
	PR ashing	
310	WET STATION(WS10C.C1-2) PR STRIP	
	PR solvent strip	
320	P5000 4호기 TEOS DEPOSITION	ILD dep.
	ILD TEOS dep 4000A +/-10%, T17 THK ellipso	
330	PR TRACK	
	PR coating, develop	
340	NIKON STEPPER	Contact hole pattern
	Source photo [Reticle : CNT]	
350	P5000-IV SIO/SIN ETCH	Contact etch
	Spacer SiO2 etch 4000A just etch, E/R check	
360	CMOS PR ASHER	
	PR ashing	
370	WET STATION WA-2 SPM PR STRIP	
	PR strip	
380	W1A 50:1BHF CLEANING metal	
	Pre metal cleaning	
390	Ti Dep,(CMOS,Endura system)	Contact gap fill
	Barrier metal Ti depo 300A	
400	TiN Dep,(CMOS,Endura system)	
	Barrier metal TiN depo 300A	

410	Al Dep,(CMOS,Endura system)	
	Al depo 4000A	
420	TiN Dep,(CMOS,Endura system)	AR coating
	AR metal TiN depo 300A	
430	PR TRACK	
	PR coating, develop	
440	NIKON STEPPER	Metal pad pattern
	MT1(Metal1) photo [Reticle : metal1]	
450	P5000-III AL ETCH	
	MT1 etch 4900A target 30% over, remain ILD THK check	
460	P5000-III PR ASHING	
	PR ashing	
470	WET STATION(WS10C.C1-2) PR STRIP	
	PR solvent strip	

Chapter 5

Conclusion

5.1 Summary of Contributions

Before fabricating the proposed device, Si and SiGe TFETs with the planar structure are fabricated firstly and then, measured to extract model parameter. From the measured results, the parameters of band-to-band tunnel (BTBT) model is calibrated that can accurately simulate the tunnel phenomena. From theses data, the calibrated model is based on the real tunnel effect in the device and the proposed device can be predicted including reality. Finally, the proposed TFETs are fabricated on a bulk Si substrate. For the fabrication of the proposed TFETs with improved performance, the vertical structure, reliable gate dielectric with EOT < 1.7 nm, and metal gate are implemented. Moreover, using a novel perpendicular tunnel direction to the channel can be fabricated. For the fabrication of the devices, additional processes such as NH_3 plasma

treatment, are developed. Detailed electrical characterization for the proposed TFETs showed a steep subthreshold swing (SS) at the low current with an operating voltage window of 0.7 V. The proposed structure implemented a tunnel direction perpendicular to the channel. By this perpendicular tunnel direction which is formed by SEG process, the tunnel width is limited. SEG processes are most likely to make a very thin layer tunnel near the source/channel interface. The fabricated TFETs show 17 mV/dec minimum subthreshold swing (SS) and 10^4 ON/OFF current ratio (I_{ON}/I_{OFF}) for sub-0.7 V gate overdrive. In addition, SS is maintained less than 60 mV/dec while the drain current increases from the complete OFF-state (10^{-13}) to more than two orders of magnitude (10^{-11}).

5.2 Future works for TFETs Design

This paper shows that the proposed TFETs have been proved to be by experiments and measured data. However, many technical issue still need to be solved for further upgrade of TFETs performance. Thus, remaining issues are to be discussed here. First, one of the most important obstacles for implementing the high performance TFETs is the small current drivability. Although the proposed devices are aimed to be used at low-power circumstance, the current drivability of the proposed device is 10 times smaller than that of the state of the art TFETs. By optimizing physical dimensions and adopting materials which can adjust band-gap in the source, the current drivability is expected to

improve.

Secondly, the modeling of fabricated TFETs should be addressed. Most of the device simulations based on Kane's BTBT models use simple empirical equations for calculation. In the BTBT model, only adapting numerically parameters, this approach does not contain energy state which has dependency on carrier tunnel.

Finally, as the first aim of this work, after achieving the successful co-integration of TFETs and MOSFETs, new design will be investigated on MOSFETs/TFETs hybrid circuits for energy- efficiency considering D.C and A.C operation.

Chapter 6

Appendix

6.1 Super-linear onset in TFETs

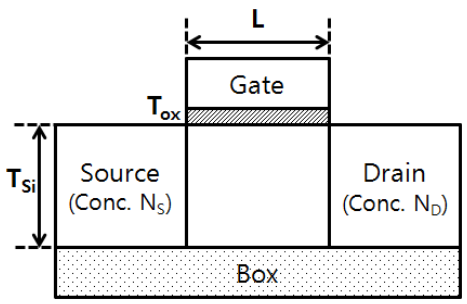
This chapter investigates the super-linear onset phenomenon in TFETs. The particular phenomenon of TFETs has been a critical issue in output characteristics. In the previous chapter, the super-linear onset of TFETs was detected in operations. In order to confirm the cause of super-linear onset, Technology Computer-Aided Design (TCAD) simulations were performed with various biases, source doping profiles and band-gap engineering. As the result, it is revealed that the super-linear onset is increased by fixed surface potential at particular situations. Additionally, the simulation shows that TFETs with abrupt source junction or SiGe source have reduced super-linear onset. It is found that the large tunnel current between source and channel is expected to reduce the super-linear onset.

6.2 Introduction

In the previous chapter, the planar TFETs were fabricated and measured. Although the fabrication of TFETs shows a degraded performance which does not satisfy industrial demands, these devices are possible to implement the analysis for unique characteristics of TFETs. In the measured results and reported results in any other papers, TFETs cannot still solve the current reduction problem in output characteristics at a low V_D, although TFETs typically show a good performance such as steep SS and high on-current. This phenomenon is defined as a super-linear onset. The property of super-linear onset can cause a problem at a low V_D due to the dramatically decreased current. It means that the low tunnel current significantly degrades the performance of TFET circuits such as rising/falling delay due to poor current drivability at small V_D. In this chapter, the super-linear onset is investigated in output curves of TFETs. In order to confirm the effects of super-linear onset, TCAD simulations were performed with various bias conditions, doping profile and source material modulation. The relation between V_D and V_G and their influences on the tunnel current are investigated. Additionally, the effect of tunnel resistance is also verified by modulating doping profile and band-gap engineering.

6.3 Device Structure

Fig. 6.1 illustrates the cross-sectional view of the simulated TFETs. The simulation is performed by Sentaurus Device 2014. 07 simulator. All the simulated



Parameter	Value
V_D	1.0 V
T_{Si}	30 nm
L	100 nm
W	1 μm
T_{ox}	1 nm
N_D	n-type 10^{20} cm^{-3}
N_I	p-type 10^{15} cm^{-3}
N_S	p-type 10^{20} cm^{-3}

Figure 6.1 Schematic cross view of TFET devices. The parameter which is used in the simulation are summarized in table.

devices have the planar structure. The devices have Si body thickness of 30 nm, and the physical gate length/active length of 100 nm. Source and drain doping of 1 x $10^{20} cm^{-3}$ with opposite doping types, and p-type body doping of 1 x $10^{15} cm^{-3}$ are used The specifications are summarized in Fig. 6.1. Non-local band to band tunnel model are used throughout the simulations for higher accuracy. The simulator automatically determines the tunnel path from the very beginning.

6.4 Simulation Results

The output characteristics of the TFETs are first studied as shown in Fig. 6.2(a). The various gate biases from 0.5 V to 1.0 V with 0.1 V of step are applied respectively. In contrast with the characteristics in MOSFETs, the super-linear onset is observable only in TFETs. The simulation result indicates this

in that super-linear onset is definitely shown when 1.0 V is applied to the gate. Conversely, when the small gate bias is applied, the super-linear onset cannot be observed. If the large gate bias is applied, a very small drain bias needs to be applied to observe the super-linear onset. In order to verify this specifically, the output curves are normalized in Fig. 6.2(b). With the gate bias increased, the super-linear onset is observed clearly.

For confirming the cause of super-linear onset in TFETs, firstly, gate bias and drain bias are applied simultaneously to verify current limitation (Fig.3.3). The difference of potential between gate bias and drain bias is maintained 1.0 V among gate bias sweeping (V_{GD} = 1.0 V). As a control group, the drain bias is fixed at 1.0 V among gate bias sweeping (V_{SD} = 1.0V). The simulation results are shown in the Fig. 6.3. At the case of V_{GD} = 1.0 V, the tunnel current increases exponentially. As the result shows, the source can supply enough current exponentially to the channel if the potential is enough to modulate the channel surface potential. This is because the potential gap between gate and drain is maintained as a 1.0 V. However, at the case of V_{SD} = 1.0 V, the transfer curve shows that tunnel current saturates as gate bias increases. Such phenomenon has been analyzed by many other papers [32]-[34]. The current saturation is originated from channel inversion by drain. In order to confirm the cause of current rigorously, the gate to drain capacitance (C_{GD}) is simulated with various drain bias in Fig. 6.4(a). As higher drain bias is applied, C_{GD} increases at more positive gate voltages due to the increase in the channel

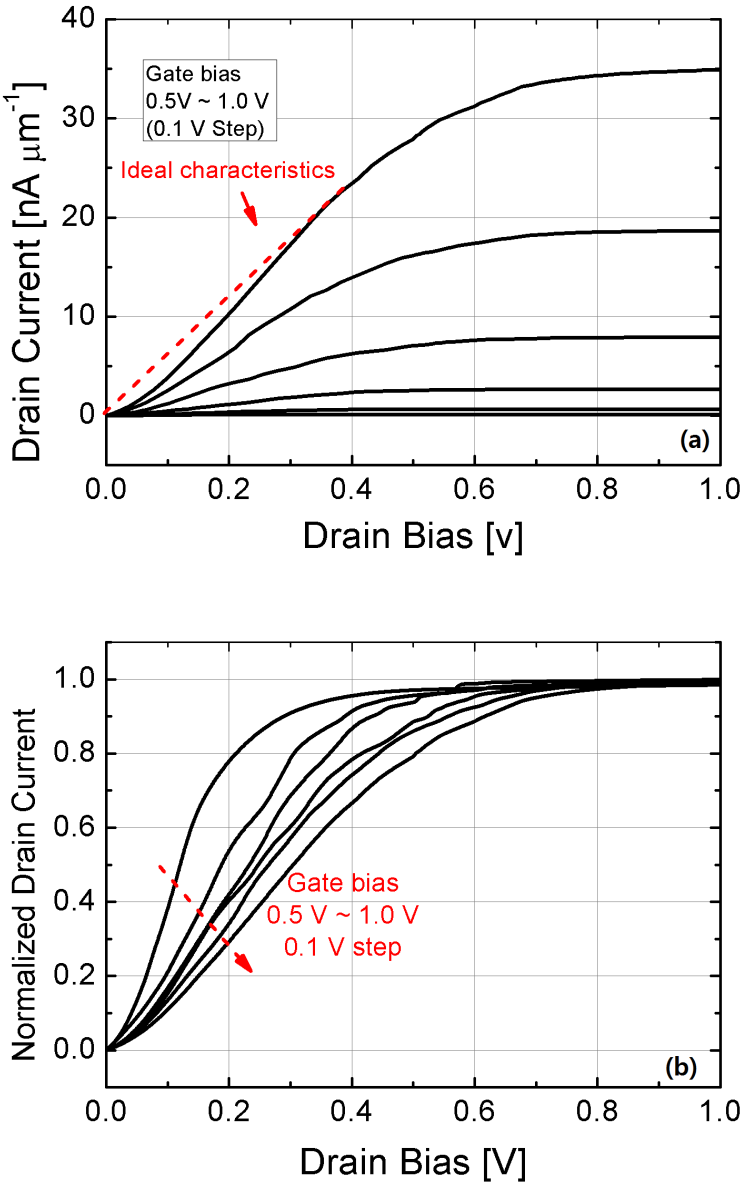


Figure 6.2 (a) Output characteristics in TFETs. The gate bias is applied from 0.5 V to 1.0 V. The super-linear onset is verified in the region of small drain bias. (b) Normalized output characteristics in TFETs.

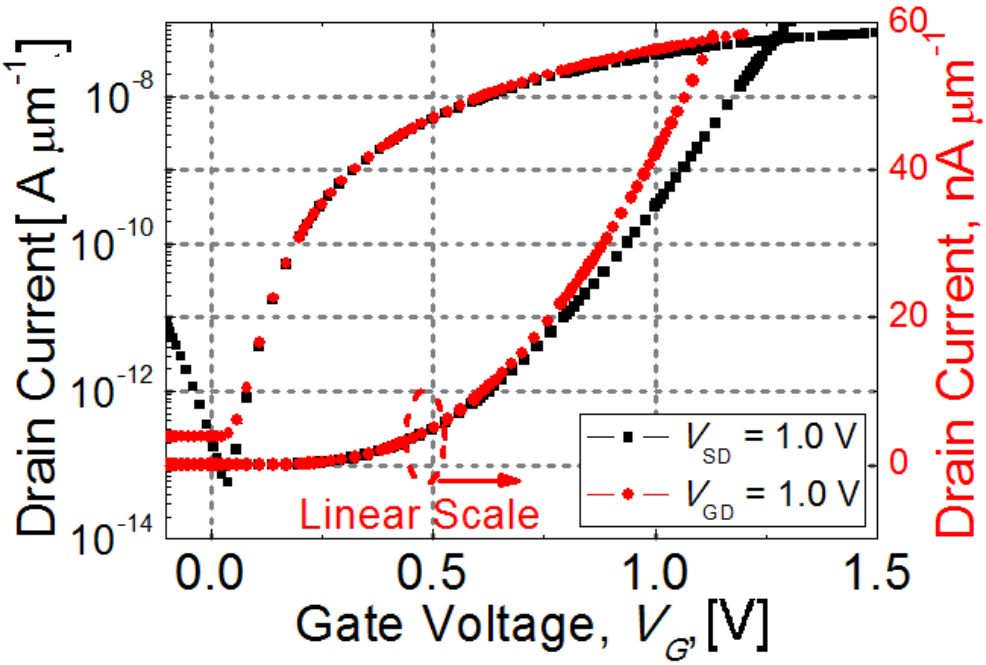


Figure 6.3 Transfer curves in TFETs. The tunnel current is saturated at V_{SD} = 1.0 V due to the channel inversion.

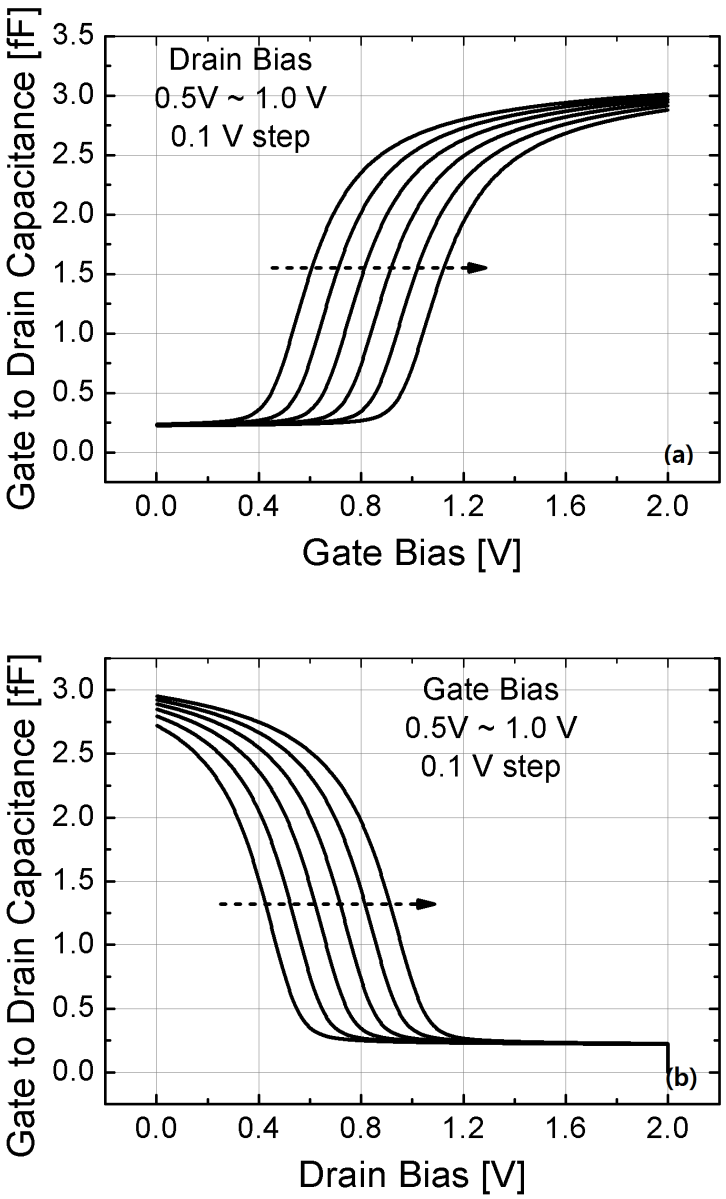


Figure 6.4 Capacitance–voltage characteristics showing gate-to-drain (C_{GD}) capacitances as a function of (a) V_{GS} (b) V_{DS}.

to drain side potential barrier. The reason is that at the lower drain bias, there is lower band-bending in the channel-drain, which implies a small barrier of the drain-to-channel. The channel inversion starts at this point and C_{GD} starts to increase. The results reveal that saturation of tunnel current has been explained as the surface potential fixes up the tunnel current even though the gate bias is modulated. In summary, the simulation results show a simple relationship between tunnel current and applied biases in TFETs. The tunnel current from the source to the channel gets slightly increased as a function of V_{DS} because of the fixed channel surface potential. The super-linear onset in output curves is explained in a similar way. In order to confirm the cause of super-linear onset, the gate to drain capacitance (C_{GD}) is simulated with various gate biases in Fig. 6.4(b). According to the results, the increasing drain voltage means that the impact of tunnel resistance is reduced. This is because channel inversion is reduced as C_{GD} decreases. When high gate bias is applied with a relatively low drain voltage, a channel inversion occurs by the carrier injection from the drain. After the channel inversion, surface potential in the channel is not modulated proportionally to the gate bias by the inversion charges. Thus, the tunnel current from the source to the channel gets slightly increased as a function of V_{DS} because of fixed channel surface potential (Fig. 6.5). Consequently, the super-linear onset is originated from the low tunnel current regardless of the V_G modulation under the particular V_G and V_D conditions.

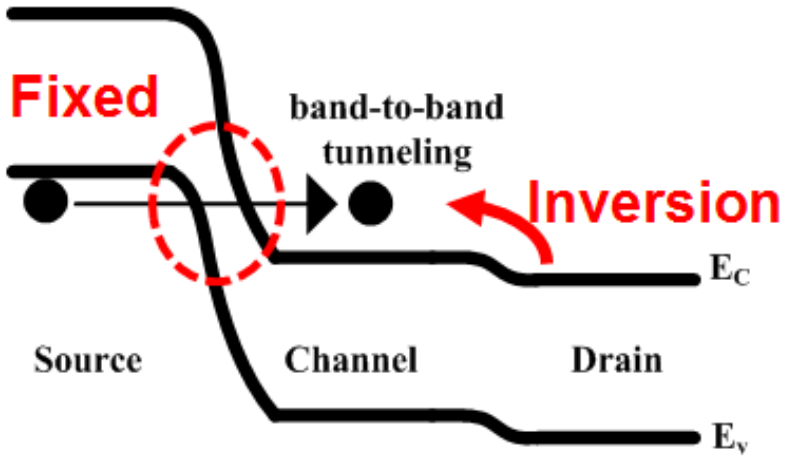


Figure 6.5 Energy band diagram when applying high gate bias and low drain bias.

6.5 Drain Threshold Voltage

In the previous section, it is demonstrated that the super-linear onset is originated from the inversion charges. Before analyzing the super-linear onset, the degree of super-linear onset should be defined rigorously. The TFETs have two threshold voltages that are gate threshold voltage and drain threshold voltage. The output characteristics show nonlinear curves due to the drain bias dependence. Therefore, in order to define transfer characteristics of TFETs, the second threshold voltage needs to be defined, which is named V_{TD}, in terms of the drain voltage. The derivatives of output characteristics are shown in Fig. 6.6(a). The various gate biases from 0.5 V to 1.0 V are applied respectively. At the maximum of $dI_D/\mathrm{d}V_{DS}$, the drain threshold voltage is extracted. In the

ideal output curve, there is no drain dependency. If the super-linear onset is not observed, the V_{TD} would not be observed, either. Thus, the V_{TD} is decreased with the reduction of super-linear onset. Fig. 6.6(b) depicts V_{TD} in terms of gate bias. The results show that the V_{TD} is increased with respect to the gate bias. Therefore, the degree of super-liner onset is detected by V_{TD} reasonably.

6.6 Tunnel Resistance

In many papers, the super-linear onset has been reported in TFETs. These studies assume that the tunnel probability is set 1. It means that the tunnel resistance are set 0. However in the real device, the tunnel probability cannot be ideal value. Therefore, the dependency on the tunnel resistance should be studied. In the previous section, it is concluded that the super-linear onset is originated from low tunnel current of the V_G modulation under the particular V_G and V_D conditions. Moreover, the degree of super-linear onset is defined rigorously in terms of V_{TD}. In order to confirm the relation of super-linear property and tunnel resistance, the doping profile to the source side needs to be changed. In Fig. 6.7(a), only the source region modulates the doping profile. Consequently, a source with abrupt doping profile makes a small tunnel resistance and increases the tunnel current by reducing energy band gap (Fig. 6.7(b)). By using this method, the tunnel current from the source is adjusted to increase. In the Fig. 6.8, the output characteristics of the TFETs are plotted with various doping profile. In the simulation results, there are various current

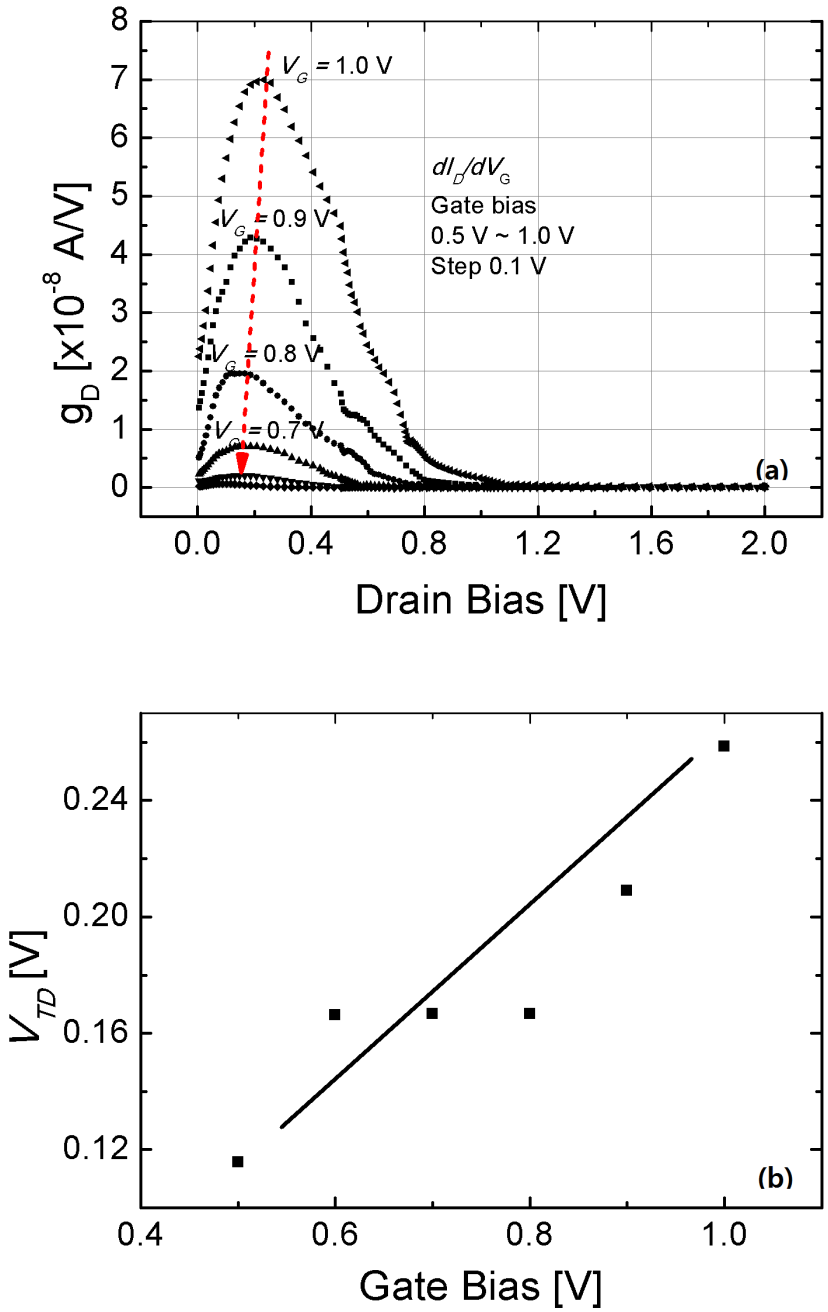


Figure 6.6 (a) $dI_D/\mathrm{d}V_{DS}$ (g_D) as a function of V_D for various V_Gs. (b) Threshold voltage in terms of V_{DS}.

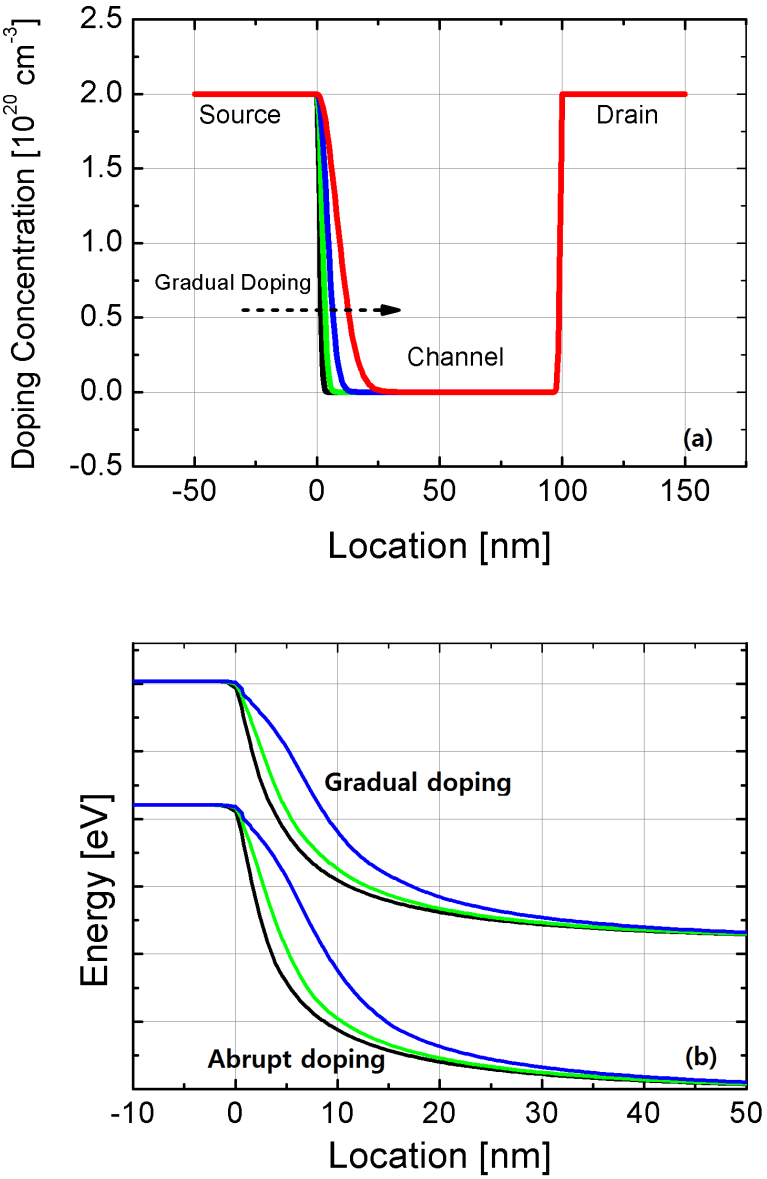


Figure 6.7 (a) Doping profile. only source region modulates the doping profile. (b) energy band diagram. A source with abrupt doping profile makes a small tunnel resistance.

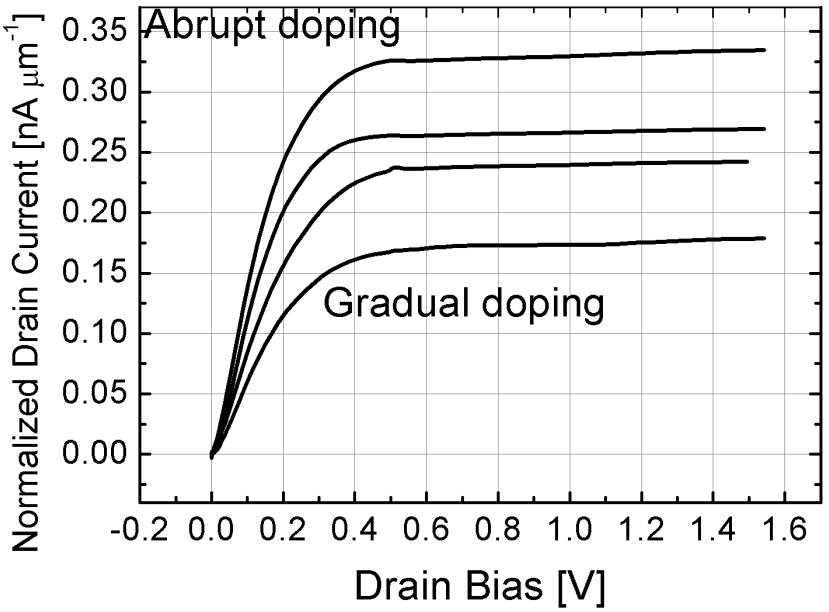


Figure 6.8 Output characteristics in TFET for different doping profile.

levels due to the source doping profile. The derivatives of output characteristics are shown in Fig. 6.9(a). At the maximum of dI_D/dV_{DS}, the drain threshold voltage is extracted (Fig. 6.9(b)). This result means that the super-linear onset is due to the low tunnel current at the particular situations of high gate bias and low drain bias. The super-linear onset can be easily controlled with the tunnel current modulation. Consequently, this problem of super-linear onset can be decreased by enhancing the current drivability. In order to confirm the relation between super-linear onset and current drivability, the Ge contents in the source region are changed additionally. The content of Ge is adjusted in the

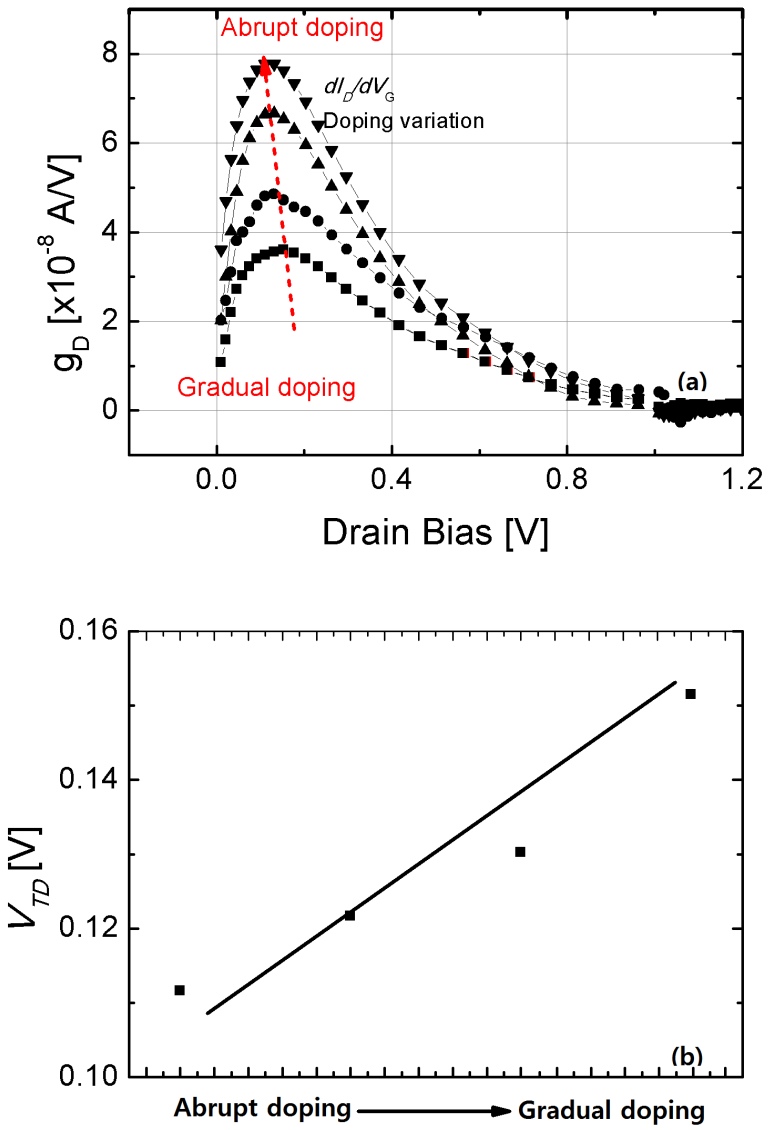


Figure 6.9 (a) dI_D/dV_{DS} (g_D) as a function of V_D for various doping profile. (b) Threshold voltage in terms of V_{DS}.

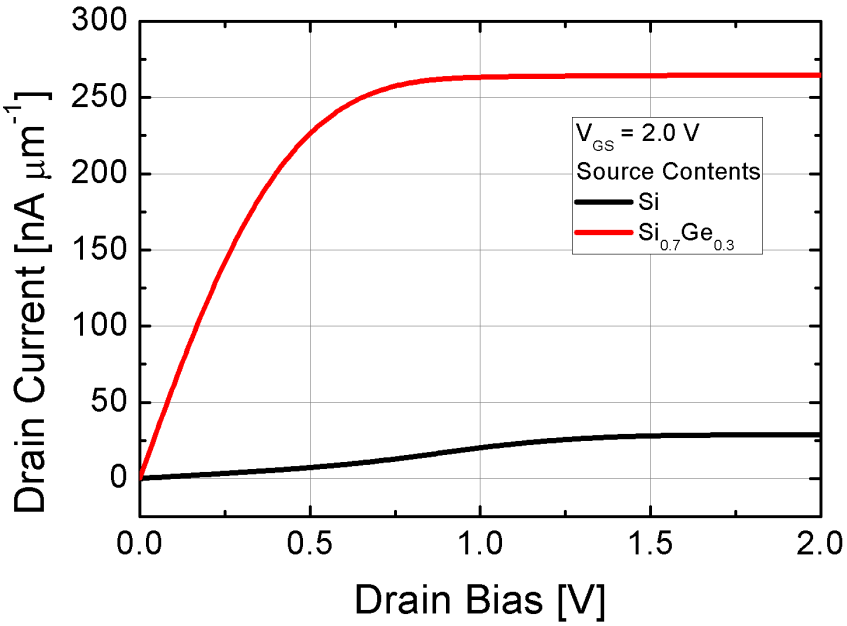


Figure 6.10 Output characteristics of TFETs with Si or SiGe source. The device with $Si_{0.7}Ge_{0.3}$ source do not show super-linear onset.

source. In Fig. 6.10, only the Ge contents in the source region are modulated from 0% to 30%. Consequently, a source with high Ge contents makes a small tunnel resistance and increases tunnel current by reducing energy band gap. By using this method, the tunnel current from the source is also intentionally increased. As a result, Fig. 6.10 indicates that the super-linear onset is not observed in TFETs with the hetero-junction source. To obtain more specific results, the V_{TD} is extracted by the current derivative as shown in Fig. 6.11(a) and (b). In Fig. 6.11(a), the peak of transconductance is not observed and the

V_{TD} is located near zero voltage in the TFETs with 30% of Ge source. This result means that the super-linear onset occur from the low tunnel current at high gate bias and low drain bias. Moreover, this phenomenon can be solved by enhancing the current drivability. The super-linear onset can be reduced with the hetero-junction technique.

6.7 Conclusion

The super-linear onset is studied in the output curves which have been detected in TFETs operations. By performing TCAD simulations, the physical origin of the super-linear onset is analyzed rigorously. As a result, it is clearly revealed that the super-linear onset occurs by fixed surface potential at the particular V_G and V_D conditions. The situations are high gate and low drain biases where the channel surface is filled with the inversion charges from the drain. The super-linear onset is due to the low tunnel current at particular situations which are high gate bias and low drain bias. However, enhancing the tunnel current in the source by making abrupt junction would be a solution for reducing super-linear property.

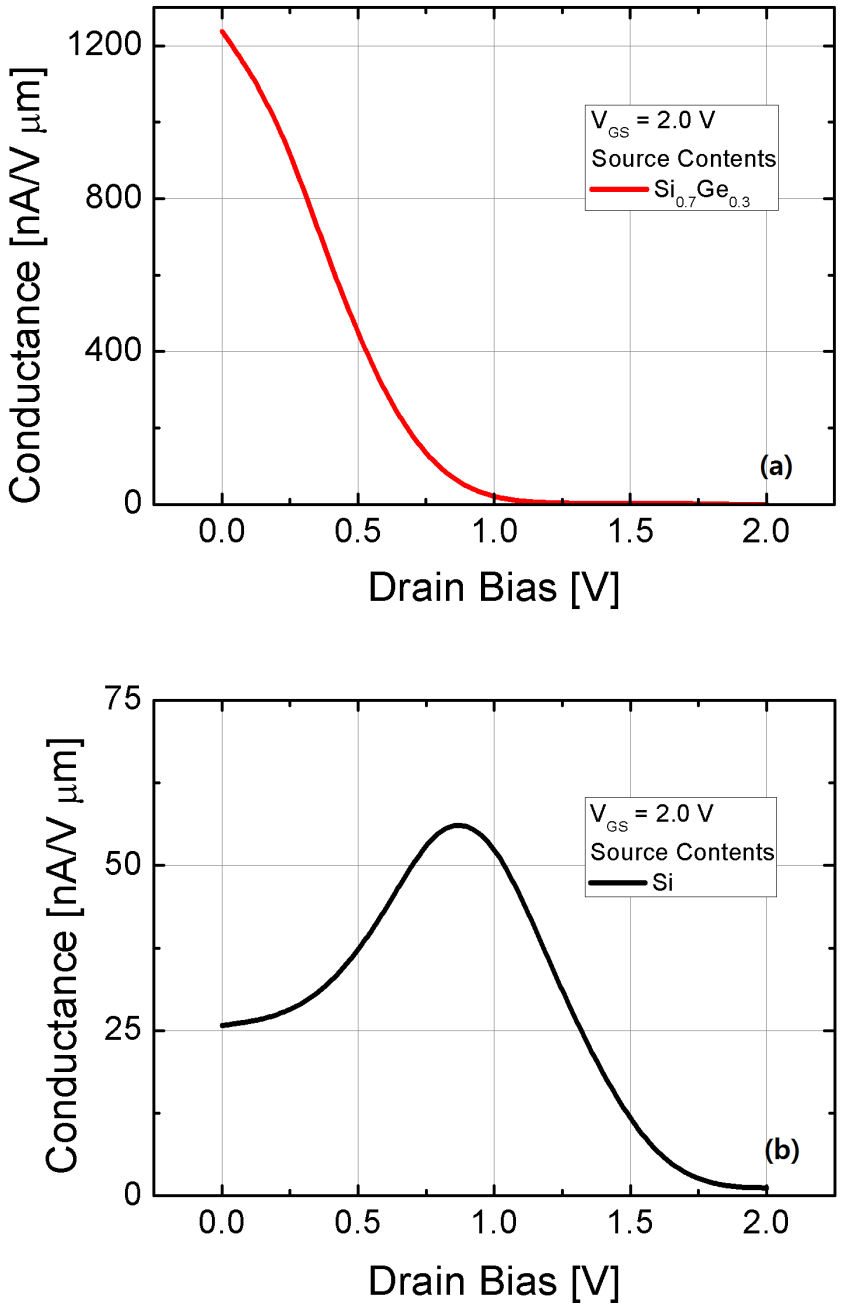


Figure 6.11 dI_D/dV_{DS} (g_D) as a function of V_D by Ge contents (a) $Si_{0.7}Ge_{0.3}$ source (b) Si source.

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초록

고집적 상보형 전계효과 트랜지스터 (CMOS) 기술로 만들어진 집적회로에서 단위 면적당 전력소비는 반드시 줄여야 되는 중대한 문제로 인식하고 있다. 이러한 문제를 해결하기 위하여 본 논문에서는 새로운 구조의 터널 전계 효과 트랜지스터를 제안하고 제작하였다. 제안된 소자는 수직형 구조를 기반으로 얇은 터널장벽을 가지고 있기 때문에 높은 전기적 성능을 보이고 벌크 Si에서 제작할 수 있는 장점이 있다.

제작에 앞서 먼저 Si과 SiGe source를 가지는 TFET의 특성을 확인해보기 위해 기준이 되는 소자제작을 하였고 그 특성을 측정하였으며 측정된 결과를 통해서 시뮬레이션에서 사용하는 band-to-band tunnel model의 parameter를 계산하여 model에 적용하였다. 사용된 시뮬레이션 프로그램은 Synopsys의 Sentaurus를 사용하였다.

위의 시뮬레이션으로 집적된 데이터를 기반으로 새로운 구조의 소자를 제안하게 되었다. 새로운 구조의 소자는 벌크 Si위에서 제작이 가능하도록 vertical 구조를 바탕으로 설계되었으며, source 영역의 옆에 수직형 터널영역을 첨가하여 높은 구동전류와 낮은 SS 특성을 보이게 된다. 또한 source 옆, 즉 수직방향으로 tunnel 전류가 형성되므로 source의 높이에 따라 구동전류를 높일 수 있는 장점을 가지고 있다. 이러한 구조를 시뮬레이션으로 통하여 확인하였으며, 이 구조의 단점으로 수직형 tunnel과 수평형 tunnel 전류가 양립하여 발생하는 hump 현상을 발견하였고 간단한 gradual doping층을 삽입하여 해결하였다.

마지막으로 실제 제안된 소자를 제작하였으며 제안된 소자는 얇은 터널 장벽을 가지는 수직형 이중게이트 터널 전계효과 트랜지스터로 명명하였다. 제작된 소자를 측정을 통하여 전기적 성질을 확인하였으며, 제작된 소자는 17 mV/dec의 SS와 10^4 수준의 ON/OFF 특성을 나타냄을 확인하였다. 결론적으로 제안된 소자는 우수한 전기적 특성을 보이며, 향후 다음 세대의 낮은전력에서 동작하는 소자로 차세대 소자들 가운데 유력한 소자가 될 것이다.

주요어: band-to-band tunnel, 터널 전계효과 트랜지스터, 수직형 구조, TFET, low power device, 수직형 tunnel, subthreshold swing, current drivability, Si substrate

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