Ph.D. Dissertation

An AC-DC LED Driver with a Two Parallel Floating Buck Topology for Reducing the Light Flicker in Lighting Applications to Low-Risk Levels

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by

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August, 2016

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An AC-DC LED Driver with a Two Parallel Floating Buck Topology for Reducing the Light Flicker in Lighting Applications to Low-Risk Levels

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An AC-DC LED Driver with a Two Parallel Floating Buck Topology for Reducing the Light Flicker in Lighting Applications to Low-Risk Levels

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Abstract

This dissertation presents an ac-dc LED driver that consists of two parallel floating buck converters. To buffer the twice-line-frequency energy, one floating buck converter conveys energy to a storage capacitor, simultaneously performing the power factor correction (PFC). The other floating buck converter regulates the LED current to maintain a constant brightness in the LEDs for reducing the light flicker to low-risk levels. The proposed architecture reduces the voltage stress and the size of the storage capacitor, enabling the use of a film capacitor instead of an electrolytic capacitor. Considering the power factor and the flicker standards, a design procedure to achieve a high power factor, while minimizing the storage capacitance and the LED current ripple, is presented. A prototype of the proposed LED driver has been implemented with an on-chip controller IC fabricated in a 0.35 μm CMOS process and its functionality and performance have been verified experimentally. It demonstrates a power factor of 0.94 and a peak power efficiency of 85.4% with an LED current ripple of 6.5%, while delivering 15 W to the LEDs.

Keywords: AC-DC power conversion, Light-emitting diodes (LEDs), LED driver, Analog and digital integrated circuit design, Pulse width modulated power converters, flicker, floating buck converter

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Chapter 1

Introduction

1.1 Motivations

Light-emitting diodes (LEDs) have been replacing traditional light sources like incandescent and fluorescent lamps in many lighting applications because LEDs have a wide color gamut, a high luminous efficacy, a long lifetime, and are environment friendly [1]–[4]. Although the first white LEDs were commercially introduced in the mid-1990s, they were not used widely because they were inefficient light sources at that time. Their luminous efficacy was much lower than other lighting technologies. Luminous efficacy, which has the unit of lumens per watt, represents lighting efficiency of light sources. However, the rapid development in LED technology is driving major changes in the lighting industry to keep up with the pace. Fig.1.1 shows the dramatic improvement in the efficacy of LEDs, as compared with other traditional light sources [5].

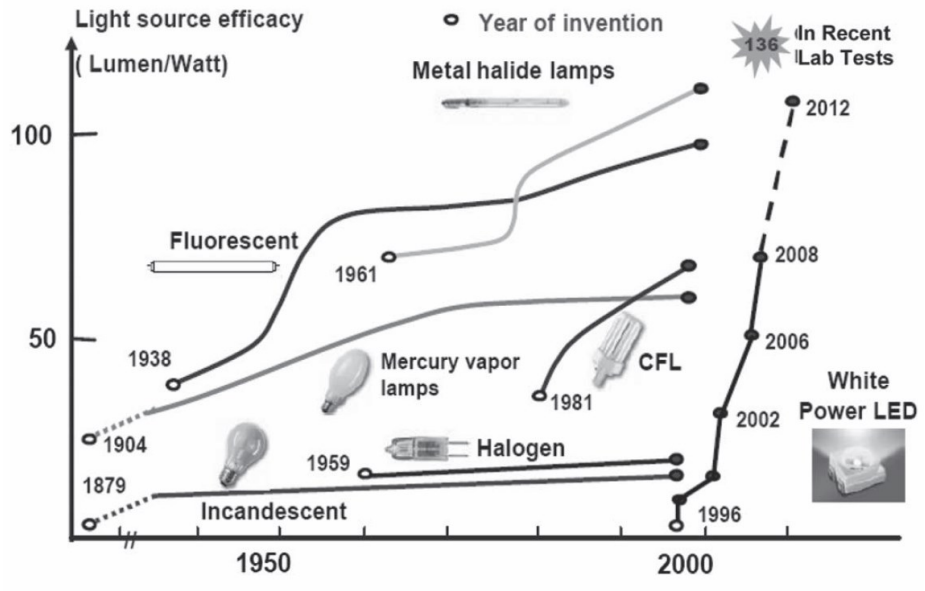


Fig. 1.1. Advancement in lighting technology [5].

The characteristics of LEDs are very sensitive to process and temperature. Fig. 1.2 (a) indicates LED has asymmetric V-I characteristics, and Fig. 1.2 (b) shows that the luminous flux is proportional to LED currents, which means the brightness of LEDs are controlled by its forward current [6]. Due to these characteristics, driving LEDs with a fixed output voltage cannot guarantee constant brightness of LEDs. Therefore, most LED drivers must regulate the currents flowing through the LED load for achieving constant luminous intensity.

Most state-of-the-art LED drivers utilizing an off-line ac voltage source employ power factor correction (PFC) circuits to comply with standards like the IEC61000-3-2 [7] and the ENERGY STAR [8], which specifies that the power factor should be higher than 0.9 for commercial applications and 0.7 for residential applications. To

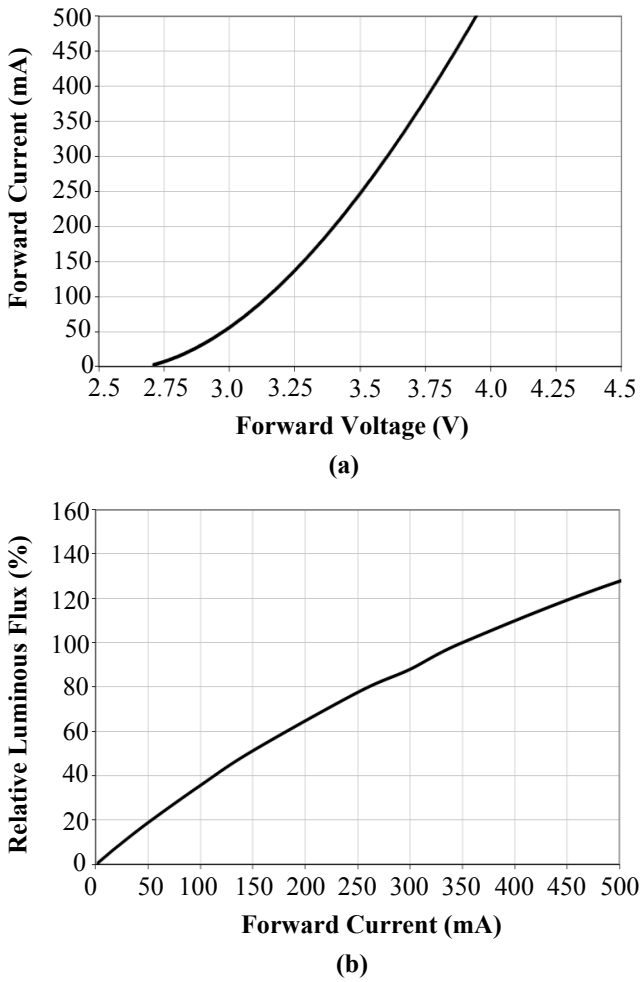


Fig. 1.2. LED characteristics: (a) Electrical characteristics (b) Relative luminous flux versus forward current [6].

meet these requirements, conventional single-stage LED drivers with PFC circuits that reduced the number of discrete components using simple structures with reduced costs and small form factors, were reported in [9]–[11].

However, the single-stage LED drivers [9]-[11] depicted in Fig. 1.3 exhibit light

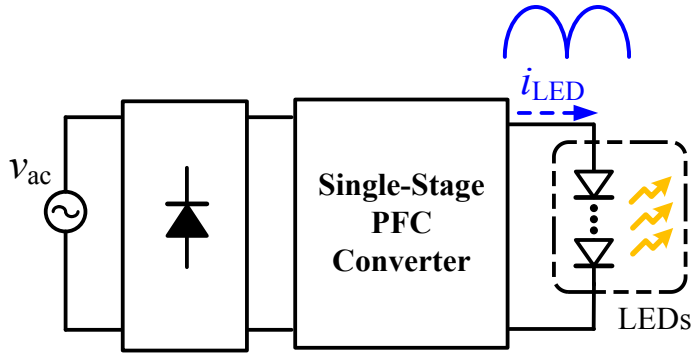


Fig. 1.3. Conventional single-stage LED drivers that exhibits light flicker.

flicker that varies at twice the ac line frequency because they mainly focus on the PFC function only and therefore have a large LED current ripple. Flicker means a rapid and repeated change over time in the brightness of light. Although light flicker at frequencies above 70 Hz is typically invisible to most people, it may induce harmful biological effects including headache, fatigue, eyestrain, and even epileptic seizures [12], [13]. Thus, the goal of this dissertation is to design an ac-dc LED driver that can achieve acceptable power factor and reduce light flicker to low-risk levels to mitigate the harmful biological effects.

1.2 Flicker Metrics and Standards

According to [14], there are two common ways to measure flicker, the Flicker Index and the Percent Flicker. With reference to Fig. 1.4, the Flicker Index and Percent Flicker, which is also known as Modulation (%), can be expressed as

$$\text{Flicker Index} = \frac{Area1}{Area1 + Area2} \tag{1.1}$$

$$\text{Percent Flicker} = 100 \times \frac{L_{MAX} - L_{MIN}}{L_{MAX} + L_{MIN}}. \tag{1.2}$$

Although the Flicker Index is mathematically able to explain differences in shape or duty cycle, the Percent Flicker is preferr ed to calculate flickers because it needs only the measurement of maximum and minimum values, whereas calculating the Flicker Index requires the accurate sampling of complex waveforms for integral. Fig.

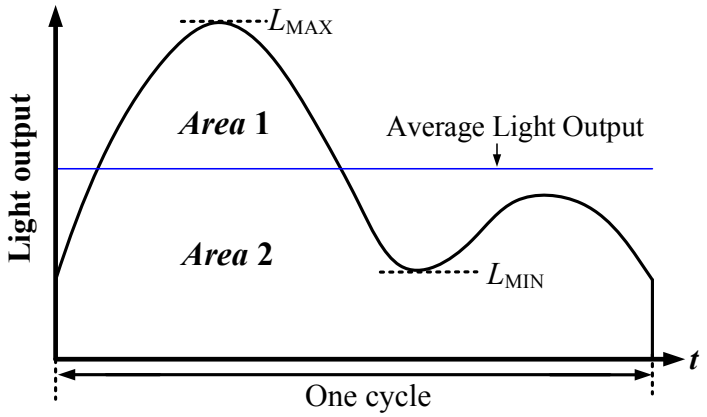


Fig. 1.4. Periodic waveform of light output in one cycle [14].

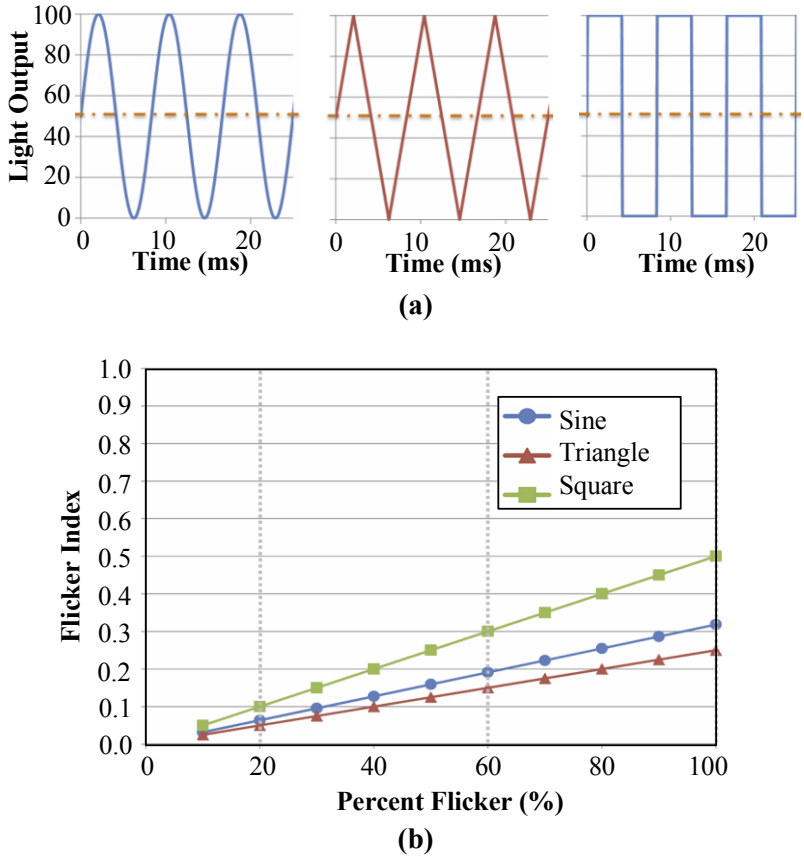


Fig. 1.5. (a) Simple periodic waveforms of light outputs (b) Flicker Index versus Percent Flicker [15].

1.5 shows the dependency between Flicker index and Percent Flicker about the three types of simple periodic waveforms: sine, triangle, and square (50% duty cycle) waveforms. Triangle waveforms always have the lowest Flicker Index when those three kinds of waveforms have the same Percent Flicker. By using this relation, calculating. By using the graph in Fig. 1.5 (b), Flicker Index can be obtained when knowing the shape of the output light waveforms and the values of Percent Flicker

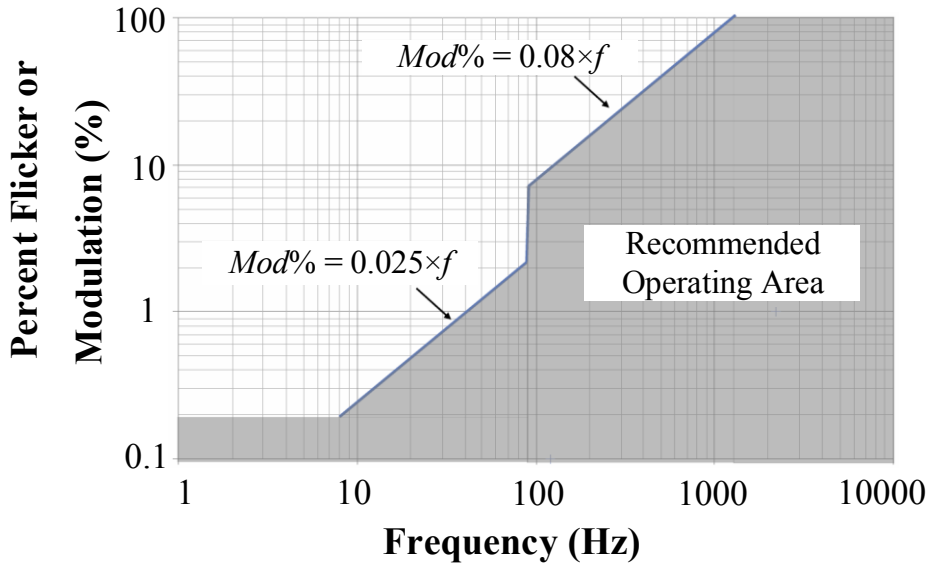


Fig. 1.6. Recommended operating area to give low risk for headaches and photosensitive epileptic seizures [17].

[25].

Studies in [13] and [14] indicate the permissible flicker in terms of the Flicker Index or the Percent Flicker by collecting experimental data from previous flicker studies. The IEEE standard 1789-2015 in [15] provides the recommended practices for modulating current in high-brightness LEDs. According to [13] and [15], in LED lighting applications with flicker frequencies above 90 Hz, Percent Flicker for low-risk level should satisfy the following:

$$\text{Percent Flicker}\left(=\text{Mod}\%\right) < 0.08 \times f_{\text{FLICKER}} \tag{1.3}$$

where f_{FLICKER} is the frequency of the flickering light. Fig. 1.6 depicts the recommended operating area to limit the biological effects. For example, a Percent Flicker

of less than 9.6% is acceptable if f_{FLICKER} is 120 Hz. The relationship between the Percent Flicker and the Flicker Index is discussed in [14], where the recommended Flicker Index is:

$$\text{Flicker Index} \leq 0.1 \ (f_{\mathrm{FLICKER}} = 100\ \mathrm{Hz}). \tag{1.4}$$

A Flicker Index of 0.1 is equivalent to a Percent Flicker of 20% and 30% for a square and sinusoidal light output, respectively. Thus, considering aforementioned standards about the power factor and flicker, the objective of this dissertation is to design an ac-dc LED driver that can achieve a power factor higher than 0.9 and a Percent Flicker less than 9.6% at 120 Hz.

1.3 Prior Works

Fig. 1.7 depicts the waveforms of an ac-dc LED driver with a constant output power, when the input power factor is unity. The input power (P_{in}) at twice the line frequency has a pulsating waveform that periodically changes above or below the

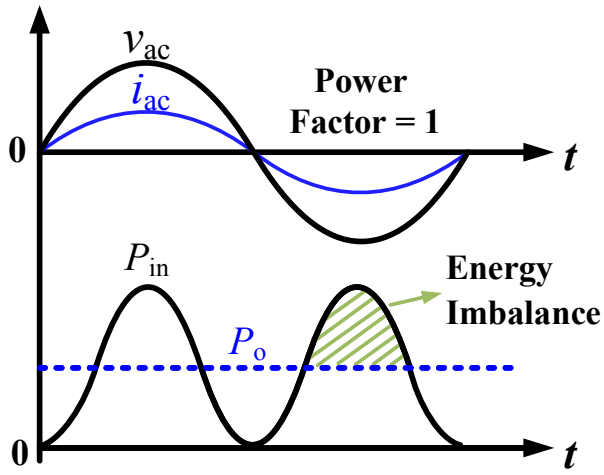


Fig. 1.7. Waveforms of an ac-dc LED driver with a constant output power when the power factor is unity.

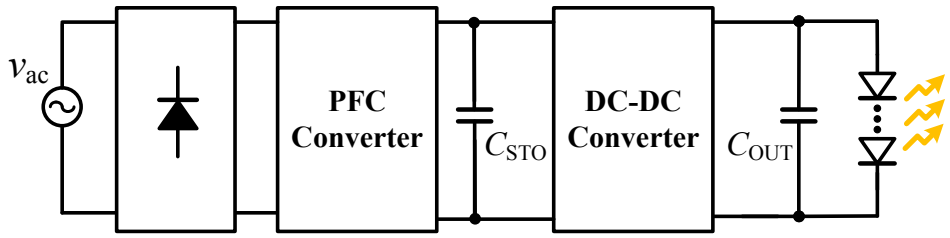


Fig. 1.8. Conventional two-stage ac-dc LED driver consisting of a first-stage PFC converter and a second-stage DC-DC converter.

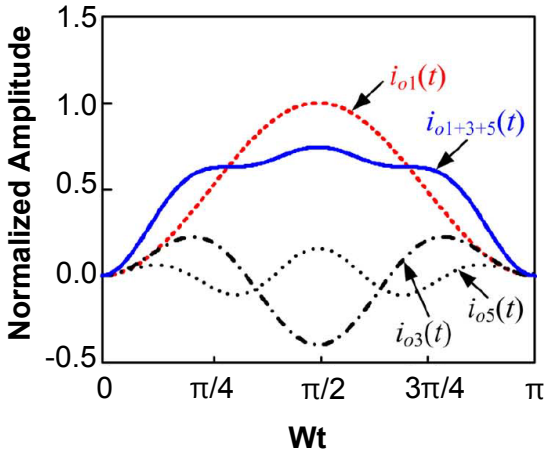


Fig. 1.9. Waveforms of output current when harmonic currents are injected to the input current [24].

constant output power (P_o). Hence, a storage capacitor as an energy buffer is required to balance out the instantaneous power differences between P_{in} and P_o. Fig. 1.8 illustrates the architecture of a conventional two-stage ac-dc LED driver with a storage capacitor (C_{STO}) [18]–[21]. Although this approach offers a near unity power factor and a precisely regulated output voltage, it would be generally more difficult to achieve a high conversion efficiency with the two-stage architecture unless an optimized control in each stage is applied, although efficiencies up to 95% have been reported. Further, this architecture requires several components relatively, resulting in large sizes and considerable costs [22]–[24].

To achieve a high power factor and reduce the output LED current ripple, several methods have been proposed [23]–[39]. The first approach is to inject odd harmonic signals like the third and the fifth harmonics [24]–[26] or the third harmonic only

[27], [28] to the input current for reducing the input current pulsation, sacrificing the input power factor down to 0.9. Fig. 1.9 represents the waveform of the output current when the third and fifth harmonics are injected to the ac line frequency [24]. While the previous studies in [24], [25], and [27] show a reduction in the size of the capacitors, recent studies in [26] and [28] consider the output light flicker characteristics. Although this approach enables the single-stage architecture without the use of C_{STO}, the study in [26] requires a large output capacitor of 500 μF for the output power of 20 W to ensure a Percent Flicker less than 40%.

The second approach is to employ a parallel [23], [29]–[32] or a series [33]–[37] ripple cancellation converter (RCC). In [23] and [29]–[32], as illustrated in Fig. 1.10, a bidirectional converter is used as an active power filter and is placed in parallel with the LED load that is directly connected to the PFC stage, for controlling the LED current ripple. While this method can achieve a dc LED current and significantly reduce the size of the output and storage capacitors, approximately 32% of the output power is converted three times before it is delivered to the output, incurring a power loss [33]–[35]. In [33]–[37], on the other hand, the output of the RCC is connected in series with the output of the PFC stage, and the LED load is connected in parallel with the two series-connected output capacitors, which is depicted in Fig 1.11. The series RCC topology can provide a higher power efficiency than the parallel RCC topology because it further reduces the proportion of the output power converted more than once. In [33] and [34], for example, 90% of the output power is directly delivered by the PFC stage, while 10% of the output power is converted twice before being delivered to the output.

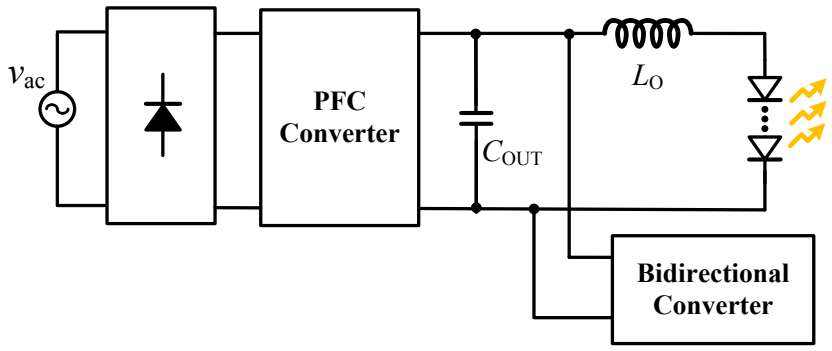


Fig. 1.10. An ac-dc LED driver employing a parallel ripple cancellation converter [30].

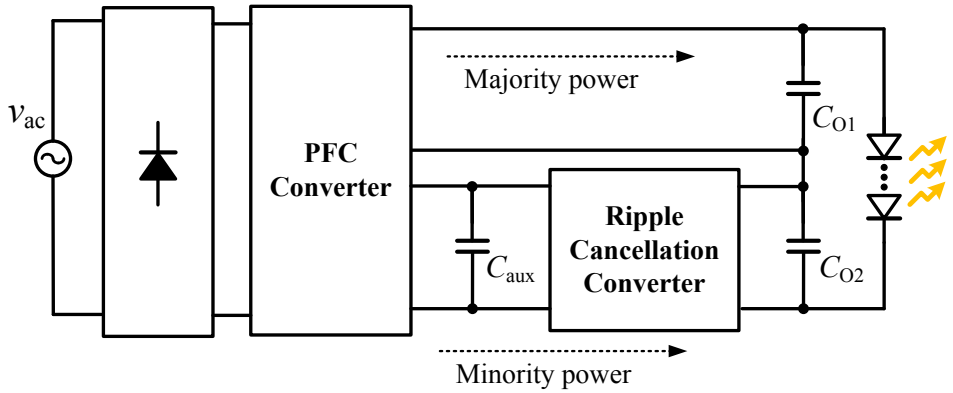


Fig. 1.11. An ac-dc LED driver employing a series ripple cancellation converter [35].

Another approach with an ac-dc power conversion architecture consisting of two stacked energy-storage capacitors across the rectifier output and two floating resonant buck converters, is proposed in [38] and depicted in Fig. 1.12. Although the stacked architecture needs an additional power combing converter composed of a switched capacitor circuit, this architecture is suitable for high-frequency operations

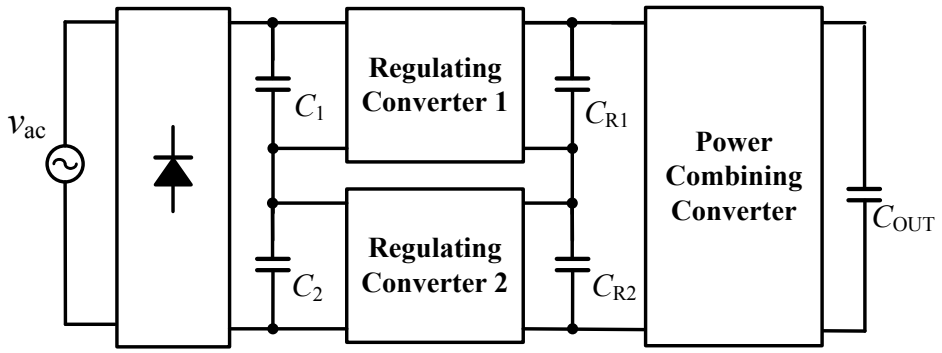


Fig. 1.12. An ac-dc power conversion architecture consisting of two stacked energy-storage capacitors [38].

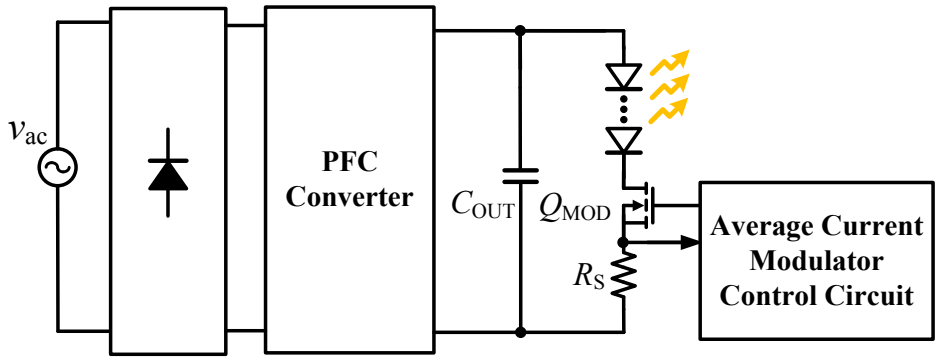


Fig. 1.13. A single-stage ac-dc LED driver employing an average current modulation method [39].

at 3-10 MHz, enabling the use of two 0.8 μH inductors for an LED power of 30 W. An average current modulation method for a single-stage LED driver is proposed in [39]. As illustrated in Fig. 1.13, the LED load is connected in series with a modulation switch, for pulsed current driving. To achieve a constant average level of the LED current in each modulation cycle, the duty cycle of the switch is controlled ac-

cording to the pulsating output voltage level. In [40], an ac-dc converter with a parallel PFC scheme is proposed. An isolated full-bridge boost converter is employed for the main power stage where 68% of the input power is directly delivered to the output, and the remaining 32% of the power is stored in a storage capacitor. A forward converter is placed in parallel with the boost converter and is used for the auxiliary power stage that provides the necessary power for dc output power by using the storage capacitor as its input source. Although only 32% of the power must be processed twice before being delivered to the output, this architecture requires two isolation transformers that are relatively complex and expensive.

1.4 Thesis Objectives and Organization

This dissertation proposes an ac-dc LED driver consisting of two parallel floating buck converters for reducing the light flicker to low-risk levels. To handle the power differences between the twice-line-frequency input power and the constant LED power, one floating buck converter conveys energy from the ac source to a storage capacitor, simultaneously performing the PFC operation. The other floating buck converter supplies constant current to the LEDs to maintain a constant brightness. The proposed architecture can achieve an input power factor higher than 0.9. Although the proposed approach offers a lower power factor than the conventional two-stage approach with a boost PFC converter [18]–[21], the proposed architecture with two floating buck converters in parallel significantly reduces the average voltage of C_{STO} to 56.5 V at the input voltage of 110 V_{rms}, whereas the average voltage of C_{STO} in the two-stage must be higher than 155 V. Moreover, the size of C_{STO} is reduced because less than 30% of the output power is initially stored in C_{STO} and then delivered to the LED load. Thus, the reduced voltage stress and size of C_{STO} enables ceramic or film capacitors to be utilized instead of electrolytic capacitors that have lifetime constraints.

In addition, the two floating buck converters have a low-side switch that reduces the design complexity of the gate driver circuit. Whereas the second approach employing an RCC [23], [29]–[37] requires a transformer or coupled inductor with several other components, the proposed architecture provides a low-cost solution and simple design for low-power LED lighting applications. The rest of the dissertation

is organized as follows: Chapter 2 introduces the background on LED drivers. Several power converter topologies and their characteristics are presented to help understand how power converters are employed in LED drivers. Configuration of LEDs and current sensing techniques used in LED drivers are introduced, and the active and passive PFC techniques are explained. Chapter 3 presents the system architecture and operation principle of the proposed LED driver. The design considerations for achieving a high power factor and efficiency is discussed, and the design procedure of the proposed LED driver is described. Moreover, circuit implementation and the simulation results of the controller IC are also presented. Chapter 4 presents the experimental results of the prototype LED driver, and Chapter 5 concludes this dissertation.

Chapter 2

Background on LED Driver

2.1 Power Converter Topologies

2.1.1 Linear Regulator

Linear voltage regulators illustrated in Fig. 2.1 are used for the dc-dc voltage conversion when the input voltage is higher than the output voltage. Here, the output voltage (V_{OUT}) can be expressed as $V_{OUT} = (1+R_1/R_2)\cdot V_{REF}$. Compared with other power converters utilizing passive energy storage elements such as inductors or capacitors, linear regulators have simple architecture and small form factor, enabling the integration with other circuits in a single chip. However, the power loss (P_{LOSS}) in the transistor M_1 increases linearly with the voltage difference between the input voltage (V_{IN}) and the output voltage (V_{OUT}) because the power loss can be expressed

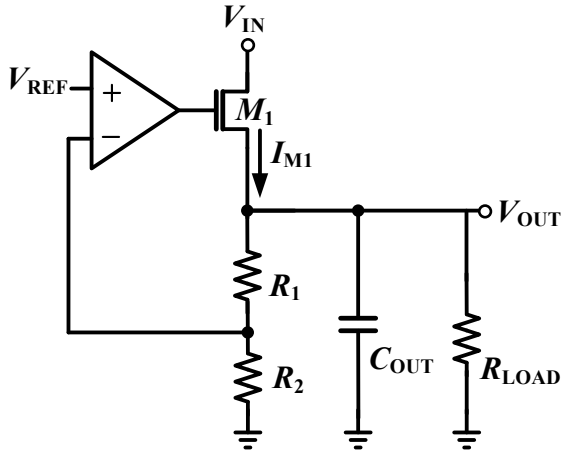


Fig. 2.1. Schematic of a linear voltage regulator.

as $P_{LOSS} = (V_{IN}-V_{OUT})\cdot I_{M1}$. Hence, it can be seen that linear voltage regulators are suitable only when the voltage difference between V_{IN} and V_{OUT} is small.

2.1.2 Switched-Capacitor Converter

Fig 2.2 illustrates a switched-capacitor (SC) converter with a Series-Parallel topology that is a two-phase system where switches turn on or off according to the number of phases, which changes the connection of the flying capacitors (C_1, C_2, and C_3) in series or parallel [41]. Hence, the ideal conversion ratio of the SC converter in Fig. 2.2 is 3 between the input voltage V_{IN} and the output voltage V_{OUT}, which can be expressed as $V_{OUT}=3V_{IN}$. In actual implementations, V_{OUT} is smaller than $3V_{IN}$ because of power losses such as conduction loss and switching loss. If the input and output ports are reversed in this topology, it can simply be transformed to a step-down voltage converter whose conversion ratio is 1/3.

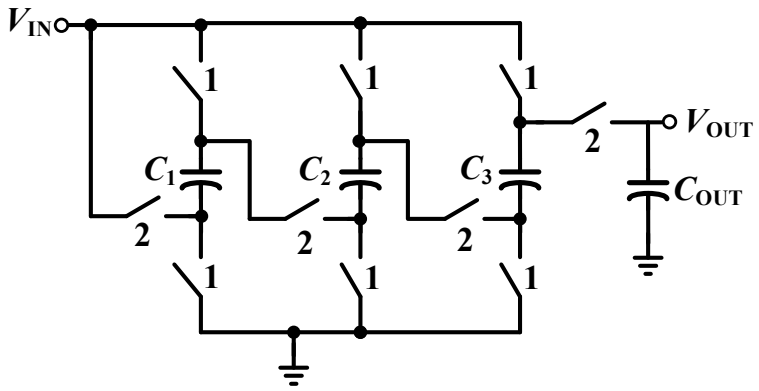


Fig. 2.2. A switched-capacitor converter with a series-parallel topology.

Compared to inductor-based converters like buck or boost converters where an inductor occupies a large portion of the area in a printed circuit board, SC converters can be implemented with smaller area and integrated in one chip when the flying capacitors have small capacitances less than few nF. However, the possible conversion ratio is only integer or fractional number because the number of capacitors and switches are finite in actual implementations. Consequently, SC converter is not suitable for an ac-dc converter that requires a continuous conversion ratio according to the ac input voltage level.

2.1.3 Inductor-Based Converters

Inductor-based converters utilize inductors as a main energy storage element to deliver power to the output load. They are divided into two categories, which are isolated and non-isolated converters. Non-isolated converters include the buck,

boost, and buck-boost converters, on the other hand, isolated converters include the flyback and forward converters. Isolated converter with a transformer operates without safety issues owing to the galvanic isolation, which has different ground levels for the primary side (input) and the secondary side (output). The galvanic isolation does not allow direct conduction path from input to output. In other words, unwanted current or voltage fluctuation from input does not affect the output. However, non-isolated converters are more attractive than isolated converters because non-isolated converters have advantages such as high efficiency due to simple structure and lower fabrication cost [6], [42].

2.1.3.1 Buck Converter (Floating buck Converter)

The buck converter and the floating buck converter shown in Figs 2.3 (a) and (b), respectively, are widely used as a voltage step-down converter. They consists of a power switch, an inductor, a diode, and a capacitor. In a synchronous buck converter, the diode D_1 can be replaced with another power switch to reduce the conduction loss due to the forward voltage drop on diode. The difference between the two converters is that the power switch M_1 is a high-side switch in the buck converter and a low-side switch in the floating buck converter. Because a hide-side switch requires a voltage bootstrapping circuit because the source of M_1 is not connected to the ground, the low-side driver can reduce the complexity of its gate driver. Although their architectures are different, their operation principle is same.

Fig. 2.3 (c) illustrates the voltage and current waveforms of the buck converter

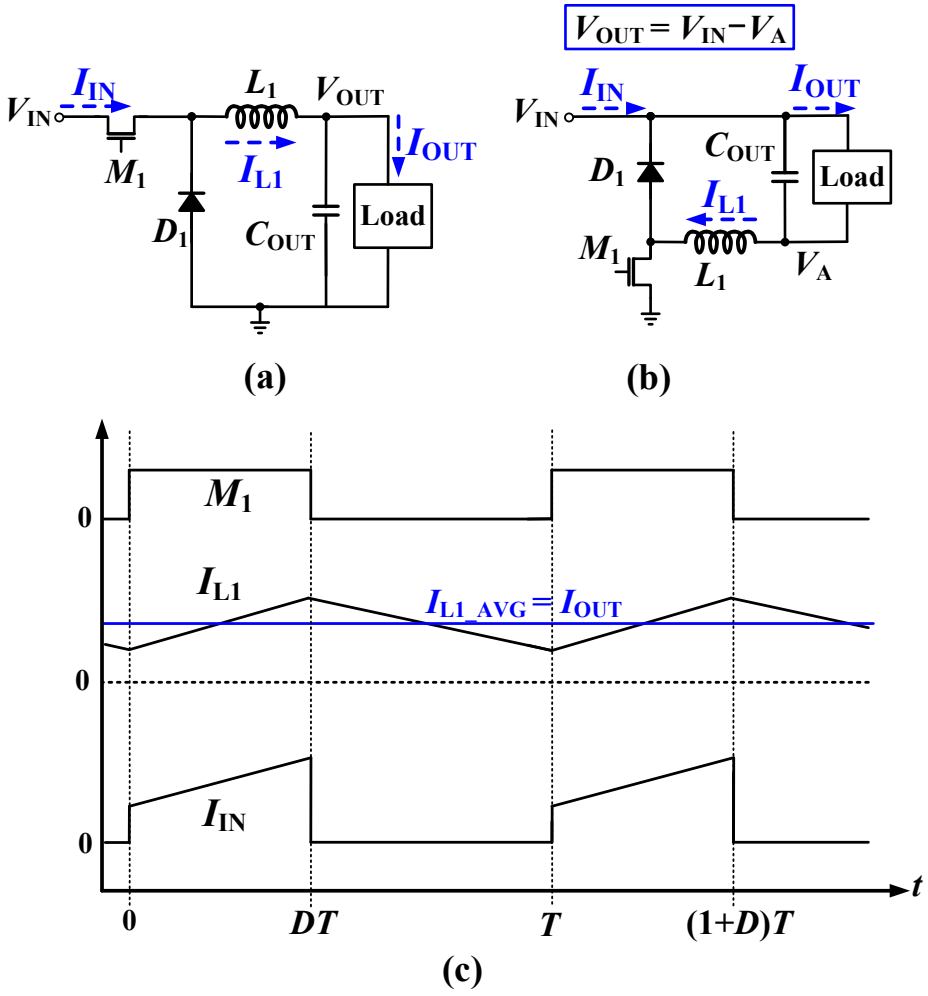


Fig. 2.3. Schematics of (a) a buck converter and (b) a floating buck converter, and the voltage and current waveforms of the buck converter in a CCM operation.

operating in CCM at steady-state. The conversion ratio $M(D)$ of the buck converter can be simply derived according to the three principles in [43], which are the inductor volt-second balance, the capacitor charge balance, and the small ripple approxi-

mation. It is assumed that the input voltage V_{IN} and the output voltage V_{OUT} are constant and there voltage ripples are negligible. Consequently, the inductor current is equal to the output current I_{OUT} and current slopes of the inductor current I_{L1} are constant. Therefore, by using $\Delta I_{L1}=0$ during one switching period, we can obtain following equations:

$$\Delta I_{L1} = \frac{(V_{IN} - V_{OUT})}{L_1} D + \frac{(-V_{OUT})}{L_1}(1 - DT) = 0 \tag{2.1}$$

By simplifying (2.1), we can get

$$DV_{IN} = V_{OUT} \tag{2.2}$$

$$M(D) = \frac{V_{OUT}}{V_{IN}} = D \tag{2.3}$$

If we assume the efficiency is 100%, we can derive (2.6) by inserting (2.2) into (2.5).

$$P_{IN} = P_{OUT} \tag{2.4}$$

$$V_{IN} I_{IN} = V_{OUT} I_{OUT} \tag{2.5}$$

$$I_{IN} = D I_{OUT} \tag{2.6}$$

Thus, the buck converter operates as a voltage step-down converter and a current step-up converter.

Buck converters have two operating modes according to the inductor current, which are continuous conduction mode (CCM) and discontinuous conduction mode (DCM), which is shown in Fig. 2.4. In some applications, the converter operates at the boundary condition, which is referred to as a critical conduction mode (CRM).

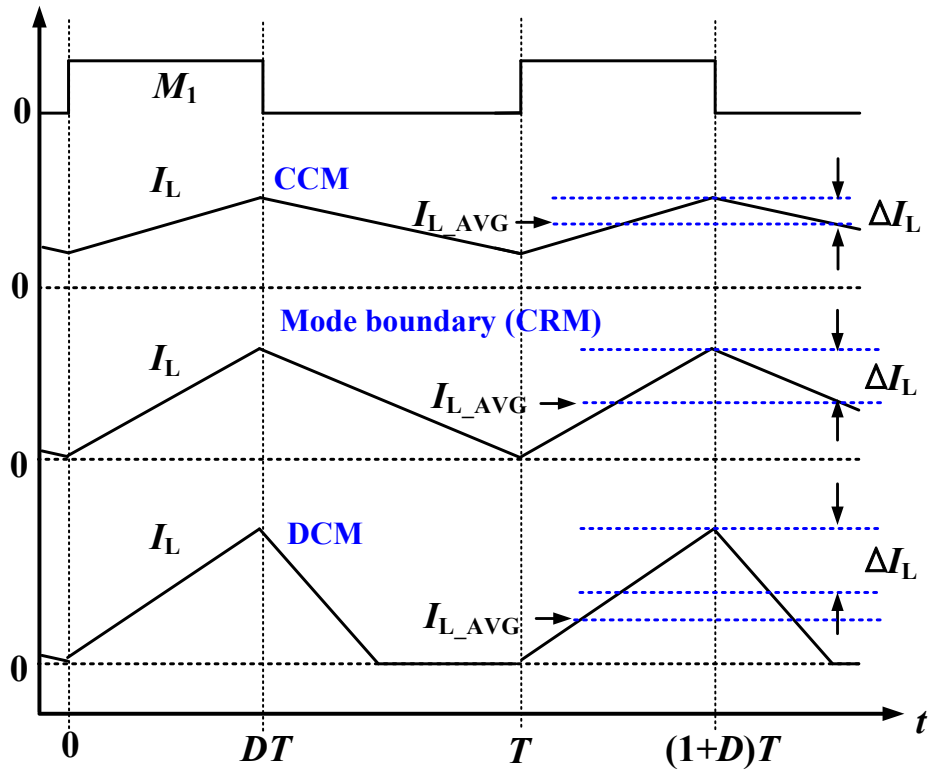


Fig. 2.4. Voltage and current waveforms illustrating the converter operation modes.

When the inductor current ripple ΔI_L is higher than average inductor current I_{L_AVG}, the converter operates in DCM. The boundary condition between CCM and DCM is $I_{L\_AVG} = \Delta I_L$. According to [44], the boundary condition K is defined as $K=2L/RT$, where R is the road resistance and T is the one switching period. If $K < (1-D)$, the buck converter operates in DCM. Otherwise, the buck converter operates in CCM.

It can be seen that there are three important design parameters (L, R, and T) to decide whether the buck converter operates in CCM or DCM. Typical examples of the DCM operation are as follows: the converter with large inductor; the converter

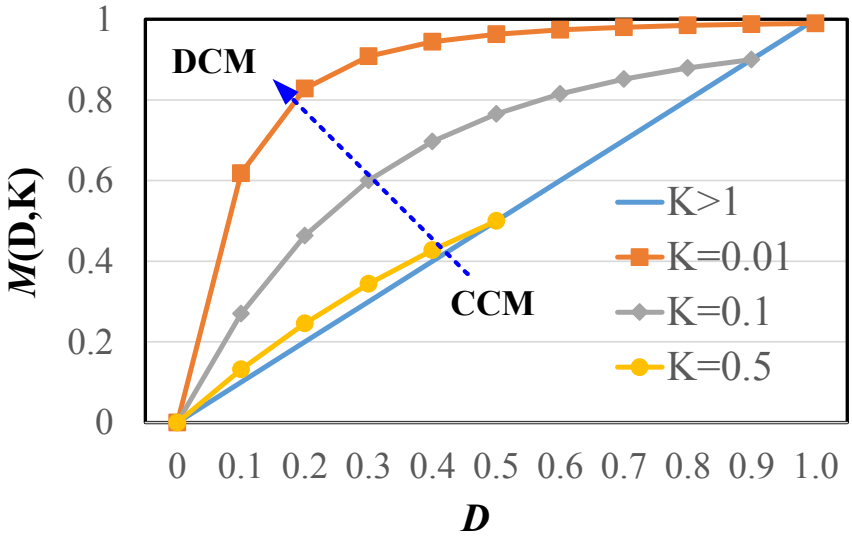


Fig. 2.5. Conversion ratios of the buck converter according to the boundary condition *K*.

operating at light load (small load current); the converter operating at low switching frequency. In DCM, the dynamics of converter change radically, and deriving the conversion ratio is not simple. Fig. 2.5 plots the conversion ratio versus the PWM duty cycle *D*, w here the conversion ratio *M(D,K)* can be expressed as [44]:

$$M(D,K) = D \qquad \text{(K > 1–D)} \qquad (2.7)$$

$$M(D,K) = \frac{2}{1+\sqrt{1+4K/D^2}} \qquad \text{(K < 1–D).} \qquad (2.8)$$

As the boundary condition *K* decreases, conversion ratio have more nonlinear curve. Therefore, the design parameters related to the boundary condition should be considered carefully when designing the buck converter.

2.1.3.2 Boost Converter

The boost converter depicted in Fig 2.6 (a) is a voltage step-up converter that the output voltage V_{OUT} is higher than the input voltage V_{IN} in a steady state. The boost converter has been widely used as a PFC converter because the input current is always continuous in CCM, which lead to higher power factor near unity than a buck

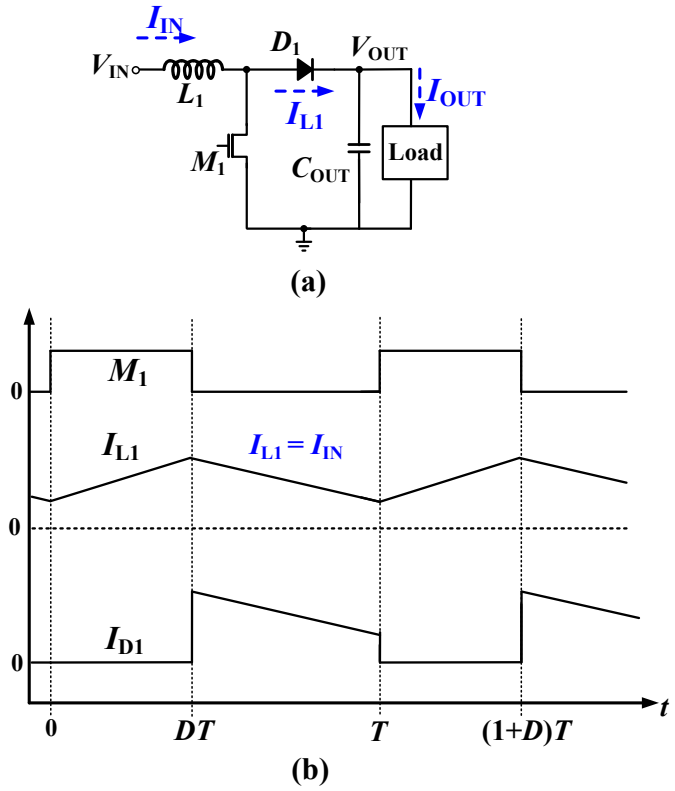


Fig. 2.6. Schematic of (a) a boost converter and (b) its voltage and current waveforms in a CCM.

converter whose input current is always discontinuous.

Fig 2.6(b) shows the voltage and current waveforms of the boost converter operating in CCM. Note that the input voltage and the output voltage is reversed in boost converter, as compared with the buck converter. When M_1 is on, the input current I_{IN} flows through M_1 and charges the inductor. When M_1 is off, the inductor is discharged, and the inductor current I_{L1} flows from the input to the output. Hence, the inductor current is always continuous, on the other hand, the current charging capacitor is discontinuous. With the same manner in the buck converter, the conversion ratio $M(D)$ of the boost converter can be derived as

$$\Delta I_{L1} = \frac{V_{IN}}{L_1} D + \frac{(V_{IN} - V_{OUT})}{L_1}(1 - DT) = 0 \tag{2.9}$$

$$M(D) = \frac{V_{OUT}}{V_{IN}} = \frac{1}{1-D}. \tag{2.10}$$

2.1.3.3 Buck-boost Converter

The buck-boost converter and floating buck-boost converter are illustrated in Figs. 2.7 (a) and (b). Like in the buck converter, the buck-boost converter has a high-side power switch M_1, hence, floating buck-boost is employed for the same reason. While the buck-boost converter has the negative output voltage, the floating buck-boost converter has positive output voltage. However, their operation principle is same. As shown in Fig 2.7 (c), when charging the inductor L_1, the input current I_{IN} flows through the power switch and the inductor, which is same with the boost con-

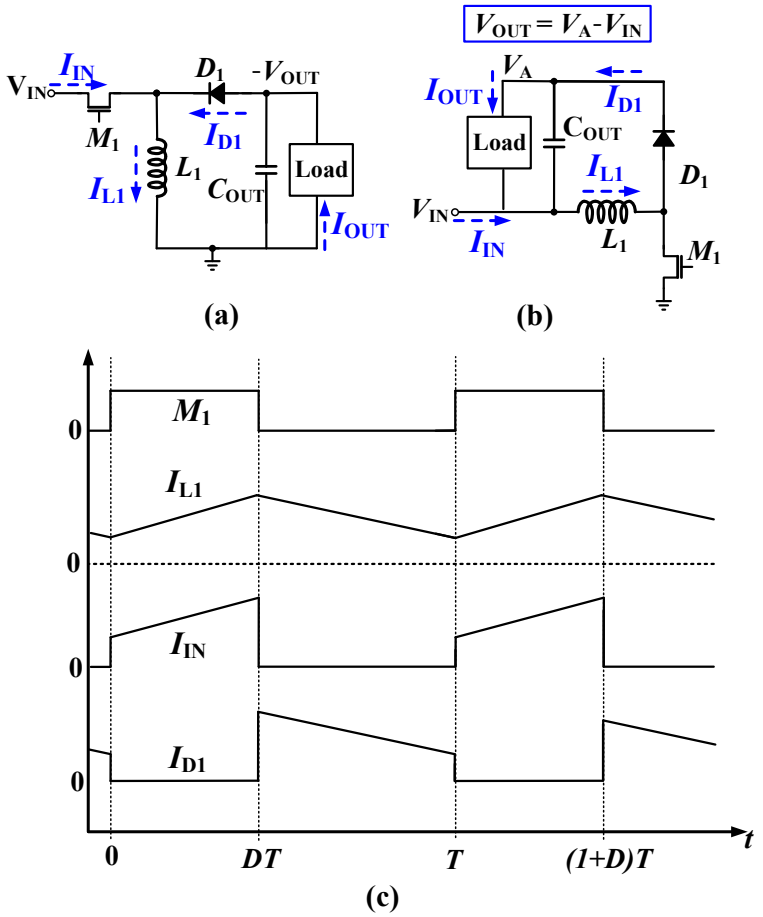


Fig. 2.7. Schematics of (a) a buck-boost converter and (b) floating buck-boost converter, and (c) their voltage and current waveforms in a CCM operation.

verter operation. On the other hand, when inductor current I_L is discharged, I_{L1} flows through the diode D_1 and the output capacitor C_{OUT}, which is same with the buck converter operation. Therefore, the buck-bo ost converter can be used as either a voltage step-up converter or a voltage step-down converter. The conversion ratio of the buck-boost converter covers the range combining the buck converter and the

boost converter. With the same way used before, the conversion ratio $M(D)$ of the buck-boost converter can be derived as

$$\Delta I_{L1} = \frac{V_{IN}}{L_1} D + \frac{(-V_{OUT})}{L_1}(1 - DT) = 0 \tag{2.11}$$

$$M(D) = \frac{V_{OUT}}{V_{IN}} = \frac{-D}{1-D}. \tag{2.12}$$

2.1.3.4 Flyback Converter

Among isolated converters, the flyback converter depicted in Fig 2.8 (a) is the most popular topology in both ac-dc and dc-dc applications. The flyback converter uses coupled inductors as a transformer network. The basic operation of the flyback converter is similar with the buck-boost converter, as shown in Fig 2.8 (b). When the power switch M_1 is on, the magnetization inductor L_M is charged and D_1 is off due to the voltage relation due to the transformer. When M_1 is off, L_M is discharged, and the transformed current I_{D1} flows through the diode and the output capacitor. The conversion ratio *M(D)* of the flyback converter can be expressed as

$$\Delta I_{LM} = \frac{V_{IN}}{L_M} D + \frac{(-V_{OUT} / N)}{L_M}(1 - DT) = 0 \tag{2.13}$$

$$M(D) = \frac{V_{OUT}}{V_{IN}} = N(\frac{D}{1-D}) \tag{2.14}$$

where N is the turn ratio of a transformer. When N=1, the flyback converter have same conversion ratio with the buck-boost converter.

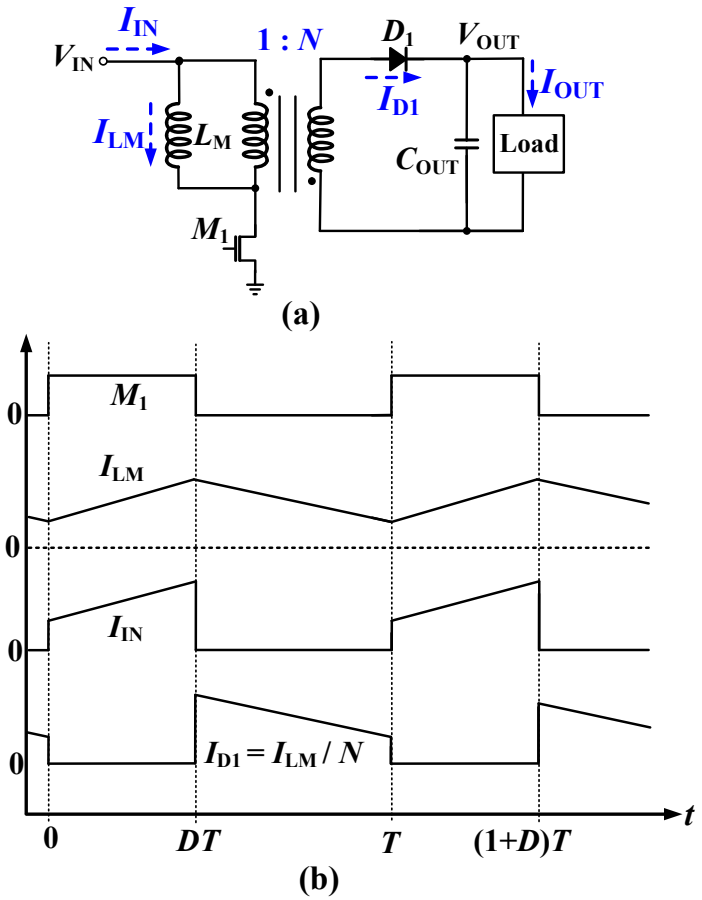


Fig. 2.8. Schematic of (a) a flyback converter and (b) its voltage and current waveforms in the CCM operation.

2.1.3.5 Summary

Fig. 2.9 plots the conversion ratios of the inductor-based converters mentioned before by using the equations (2.3), (2.10), (2.12), and (2.14). Here, it is assumed

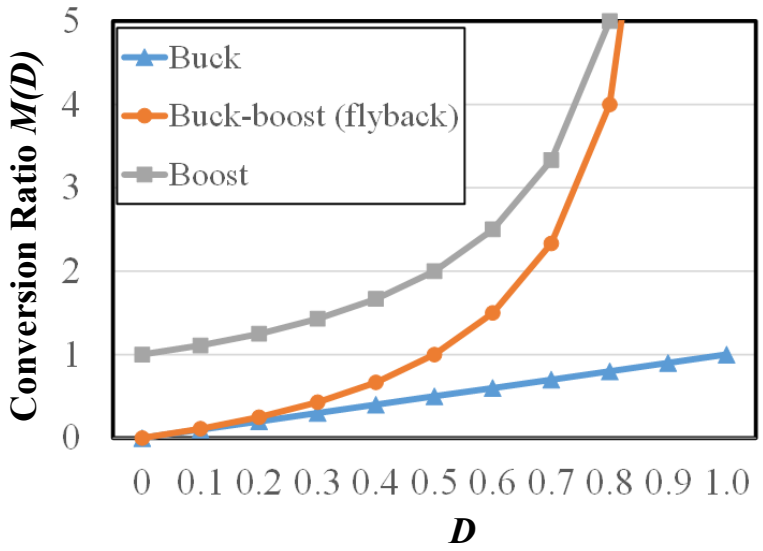


Fig. 2.9. Conversion ratios of the inductor-based converters in a CCM operation.

that the buck -boost converter has non-inverting topology like floating buck-boost and the flyback converter has the 1:1 turn ratio between the primary and secondary side. According to the configuration of the input and output voltage level, all inductor-based converters can be adopted in ac-dc and dc-dc applications. In ac-powered LED drivers, conversion ratios needs to be controlled according to the level of the ac input voltage in order to obtain a desired level of voltage or current.

2.2 Basics for LED Drivers

2.2.1 LED Configurations

In LED drivers, there are two common ways to configure LEDs, which are the series topology and parallel topology, as shown in Fig. 2.1. In series connected LEDs shown in Fig. 2.1 (a), the LED current I_{LED} flows through the all LEDs. Hence, they have same current, leading to same luminance level because the luminous flux is proportional to the LED current. However, the output voltage V_{LED} limits the number of LEDs in high power LED applications because the output voltage V_{OUT} is proportional to the number of LEDs in series.

On the other hand, the output voltage V_{OUT} is relatively low in a parallel configuration of LEDs in Fig 2.1 (b), which can alleviate the voltage limit. However, LED drivers are required to have high output current to achieve desired luminance level

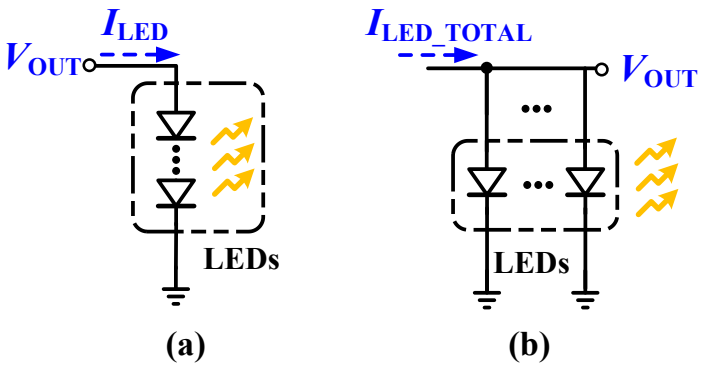


Fig. 2.10. LED configurations in LED drivers: (a) series (b) parallel.

because the tota l LED current I_{LED_TOTAL} is distributed to each LED. Moreover, their brightness level m ight be different because LEDs have turn-on voltage variations during the manufacturing process because the same output voltage is applied to all LEDs.

2.2.2 Current Sensing Techniques in LED Drivers

In order to regulate the current flowing through the LED load to a desired luminance level, first of all, a current sensing technique is required and then a feedback loop controls the PWM duty cycle *D* of the main power transistor. The simple and direct way to sense LED current is to place a resistor with the LEDs in series, as shown in Fig. 2.11. This method is employed in many LED drivers [3], [10], [19] because it can provide very accurate sense voltages to a feedback controller. How-

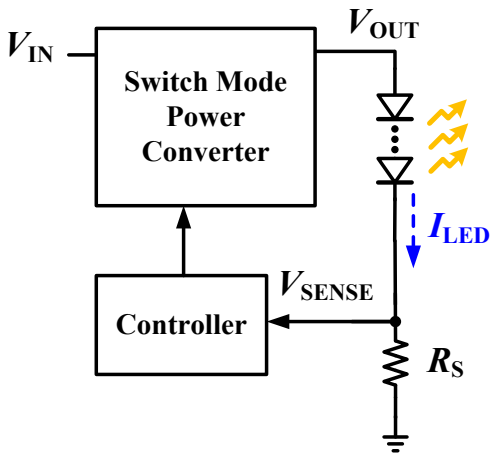


Fig. 2.11. Basic configuration of a constant current LED driver

ever, the conduction loss on R_S (= $I_{LED}^2 R_S$) might be not adequate when a series resistor with large resistance is required because the sense circuit such as a comparator or an op-amp have poor resolution. In addition, this method cannot be adopted in some LED drivers due to their converter architectures. For example, floating buck or buck-boost converters have a floating output capacitor and a LED load which are not referenced to the ground [6]. Hence, they requires a differential current sensing technique and a more complicated sense circuit. In flyback converters, an additional opto-coupler is needed because the LEDs are placed in the secondary side, on the other hand, the controller circuit is placed in the primary side due to the galvanic isolation [43].

There are indirect current sensing techniques, which can sense the currents flowing through the power switch or an inductor. A sense-FET based topology shown in Fig. 2.12 (a) senses 1000 times smaller input current by forcing the drain voltage of the two PMOS transistors (P_{MAIN} and P_{SESNE}) have same voltage level [45]. This

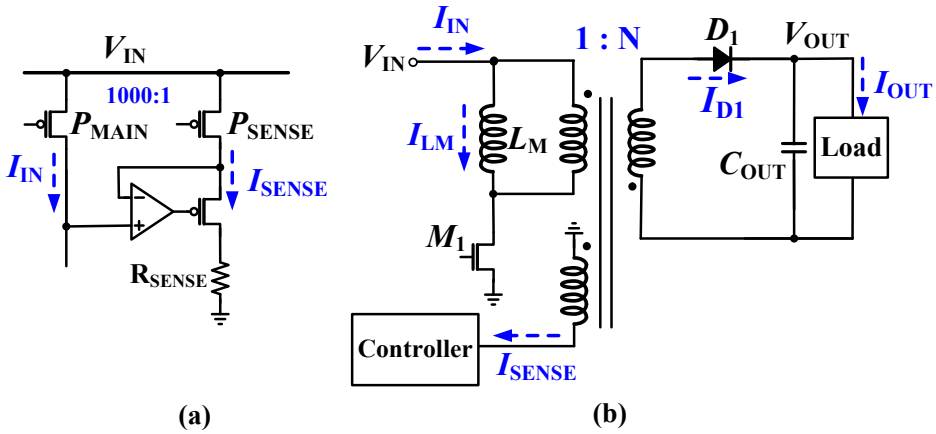


Fig. 2.12. Indirect current sensing techniques: (a) sense-FET (b) auxiliary winding.

method is suitable to an on-chip power converter where the current mirror network can be simply designed. With this technique, the LED current level can be obtained by sensing inductor current which have a certain relation with the LED current. For example, the average inductor current is equal to the average LED current in buck converter with a CCM operation. Moreover, this method can be used for a zero current detection (ZCD) in converters which operate at DCM or CRM. Fig. 2.12(b) shows an example of indirect current sensing technique in a converter where the magnetization inductor current I_{LM} is transformed to the sense current I_{SENSE}. However, converters adopting a coupled inductor can use this method by adding an auxiliary winding to the transformer.

2.3 PFC Techniques in LED Drivers

2.3.1 Power Factor

Power factor is a figure of merit which evaluates how effectively energy is transferred from input to the output load. It is defined as the ratio of the real power flowing to the output load to the apparent power in the ac system. It is also defined as

$$\text{Power factor} = \frac{P_{IN\_AVG}}{V_{AC\_RMS} \times I_{AC\_RMS}} \tag{2.15}$$

where P_{IN_AVG} is the average input power, V_{AC_RMS} and I_{AC_RMS} are the ac input voltage and current respectively. The power factor has always a value range from zero to one. When the power factor is unity, the waveforms of the input voltage and current have the same shape and same harmonic spectrum [44].

2.3.2 Passive PFC Circuit

Figure 2.13 shows two conventional passive LED driver. Although they have very simple structures with only passive elements, they do not achieve high power factor. A resistive LED driver shown in Fig. 2.13 (a) have a power factor higher than 0.8. The limitation of this topology is that the conduction time of the LED current does not fully cover one ac cycle due to the turn-on voltages of the LEDs. Fig. 2.13 (b) illustrates a resistive LED driver with a valley fill circuit that is employed to increase the conduction time of the input. Hence, this valley fill type LED driver

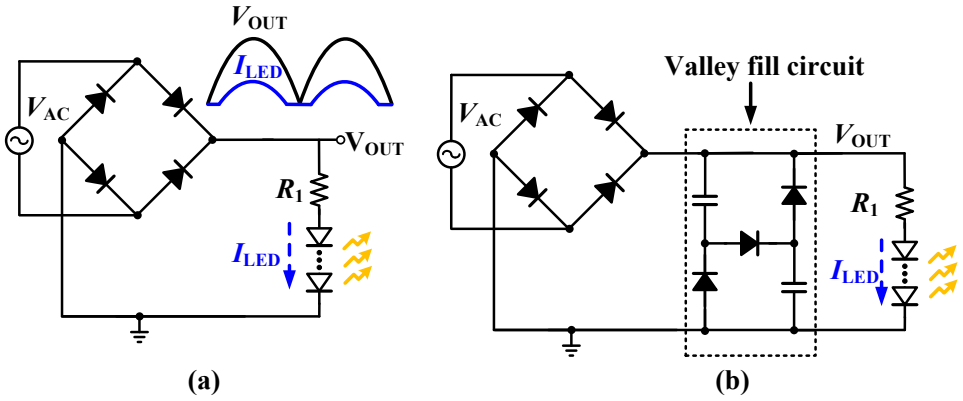


Fig. 2.13. Conventional passive PFC LED driver: (a) Resistive type (b) Valley fill type.

might achieve a power factor higher than 0.9.

2.3.3 Active PFC Circuit

Aforementioned inductor-based converters in Chapter 2.1.3 can be adopted as an active PFC circuit. A boost converter shown in Fig. 2.14 is a suitable solution to

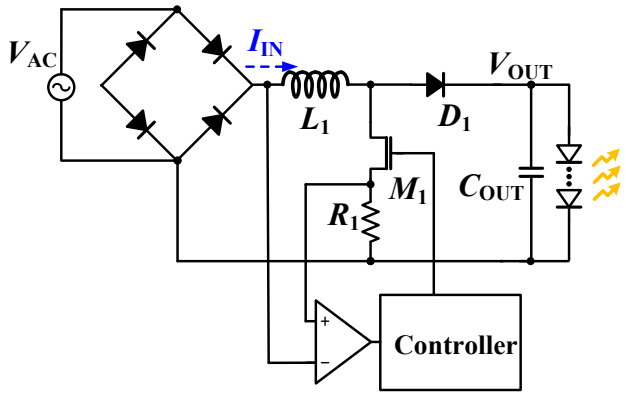


Fig. 2.14. A boost type LED driver with a PFC controller.

achieve high power factor because its input current is always continuous in a CCM operation. Therefore, if the controller circuit forces the input current to follow a reference voltage divided from the input voltage, it can achieves near unity power factor. However, the output voltage V_{OUT} is usually above 400 V in a boost type LED driver powered by a 220 V_{rms} input voltage because V_{OUT} should be higher than the input voltage in boost converters, which results in use of a bulky electrolytic capacitors and excessive number of LEDs in series.

To avoid such a voltage limitation in boost converters, many LED drivers em-

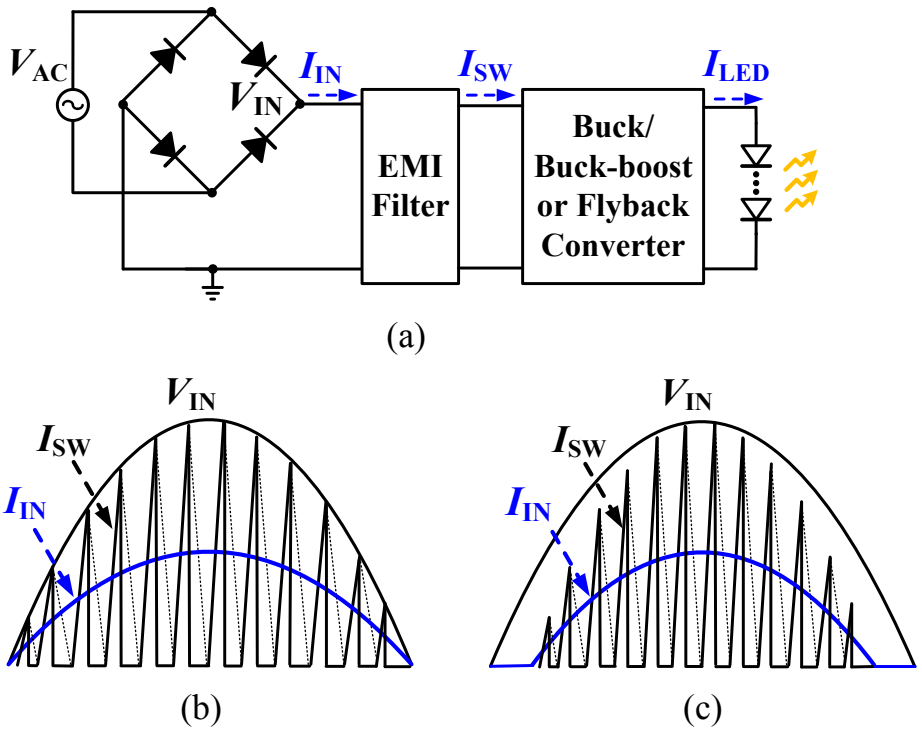


Fig. 2.15. (a) Single stage LED driver with an input EMI filter. Voltage and current waveforms of (b) a buck-boost or a flyback, and (c) a buck converter in the CRM opera-

ploys the buck or buck-boost or flyback topologies as depicted in Fig. 2.15 (a). These topologies have discontinuous input current due to the switching behavior, which limits to achieve high power factor. However, owing to the input EMI filter, the switching input current I_{SW} is shaped, consequently, the waveform of the input current I_{IN} has the shape of averaged I_{SW}. Therefore, a buck-boost [6] or a flyback [42] converters can achieve a high power factor up to 0.99 in the CRM (or DCM) operation with a fixed PWM duty cycle, as shown in Fig. 2.15 (b). In a buck converter shown in Fig. 2.15(c), it can achieve a power factor up to 0.95 because the conduction time of the input current I_{IN} is limited in buck converters [38]. In these single-stage PFC converters, high switching frequency is desirable to minimize the size of the input EMI filter.

2.4 Dimming Techniques

There are two popular techniques for dimming LEDs that are the PWM dimming and analog dimming (also called as continuous current reduction (CCR) dimming), which is shown in Fig. 2.16. In a PWM dimming, LED turns on and off at during every dimming period. A nominal rated current flows through the LEDs while the PWM switch is on, whereas there is no LED current while the PWM switch turns off. Since the average current level is changed by the PWM duty cycle, the brightness level also varies. However, the PWM dimming might exhibit light flickers because the current amplitude fluctuates between zero and the rated current, incurring a Per-

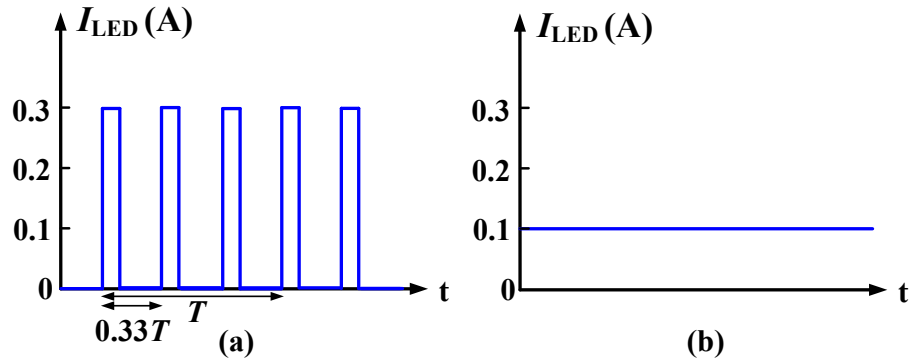


Fig. 2.16. Two popular dimming methods: (a) PWM dimming (b) analog dimming.

cent Flicker of 100%. Thus, as presented in Chapter 1, the dimming frequency should be higher than 1.2 KHz in order to avoid harmful effects to people.

On the other hand, the LED current flows continuously in an analog dimming. Instead, output current level is directly modulated because the brightness of LEDs is proportional to its forward current. Accordingly, analog dimming can be considered as an inherently flicker-free dimming method.

Chapter 3

Design of an AC-DC LED Driver with a Two Parallel Floating Buck Topology

3.1 Proposed System Architecture and Operation Principle

3.1.1 Overall Architecture

Fig. 3.1 illustrates the overall architecture of the proposed LED driver that consists of a full bridge rectifier, an EMI filter, two parallel floating buck converters, and an on-chip controller IC. The upper floating buck converter composed of M_1, L_1, D_1, D_2, and C_{STO} performs the PFC function while simultaneously transmitting energy from an ac source to a storage capacitor C_{STO}, to buffer the instantaneous power

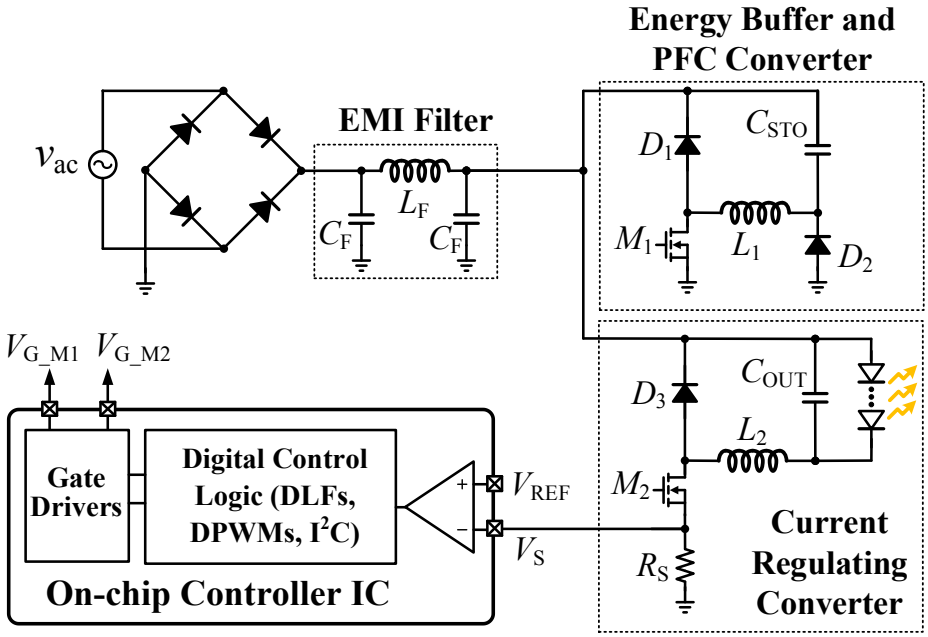


Fig. 3.1. Overall architecture of the proposed ac-dc LED driver with two parallel floating buck converters.

differences between the input power and the output LED power. The other floating buck converter consisting of M_2, L_2, D_3, and C_{OUT} regulates the output current to maintain the brightness of the LEDs to reduce light flicker. The EMI filter suppresses electrical noises from the AC source and the switching circuits, and shapes the ac input current for the PFC.

The duty cycle of the switches M_1 and M_2 are controlled by a digital control logic composed of programmable digital loop filters (DLFs) and digital pulse width modulators (DPWMs). For a 10 bit DPWM, the upper 6 bit resolution is realized by a counter-based DPWM and the lower 4 bit resolution is obtained by a phase interpo-

lator circuit to improve the input clock frequency requirement [46]. For example, if the input clock frequency is 64 MHz, the output switching frequency is 1 MHz.

Floating buck converters also known as inverted buck converters have been widely used as current regulators in dc-dc [47], [48] and ac-dc LED drivers [10], [11], [21], [38]. While the traditional buck converter with a high-side switch requires additional bootstrapping circuits, the floating buck converter with a low-side NFET can be easily driven by a gate driver circuit. Therefore, the proposed ac-dc LED driver with two floating buck converters in parallel can be cost effective because of a reduced component count [47]. Further, as a floating buck converter has a floating output voltage, the voltage stress of C_{STO} can be greatly reduced if the voltage across C_{STO} is well regulated by the controller circuit. Hence, ceramic or film capacitors can be employed for C_{STO} in place of electrolytic capacitors.

3.1.2 Operation Principle

Fig. 3.2 (a) depicts the concept of energy flow in the proposed architecture with two alternating operating modes, *Mode* 1 and *Mode* 2; Fig. 3.2 (b) illustrates its theoretical input and output power waveforms. The energies stored and released by the storage capacitor, indicated as E_{stored} and E_{released}, respectively, can be expressed as

$$E_{\text{stored}} = \int_{t_1}^{t_2} (P_{\text{in}}(t) - P_{\text{o}})\, dt \tag{3.1}$$

$$E_{released} = \int_{t_2}^{t_3} Po\, dt = P_o \times (t_3 - t_2)\,. \tag{3.2}$$

During *Mode* 1, energy from the ac input source is delivered to both the LEDs and

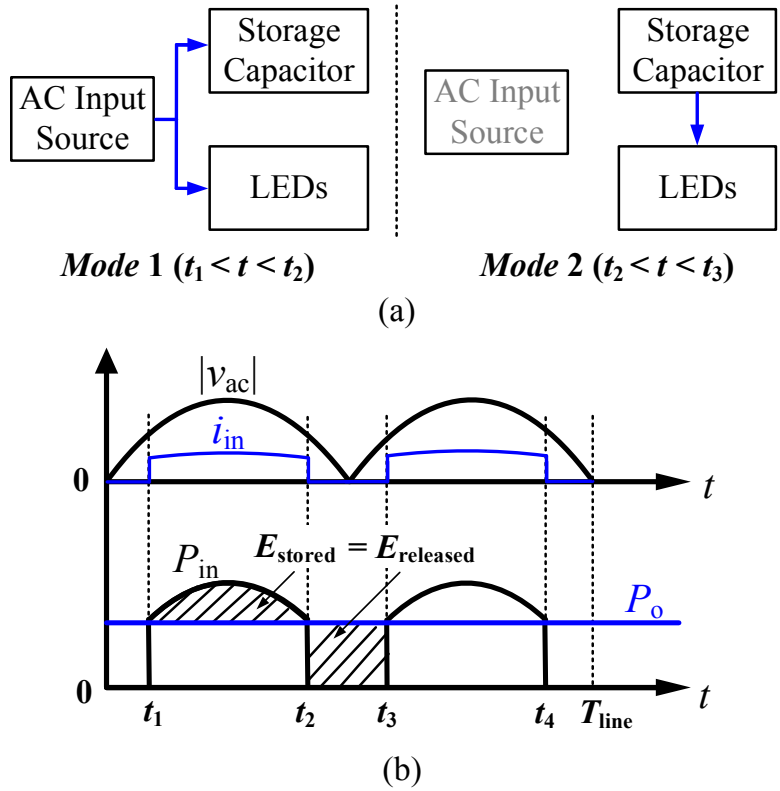


Fig. 3.2. (a) Energy flow concept and (b) input and output waveforms of the proposed LED driver with two alternating operating modes.

the storage capacitor. During *Mode* 2, the stored energy E_{stored} is transferred to the LEDs without the help of the ac source. Therefore, the LED load has a constant output current regardless of the mode of operation. The detailed explanation for each mode of operation is as follows:

1) *Mode* 1: when $|v_{ac}| > v_{sto}$ ($t_1 < t < t_2$)

Figs. 3.3 and 3.4 illustrate the operating modes and the block diagram of the proposed LED driver with two parallel floating buck converters, respectively, and Fig.

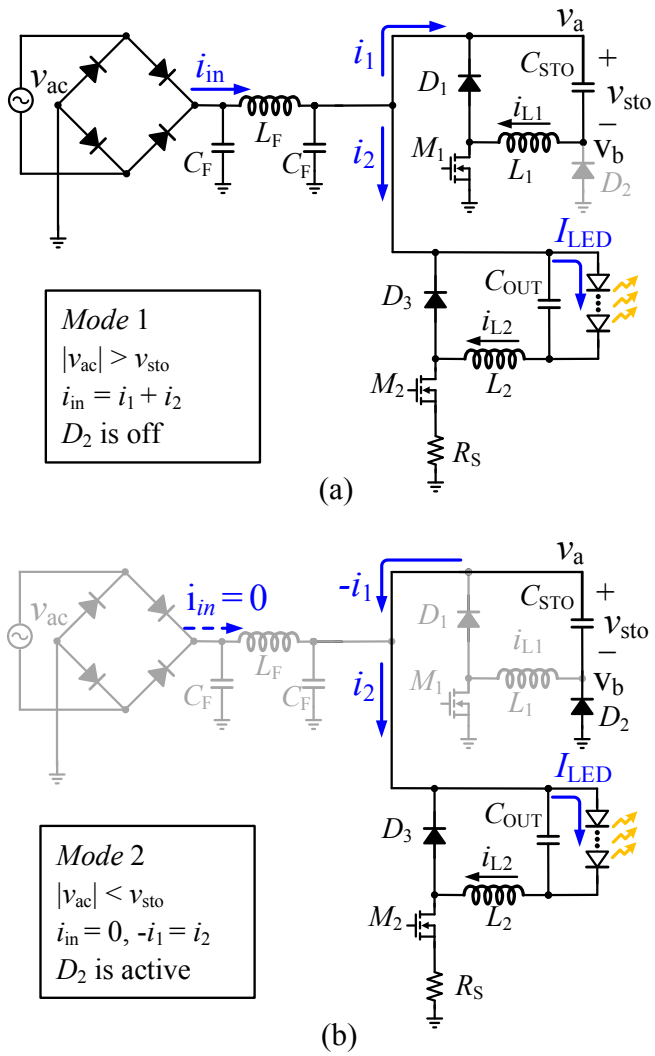


Fig. 3.3. Operating modes of the proposed LED driver: (a) *Mode* 1 when $|v_{ac}| > v_{sto}$ and (b) *Mode* 2 when $|v_{ac}| < v_{sto}$.

3.5 shows its theoretical voltage and current waveforms. The two operating modes alternate according to the voltage relationship between the ac input voltage (v_{ac}) and

the voltage across C_{STO}, denoted as v_{sto}. During *Mode* 1 when $|v_{ac}| > v_{sto,}$ the input voltage and current can be expressed as

$$v_{ac}(t) = V_m \sin wt \tag{3.3}$$

$$i_{in} = i_1 + i_2 \tag{3.4}$$

where i_1 and i_2 are input currents of the two floating buck converters, respectively. As shown in Fig. 3.3 (a), the input current (i_{in}) can be expressed as the sum of i_1 and i_2 because the two floating buck converters operate separately in *Mode* 1.

The lower floating buck converter regulates the current flowing through the LEDs regardless of the two operating modes to provide a constant current to the LEDs. This regulating converter operates in a fixed-frequency continuous conduction mode (CCM) to reduce the output voltage ripple. As shown in Fig. 3.4, the duty cycle (D_{LED}) of switch M_2 is controlled by the feedback loop to achieve the desired LED current. If we assume that the power efficiency of the current regulating con-

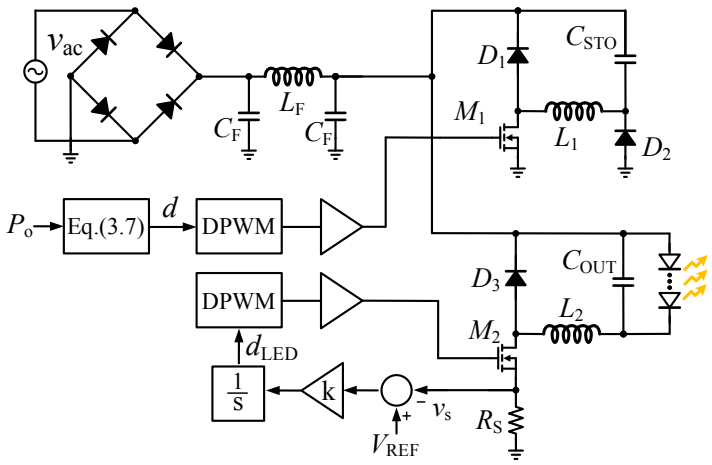


Fig. 3.4. Block diagram of the proposed LED driver with a two parallel floating buck topology.

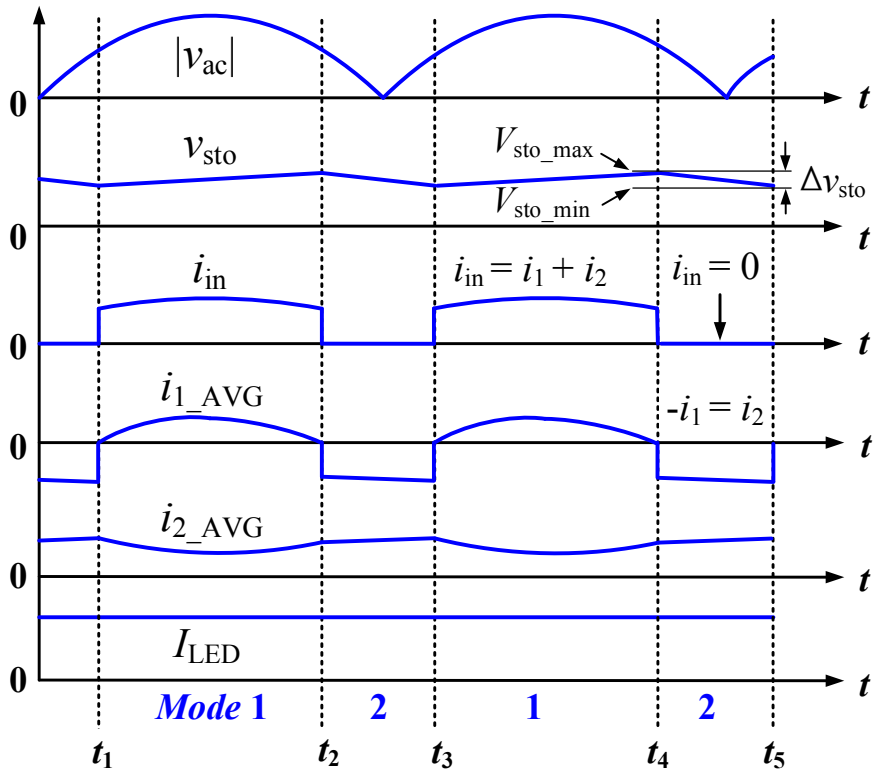


Fig. 3.5. Theoretical voltage and current waveforms of the proposed LED driver.

verter is 100%, the averaged current (i_{2_AVG}), flowing into the regulating converter in one switching cycle can be expressed as

$$i_{2\_AVG}(t) = \frac{P_o}{V_m|\sin wt|}. \tag{3.5}$$

As shown in Fig. 3.5, i_{2_AVG} is inversely proportional to the ac input voltage (v_{ac}), i.e., an additional PFC circuit is required for a high power factor. Therefore, the other floating buck converter is employed for the PFC function and placed in parallel

with the current regulating converter. Although employing a bidirectional boost converter instead of a floating buck converter is a possible approach that applies to the energy flow concept shown in Fig. 3.2, the one buck and one boost approach requires higher voltage stress in C_{STO}; i.e., v_{sto} should be higher than the ac input voltage.

To achieve a high power factor, the upper floating buck converter shown in Fig. 3.3 (a) operates in a discontinuous conduction mode (DCM) with a fixed duty cycle (D) and the diode D_2 is always off during *Mode* 1. As shown in Fig. 3.4, the duty cycle D of power switch M_1 is obtained from (3.7) and programmed to the digital control logic through an inter-integrated circuit (I^2C) interface. Although the buck PFC converter with a clipped-sinusoidal input current usually has a lower power factor than the boost PFC converter, it can achieve a power factor ranging from 0.82 to 0.98 and meet the harmonic requirements (IEC61000-3-2) [49]–[51]. Besides, its low output voltage permits the use of lower voltage-rated semiconductor devices and capacitors [49]–[51]. The averaged current (i_{1_AVG}) flowing into the buck PFC converter operating in a DCM can be expressed as

$$i_{1\_AVG}(t) = \frac{D^2}{2L_1 f_{sw}}(V_m|\sin wt| - v_{sto}(t)) \tag{3.6}$$

where D is the duty cycle of the power switch M_1 and f_{sw} is the switching frequency of the buck PFC converter [49]. It is noted that i_{1_AVG} shown in Fig. 3.5 is proportional to the voltage difference between the input voltage (v_{ac}) and the output voltage (v_{sto}). Inserting (3.5) and (3.6) into (3.4), the input current (i_{in}) is obtained as

$$i_{in}(t) = \frac{D^2}{2L_1 f_{sw}}(V_m|\sin wt| - v_{sto}(t)) + \frac{P_o}{V_m|\sin wt|} \tag{3.7}$$

where the input current (i_1) of the PFC converter cancels out the input current (i_2) of the regulating converter.

Further, the PFC converter also stores energy in C_{STO} to buffer the twice-line-frequency energy. Because this converter does not have a load to consume the output power, the energy charged onto the inductor (L_1) by the ac input source is stored in C_{STO}. Consequently, the storage capacitor voltage (v_{sto}) shown in Fig. 3.5 increases until it enters *Mode* 2 and can be expressed as

$$v_{sto}(t) = V_{sto\_min} + \frac{1}{C_{STO}}\int_{t_1}^{t} i_{L1}(t)\,dt\,,\ (t_1 < t < t_2). \tag{3.8}$$

By using the minimum and maximum voltage values of the storage capacitor, the stored energy E_{stored} is expressed as

$$E_{stored} = \frac{C_{STO}}{2}(V_{sto\_max}^2 - V_{sto\_min}^2) = C_{STO} \cdot \Delta v_{sto} \cdot V_{sto\_AVG} \tag{3.9}$$

where $\Delta v_{sto} = V_{sto\_max} - V_{sto\_min}$ and V_{sto_AVG} is the average voltage of v_{sto} across C_{STO}.

As the floating buck converter has a floating output voltage, the positive terminal voltage (v_a) of C_{STO} is equal to $|v_{ac}|$ in *Mode* 1 and the negative terminal voltage (v_b) can be expressed as

$$v_b(t) = |v_{ac}(t)| - v_{sto}(t)\,. \tag{3.10}$$

As the voltage level of $|v_{ac}|$ decreases, v_b also decreases and approaches ground. When $|v_{ac}|$ falls below $v_{sto,}$ v_b becomes negative. Consequently, a transition from *Mode* 1 to *Mode* 2 occurs when diode D_2 becomes active and starts conducting.

2) *Mode* 2 when $|v_{ac}| < v_{sto}$ ($t_2 < t < t_3$)

As illustrated in Fig. 3.3 (b), the full bridge rectifier is off and the PFC converter

is idle because v_{sto} is higher than $|v_{ac}|$. Thus, the input current (i_{in}) and the current (i_2) flowing into the lower floating buck converter are:

$$i_{in} = 0 \text{ and } i_2 = -i_1 . \tag{3.11}$$

The storage capacitor C_{STO} operates like a ground-connected capacitor and acts as an energy source for the regulating converter. When the switch M_2 is on, the diode D_2 turns on and the energy stored in C_{STO} during *Mode* 1 is delivered to the LEDs. Hence, v_{sto} decreases until it enters *Mode* 1, whereas, the averaged current (i_{2_AVG}) increases because the input current of the regulating converter is inversely proportional to the input voltage. Similar to the derivation of (3.5) in *Mode* 1, v_{sto} and i_{2_AVG} as shown in Fig. 3.5, can be expressed as

$$i_{2\_AVG}(t) = \frac{P_O}{v_{sto}(t)} \tag{3.12}$$

where $$v_{sto}(t) = V_{sto\_max} - \frac{1}{C_{STO}}\int_{t_2}^{t} i_2(t)\, dt \quad (t_2 < t < t_3). \tag{3.13}$$

Here, the voltage (v_{sto}) on the storage capacitor should be higher than the output voltage across the LED load for the buck operation, i.e., $V_{sto\_min} > V_{out}$.

In the following ac cycle, when the ac input voltage increases above v_{sto}, the full bridge rectifier is turned on, the diode D_2 is off and *Mode* 1 starts again. It is noted that the input voltage of the regulating converter is v_{ac} in *Mode* 1 and v_{sto} in *Mode* 2. Hence, the input voltage level is continuous because mode changes occur when the two voltages (v_{ac} and v_{sto}) have the same voltage level. Therefore, the regulating converter can supply a dc current to the LEDs without causing a fluctuation in I_{LED} during the transition period between the two operating modes.

3.1.3 Discussion on Dimming

Although the proposed LED driver does not have the dimming function, the proposed architecture could accommodate analog dimming operation. The regulating buck converter can adjust the continuous value of the LED current while changing the dimming level of LEDs by setting the reference voltage (V_{REF}) shown in Fig. 3.4. Owing to the P_o variations with the dimming of LEDs, the level of v_{sto} varies because the amount of energy stored and released by C_{STO} is proportional to P_o. Therefore, the duty cycle D of M_1 in the PFC converter must be controlled by a feedback loop to maintain v_{sto} in the proper operating range during the dimming operation. If the feedback loop for the dimming operation is added to the controller IC, we expect that analog dimming would be possible in this approach. A behavioral simulation is

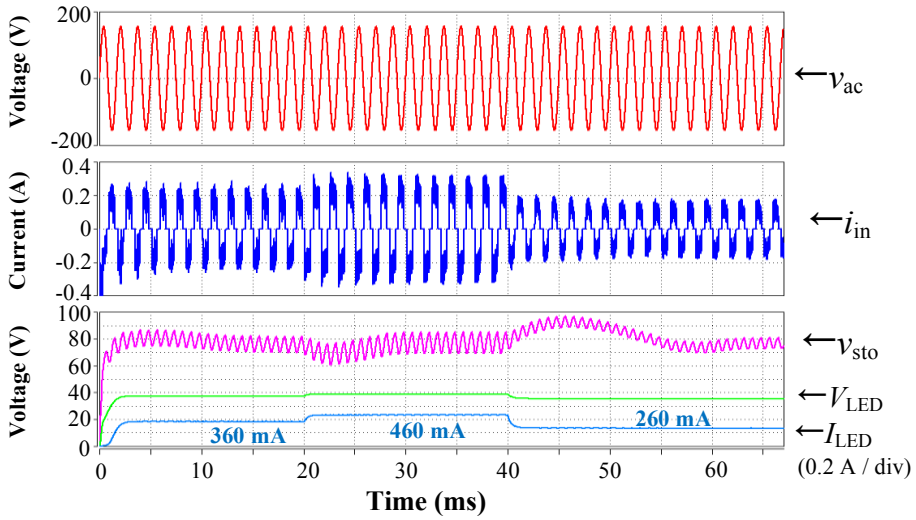


Fig. 3.6. Simulated waveforms that represents LED dimming operation.

performed to demonstrate the dimming function, where the duty cycle of M_1 is controlled by a feedback loop. As shown in Fig 3.6, the LED current settles to a new value after adjusting the reference voltage to set the LED current level.

3.2 Design of the Proposed Topology

3.2.1 Relationship Between the Input Current Waveform and the Power Factor

The line input current (i_{in}) consists of two current components (i_1 and i_2) that flow into the respective floating buck converters in *Mode* 1. By substituting $a_1 = \frac{D^2}{2L_1 f_{sw}}$ into (3.7), the input current is rearranged as

$$i_{in}(t) = a_1 (V_m |\sin wt| - v_{sto}(t)) + \frac{P_o}{V_m |\sin wt|}. \quad (3.14)$$

The input current waveform is determined by the design parameter (a_1), the storage capacitor voltage (v_{sto}), and the output power (P_o). Fig. 3.7 illustrates the variations in the input current waveform according to the amplitude of i_1 that is the input current of the PFC converter, in *Mode* 1. It is assumed that the output power (P_o) is 15 W, v_{sto} (t) has a constant value of $V_m/2$ for simplicity, and the power efficiency is different in each case to show variations of the input current waveform. Figs. 3.7 (a) and 3.7 (b) show the averaged currents i_{1_AVG} and i_{2_AVG} in one switching cycle, respectively, and Fig. 3.7 (c) depicts an example of the input current's (i_{in}) waveform by summing the two input current components. As the amplitude of i_1 increases, the input current increasingly resembles a sine curve and achieves a higher power factor, of up to 0.97.

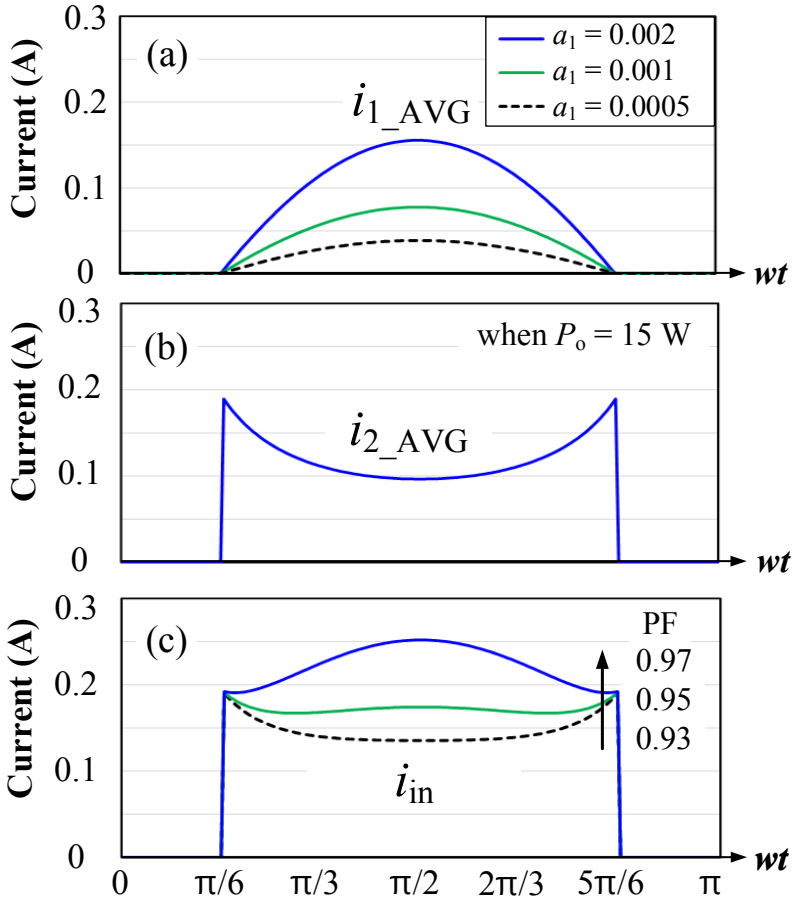


Fig. 3.7. Example of the input current waveforms according to the amplitude of i_1 in *Mode* 1, when $v_{sto}(t)$ is $V_m/2$ (= 77.8 V) and the output power (P_o) is 15 W.

3.2.2 Design Considerations for Deciding the Storage Capacitor Voltage

As described in section II, the storage capacitor voltage (v_{sto}) increases in *Mode* 1, whereas, it decreases in *Mode* 2. The average voltage of v_{sto} settles to a certain value where the stored energy (E_{stored}) in C_{STO} is equal to the released energy ($E_{released}$) for the LED load. Fig. 3.8 describes the variations in the waveforms of the respective input currents (i_{in_1} and i_{in_1}) and the input powers (P_{in_1} and P_{in_2}) depending upon the voltage across the storage capacitors (V_{sto_1}: 110 V and V_{sto_2}: 77.8 V), respectively. Here, the output power (P_o) is 15 W; it is assumed that V_{sto_1} and V_{sto_2} are constant and the power conversion efficiency is 100%. The conduction periods of i_{in_1} and i_{in_2} are 1/2 and 2/3, respectively, of a half line cycle, as they are decided by the voltage levels of v_{sto_1} and v_{sto_2}, respectively. In other words, the stored energy ratio (E_{stored} / E_{total}) is 1/2 in *case* 1 and 1/3 in *case* 2, where E_{total} is the total input energy for one half line cycle. Therefore, as shown in Fig. 3.8 (c), the input power (P_{in_1}) is higher than P_{in_2} for most of the conduction period so that more energy is stored in C_{STO}. As shown in Fig. 3.8 (b), compared to i_{in_2}, it should be noted that i_{in_1} leads to a lower power factor of 0.9 owing to a shorter conduction period, although its waveform is more similar to the line voltage.

Fig. 3.9 plots the stored energy ratio (E_{stored}/E_{total}) and the power factor with respect to the average values of the storage capacitor voltage denoted as V_{sto_AVG}, when the output power is 15 W and the input voltage is 110 V_{rms}, where it is assumed that the efficiency is 100% and v_{sto} has a constant value of V_{sto_AVG}. The stored energy ratio (E_{stored}/E_{total}) increases from 0.21 to 0.56 with the voltage level of V_{sto_AVG} that

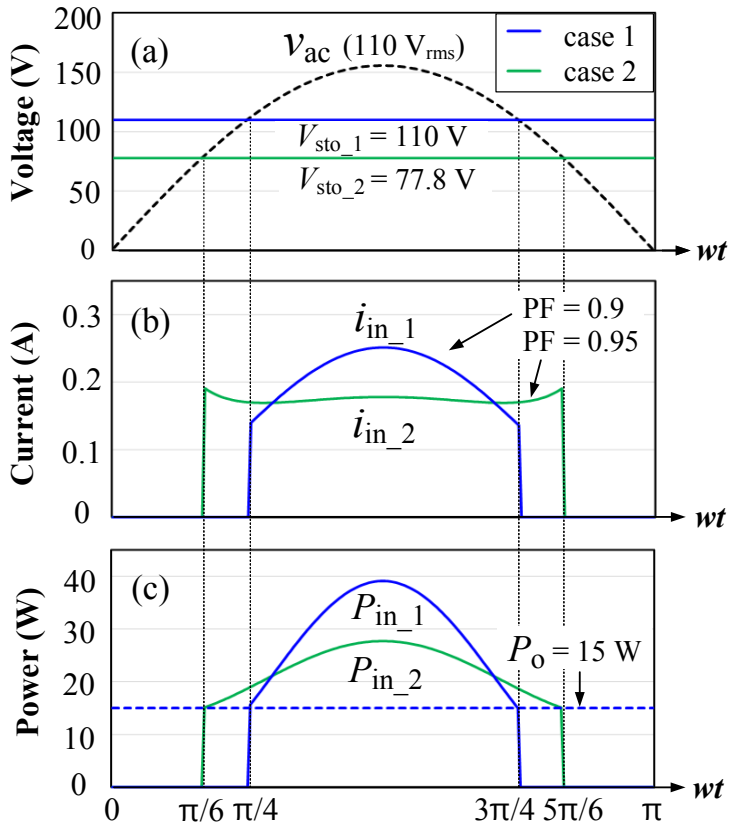


Fig. 3.8. Waveforms of the input current and input power at two different voltage levels of v_{sto}, when the output power (P_o) is 15 W: (a) v_{sto} (case 1: 110 V, case 2: 77.8 V), (b) i_{in}, and (c) P_{in}.

decides the length of the *Mode* 2 period, where the LED load is driven by the stored energy E_{stored} in the storage capacitor. Minimizing E_{stored}/E_{total} is desirable for improving the efficiency of the proposed LED driver because E_{stored} is the energy that is converted twice before it is finally delivered to the LED load. Moreover, according to (13), the voltage stress and the size of the storage capacitor can be reduced if

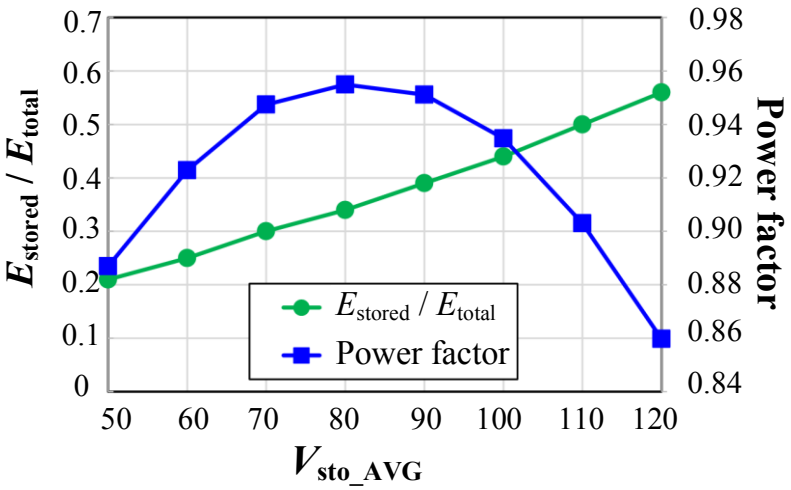


Fig. 3.9. Stored energy ratio (E_{stored}/E_{total}) and power factor with respect to the average values of the storage capacitor voltage, when the input voltage is 110 V_{rms}.

E_{stored} is decreased.

As V_{sto_AVG} increases from 50 to 120 V, the values of the power factor increase from 0.89 to 0.95 until V_{sto_AVG} is 8 0 V and then they decrease from 0.95 to 0.86. When V_{sto_AVG} is below 80 V, the input power factor is primarily influenced by the amplitude of the input current component for the PFC. However, when V_{sto_AVG} is above 80 V, the power factor is degraded by the reduced conduction time of the input current. For a power factor greater than 0.9, to comply with the ENERGY STAR standards [6], the possible voltage range of V_{sto_AVG} is 55–110 V, in this example. Therefore, a design trade-off between minimizing E_{stored}/E_{total} and achieving a high power factor needs to be considered when deciding the storage capacitor voltage.

3.2.3 Analysis of the Proposed LED Driver with Line Voltage Variations

The graphs of the power factor and E_{stored}/E_{total} plotted in Fig. 3.9 maintain the same shape as the line voltage varies. However, the values of V_{sto_AVG} shown on the x-axis vary proportionally with the line voltage because the conduction time of the input current is decided by V_{sto_AVG}; i.e., the operating mode changes when $V_m \sin wt = v_{sto}$. According to (3.7), with line voltage variations, the two current components of the input current (i_{in}) increase or decrease in opposite directions because the buck PFC converter operates with a fixed duty cycle *(D)*. In other words, the stored energy ratio (E_{stored}/E_{total}) and the ratio of $V_{sto\_AVG}/V_{in,rms}$ increase with the line voltage.

To handle line voltage variations ranging from 80 to 132 V_{rms}, V_{sto_AVG} must be maintained within a voltage range from $V_{in,rms}/2$ to $V_{in,rms}$ for PF > 0.9, which is equivalent to E_{stored}/E_{total} being 0.23–0.5. For example, V_{sto_AVG} must be less than 132 V for $E_{stored}/E_{total} < 0.5$ when the input voltage is 132 V_{rms}. On the other hand, V_{sto_AVG} must be higher than 40 V for $E_{stored}/E_{total} > 0.23$ when the input voltage is 80 V_{rms}. Here, $V_{sto\_min} > V_{out}$ must be satisfied for proper operation of the LED driver. If V_{sto_AVG} becomes too low, i.e., $V_{sto\_min} > V_{out}$ cannot be satisfied, the Percent Flicker increases because the LED load cannot be fully driven by C_{STO} during *Mode* 2.

The input voltage range of the proposed LED driver can be derived by calculating the stored energy (E_{stored}) for a half line cycle when the stored energy ratio (E_{stored}/E_{total}) is 0.23 and 0.5. For simplicity of analysis, it is assumed that the efficiency is 100% and v_{sto} has a constant value of V_{sto_AVG} that is higher than V_{out}. According to Fig. 3.9, the two cases can be summarized as follows:

1) When $V_m = V_{m\_min}$, $E_{stored1}/E_{total} = 0.23$ and $V_{sto\_AVG1} = 0.5 \times \frac{V_{m\_min}}{\sqrt{2}}$

2) When $V_m = V_{m\_max}$, $E_{stored2}/E_{total} = 0.5$ and $V_{sto\_AVG2} = \frac{V_{m\_max}}{\sqrt{2}}$

where V_{m_min} and V_{m_max} are the minimum and maximum amplitudes, respectively, of the input voltage in each case. Because the total input energy (E_{total}) is equal in each case, the relationship between $E_{stored1}$ and $E_{stored2}$ is

$$E_{stored1} = (0.23/0.5) \times E_{stored2}. \tag{3.15}$$

Because E_{stored} is the input power of the PFC buck converter, it can be expressed as

$$E_{stored} = \int_{t_1}^{t_2} v_{ac}(t) \times i_1(t)\, dt\,. \tag{3.16}$$

By substituting $v_{ac}(t)$ with (3.3) and $i_1(t)$ with (3.6), $E_{stored1}$ is derived as

$$\begin{aligned} E_{stored1} &= \int_{t_1}^{t_2} (V_{m\_min} \sin wt) \times \frac{D^2}{2L_1 f_{sw}} (V_{m\_min} \sin wt - V_{sto\_AVG1})\, dt \\ &= \frac{D^2 {V_{m\_min}}^2}{2L_1 f_{sw}} \int_{t_1}^{t_2} \sin wt \times (\sin wt - \frac{V_{sto\_AVG1}}{V_{m\_min}})\, dt \end{aligned} \tag{3.17}$$

where $t_1 = 0.115 \times (T_{line}/2)$ and $t_2 = (1 - 0.115) \times (T_{line}/2)$. In the same manner, $E_{stored2}$ is obtained as

$$E_{stored2} = \frac{D^2 {V_{m\_max}}^2}{2L_1 f_{sw}} \int_{t_1}^{t_2} \sin wt \times (\sin wt - \frac{V_{sto\_AVG2}}{V_{m\_max}})\, dt \tag{3.18}$$

where $t_1 = 0.25 \times (T_{line}/2)$ and $t_2 = (1 - 0.25) \times (T_{line}/2)$.

By inserting (3.17) and (3.18) into (3.15) and calculating the integral values, the ratio of V_{m_max}/V_{m_min} is derived as

$$2.33\text{e-}3 \times V_{\text{m\_min}}{}^2 = 0.46 \times 7.57\text{e-}4 \times V_{\text{m\_max}}{}^2$$
$$\frac{V_{\text{m\_max}}}{V_{\text{m\_min}}} = 2.59\,. \tag{3.19}$$

Thus, if the proposed LED driver is designed to have $E_{\text{stored}}/E_{\text{total}} = 0.23$ at the input voltage of 80 V_{rms}, it can operate with an input voltage of up to 207 V_{rms}, where $E_{\text{stored}}/E_{\text{total}} = 0.5$.

3.2.4 Design of the Floating Buck Converter for PFC and Energy Buffering

Based on these considerations, the design procedure for the floating buck converter for PFC and energy buffering is presented. The target value of $V_{\text{sto\_AVG}}$ at the input voltage of 80 V_{rms} is set as 50 V to satisfy $V_{\text{sto\_min}} > V_{\text{out}}$, where V_{out} is approximately 43 V at the LED current of 350 mA for an output power of 15 W in our design. Here, the input power factor is 0.945 and $E_{\text{stored}}/E_{\text{total}}$ is 0.291 according to Fig. 3.9. When the range of $E_{\text{stored}}/E_{\text{total}}$ is reduced to 0.291–0.5, the ratio of $V_{\text{m\_max}}/V_{\text{m\_min}}$ is obtained as 2.08 by using (19)–(23), i.e., the allowed input voltage range is 80–166 V_{rms} when the target value of $V_{\text{sto\_AVG}}$ is chosen as 50 V at the input voltage of 80 V_{rms}. Thus, the proposed LED driver can handle the 110 V_{rms} line voltage variation ranging from 80 to 132 V_{rms}, as plotted in Fig. 3.10 where the range of $E_{\text{stored}}/E_{\text{total}}$ is 0.291–0.437 and the power factor is higher than 0.9.

By rearranging (13), the storage capacitance is obtained as

$$C_{\text{STO}} = \frac{E_{\text{stored}}}{\Delta v_{\text{sto}} \cdot V_{\text{sto\_AVG}}}\,. \tag{3.20}$$

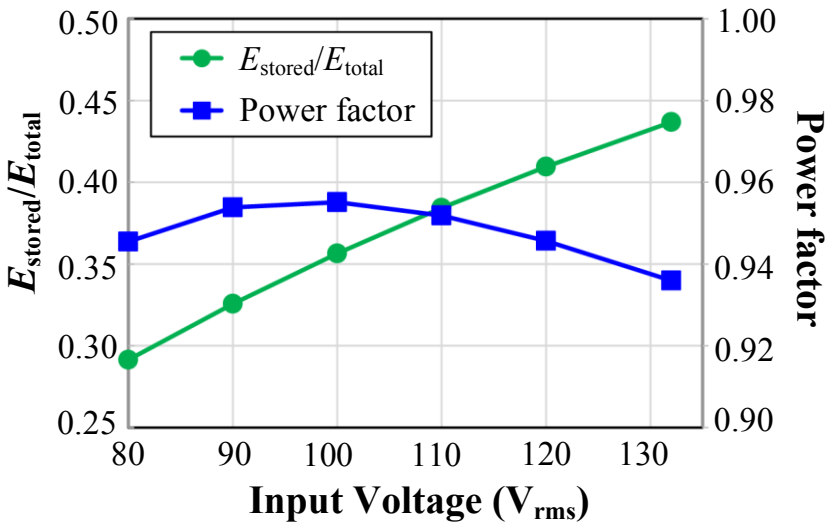


Fig. 3.10. Stored energy ratio (E_{stored}/E_{total}) and power factor with respect to an input voltage ranging from 80 to 132 V_{rms}.

As plotted in Fig. 3.11, the worst case in terms of the size of C_{STO} is when the line voltage is at the minimum voltage of 80 V_{rms}. This is because V_{sto_AVG} increases faster than E_{stored} as the line voltage increases according to the data in Figs. 10 and 11. The estimated value of C_{STO} at the minimum line voltage of 80 V_{rms} is 33.9% higher than that of C_{STO} at the line voltage of 110 V_{rms}. Moreover, when the input voltage is 80 V_{rms}, V_{sto_AVG} has its minimum value, and the allowed Δv_{sto} is reduced because $V_{sto\_min} > V_{out}$ must be satisfied. Thus, the required capacitance of C_{STO} is determined by the minimum input voltage of 80 V_{rms}, as plotted in Fig. 3.12. Because the maximum allowable Δv_{sto} is 14 V when V_{out} is about 43 V, and the capacitance for C_{STO} calculated with (24) is 52.5 μF. According to Figs. 3.9 and 3.10, when the input voltage is 132 V_{rms}, E_{stored}/E_{total} is 0.437 and the corresponding V_{sto_AVG} is

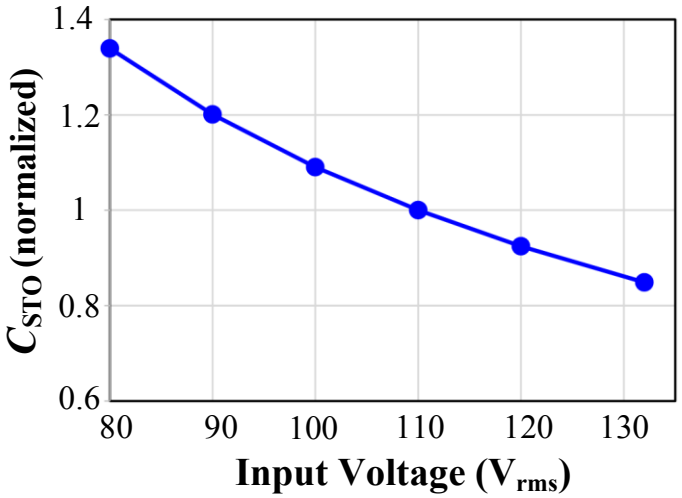


Fig. 3.11. Required size of C_{STO} with a constant Δv_{sto} with respect to an input voltage ranging from 80 to 132 V_{rms}.

118.3 V with Δv_{sto} of 8.8 V, i.e., the maximum voltage rating on C_{STO} is approximately 123 V. Therefore, for the design margin, we used a 68 μF, 250 V film capacitor for C_{STO}. This can be replaced by a capacitor with a lower voltage rating (e.g., 160 V).

The buck PFC converter with no load operates in a DCM with a fixed duty cycle (D). Fig. 3.13 shows the waveform of the inductor current I_{L1} in the DCM where $D'T_{sw} < T_{sw}$. The boundary condition between the CCM and DCM operation is

$$\frac{|v_{ac}(t)| - v_{sto}(t)}{L_1} DT_{sw} + \frac{-v_{sto}(t)}{L_1}(1-D)T_{sw} = 0 \tag{3.21}$$

where the duty cycle (D) is derived as

$$D = \frac{v_{sto}(t)}{|v_{ac}(t)|} \text{ (for the boundary condition)}, \quad D < \frac{v_{sto}(t)}{|v_{ac}(t)|} \text{ (for the DCM)}. \tag{3.22}$$

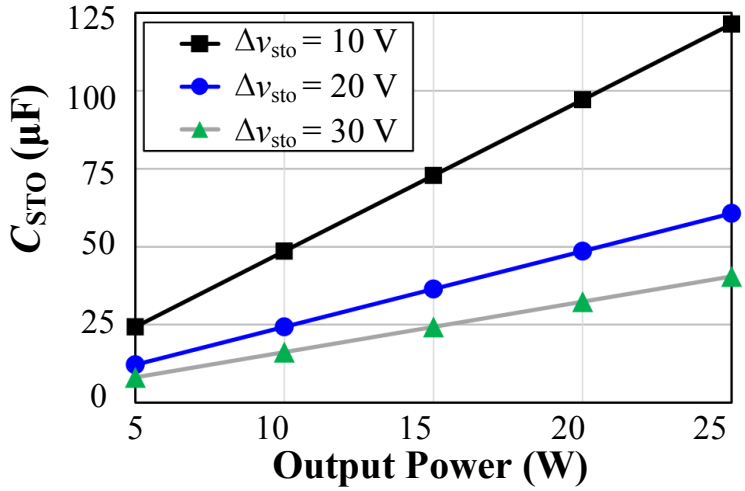


Fig. 3.12. Required capacitance for C_{STO} with respect to the output power, when V_{sto_AVG} is 50 V and the input voltage is 80 V_{rms}.

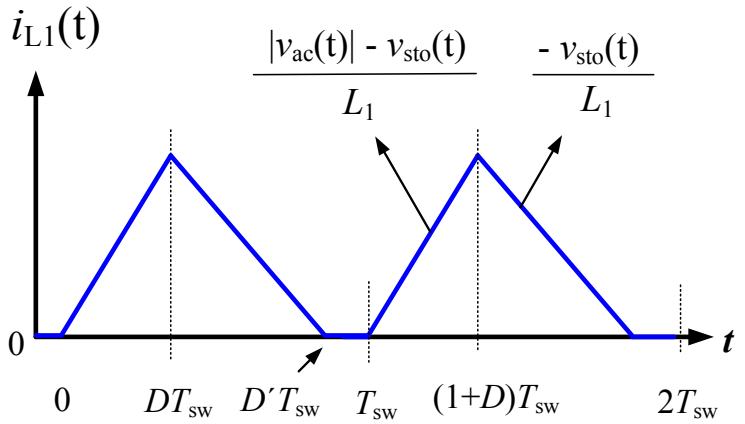


Fig. 3.13. Inductor current waveform of the buck PFC converter operating in a DCM.

In our design, the duty cycle (D) should be less than 0.32 to operate in a DCM. The value of the duty cycle (D) can be calculated by $D = \sqrt{2 \cdot a_1 \cdot L_1 \cdot f_{sw}}$, derived

from (3.14). The design parameter a_1 is obtained as 1.49e-3 when it is assumed that the efficiency is 100%. The switching frequency (f_{sw}) of the PFC converter is chosen as 1 MHz to reduce the inductance (L_1) that is selected as 22 μH. Because the proposed LED driver handles the relatively low power level, the frequency of 1 MHz is selected as a trade-off. Consequently, the calculated value of D is 0.256 that satisfies the DCM operation condition of (3.22).

3.2.5 Design of the Floating Buck Converter for LED Current Regulation

When deciding the design parameters of the floating buck converter for regulating the LED current, the output voltage and current ripples should be considered for reducing output light flicker. As described in Section I, the Percent Flicker should be less than 9.6% at 120 Hz to be considered as low-risk levels, obtained by using (1.3). Fig. 3.14 shows the characteristics of the CREE XLamp MX-3 LED that is employed as the LED load in this study [6]. Although the LED current is 350 mA at 3.7 V at 25 ℃, and 14 series-connected LEDs were required for an output power of 15 W due to the forward voltage variation. Referring to Fig. 3.14 (b), the peak-to-peak LED current ripple should be less than approximately 85 mA for a Percent Flicker below 9.6%. To provide a design margin, the limit of the peak-to-peak current ripple is set to 67 mA that is equivalent to an LED current ripple of 9.6%, when I_{LED} is 350 mA. Consequently, the corresponding peak-to-peak voltage ripple in Fig. 3.14 (a) is around 0.11 V that is approximately 1.54 V for 14 LEDs.

The floating buck converter for regulating the LED current operates in a CCM

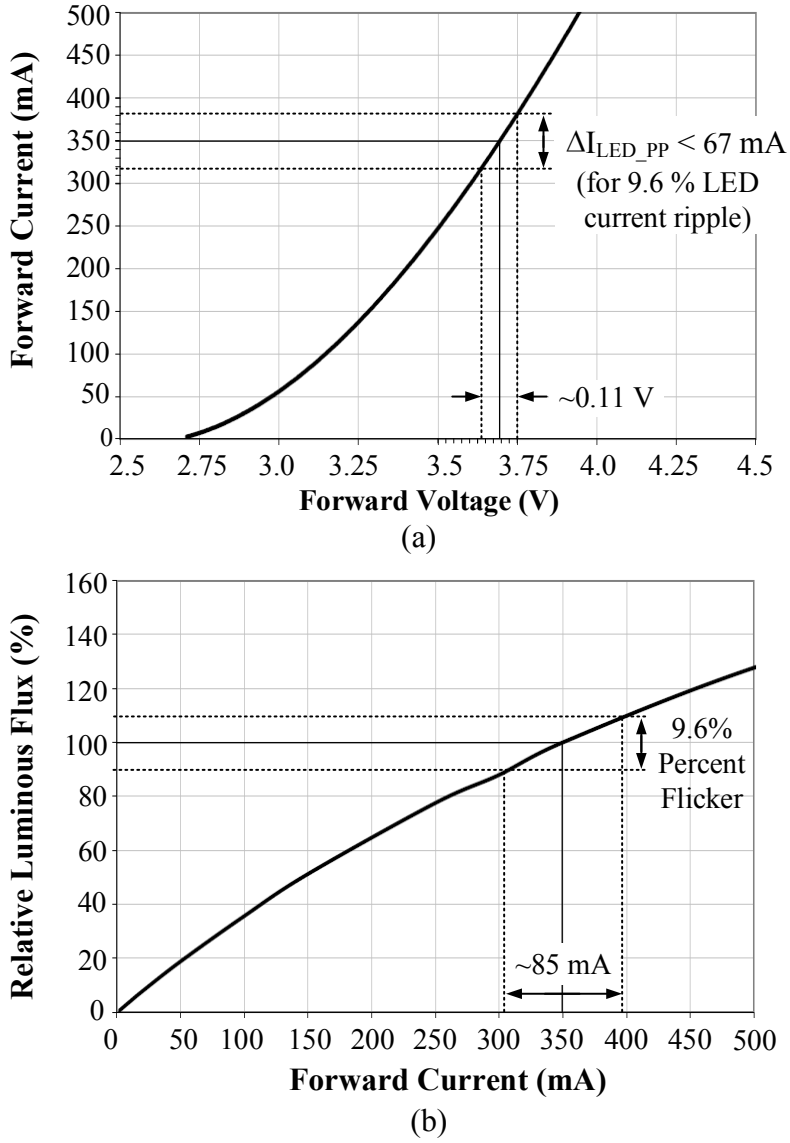


Fig. 3.14. Characteristics of the CREE XLamp MX-3 LED: (a) voltage vs. current, (b) current vs. relative luminous flux [6].

and its output voltage and inductor current waveforms are shown in Fig. 3.15. The

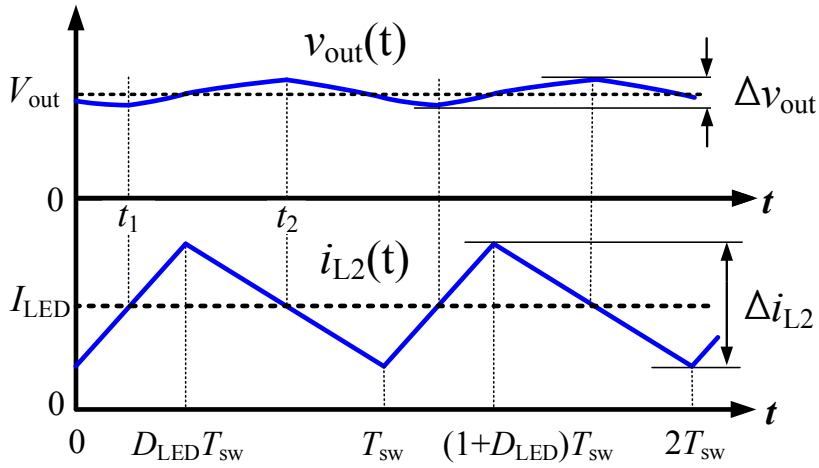


Fig. 3.15. Waveforms of the output voltage and the inductor current of the regulating converter operating in a CCM.

output voltage ripple (Δv_{out}) is expressed as

$$\Delta v_{out} = \frac{1}{C_{OUT}} \int_{t_1}^{t_2} i_{L2}(t) - I_{LED}\, dt \approx \frac{\Delta i_{L2}}{8 \cdot C_{OUT} \cdot f_{sw}} \tag{3.23}$$

where the inductor current ripple (Δi_{L2}) is

$$\Delta i_{L2} = \frac{V_{out} \cdot (1 - D_{LED})}{L_2 \cdot f_{sw}} \tag{3.24}$$

wherein D_{LED} is the duty cycle of the low-side switch. By inserting (3.24) into (3.23), the output capacitance C_{OUT} is derived as

$$C_{OUT} = \frac{V_{out} \cdot (1 - D_{LED})}{8 \cdot \Delta v_{out} \cdot L_2 \cdot f_{sw}^{\,2}}. \tag{3.25}$$

By using the CCM operating condition ($2 \times I_{LED} > \Delta i_{L2}$), the range of the induct-

ance L_2 is derived as

$$L_2 > \frac{V_{out} \cdot (1 - D_{LED})}{2 \cdot I_{LED} \cdot f_{sw}}. \tag{3.26}$$

As the input voltage level of the regulating converter varies according to time, the duty cycle (D_{LED}) is controlled by the feedback loop to deliver constant currents to the LED load. Consequently, the inductor current ripple (Δi_{L2}) and the output voltage ripple (Δv_{out}) vary with the input voltage level. According to (3.23) and (3.24), the largest values of Δi_{L2} and Δv_{out} is obtained when D_{LED} has a minimum value, i.e., the ac input voltage has its peak value. Here, the minimum value of D_{LED} is obtained as $V_{out}/V_m = 0.23$, when V_{out} is approximately 43 V and the input voltage is 132 V_{rms}; the switching frequency (f_{sw}) is selected as 1 MHz to reduce the inductance (L_2). For the CCM operation, the inductance (L_2) obtained using (3.26) should be higher than 47.3 μH. By selecting a value of 68 μH as L_2, the required output capacitance C_{OUT} obtained using (3.25) is 0.04 μF, when the output voltage ripple (Δv_{out}) is 1.32 V for an LED current ripple of 9.6%. For the design margin, the output capacitance C_{OUT} is selected as 0.47 μF.

3.3 Circuit Implementation

3.3.1 Controller Circuit Architecture

Fig. 3.16 illustrates the block diagram of the on-chip controller circuit, which consists of a feedback loop for LED current regulation and an open-loop control block for the PFC buck converter.

The feedback loop has a sensing circuit composed of a clocked comparator and a latch circuit. The digital control logic consists of digital loop filters (DLFs) and digital pulse width modulators (DPWMs), which are configured by an inter-integrated circuit (I^2C) logic. A phase interpolator (PI) circuit is employed to achieve high

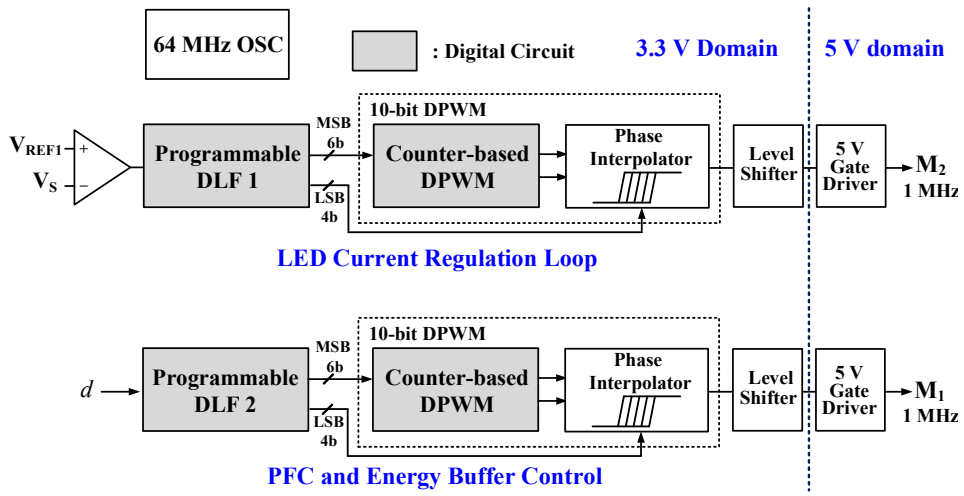


Fig. 3.16. Block Diagram of the proposed controller IC.

resolution for the 10-bit DPWM. The feedback loop sense the voltage (V_S) and controls the duty cycle of the PWM signals for regulating the LED current. An oscillator circuit generates a 64 MHz clock signal for the digital logic. This controller circuit operates at 3.3 V supply voltage except the 5 V gate drivers which require high voltage swings to drive off-chip discrete power field-effect transistors (FETs) that usually have the threshold voltages higher than 1.5 V.

3.3.2 LED Current Regulation Loop Design

Fig. 3.17 (a) illustrates the schematic of the LED current regulating converter which employs a floating buck converter according to on and off of the switch M_2. A comparator circuit senses the voltage across a sense resistor R_{SENSE} denoted as V_S and the switch control logic including a DLF and a DPWM determines the duty cycle of M_2 to achieve the desired level of the LED current. Unlike the conventional buck topology as depicted in Fig. 3.18, the floating buck topology has a structural advantage of being able to use a low-side switch (also called a ground-referenced switch), which simplifies the gate driver circuit and reduces the size of a printed circuit board (PCB). On the other hand, the configuration of the output is not referenced to the ground, which requires a complicated control scheme to sense the LED current I_{LED}.

To regulate the output LED current, it is needed to know how much current flows through the LEDs. Because the average output current is equal to the average inductor current in a buck converter operating in CCM, the inductor current I_{L2} is measured by placing the R_{SENSE} to the source node of the M2. As shown in Fig. 3.17 (b),

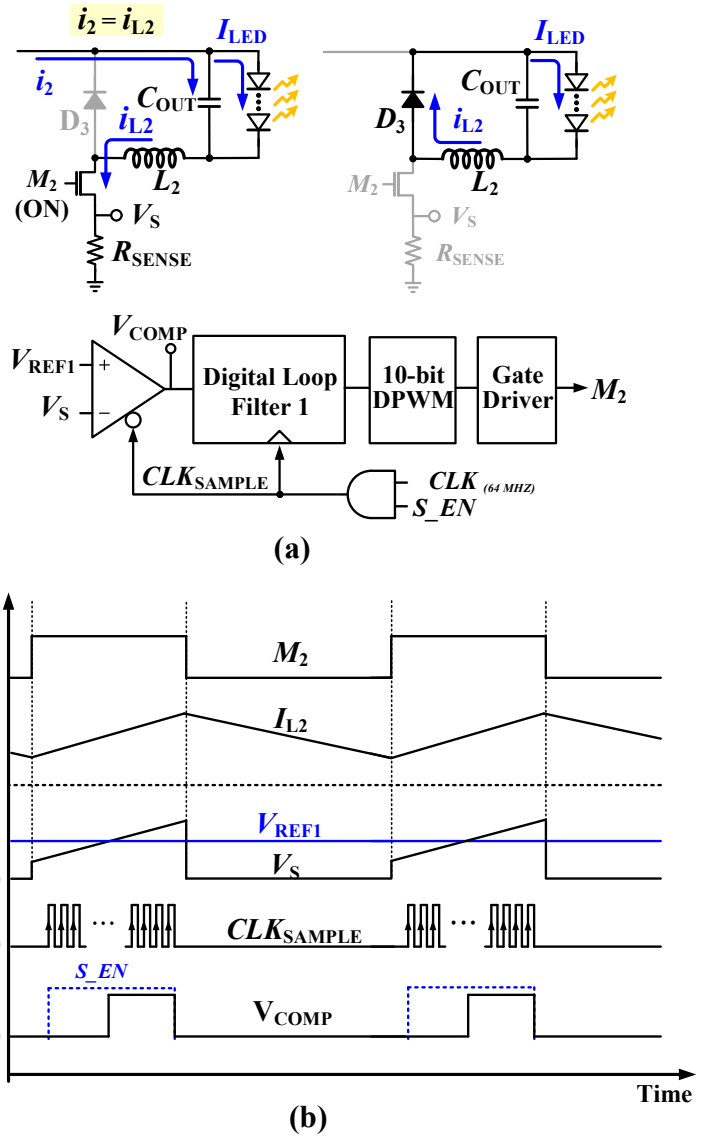


Fig. 3.17. (a) Schematic of the LED current regulating converter and its simplified feedback loop (b) Voltage and current waveforms.

the waveform of the voltage V_S is proportional to the inductor current I_{L2} while the

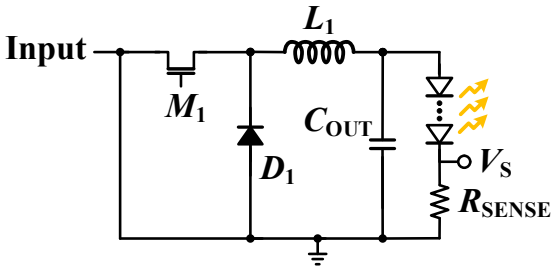


Fig. 3.18. Schematic of the conventional buck LED driver.

switch M_2 is on. The comparator circuit compares V_S with a reference voltage V_{REF1} and decides its output voltage (V_{COMP}) according to a sampling clock (CLK_{SAMPLE}). Note that the comparator output is stuck at the logical low while M_2 turns off because the inductor current I_{L2} do not flow through the R_{SENSE}. To obtain valid comparator outputs for the DLF, the sampling clock CLK_{SAMPLE} is produced by the clock signal *CLK* and a logic signal (*S_EN*) that indicates the valid sampling period. The pulse width of the *S_EN* is a little shorter than that of the M_2 to avoid transient periods where V_S may not settle yet.

3.3.3 Building Blocks

3.3.3.1 Comparator

The comparator circuit depicted in Fig. 3.19 adopts a StrongARM latch topology with an input offset compensation circuit that is designed to handle the input-referred offset voltage due to the mismatches between M_2 and M_3. A PMOS-type clocked comparator is used because the input voltage level is closer to the ground

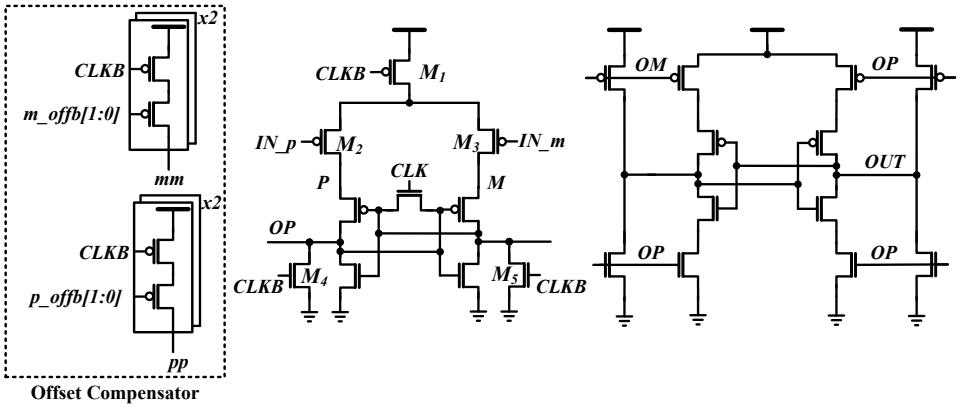


Fig. 3.19. Schematic of a clocked comparator based on StrongARM latch topology.

than the supply voltage. According to [52], the StrongARM latch is widely used because it dissipates zero static power and produce outputs with a rail-to-rail voltage level. Basic operation of this clocked comparator is as follows. When the clock signal *CLKB* is logical high, nodes *P*, *M*, *OP*, and *OM* are pre-discharged to 0 V. When *CLKB* becomes logical low, the M_4 and M_5 turns off, whereas as M_1 turns on, producing outputs at nodes *OP* and *OM* in response to the polarity between the input voltages V_{INP} and V_{INM}. The following latch maintains the value of the output voltage V_{OUT} during one clock period.

3.3.3.2 Oscillator

Fig. 3.20 depicts the schematic of an oscillator circuit and its timing diagram, where a relaxation oscillator is employed to generate a clock signal with a wide frequency tuning range and low power consumption [53]. This oscillator consists of

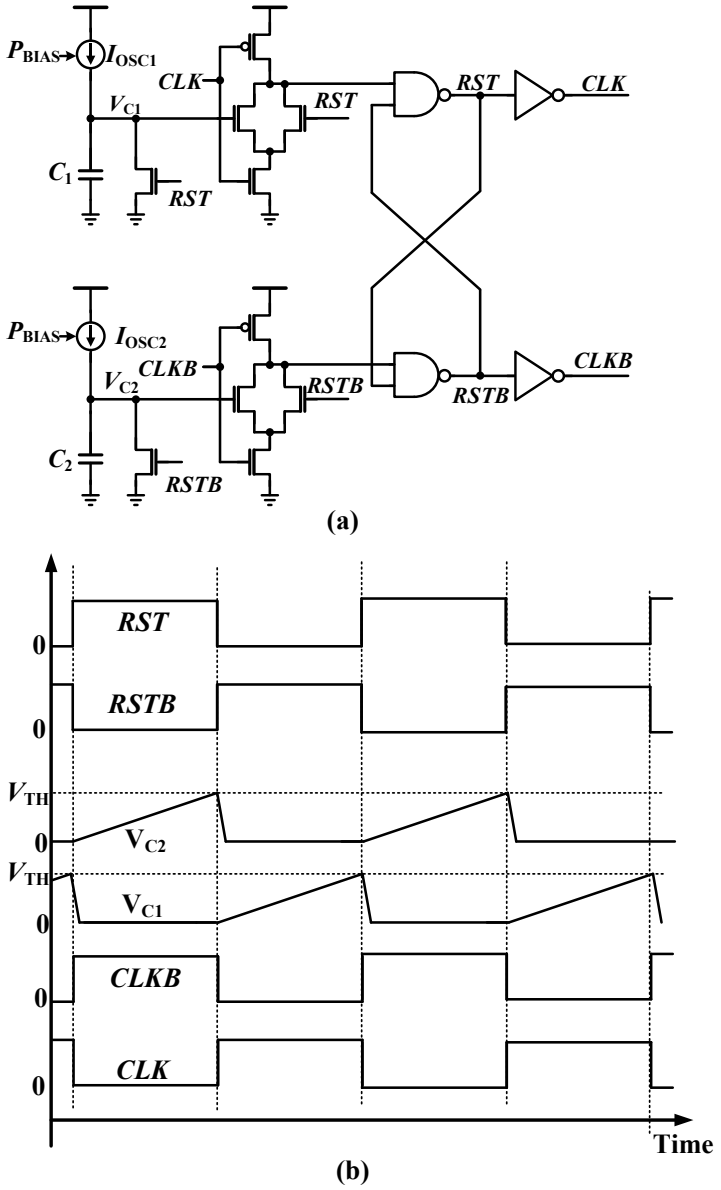


Fig. 3.20. (a) Schematic and (b) timing diagram of the relaxation oscillator circuit.

two charge-pump based ramp signal generators and two crossing detectors, and a

set-reset (SR) latch with a pair of cross-coupled NAND gates. Basic operation is as follows. As shown in Fig. 3.20 (b), an integrating capacitor C_1 is charged by a PMOS current sources I_{OSC1}. When the voltage across C_1 denoted as V_{C1} increases above a certain threshold voltage level Vth, a reset signal *RST* is triggered and then the clock signals *CLK* and *CLKB* are produced. At the same time, the other integrating capacitor C_2 starts being charged by I_{OSC2}. By operating in an alternating fashion, the oscillator can generate 50% duty cycle clock if the integrating slopes of C_1 and C_2 are same. The target oscillation frequency is 64 MHz to achieve 1 MHz DPWM output, which will be explained later.

3.3.3.3 PI-based Digital Pulse Width Modulator (DPWM)

The DPWM employs a phase-interpolating architecture to achieve 10-bit high resolution and 1 MHz output as depicted in Fig. 3.21 (a) [46]. The upper 6-bit resolution is realized by a conventional counter-based DPWM and the lower 4-bit resolution is achieved by the PI using a current steering digital-to-analog converter (DAC). While the required input clock frequency is 1024 times higher than its output signal frequency in a conventional 10-bit resolution counter-based DPWM, the input clock frequency of PI-based DPWM is 64 MHz for 1 MHz output frequency because the PI alleviates the frequency requirement. Basic operation of this DPWM is as follows. According to the coarse input code *DIN* [9:4] from a digital loop filter, the 6-bit counter-based DPWM produces the output *PWM* and the one-clock delayed output PWM_{DELAY} as shown in Fig. 3.21 (b). The PI produces the interpolated output PI_{OUT} using those two input PWM signals with different phases according to the fine

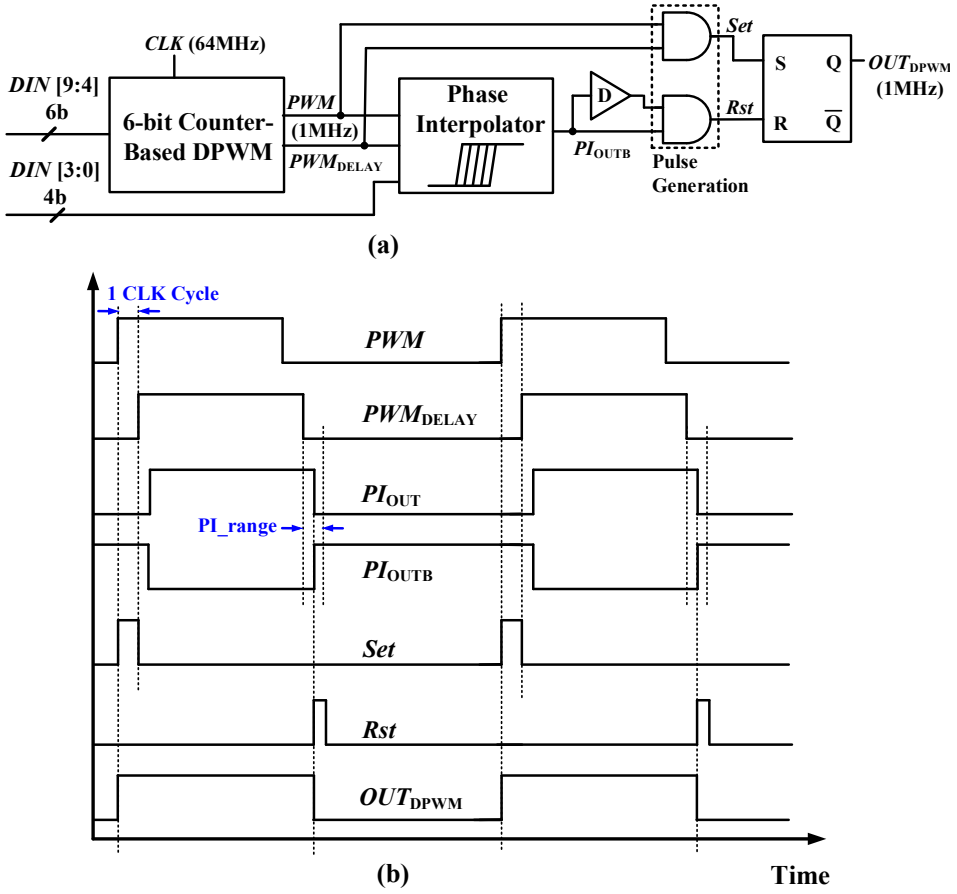


Fig. 3.21. (a) Architecture and (b) timing diagram of the PI-based DPWM.

input code *DIN* [3:0], and the pulse generation circuit sets and resets the SR latch to produce the final 10-bit output OUT_{DPWM}. The simulation result of the DPWM is shown in Fig. 3.22.

Fig. 3.23 (a) shows the schematic of the PI using a current-steering DAC [46]. The basic operation of the PI is similar to that of the oscillator presented before except the interpolation stage where integrating capacitors (C_1 and C_2) are charged by

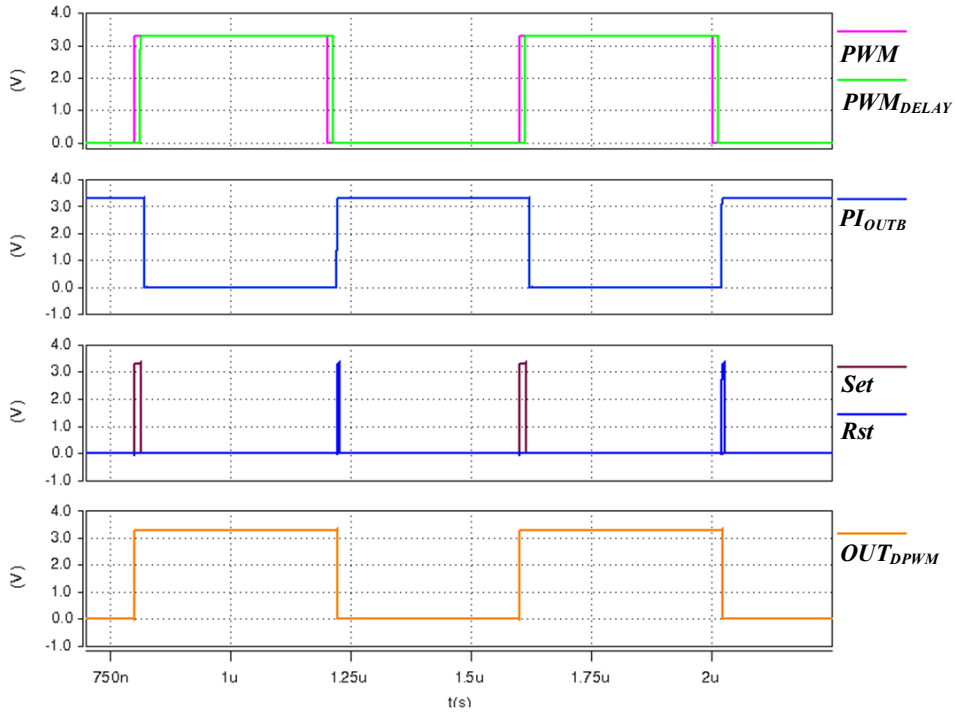


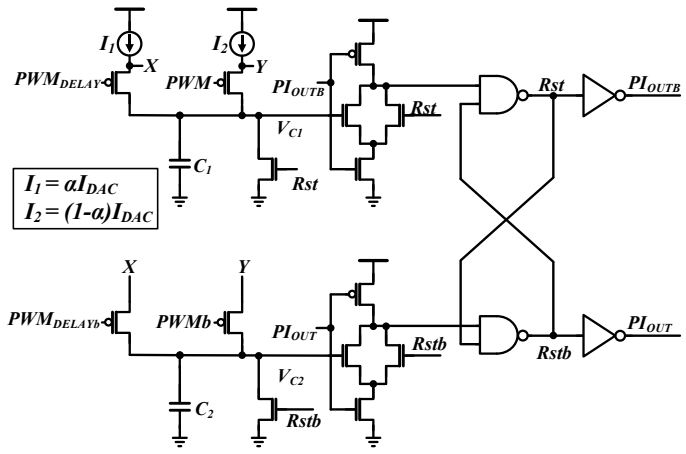
Fig. 3.22. Simulated waveforms of PI-based DPWM.

the two currents (I_1 and I_2) from an M2M-ladder-type current-steering DAC illustrated in Fig. 3.24. The current relation between the current I_1 and I_2 is as follows:

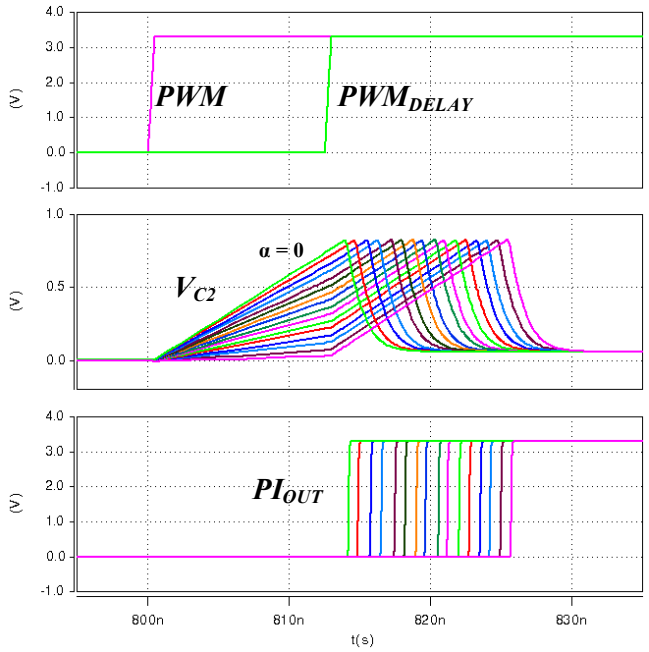
$$I_1 = \alpha \times I_{DAC} \tag{3.27}$$

$$I_2 = (1-\alpha) \times I_{DAC} \tag{3.28}$$

As shown in Fig. 3.23 (b), when the input signal *(PWM*) is logical high and the other input signal PWM_{DELAY} is logical low, the current I_2 charges the shared capacitor C_2, and then if the both input signals become logical high, the two currents simultaneously charge the capacitor C_2. Thus, the phase-interpolated output PI_{OUT} is produced by adjusting the current ratio α between the two currents I_1 and I_2.



(a)



(b)

Fig. 3.23. (a) Schematic and (b) simulated waveforms of the phase interpolator circuit.

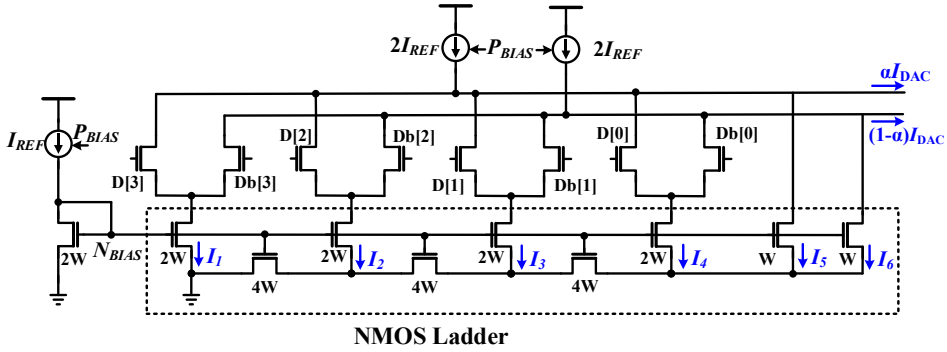


Fig. 3.24. Schematic of an M2M-ladder-type current-steering DAC.

3.3.3.5 DAC and Voltage Level Shifter

The 4-bit current-steering DAC employing an M2M-ladder-type topology is illustrated in Fig. 3.24 [54]. An NMOS ladder provides binary weighted currents $I_N=I_{REF}/2^{N-1}$ (N=1-5, $I_5=I_6$) like an R-2R ladder. The current ratio α is decided by the

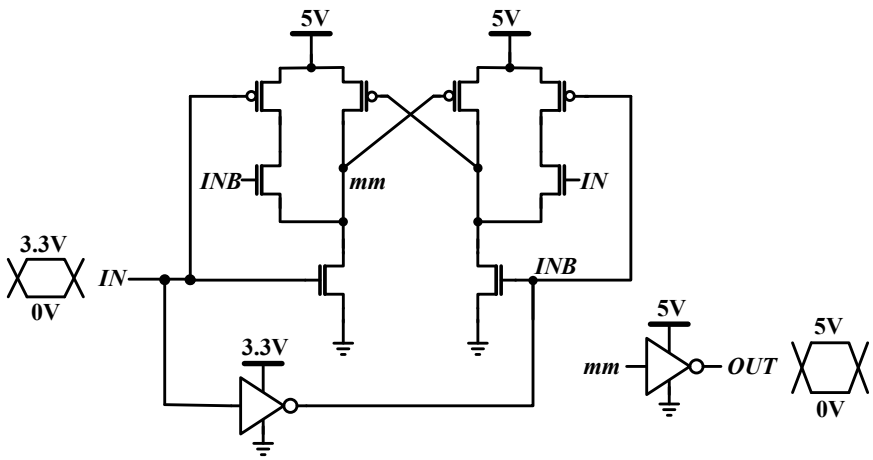


Fig. 3.25. Schematic of a voltage level shifter circuit.

4-bit digital input code D [3:0] from the DLF. A voltage level shifter circuit depicted in Fig. 3.25 is employed to change voltage level from 3.3 V to 5 V because the supply voltage of gate driver is 5V to drive off-chip power transistors which usually require voltage swings from 5 V to 10 V to obtain small on-resistance.

Chapter 4

Experimental Results

4.1 Experimental Setup

A prototype of the proposed LED driver has been implemented using discrete passive components, power transistors, and an on-chip controller IC fabricated in a 0.35 μm CMOS process, which is mounted in a 128-pin thin-quad-flat package (TQFP). Fig. 4.1 shows the photograph of the prototype board and its components are listed in Table 4.1. The numbers marked in the prototype board represents which part they are in the presented LED driver: (1) full-bridge rectifier and EMI filter, (2) floating buck converter for the PFC and energy buffering, (3) floating buck converter for the LED current regulation, (4) prototype controller IC mounted on a socket.

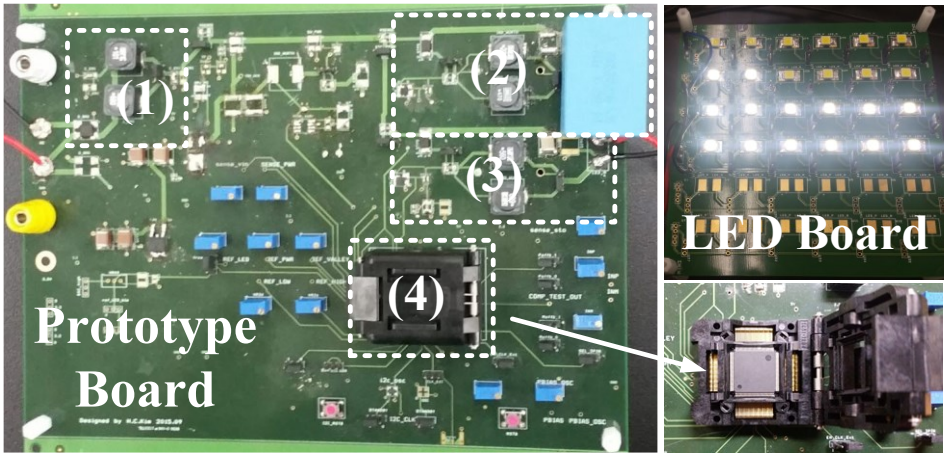


Fig. 4.1. Prototype board of the proposed LED driver.

Table 4.1. List of Components Used in the Prototype LED Driver

Component	Description	Part number
LEDs	CREE XLamp MX-3 LEDs, 3.7 V, 0.35A	MX3AWT-A1
L_1	PFC converter, 22 μH, 5.3 A	7447709220
L_2	Regulating converter, 68 μH, 3.2 A	7447709680
L_F	EMI filter, 100 μH, 2.5 A	7447709101
C_{OUT}	0.47 μF, 250 V, ceramic	GRM55DR72E474KW01L
C_{STO}	68 μF, 250 V, film	B32526R3686K
C_F	EMI filter, 15 nF, 250 V, ceramic	C2012X7R2E153K125AA
R_S	Sensing resistor, 0.5 Ω	CSR1206FKR500
D_1-D_3	Schottcky, 200 V, 2 A	STPS2200UF
Bridge rectifier	Full bridge rectifier, 400 V, 1 A	DSRHD04-13
M_1, M_2	MOSFET N-CH, 200 V, 7 A	BSZ22DN20NS3 G
LDO	3.3V, 0.3A	TPS7A6550QKVURQ1

The photograph of the controller IC is shown in Fig. 4.2 and its characteristics

Table 4.2. Characteristics of the Prototype Controller IC

Process technology	0.35 μm CMOS
Supply voltage	3.3 V (Core), 5 V (IO)
Oscillator frequency range	6.4–64 MHz
Output switching frequency	0.1–1 MHz
Power consumption (at 1 MHz)	33 mW (3.3 V)
	17 mW (5 V)
Active area	2.3 x 1.1 mm^2

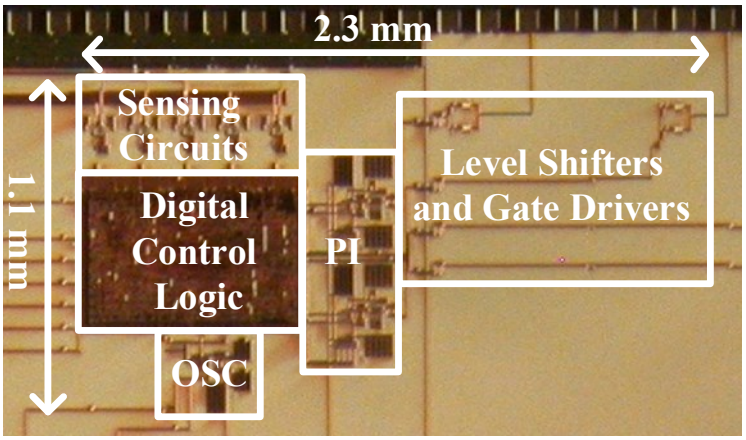
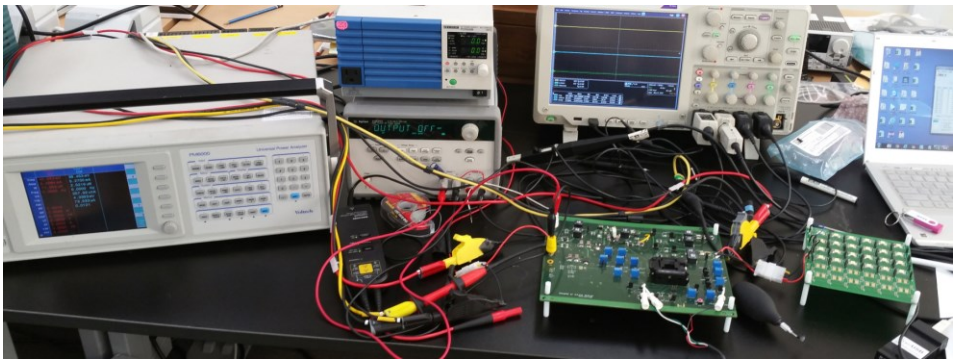


Fig. 4.2. Photograph of the implemented controller IC.

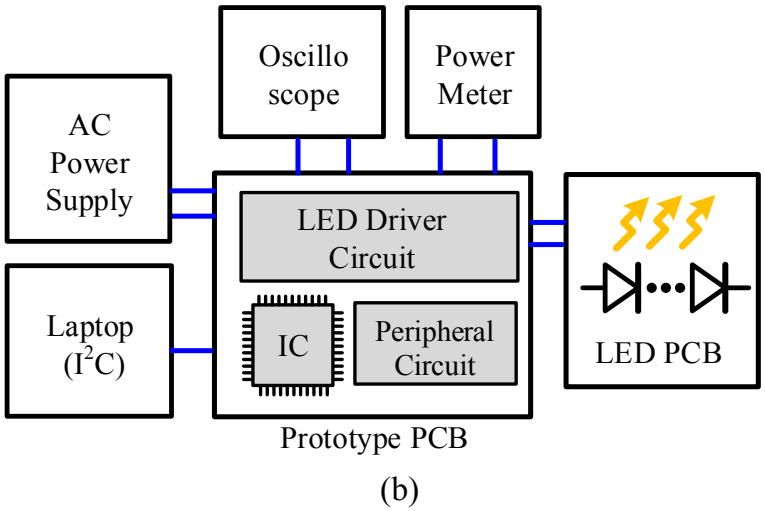
are summarized in Table 4.2. The controller IC consumes 50 mW from a 5 V dc power supply. The die is divided into two voltage domains: 3.3 V domain for core building blocks including the voltage or current sense circuits, digital logic, PI, and an oscillator; 5-V domain for the voltage level shifters and gate drivers. Because the

process design kit supported only 3.3 V pads, the 5 V area was configured with just bond pads, which might be vulnerable to noises from the off-chip power transistors. Hence, we used two pad for one gate driver output because gate driver circuits consumes a large amount of peak current, which may cause voltage noises from bond wire inductances. Moreover, several power and ground pins were inserted among the output signals, which caused the gate drivers to occupy a large portion of the die.

As shown in Fig. 4.3, the prototype LED driver is powered by an ac power supply (Kikusui, PCR500M) and tested at the input voltage of 80–132 V_{rms}. A laptop computer is used to configure the programmable parameters in the digital control logic through an I^2C interface. The voltages and currents are measured using an oscilloscope (Tektronix, DPO5104) with the voltage probes (Tektronix, TPP1000 and THDP0200) and current probes (Tektronix, TCP202 and TCP0030); the power and the power factor are measured using a power meter (Voltech, PM6000).



(a)



(b)

Fig. 4.3. (a) The photograph and (b) block diagram of the experimental setup.

4.2 Measurement Results

Fig. 4.4 shows the measured waveforms of the critical nodes in the proposed LED driver, when delivering 15 W to the LEDs. Fig. 4.4 (a) depicts the ac input voltage and current (v_{ac} and i_{in}); the storage capacitor voltage (v_{sto}) and the positive and negative terminal voltages (v_a and v_b) of v_{sto}. According to the two alternating operating modes, v_{sto} settles to an average voltage of 86.8 V with a ripple voltage of 10.5 V. As shown in Fig. 4.5, the measured minimum V_{sto_AVG} for PF > 0.9 is 56.5 V that is very close to the theoretical limit of 55 V when the input voltage is 110 V_{rms}, as described in Section III. According to [55], IEC 61000-3-2 requires that the third and fifth harmonic currents shall not exceed 86% and 61% of the fundamental current, respectively, for the lighting equipment with an input power lower than or equal to 25 W. Because the measured third and fifth harmonics of the input current (i_{in}) are 21.7% and 17.0% of the fundamental current, respectively, our solution is compliant with some residential LED bulbs and office LED tubes of power less than 25 W. Fig. 4.4 (b) shows the output voltage and the LED current. Regardless of the operating modes, I_{LED} is regulated to 344 mA and the peak-to-peak current ripple (ΔI_{LED_PP}) is 42.7 mA that is equivalent to an LED current ripple of 6.2%.

Fig. 4.6 shows the measured waveforms of the ac input voltage and current (v_{ac} and i_{in}) with a power factor of 0.93 and the currents flowing into each floating buck converter (i_1 and i_2). These waveforms demonstrate that the two converters operating separately, regulate the LED current and perform the PFC function in *Mode* 1; the stored energy in the storage capacitor is delivered to the LEDs without drawing cur-

rent from the ac input source in *Mode* 2. Fig. 4.7 shows the measured waveforms of the proposed ac-dc LED driver when the input voltage is 80 V_{rms} and 132 V_{rms}, respectively. Fig. 4.8 shows the measured close-in waveforms of the ac input voltage and the gate-source voltages (V_{M1} and V_{M2}) and the inductor currents (I_{L1} and I_{L2}), and Fig. 4.9 shows that the waveforms of the inductor currents (i_{L1} and i_{L2}) indicate the DCM operation of the PFC converter and the CCM operation of the regulating converter, respectively.

Fig. 4.10 plots the measured power factor and stored energy ratio (E_{stored}/E_{total}) of the prototype LED driver with an input voltage ranging from 80 to 132 V_{rms}, where the peak power factor is 0.94. Although the power factor is slightly reduced, the graphs of the measured PF and E_{stored}/E_{total} have similar shapes compared to the simulated data in Fig. 3.10. The measured values of power factor are higher than 0.9, which complies with the power factor standards presented in Chapter 1. Fig. 4.11 plots the measured power efficiency, where the peak efficiency is 85.4%. Fig. 4.12 plots the 120 Hz LED current ripple of the proposed LED driver, where the peak LED current ripple is 6.5%, equivalent to a Percent Flicker less than 9.6%. Table 4.3 summarizes the performance of the proposed prototype LED driver in comparison with recent works. Because the required size of C_{STO} depends on the input voltage range of the proposed LED driver, a relatively larger capacitance of 68 μF is employed for C_{STO} to handle the line voltage variations ranging from 80 to 132 V_{rms}. However, if we reduce the design margin of the input voltage range, the size of C_{STO} can be reduced. For example, C_{STO} can be reduced to 20 μF when the input voltage range is 100–132 V_{rms}.

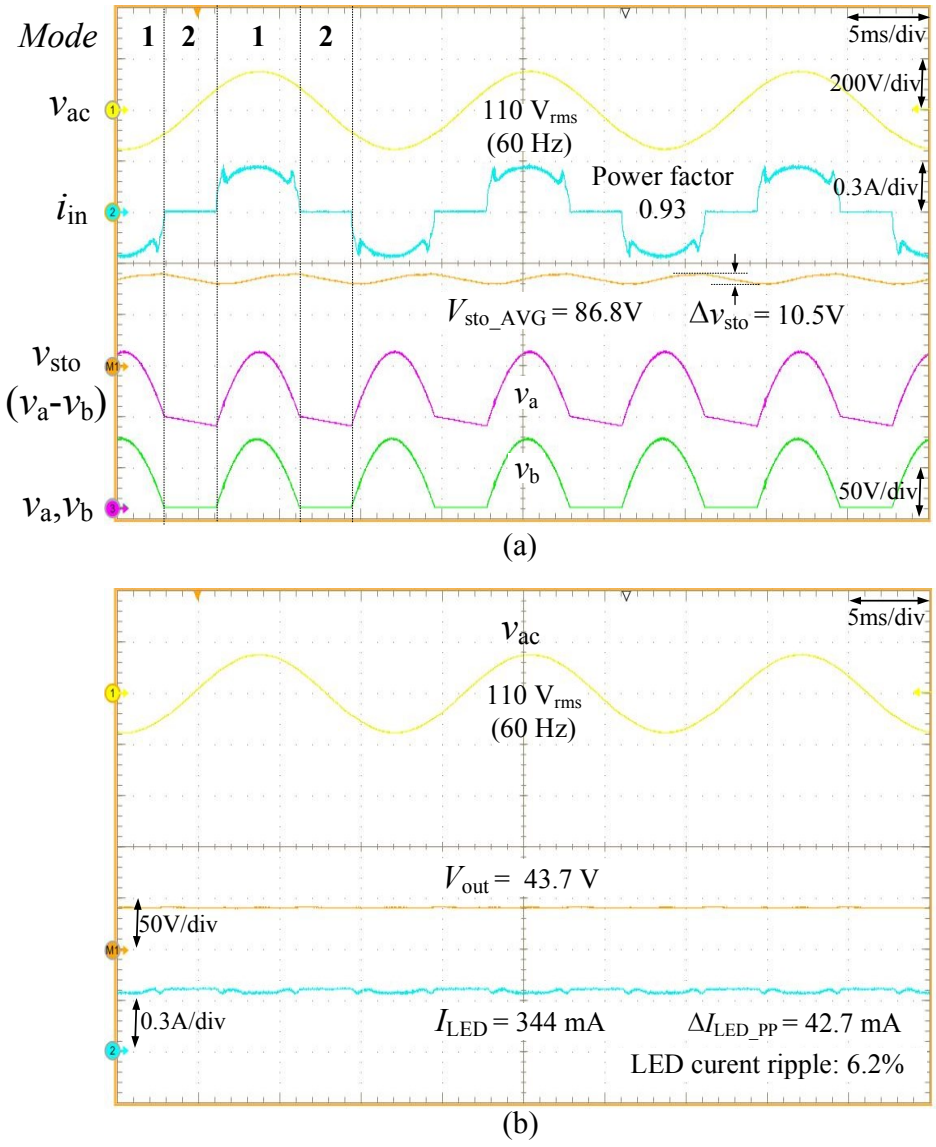


Fig. 4.4. Measured waveforms of the proposed ac-dc LED driver with a two parallel floating buck topology.

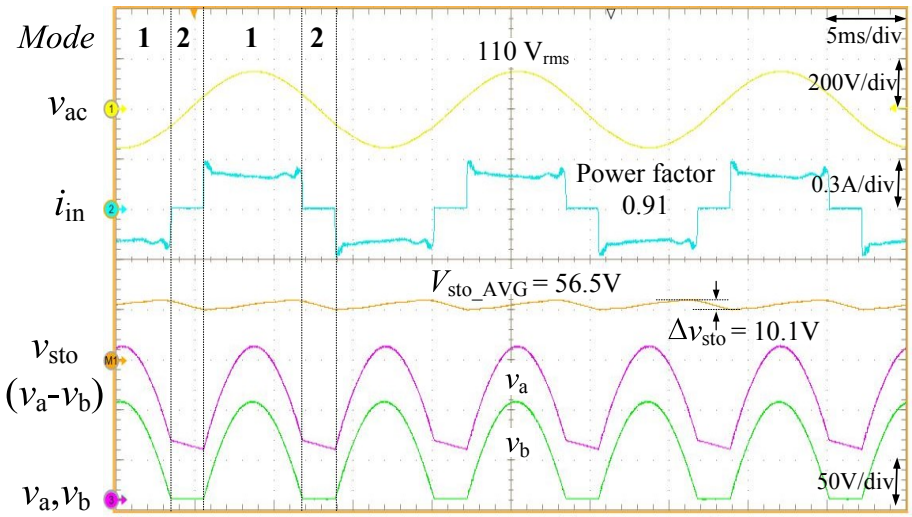


Fig. 4.5. Measured waveforms of the proposed ac-dc LED driver to demonstrate that the minimum V_{sto_AVG} for PF > 0.9 is 56.5 V.

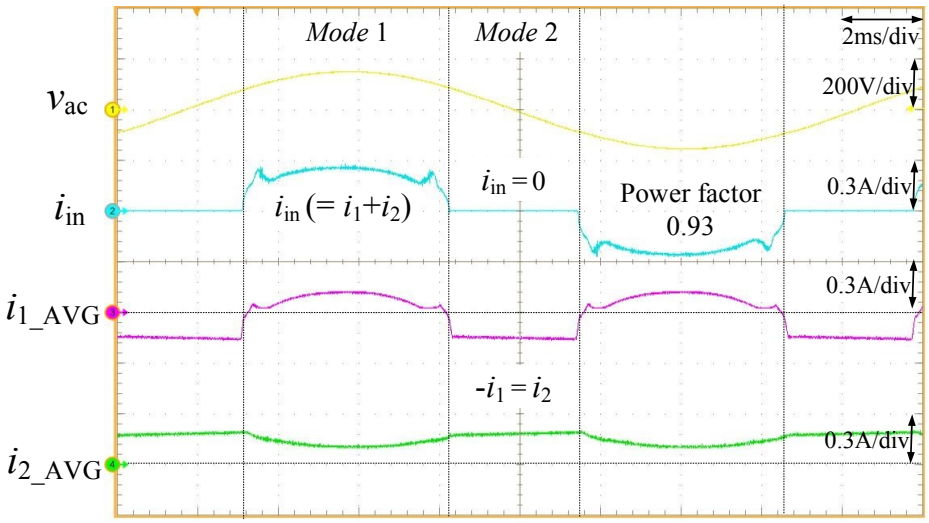


Fig. 4.6. Measured waveforms of the ac input voltage and current (v_{ac} and i_{in}), and the currents flowing into the respective floating buck converters, (i_1 and i_2).

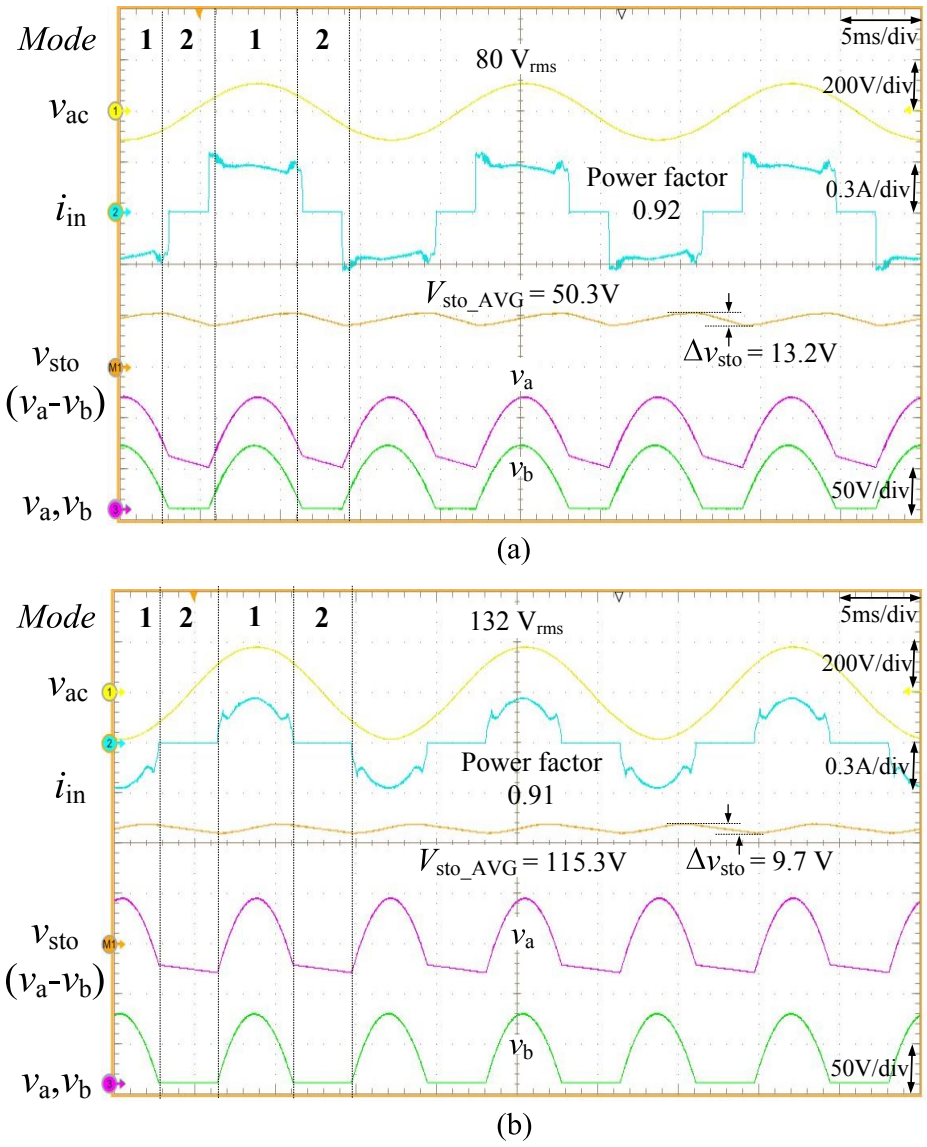
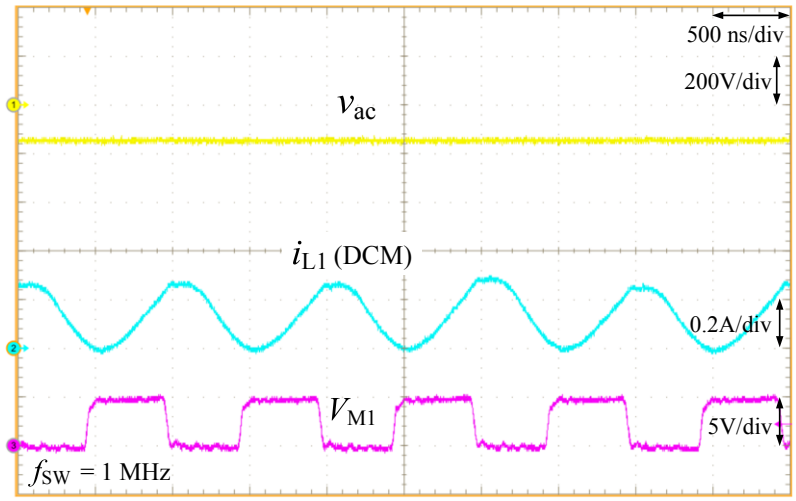
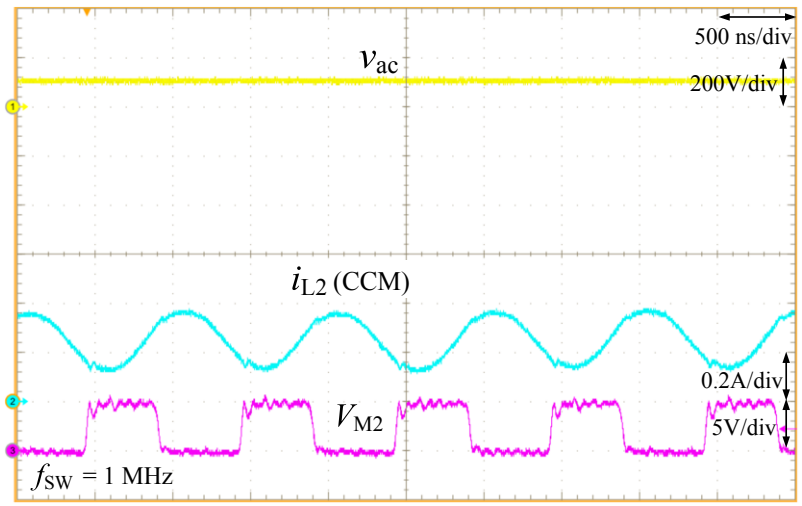


Fig. 4.7. Measured waveforms of the proposed ac-dc LED driver when the input voltage is (a) 80 V_{rms} and (b) 132 V_{rms}.



(a)



(b)

Fig. 4.8. Measured close-in waveforms of the ac input voltage and the gate-source voltages (V_{M1} and V_{M2}) and the inductor currents (I_{L1} and I_{L2}): (a) buck PFC converter (b) regulating converter

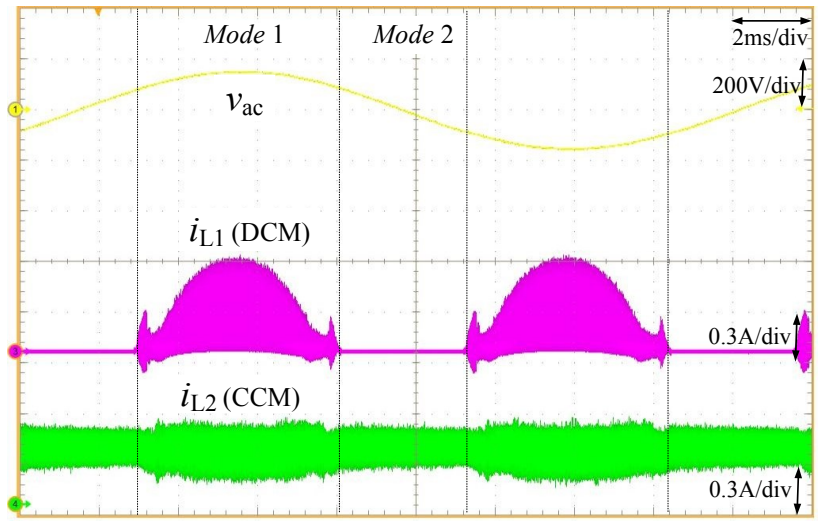


Fig. 4.9. Measured waveforms of the ac input voltage and the currents flowing through the inductors.

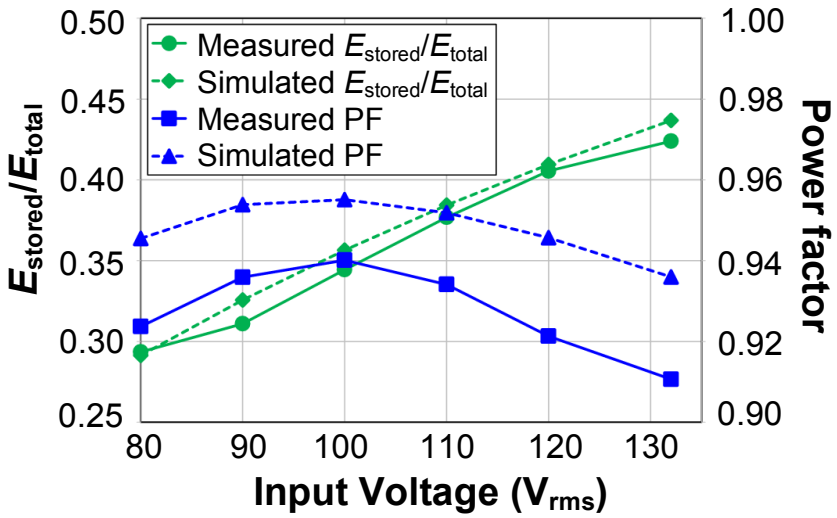


Fig. 4.10. Measured power factor and stored energy ratio (E_{stored}/E_{total}) of the proposed LED driver.

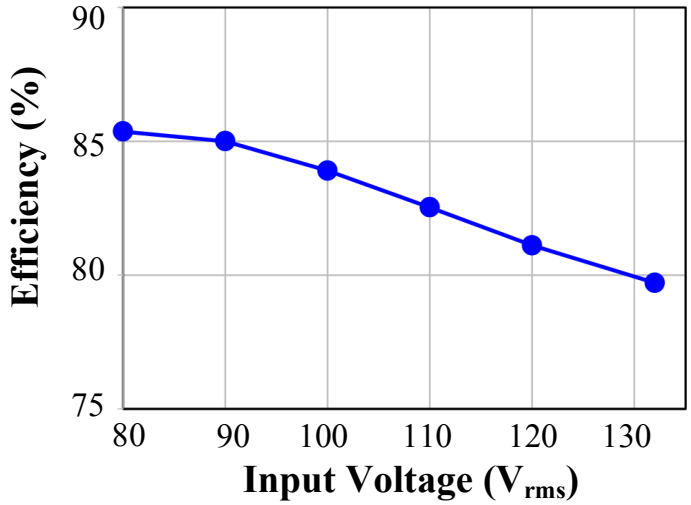


Fig. 4.11. Measured power efficiency of the proposed LED driver.

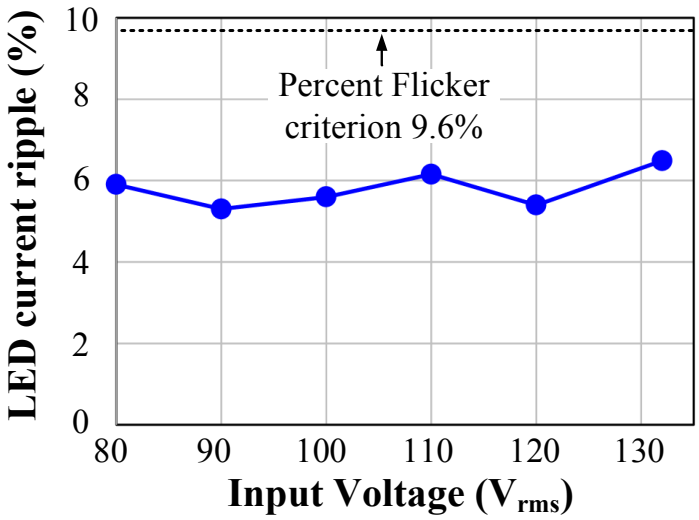


Fig. 4.12. Measured 120 Hz LED current ripple of the proposed LED driver.

Table 4.3. Performance Comparison with State-of-the-art ac-dc LED drivers

	ECCE 2015[15]	TPEL 2015 [23]	TPEL 2016 [25]	TPEL 2014 [28]	JESTPE 2015 [32]	This work
Topology	Cascaded boost PFC + dc-dc LLC	Flyback with harmonic current injection	Boost with harmonic current injection	Flyback with a parallel RCC	Buck-boost with a series RCC	Two parallel inverted buck
Input voltage	90–264 V_{rms}	120 V_{rms}	90–265 V_{rms}	90–264 V_{rms}	110–230 V_{rms}	80–132 V_{rms}
Output voltage	43 V	35 V	420 V	48 V	50 V	43.7 V
Max. output power	150.1 W	20 W	20 W	33.6 W	10 W	15.3 W
Switching frequency	140 kHz	30 KHz	120 kHz	140 kHz	N/A	1 MHz
Inductor	350 μH, 33, 16.5 μH,	1.2 mH	1.1 mH	30 μH, 1.2 mH	985 μH	22 μH, 68 μH
Output capacitor	10 μF (N/A)	500 μF (N/A)	8.8 μF (film)	0.47 μF (N/A)	60 μF, 4.7 μF (ceramic)	0.47 μF (ceramic)
Storage capacitor	30 μF (N/A)	No use	No use	4.7 μF (N/A)	20 μF (ceramic)	68 μF (film)
Power factor	0.97–0.99	> 0.9	0.91	0.99	0.9–0.99	0.91–0.94
Peak efficiency	90.4%	N/A	N/A	87%	87%	85.4%
LED current ripple (120Hz)	18.8%	N/A	10%	8%	5.5%	6.5%
Percent Flicker(1)	N/A	38%	N/A	8.7% (est.)	4.9% (est.)	5.5% (est.)

(1) Estimated values are obtained by using the characteristic graph (forward current vs. relative luminous flux) in each LED datasheet.

Chapter 5

Conclusion

An ac-dc LED driver that can drive the LEDs with the low-risk levels of flicker has been presented in this study. A two parallel floating buck topology is proposed to achieve a high power factor and a low LED current ripple. The PFC converter buffers the twice-the-line-frequency energy, while simultaneously performing the PFC function and the regulating converter provides a constant current to the LEDs. Further, the proposed architecture reduces the voltage stress and size of the storage capacitor, thereby, a film capacitor can be used instead of the limited life-time electrolytic capacitor. The relationship between the input power factor and the stored energy ratio in accordance with the storage capacitor voltage, to achieve a high power factor and efficiency, is discussed in this study. A 15 W prototype LED driver has been implemented and tested to validate the design of the proposed ac-dc LED driver, exhibiting a power factor of 0.94 and a power efficiency of 85.4%.

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초 록

본 논문에서는 두 개의 평행한 벅 컨버터로 구성된 교류-직류 엘이디 구동 회로를 제안한다. 입력 교류 주파수의 2 배의 성분을 가지는 에너지의 영향을 완화 시키기 위하여, 하나의 플로팅 (또는 인버티드) 벅 컨버터는 저장용 커패시터에 에너지를 전달한다. 다른 플로팅 벅 컨버터는 플리커를 낮은 위험수준으로 줄이기 위해 엘이디가 일정한 밝기를 유지할 수 있도록 엘이디 전류를 조정한다. 제안하는 구조는 저장용 커패시터의 크기와 가해지는 양단 전압의 크기를 줄여주기 때문에, 전해 커패시터 대신 필름 커패시터의 사용을 가능하게 해준다. 역률과 플리커 표준들을 고려하여, 높은 역률을 달성하면서 동시에 저장용 커패시턴스 크기와 엘이디 전류 리플을 최소화 하기 위한 설계 과정이 제시된다. 제안하는 엘이디 구동회로의 시제품은 0.35-μm CMOS 공정으로 제작된 온칩 제어 집적회로와 함께 구현 되었고, 시제품의 기능과 성능은 실험적으로 검증 되었다. 실험 결과에 따르면, 15W 의 전력을 엘이디에 전달하면서, 0.94 의 역률, 최대 85.4%의 전력 효율과 6.5%의 엘이디 전류 리플을 달성하였다.

주요어 : 교류-직류 변환, 엘이디, 엘이디 구동회로, 벅 컨버터, 플로팅 벅 컨버터, 인버티드 벅 컨버터, 역률 보정, 디지털 펄스 폭 변조

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