PH.D. DISSERTATION

PERFORMANCE ENHANCING TECHNIQUE FOR THE SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERTER

축차 비교형 아날로그-디지털 변환기의 성능 향상을 위한 기법에 대한 연구

BY

HYONGMIN LEE

AUGUST 2016

DEPARTMENT OF ELECTRICAL ENGINEERING AND
COMPUTER SCIENCE
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

PERFORMANCE ENHANCING TECHNIQUE FOR THE SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERTER

축차 비교형 아날로그-디지털 변환기의 성능 향상을 위한 기법에 대한 연구

지도교수 김 수 환

이 논문을 공학박사 학위논문으로 제출함

2016 년 8 월

서울대학교 대학원

전기컴퓨터 공학부

이 형 민

이형민의 공학박사 학위논문을 인준함

2016 년 8 월

위 원 장 : _____(印)
부위원장 : _____(印)
위 원 : _____(印)
위 원 : _____(印)
위 원 : _____(印)

ABSTRACT

PERFORMANCE ENHANCING TECHNIQUE FOR THE SUCCESSIVE APPROXIMATION ANALOG-TO-DIGITAL CONVERTER

HYONGMIN LEE
DEPARTMENT OF ELECTRICAL ENGINEERING AND
COMPUTER SCIENCE
COLLEGE OF ENGINEERING
SEOUL NATIONAL UNIVERSITY

This thesis is written about a performance enhancement technique for the successive-approximation-register analog-to-digital converter (SAR ADC). More specifically, it focuses on improving the resolution of the SAR ADC. The basic operation principles and the architecture of the conventional SAR ADC is examined. To gain insight on areas of improvement, a deeper look is taken at the building components of the SAR ADC. Design considerations of these components are discussed, along with the performance limiting factors in the resolution and bandwidth domains. Prior works which challenge these problems in order to improve the performance of the SAR ADC are presented. To design SAR ADCs, a high-level modeling is presented. This model includes various non-ideal effects that occur in the

design and operation. Simulation examples are shown how the model is efficient and useful in the initial top-level designing of the SAR ADC. Then, the thesis proposes a technique that can enhance the resolution. The SAR ADC using integer-based capacitor digital-to-analog converter (CDAC) exploiting redundancy is presented. This technique improves the mismatch problem that arises with the widely used split-capacitor structure in the CDAC of the SAR ADC. Unlike prior works, there is no additional overhead of additional calibration circuits or reference voltages. A prototype SAR ADC which uses the integer-based CDAC exploiting redundancy is designed for automotive applications. Measurement results show a resolution level of 12 bits even without any form of calibration. Finally, the conclusion about the operation and effectiveness on the proposed technique is drawn.

Keywords: successive-approximation-register(SAR) ADC, integer-based split-capacitor DAC, redundancy, automotive applications

Student Number: 2010-30228

CONTENTS

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

The successive-approximation-register analog-to-digital converter (SAR ADCs) is one of the hottest and arguably the most widely used ADC in the market today. It is well-known for its low-power characteristics and simple structure. The history of the SAR ADC goes back decades. The concept is very straight-forward; it is based on binary searching. The name “successive-approximation-register” therefore comes from the way the logic (registers) operates in a successive manner. However, until quite recently, the Nyquist ADC market have been dominated by other types of ADCs. Flash ADCs have been widely used for high-speed low resolution applications. The flash ADC is extremely fast due to a single stage of comparison for an analog-to-digital conversion. The sampled signal is compared to a series of reference voltages simultaneously by multiple comparators and the digital outputs are generated at the same time. The power consumption is inevitably high, but the flash ADC has its very

strong characteristic that stands out. Applications that require moderate-to-high resolutions typically have adopted the pipeline ADC. The pipeline ADC, has a nice balance between resolution and operation bandwidth. A sampled signal is compared to a reference voltage, and then the difference is multiplied, and the resulting voltage is sent to the consecutive stages. The pipeline ADC achieves moderate-to-high resolutions due to the multiple multiplying digital-to-analog converter (MDAC) stages which use operating amplifiers in the converting operation. Moreover, the operation bandwidth is relatively high in the region of tens of MHz up to the low hundreds due to the stages working in a 'pipeline' manner, hence the name. These serial stages that generate each digital bit progressively allow the throughput to be equal to the sampling frequency. This is a very powerful and effective advantage of the pipeline ADC. For example, the cyclic ADC works with the sample operating principles, but the difference is that there is only a single MDAC which is used repeatedly. Therefore, the throughput of the ADC is much slower - almost 1/N times for an N-bit resolution - as one sample must be iterated for N cycles. The downside of the pipeline ADC is the excessive power consumption of the MDAC stages, but nevertheless the pipeline ADC has dominated the market of Nyquist ADCs until recently.

The SAR ADC, although the history is quite long, has been left in the cold until recently. Although the SAR ADC has a very simple structure and straightforward operation principles, the major drawback is the resulting inherent operation bandwidth limit. As will be explained in detail in the following sections ahead, the SAR ADC

converts analog signals to digital codes by conducting a binary search. The generation of the digital bits are done at a single bit at a time. Unlike the pipeline ADC, however, the SAR ADC has no method of manipulating the value of the charge of the sampled signal, due to the lack of op-amps. Therefore the proceeding sampling sequence must wait until all the digital bits are generated, which results in an ADC operation bandwidth which is 1/N times lower than compared to the pipeline counterpart. This limitation in the operation speed has cut down the value of the SAR ADC until quite recently. The only non-trivial advantage that the SAR ADC held in the early days was that the power consumption in the analog domain was extremely low compared to other ADCs, and this was due to the absence of op-amps and numerous comparators. But the digital logics that comprise the SAR ADC was too costly and slow for practical usage.

The SAR ADC began to gain be reevaluated, however, as the technology continued to develop. In the analog circuit designer point of view, the technology development is in some aspects unwelcome. This is mainly due to the process scaling issue where the supply voltage continues to decrease yet the threshold voltage decrease of the transistor cannot keep up. A typical problem that arises is that with finer technology, it becomes harder and harder to reach gain levels that were met with larger scaled processes. This effects the development of the pipeline ADC, and the performance enhancement due to technology scaling was not as significant as that of digital circuits. On the contrary, the SAR ADC hardly suffers at all from these problems, since the analog circuitry required is mainly a comparator and capacitor arrays and

switches, and therefore quite friendly to technology scaling. Moreover, due to the speed-up of the digital logic, the successive binary-search algorithm could be now carried out more quickly, thus diminishing the operation bandwidth disadvantage. Nowadays, the SAR ADC is actively being used in applications that require moderate bandwidth and high resolution, which traditionally used pipeline ADCs. The low-power characteristics are becoming more important than ever as the supply voltages are continuously dropping. This can be explained by the plot of the ADC architecture versus the resolution and sampling rate shown in Fig. 1.1.1 [1.1.1]. The SAR ADC is currently or potentially replacing the mid-range performance domain that traditionally

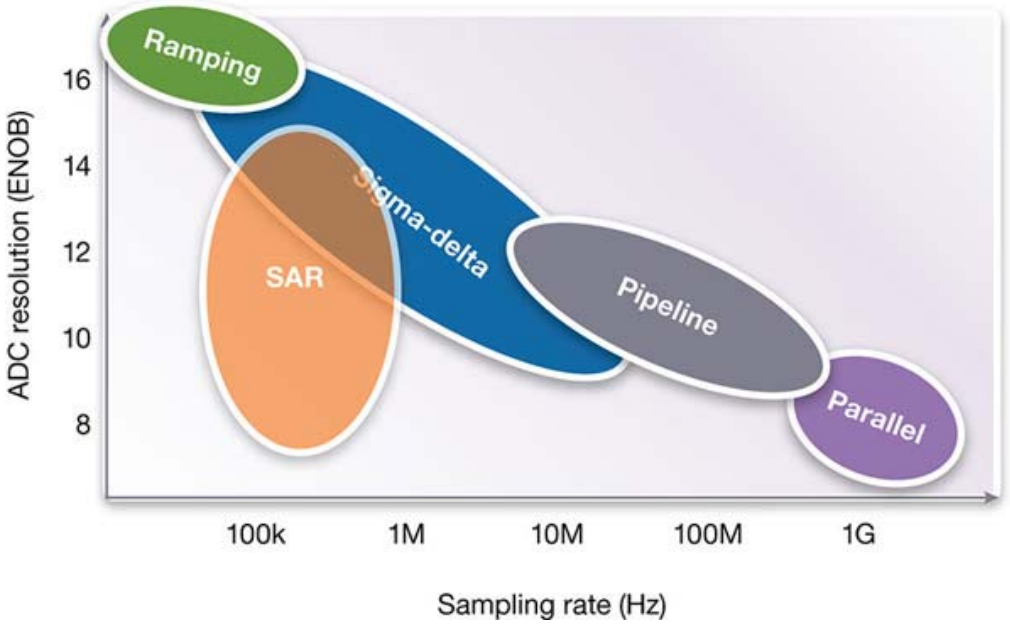


Fig. 1.1.1 Plot of ADC architecture versus the resolution and sampling rate [1.1.1].

was dominated by the pipeline ADC. The SAR ADC can achieve resolutions over ten bits and more and sampling rates of a few tens of MHz.

This thesis focuses on the performance enhancement of SAR ADCs for further potential replacement of the pipeline ADC. Using a finer technology will obviously increase the performance without doubt, but the cost may be limited or other circumstances may allow only the use of less finer processes. Therefore, this thesis presents a technique that enhances the resolution of the ADC. The technique is named "SAR ADC using integer-based capacitor digital-to-analog converter (CDAC) exploiting redundancy", and focuses on reducing the mismatches in the CDAC of the SAR ADC in order to prevent resolution degradation. A prototype SAR ADC for automotive applications is designed and presented.

1.2 THESIS ORGANIZATION

The thesis is organized as follows. The introduction is in Chapter 1, where the motivation and the organization of the thesis is shown. In Chapter 2, the conventional SAR ADC will be covered. The contents include the characteristics and operation principle of the typical SAR ADC, and also the limitations and the critical design consideration points. To gain insight on how to enhance the performance, the trend prior works of the development of the SAR ADC will be discussed. Chapter 3 will show a MATLAB model of the SAR ADC which was actually used in the top-level

design stage. Weight distribution, redundancy, the structure of the CDAC and the non-idealities will be covered and their effects shown by simulation results. In Chapter 4, the technique in performance enhancement of the SAR ADC proposed by this thesis is presented. It is designed for automotive applications, so the background of the automotive solution will be described. Then, the “the integer-based capacitor digital-to-analog converter (CDAC) exploiting redundancy” will be illustrated in detail. The actual design of the SAR ADC will be demonstrated with simulation and measurement results. Finally, the conclusion and discussion of future work is given in Chapter 5.

CHAPTER 2

CONVENTIONAL SUCCESSIVE-APPROXIMATION-REGISTER ANALOG-TO-DIGITAL CONVERTERS

2.1 INTRODUCTION

In this chapter, the successive-approximation-register analog-to-digital converter (SAR ADC) will be described in a typical sense. Background information on the SAR ADC will be described in detail, including the operation principle and the basic structure so that a general knowledge on the concept of the SAR ADC will be delivered. Moreover, the building blocks that comprise the ADC will also be discussed in further detail. These include the capacitor digital-to-analog converter (CDAC), the comparator, and the digital control logic. Based on this information, the following sections will take a deeper look into the design considerations that must be carefully considered in the implementation of the SAR ADC for each block. The performance limiting factors will also be examined, as these problems are the motivations for improvement. These

examinations will be given in aspects of resolution and operation speed. The resolution degrading factors include the under-settling of the CDAC, mismatch and parasitic capacitance and other non-linearities in the CDAC, and comparator issues such as kick-back noise, memory effects, and the intrinsic circuit noise. The operation speed limitations are broken down to respective causes; the settling of the CDAC, the comparator decision time, and the logic delay. Prior works which develop the conventional SAR ADC into higher-performing converters is studied in the final sections of the chapter. Widely-used techniques such as the split-capacitor DAC and implementation of redundancy will be discussed.

2.2 OPERATION PRINCIPLE OF THE CONVENTIONAL SAR ADC

2.2.1. OVERVIEW OF THE OPERATION

The principle of the operation of the SAR ADC is based on the binary search algorithm. The closest digital representation of the analog signal value is determined by N binary search stages for an N-bit resolution ADC. The conversion can be divided into two phases; the sampling phase and the conversion phase. These two phases comprise the period of the conversion time, and therefore determine the sampling frequency of the ADC. In the sampling phase, the main objective is to store the analog input signal information into the sampling capacitor. Once the input signal information

is sampled with errors less than the intended resolution, the conversion phase begins. In the phase, the input signal information is compared with reference voltages in a binary search manner. For example, if the range of the input is from zero to one for simplicity, the input is first compared with 0.5. Then depending on the output, the input value is then compared with 0.25 if the previous comparison result was low, or 0.75 if the previous comparison result was high. The step of the change in the reference voltage is 0.25. In the next conversion stage, the reference voltage will change by 0.125 in the direction determined by the previous comparison result. This conversion stage is repeated and the digital representation of the input signal is the collection of the sequential comparison results.

Compared to the pipeline ADC, it is quite similar that the conversion process is processed one bit at a time in a binary manner. The difference is that while the pipeline ADC converts multiple samples at a single time, the SAR ADC converts only a sample at once. This is due to the fact that the SAR ADC cannot supply extra charge to the sampled charge. The voltage of the CDAC given by the sampled input is only manipulated through charge redistribution among the capacitors in the CDAC array. Therefore, for a sampled input, the whole conversion process must be finished before the next input can be sampled. This is unlike the pipeline ADC, where the transfer of charge is achieved by the use of amplifiers.

2.2.2. SAMPLING PHASE

In the sampling phase, the input signal is sampled onto the sampling capacitor and the charge is stored. The input is sampled onto the sampling capacitor at the bottom-plate, whereas the top-plate is grounded to the common-mode voltage. A simple figure illustrates this procedure with simple block diagrams in the Fig. 2.2.1. Here, the sampling capacitor is the sum of all the capacitors of the CDAC. Therefore, the total size of the sampling capacitor C_s would be 2^N C. The charge stored in the sampling capacitor can be given by the equation 2.2.1.

$$Q_S = C_S \times (V_{com} - V_{in}) . \tag{2.2.1}$$

Q_s is the charge sampled onto the sampling capacitor with respect to the top-plate of the sampling capacitor, namely the output of the CDAC. C_s is the capacitance of the

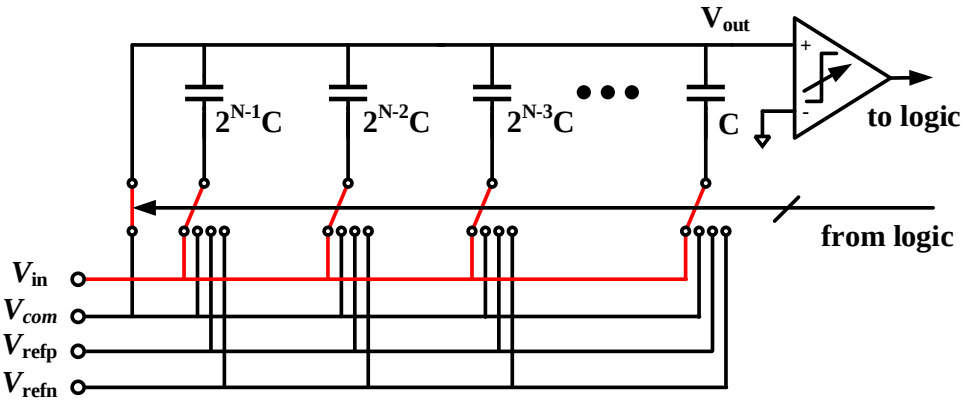


Fig. 2.2.1 Sampling phase operation of the SAR ADC.

sampling capacitor, V_{com} is the common-mode voltage, and the V_{in} is the sampled input voltage. This is the ideal case, and actually there will be some deviation from this ideal value due to the settling of the capacitor. The incomplete settling is caused by the finite resistance of the sampling switch, which generates an RC delay in accordance with the sampling capacitor. For the performance to match the full specified resolution, the error due to this incomplete settling must be smaller than half the least significant bit (LSB) size so that it is not larger than the quantization noise. Detailed discussion on the incomplete settling will be done in the following chapter. When the input is fully sampled onto the sampling capacitor, the DAC is now ready to redistribute the charge according to the comparator output. All switches are turned off, and the capacitor is left floating, which ideally would conserve the charge indefinitely.

2.2.3. CONVERSION PHASE

After the sampling phase has concluded, the conversion phase can now take place. Since the charge in the capacitors are now trapped, the total charge will remain unchanged for this sample due to the electrical charge conservation law. The idea now is to manipulate the voltage seen at the output of the CDAC by switching the reference voltages at the other side of the capacitors, namely the bottom-plates. Initially, the bottom-plates are all connected to V_{COM}, which is the common-mode voltage of the input range. Thus, the voltage at the output of the CDAC, V_{out}, is given by the following

equation:

$$V_{out} = V_{com} + \frac{Q_s}{C_s}. \tag{2.2.2}$$

The charge Q_s in the sampling capacitors is defined by equation (2.2.1), and solving for these two equations gives the output voltage of the CDAC to be,

$$V_{out} = 2V_{com} - V_{in}. \tag{2.2.3}$$

Therefore, the output of the DAC is a linear function of the sampled input voltage. The simplified block diagram of this step is shown in Fig. 2.2.2. The CDAC output voltage is then compared with V_{com}, and the comparator result is the first bit of the analog-to-digital conversion. For example, let's assume that the sampled input was a very small signal close to zero. Then, the output voltage of the CDAC according to equation (2.2.3) would be close to $2*V_{Com}$, and comparing this with V_{com} would result in a positive

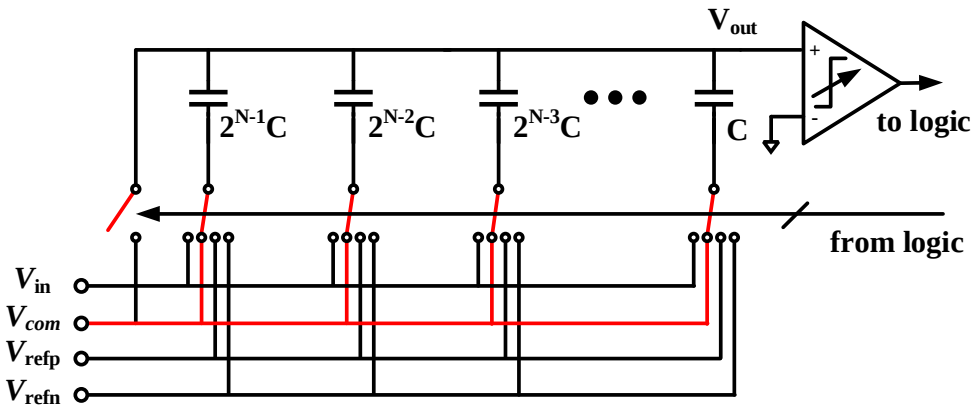


Fig. 2.2.2 First conversion phase operation of the SAR ADC.

output. Due to the bottom-plate sampling, the signal of the sampled input V_{in} is negative, and therefore a positive output is the same as '0' for the most significant bit (MSB).

Next, the bottom-plate of the largest capacitor in the CDAC is switched from V_{COM} to either the top reference voltage of the bottom reference voltage. The capacitors comprising the CDAC and therefore the sampling capacitor are weighted in a binary manner in the conventional SAR ADC, and therefore the capacitance value of the largest capacitor is half of C_s. This procedure results in the output voltage of the CDAC as given in the following equation:

$$V_{out} = \frac{1}{2}(V_{com} - V_{refp}) + \frac{Q_s}{C_s}, \text{ (when MSB = 0)}$$

$$V_{out} = \frac{1}{2}(V_{com} - V_{refn}) + \frac{Q_s}{C_s}, \text{ (when MSB =1)} \quad . \tag{2.2.3}$$

V_{refp} and V_{refn} are respectively the top and bottom values of the reference voltage. The block diagram of this is illustrated in Fig. 2.2.3, with the input signal the same as the previous example. This output voltage is again compared with the common-mode voltage, and it can be easily seen that again, the comparator output will result in a positive output, which means '0' for the 2nd MSB as well.

Once a capacitor stage of the CDAC is switched to a reference voltage, it is held until the whole conversion is over. The following stage now switches the bottom-plate of the 2nd capacitor to either V_{refp} or V_{refn}, according to the comparator output of the previous cycle. This process is carried out until all the bits are generated, and thus the

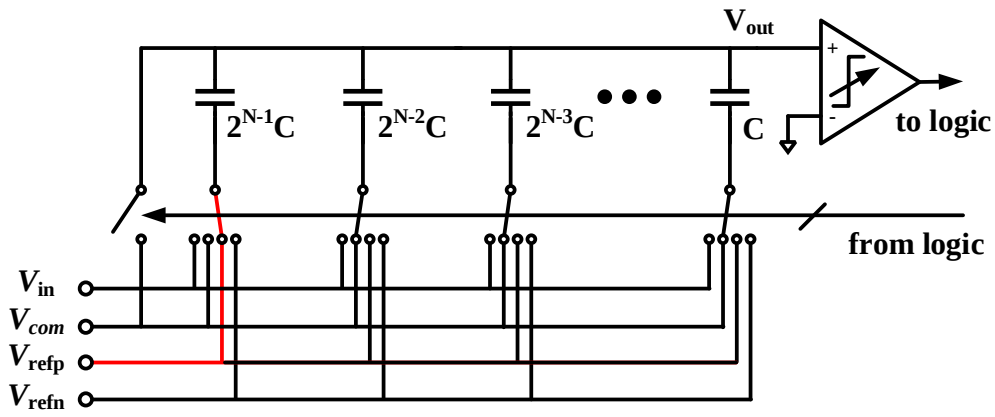


Fig. 2.2.3 Second conversion phase operation of the SAR ADC.

conversion of a single input sample is complete. A 6-bit example waveform with an input close to zero as explained above is shown in Fig. 2.2.4. It can be seen that as the conversion phases proceed, the DAC output voltage V_{out} seems to converge to V_{com}. This is exactly the case, since the input has been bottom-plate sampled onto the CDAC.

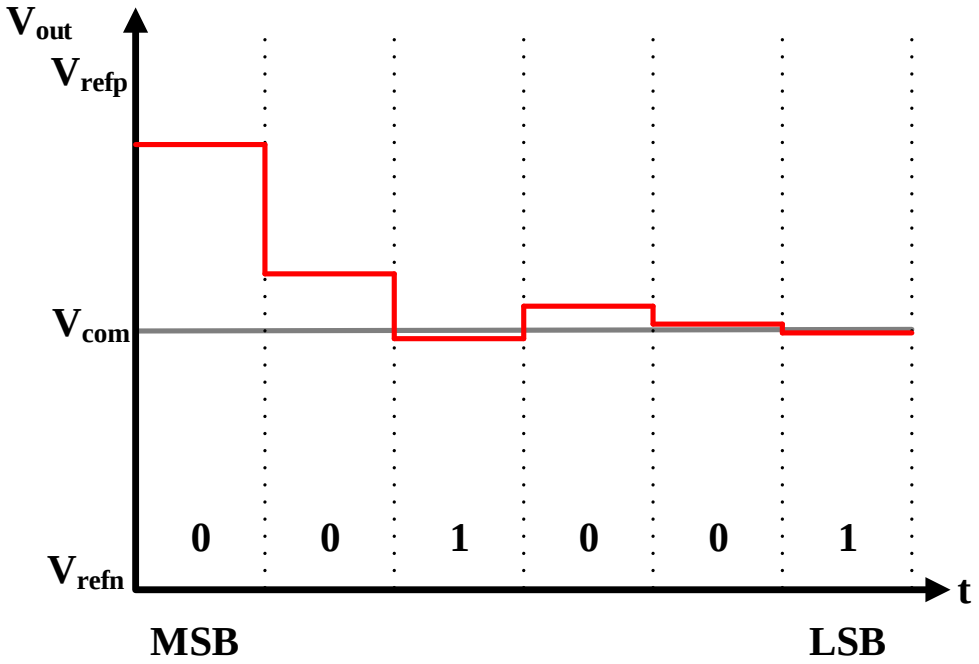


Fig. 2.2.4 Conversion phases waveform example for a 6-bit SAR ADC.

2.3 STRUCTURE OF THE CONVENTIONAL SAR ADC

2.3.1. FULL STRUCTURE OF THE CONVENTIONAL SAR ADC

One of the main advantages of the conventional SAR ADC is the simple architecture. It can be divided into three main blocks; the CDAC, the comparator, and the control logic. A block diagram of the full structure is shown in Fig. 2.3.1. The

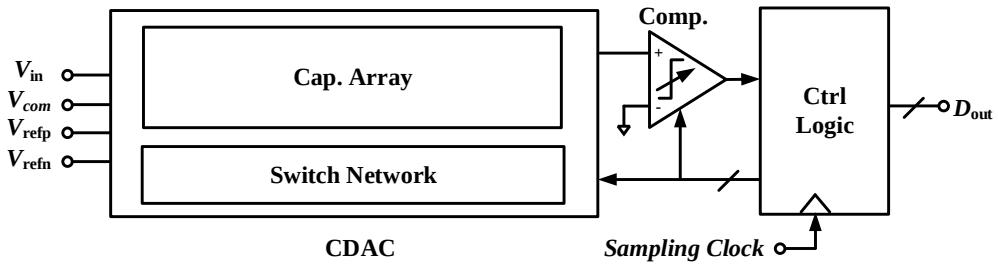


Fig. 2.3.1 Block diagram of the conventional SAR ADC including the CDAC, the comparator, and the control logic..

CDAC is the heart of the analog process in the analog-to-digital conversion. The track-and-hold circuit which is commonly used in ADCs is merged with the CDAC because both are capacitive in nature. Sampling the input and the manipulation of the output voltage for binary-searching is carried out in this block. The sampling capacitor and the CDAC is typically merged into one structure for a more compact and simple architecture. The analog output is connected to the input of the comparator.

The main function of the comparator is to decide whether the output of the CDAC is larger or smaller than the reference voltage in the binary search algorithm, and send this information to the logic. The comparator can be seen as the transition block between the analog domain of the CDAC and the digital domain of the control logic block. The output of the comparator is sent to the control logic.

The control logic serves three main purposes. First, it provides the clocking signals that are fed to the CDAC and the comparator for the interactive operation of the sampling and conversion cycles. It should be noted that the internal clocking signals

are over N times faster than the sampling frequency of the ADC for an N-bit resolution, and therefore the internal clocking should be considered as a high-speed digital circuit. The second function of the control logic block is the generation of the negative feedback control signals to the CDAC for the binary search operation. Based on the comparator decision for the current conversion cycle, the control logic generates the control signals for the next cycle that manipulates the switches in the CDAC to connect the relevant reference voltages for the binary search operation. The final function is the digital error correction, which refers to the generation of the final digital output bits of the ADC.

2.3.2. CAPACITOR DIGITAL-TO-ANALOG CONVERTER (CDAC)

The capacitor digital-to-analog converter (CDAC) is the key block in defining the specifications of the SAR ADC. Depending on the design, the performance is decided. Fig. 2.3.2 shows the schematic of the conventional CDAC. It is typically designed in a symmetrical differential structure, but for simplicity the schematic shows the single-ended version. The CDAC is comprised of the capacitor array and the switch network. No static current is drawn in the CDAC.

The capacitor array is comprised of binary-weighted capacitors with the top-plates connected together as the output node. The bottom-plates of the capacitors are connected to the respective switches in the switch network. Bottom-plate sampling is

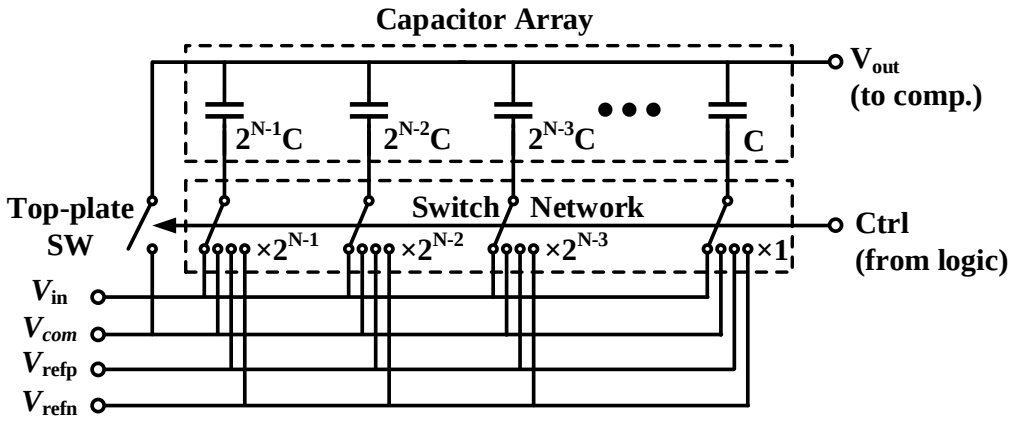


Fig. 2.3.2 Block diagram of the CDAC, including the capacitor array, the switch network, and the top-plate switch.

commonly used in high-resolution ADCs because it is very robust to parasitic capacitance in the CDAC. Also, charge injection that occurs when sampling the input does not affect the sampled value if the switching clocks are operated properly. The size of the capacitors affect the resolution and the power consumption of the SAR ADC. First of all, the capacitors of the CDAC also act as the sampling capacitor of the ADC, and therefore the total sum of the capacitors is bound by the kT/C noise limit. However, for high-resolution SAR ADCs, the binary-weighted capacitor array imposes a much higher lower-limit to the size of the capacitors. For example, a 12-bit resolution SAR ADC would need a total unit capacitor number of 4096. If the unit capacitor size is 10 fF, which is quite small even considering recent technologies, the total capacitance would be 40 pF, which would be quite too large for practical cases, while the kT/C

noise limit of the sampling capacitor is under 1 pF. However, if the unit capacitor value is too small, then there will be mismatch problems. For example, if the sampling capacitance is 1 pF for a 12-bit resolution SAR ADC, then the unit capacitor size would now be about 250 aF, which will have serious mismatch issues. It is known that the physical dimensions of a capacitor are inversely proportional to mismatch. The standard deviation of the mismatch that occurs in a capacitor can be shown as the following equation,

$$\sigma(\frac{\Delta C}{C}) = \frac{A_C}{\sqrt{WL}}, \tag{2.3.1}$$

where C is the capacitance value, A_c is the process-dependent Pelgrom coefficient, and W and L are the physical dimensions of the capacitor. From this equation, it can be seen that the capacitor size must be increased for higher resolution, and therefore there is a tradeoff between both the settling time and the power consumption of the CDAC versus the resolution. Techniques that alleviate this trade-off will be explored in the following section in this chapter.

The switch network is the connection between the capacitor array and the input signals or reference voltages. As can be seen from the block diagram of the CDAC above in Fig. 2.3.2, there are three reference voltages in the block diagram: a high reference V_{refp}, a low reference V_{refn}, and the common voltage V_{com}. This structure is commonly called the V_{cm}-based switching, and offers such advantages as low-power characteristics and symmetrically distributed redundancy centering the decision level,

for the cost of an extra reference voltage [2.3.1]. There are four switches at the bottom-plate of per capacitor stage in the CDAC; the input sampling switch and switches that connect to the three reference voltages. Bootstrapped switches are commonly used for the input signal sampling switches for high-performance ADCs [2.3.2]. This not only allows a relatively constant on-resistance of the sampling switch for different voltage levels of the input signal, it also allows to design the switches smaller, instead of CMOS switches with large dimensions. The physical size of the switches are of importance because for a capacitor stage, because not only are there four switches per capacitor, the switch sizes must be linear with the capacitor size in order for the fast settling of the CDAC [2.3.3]. The switch sizes are drawn next to the switches in the Fig. 2.3.2. This becomes a non-trivial issue as the binary-weight of the CDAC exponentially increases the capacitor sizes to very high values, especially in high-resolution SAR ADCs. For example, even if a minimum-sized transistor was used as the switch for the unit capacitor for the LSB, the MSB capacitor would be 2048 times larger, and therefore the resistance of the switch would have to be 2048 times smaller to keep the time constant the same value. This in turn means that the transistor switch width would have to be 2048 times longer, resulting in painful layout problems regarding mismatch and area.

The single switch at the common top-plate node of the capacitor array is connected to the common-mode voltage V_{com}, and is turned on when the input signal is being sampled on the bottom-plates. It is turned off after the sampling phase so that the top-

plate node of the capacitor array is left floating for the rest of the conversion phase so that the charge is conserved. A non-overlapping clock must work between the sampling switch signals and the top-plate switch so that there is no loss of charge. The size of this top-plate switch must also be carefully designed so that the inputs up to the Nyquist rate can be sampled adequately without any settling errors due to large RC time constant of the top-plate switch.

2.3.3. COMPARATOR

The comparator is the bridge between the analog domain and the digital domain in the ADC. It is fed the analog voltages of the differential outputs of the DAC at the inputs, and then generates a digital output which is sent to the logic control block to be processed. The structure of the comparator varies, and since the operation is relatively straightforward and simple, any type of comparator would function.

The types of comparators may be classified into two categories; comparators that have a pre-amplifier and those that do not. The former is mainly used for high resolution ADCs. The use of a preamplifier allows the reduction of input-referred noise in the comparison process [2.3.1][2.3.4], including the kick-back noise. However, the bandwidth maybe limited by the amplifier, and there will always be static power consumption. This may degrade the low-power consuming quality of the SAR ADC. The latter type of comparator, which does not use a pre-amplifier, is mostly used for

low power consumption and high-speed ADCs. A dynamic latch-type architecture such as the Strong Arm latch is widely used due to its simplicity, zero static power consumption, fast operation speed etc. However, it may be prone to error in noisy environments. Fig. 2.3.3 shows the basic latch-type comparator which is widely used in SAR ADCs. The input transistors are M_{inp} and M_{inn}, and the latchs are formed by transistors $M_{n1\text{-}2}$ and $M_{p1\text{-}2}$. $M_{rst1\text{-}2}$ are for resetting the internal nodes while the comparator is not operating, and M_{tail} is the tail current source.

For faster operation, there have been improvements on the basic dynamic-latch structure to include an extra tail current source, so that the input transistor pair and the latches operate with independent biases [2.3.5]. This allows the latch input transistor

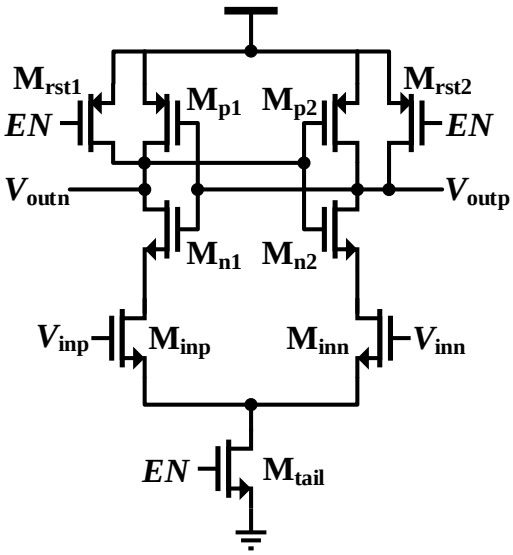


Fig. 2.3.3 Schematic of the Strong Arm latch comparator.

pair to continuously operate in the saturation region, thus allowing faster comparison. This does not affect the power consumption due to the fact that it still works as a dynamic latch; only a little area overhead has been included for the speed improvement.

2.3.4. CONTROL LOGIC

The control logic block is essentially the algorithm that performs the binary-search by manipulating the switch network in the CDAC. The control logic consists of three main blocks; the internal clock signal generator, the dynamic register bank, and the digital error correction block. The internal clock phase signal generator is the block where the phase control signals for the sampling and the conversion cycles take place. The block receives an external sampling clock, and divides it into multiple phases that are at least (N+1) times faster for an N-bit resolution ADC. These multi-phases are used for the sampling phase and the N conversion cycles, so internally the digital logic operates at a bandwidth that is an order higher than the sampling bandwidth.

The dynamic register bank is the block where the controls for the binary-search in the CDAC are generated. The dynamic registers are connected in a sequential method. It is thanks to this successive register architecture that the SAR ADC got its name. Although the same function could be written and synthesized using HDL, this simple yet powerful architecture allows seamless operation with minimal logic delay. It should be noted that this dynamic register bank is specifically for controlling the V_{cm}-based

CDAC architecture, and has an extra row of registers than the most basic successive approximation register. A more detailed explanation will be included in the following chapters in the proposed SAR ADCs.

2.4 PERFORMANCE LIMITING FACTORS

In this section, some major issues that degrade the performance of the SAR ADC will be illustrated. Unfortunately for the designer, simple as it is, the SAR ADC will not always perform in the ideal way as described in the previous section. Non-idealities as well as practical issues will cause undesired or unexpected effects that must be considered if the ADC is to perform as its intended specifications. The performance of the SAR ADC will be examined by the two dominant specifications; operation bandwidth and resolution.

2.4.1. RESOLUTION LIMITING FACTORS

Resolution can be limited in the SAR ADC for various reasons. The resolution problem is limited to the analog domain, which includes the CDAC and the comparator. Fig. 2.4.1 shows the most critical limitation locations and the reasons in the block diagram of an SAR ADC. The most obvious problem in the resolution degradation is the settling error of the CDAC. As explained previously, the capacitor of the CDAC

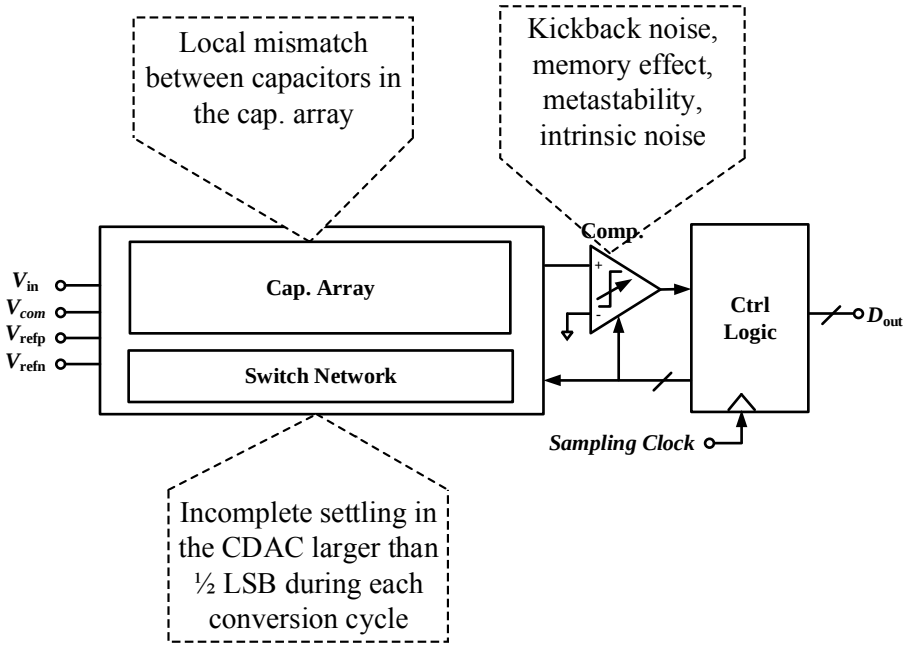


Fig. 2.4.1 Resolution limiting factors and their locations in the SAR ADC.

and the corresponding switch network inevitably forms an RC time constant, and any voltage change will take time to settle to the tolerated error range. This applies to both the sampling phase and the conversion phase of the CDAC operation. At the sampling phase, a sufficient sampling period must be allocated for the input signal to be adequately tracked and sampled. The error from the ideal input and the sampled input must be smaller than the quantization noise ADC, or there will be degradation in the resolution. This is a general statement that applies to all types of ADCs. For the conversion phase, the matter is specifically for the SAR ADC. As mentioned previously, the RC time constant of each capacitor and its corresponding switch network has been

designed the same, so that ideally there will be no delay in the voltage change at the common top-plate which is the CDAC output [2.3.3]. However, the capacitance and resistance are subject to mismatch and parasitics, and therefore sufficient settling time must be allocated to each cycle of the conversion phase. The voltage error due to incomplete settling of the CDAC must be less than 1/2 LSB in order for the domination of the quantization noise.

The mismatch in the capacitance values of the capacitors in the CDAC also cause resolution degradation. Capacitor mismatch inevitably occurs in the implementation process, and depends heavily on the used technology. The local mismatch however can be determined by the model, which was explained in previous section. If the physical dimensions of the capacitors are too small, then the mismatch will be too large and this mismatch will cause resolution degradation. Moreover, other than the intrinsic mismatch between unit capacitors, the mismatch due to the parasitic capacitance is also a degradation factor. Even with symmetrical and systematic layout, connecting metals will generate parasitic capacitance which will contribute to the overall capacitance of each capacitor stage. If this capacitance gain is too large, then the binary weighting between capacitors will ultimately be non-linear, which will undoubtedly cause errors in the binary-search process.

The comparator also may affect the performance of the ADC in terms of resolution. First of all, the kickback noise may deter the voltages of the DAC. No charge is transferred, so in the long term no error is accumulated. However, the kickback is

generated when the comparator is turned on and the voltages of the internal nodes of the operating comparator alter the CDAC by the parasitic capacitance of the input transistors. This voltage change takes place at both nodes with approximately the same amount, so it is a trivial situation for most cases. However, for high resolution SAR ADCs, just a subtle amount of voltage change may cause the initial CDAC voltages for comparison to switch polarity, causing a comparison error that may not be restored in binary-search algorithms. Second, the memory effect can also cause errors in the comparator decision, causing the resolution of the ADC to suffer. Memory effects are caused by incomplete reset of the internal nodes of the comparator. The comparator must always start its comparison with all the internal nodal pairs at the same voltage level. Internal reset switches which connect the nodes of interest to either supply or ground must therefore be able to charge or discharge enough current in the given reset time. Switches that connect the internal nodal pairs to each other may also alleviate the memory effect. However, this in turn will again add additional loads to the internal nodes and therefore slow up the comparison process and cause additional power consumption. The metastability issue is also a potential cause of comparison error. In the conventional SAR ADC, time is allocated for the comparator to generate a valid output before the dynamic registers use this information to control the CDAC. The comparator must be able to generate the correct output in the allocated time for inputs with differences up to 1/2 LSB. However, the problem is that it is with uniform probability in which cycle the inputs will be the closest together. Therefore, the

comparison time allocation must take account this worst case for all the cycles. Lastly, the internal noise of the comparator itself may cause errors in the decision-making. As explained earlier, the actual operation bandwidth of the comparator is at least an order faster than the sampling bandwidth of the whole SAR ADC. Therefore, the comparator must be able to make the correct decisions even with high frequency noises. One simple way of reducing the noise would be to add capacitance at the internal nodes; however this would again slow down the operation of the comparator and increase the power consumption.

2.4.2. OPERATION BANDWIDTH LIMITING FACTORS

To examine the operation bandwidth limiting factors in the operation of the SAR ADC, a breakdown of the SAR ADC operation in speed aspects is done. The sampling and conversion must be done inside the given sampling bandwidth with some margin, and therefore time phases must be carefully allocated. These can be categorized according to its components: the settling time of the CDAC, the decision time of the comparator, and the logic delay of the control logics. Figure 2.4.2 shows the block diagram of the conventional SAR ADC with the location of the operation bandwidth limiting factors highlighted.

The settling time of the CDAC varies from cycle to cycle, and it is a function of the capacitor size of the cycle of interest. As explained in the previous sections on the

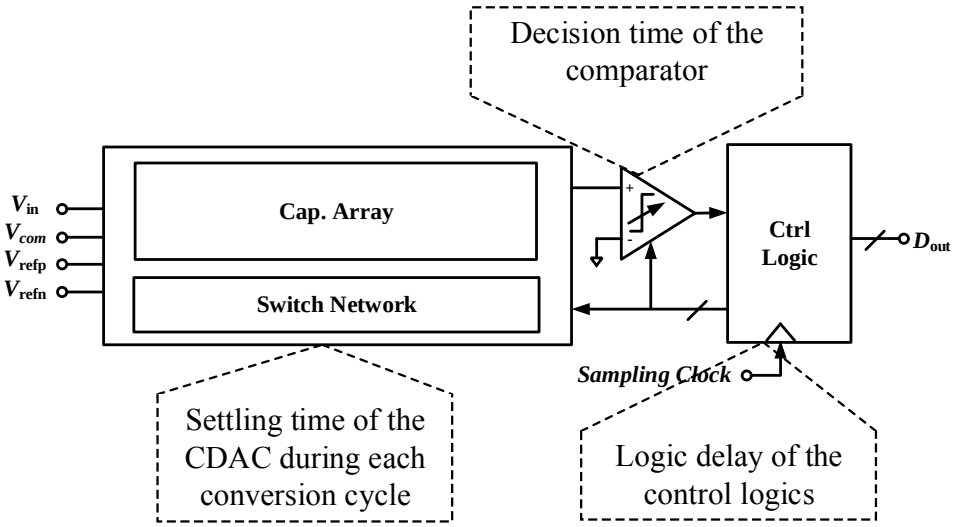


Fig. 2.4.2 Operation bandwidth limiting factors and their locations in the SAR ADC.

principle of the operation of the SAR ADC, the CDAC changes voltages in an attempt to binary-search the sampled voltage. These changes in the output voltage of the CDAC are proportional to the capacitor size; this means that the first cycle will have to change the voltage of a half of the input range, the second cycle change would be a quarter of the input range, and so on. Therefore it is safe to assume the earlier the cycle is in the conversion process, the longer the settling will be. Enough time must be allocated so that the DAC voltage can settle sufficiently to within half LSB, or it would results in a conversion error. If the total capacitor size is minimized and reduced to the limit bound by kT/C noise, settling time of the capacitor DAC would also be minimized. However, designing is not this simple, as minimal capacitor sizing results in critical mismatch,

which was explained using the Pelgrom coefficient.

The comparator decision time is another part of the time allocated in the conversion process. It is largely dependent on the comparator structure, and typically a dynamic latch type is used for fast operation. Generally, if more power is consumed in the comparator design, the faster the decision time will be. Comparator decision time may take extremely long in the case of inputs which are very close together, and in this case it is said that the comparator has fallen into a metastable state. However, it must be designed that if the comparator were to fall into the metastable state, the inputs difference would have been smaller than 1/2 LSB so that whatever the comparator decision is will not result in an error. The logic delay is mainly technology dependent, and as explained in the introduction, the development of faster logic due to finer process was the key in the current day research on SAR ADCs. However, the logic critical path must be kept as simple as possible, and the successive dynamic register structure is currently the best solution in the fast operation of the control logic.

2.5 PRIOR WORK

2.5.1. INTRODUCTION

There have been very many trends of development in the research for development of the SAR ADC. The main interest of research on the performance of the SAR ADC can be divided into the following; further lowering the power consumption for ultimate

figures of merit, enhancing the speed of operation which is a clear disadvantage of the SAR ADC, and enhancing the resolution of the SAR ADC without trade-offs with its other advantages. This thesis will focus on the latter two aspects; the speed enhancement and resolution enhancement. Prior works cannot all be classified into a single aspect, and therefore some very revolutionary works will be introduced as well as more recent works of interest.

2.5.2. SPLIT-CAPACITOR STRUCTURE OF THE CDAC

The split-capacitor structure is a technique that is used in the capacitor array of the CDAC in order to reduce the total required number of unit capacitors. The capacitors in a conventional SAR ADC must be weighted in a binary manner for the binary-search algorithm to be processed. However, this would mean that the capacitors will become exponentially large for higher resolution SAR ADCs. For example, a conventional 12-bit SAR ADC would need a total capacitance of 4096 unit capacitors, which will be impractical to implement. Therefore, without a method for reducing the physical capacitance, the SAR ADC can only be used for low-resolution applications.

It is possible to maintain the binary ratio between the capacitance stages while reducing the total capacitance by inserting a capacitor in series with the top-plates of the capacitor array. Fig. 2.5.1 shows the bridge capacitor and the resulting split-capacitor CDAC. This inserted capacitor is called the bridge capacitor, and controls the

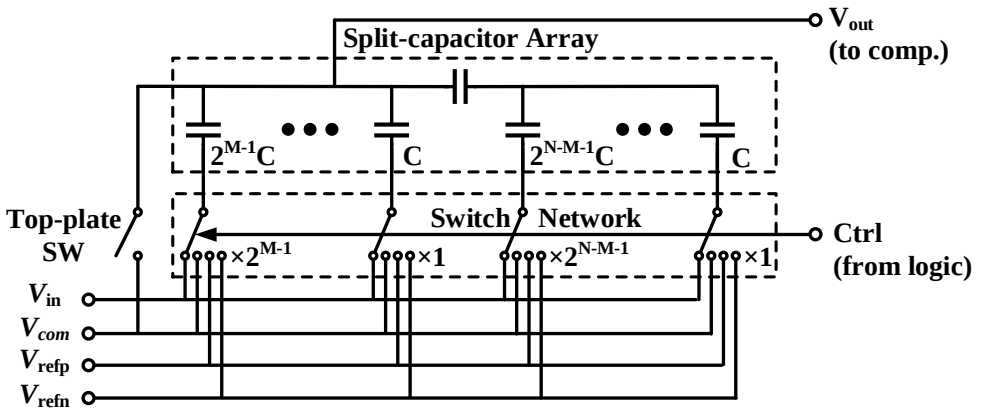


Fig. 2.5.1 Split-capacitor structure CDAC schematic in the SAR ADC.

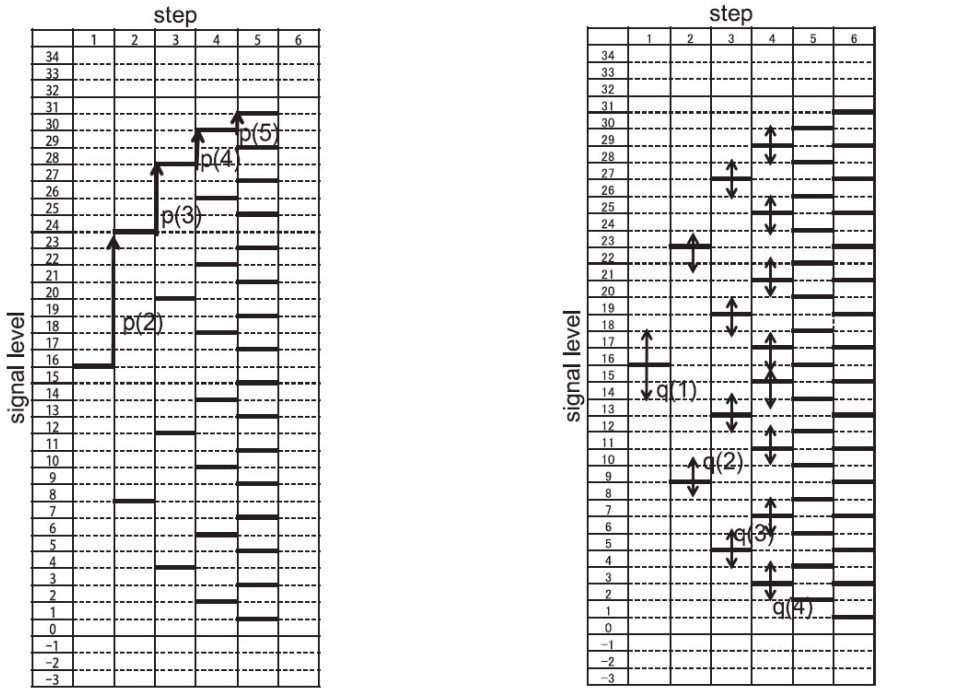
effective capacitance seen by the lower split-capacitor array. This simple but efficient technique can reduce the total capacitance in an exponential manner. For example, in the same 12-bit SAR ADC the capacitor DAC resulted in a total input capacitance of 4096 unit capacitors. However, if a bridge capacitor with the appropriate sizing were to be inserted between the 6^{th} stage and the 7^{th} stage, the total input capacitance is now reduced to just 64 unit capacitors. Given that the unit capacitor is large enough so that the kT/C limit is met, a smaller input capacitance will increase the operation speed and lower the power consumption in the SAR ADC. Details on the values of the capacitor values and the effects of parasitics will be discussed in detail in the next chapter.

2.5.3. REDUNDANCY AND CDAC WEIGHT DISTRIBUTION

Redundancy is a technique that has been used in numerous circuits, including the pipeline ADC in Nyquist ADCs[2.3.3][2.5.1]. In the SAR ADC, redundancy can also be used so that small dynamic errors in the binary-search algorithm may be corrected. It is an effective method of enhancing both the resolution and the operation speed of the SAR ADC. Redundancy can be implemented in the SAR ADC by the redistributing the conventional binary weight of the capacitors in the CDAC[2.5.2].

In a binary-weighted capacitor DAC of a basic SAR ADC, the capacitance of a stage is equal to the sum of the total sum of the capacitances of the lower stages, and the operation is based on binary-search algorithm. However, in a sub-radix-2-weighted capacitor DAC, the capacitance of a stage is now less than the total capacitances of the lower stages; this introduces some redundant ranges near the border of the decision levels. This of course comes at the cost of additional stages, as the total sum of the weights of the capacitor DAC must be a power of 2. This sub-radix-2-weighted capacitor DAC is quite simple in principle; however the values of the capacitors are non-integer multiples of the unit capacitance due to the non-integer radix. Since unit capacitances cannot be used, layout problems will induce mismatch issues and degrade the linearity of the SAR ADC. Another way to exploit redundancy is by using integer-weighted capacitance values, but with the capacitance of a stage being equal or less than the sum of the total capacitance of the lower stages. Compared to the sub-radix-2-

weighted method, the redundancy per stage is now a non-fixed number; it can be controlled by the designing of the weights. Moreover, the capacitance values now can be chosen as integer-multiple valu es of the unit capacitor, allowing systematic and matched layout for good linearity. Fig. 2.5.2 shows a graphical comparison between the conventional binary-search algorithm and the redundant-search algorithm [2.5.1]. The example is a 5-bit ADC. [i]As can be seen the binary search takes 5 steps for the whole search, but any error will not be tolerated. In the redundant search however, the whole



Binary search algorithm of a 5-bit 5-step SAR ADC. Redundant search algorithm of a 5-bit 6-step SAR ADC

Fig. 2.5.2 Graphical representation of comparison between binary-search algorithm and redundant search algorithm [2.5.1].

search will now take 6 steps. That is one more step, and the search range of each step is now the same or smaller than the binary search, but now error may be correctable in the following steps depending on the error size. This correctable error size is shown with the both-sided arrows in the graphical table on the right.

The effect of redundancy is positive in both the resolution and the operation bandwidth of the SAR ADC. Comparison errors that occur in the range of redundancy can be corrected in the following cycles, whereas in non-redundant radix-two SAR ADCs, comparison errors always result in the final output error. Another interesting fact is that the operation bandwidth can also be improved by the use of redundancy. The usage of redundancy can potentially correct errors due to dynamic causes, including the pre-settling of the CDAC. Without redundancy, the CDAC must settle within 1/2 LSB and therefore much time must be allocated for every cycle. However, the use of redundancy allows up to some pre-settling of the CDAC, given that the CDAC will eventually settle after the comparison. Therefore the time allocated does not have to ensure a settling error less than 1/2 LSB, and even though through redundancy there will be extra cycles needed, this can have a large improvement in the operation bandwidth if the CDAC settling was the bottleneck in the operation of the CDAC. A detailed explanation of the implementation and effects of exploiting redundancy in SAR ADCs will be shown with simulation results in the next chapter.

2.5.4. ASYNCHRONOUS CONTROL LOGIC

Asynchronous control logic is used in the SAR ADC control for higher operation speed. It is effective in the fact that the allocated time for waiting for the comparator to generate a valid decision can be spread out more efficiently. In the synchronous SAR ADC, the internal clock would activate the successive dynamic register bank in the control. The operation of the SAR ADC will have at one cycle where the CDAC voltage difference is closet to V_{COM} at a value under 1 LSB. This cycle will cause the comparator the longest time to generate its output, since the input difference is so small. Unfortunately, it is impossible to know which cycle this would be, so the worst case time must be allocated for every cycle, or it will result in an error. With asynchronous timing however, this can be alleviated by making the internal clock signal for the successive dynamic register bank. This internal clock signal can be simply made by the XOR of the comparator differential output. It means that the comparator has generated a valid output, so that the dynamic registers can use this information to process and generate the control signals for the next cycle.

A more complex asynchronous clocking has also been introduced to efficiently allocate the timing for the settling of the DAC [2.5.3]. This work implements a self-timing DAC, which is actually a dummy DAC, and uses it to operate asynchronously to enhance the DAC settling time. The dummy DAC and the timing diagram is shown in Fig. 2.5.3.

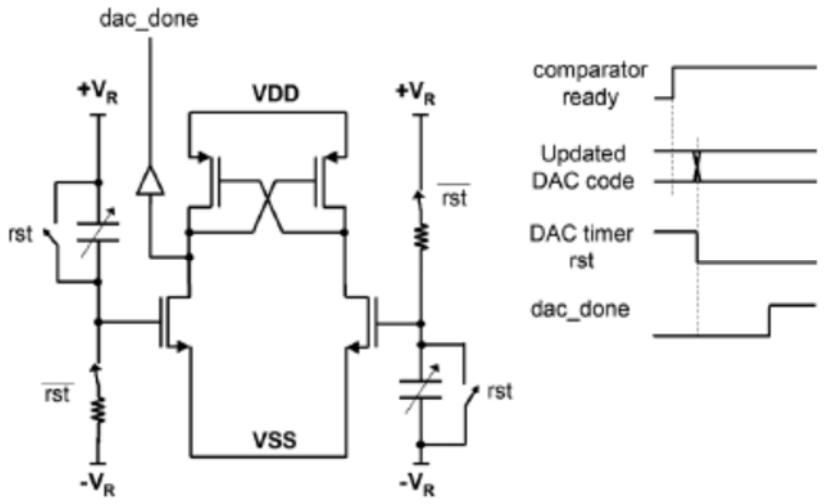


Fig. 2.5.3 A self-timing DAC is used by generating the asynchronous DAC settling signal with the use of a dummy DAC [2.5.3].

2.5.5. CALIBRATION TECHNIQUES

Calibration techniques are extremely powerful, most works at resolutions of 12 bits have some kind of calibration at work. The resolution of the SAR ADC suffers from the limiting factors described previously, but the calibration techniques intend on compensating for the static limiting factors, such as the CDAC mismatch. CDAC weight calibration can be done in an analog manner, where trimming capacitors with steps much smaller than the unit capacitors are connected to the CDAC [2.5.4]. These trimming capacitors are tuned for each digital code and the tuning codes are saved in some kind of memory. In this way, the capacitor mismatch may be reduced. It requires

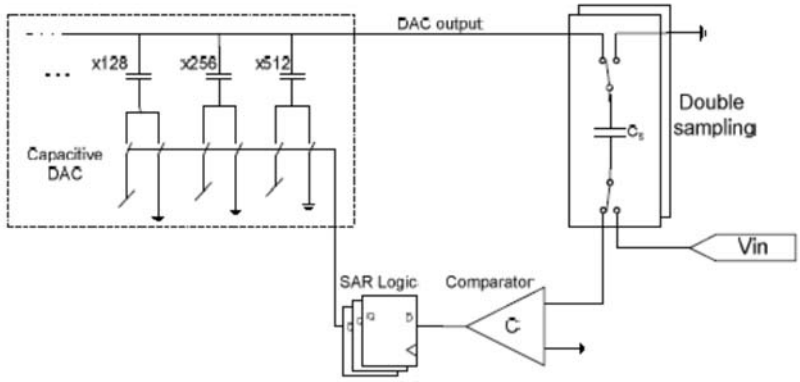


Fig. 2.5.4 Analog calibration of CDAC using trimming capacitors and memory [2.5.4].

excessive circuits including a fine tuning capacitor array and some kind of memory. Digital calibration is done by varying the weights of the capacitors in the digital error correction block from the ideally designed weights [2.5.5]. It requires a more complicated computing circuitry at the ADC output.

2.5.4. DOUBLE-SAMPLING TECHNIQUE FOR SAMPLING TIME REDUCTION

The SAR ADC suffers in the operation bandwidth in the sense that for a given sampling frequency, the actual sampling and conversion must all occur in this period. This is on the contrary to the pipeline ADC, where the sampling and conversion are all divided into stages that have the whole given sampling period to use. In the SAR ADC, a technique called double sampling is used to separate the input sampling period from

the conversion period [2.5.6]. The input is sampled on to a sampling capacitor other than the CDAC. Then, the charge in this sampling capacitor is connected to the CDAC so that charge redistribution can occur, while the next input sampling occurs simultaneously on another sampling capacitor. Although the sampling and conversion is now separated into different time phases which can occur simultaneously, this technique may suffer in the resolution that the effective charge may be reduced in the charge sharing between the sampling capacitor and the CDAC. The double sampling schematic is shown in Fig 2.5.5, where it can be seen that the sampling capacitors are independent from the CDAC.

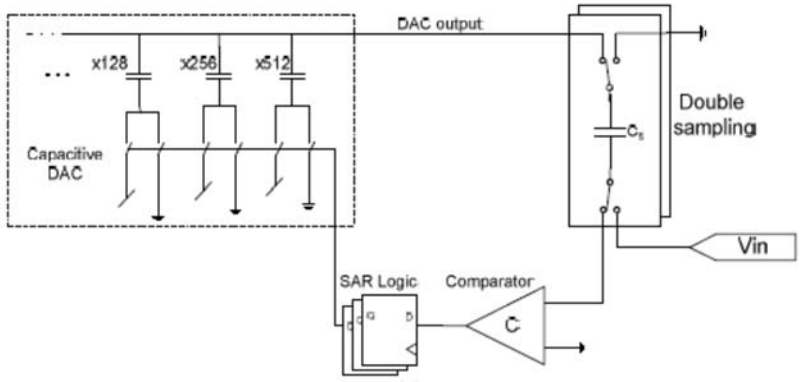


Fig. 2.5.5 Double sampling schematic, with independent sampling capacitors from the CDAC [2.5.6].

2.5.6. Two-comparator Architecture for Comparator Decision Time Reduction

A two-comparator architecture can be used to enhance the comparator decision time, especially when an input very small may cause metastability in the comparator [2.3.4]. This can be used to speed up the comparison time of the SAR ADC, or it can be used to loosen the comparator design constraints for less power consumption. Two comparators with slightly different offsets are used together with the same inputs. When the input difference is large, then the comparators will both make the same decision quickly, and it can be used. When the input difference is small, then at least one of these comparators may fall into metastability, but since the offsets differ, both of them will not fall into metastability. Therefore, the comparator which produces the output first can be used. The scheme is shown in Fig. 2.5.6.

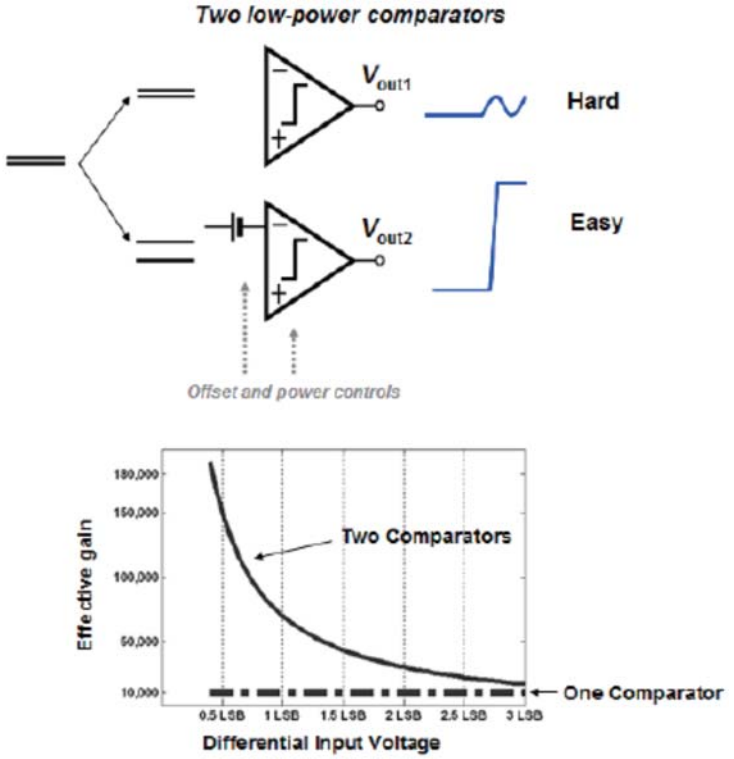


Fig. 2.5.6 Concept of the two-comparator architecture [2.3.4].

2.5.7. MAJORITY VOTING FOR RESOLUTION ENHANCEMENT

This work enhances the resolution an extra bit with the hardware capable of a limited resolution by making the final decision extra times [2.5.7]. The LSB decision is made 5 times, and in most cases due to noise and other uncertainties, the output will differ. A majority voting is done to decide the actual LSB. Experimental results show

that this actually increases the resolution for the sake of extra cycles for the majority voting and the additional logic.

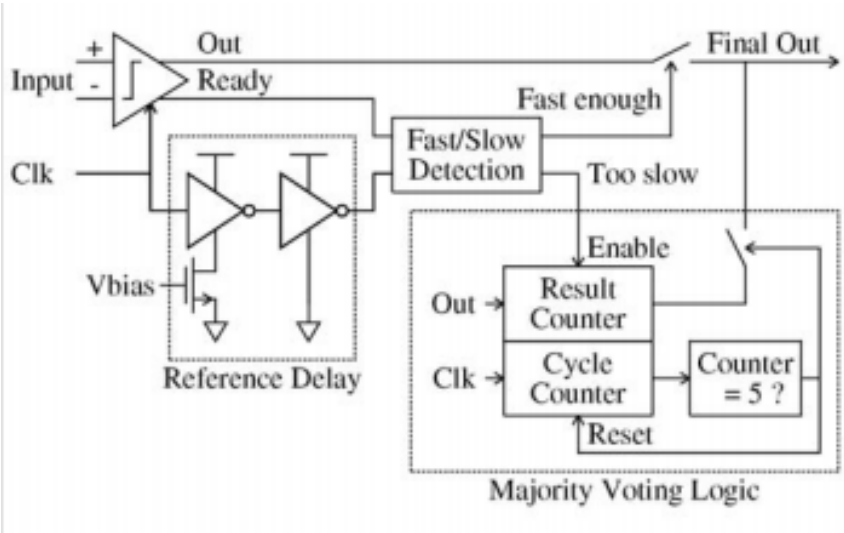


Fig. 2.5.7 Block diagram of the control of the majority voting technique [2.5.7].

CHAPTER 3

MODELING OF THE SAR ADC

3.1 INTRODUCTION

This chapter presents the SAR ADC model used in the top-level designing of the ADC. In designing the SAR ADC, the modeling step should be taken as it offers numerous advantages. There are various aspects and characteristics with tradeoffs that must be considered when designing an SAR ADC that is appropriate for the chosen application. For example, redundancy may enhance the resolution by allowing a small amount of settling error in the earlier stages; however the extra stages may reduce the operation speed. The total capacitance of the capacitor DAC of the SAR ADC will enhance the resolution, but the settling time will be longer and therefore a tradeoff with the operation speed. Similar tradeoffs can be found with the use of the split-capacitor DAC technique and the placement of the bridge capacitor. This chapter will go through the choices in choosing the structure of the SAR ADC, and show the modeling of the SAR ADC in MATLAB which was used to see the effects of the different structures in

the performance of the ADC. The model presented in this chapter was used to decide the weights of capacitor DAC of the proposed SAR ADC, and even in the transistor-level designing step, iterations were taken between the modeling and transistor-level schematic.

The model was exceptionally important that it can actually simulate the effect of the distributed redundancy against the reduced settling time before the transistor-level simulations, so that the CDAC weight-distribution could be designed without much painful iterations in the transistor-level. Moreover, it covers a variety of widely used structures; the conventional binary SAR ADC, the sub-radix-2 SAR ADC, the split-capacitor DAC ADC, and even the TCC-CDAC hybrid SAR ADC which will be proposed in Chapter 5.

3.2 WEIGHT DISTRIBUTION OF THE CAPACITOR DAC AND REDUNDANCY

Although the SAR ADC is known for its simple structure and low-power operation, the biggest limitation is its relatively low operation speed. Exploiting redundancy is an effective method of enhancing both the resolution and the operation speed of the SAR ADC. Redundancy is built into the structure of the SAR ADC by distribution of the total capacitance of the capacitor DAC into each stage. In a binary-weighted capacitor DAC of a basic SAR ADC, the capacitance of a stage is equal to the sum of the total

sum of the capacitances of the lower stages, and the operation is based on binary-search algorithm.

However, in a sub-radix-2-weighted capacitor DAC, the capacitance of a stage is now less than the total capacitances of the lower stages; this introduces some redundant ranges near the border of the decision levels. This of course comes at the cost of additional stages, as the total sum of the weights of the capacitor DAC must be a power of 2. This sub-radix-2-weighted capacitor DAC is quite simple in principle; however the values of the capacitors are non-integer multiples of the unit capacitance due to the non-integer radix. Since unit capacitances cannot be used, layout problems will induce mismatch issues and degrade the linearity of the SAR ADC. A better way to exploit redundancy is by using integer-weighted capacitance values, but with the capacitance of a stage being equal or less than the sum of the total capacitance of the lower stages. Compared to the sub-radix-2-weighted method, the redundancy per stage is now a non-fixed number; it can be controlled by the designing of the weights. Moreover, the capacitance values now can be chosen as integer-multiple values of the unit capacitor, allowing systematic and matched layout for good linearity. The operation of a weighted capacitor DAC of the SAR ADC is given as the equation below.

$$v_{dac}(i) = v_{dac}(i-1) + 2 \times (d(i-1) - 0.5) \times (\mathrm{W}(i-1)/W_{total}) \times \frac{v_{ref}}{2}, \qquad (3.1.1)$$

where $v_{dac}(i)$ is the output of the DAC, d(i) is the digital output of the i^{th} stage, and W(i) is the weight of the i^{th} stage. This is the most basic equation of the SAR ADC, and it

can be seen that the previous stage decision affects the current stage output voltage, which is then compared with the sampled input signal to generate the decision of this stage.

The modeling of the SAR ADC shows how changing the weight of the capacitor DAC distributes redundancy among the stages. The model calculates the redundancy that a stage is allocated so that a decision error with the error in the range of redundancy can be tolerated. By the redundancy calculations, designing the DAC becomes much more intuitive. The redundancy for each stage of a SAR ADC can be calculated as the following equation.

$$R(i) = R(i-1) + W(i-1) - 2 \times \mathrm{W(i)}\,, \tag{3.1.2}$$

where R(i) is the redundancy of the i^{th} stage. It can be seen that redundancy of a stage is not only affected by the weights of the current stage and the previous stage, but also by the redundancy of the previous stage. It can be intuitively thought as redundancy that is introduced in the previous stage can be kept or used up in the following stage. In designing the SAR ADC, with the use of equation (3.1.2), redundancy can be calculated for different weight distributions and number of stages. The effect of the distributed redundancy can be shown by simulation of the model with practical settling errors, which will be described in the following sections.

3.3 SPLIT-CAPACITOR ARRAY TECHNIQUE

The split-capacitor array technique and the according weight distribution in the capacitor DAC is also included in the modeling of the SAR ADC [3.3.1]. The use of split-capacitor arrays in a capacitor DAC is a very effective way of reducing the overall capacitance while maintaining the ratio between the capacitance stages. This is especially useful for SAR ADCs, as total capacitance of the DAC is bound by the kT/C noise, but as the number of bits grows, the binary-weighted stages accumulate to an impractically large capacitance value. Inserting a bridge capacitor in between the common plates of the capacitors connected in parallel can reduce the total capacitance in an exponential manner. For example, in a 12-bit SAR ADC the capacitor DAC is commonly an 11-bit structure when using the V_{cm}-based method. This results in a total input capacitance of 4096 unit capacitors. However, if a bridge capacitor with the appropriate sizing were to be inserted between the 6th stage and the 7th stage, the total input capacitance is now reduced to just 64 unit capacitors. Given that the unit capacitor is large enough so that the kT/C limit is met, a smaller input capacitance will increase the operation speed and lower the power consumption in the SAR ADC. The equation (3.1.1) is now modified accordingly as the following.

$$v_{dac}(i) = v_{dac}(i-1) + \frac{2 \times (d(i-1) - 0.5) \times C_{MSB}(i-1) \times (1 + \frac{C_{bridge}}{C_{LSBtotal}})}{C_{MSBtotal} + (C_{MSBtotal} + C_{LSBtotal}) \times \frac{C_{bridge}}{C_{LSBtotal}}} \times \frac{v_{ref}}{2}. \qquad (3.2.1)$$

Here, $C_{MSB}(i)$ refers to the capacitor value of a stage in the MSB-side of the capacitor DAC. $C_{LSB}(i)$ on the other hand refers to the capacitor value of a stage in the LSB-side. C_{bridge} is the capacitor value of the bridge capacitor. This equation looks complicated, but this is due to the fact that the capacitor values of the LSB-side do not represent the weights, but are attenuated by the bridge capacitor. With the conventional approach, where the capacitors are binary-weighted, the equation is simplified greatly. The model presented, however, is effective for all weighting and bridge capacitor values.

3.4 PARASITIC EFFECTS OF THE CAPACITOR DAC

Parasitic capacitances tend to deviate the capacitor DAC of the SAR ADC from performing the ideal search-algorithm that was initially designed by proper weighting of the capacitor stages, and their effect on the resolution is included in the modeling of the SAR ADC. The parasitic capacitances that affect the resolution of the ADC can be classified into mainly three parts; the parasitic at the top plate of the MSB-side of the split-capacitor DAC, the parasitic at the top plate of the LSB-side of the split-capacitor DAC, and the parasitic that is parallel to the bridge capacitor. The location of these parasitic capacitances are shown in Fig. 3.4.1. The parasitic capacitance at the bottom plates of the capacitor stages are not included in the model, as they do not have significant effect. The bottom plates are directly connected to the input of the ADC or

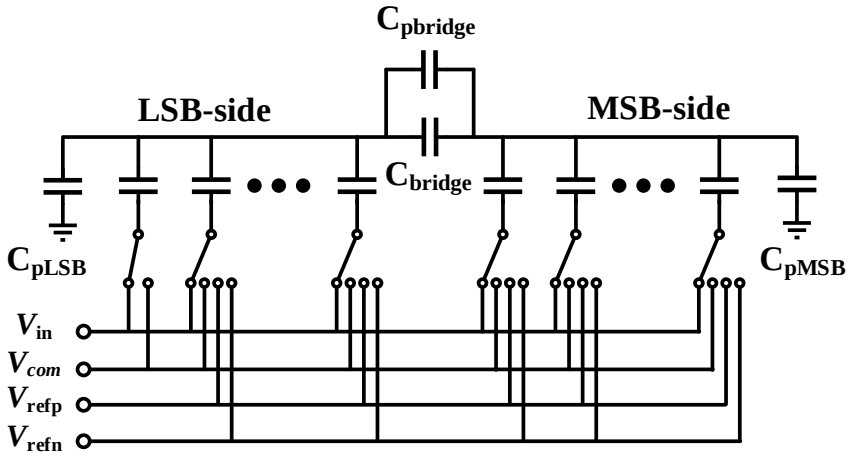


Fig. 3.4.1 Parasitic capacitances of importance in the capacitor DAC of the SAR ADC.

some DC voltage at all times, and therefore parasitic capacitance does not transfer charge.

The parasitic capacitance at the top plate of the MSB-side of the split-capacitor DAC affects the overall conversion gain of the SAR ADC. In the model, the capacitance value of the parasitic is added up to the total capacitance of the capacitor DAC to the numerator. Since the parasitic capacitance is bound to be much smaller than the ideal capacitance of the DAC itself, there will be a very fractional attenuation in the conversion range. Equation (3.2.1) can be used as the same, if the parameter $C_{MSBtotal}$ now includes the value C_{pMSB}.

The parasitic capacitance of the LSB-side top plate in the split-capacitor gives rise to much more serious linearity issues. It affects the total capacitance of the capacitor

DAC just as the parasitic of the MSB-side, but the effect is attenuated by the bridge capacitor. The more serious effect is that the total capacitance of the LSB-side of the split-capacitor DAC is increased due to the LSB-side. From an intuitive view, this will cause the same problem with the LSBs just as the MSB-side parasitic caused the total conversion: a slight attenuation in the gain of the analog-to-digital conversion. However, a slight variation of the gain in the transfer function of the LSBs means a periodic distortion of the overall transfer function, and therefore serious linearity degradation occurs. Now, equation (3.2.1) must include the value C_{pLSB} within the parameter $C_{LSBtotal}$.

A similar effect is shown with the parasitic of the bridge capacitor. Although the parasitic capacitance parallel to the bridge capacitor has only a minor contribution to the change in the total capacitance of the DAC, and therefore the linearity of the SAR ADC. The critical contribution is not to the gain of the total conversion, but to the gain of the transfer function of the LSBs. When ideally size, the bridge capacitor and the total capacitance of the LSB-side of the split-capacitor array that are connected in series would attenuate the total capacitance of the LSB-side so that the ratio between it and the last stage capacitor of the MSB-side is a desired radix, i.e., two in the example of a conventional non-redundant SAR ADC. However, the parallel parasitic capacitance now changes the attenuation factor of the LSB-side. To be more precise, since the parasitic capacitance increases the effective size of the bridge capacitor, the attenuated LSB-side total capacitance value increases. This, in tendency terms, is the same as the

effect of the above mentioned LSB-side top plate parasitic capacitance.

3.5 MISMATCH MODEL OF THE CAPACITOR DAC

In designing the size of the capacitive DAC in the SAR ADC, the total capacitance must be larger than the kT/C noise, so that the dominant noise is the quantization noise, and not the thermal noise. However, there is also mismatch to be considered. Other than the parasitic capacitance of capacitors of the DAC array, which may be minimized or kept a constant ratio to the capacitor value by careful layout techniques, the local mismatch among the capacitors is a practical issue that may not be avoided. The standard deviation of the mismatch that occurs in a capacitor is shown as the following equation,

$$\sigma(\frac{\Delta C}{C}) = \frac{A_C}{\sqrt{WL}}, \tag{3.5.1}$$

where C is the capacitance value, A_c is the Pelgrom coefficient which is process-dependent, and W and L are the physical dimensions of the capacitor. As can be seen from this equation, the capacitor size must be increased to reduce the deviation of the capacitor, and therefore the mismatch between capacitors in the DAC. Of course, as the capacitors become larger, the settling time required to charge and discharge the DAC increases as well as the charge itself, and therefore there is a tradeoff between the resolution of the SAR ADC and the operation speed or the power consumption. In the

proposed model of the SAR ADC, the standard deviation of the value of the capacitors is parameterized. Local mismatch is induced into the capacitor DAC by using the MATLAB function *normrnd()*, which generates random numbers that follow the normal distribution. A capacitor is thus introduced to local mismatch by the following equation.

$$C_{mismatch} = C_{ideal} + \text{normrnd}(0, deviation \times \sqrt{C_{ideal}}) \quad (3.5.2)$$

Here, $C_{mismatch}$ is the practical capacitive value affected by local mismatch of the ideal capacitance C_{ideal}, deviation is the aforementioned standard deviation that is fixed by the unit capacitor size and the process-dependent Pelgrom coefficient. The model is capable of giving local mismatch effect to the MSB-side and the LSB-side of the split-capacitor DAC and/or to the bridge capacitor to see the effects of local mismatch among capacitors in different locations in the DAC in order to gain some insight in designing and the DAC of the SAR ADC.

An example of the usage in designing will be explained. For a conventional 12-bit binary-weighted SAR ADC, the model suggests an ENOB of 11.46 bits for a capacitor mismatch given with the deviation value of 0.01. However, the capacitor values would be impractically high, and therefore a bridge capacitor is inserted, splitting the DAC into 5 MSB-side stages and 6 LSB-side stages. It is assumed that the unit capacitor size remains the same. When simulated again with the model, the ENOB now drops drastically to 8.88 bits for the same standard deviation value of 0.01. To locate the dominant factor for this degradation in resolution, the local mismatch is applied only

to one of the three locations: MSB-side, LSB-side, and the bridge capacitor. Simulation of the model respectively show ENOB values of 8.91 bits, 11.88 bits, and 10.96 bits. From this, we learn that the MSB-side is the most vulnerable to mismatch, and the bridge capacitor follows. This can be intuitively understood as the fact that the MSB-side is responsible for generating the most significant bits, and therefore the mismatch effect will show more.

In the example above, the bridge capacitor then can be moved for further effect. The same simulation of the model occurs, but now with the MSB-side having 10 stages and the LSB-side having only one stage. The respective ENOB values for the mismatch applied to all capacitors, only MSB-side, only LSB-side, and only bridge capacitor are respectively 11.09 bits, 11.09 bits, 11.91 bits, and 11.91 bits. This shows that now the MSB-side has much more stages, the capacitance values have exponentially increased, and therefore more robustness against mismatch has been gained.

3.6 SETTLING ERROR OF THE DAC

The settling error of the DAC in the SAR ADC is defined as the difference between the ideal voltage level and the practical, exponentially settling voltage level of the output of the DAC. The settling error is a function that is dependent on the time constant of the DAC and the time allocated for the DAC to change values. Time constant of the DAC is a function of the size of the unit capacitor and the unit switch.

In the model, the settling error is parameterized as a constant value, the settling error ratio, multiplied by the ideal settling level. This is reasonable because in the actual transistor level design of the capacitor DAC, the capacitor size of each stage and the according switch size are designed to be proportional, so that the capacitance value and the resistance value are inversely proportional, and therefore the time constant of all the stages are the same. The time allocated for DAC settling is also kept the same in the actual operation of the SAR ADC. Therefore, the settling error ratio is constant regardless of which stage the DAC is currently processing. The model now defines the decision level of the SAR ADC by calculating the output of the DAC by the following equation.

$$v_{dac}(i) = v_{dac}(i-1) + 2 \times ((d(i-2) - 0.5) \times C_{MSB}(i-2) \times e_{settling} + (d(i-1) - 0.5 \times C_{MSB}(i-1) \times (1 - e_{settling})) \times \frac{(1 + \frac{C_{bridge}}{C_{LSBtotal}})}{C_{MSBtotal} + (C_{MSBtotal} + C_{LSBtotal}) \times \frac{C_{bridge}}{C_{LSBtotal}}} \times \frac{v_{ref}}{2}$$

(3.6.1)

More adjustments have been made to the equation (5.2.1), where $e_{settling}$ is the settling error ratio. We can see that in a stage, the output voltage of the DAC is defined both by the 'then unsettled' voltage from two stages ago, and the unsettled voltage from the previous stage and their digital outputs. Here, the model assumes that the voltage variation due to the previous stage switching of the DAC has settled. This is a fair assumption, since the SAR ADC will not operate properly at all if decisions were made

while the DAC output was constantly varying due to switching from earlier stages.

The settling error obviously introduces error in the conversion of the SAR ADC, and therefore the linearity will degrade as the settling error ratio is increased. However, the settling error can be tolerated up to a certain level by exploiting redundancy, and if the distribution of the redundancy effects the level of tolerance. The model of the SAR ADC demonstrates this feature with the following example simulations.

Again, for the example, the conventional 12-bit binary-weighted SAR ADC is simulated with the model. The Fig. 3.6.1 shows the ENOB values for this conventional SAR ADC with settling error ratio values of 1, 0.99, and 0.95 respectively.

The simulation of the model shows ENOB values for the respective settling error ratios as 11.91 bits, 11.02 bits and 7.97 bits. The results show that even a settling error of 1% degrades the performance of the SAR ADC by approximately 1 bit. This means that when designing the SAR ADC, a long settling time must be allocated for complete settling of the voltage of the DAC, which means that the operation speed will be inherently slow.

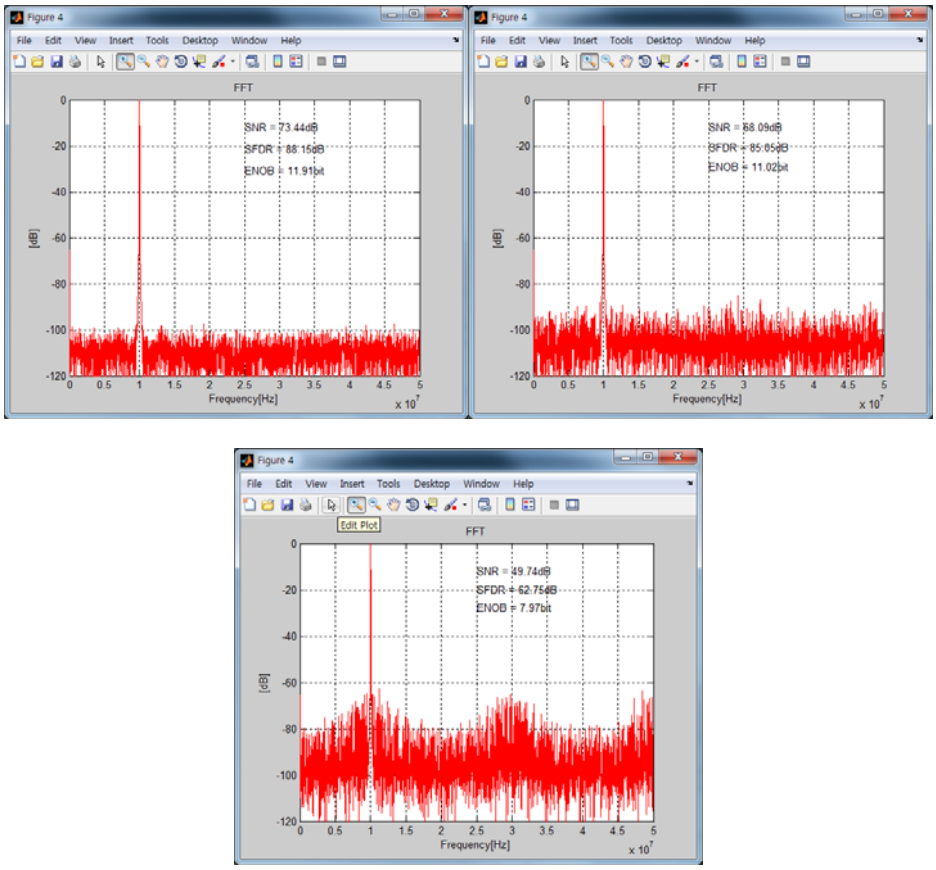


Fig. 3.6.1 Simulation of the modeling of the 12-bit conventional SAR ADC with settling error ratios of 1, 0.99, and 0.95, respectively.

However, an optimized 12-bit SAR ADC can be designed with redundancy. With an extra 4 bits for redundancy, the total stage number is now 16, with the weights of each stage being [1024, 382, 240, 150, 100, 60, 35, 20, 15, 9, 5, 3, 2, 1, 1]. The weights were calculated by optimizing redundancy distribution through all stages and then rounding them to integer values. To fully demonstrate the effect, the simulation of the

model is now done with settling error ratio values of 0.8, 0.75, and 0.7.

Simulation results show a drastic improvement compared with the conventional SAR ADC. Even with 75% settling only, the reduction in ENOB is less than 0.5 bit, and when the settling is 70%, the ENOB drops rapidly. This is because the amount of error that an optimized 12-bit SAR ADC with 4 extra bits for redundancy can handle is

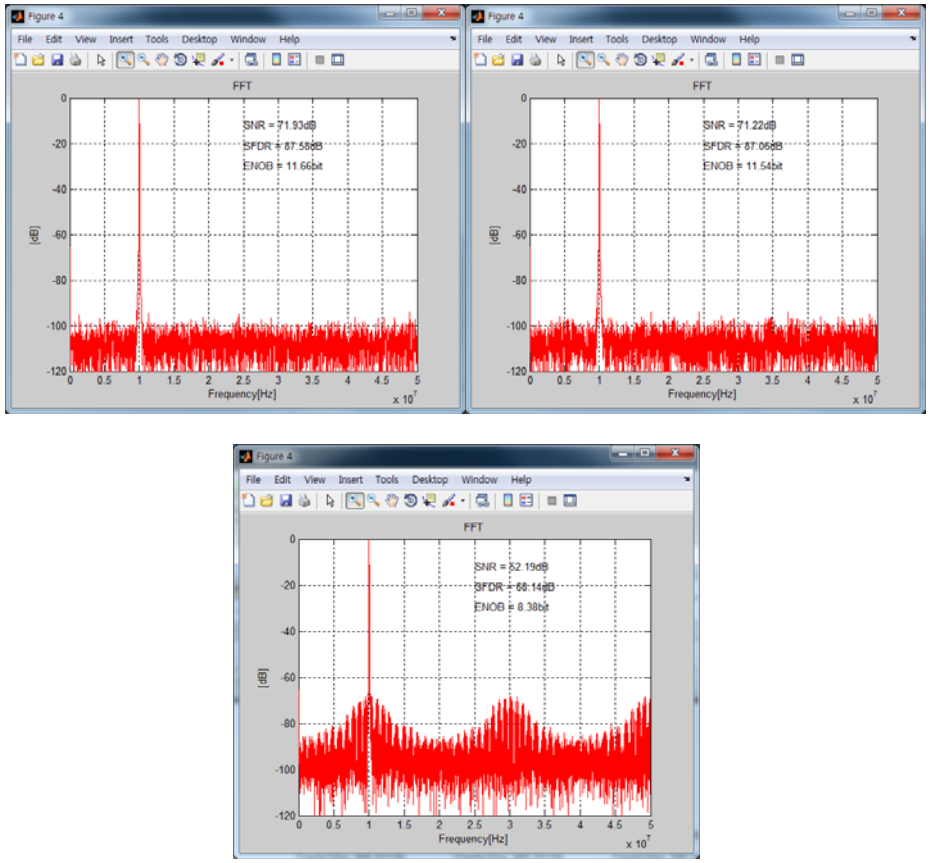


Fig. 3.6.2 Simulation of the modeling of the optimized 12-bit redundant SAR ADC with settling error ratios of 0.8, 0.75, and 0.7, respectively.

over 25% and less than 30%. From these results, the usefulness and necessity of accurate and precise weight distribution through beforehand modeling of the SAR ADC can be easily seen.

3.7 COMPARATOR DECISION ERROR

Finally, the comparator decision error is included in the model also. The comparator decision error is the error made by the comparator when it has to compare inputs with very small difference. The static error, which is commonly called the offset of the comparator, is not of interest here, as it would only shift the transfer curve and the linearity will be unaffected. The dynamic noise generated by the transistors of the comparator will affect the error ratio. The input-referred noise of the comparator was seen as a white noise source which could result in an error at the comparator out. Therefore in our model, the decision level was differed by the comparator. By using the awgn() function of MATLAB, which is generating a white Gaussian noise to a signal, the comparator decision level now changes according to the following equation.

$$v_{comp\_error}(i) = awgn(v_{ideal}(i), comp\_SNR), \tag{3.7.1}$$

where v_{comp_error} is the decision level, v_{ideal} is the original decision level, and comp_SNR is a parameter that shows the signal-to-noise ratio specification of the designed comparator in transistor level. The model of the comparator noise was used as a guide on how the noise of the comparator affects the resolution of the ADC.

3.8 DIGITAL ERROR CORRECTION

The final part of the model of the SAR ADC operation is the digital error correction part. The capacitor weights must be accounted for when processing the digital outputs of the SAR ADC. There are two methods of actually generating the outputs from the digital bits. The bits can be added up from 0 with the weights doubled, or the starting point can be at the center value of the digital range, and the bit 0 subtracts the corresponding weight while the bit 1 adds the weight value. For binary-search radix-2 SAR ADC, it is the same value. However, for ADCs with redundancy, the correct digital error correction method must be used according to the CDAC structure. For the V_{cm}-based structure, the latter must be used. Digital calibration was also implemented in the MATLAB model in this digital error correction domain, so as to induce random mismatch into the model, and then calibrate this model through digital calibration. However, calibration is beyond the scope of interest of this thesis, and details will not be included.

CHAPTER 4

SAR ADC WITH INTEGER-BASED CDAC EXPLOITING REDUNDANCY FOR AUTOMOTIVE APPLICATIONS

4.1 INTRODUCTION

In this chapter, an SAR ADC implementation with enhanced performance will be presented. The SAR ADC will be implemented for use in automotive applications. In the first section, the motivation for the design of the SAR ADC for automotive applications will be presented. A background knowledge on the characteristics and examples of commercial solutions of currently used ADCs will be given. The characteristics of automotive applications include a relatively low bandwidth operation of under 1 MHz, and a resolution of 10 to 12 bits. SAR ADCs have been used in commercial solutions for automotive applications. The bandwidth is a trivial matter in designing the SAR ADC, however the resolution of 12 bits is a challenge. For the implementation of a high-resolution SAR ADC, this work focuses on the

implementation of the split-capacitor CDAC with only using integer multiples of unit capacitors for maximum matching characteristics. Prior works on integer-based CDACs for SAR ADCs will be presented. Next, the proposed work, the integer-based CDAC exploiting redundancy for the SAR ADC is presented. It allows the design of the CDAC with the use of only unit capacitors by exploiting redundancy, thus there is no need for additional circuits or reference voltages, or any other disadvantages the prior works potentially showed. Even without calibration, the good matching characteristics result in a performance of 12 bits. The operation principle, design procedure and the circuit structure will be fully explained. A prototype of the chip will be presented with experimental results.

4.2 MOTIVATION

With automotive electronics demand higher than ever, automotive semiconductors is a very active market in the current day. There are more than two hundred sensors in the average automotive vehicle today, and for these sensors to function properly and interact, there must be ways to a way to interface these vast number of sensors. With the growing number of sensors, the number of sensor interface readout integrated circuits (ROIC) is growing linearily. Back in the past when not many sensors were used, the built-in general-purpose ADCs inside the MCU suited the job. However, the number of sensors is too vast, and also, the MCU cannot be centralized in the vehicle

for so many sensors located just about everywhere inside and outside of the vehicle. Therefore, there is a demand for a general purpose ADC which can be used for typical automotive sensor applications, and it must be small in cost so that the increasing numbers are not burdensome.

The sensor applications inside a vehicle are not very demanding in the operation bandwidth aspect compared to newer technologies. It typically is under 1 MS/s, since the actual movement of the automotive vehicle is very slow when seen in these high frequencies. For example, the automotive vehicle which is travelling at 100 km/h actually moves approximately 0.3 mm in 1 μs, and therefore faster operations on learning the conditions of the vehicle or the surrounding environment is excessive. The required resolution for general purpose usage is also currently at 10 – 12 bits.

It should be pointed out that the environment of the automotive applications is very harsh, especially in the temperature range of -40 °C to 125 °C. Therefore, the type of ADC that is used must be stable against temperature. The SAR ADC fits this specification very well. This is because the main analog block of the SAR ADC is the capacitor array in the CDAC, and the resolution is decided by the ratio between the capacitors rather than the absolute value. The temperature change will bring about a global change in the capacitor values, but their ratio will remain intact. Moreover, the SAR ADC does not use the more sophisticated analog blocks such as the operation amplifier of the pipeline ADC, only a dynamic latch-type comparator and digital logics. Therefore, it is safe to assume that it is one of the most robust types of ADCs against

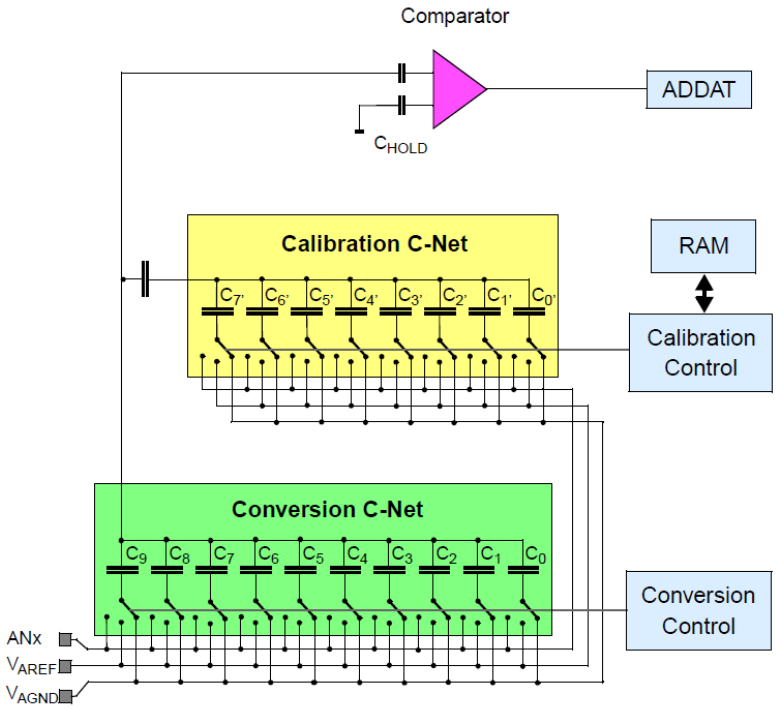


Fig. 4.2.1 Typical commercial example of the SAR ADC for automotive applications [4.2.1].

temperature variations. This is the reason for the wide usage of SAR ADCs in commercial automotive applications. The challenge is the resolution which the demand is up to 12 bits in some applications. In order to achieve 12 bits, the mismatch between capacitors must be accounted for, and a solution to alleviate this problem is needed.

Fig. 4.2.1 shows the block diagram of a commercial example of an SAR ADC for automotive applications [4.2.1]. The block diagram shows a capacitor array that is suitable for resolutions up to 10 bits. This is a typical SAR ADC in commercial use

today, and has calibration control to adjust for the mismatch that occurs in the CDAC. In this case, the mismatch calibration would not be required if the unit capacitors were designed larger; but without the split-capacitor CDAC structure, this would again become impractical. However, the usage of a split-capacitor CDAC structure would require another type of calibration scheme in order to compensate for the mismatch that arises by the use of non-integer multiple of the unit capacitor at the bridge capacitor. Thus, this chapter examines integer-based CDAC solutions from prior works, and further proposes a new solution to solve this resolution challenge.

4.3 PRIOR WORK ON RESOLVING THE SPLIT-CAPACITOR CDAC MISMATCH FOR THE SAR ADC

4.3.1. CONVENTIONAL SPLIT-CAPACITOR CDAC FOR THE SAR ADC

The conventional split-capacitor CDAC structure is revisited in this section. The split-capacitor CDAC structure is shown in the Fig. 4.3.1. As explained previously, using this type of structure is essential for high resolution SAR ADCs, as the exponentially-sized capacitors become too large for practical usage over 10 bits. The biggest problem is that, however, to maintain the ratio that was designed before using the split-capacitor technique, the bridge capacitor must be sized accordingly so that the effective capacitance seen from the MSB-side top-plate of the CDAC towards the LSB-

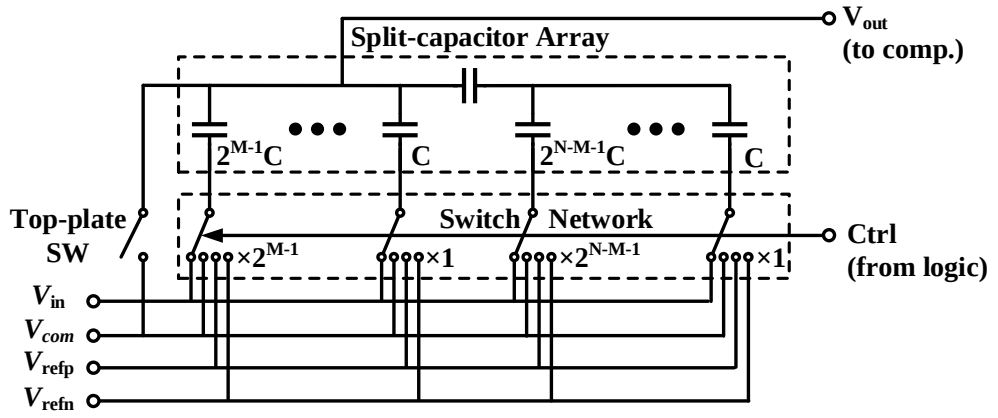


Fig. 4.3.1 Split-capacitor structure CDAC schematic in the SAR ADC.

side is the original ratio. This results in a non-integer sized bridge capacitor; in other words, unit capacitors cannot be used in designing this CDAC.

As it is well-known, it is common practice to use unit elements in designing arrays of the same elements to reduce unwanted effects such as mismatch. It is also much easier to layout with the same parasitics, and with common-centroid symmetry. In the previous chapter, it could be well seen that the slightest mismatch especially in the bridge capacitor can have a huge impact on the whole resolution of the ADC. Therefore, there have been a research trend on solving this mismatch issue of the split-capacitor CDAC for the SAR ADC.

4.3.2. SPLITTING THE LAST STAGE OF THE LSB-SIDE OF THE CDAC

The simplest way of exploiting the split-capacitor architecture with only using integer-based capacitors is by splitting the capacitor array at the last stage [4.3.1]. The schematic is shown in Fig. 4.3.2. This will result in a bridge capacitor value of 2. There is no additional circuits or reference voltages, so absolutely no overhead compared to a non-split CDAC. However, the capacitor reduction effect is extremely small; only by half, whereas if the bridge capacitor were located at the center of the CDAC, then the reduction would exponentially decrease. Therefore, this structure is not suitable for high-resolution SAR ADCs, where the reduction of the total capacitance is a critical issue.

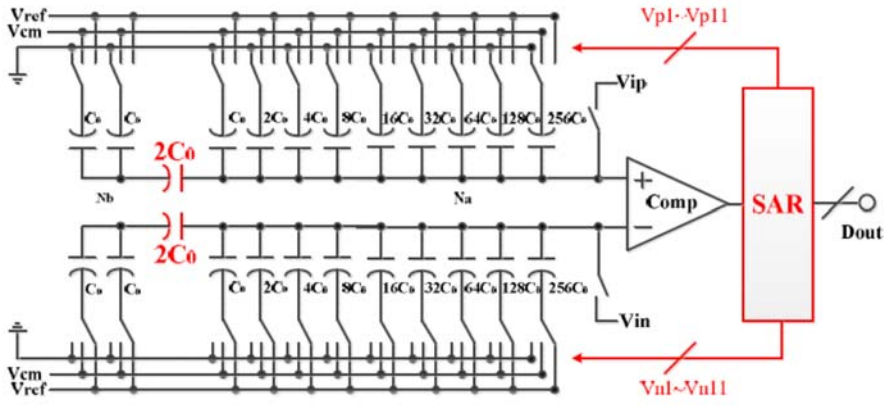


Fig. 4.3.2 Schematic of the split-capacitor architecture with the bridge capacitor at the last stage [4.3.1].

4.3.3. CALIBRATION OF THE NON-INTEGER MULTIPLE BRIDGE CAPACITOR

Prior works even only focus solely on calibrating the bridge capacitor of the CDAC [4.3.2]. The schematic is shown in Fig. 4.3.3. It can be seen that this work acknowledges the parasitic capacitance in parallel with the bridge capacitor, and that this variation will cause much reduction in the resolution. Therefore, this work initially designs the bridge capacitor smaller than the ideal value, and has a calibration capacitor in parallel at the LSB-side, so that tuning this capacitor will in turn match the ratio between the LSB-side capacitors and the MSB-side capacitors. The ratio may be calibrated in this method. However, this generates an overload of additional calibration circuitry, even a type of memory to store the calibration information in some cases as seen in the commercial example.

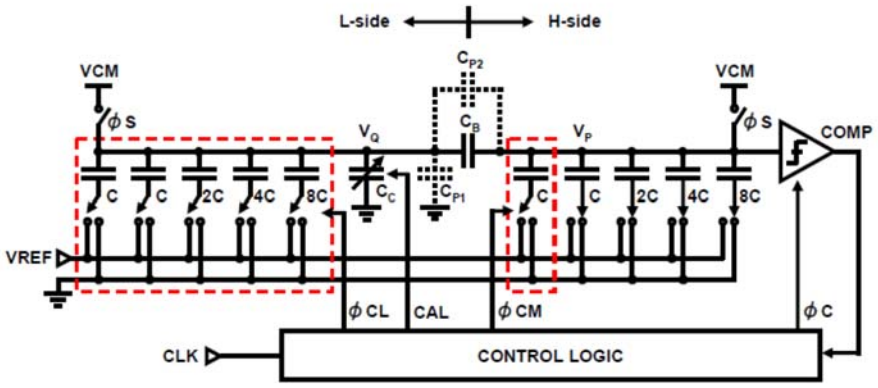


Fig. 4.3.3 Calibration of the weight mismatch of the bridge capacitor and the LSB-side capacitor to match the ratio with the MSB-side capacitors [4.3.2].

4.3.4. INTEGER-MULTIPLE BRIDGE CAPACITOR WITH LSB-SIDE CAPACITOR ARRAY CALIBRATION

This work is similar in idea to the previous work in the section above. This work however, draws to bridge capacitor as an integer, although it is known that this results in the wrong ratio between the MSB-side and the LSB-side [4.3.3]. The work then calibrates the LSB-side capacitor weights, so that the LSB-side now can retain the intended ratio even with a single unit capacitor as the bridge capacitor, which is smaller than the needed value. Again, this method requires additional capacitors and calibration circuitry, so the complexity rises. The schematic is shown in Fig. 4.3.4.

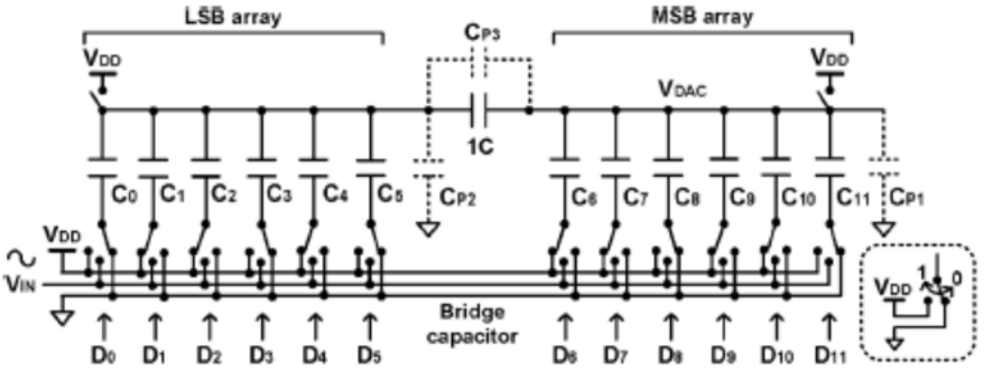


Fig. 4.3.4 Intentional error at the bridge capacitor by using a unit capacitor, and compensating the ratio through LSB-side calibration [4.3.3].

4.3.5. OVERSIZED BRIDGE CAPACITOR WITH ADDITIONAL FRACTIONAL REFERENCE VOLTAGE

Another prior work intentionally uses a very large integer-multiple of the bridge capacitor, and then fixes the ratio to the intended value by using additional fractional reference voltages [4.3.4]. The schematic is shown in Fig. 4.3.5. Although this may be able to make the ratios as the designed values, there is the overhead of an extra reference voltage. Moreover, the ratio of the reference voltage now must be exact, and therefore a mismatch in the ratio between the reference voltages will again reduce the resolution.

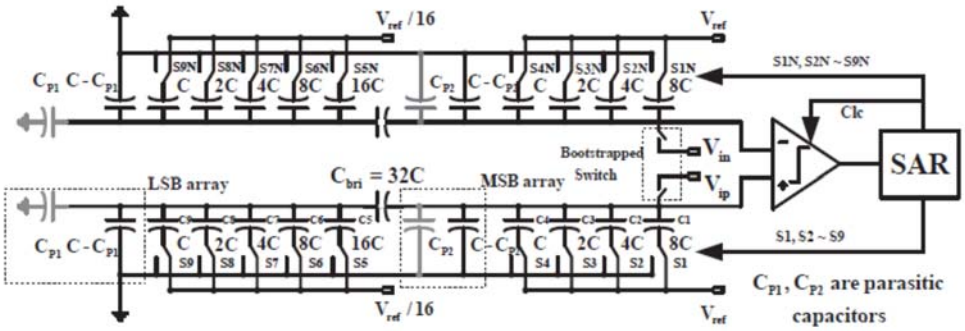


Fig. 4.3.5 The usage of an additional fractional reference voltage to compensate the ratio variation in using a large integer-multiple unit capacitor as the bridge capacitor [4.3.4].

4.4 PROPOSED INTEGER-BASED CDAC EXPLOITING REDUNDANCY FOR THE SAR ADC

This section proposes an integer-based CDAC which does not require any additional overhead including trimming capacitors, calibration circuitry or reference voltages for the SAR ADC. This is possible by exploiting redundancy in the designing of the CDAC. It was explained that in a binary-weighted CDAC, the splitting of the capacitor array would generally result in a non-integer bridge capacitor. However, if redundancy is exploited, careful weight distribution allows the use of only integer-multiples of the unit capacitor. This is because redundancy allows some degree of freedom in choosing the weight ratio between the capacitors. By setting the weight ratio between the capacitors across the bridge capacitor to an optimal value, the bridge capacitor can be made an integer-multiple of the unit capacitor without any additional capacitors or calibration schemes. Moreover, another advantage is that this allows the integer-multiple bridge capacitor to be located at the center of the DAC without any penalties for maximum capacitance reduction. This means that the unit capacitor can be increased if needed for even better matching characteristics.

To see how this can be achieved, the equation of the size of the bridge capacitor in a split-capacitor array is presented again.

$$C_{bridge} = \frac{C_{LSB\_total}}{C_{MSB\_last} - 1} \text{ ..} \tag{4.4.1}$$

C_{LSB_total} is the total sum of the capacitance of the LSB-side, and C_{MSB_last} is the capacitor value of the last capacitor stage of the MSB-side. In a conventional binary-weighted capacitor DAC, this would result in a C_{bridge} value of

$$C_{bridge} = \frac{2^k}{2^k - 1} C_{unit}, \tag{4.4.2}$$

where k is the number of stages of the LSB-side. As can be seen in the above equation, this results in a non-integer unit capacitance. For example, if the bridge capacitor were place at the center of a 11-bit CDAC for maximum capacitance reduction, the bridge capacitor value would have to be 32/31 C_{unit}. It would be extremely difficult to implement this fractional capacitor, and parasitics would undoubtedly vary the efficient capacitance even more. This can be a serious problem for higher-resolution SAR ADCs, because the non-integer unit capacitance has critical layout and matching issues.

Looking back again at the equation (4.1), if the numerator were a multiple of the denominator, then the bridge capacitor value is an integer-multiple of the unit capacitor. Redundancy allows the "tweaking" of the values of the capacitors to some freedom, as long as there is sufficient redundancy in the MSB stages and the total capacitors add up to the power of two. The integer multiple value can start from two (if it were one, this would be an ADC with missing codes), and the larger the multiple value, the more redundancy is induced along with more cycles. The actual weight distribution by this technique will be shown in the following section.

4.5 CIRCUIT DESIGN

4.5.1. PROPOSED INTEGER-BASED CDAC EXPLOITING REDUNDANCY FOR SAR ADC

The proposed integer-based CDAC can be designed by careful weight distribution of the capacitors according to the equation (4.1), and the resulting allocated redundancy, equation (3.1) should also be properly designed for maximum performance. The CDAC, as shown in Fig. 4.4.2, is a V_{cm}-based structure with bottom-plate sampling. Two extra stages have been inserted in the CDAC in order for more robust operation against the noisy environment of the automotive application. Therefore, the total stages in the capacitor DAC is now for 14 bits instead of 12. The redundancy is distributed as shown in Table 6.2.1. The 7th – 8th stage capacitors are the capacitors that actually induce the redundancy for the previous stages. As can be seen, the rest of the capacitors are weighted in a binary fashion, that is, the capacitor size is double the following stage capacitor size. The first capacitor size is an exception, as it has been reduced to make the total sum of the capacitors 2048 C_{unit}. In our design, referring to Table 6.2.1, the weights of stage no. 7 and 8 are set as 33 and 32 C_{units}, respectively. This leads to a C_{bridge} value of 2 C_{units}, which is easily implementable without layout or mismatch issues. The binary-weighted MSB-side and the LSB-side are almost identical, except for the slightly smaller MSB capacitor, and therefore allows systematic layout for better matching.

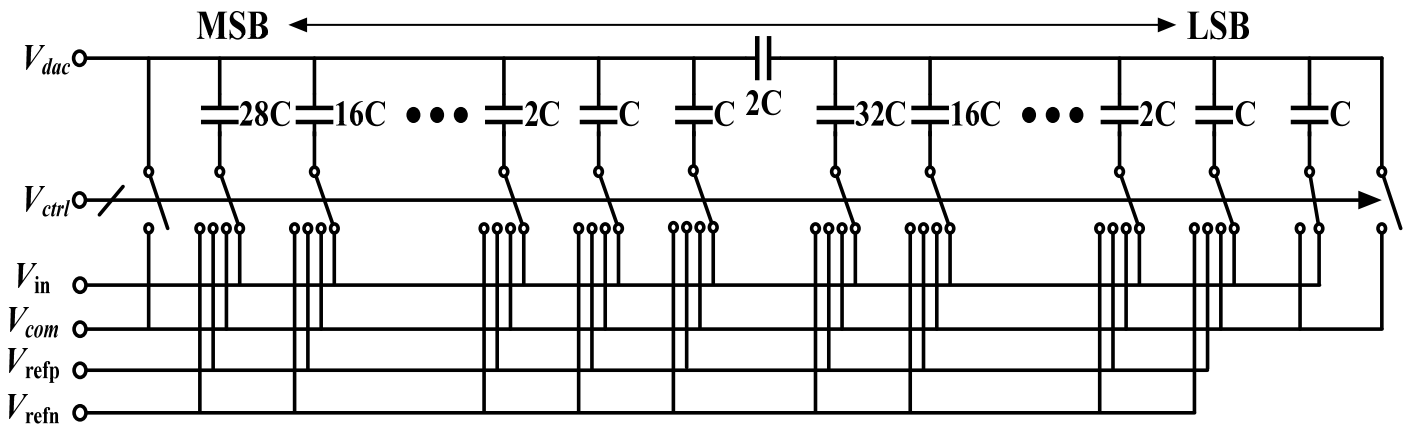


Fig. 4.5.1 Schematic of the capacitor DAC of the proposed SAR ADC.

Table. 4.5.1 Capacitor size, weight, and redundancy of each stage in the capacitor DAC.

Stage No.	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Size [C_{unit}]	28	16	8	4	2	1	1
Weight [C_{unit}]	924	528	264	132	66	33	33
Redundancy [LSB]	196	64	64	64	64	64	31
Stage No.	**8**	**9**	**10**	**11**	**12**	**13**	**Dummy**
Size [C_{unit}]	32	16	8	4	2	1	1
Weight [C_{unit}]	32	16	8	4	2	1	1
Redundancy [LSB]	-	-	-	-	-	-	-

4.5.2. COMPARATOR

For the comparator of the SAR ADC, a double-tailed comparator has been used [2.3.5]. The schematic of the comparator is shown in Fig. 4.5.2. This comparator is an improvement of the widely used Strong Arm latch, in that the tail current source is divided so that the input transistors and the latches use separate sources. This allows the input transistors to fully operate in the saturation region, therefore a more certain comparison can be made even in the noisy environment of the automotive application. The input transistors are sized large enough so that the input-referred noise of the comparator does not result in comparison errors for the resolution of 12 bits.

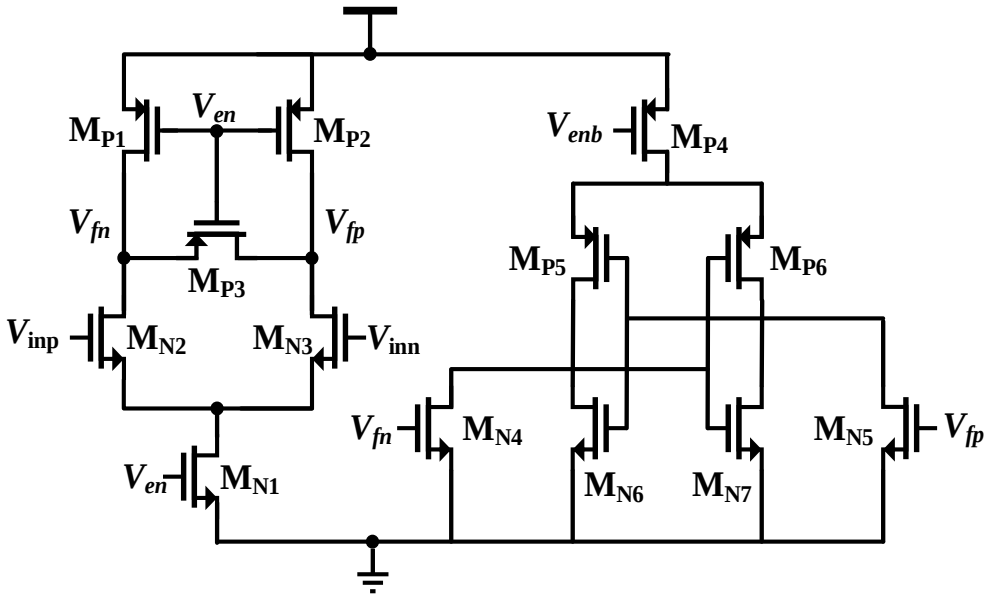


Fig. 4.5.2 Schematic of the double-tailed comparator

4.5.3. CONTROL LOGIC

The control logic of the proposed SAR ADC is designed manually by using standard digital cells. Although the used process has a minimum transistor length of 0.5µm, it was enough for the internal operation of the SAR ADC, which was approximately 20 MHz. Three registers form one unit that is responsible for the control signals of the switches of a capacitor stage. First, the conversion cycle is initiated when the sampling clock falls from high to low. This resets all the dynamic registers so that all the bottom-plates switches are connected to V_{com} which is neglected in the figure of simplicity. The clock signals for each conversion cycle will now activate each 3-register

unit successively. The comparator output is fed to the input of the registers, and the control signals for the current conversion cycle will be generated and sent to the CDAC.

Asynchronous logic has been used in this SAR ADC implementation, not because of the speed improvement, but because the internal generation of a multiphase clock was unnecessary, as it would consume additional power, and moreover contribute to noise. The dynamic registers only need operate when the comparators have generated a valid output, and therefore a simple NAND gate (for comparator outputs reset to high) is sufficient to generate an internal asynchronous clock. The block diagram of the control logic is shown in Fig. 4.5.3.

4.6 IMPLEMENTATION AND EXPERIMENTAL RESULTS

4.6.1. LAYOUT

The prototype SAR ADC that utilizes the integer-based CDAC exploiting redundancy has been implemented in a 0.5 μm technology for automotive applications with a supply voltage of 5 V. The active area of the chip is 550 μm x 300 μm. Fig. 4.6.1 shows the layout of the implemented SAR ADC. The layout is symmetrical and with the comparator located at the center between the differential CDAC. The digital control is also located at the center for reduced wiring, since the number of control signals for a differential 13-bit (11 bits with 2 redundant bits) CDAC is very large; since there are

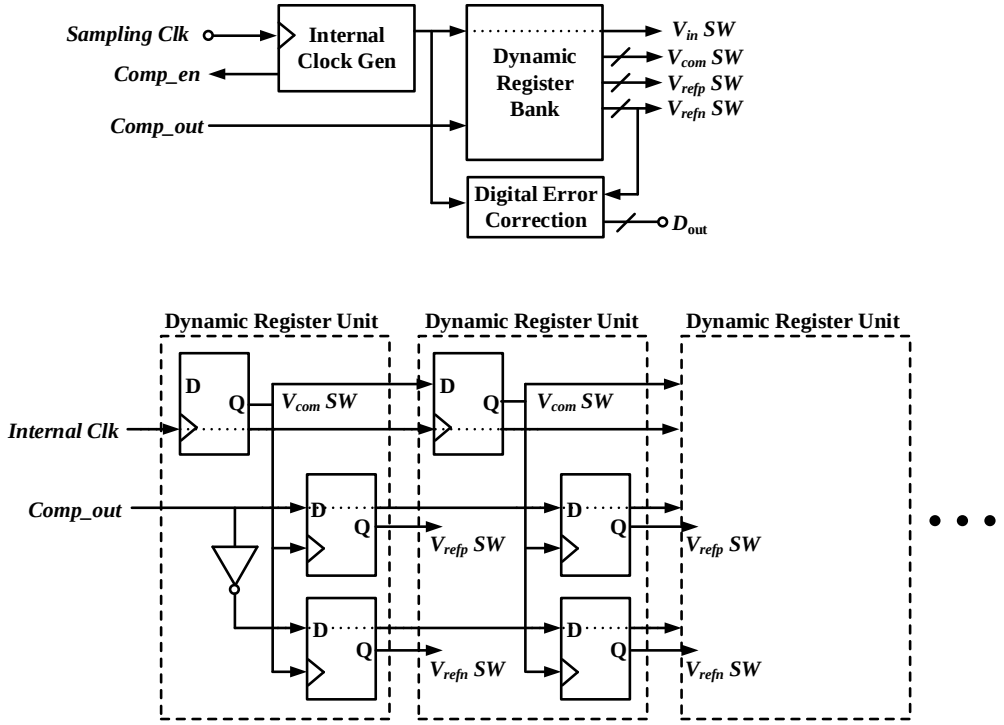


Fig. 4.5.3 Block diagram of the control logic block, with the dynamic register bank in more detail at the bottom.

four to control switches per capacitor.

The layout of the capacitor array is the most important factor in retaining the desired resolution. The unit capacitors that form the capacitor stages are all connected in a single line manner, so that the parasitics that inevitably arise between adjacent capacitors and also with the connecting wiring are all identical. This ensures that even with the additional parasitic capacitance, the ratio between the capacitors will be varied

as little as possible. Capacitors are placed tightly close together. This may be odd, but this is because the wiring connecting the capacitors must be as short as possible to reduce any unnecessary parasitics. The parasitics that arise between adjacent capacitors are actually trivial, because the top-plates are all the same nodes and therefore do not contribute capacitance, and the bottom-plate capacitances are negligible since they are switched to voltage sources. The top-plate wires and the bottom-plate wires are drawn as far as possible to also reduce any unnecessary parasitics. These points in the layout of the capacitor array have been tested thoroughly with a full post-layout extraction simulation and their effects have been confirmed. These have been illustrated in the Fig.

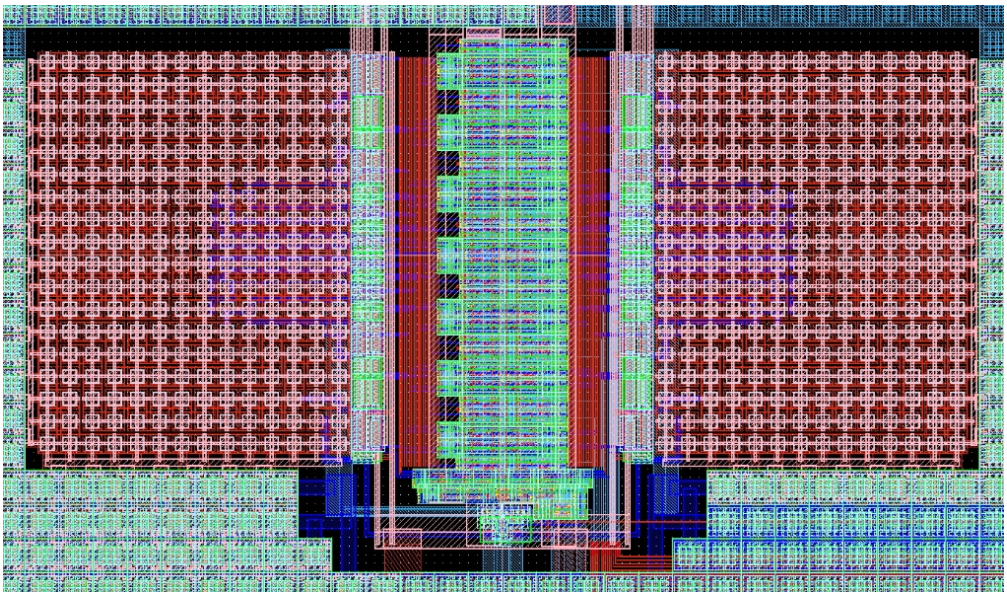


Fig. 4.6.1 Layout of the SAR ADC utilizing integer-based split-CDAC using redundancy. Active area is 550 µm x 300 µm.

4.6.2. The dummy capacitor, 1C, 2C and the 4C stages are drawn with the top-plates all connected in a cross-like metal wiring, bottom-plates for the stages connected through a single file as can be seen in the 4C stage. These top and bottom metal wiring are as far apart as possible.

The single-ended layout of the whole CDAC including the capacitor array and the switch network is shown in Fig. 4.6.3. As can be seen, the MSB-side and the LSB-side are almost identically symmetrical, except for the slightly undersized MSB capacitor. This allows systematic layout with symmetric properties. A placement diagram of the

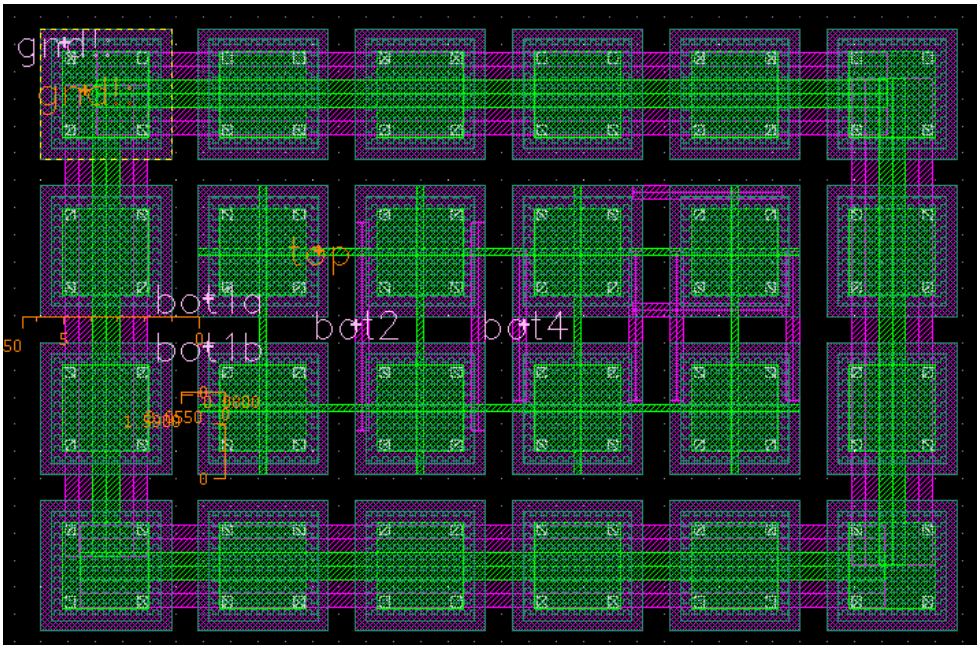


Fig. 4.6.2 Experimental layout example for drawing the capacitor arrays with MIM capacitors. Dummy cap of C, C, 2C, and 4C stages drawn.

capacitors has also been included in the figure. Every capacitor stage can be accessed directly from the outside without the routing metal having to pass under other capacitor stages. This ensures that parasitics between different capacitor stages are minimized, which is extremely important for the desired resolution conservation. The vias which connect the bottom-plate of the bridge capacitor to the top-plates of the LSB-side capacitor array have been drawn the same as the MIM capacitors with the exclusion of the MIM layer for matching purposes. Following these techniques, the capacitors can be drawn very tightly and in a relatively easy layout manner. Some prior works tend to "wrap" every capacitor up with dummy capacitors and grounded metals; however this only complicates the layout and potentially induces extravagant parasitics into the capacitor array.

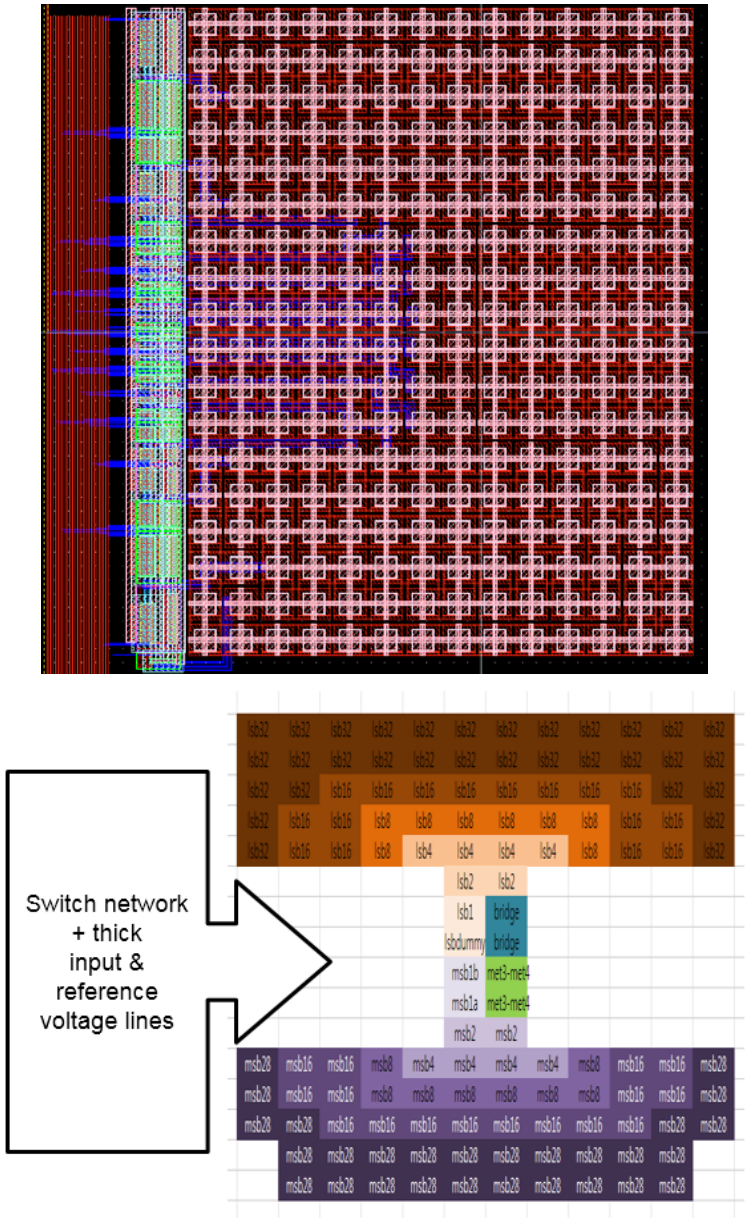


Fig. 4.6.3 Layout and placement of the capacitor array of the CDAC.

4.6.2. MEASUREMENT RESULTS AND CONCLUSIONS

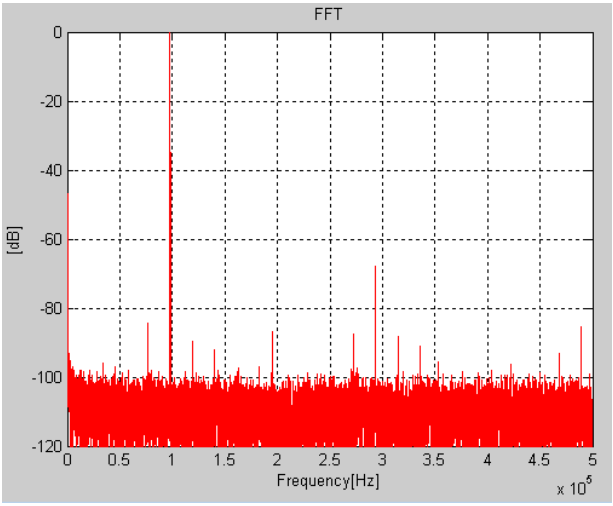
The specifications of the SAR ADC for automotive applications are a resolution of 12 bits at a maximum operation bandwidth of 1 MS/s. The proposed SAR ADC utilizing the integer-based CDAC with redundancy is measured to have an SNDR, SFDR, and ENOB of 67.2 dB, 86.6 dB, and 10.9 bits, respectively when operating at 1 MS/s. The power consumption is 1.8 mW with a voltage supply of 5 V. The input voltage range is from 1.25 V to 3.75 V, for a peak-to-peak voltage of 2.5 V. The measurement FFT plot and the measurement summary are both shown in Fig. 4.6.4.

The measurement environment is as follows: the input signal was given differentially by using Audio Precision 2722, which is commonly used to generate high-resolution signals for audio applications. However, the bandwidth is limited, and therefore an input of 100 kHz has been applied. It should be noted that to show that the ADC performs in the Nyquist region, measurements were also done using the Agilent 81150A as the input signal generator. Here, the ENOB was 10.3 b for Nyquist rate, and for comparison, 10.4 b at 100 kHz. Also for automotive application purposes, measurement in the temperature range of -40 to 150 showed only a drop of less than 0.15 ENOB from the peak value.

The linearity of the proposed SAR ADC has also been measured, and the results are given in Fig. 4.6.5. As shown, the DNL is measured to be from -0.76 to +0.58 LSB, and the INL is from -1.1 to +0.55 LSB. It should be noted that even with no calibration,

the linearity figures are very competitive.

Unfortunately, the high supply voltage and the large dimensions of the automotive



Parameter	Value
Supply voltage	5 V
Technology	0.5 um 1P4M
Resolution	12 bits
Sampling Frequency	1 MS/s
Input Frequency	100 kHz
SNDR	66.66 dB
ENOB	10.8 bits
FoM	2.019 pJ/conv.-step
Power consumption	3.6 mW
Area	550 um x 300 um

Fig. 4.6.4 Measurement results of the proposed SAR ADC using integer-based split-CDAC with redundancy implemented in 0.5um CMOS process..

semiconductor process limit comparison with the figures-of-merit of other prior works due to the relatively high power consumption. The digital power alone stands at 77% of the total power consumption. Currently, according to the figure-of-merit equation widely used to compare the performance of ADCs given by the equation

$$\text{figure of merit } = \frac{\text{power}}{2^{\text{ENOB}} \times f_s} \tag{4.6.1}$$

the FoM of the proposed SAR ADC sits at 0.94 pJ/conversion-step.

However, it can be pointed out that the resolution is maintained at a 12-bit level even without any calibration techniques, even for a reduced input range of half the supply voltage. This indicates that an even higher resolution could be achieved with the proposed technique, and also that it may be used effectively with finer technologies.

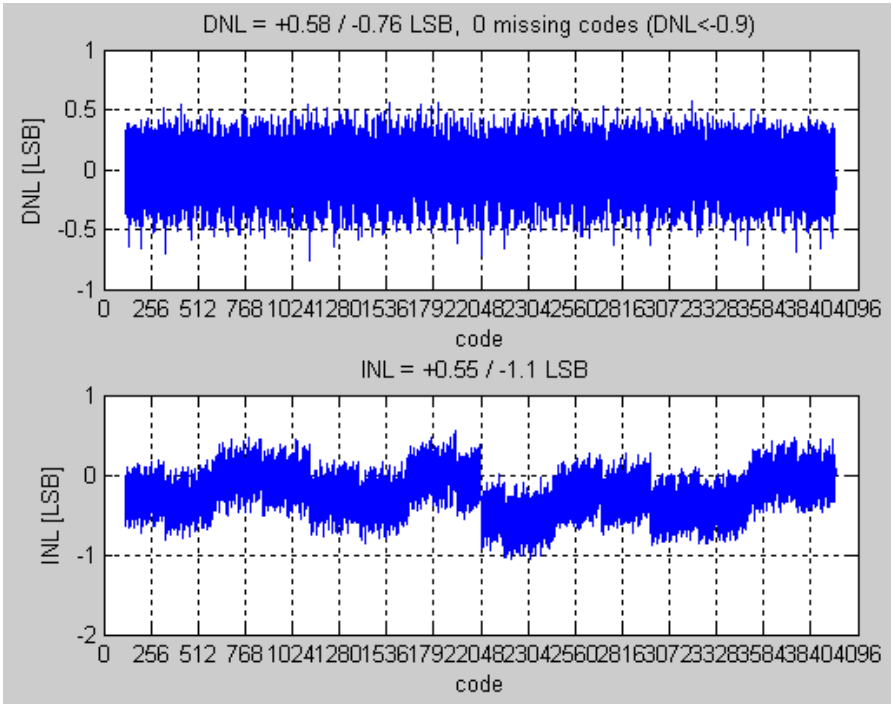


Fig. 4.6.5 Linearity measurement results of the proposed SAR ADC (DNL, INL).

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 CONCLUSION

In this thesis, a study was conducted on the performance of the SAR ADC. First, the conventional structure and the operation principles were examined. Then, potential factors that may degrade the performance of the SAR ADC in aspects of resolution and operation bandwidth were presented. A deeper look at each factor was conducted so as to gain insight on the problem and potential solutions. Then, prior works which try to solve the resolution and speed limits of the SAR ADC were given.

Prior to proposing solutions, the high-level model of the SAR ADC is presented. This model was used in the designing of the SAR ADCs that were proposed, and is helpful in predetermining the effects of various design considerations before designing in the transistor level. It supports many architectures, and is especially useful in the designing of the CDAC and distributing the weight and therefore redundancy. The effect of mismatch can also be seen clearly for choosing the right structure and capacitor sizes.

Next, this paper proposes a technique which tackle the same problems in the aspect of resolution. The technique is the SAR ADC using a integer-based split-capacitor DAC exploiting redundancy. The mismatch problem in the widely used split-capacitor DAC of the SAR ADC is a problem which many have tried to solve. The proposed technique allows to design a CDAC that only uses integer multiples of the unit capacitor, without any ratio errors. No additional circuitry for calibration or additional reference voltages are needed. This is achieved by exploiting redundancy and the degree of freedom in choosing the ratio of the capacitors. A prototype has been implemented for automotive applications in automotive semiconductor process of 0.5 um, and measurement results show that the proposed CDAC maintains the resolution of the specified 12 bits.

5.2 FUTURE WORK

The presented work in this thesis has a novel structure and new ideas regarding the designing of the SAR ADC. In further study which will be included in the appendix due to the incompleteness, the scheme that can improve the bandwidth of the SAR ADC is given. A technique called the SAR ADC using threshold-configuring comparators is presented for ultrasound imaging systems. By using the threshold comparator as a coarse ADC, the settling time of the capacitor DAC is relieved and thus the SAR is able to operate at faster conditions. Redundancy is optimally distributed throughout the conversion stages so that the TCC resolution is not the bottleneck. The SAR ADC was

designed in 0.18um 1P4M CMOS technology with a 1.8V supply voltage. Simulation results show that at 35 MS/s with a near-Nyquist 15.1MHz input of differential peak-to-peak amplitude of 1.6V, the SNDR was 68.4 dB, resulting in an ENOB of 11.07 bits. Power consumption is 5.69mW, and the figure-of-merit is 75.6 fJ/conversion-step. Simulation results compared with similar SAR ADCs of the same technology length show excellent competitiveness.

APPENDIX

SAR ADC USING THRESHOLD-CONFIGURING COMPARATOR FOR ULTRASOUND IMAGING SYSTEMS

APX.1. INTRODUCTION

The appendix introduces a new application for the SAR ADC; ultrasound imaging systems. Due to the incompleteness of the work, it is not inserted in the formal chapters of the thesis. However, the work shows potential and novelty and therefore has been inserted in the appendix.

Ultrasound imaging is a technology that is used widely in medical and clinical applications such as radiology, obstetrics, vascular and cardiology, and the market is growing ever larger. Ultrasound imaging systems are gaining popularity due to the fact that they can obtain real-time information with little cost. Moreover, the operation is non-ionizing, and therefore safe for various bio-medical applications.

The conventional ultrasound imaging receiver consists of the probe, the analog

coaxial cable, and the image processing system. Transducers inside the probe generate analog signals, and the signals are sent via the analog coaxial cable to the image processing system, where they are digitized by the analog front-end (AFE) circuits inside the image processing system. These digital signals are readily displayed as images for the user. For higher performance, the number of transducers inside the probe are currently increasing. For example, with the use of multi-channels, the transducers number will be a few hundred up to a few thousand depending on the imaging mode. For example, with the Doppler brightness modes, the number of channels are 1 – 256, whereas the 3D and 4D imaging modes require 1024 – 4096 channels. This results in a bulkier analog cable, thus the cost of the ultrasound imaging systems increases. However, if the AFE of the image processing system were to be placed inside the probe, then the bulky analog coaxial cable could be removed, and the image data could be transmitted digitally. Digital transmission of data is much easier and cost-efficient than analog transmission. Moreover, it is further potentially suitable for portable and wireless probes. Therefore, the motivation of this work is in the relocation of the AFE inside the image processing system so that it is placed within the probe with the transducers.

Power consumption is the critical issue when the AFE is located inside the probe. A conventional ultrasound imaging system AFE consists of a low-noise amplifier, a programmable gain amplifier and attenuator, an anti-aliasing filter, and an analog-to-digital converter (ADC). The ADC is typically a 12-bit pipeline structure. However,

although the pipeline ADC has a high resolution with high speed, it is very power-hungry and consumes near half of the total power consumed in the AFE, as can be seen with the popular commercial solution examples.

This work proposes an SAR ADC that can replace the high-power pipeline ADCs in the conventional ultrasound imaging system AFE. The operation bandwidth of the SAR ADC is enhanced by the use of a threshold-configuring comparator (TCC) so that the bandwidth requirements of the ultrasound imaging system are met, and the pipeline ADC can be replaced.

First, the background knowledge and motivation will be presented. Then, the concept of the threshold-configuring comparator will be introduced, with prior works of similar concepts. Next, proposed SAR ADC using the TCC will be presented, with details on the operation principle and the sub-blocks consisting the architecture. The circuit design is illustrated, and the implementation of a prototype SAR ADC using the TCC is shown. Finally, the simulation and measurement, and the discussion on these results are presented.

APX.2. MOTIVATION

APX.2.1. CONVENTIONAL ULTRASOUND IMAGING SYSTEM

The ultrasound imaging system has gained much popularity due to its numerous advantages compared to other imaging techniques that can generate similar output. The

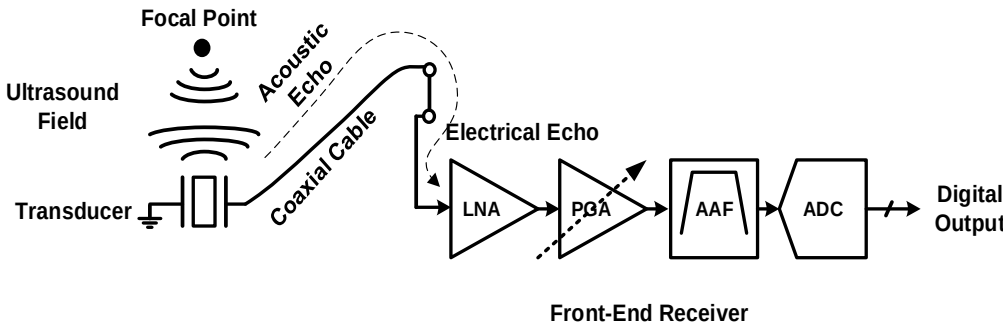


Fig.Apx.2.1 Block diagram of the conventional ultrasound imaging system.

building components of the conventional ultrasound imaging system receiver will be illustrated in this section, as well as the part each block plays in constructing an ultrasound image.

The conventional ultrasound imaging system consists of the probe, analog coaxial cable, and the image processing system. The block diagram of the conventional ultrasound imaging receiver is shown in Fig. Apx.2.1 [Apx.2.1]. As the name suggests, the probe is the block where the ultrasound signal is sent towards the target of interest. The probe contains elements called transducers, which are the physical blocks that actually emit the acoustic pulses. These pulses then propagate through the medium towards the designated target of interest. Upon reaching the target, the pulses will now be reflected back the way they came. Theses reflected echo signals are then received by the same transducers inside the probe, and the converted into electrical echo signals.

Now the probe and its transducers have finished their part.

The electrical echo signals are transmitted through a cable, which connect the probe and the image processing unit. Since the echo signals can be very small in amplitude and therefore sensitive to even subtle changes in the surrounding environment, the connecting cable is an analog coaxial cable. The coaxial cable can transfer signals even in noisy environments because the signal line is surrounded by a thick noise-blocking layer. However, the cost of a coaxial cable that can transmit analog signals is quite significant, and the cost rises even higher as the coaxial cable needs to deal with many signals from multiple channels. For example, in certain performance-enhancing modes as explained previously, the number of channels will be in the few thousands. An analog coaxial cable that could transfer these multiple analog signals would be very expensive and bulky. This raises the cost of the system, and moreover denies the opportunity for a more compact and possibly portable solution.

The electrical echo signals transmitted through the cable is received by the ultrasound imaging unit. More specifically, the signals are received by the AFE inside the image processing unit. The AFE converts the analog signals into digital signals for the back-end of the image processing unit to generate images to be displayed on the monitor for the user. The detailed operation and the specific building blocks of the AFE is explained in the following section.

The performance specification of the ultrasound imaging system is a function of the specifications of the individual blocks. However, the performance is generally

shown by the performance of the receiver path of the system. If looked into more closely, the performance of the receiver is dominated by the performance of the AFE. Although the transducers inside the probe and the coaxial cable all contribute to the performance, these are typically issues on the choice of products and materials to use. The specifications of the AFE of the receiver is the actual bottleneck in the whole system performance, and in the designer's point of view, choosing the specifications of the AFE is the critical factor in deciding the performance of the whole system. Some of the more important specifications include the signal-to-noise ratio (SNR), resolution, dynamic range (DR), and the frame rate [Apx.2.2-4].

APX.2.3. DESIGN CONSIDERATIONS OF THE ANALOG FRONT-END

Ultrasound imaging systems are used in such numerous and diverse applications that it is very difficult to define general specifications. Therefore, the specifications and design considerations in the section will be in a broad sense. The typical ultrasound imaging system used in medical applications must cover a signal bandwidth of the reflected acoustic echo signal. This differs from application to application, but it can be generalized to the range of a few MHz up to 20 MHz. Widely used commercial products therefore must cover the whole signal bandwidth with a maximum frequency of 20 MHz in order to be used in numerous applications. However, this comes at an unnecessary cost increase for fixed applications, especially if the frequency of interest

is much lower than the maximum ultrasound frequency.

The image quality that is required varies as well from application to application. However, a look at today's popular commercial products suggests that the widely used resolution range is from 8 to 12 bits. The AFE must ensure that even for small reflected echo signals, the signal power is much larger than the noise power. Therefore the signal must be amplified without introducing excessive noise, and moreover the gain must be large enough to suppress the input-referred noise. Also, for maximum SNR performance, it must be able to control the gain so that the amplitude of the signal fits the full-scale range of the ADC without saturation. As the initial amplitude of the echo signal varies according to the environment and focus depth, there must be some form of variable gain control, and the range of the amplification and attenuation is also an important specification.

Considering the points mentioned above, the challenges in designing the AFE can be summarized as the following. First, the signal-path chain must operate with low noise in order to preserve a high sensitivity and accuracy. Second, a high gain is essential to attenuate the input-referred noise of proceeding blocks in the signal chain, particularly with a weak reflected input signal. On the other hand, the amplifier must also be able to provide a low gain for large ultrasound signals in order to avoid saturation. Third, an adequate operation bandwidth is required to minimize harmonic distortion and accommodate high-frequency imaging signals. Finally, while monolithic CMOS implementation is in high demand due to the much lower cost, it presents

obvious drawbacks in terms of noise, linearity, and bandwidth, in comparison with its bipolar or bi-CMOS counterparts. Hence, the design of an AFE involves careful considerations on multiple tradeoffs among noise, linearity, bandwidth, stability, power, and process.

APX.2.4. COMPONENTS OF THE ANALOG FRONT-END

The typical AFE of the ultrasound imaging system receiver consists of the low-noise amplifier (LNA), programmable gain amplifier (PGA), anti-aliasing filter (AAF), and the ADC. The low-noise amplifier acts as a preamplifier that amplifies the returning echo signals. Since these signals can be very small compared to the supply voltage of the circuits, the amplification process must suppress additional noise generation as much as possible. The gain may have a fixed value or a variable value, but typically the range is not very wide because the main task of the LNA is amplification with noise suppression, not acquiring a wide dynamic range. The input-referred noise level must be low enough for the ultrasound signals to be detected with the desired resolution. Recent works achieve levels of up to a few nV/√Hz with standard CMOS technology.

The programmable gain amplifier then amplifies the output signal of the low-noise amplifier so that the signal magnitude is now the full-scale of the input range of the ADC. Depending on the signal level, the PGA may also include an attenuator, so that it can also decrease the output signal from the LNA, if it is larger than the full-scale of

the following ADC and the end of the AFE. Whereas the LNA was primarily focused on the amplification of the input signal with as small noise as possible in order to reduce the input-referred noise, the main purpose of the PGA is to maximize the signal within the input range of the ADC. The input-referred noise is not as critical as the LNA since the PGA is behind in the signal line.

The anti-aliasing filter is included in the main signal path. The user only needs information in the bandwidth of the ultrasound range, which is approximately under 20 MHz or less, depending on the specific application. However, the reflected acoustic signal will contain frequencies above the desired range, and noise will have been included in the process of amplifying by the LNA and the PGA. Therefore, the AAF acts as a low-pass or a band-pass filter, so as to filter the out-band noises from the signal bandwidth.

Finally, at the end of the analog signal path is the ADC. The ADC digitizes the amplified and filtered electrical echo signal, converting the information into digital data for the following image processing unit to generate the ultrasound images. The ADC bandwidth must of course cover the range of ultrasound frequencies, and therefore the operation speed is from a few to tens of MHz, depending on application. This is why Nyquist ADCs are used rather than oversampling types. The resolution of the ADC is likely to bind the resolution of the total system, since the noise level of the preceding amplifiers are quite easily designed to be higher than the resolution of the Nyquist ADC. Typically the ADC of the AFE requires enough signal-to-noise ratio (SNR) to

accommodate the preceding amplifier chain, therefore approximately 12 bits.

APX.2.5. COMMERCIAL EXAMPLE OF THE AFE

To gain more insight on the specifications of the AFE and the design of its components, a widely used commercial AFE solution will be examined. The AFE5808 from Texas Instruments is a commercial solution for a wide range of ultrasound applications. It is intended for wide usage in medical ultrasound imaging and nondestructive evaluation equipments. The performance is high-end, allowing it to be used for a wide range of products. The block diagram of the AFE5808 is given in Fig. Apx.2.2. [Apx.2.5]. The blocks in the main signal path consist of a LNA, a voltage-

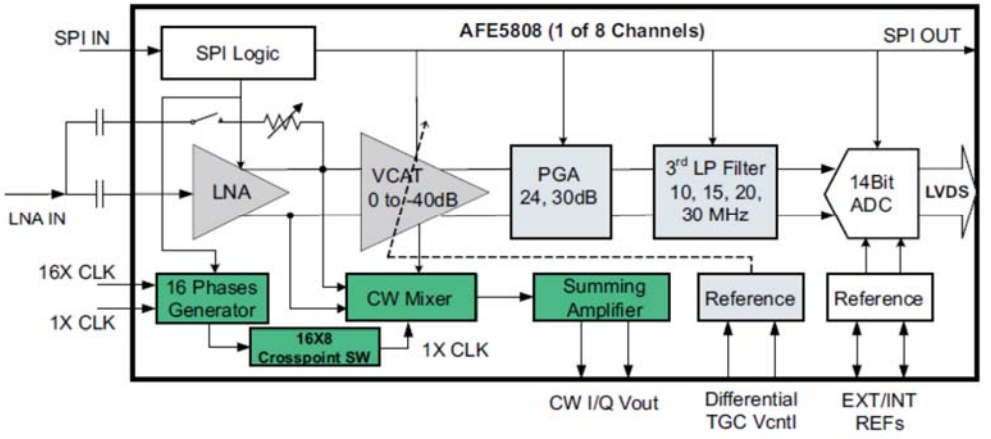


Fig. Apx.2.2 Block diagram of widely used commercial analog front-end for receiver of ultrasound imaging systems [Apx.2.5].

controlled attenuator, a PGA, a low-pass filter, and an ADC at the end. It can be seen that this is basically the same structure described in the above sections.

The specific specifications are as follows: the noise level is at 0.75 nV/√Hz at an operation speed of 65 MS/s with a resolution of 14 bits. At 40 MS/s, the noise level is 1.1 nV/√Hz. In these operation speeds respectively, the power consumption per channel is 153 mW and 98 mW. The specifications are extremely high and therefore, this solution is very popular in the ultrasound market. However, as all thing, it comes at a high cost. The noise level is kept to very low values; this is due to the fact that the process used to design the blocks in the chip is not all standard CMOS, but rather the better-performing bipolar technology has been used in the preceding amplification stages for low-noise characteristics. Also, although the resolution is very high, so that it may suit the purpose of the majority of ultrasound applications, the power consumption is quite extravagant. A trade-off can be considered here: the high performance of the AFE versus the power consumption. Many ultrasound imaging applications do not need the full range bandwidth of 20 MHz, and the resolution of 14 bits is rarely used. Moreover, to adapt to the ever-growing number of channels due to massive transducer arrays and the demand of portability and handheld devices, cutting down on the power consumption is a very important need in the designing of ultrasound imaging receiver AFEs.

A breakdown of the power consumption of the signal bath of the AFE5808 gives some insight on how to potentially reduce this power consumption. To recall, the power

consumption per channel was 153 mW and 98 mW respectively at operation speeds of 65 MS/s and 40 MS/s. The power consumption of the ADC of the AFE is 59 mW and 46 mW at their respective speeds. This is calculated to be around 39 – 47% of the total power consumption. The type of ADC used in AFE5808 is the pipeline ADC. The pipeline ADC offers fast sample rate and moderate resolution, and therefore is the ideal choice for ultrasound imaging applications in terms of bandwidth and resolution. This can be seen in Fig. X, by noticing where the pipeline ADC lies on the plot. The bandwidth of the ultrasound imaging, which is up to 20 MHz can be easily achieved by pipeline ADCs and flash ADCs. The resolution of 10 – 12 bits is met by pipeline ADCs, SAR ADCs, and oversampling ADCs. However, the major weakness of the pipeline ADC is of course its high power consumption compared to other ADCs in the all-round performance range. The pipeline ADC consists of multiple stages with a high-gain op-amp within each multiplying digital-to-analog converter (MDAC) stage. This fact is even worsened with finer technology processes with lower supply voltage, as it becomes more difficult to design op-amps with sufficient gain.

The earlier sections have discussed the following issues. First, an introduction to the conventional ultrasound imaging system was given. It was outlined that the power consumption must be reduced in order to locate the AFE inside the probe for potential wireless applications. After referencing a popular commercial product of ultrasound imaging AFE, the ADC was found to consume the most power. The ADC that is used is a pipeline ADC, which is widely adopted for its relatively high operation speed and

moderate resolution. The SAR ADC was then introduced, as it was seen as a potential candidate for replacing the power-hungry pipeline ADC. SAR ADCs are extremely low-power consuming, but are among the slowest types of Nyquist ADCs. The conventional SAR ADC was presented in the previous chapters. The structure was shown to fully understand the characteristics of the SAR ADC, and then the operation principle was illustrated. The binary search algorithm and the following successive approximation technique is the intrinsic limit to the operation speed. To learn about the possible improvement in bandwidth terms, a speed breakdown in the operation of the conventional SAR ADC was performed. Moreover, some recent techniques that challenged the speed limit were presented.

In the following section, an SAR ADC with enhanced operation speed is proposed. The use of a threshold-configuring comparator (TCC) alleviates the delay time in the settling time of the capacitor DAC. Redundancy is distributed precisely throughout the stages so as to tolerate the decision errors that arise with further speed enhancement. A new technique so that the capacitors in the DAC are all integer-multiples of the unit capacitor is also proposed. The SAR operates with asynchronous logic for further speed enhancement.

APX.3. THE PROPOSED SAR ADC USING THRESHOLD-CONFIGURING COMPARATOR

APX.3.1. STRUCTURE OF THE PROPOSED SAR ADC USING THRESHOLD-CONFIGURING COMPARATOR

An SAR ADC with various techniques that improve the performance is proposed. The focus is on reducing the required settling time of the voltage of the capacitor DAC. The output voltage of the capacitor DAC must settle within one least significant bit (LSB), or else the difference would result in an error that degrades the effective resolution. Moreover, since the voltage steps of the capacitor DAC are larger for the most significant bits (MSBs) – half of the common-mode voltage V_{CM} for the first cycle, quarter of V_{CM} for the second cycle and so on – the worst case settling time is likely to occur at the MSB bit, but this worst case settling time must be allocated at for every cycle. We remove the large settling times of the 6 MSB cycles of the capacitor DAC by the use of a TCC [Apx.3.1-3]. The proposed SAR ADC is a TCC and DAC hybrid structure. The block diagram in shown in Fig. Apx.3.1.

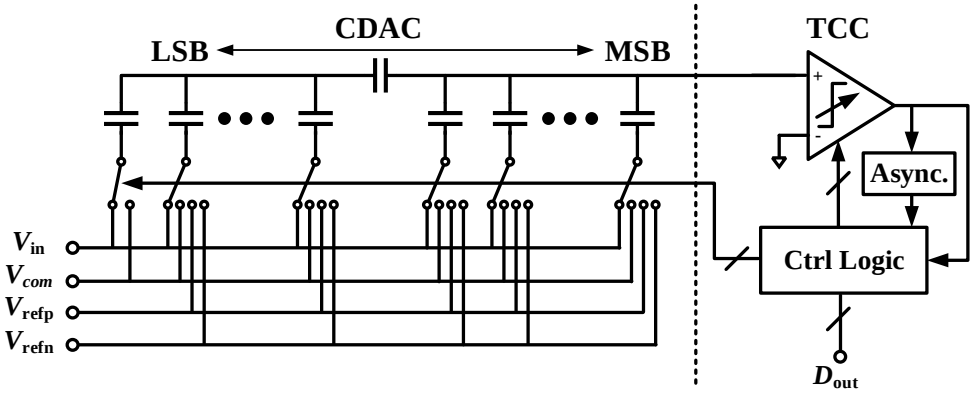


Fig. Apx.3.1 Block diagram of the proposed SAR ADC using threshold-configuring

APX.3.2. OPERATION PRINCIPLE OF THE SAR ADC USING THRESHOLD-CONFIGURING COMPARATOR

The TCC acts as an independent 'coarse ADC', achieved by configuring the internal threshold of the comparator. Thus determining the 6 MSBs without varying the capacitor DAC voltage, which takes a great deal of time to settle at every cycle, reduces the worst case settling time, which would have been needed to be allocated to every cycle. The input is sampled on the capacitor DAC as in the conventional SAR ADC. Then, comparisons are made and digital bits are generated by the TCC, without making any changes to the capacitor DAC output voltage. When 6 conversion cycles are complete, the 6 MSBs are applied to the capacitor DAC simultaneously for a single switching. Then, for the remaining conversion cycles, the LSB bits are decided

consecutively as a conventional SAR. The use of TCC for the 6 MSBs merges the 6 settling times at each MSB cycle into a single settling time, and therefore enhancing the conversion speed. The waveforms that illustrate the principle of the SAR ADC using TCC is shown in Fig. Apx.3.2, with an example of a 6-bit SAR with 3-bit TCC. Compared to the example shown in Fig. 2.2.4, it can be seen that the MSB cycles do not change the output voltage of the DAC. These are done now internally inside the TCC. It should be noted that the voltage variation at the MSBs were in fact the largest,

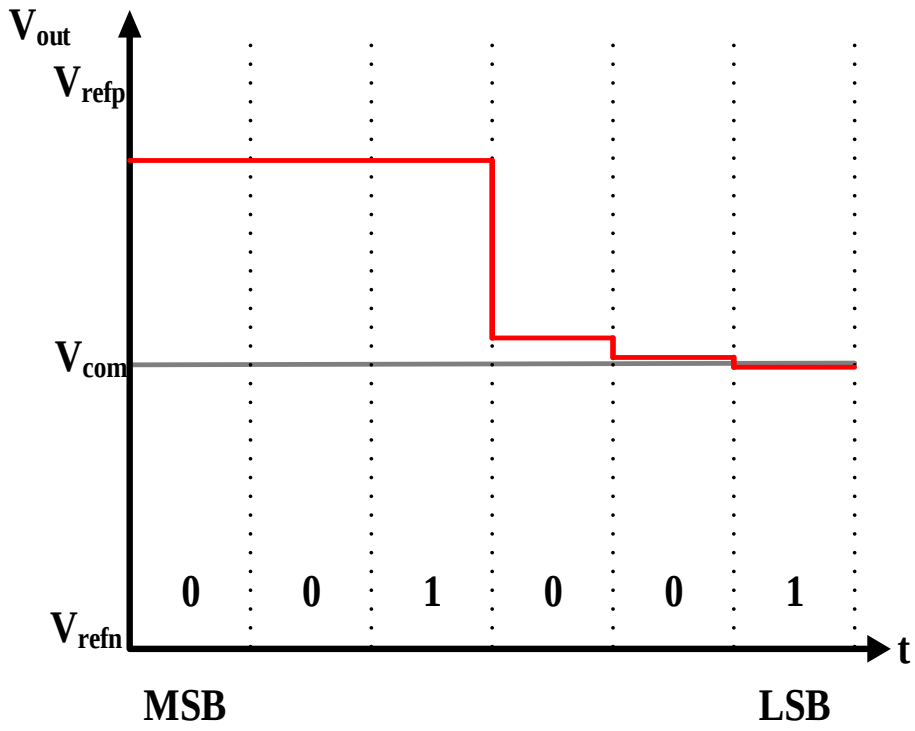


Fig. Apx.3.2 Operation principle of the proposed SAR ADC using threshold-configuring comparator.

so removing the allocated times for these large voltage variations to settle will contribute to speeding up the operation of the proposed SAR ADC.

Using the TCC as a 'coarse ADC' results in a resolution limit that is much lower than the desired 12 bits. Therefore, redundancy is distributed accordingly in the capacitor DAC in order to compensate for the decision errors that may have occurred in the TCC. Two extra conversion cycles distribute the redundancy for a total of 14 conversion cycles. The 14 digital output bits, D_{out}, are post-processed externally. This is not a problem in our application of ultrasound imaging systems, as there is a image-processing system that receives D_{out}. Precise distribution of redundancy also allows the capacitor DAC to be only multiples of unit capacitors, which is a great advantage in mismatch and layout issues that can limit the resolution of the capacitor DAC in high-resolution SAR ADCs. The SAR operates with asynchronous logic, allowing faster operation and less power consumption due to the absence of internal clock generators.

APX.4. CIRCUIT DESIGN

APX.4.1. THRESHOLD-CONFIGURING COMPARATOR

The threshold configuring comparator is a comparator that has control capabilities on its threshold. It is typically used to cancel the offset in comparators, but the same techniques can be used to induce intentional offset. There are various ways to induce

intentional offset in comparators. Figure Apx.4.1 shows a dynamic latch-type comparator. Adding asymmetrical capacitive loads at the output nodes of V_{outp} and V_{outn} is one way to configure the threshold voltage [Apx.3.1]. However, this method is not suitable for high-speed applications, as the charging of the load capacitors slow down the operation . The size of the input transistors may be controlled asymmetrically as an alternative method. However, this is used for generating built-in thresholds or offsets rather than a dynamic threshold that must be configured real-time. In our work, current sources are inserted in parallel to the input transistors [Apx.3.2]. This method changes

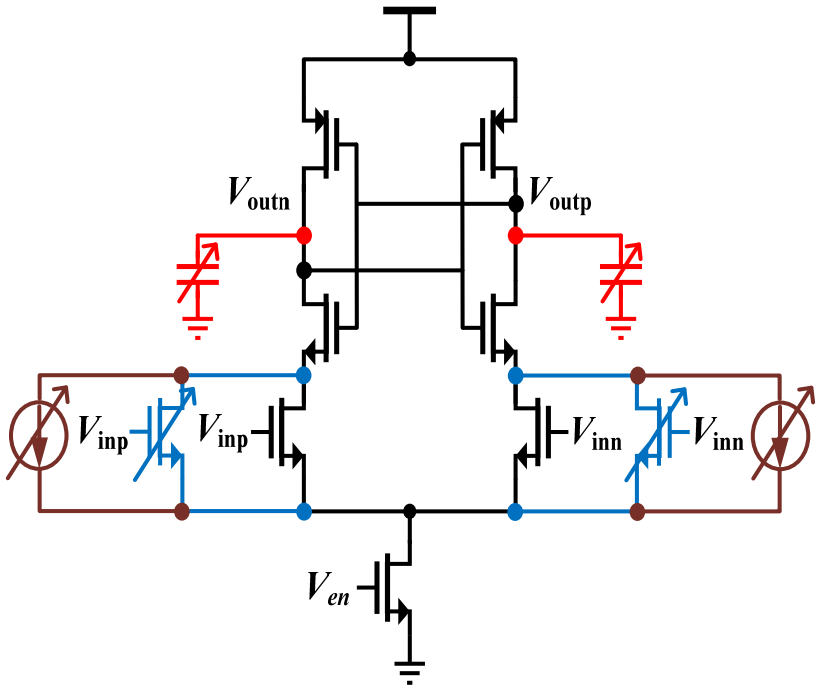


Fig. Apx.4.1 Schematic of the dynamic latch-type comparator with various methods of configuring the threshold voltage.

the currents that flows through the two branches of the comparator, and therefore can control the threshold.

In the proposed SAR ADC, the TCC has been used as a 'coarse ADC' for the MSBs, and then the threshold is set to zero and the TCC operates as a typical comparator for the LSBs. The schematic diagram of the TCC is shown in Fig. Apx.4.2. It is based on the double-tail dynamic comparator structure with binary-weighted parallel current sources, shown only on one side for simplicity, M_{N4}-M_{N8}. For linearity, the parallel current sources are controlled with the common-mode voltage V_{cm}. It is stated that when using a TCC, the maximum resolution achievable is around 6 – 7 bits without calibration [5.3.1-3]. In our work, there are 5 binary-weighted current sources on each branch of the input stage of the comparator, and therefore a total of 6 most significant bits are generated by the TCC. For the TCC and the capacitor DAC to work in a 'coarse-fine' operation, the TCC weight for each cycle must match the DAC weights. However, the TCC weight may be changed due to the local mismatch in transistors, variation in the driving V_{CM}, voltage fluctuations due to kickback noise and so on. Moreover, the DAC weight is also attenuated from the designed values due to the parasitic capacitances on the output node. These parasitics, which may be from the comparator, switches, or wiring metals in the layout, are a trivial issue with the conventional SAR. However, in the SAR ADC using TCC as a coarse ADC, mismatch in the TCC and the DAC weights causes non-linearity, and will possibly generate missing codes. Therefore, to calibrate for the weight mismatch, the bias current of the

TCC can be controlled to adjust the TCC weight.

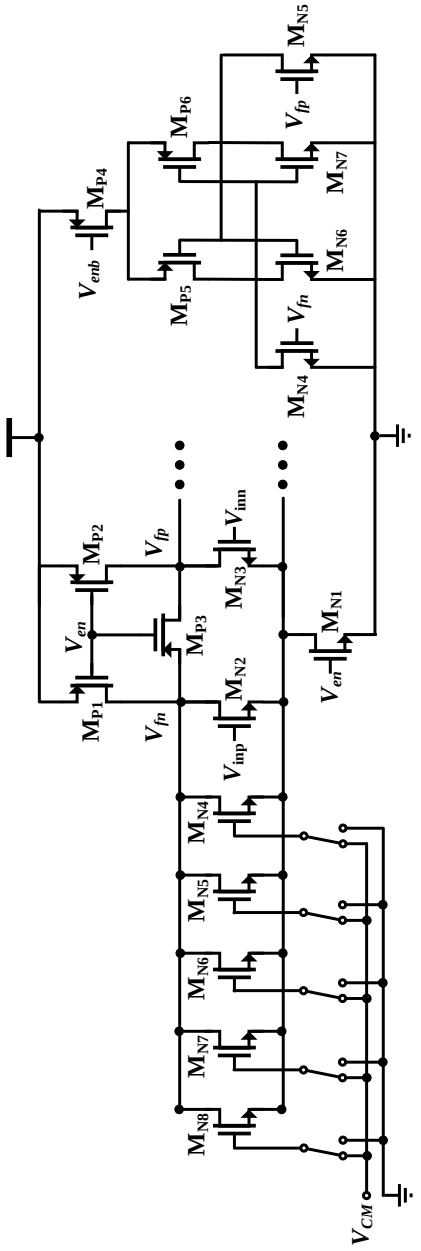


Fig. Apx.4.2. Schematic of the dynamic double-tailed threshold-configuring comparator..

APX.4.2. CAPACITOR DIGITAL-TO-ANALOG CONVERTER

The capacitor DAC, as shown in Fig. Apx.4.3, is a V_{cm}-based structure with bottom-plate sampling. As explained above, redundancy has been inserted in the capacitor DAC in order to compensate for the low-resolution of the TCC. Therefore, the total stages in the capacitor DAC is now for 14 bits instead of 12. The redundancy is distributed as shown in Table Apx.4.1. The TCC determines the 6 MSBs, and since the resolution of the TCC is under 7 bits, there is a redundancy of 64 LSB or more, which corresponds to 5 bits, until the sixth stage. The 6th – 7th stage capacitors are the capacitors that actually induce the redundancy for the previous stages. As can be seen, the rest of the capacitors are weighted in a binary fashion, that is, the capacitor size is double the following stage capacitor size. The first capacitor size is an exception, as it has been reduced to make the total sum of the capacitors 2048 C_{unit}

The top-plates of the capacitors are shorted, and then split into two by the bridge capacitor connected in series. Inserting the bridge capacitor in series inside the capacitor DAC is an effective way of reducing the total capacitance value, or else it would rise exponentially as the number of resolution bits increases, reaching impractical values at above 10 bits. The bridge capacitor size is given as the following equation

$$C_{bridge} = \frac{C_{LSB\_total}}{C_{MSB\_last} - 1} \text{ ..} \qquad \text{(Apx.4.1)}$$

C_{LSB_total} is the total sum of the capacitance of the LSB-side, and C_{MSB_last} is the

capacitor value of the last capacitor stage of the MSB-side. In a conventional binary-weighted capacitor DAC, this would result in a C_{bridge} value of

$$C_{bridge} = \frac{2^k}{2^k - 1} C_{unit}, \quad \text{(Apx.4.2)}$$

where k is the number of stages of the LSB-side. As can be seen in the above equation, this results in a non-integer unit capacitance. This can be a serious problem for higher-resolution SAR ADCs, because the non-integer unit capacitance has critical layout and matching issues.

There are some differences from this integer-based split-capacitor CDAC and the CDAC used in the SAR ADC for automotive applications. First, in this version, bootstrapped switches have been used for the input switches. This is because the operation bandwidth of the ultrasound application is must higher than that of the automotive application. Therefore bootstrapping was used in order to sample the inputs without sampling errors due to the high resistance of the input switches. Another fact is that the unit capacitor size has been reduced from approximately 100 fF in the automotive application to 25 fF in this version. This was again due to the higher bandwidth, since the specifications are much more tight in the current application. Of course, Monte carlo simulations have been simulated with the model presented in Chapter 3, and also in the transistor level to ensure a 12-bit resolution.

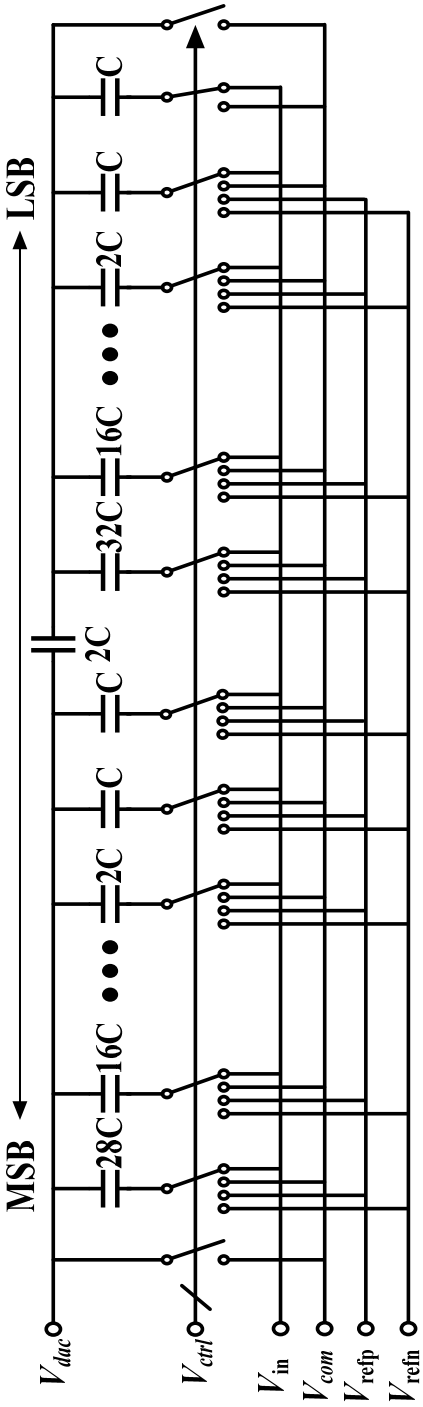


Fig. Apx.4.3 Schematic of the capacitor DAC of the proposed SAR ADC.

Table. Apx.4.1 Capacitor size, weight, and redundancy of each stage in the capacitor DAC.

Stage No.	**1**	**2**	**3**	**4**	**5**	**6**	**7**
Size [C_{unit}]	28	16	8	4	2	1	1
Weight [C_{unit}]	924	528	264	132	66	33	33
Redundancy [LSB]	196	64	64	64	64	64	31
Stage No.	**8**	**9**	**10**	**11**	**12**	**13**	**Dummy**
Size [C_{unit}]	32	16	8	4	2	1	1
Weight [C_{unit}]	32	16	8	4	2	1	1
Redundancy [LSB]	-	-	-	-	-	-	-

APX.4.3. CONTROL LOGIC OF THE SAR ADC USING TCC

The control logic of the SAR ADC using TCC can be divided into two parts, the controls for the MSBs which use the TCC, and the conventional logic for the LSBs. The TCC control logic was implemented so that dynamic registers were also be able to be used for the control of the TCC. In order to do so, the parallel sources of the TCC are controlled in a ‘top-down’ method. This is shown in Fig. Apx.4.4. The bottom-up method and the differential control all proved to be non-linear with binary-weighted parallel current sources. Therefore, in prior work with the TCC, a look-up table has been used for the linear control of the TCC. However, with the ‘top-down’ method, linearity for the resolution of 6-bits can be maintained. This allows only one switching

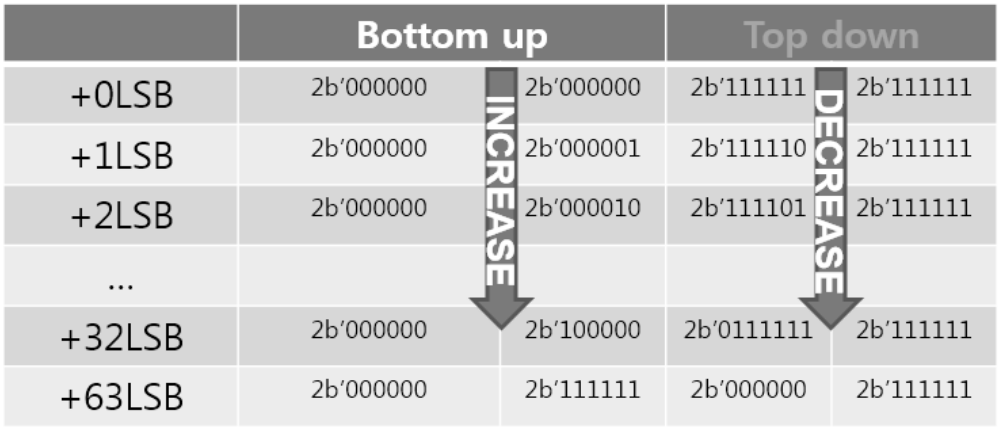


Fig. Apx.4.4 Top-down control scheme of the parallel current sources in the TCC allow one-bit change at a time with linearity conserved.

control code at a time, and therefore a slight modification of the conventional successive register control can be used without any lookup tables for simpler architecture and faster speed.

An SAR ADC needs an internal clock of the number of bits times the sampling frequency. For example, a 14 bit (including redundant bits) ADC that runs at a sampling frequency of 35 MS/s would need an internal clock of approximately 500 MHz. Supplying this kind of high frequency clock off-chip is a very difficult task, and generating it internally by a clock generator results in high power consumption, which would degrade the main advantage of the SAR ADC. Therefore, asynchronous logic is widely used in high-speed high-resolution SAR ADCs. The comparator differential outputs, which are reset to the same value when turned off, are driven to different values

with a valid output. These differential outputs are used to generate a ready signal, indicating that the comparison is complete and the digital logic control can create the according control signals. Other than power consumption, using asynchronous logic now saves conversion time, since the worst-case comparison time does not have to be allocated to every conversion cycle, as must be done in a synchronous operating ADC.

Another scheme change in order to raise the operation bandwidth is the usage of true single-phase clock (TSPC) registers for the dynamic register bank in the core of the SAR ADC control logic. The TSPC register is known for faster speed due to less logic delay, however it has a disadvantage when having to hold a value for a long time due to leakage. However, the successive dynamic registers of the SAR ADC control do not have to hold values for a long time when in operation, so TSPC registers were used. These in simulation freed up over 100 ps more in timing margin, which is quite a lot when considering the internal frequency in the hundreds of MHz.

APX.5 LAYOUT AND EXPERIMENTAL RESULTS

APX.5.1. LAYOUT

The proposed SAR ADC utilizing TCC has been designed in 0.18um CMOS 1P4M CMOS process. The layout of the SAR ADC is shown in Fig. Apx.5.1. The digital control logic is in the center, and the capacitor arrays forming the differential

capacitor DAC are symmetrically drawn along with the switch network. For input sampling, bootstrap switches have been implemented. The TCC is below the digital control logic. The digital control logic was place at the center for minimized control signal wiring. Since the SAR ADC is intended for high-speed operation, the digital control logic is the bottleneck in the operation speed. Minimizing the parasitic capacitance of the internal and output control signals of the logic is extremely important. The area of the SAR is 560 um x 380 um. The basic floorplan is similar to that of the SAR ADC for the automotive applications. The layout techniques on the capacitor array in Chapter 4 also have been applied to this design.

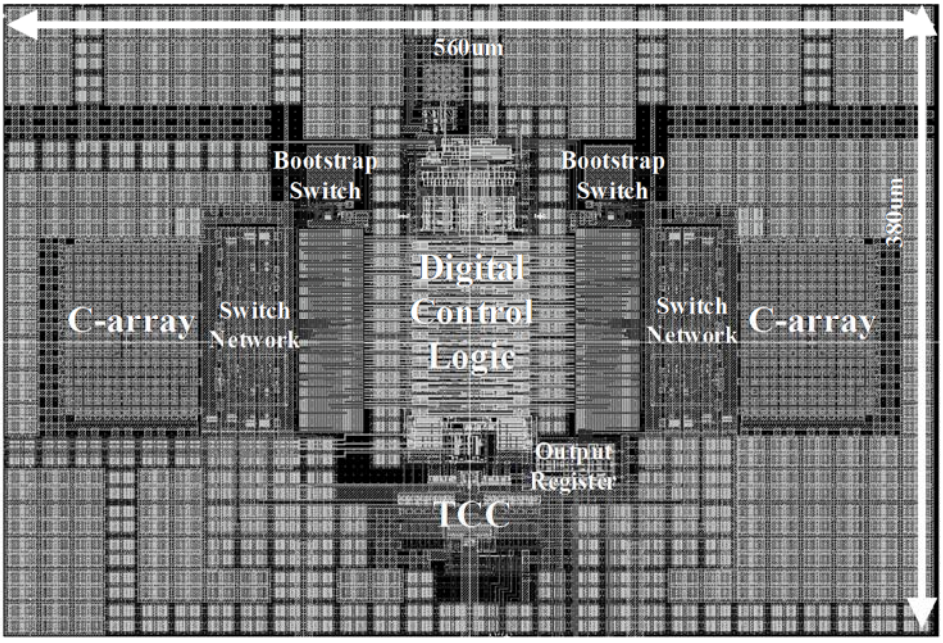


Fig. Apx.5.1 Layout of the proposed SAR ADC using threshold-configuring comparator.

APX.5.2. SIMULATION RESULTS

Simulation results show that at a sampling frequency of 35 MS/s with a near-Nyquist input of 15 MHz with a differential peak-to-peak amplitude of 1.6 V, the SNDR is simulated to be 68.4 dB for an effective number of bits of 11.07 bits. The FFT plot is shown if Fig. 11. The supply voltages are 1.8V. The power consumption of the analog and digital powers are respectively 2.56mW and 3.13mW for a total of 5.69mW. The figure of merit is 75.6 fJ/conversion-step. The results are summarized in Table Apx.5.1.

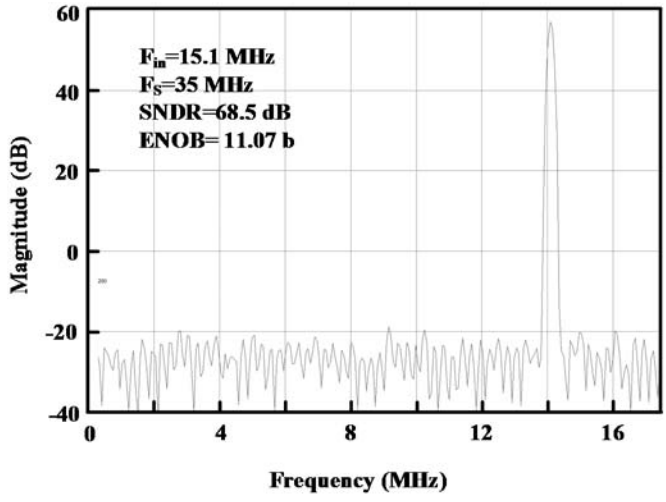


Fig. Apx.5.2 FFT plot of the simulated data with Nyquist input at a sampling frequency of 35 MHz.

Table. Apx.5.1 Performance summary of the proposed SAR ADC using threshold-configuring comparator.

Parameter	Value
Supply voltage	1.8V
Technology	0.18 ㎛ 1P4M CMOS
Resolution	12-bit
Sampling frequency	35 MS/s
Input range	Differential 1.6 V_{P-P}
Input frequency	15.1 MHz
SNDR	68.4 dB
ENOB	11.07 bits
FoM	75.6 fJ/conv.step
Power consumption	5.69mW
Area	560um x 380um

Some comparisons have been made with prior works which have been implemented using the length process of 0.18 um technology. This is shown in Table Apx.5.2. Also, to make more comparisons in the similar operation bandwidth region, Table Apx.5.3 makes comparisons with more prior works. It can be seen that with simulation results, the proposed TCC is the best performing SAR ADC designed in the same length process of 0.18 um.

Table. Apx.5.2 Performance comparison with prior works designed with same 0.18 um technology.

	ASSCC '07	JSSC '07	JSSC '07	ISSCC '08	ASSCC '09	SOVC '10	JSSC '11	CICC '11	ESSCIRC '11
Resolution [bits]	10	12	8	10	10	10	10	10	10
Sampling Freq. [MS/s]	1	0.1	0.2	0.1	0.5	10	0.1	0.001	1
ENOB [bits]	8.2	10.55	7.58	9.4	9.4	9.83	9.3	8.52	8.38
FoM [fJ/conv.-step]	374	167	65	56	124	11	21	6.8	21.56
Power [mW]	0.11	0.025	0.00247	0.0038	0.042	0.098	0.0013	0.00025	0.00716
	TCAS-II '11	**JSSC '12**	**JSSC '12**	**ISCAS '12**	**NEWCAS '13***	**AICSP '13**	**MIEL '14***	**TCAS-II '14**	**TCAS-I '15**	**This Work***
Resolution [bits]	10	10	10	10	12	12	8	10	10	12
Sampling Freq. [MS/s]	0.08	1	0.768	0.5	0.2	0.2	20	0.11	2	**35**
ENOB [bits]	8	9.18	9.83	9.24	10.6	11.13	6.88	9.03	9.07	**11.07**
FoM [fJ/conv.-step]	19.5	9.11	74	47	4.87	220	1002	20	20.6	75.6
Power [mW]	0.0004	0.0053	0.058	0.014	0.00149	0.947	2.36	0.00116	0.02212	5.69

* Simulation-based results

Table. Apx.5.3 Performance comparison with prior works designed with similar operation bandwidth.

	ASSCC '09	SOVC '09	JSSC '10	ASSCC '11	JSSC '11	JSSC '11	ISOCC '14	JSSC '10	ASSCC '11	JSSC '15
Resolution [bits]	10	12	10	10	12	10	10	10	11	13
Technology [nm]	130	130	130	130	130	130	130	90	90	90
Freq. [MS/s]	12	11	50	40	45	40	20	100	25	50
ENOB [bits]	8.16	10.17	9.18	7.92	10.85	8.11	9.56	9.1	9.5	11.17
FoM [fJ/conv.-step]	95	311	29	117	36.7	50	41	77	38.8	36.5
Power [mW]	0.32	0.97	0.826	1.15	2.82	0.55	0.62	3	0.58	4.2
	ISSCC '10	**BioCAS '10**	**CICC '12**	**CICC '13**	**JSSC '14**	**JSSC '14**	**ISSCC '15**	**SOVC '14**	**JSSC '15**	**This Work**
Resolution [bits]	10	10	10	11	12	11	14	15	10	12
Technology [nm]	65	65	65	65	65	40	40	28	28	**180**
Freq. [MS/s]	100	50	220	95	80	40	35	100	240	35 MS/s
ENOB [bits]	9.51	9.1	8.3	10.2	9.38	8.98	12.1	11.5	8.51	11.07
FoM [fJ/conv.-step]	15.5	29.7	63	22	111.3	73	355	25.9	7.8	75.6
Power [mW]	1.13	0.82	4.3	1.36	5.91	1.45	54.5	8	0.68	5.69

APX.5.4. CONCLUSIONS

The prototype of the SAR ADC using a threshold-configuring comparator for ultrasound imaging system applications was presented. By using the TCC, the operation bandwidth could be raised to over 35 MHz in the simulations, so that it could potentially replace the power-hungry pipeline ADCs of the analog front-end receivers. Simulation results are positive, showing a resolution of ENOB of 11.07 bits at 35 MS/s. When simulation results are compared to prior works designed with the same length process of 0.18 um, this work is superior.

Although the work on the use of TCC in the SAR ADC is incomplete yet, it shows potential in improving the bandwidth of the operation of the SAR ADC. Moreover, it is a novel structure, and many ideas have been implemented in the design of the circuit.

BIBLIOGRAPHY

[1.1.1] M. Mota, "Scalable Architectures for Analog IP on Advanced Process Nodes," *Synopsis Insight Letter*, Issue 3, 2013.

[2.3.1] Y. Zhu, C.-H. Chan, U.-F. Chio, S.-W. Sin, "A 10-bit 100-MS/s Reference-Free SAR ADC in 90 nm CMOS" *IEEE JSSC*, vol. 45, no. 6, pp. 1111–1121, 2010.

[2.3.2] A. M. Abo, P. R. Gray, "A 1.5-V, 10-bit, 14.3-MS/s CMOS pipeline analog-to-digital converter" *IEEE JSSC*, vol. 34, no. 5, pp. 599–606, 1999.

[2.3.3] A. H. Chang, H.-S. Lee, D. S. Boning, "Redundancy in SAR ADCs" *Proceeding GLSVLSI*, pp. 283–288, 2011.

[2.3.4] J. J. Kang, M. P. Flynn, "A 12b 11MS/s successive approximation ADC with two comparators in 0.13 um CMOS" *Symposium on VLSI Circuits*, pp. 240–241, 2009.

[2.3.5] D. Schinkel, et al. "A Double-tail Latch-type Voltage Sense Amplifier with 18ps Setup+Hold Time" *IEEE ISSCC*, pp. 314–605, 2007.

[2.5.1] T. Ogawa, H. Kobayashi, M. Hotta, Y. Takahashi, S. Hao, and N. Takai, "SAR ADC algorithm with redundancy," *IEEE APCCAS*, pp. 268-271, Nov. 2008.

[2.5.2] F. Kuttner, "A 1.2V 10b 20MSample/s non-binary successive approximation ADC in 0.13 um CMOS," *IEEE ISSCC*, pp. 176-177, 2002.

[2.5.3] R. Kapusta, J. Shen, S. Decker, H. Li, E. Ibaragi, H. Zhu, "A 14b 80 MS/s SAR ADC With 73.6dB SNDR in 65 nm CMOS," *IEEE JSSC*, vol. 48, no. 12, Aug. 2013.

[2.5.4] M. Yoshioka, et. al, “A 10-b 50-MS/s 820-uW SAR ADC With On-Chip Digital Calibration” *IEEE Trans. BioCaS*, vol. 4, no. 6, pp. 410–416, 2010.

[2.5.5] W. Liu, P. Huang, Y. Chiu, “A 12-bit, 45-MS/s, 3-mW Redundant Successive-Approximation-Register Analog-to-Digital Converter With Digital Calibration” *IEEE JSSC*, vol. 46, no. 11, pp. 2661–2672, 2011.

[2.5.6] R. Vitek, E. Gordon, S. Maerkovich, A. Beidas, “A 0.015mm^2 63fJ/conversion-step 10-bit 220MS/s SAR ADC with 1.5b/step redundancy and digital metastabitily correction,” *IEEE Custom Integrated Circuits Conference*, pp. 1-4, Sep. 2012.

[2.5.7] P. Harpe, E. Cantatore, A. van Roermund, “A 2.2/2.7fJ/conversion-step 10/12b 40kS/s SAr ADC with Data-Driven Noise Reduction,” *IEEE ISSCC*, pp. 270-271, Sep. 2013.

[3.3.1] Y. Zuh, C.-H. Chan, U.-F Chio, S.-W. Sin, S.-P. U, R. P. Martins, and F. Maloberti, “Split-SAR ADCs: Improved Linearity With Power and Speed Optimization,” *IEEE Transactions on Very Large Scale Integration Systems*, vol. 22, no. 2, Feb. 2014.

[4.2.1] Infineon, TC1796 datasheet

[4.3.1] L. Deng et al., “A 12-bit 200KS/s SAR ADC with a Mixed Switching Scheme and Integer-Based Split Capacitor Array,” *IEEE NEWCAS*, pp. 1-4, Jun. 2013.

[4.3.2] Y. Chen, X. Zhu, H. Tamura, M. Kibune, Y. Tomita, T. Hamada, M. Yoshioka, K. Ishikawa, T. Takayama, J. Ogawa, S. Tsukamoto, and T. Kuroda, “Split Capacitor DAC Mismatch Calibration in Successive Approximation ADC,” *IEEE Custom Integrated Circuits Conf.*, Sep. 2009, pp. 279-282.

[4.3.3] J.-Y. Um, Y.-J. Kim, E.-W. Song, J.-Y. Sim, and H.-J. Park, “A Digital-Domain Calibration of Split-Capacitor DAC for a Differential SAR ADC Without Additional Analog Circuits,” *IEEE Trans. Circuits and Systems – I: Regular Papers*, vol. 60, no. 11, pp. 2845-2856, Nov. 2013.

[4.3.4] W. Guo, and S. Mirabbasi, “A Low-Power 10-bit 50-MS/s SAR ADC Using

a Parasitic-Compensated Split-Capacitor DAC," *IEEE Int. Symp. Circuits and Systems*, May 2012, pp. 1275-1278.

[Apx.2.1] R. Reeder and C. Petersen, "The AD9271 - a revolutionary solution for portable ultrasound," *Analog Dialogue* 41–07, Jul. 2007.

[Apx.2.2] B. A. J. Angelsen, H. Torp, S. Holm, K. Kristoffersen, and T. A. Whittingham, "Which transducer array is best?" *Eur. J. Ultrasound*, vol. 2, no. 2, pp. 151–164, 1995.

[Apx.2.3] H. Huang and D. Paramo, "Broadband electrical impedance matching for piezoelectric ultrasound transducers," *IEEE Trans. Ultrason. Ferroelectr. Freq. Control*, vol. 58, no. 12, pp. 2699–2707, Dec. 2011.

[Apx.2.4] E. Brunner, "Ultrasound system considerations and their impact on front-end components," *Analog Dialogue, Analog Devices Inc.*, vol. 36, no. 3, 2002.

[Apx.2.5] Texas Instruments, "Fully Integrated, 8-Channel Ultrasound Analog Front End With Passive CW Mixer, 0.75 nV/rtHz, 14/12-Bit, 65 MSPS, 153 mW/CH," AFE5808 datasheet, Sep. 2010 [Revised Jan. 2014.]

[Apx.3.1] C. Nani, C. Armiento, A. Sangiovanni-Vincentelli, J. Craninckx, G. Van der Plas, "A 6-Bit 50-MS/s Threshold Configuring SAR ADC in 90-nm Digital CMOS," *IEEE Transactions on Circuits and Systems I*, vol. 59, no. 1, pp. 80-92, Jul. 2011.

[Apx.3.2] K. Yoshioka, A. Shikata, R. Sekimoto, T. Kuroda, H. Ishikuro, "An 8 bit 0.3-0.8 V 0.2-40 MS/s 2-bit/Step SAR ADC With Successively Activated Threshold Configuring Comparators in 40 nm CMOS," *IEEE Transactions on Very Large Scale Integration Systems*, vol. 23, no. 2, pp. 356-368, Feb. 2014.

[Apx.3.3] G. Van der Plas, B. Verbruggen, "A 150MS/s 133uW 7b ADC in 90nm digital CMOS Using a Comparator-Based Asynchronous Binary-Search sub-ADC," *IEEE International Solid-State Circuits Conference*, pp. 242-610, Feb. 2008.